Fechas importantes 2^{do} cuatrimestre 2019:

- Exámen:
  - Primer parcial - 17/10
  - Primer recuperatorio - 07/11
  - Segundo recuperatorio - 12/12
- Trabajos Prácticos:
  - Presentación TP0 - 22/08
  - Entrega TP0 -
  - Presentación TP1 - 05/09
  - Entrega TP1 -
  - Presentación TP2 - 26/09
  - Entrega TP2 -
  - Presentación TP3 - 31/10
  - Entrega TP3 -

Semana	Temas	Lecturas	Ejercicios
01 - 22/08	Rég. cursada, Tools, Amdahl, TP0	ch.1 [1]	1.1 1.2 1.3
02 - 29/08	Ec. de desempeño, ABI, MIPS	ch.1 [1]	
03 - 05/09	ISA, Ejs ABI, TP1	ch.2 [1]	
04 - 12/09	Assembly, ABI		
05 - 19/09	Memoria cache	ch.5 [1]	
06 - 26/09	Memoria cache, TP2		
07 - 03/10	Memoria virtual	ch.5 [1] Sec. 3 y 4 [6]	
08 - 10/10	Memoria virtual	[6] ch.5 [1] [3] [4]	
09 - 17/10	Exámen parcial		
10 - 24/10	Datapath, resolución ex. parcial		
11 - 31/10	Pipeline, Hazards, TP3		
12 - 07/11	1^{er} recup.		
13 - 14/11	Predictores salto, pipeline FP, desempeño		
14 - 21/11	Presentaciones TP		
15 - 28/11	Presentaciones TP		
16 - 05/12	Presentaciones TP		
17 - 12/12	2^{do} recup.		

Lecturas

[1] David Patterson, John Hennessy, *Computer Architecture a Quantitative Approach*, Elsevier, 3rd edition. ISBN: 1-55860-596-7. May 2002.

[2] David Patterson, John Hennessy, *Computer Organization and Design, the Hardware/Software Interface*, Elsevier, 3rd edition. ISBN: 1-55860-604-1. Aug. 2004.

[3] B.L. Jacob and T.N. Mudge, *Virtual Memory: Issues of Implementation*, Computer, Vol. 31, No. 6, June 1998, pp. 33-43.

[4] B.L. Jacob and T.N. Mudge, *Virtual Memory in Contemporary Microprocessors*, IEEE Micro, Aug. 1998.

[5] Jean-Loup Baer, *Microprocessor Architecture. From Simple Pipelines to Chip Multiprocessors*, Cambridge University Press. ISBN-13 978-0-521-76992-1. 2010

[6] Ulrich Dreper, *What every programmer should know about memory*

[7] Rajeev Balasubramonian and Norman P. Jouppi and Naveen Muralimanohar, *Multi-Core Cache Hierarchies*, Morgan and Claypool Publishers, 2011.

[8] System V Application Binary Interface, MIPS RISC Processor, 3rd Edition, The Santa Cruz Operation, February 1996 (http://www.sco.com/developers/devspecs/mipsabi.pdf).