

Fechas importantes 1^{er} cuatrimestre 2019:

■ Exámen:

- Primer parcial - 23/5
- Primer recuperatorio - 13/6
- Segundo recuperatorio - 04/7

■ Trabajos Prácticos:

- Presentación TP1 - 11/4
- Entrega TP1 - 25/4
- Presentación TP2 - 30/5
- Entrega TP2 - 20/6

| Semana | Temas | Lecturas | Ejercicios |
|-----------|--|---------------------|---------------------|
| 01 - 14/3 | Herramientas, Ley de Amdahl | ch.1 [1] | 1.1 1.3 |
| 02 - 21/3 | Ley de Amdahl, Ecuación de desempeño, MIPS | ch.1 [1] | 1.2 1.4 |
| 03 - 28/3 | ISA | ch.2 [1] | 2.1 2.2 2.3 |
| 04 - 04/4 | Assembly, ABI | Ap.A [1] [8] | |
| 05 - 11/4 | Memoria cache | ch.5 [1] | 3.3 3.4 3.5 3.6 3.8 |
| 06 - 18/4 | | | |
| 07 - 25/4 | Memoria cache | ch.5 [1] Sec. 3 [6] | 3.18 3.19 3.20 |
| 08 - 02/5 | Memoria virtual | ch.5 [1] Sec. 4 [6] | 3.9 3.11 3.12 3.15 |
| 09 - 09/5 | Memoria virtual | ch.5 [1] [3] [4] | 3.1 3.2 |
| 10 - 16/5 | Simil parcial | | |
| 11 - 23/5 | Exámen parcial | | |
| 12 - 30/5 | Data path | ch.4 [2] | |
| 13 - 06/6 | Pipeline | App. A [1] | |
| 14 - 13/6 | 1 ^{er} recup. | | |
| 15 - 20/6 | | | |
| 16 - 27/6 | Pipeline | App. A [1] | |
| 17 - 04/7 | 2 ^{do} recup. | | |

Lecturas

- [1] David Patterson, John Hennessy, *Computer Architecture a Quantitative Approach*, Elsevier, 3rd edition. ISBN: 1-55860-596-7. May 2002.
- [2] David Patterson, John Hennessy, *Computer Organization and Design, the Hardware/Software Interface*, Elsevier, 3rd edition. ISBN: 1-55860-604-1. Aug. 2004.
- [3] B.L. Jacob and T.N. Mudge, *Virtual Memory: Issues of Implementation*, Computer, Vol. 31, No. 6, June 1998, pp. 33-43.
- [4] B.L. Jacob and T.N. Mudge, *Virtual Memory in Contemporary Microprocessors*, IEEE Micro, Aug. 1998.
- [5] Jean-Loup Baer, *Microprocessor Architecture. From Simple Pipelines to Chip Multiprocessors*, Cambridge University Press. ISBN-13 978-0-521-76992-1. 2010

- [6] Ulrich Dreper, *What every programmer should know about memory*
- [7] Rajeev Balasubramonian and Norman P. Jouppi and Naveen Muralimanohar, *Multi-Core Cache Hierarchies*, Morgan and Claypool Publishers, 2011.
- [8] System V Application Binary Interface, MIPS RISC Processor, 3rd Edition, The Santa Cruz Operation, February 1996 (<http://www.sco.com/developers/devspecs/mipsabi.pdf>).