

Large-scale integration of wavelength-addressable all-optical memories on a photonic crystal chip

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Photonic integration has long been pursued, but remains immature compared with electronics. Nanophotonics is expected to change this situation. However, despite the recent success of nanophotonic devices, there has been no demonstration of large-scale integration. Here, we describe the large-scale and dense integration of optical memories in a photonic crystal chip. To achieve this, we introduce a wavelength-addressable serial integration scheme using a simple cavity-optimization rule. We fully exploit the wavelength-division-multiplexing capability, which is the most important advantage of photonics over electronics, and achieve an extremely large wavelength-channel density. This is the first demonstration of the large-scale photonic integration of nanophotonic devices coupled to waveguides in a single chip, and also the first dense wavelength-division-multiplexing nanophotonic devices other than filters. This work paves the way for optical random-access memories and for a large-scale wavelength-division-multiplexing photonic network-on-chip.

Photonic integration has long been studied, but its degree of integration is still very limited compared with electronic integration where billions of transistors can now be integrated on a single chip. Photonic devices are generally unsuitable for large-scale integration because of their large footprint, high power consumption and poor integrability. However, the demand for large-scale photonic integration has recently been increasing because it is anticipated that it will be possible to reduce the energy consumption and heat generation of processor chips with the introduction of optical

communication on a chip, in other words, a photonic network-on-chip architecture^{1,2}. To install a sophisticated photonic network on a chip, various photonic functions (wavelength-division multiplexing (WDM), switching networks and photonic routing) implemented by integrated nanophotonic technologies will be required. In this regard, nanophotonics is very important, especially for use in high-quality-factor (Q) nanocavities, because the power consumption can be dramatically reduced as a result of enhanced light–matter interactions³. Indeed, there have been a number of

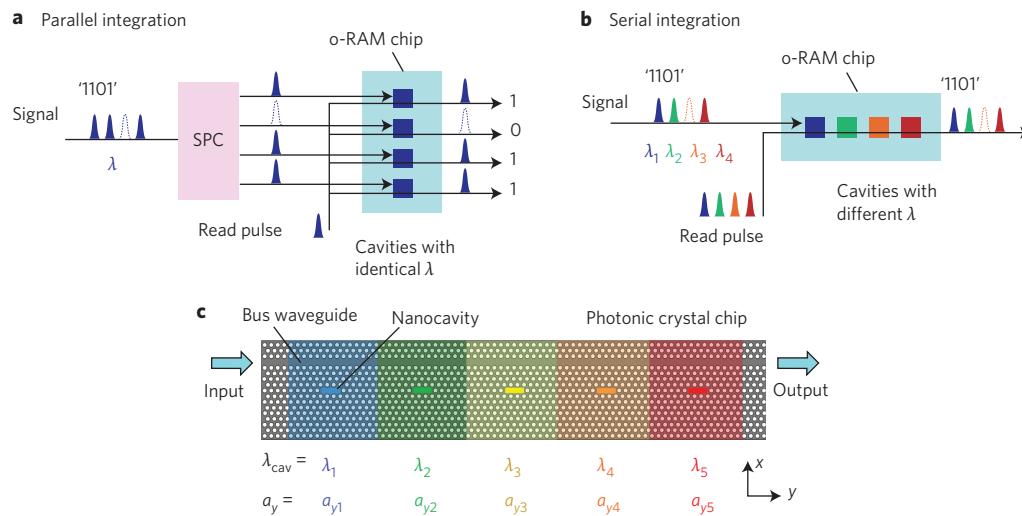


Figure 1 | Designs of integrated multi-bit optical memory (o-RAM) arrays. **a**, Parallel integration: multiple bistable cavities with the same resonant wavelength are integrated in parallel on a single chip. Input signal information is spatially decoded by a serial-to-parallel converter (SPC) and stored in each cavity. The stored information is retrieved by injecting a set of read pulses. **b**, Serial integration: multiple bistable cavities with different resonant wavelengths are integrated serially and coupled with the same bus waveguide on a single chip. Input WDM signal information is stored in each cavity with the corresponding wavelength channel. The stored information is retrieved by injecting a set of read pulses. **c**, Proposed design of nanocavity-based serially integrated o-RAMs on a photonic crystal chip. The resonant wavelength of a nanocavity (λ_{cav}) is varied by locally modulating the lattice constant a of the photonic crystal in the y -direction (parallel to the waveguide).

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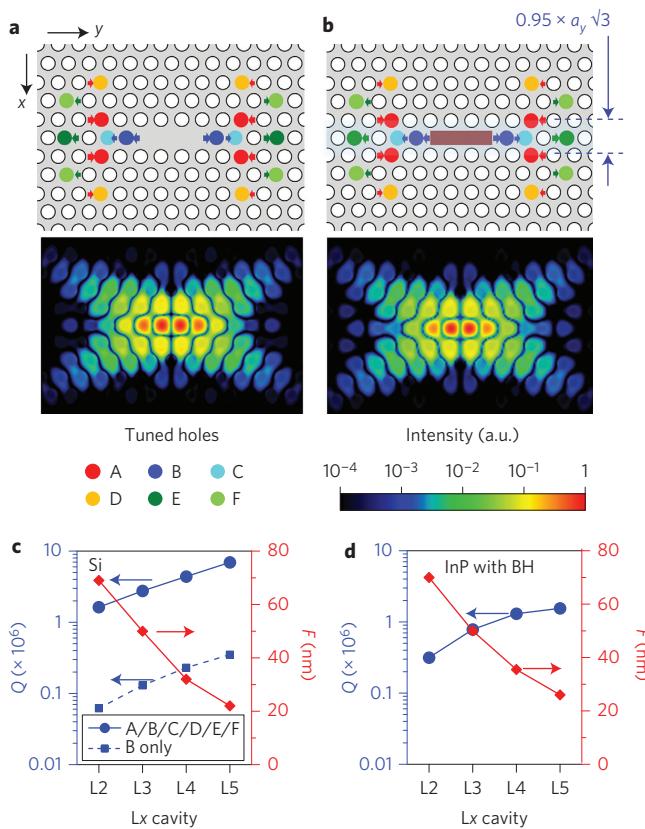


Figure 2 | Modified Lx ($x \approx 2-5$) nanocavity design and characteristics.

a,b, Structural design (top) and magnetic field (H_z) intensity distribution (bottom) of the modified L3 cavity in a Si photonic crystal (**a**) and an InGaAsP/InP BH photonic crystal (**b**). shift(A) = s_1 , shift(B) = s_2 , shift(C) = $s_2/2$, shift(D) = $s_1/2$, shift(E) = s_3 and shift(F) = $s_3/2$. **c**, Q and F of modified Lx cavities in Si photonic crystals ($x \approx 2-5$; membrane thickness = 215 nm; $a = 408$ nm; $r = 100$ nm). **d**, Q and F of modified Lx cavities in InGaAsP/InP BH photonic crystals ($x \approx 2-5$; membrane thickness = 245 nm; $a = 434$ nm; $r = 100$ nm; BH dimensions = 300 nm \times 145 nm \times $3a$).

Calculations were performed with our home-made three-dimensional finite-difference time-domain (FDTD) simulation code^{9,13,18}. The size of the calculation area was 27 and 37 hole rows for the x - and y -directions and the mesh sizes were $a/24$ (Si) and $a/14$ (InP-BH), respectively. (For more details see Supplementary Information, Chapter 1).

leading-edge studies that have reported various functional devices, such as lasers^{4,5}, detectors⁶⁻⁸, switches^{3,9}, modulators¹⁰ and memories¹¹⁻¹³, which were realized by employing nanophotonic platforms including photonic crystals and plasmonics. However, these previous demonstrations were limited to the operation of one or a few devices¹³ or simple coupled cavity waveguides^{14,15}. In addition, it is particularly important to demonstrate chip-scale WDM capability, as this is the most significant advantage of photonics over electronics. In terms of photonic integration in general, a fairly large scale of integration has already been achieved in image sensors or phased arrays¹⁶. However, these are designed for free-space optics and are not directly applicable to on-chip photonic networks, which need a planar circuit configuration (that is, the elements should be interconnected by in-plane waveguides).

Here, we demonstrate the large-scale integration of wavelength-addressable optical bit memories. Our device (Fig. 1c) is integrated into a photonic crystal chip, where high-Q nanocavities with a wide mode spacing and different resonant wavelengths are coupled to a common bus waveguide. This structure realizes bistable memory operation with a very small footprint and low energy consumption because of the enhanced optical nonlinearity in its nanocavities.

This result is achieved by a simple nanocavity optimization rule and precise nanophotonic integration technology. In this configuration, we fully exploit the WDM capability to address each memory bit independently by selecting its wavelength. The total power consumption for 28-bit memories is estimated to be less than 150 μ W. This is the first demonstration of the large-scale photonic integration of nanophotonic devices on a single chip in a planar circuit configuration (other than devices for free-space optics), and also the first to implement the WDM function in dynamic nanophotonic devices (other than static devices such as filters or couplers). Optical random access memories (RAMs) are desired for various types of optical processing, including network routing. However, RAMs are considered difficult to realize using photonics because they require a large number of integrated memories (approximately kilobyte capacity) and extremely small power consumption. The present result reveals the great potential of using photonic crystal nanocavities for large-scale all-optical RAMs, which are expected to play an important role in future photonic networks-on-chip.

Design

We have already reported the successful demonstration of four-bit all-optical memories based on photonic crystal nanocavities (Fig. 1a), in which four identical cavities are integrated in parallel with different waveguides separated at intervals of 50 μ m (ref. 13). As is generally observed in a nonlinear resonator, the intensity of the light output via the cavity exhibits bistability and hysteresis as a function of the input light intensity, because of optical nonlinearity. Accordingly, when there is a constant bias input, we can switch between two bistable states by injecting a set/reset pulse, which functions as a memory. Each bit is independently addressed using an all-optical switching addresser. As reported in detail in our previous reports¹³, the four-bit all-optical memories perform very well. However, this parallel integration is hard to extend to a very large scale because the bit number is limited by the performance of the all-optical addresser. Another possible form of integration is shown in Fig. 1b, where nanocavities with different resonant wavelengths are integrated in a serial fashion and coupled to a single bus waveguide (serial integration). For this cascaded configuration, we can fully exploit the WDM capability and each bit can be addressed by choosing its operating wavelength. Because all the cavities can share a common waveguide, the packing density can be increased. In future, we may combine these two types of integration into a matrix form to realize a very large-scale array of memories. Our present aim is to demonstrate the large-scale integration of all-optical memories in a serial configuration.

Here, we examine a concrete design for serial integration in photonic crystals (Fig. 1c). Although the cavities are end-coupled to the waveguide^{17,18} in a parallel integration¹³, the cavities in the serial integration should be side-coupled to form a cascade. Generally, the bistable switching contrast is smaller in the side-coupling configuration than in the end-coupling configuration. This means that serial integration requires a higher Q to achieve sufficient memory operation. Wavelength addressability is simply achieved by varying the lattice constant in each unit consisting of a cavity and a waveguide¹⁹ (Fig. 1c).

For this serial integration design, nanocavities should satisfy the following two requirements. First, they should have a high loaded Q with large cavity-waveguide coupling, which is necessary for high-contrast bistable switching. Second, they should have a large cavity-mode spacing between the fundamental and first higher-order modes (free spectrum range, F). To guarantee independent addressability, no cavity mode should overlap with other modes (see Supplementary Information, Chapter 1). Thus, F limits the total bandwidth and subsequently limits the total number of bits. Note that these two requirements are difficult to satisfy in nanocavities

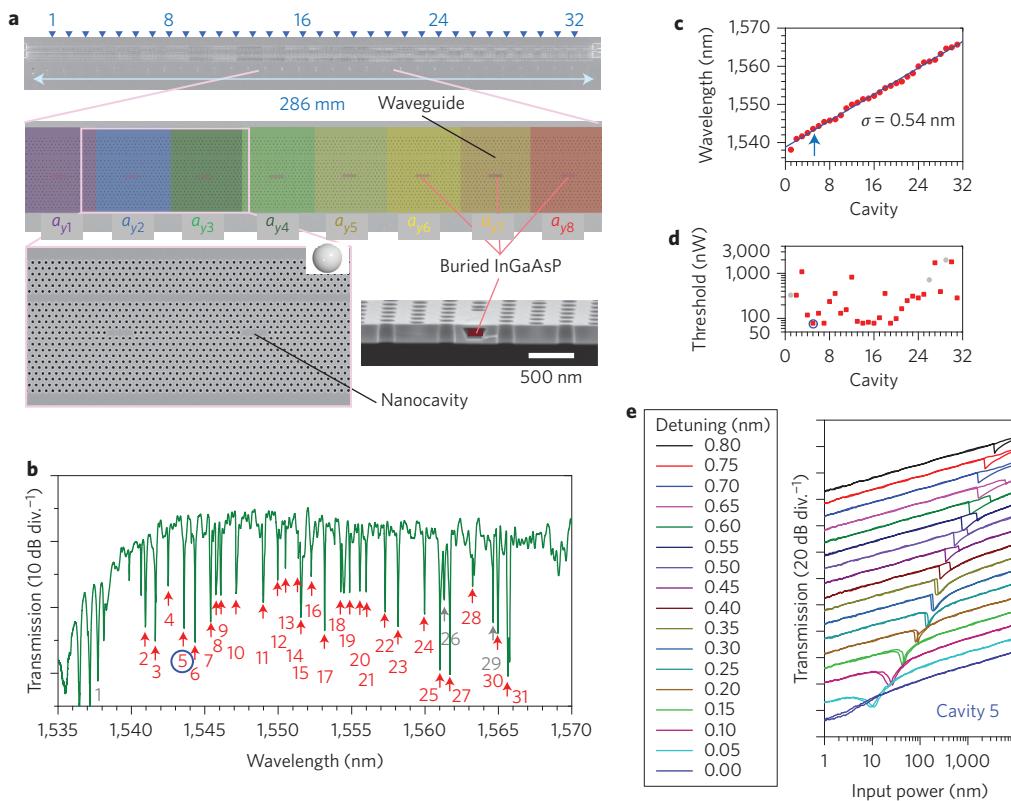


Figure 3 | Thirty-two cascaded integrated InGaAsP/InP BH nanocavities and their bistable operation. **a**, Scanning electron microscopy (SEM) images with different magnifications. The lattice constant a_y of each cavity is monotonically varied between 420 and 435.5 nm in 0.5 nm steps, arranged with a spacing of $20a$ ($\sim 8.5 \mu\text{m}$). a_x is fixed at $420 \times \sqrt{3} \text{ nm}$. An InGaAsP BH structure is embedded in the centre of every cavity. **b**, Transmission spectrum via the output port; 31 dips are confirmed to correspond to different cavities. The 28 cavity modes marked in red are operated as o-RAMs in Fig. 4. **c**, Wavelengths for the 31 dips. The blue line is a fitted line and σ is the standard deviation of the residuals from the fitted line. **d**, The threshold power of the bistability of the 31 cavities. **e**, Output intensity versus input intensity for various wavelength detunings δ for cavity 5. Clear hysteresis is observed, which is proof of bistable operation. The detuning δ is the wavelength difference between the incident c.w. light and the original resonant peak (at 1,542.80 nm, the slight wavelength difference from **b** is due to the temperature variation).

other than photonic crystal nanocavities, such as whispering-gallery-mode cavities²⁰. In our previous optical RAMs¹³ we used modulated mode-gap cavities^{18,21}, which have a fairly high Q but relatively small F . In addition, the cavity-mode profile is extended in the waveguide direction, which is unsuitable for serial integration. In contrast, L3 cavities, which are in-line three-point defects with end-hole shifting²², have a large F and a compact mode profile, but their intrinsic Q is too small. L4 or L5 cavities have slightly higher Q values but their F values are too small (Fig. 2).

To meet these requirements, we adopted the optimized cavity design shown in Fig. 2a. In conventional L3 cavities, only two holes (denoted ‘B’), are shifted to optimize the cavity Q . In the present design, we shift other holes (denoted ‘A’ to ‘F’) to further optimize Q . Similar modifications of L3 cavities by adjusting multiple holes have already been reported²³, where the optimum modifications were determined step by step after extensive trial-and-error computations^{24,25}. Here, we adopt an empirical model for optimization in which the shifts of six different holes have a simple relationship ($s_1 = -\text{shift}(\text{'A}') = -2 \text{ shift}(\text{'D}')$, $s_2 = \text{shift}(\text{'B}') = 2 \text{ shift}(\text{'C}')$, $s_3 = \text{shift}(\text{'E}') = 2 \text{ shift}(\text{'F}')$) expressed using only three parameters (s_1, s_2, s_3). We found empirically that this simple rule generally leads to fast optimization. The optimization enhances the theoretical Q nearly ten times (1.4 million) without changing the effective mode volume ($V_{\text{eff}} \approx 0.08 \mu\text{m}^3$) and F (49 nm), as shown in Fig. 2c and Supplementary Table 1. In this study, we also investigate InGaAsP/InP buried-heterostructure (BH) photonic crystals in which an ultrasmall InGaAsP region is embedded in the cavity as

an optical nonlinear medium¹³. In our previous studies^{5,13,26} we used a similar BH design for modulated mode-gap cavities²⁰, but here we investigate a BH design for L3 cavities as shown in Fig. 2b. The BH structure leads to efficient carrier confinement and enhanced heat escape (detailed features of the BH structure have been described elsewhere²⁶). Although the presence of the BH region strongly affects the index profile of the L3 cavity, we found that we can adopt the same optimization rule. As shown in Fig. 2d, we observed a one order of magnitude improvement in BH design for Q (0.4 million) with V_{eff} and $\Delta\lambda$ unchanged (Supplementary Table 1).

Results

We fabricated the 32 serially integrated nanocavities according to the design in Fig. 2b in InGaAsP/InP BH photonic crystals (Fig. 3a). Details of the design are described in the Methods. The transmission spectrum (Fig. 3b) monitored via bus waveguides reveals distinctive multiple dips. The spectrum contains more dips than cavities. We confirmed that some of them are due to Fabry-Pérot modes that do not exhibit optical nonlinearity, and 31 correspond to the fundamental cavity resonance at a different cavity. The higher-order mode is not observed in this spectrum range. Note that the dips are deep enough ($> 10 \text{ dB}$) for bistable operation. Although a few dips are close to each other, most are also sufficiently separated. The average wavelength spacing is 0.9 nm, which corresponds to an average WDM channel density of $\sim 100 \text{ GHz}$. The loaded Q of these resonances is $\sim 1 \times 10^4$, and the estimated unloaded Q is $\sim 5 \times 10^4$. Figure 3c summarizes the wavelengths of all the dips in

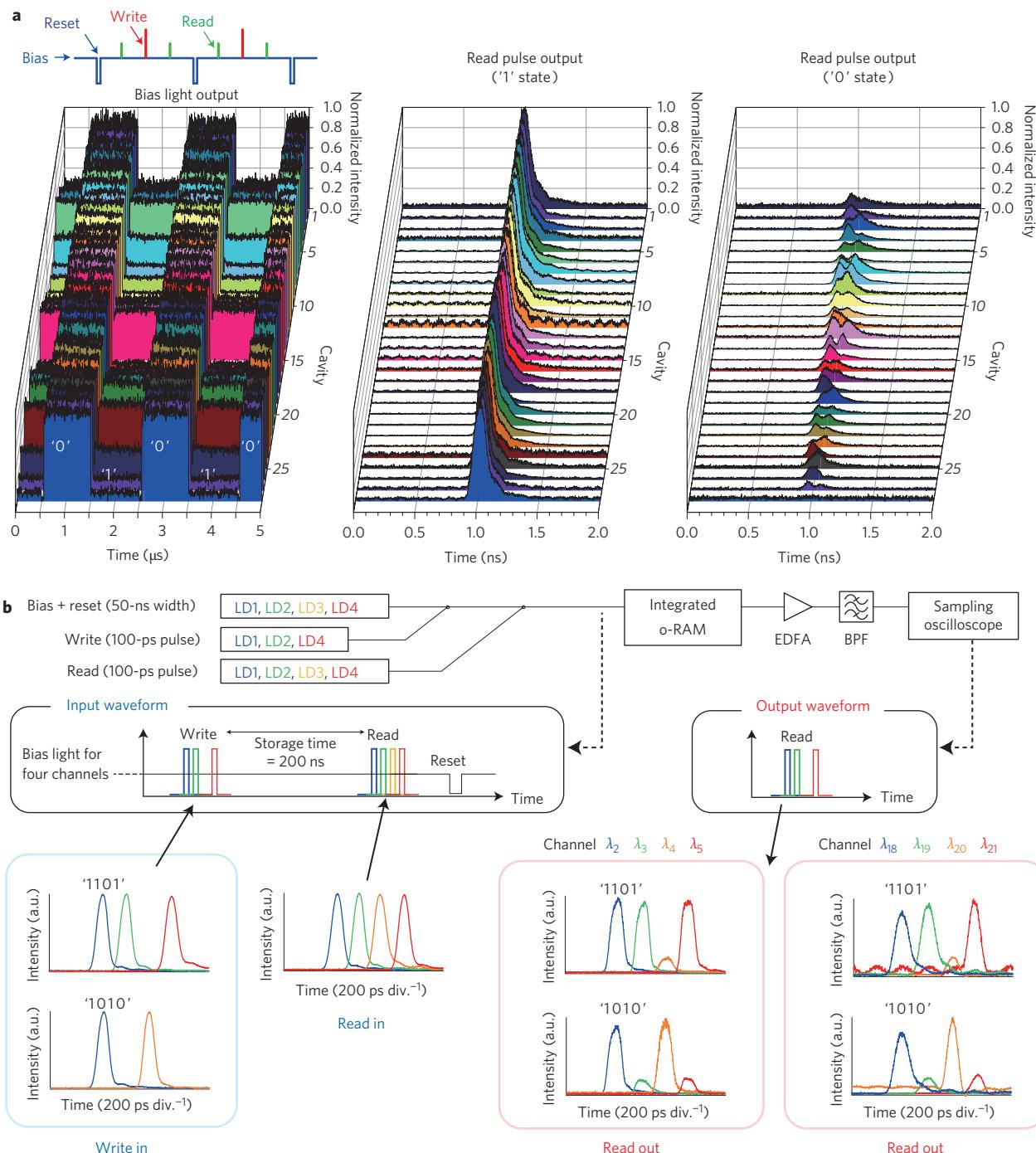


Figure 4 | Demonstration of 28-bit write/readout bit-memory operation in an InGaAsP/InP BH nanocavity array. **a**, Channel-by-channel memory operation of 28 bits. Left: output waveforms of 28 channels for the bias light output, showing the stored information. Those memories were operated by injected bias light with reset, write and read pulses. A simplified bias input waveform corresponding to the output waveforms (bottom) is shown on top. (See Supplementary Information, Chapter 3, for details) The bias light wavelengths for all channels are provided in Supplementary Table 2. Middle and right: Output waveforms of 28 channels for the read pulse at '1' (middle) and '0' (right). Note that the '0' ('1') state corresponds to high (low) output for the bias light, and low (high) output for the read pulse. This difference is attributed to the different detuning condition for the bias and read pulses. **b**, Simultaneous operation of four bits. Top: measurement set-up (LD, laser light source with modulator; EDFA, erbium-doped fibre amplifier; BPF, band-pass filter.) Two sets of four sequential channels ($\{\lambda_2, \lambda_3, \lambda_4, \lambda_5\}$ and $\{\lambda_{18}, \lambda_{19}, \lambda_{20}, \lambda_{21}\}$) are chosen from the 28 channels. The input waveforms consist of the bias light with negative reset pulses, write pulses and read pulses. The write pulses are composed of four-bit light pulse signals with different wavelengths. Two types of write pulses ('1101' and '1010') are injected in the experiment. The output waveforms show the four-bit readout information for both sets of channels. The stored information is successfully read out in all cases. (See Supplementary Information, Chapter 4, for more details.)

the same device. The standard deviation of the dip wavelength residual from the linear relation, σ , is 0.54 nm. The total bandwidth is ~ 25 nm.

We investigated the input power dependence of all the dips, and observed clear optical bistability for 31 of them. Figure 3e shows the transmitted output power as a function of input power under

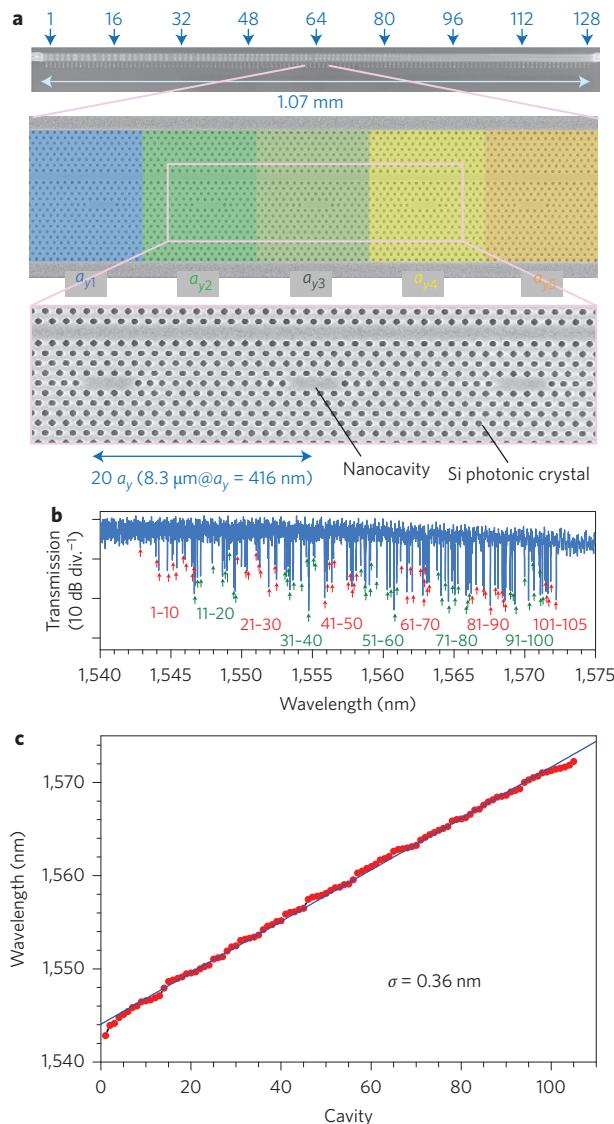


Figure 5 | Cascaded integrated 128-Si-nanocavity array. **a**, SEM images of the fabricated 128-nanocavity array with a periodicity of $20a_y$ at different magnifications. The lattice constant a_y of each cavity is systematically varied between 408 and 423.875 nm ($\Delta a_y = 0.125$ nm). a_x was fixed at $408 \times \sqrt{3}$ nm. **b**, Transmission spectrum via the output port; 105 dips are confirmed to correspond to different cavities. **c**, Wavelengths for the 105 dips. The blue line is a fitted line and σ is the standard deviation of the residuals from the fitted line.

various detuning conditions for one of the dips (fifth dip in Fig. 3b). The curve shows a clear hysteresis when the input light is detuned to a shorter wavelength than the dip, which is a signature of bistable operation based on optical nonlinearity via photoexcited carriers^{9,13,17}. In this case the threshold power, given by the onset of bistability with clear hysteresis, is 79 nW. The power is defined as the light intensity in the bus waveguide. The bistable thresholds for all the dips are shown in Fig. 3d, and range from 79 nW to 2 μ W. The total sum of the bistable threshold power for all dips is ~ 13 μ W.

We next examined channel-by-channel bit-memory operation (Fig. 4a). We observed successful bit-memory operation for 28 dips out of 32 cavities. In the experiment each memory was initially in one of the bistable states (denoted ‘0’). We then injected a write pulse that switched the memory to the other state, ‘1’ (Write).

This state (and therefore the stored bit information) is maintained until the bias light is blocked (Reset). As long as the bit information is stored, we can read it out with arbitrary timing by injecting a read pulse (Read). The left panel in Fig. 4a shows the output waveform of the bias light slightly blue-detuned from cavity resonance, and shows the state of each memory. The centre and right panels show the output waveforms of the read pulse for two cases (with and without write pulse injection, that is, with ‘1’ and ‘0’ information stored) for which the wavelength is on-resonance with the cavity (zero detuning). Because the side-coupling configuration is used, the low and high power states in the lower left panel correspond to ‘1’ and ‘0’, respectively, which is the opposite of previous reports^{2,13} where the cavity was in an end-coupling configuration. As expected, when the write pulse is injected ‘1’ is retrieved, and when there is no write pulse, ‘0’ is retrieved for all channels. For this operation, the bias power was between 1.6 and 7.9 μ W, and the write/read pulse energy was 100–200 fJ. This result clearly shows that we have achieved 28-bit memory operation. The total power consumption for 28 bits in Fig. 4a is 137 μ W.

To demonstrate that this 28-bit memory can operate as a multi-bit RAM and that different bits can be addressed simultaneously, we simultaneously injected a four-bit signal and examined the RAM operation (Fig. 4b). Two sets of four sequential channels (dips 2–5 and dips 18–21) were chosen from the 28 channels. Write pulses were composed of four-bit light pulse signals with different wavelengths. In the experiment, two types of write pulse ('1101' and '1010') were injected. The two sets of readout waveforms for both sets of channels demonstrate that the stored information was successfully read out in all cases. With the two different dip sets, the results clearly show that different memories can be accessed independently and simultaneously without noticeable crosstalk or mutual interference. This is the first demonstration of wavelength-addressable multi-bit RAM. For more details about the experiments in Fig. 4a,b, see the Methods and Supplementary Information, Chapters 3 and 4.

With the present device, the number of bits is limited by three factors: the available bandwidth, the cavity-resonance width and the wavelength accuracy. To demonstrate the greatest degree of integration we next fabricated similar integrated memories (design shown in Fig. 1d) using Si photonic crystals, because they are superior to InGaAsP/InP BH photonic crystals in terms of the last two factors. In fact, the modified L3 cavity design with Si photonic crystals leads to a maximum measured Q of ~ 1 million, which is an order of magnitude greater than that in InGaAsP/InP BH photonic crystals. We fabricated 128 cavity devices (Fig. 5a) with a_y varied in 0.125 nm steps, as described in the legend of Fig. 5.

Figure 5b shows the transmission spectrum of the fabricated device. A total of 115 dips (except for Fabry-Pérot modes) related to the fundamental nanocavity mode are resolved, and the total bandwidth is 30 nm. The dips are 10–20 dB deep, and the average intrinsic Q for the dips is about 0.5 million. Figure 5c summarizes the wavelengths for all the dips in the same device (σ is 0.36 nm). The values of Q and σ are significantly improved compared to those of the InGaAsP/InP devices. The average wavelength spacing is 0.23 nm, corresponding to an average WDM channel density of 30 GHz. We examined the input power dependence, and 105 dips exhibited clear optical nonlinearity¹⁷ without overlapping with other cavity modes.

We next investigated bistable memory operation with this Si device and examined how many bits could be operated (Fig. 6). The procedure shown in Fig. 6a is essentially the same as for the InGaAsP/InP devices. Figure 6b shows the temporal waveform of the bias light output for 105 channels, revealing the instantaneous state of the optical memory. Each memory was initially in the ‘0’ state and, after a write pulse was injected, the state switched to the ‘1’ state until the reset operation. This result shows that bistable

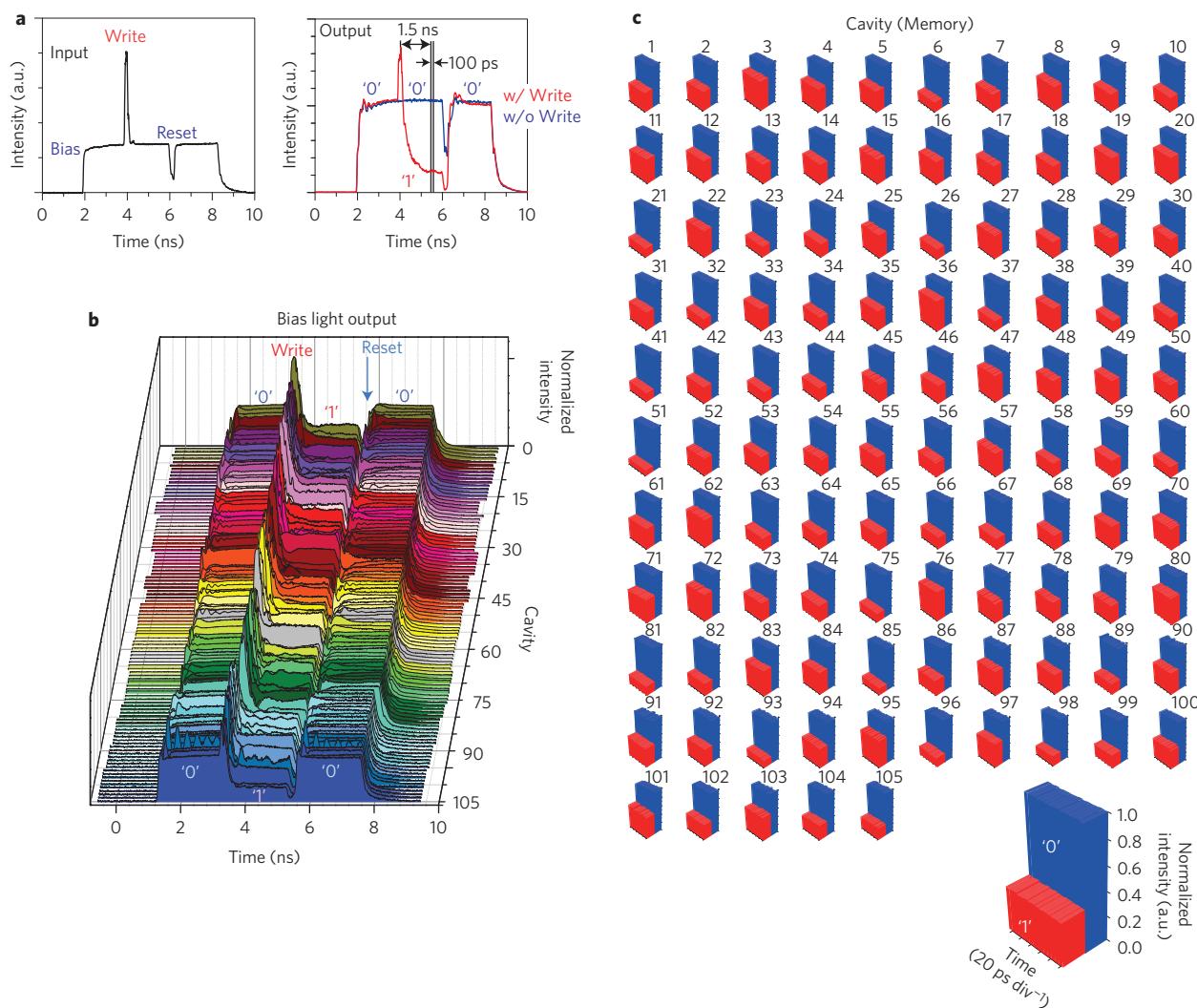


Figure 6 | Bistable 105-bit memory operation of integrated Si nanocavities. **a**, Left: input waveform consisting of the bias light with a negative reset pulse, a write pulse and a read pulse. Right: output waveforms for cavity i ($i \approx 1-105$) with (red) and without (blue) a write pulse input. The period of 100 ps indicated by a pair of arrows shows the fixed time window used for clipping snapshots. **b**, Temporal waveforms of the bias light output of all 105 operational channels, showing the stored information ('0' and '1'). The intensity is normalized at the '0' level. The peak appearing between '0' and '1' corresponds to the direct output of the input write pulse, which was not visible in Fig. 4a because of the long sampling time. The bias light wavelengths for all channels are shown in Supplementary Table 3. **c**, Snapshots for the bias light output clipped for a fixed 100 ps time window with (red) and without (blue) a write pulse. The binary contrast in 105 bit memories shows the stored information (either '1' or '0').

memory operation is achieved for 105 bits in this chip. The bias power for this operation was in the range 79–400 μ W. The memory time was limited to less than 10 ns, similar to our previous Si-based memories¹⁷. To visualize the memory operation for 105 bits, Fig. 6c shows snapshots with (red bars) and without (blue bars) the write pulse for all operating bits, which are clipped for the fixed 100 ps time window shown in Fig. 6a. The observed clear binary contrast shows that all 105 bits successfully memorized the '1' and '0' information. Although the operating power is greater than that for InGaAsP/InP memories, we have demonstrated the larger degree of memory integration due to the high fabrication accuracy in Si.

Summary and outlook

We have successfully demonstrated wavelength-addressable integrated optical memories, achieved by the serial integration of high-Q nanocavities in a photonic crystal chip. We have achieved 28-bit and 105-bit memory operation in InGaAsP/InP BH and Si photonic crystals, respectively. This is the first realization of

large-scale integrated dynamic nanophotonic devices other than static wavelength filter devices^{27,28}. The present result has clearly revealed the capacity of nanophotonics for dense integration. Because current progress in photonic integrated circuits will soon be limited by the large footprint and high power consumption of conventional photonic devices, our result represents an important step towards future fully fledged photonic integration.

The present form of the WDM function is widely applicable, and we can realize other devices (such as lasers, detectors and switches) with a WDM function employing the present cascaded cavity design. Although there are obviously a number of problems to be solved, such as improving the wavelength controllability, our result paves the way for the nanophotonic WDM elements that will be a key ingredient of future integrated nanophotonic circuits. Note that when we introduce the WDM into a chip, the area per wavelength channel should be as small as possible because the area cost will be critical. Our present result corresponds to $\sim 20 \mu\text{m}^2$ per 30 GHz. The inverse product of the footprint area and bandwidth represents the channel density (the number of channels in a given

area). In our case, this product is equal to $\sim 2 \times 10^3$ (1/GHz mm²), which is much larger than that for conventional WDM devices. This number literally indicates the order of a million channels within a 1 mm² area in the C band (~ 8 THz).

With respect to WDM implementation, one problem to be overcome is finding a way to cope with the wavelength variation for each cavity resonance. The results in Figs 3 and 5 show that the wavelength steps are not equidistant; this was caused by fabrication error (hole radii, hole shape, slab thickness, BH size and so on) introduced during electron-beam writing, etching and crystal growth processes. Although the error is decreasing year by year as processes are improved, it will be very important to introduce technologies to tune finite wavelength variations. At the time of writing, it is still an open question whether such tuning is feasible, but here we point out several possible solutions. With memories, the simplest solution is to adjust the bias power, because we can change the operation wavelength by altering this power (which is accompanied by a slight additional power consumption). To find the optimum bias condition, the device should be scanned only once when it is installed on a chip. We might also rely on one of the various nanocavity post-tuning processes that have already been studied extensively^{29–32}. In addition, we would like to emphasize that any sophisticated chip-scale WDM network may require flexible bit-scale wavelength converters with low energy consumption. We believe that such devices will be realized by nanophotonics and solve the wavelength variation problem.

Finally, we discuss the outlook for multi-bit memory applications. In networks, memories are generally required as a buffer for the routing process. At present, electronic RAMs are widely used in commercial networks, but the use of optical RAMs will be feasible because they are more suitable for high-bit-rate data packets due to the fact that optical memories do not require power-consuming O/E and E/O conversions and can directly store high-bit-rate (10–40 Gbps) data. This is also the case with the chip-scale network. On-chip electric routers have already been installed in many-core processors to handle chip-scale networks, and we believe that on-chip optical routers will be needed when the bit rate increases. We anticipate that optical RAMs will be applied under these circumstances. As noted earlier in this Article, it has been predicted that kilobyte optical RAMs will be needed for photonic routing. We believe that the most promising way to realize this scale of optical RAM is to employ a matrix of integrated memories achieved by combining the present WDM serial integration scheme with parallel integration. Finally, we note that the present memories can also be used for devices other than RAMs, such as a wavelength-selective bistable switch array, which can open/close a specific WDM channel by switching between two bistable states. Moreover, the serial integration of bistable elements will be vital for the construction of integrated optical logic.

Methods

Device preparation. All the photonic crystal patterns in the samples were defined by electron-beam lithography. The electron beam writer had a high acceleration voltage of 100 kV and the minimum step of the position setting was 0.125 nm; the latter met the requirement of 0.125 nm step modulation of a in the Si cavity array. ZEP-520 (ZEON) positive-tone electron-beam resist was used. With both Si- and InP-based photonic crystals, inductively coupled plasma dry-etching machines were used to transfer the pattern onto the slab layer. Silicon-on-insulator substrates were used for Si photonic crystal fabrication, and the top device Si layer was 200 nm thick. The silicon oxide layer immediately beneath the photonic crystal pattern was wet-etched by buffered hydrogen fluoride acid to form an air-bridge structure. As shown in the Supplementary Information, Chapter 2, setting $s_1:s_2:s_3 = 0.050a, 0.290a, 0.030a$ realized a loaded Q of 9×10^5 for an L3 cavity with $a = 408$ nm and with an air-hole radius r of 95 nm. The cavity wavelength range of the Si 128 L3 cavity array (for parameters, see legend of Fig. 5) immediately after fabrication was 1,567–1,596 nm. Thermal oxidation at 900 °C was used to shift the range to the C + L telecommunication band (1,543–1,572 nm), as shown in Fig. 6b, which degraded the intrinsic Q of the cavity from 9×10^5 to 5×10^5 .

To fabricate the InP photonic crystals we first grew an InGaAs sacrificial layer and an active region including a 145-nm-thick InGaAsP layer with a 1.45 μm photoluminescence peak on an InP substrate¹¹. The parameters of the photonic crystal and BH L3 cavity array are described in the legends of Figs 2 and 3. The empirical tuning realized a loaded Q of 4.5×10^4 ($s_1:s_2:s_3 = 0.060a, 0.330a, 0$) where $a = 426$ nm and $r = 100$ nm.

Details of memory operation experiments. The detailed experimental set-up is provided in Supplementary Fig. 2. To acquire the individual memory operation shown in Fig. 4a, we adjusted the wavelength and energy of the input light for each memory channel. The average wavelength detunings from the original resonant wavelength for the bias light, write pulse and read pulse were -0.6 to -0.4 , -0.2 to -0.1 , and -0.1 to 0 nm, respectively. All the light inputs were obtained by modulating the continuous-wave (c.w.) light with a lithium niobate modulator, where the pulse widths for both write and read pulses were 100 ps, and the reset pulse was 50 ns. The spectral linewidths of the bias light and two pulses were <100 kHz (the laser source itself) and 8.2 GHz, respectively. The average pulse energies for the write and read pulses were 100–200 and 30–50 fJ, respectively. The bias power was between 1.6 and 7.9 μW. These light inputs were coupled into a single fibre and were injected into the sample, with the reset pulse applied 1 μs after the write pulse, and the read pulse injected 500 ns after each write and reset pulse. The output read pulse trains were observed by using a sampling oscilloscope with an erbium-doped fibre amplifier and a band-pass filter.

To demonstrate WDM operation of a multi-bit RAM where four different bits can be addressed simultaneously (as shown in Fig. 4b), we injected multi-wavelength light into the chip. We chose the sequential resonant channel sets of $\{\lambda_2, \lambda_3, \lambda_4, \lambda_5\}$ and $\{\lambda_{18}, \lambda_{19}, \lambda_{20}, \lambda_{21}\}$, where the subscripts indicate the cavity mode number. Four laser sources were used to generate a bias light with a 50-ns-wide reset pulse, and four other laser sources were also used for write pulses with widths of 100 ps. A read pulse train consisting of all four channels with a pulse width of 100 ps was also generated and provided 200 ns after the write pulses. The bias power, write pulse energy and read pulse energy were 6.5–13 μW, 160–270 fJ and 50–70 fJ, respectively. All were coupled and injected into the photonic crystal memories. See Supplementary Information, Chapter 4, for details.

For Si nanocavity memory operation, we input a waveform as shown in Fig. 6a. To suppress device heating, a rectangular pulse with a width of 6 ns was used as a bias light. The bias light wavelengths for all 105 cavities are provided in Supplementary Table 3. The bias power was 79–400 μW, which is nearly two orders of magnitude higher than that of the InP-based BH cavities, as a result of poor carrier plasma nonlinearity. The energy and width of the write pulse were 80–800 fJ and 200 ps, respectively. A reset pulse with a width of 250 ps was applied 2 ns after the write pulse.

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Author contributions

M.N. planned the project. E.K., A.S., K.N. and M.N. designed the device. E.K. designed the cavity and performed the numerical simulations. E.K. and K.T. prepared the pattern data. E.K. and H.S. fabricated the Si samples. K.T., T.S., S.M. and E.K. fabricated the InP-based samples. K.N. and E.K. performed measurements. E.K. and M.N. wrote the manuscript.

Additional information

Supplementary information is available in the online version of the paper. Reprints and permissions information is available online at www.nature.com/reprints. Correspondence and requests for materials should be addressed to E.K. and M.N.

Competing financial interests

The authors declare no competing financial interests.