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departamento de eletrónica,
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ESPRESSIF ESP32-DEVKITC

Architecture and Hardware aspects

Part 1

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Definition

ESP32 is a series of low-cost, low-power microcontrollers. It is also a system-on-chip with integrated microcontroller, Wi-Fi, Bluetooth and includes an integrated RF antenna.

COMPONENTS

1 Micro USB port

2 Boot Button

3 EN Button

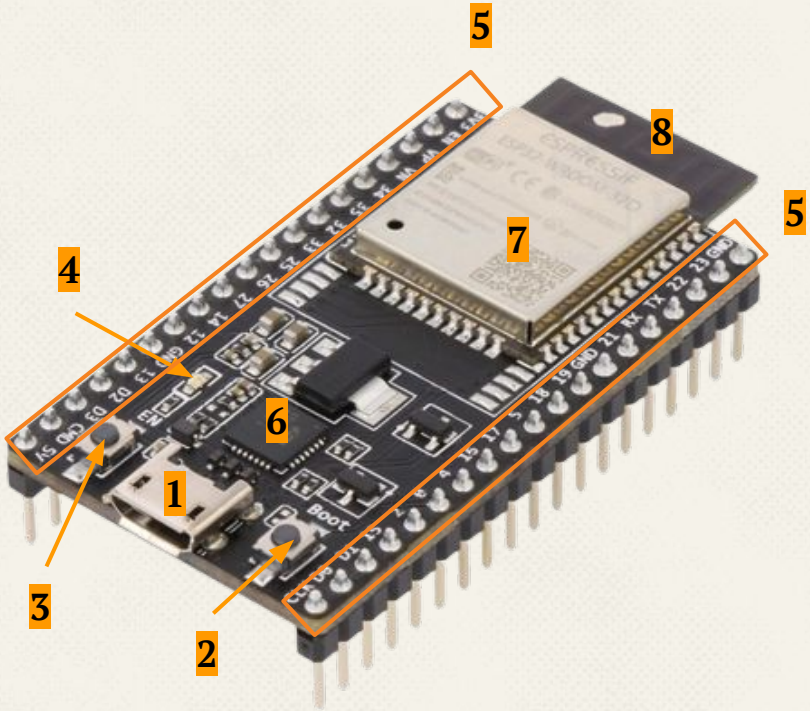
4 5V Power On LED

5 I/O

6 USB-to-UART Bridge

7 ESP32-WROOM-32 processor

8 Antenna



Specifications

Processor

Dual or single-Core 32-bit LX6 microprocessors, which runs up to 600 DMIPS with 2 cores:

- Protocol CPU (PRO_CPU) - WiFi, Bluetooth and other internal peripherals
- Application CPU (APP_CPU) - application code
- Ultra low power co-processor: allows you to do ADC conversions, computation, and level thresholds while in deep sleep
- Has Real Time Clock

Wireless connectivity

Wi-Fi: 802.11 b/g/n/ (bit rate: 802.11n up to 150 Mbps)

Bluetooth: v4.2 BR/EDR and BLE

Antenna Options

ESP32-WROOM-32E: On-board PCB antenna or ESP32-WROOM-32UE: external antenna via a connector.

Specifications

Internal Memory

448 KBytes ROM (booting and core functions), 520 KBytes on-chip SRAM (data and instruction),

16 KBytes SRAM in RTC (8 KBytes - slow memory and 8 KBytes - fast memory) - used for boot, deep-sleep mode, eFuse (dynamic reprogramming of chips in real time) and 13 modules of DMA operations.

External Memory (Parts of the embedded memory can be used as transparent cache for this external memory)

- Supports up to 16 MB off-Chip SPI Flash.
- Supports up to 8 MB off-Chip SPI SRAM.

Peripherals

SD card, UART, SPI, SDIO, I2C, PWM, Motor PWM, I2S, IR, pulse counter, GPIO, capacitive touch sensor, ADC, DAC, TWAI, CAN.

Power Supply

- **USB**
- **Unregulated power to GND and 5V pins**
  - Using unregulated voltage between 5V and 12V, connected to the 5V and GND pins. This voltage is regulated on-board.
- **Regulated power to GND and 3.3V pins**
  - Using regulated 3.3V voltage, connected to the 3.3V and GND pins.

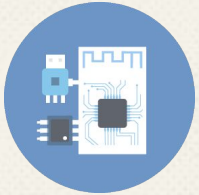
Key Features

Wi-Fi and Bluetooth Connectivity

Integrates Wi-Fi and Bluetooth functions.

Rapid Prototyping

Achieves optimal RF performance.



Flexible and Feature-Rich

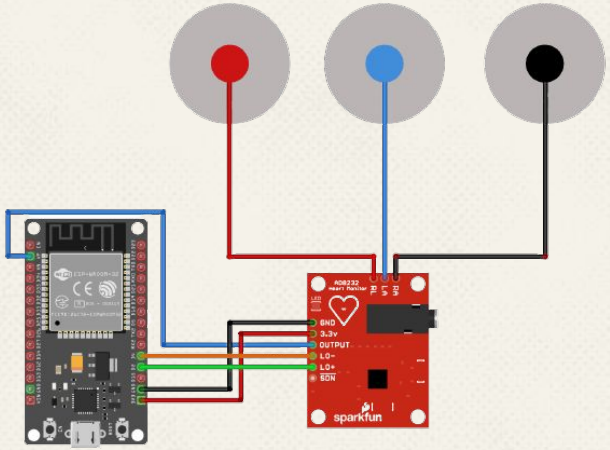
Contains the entire support circuitry of ESP32-WROOM, ESP32-WROVER and ESP32-SOLO series of modules.

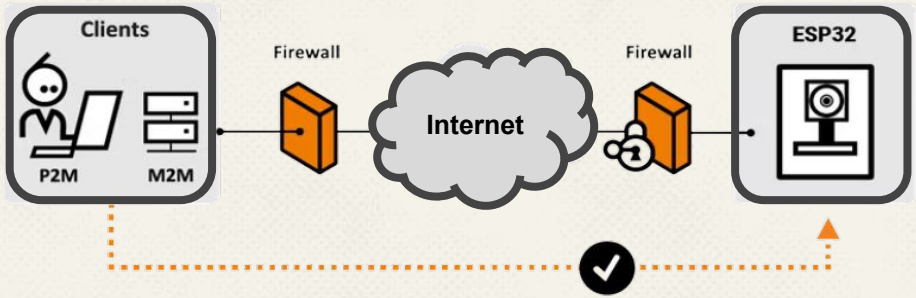
Breadboard Friendly

The ESP32-DevKitC pinout is optimized to enable prototyping on a breadboard.

Preferred Applications

- Networking
- Data Processing
- P2P Connectivity
- Web Server
- Smart industrial devices
- Smart medical devices
- Smart energy devices
- Smart security devices



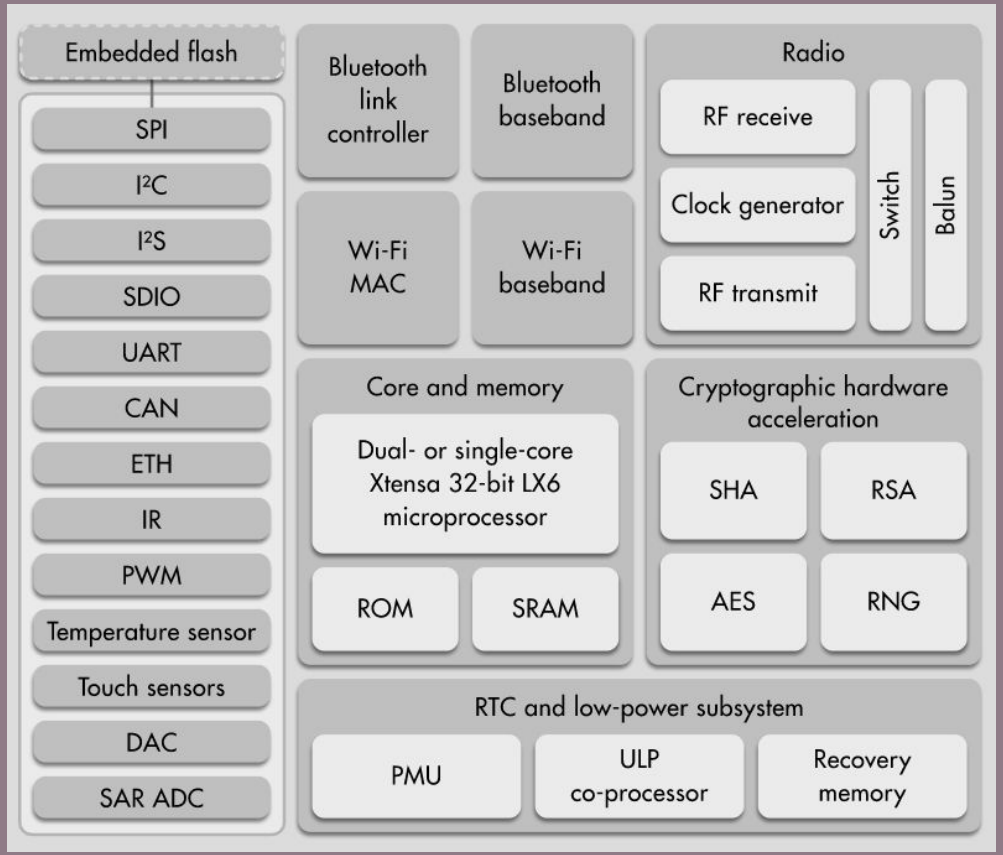


Block diagram

Peripherals and Sensors

- GPIO, UART, SPI, I2C, I2S, PWM, DAC, ADC, CAN, Temperature and Touch Sensors

Cryptographic hardware acceleration is the use of hardware to perform cryptographic operations faster than they can be performed in software.

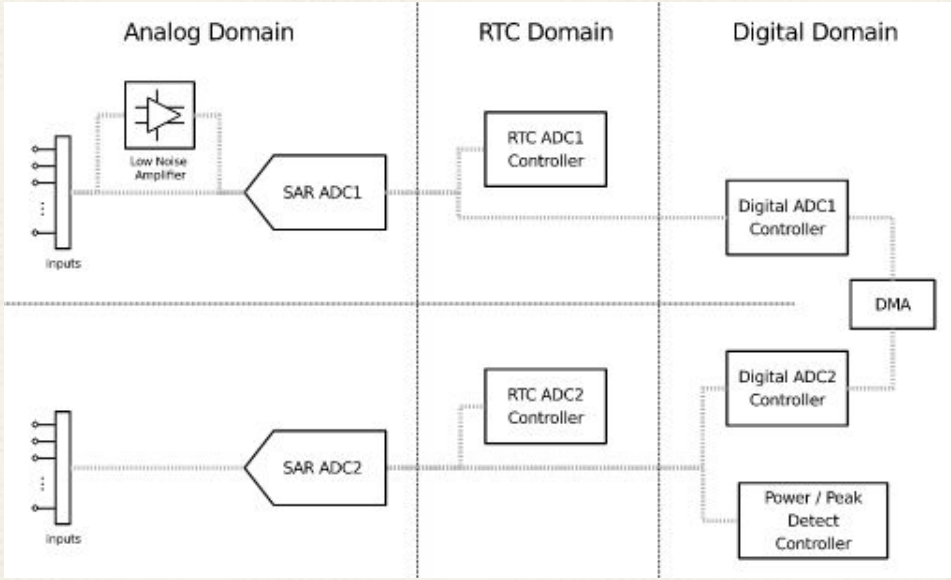


ADC Introduction

- An ADC is an electronic circuit that’s usually integrated into different microcontrollers or comes in as a dedicated integrated circuit. An ADC is used to measure/read the analog voltage from different sources or sensors.
- Most parameters are analog and the electronic sensors used to capture this information are also analog. Just like temperature, light, pressure, and more other sensors are all analog.
- Goal: read the analog voltage value using digital microcontrollers. Convert the input analog voltage to a digital value.
- The ESP32 integrates 12-bit 2 SAR ADCs, supporting a total of 18 analog pads. Each ADC operate in multiple modes to achieve certain design goals (high-performance or low-power consumption).

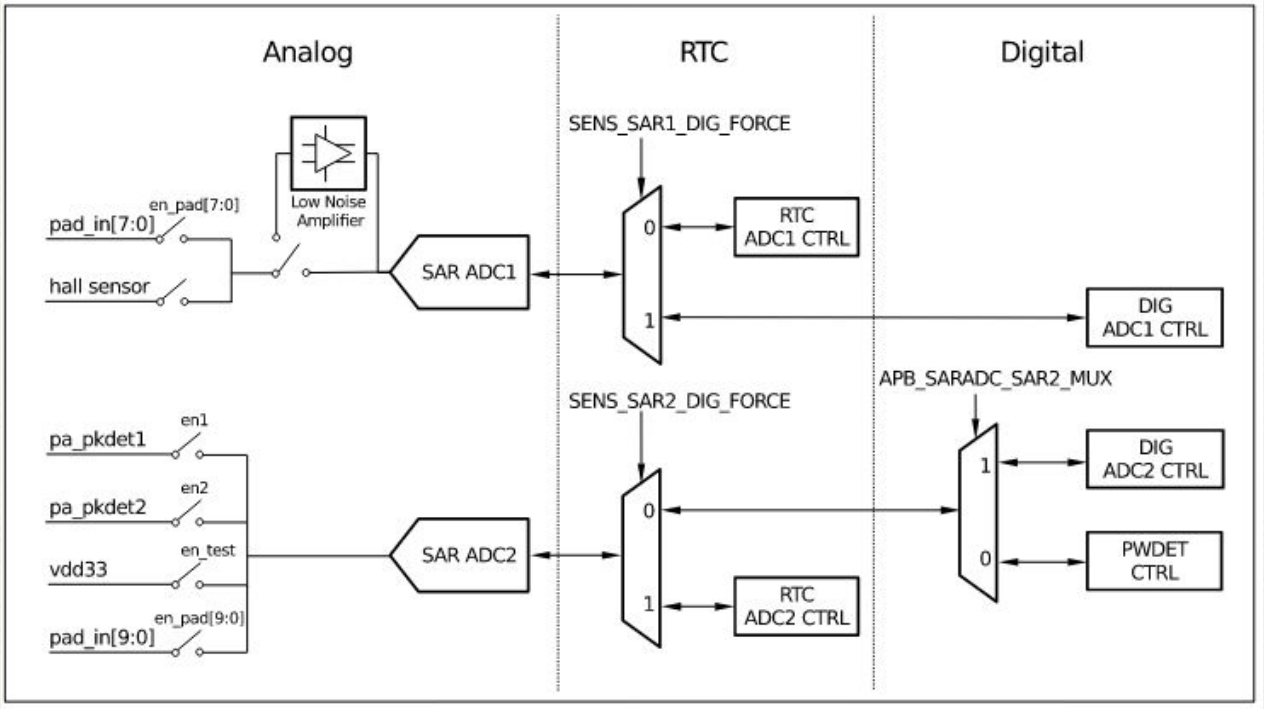
SAR ADC Depiction

- Each ADC unit supports two work modes, **ADC-RTC** or **ADC-DMA** mode.
- ADC-RTC is controlled by the **RTC controller** and is suitable for low-frequency sampling operations.
- ADC-DMA is controlled by a **digital controller** and is suitable for high-frequency continuous sampling actions.



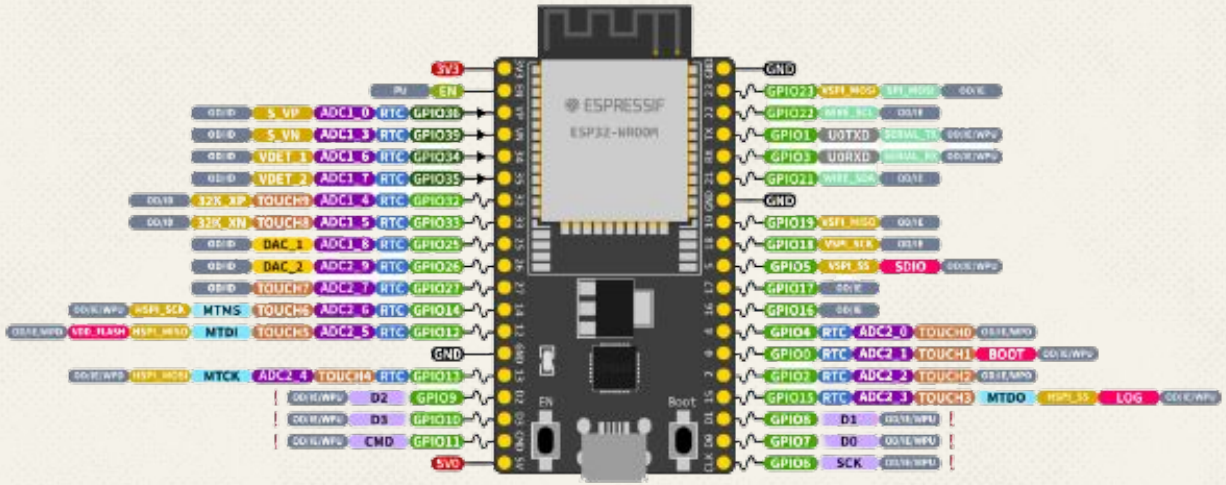
SAR ADC Outline of Function

- The SAR ADC module's major components, and their interconnections.



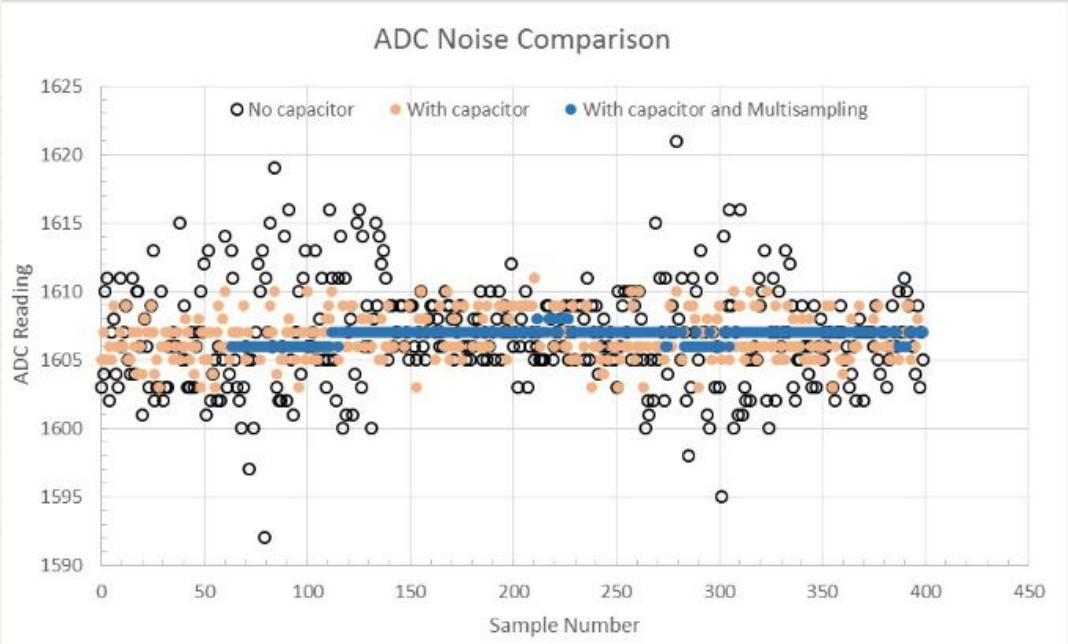
ADC Channels

- Channel ADC1:
  - 8 channels: GPIO32 - GPIO39
- Channel ADC2:
  - 10 channels: GPIO0, GPIO2, GPIO4, GPIO12 - GPIO15, GOIO25 - GPIO27
- ADC in ESP32 have a maximum resolution of 12-bits although, the resolution of ADC is configurable with possible values include 9-bit, 10-bit, 11-bit and 12-bit.



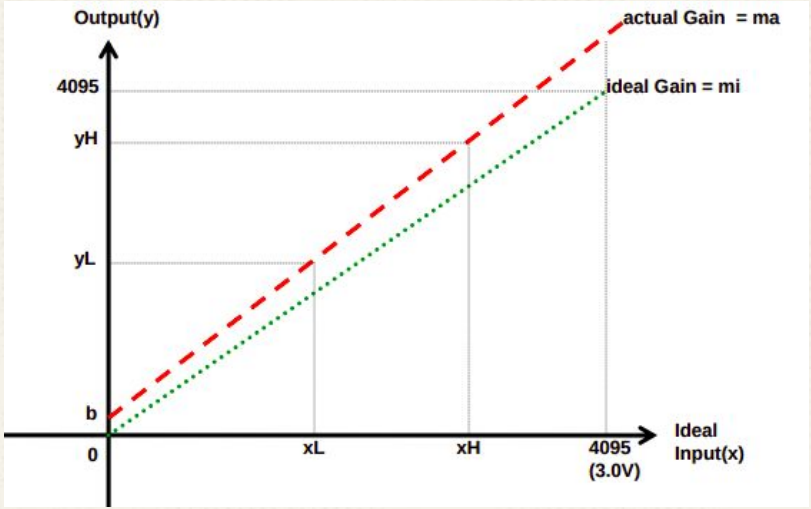
Minimizing Noise

- The ESP32 ADC can be sensitive to noise leading to large discrepancies in ADC readings.
- Users may connect a bypass capacitor.
- Multisampling may also be used.



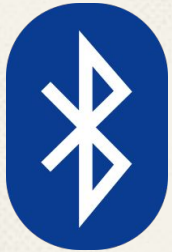
ADC Calibration

- Calibration is performed by feeding two known reference values into two ADC channels and calculating a calibration gain and offset to compensate the input readings from the other channels.
- Calibration values are used to generate characteristic curves that account for the variation of ADC reference voltage of a particular ESP32 chip. There are currently 3 source(s) of calibration values.
  - **Two Point:** represent each of the ADC readings at 150 mV and 850 mV.
  - **eFuse Vref:** represents the true reference voltage of the ADC.
  - **Default Vref:** is an estimate of the ADC reference voltage provided by the user as a parameter during characterization.



Bluetooth and Wi-Fi

- The chip integrates a Bluetooth link controller and Bluetooth baseband, which carry out the baseband protocols and other low-level link routines, such as modulation/demodulation, packet processing, bit stream processing and frequency hopping.



- ESP32 implements TCP/IP, full 802.11 MAC protocol, and Wi-Fi Direct specification.
- Wifi-Direct is good option for peer-to-peer connection without the need of an access point.
- Data transfer speeds are much better than bluetooth.

Radio

The radio module consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- bias and regulators
- balun and transmit-receive switch
- clock generator

RTC and low-power Subsystem

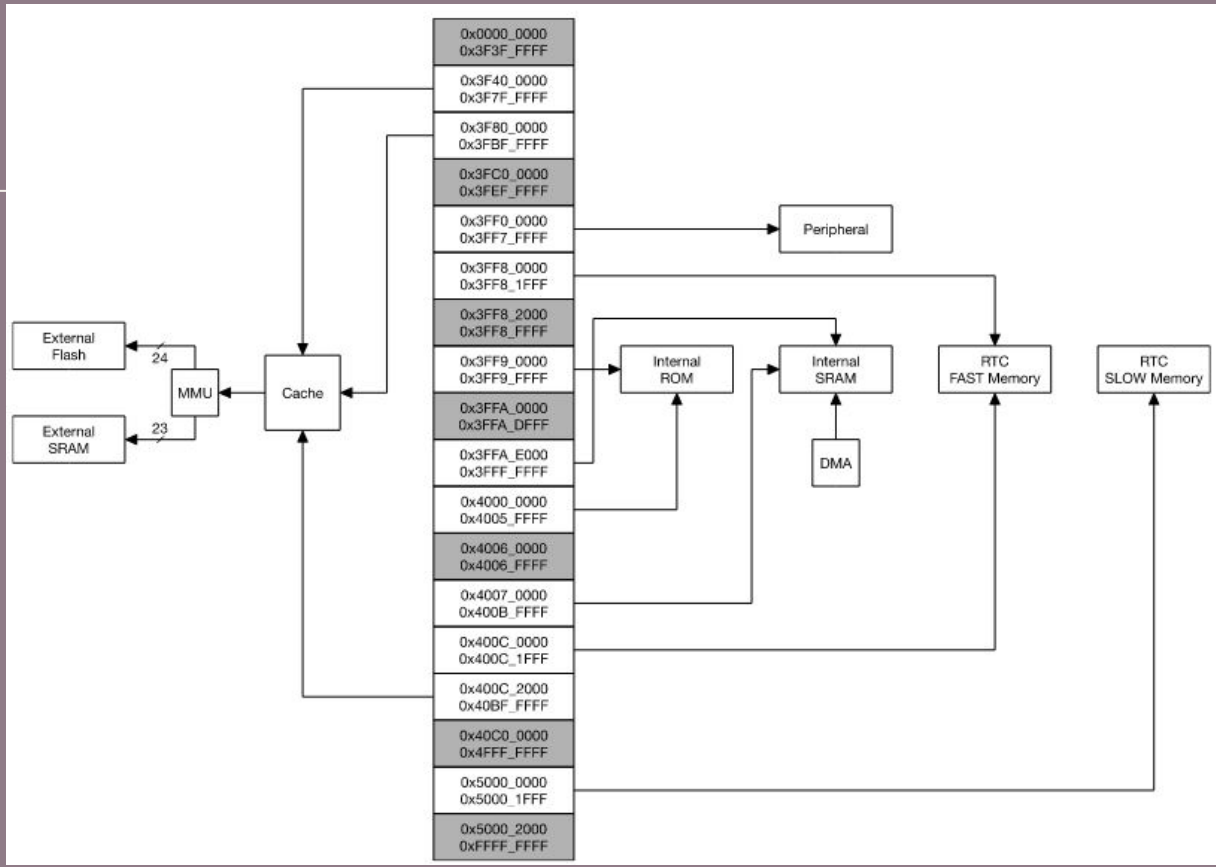
Power modes

- Active mode: The chip radio is powered on. The chip can receive, transmit or listen.
- Modem-sleep mode: The CPU is operational and the clock is configurable. The Wi-Fi/Bluetooth baseband and radio are disabled.
- Light-sleep mode: The CPU is paused. The RTC memory and RTC peripherals, as well as the ULP (ultra low power) coprocessor are running. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip.
- Deep-sleep mode: Only the RTC memory and RTC peripherals are powered on. Wi-Fi and Bluetooth connection data are stored in the RTC memory. The ULP coprocessor is functional.
- Hibernation mode: The internal 8 MHz oscillator and ULP coprocessor are disabled. The RTC recovery memory is powered down. Only one RTC timer on the slow clock and certain RTC GPIOs are active. The RTC timer or the RTC GPIOs can wake up the chip.

Address space

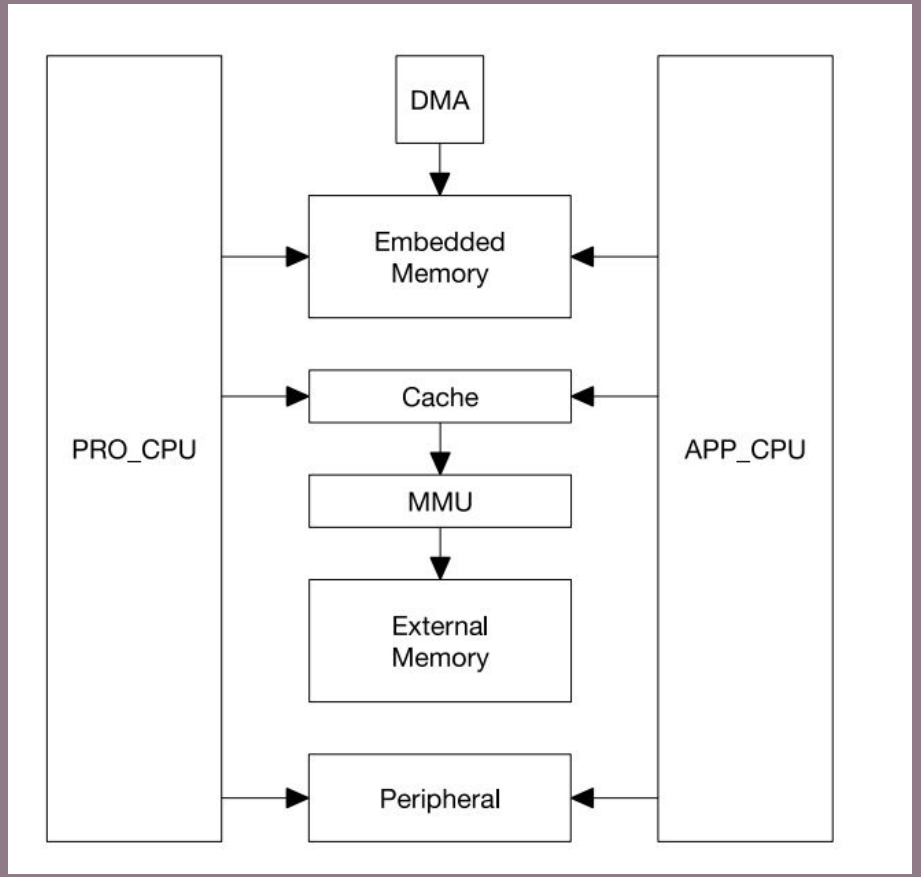
Each of the two CPUs has 4 GB (32-bit) address space.

- Below 0x4000_0000 are serviced using the data bus
- Between 0x4000_0000 and 0x4FFF_FFFF are serviced using the instruction bus
- Over 0x5000_0000 are shared by the data and instruction bus.



Address space

- Both processors are mapped symmetrically to this address space.
- It means, a register, for example, can be accessed from same address location from both the CPUs.



Address Mapping

- The data bus and instruction bus are both little-endian.
- The CPU can access data bus addresses via aligned or non-aligned byte, half-word and word read-and-write operations. And can read and write data through the instruction bus, but only in a word aligned manner.
- Each CPU can directly access embedded memory through both the data and instruction bus, external memory which is mapped into the address space (via transparent caching and MMU), and peripherals.

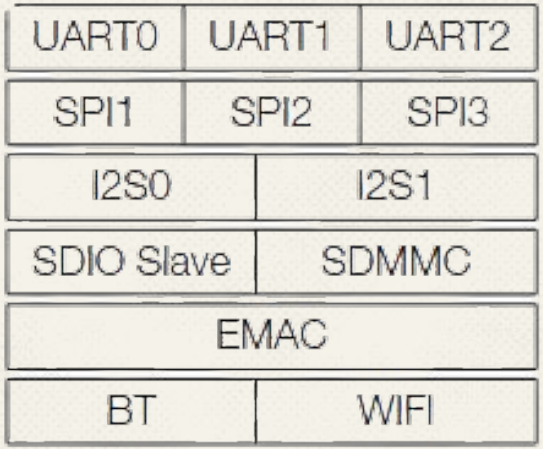
Bus Type	Boundary Address		Size	Target
	Low Address	High Address		
	0x0000_0000	0x3F3F_FFFF		Reserved
Data	0x3F40_0000	0x3F7F_FFFF	4 MB	External Memory
Data	0x3F80_0000	0x3FBF_FFFF	4 MB	External Memory
	0x3FC0_0000	0x3FEF_FFFF	3 MB	Reserved
Data	0x3FF0_0000	0x3FF7_FFFF	512 KB	Peripheral
Data	0x3FF8_0000	0x3FFF_FFFF	512 KB	Embedded Memory
Instruction	0x4000_0000	0x400C_1FFF	776 KB	Embedded Memory
Instruction	0x400C_2000	0x40BF_FFFF	11512 KB	External Memory
	0x40C0_0000	0x4FFF_FFFF	244 MB	Reserved
Data / Instruction	0x5000_0000	0x5000_1FFF	8 KB	Embedded Memory
	0x5000_2000	0xFFFF_FFFF		Reserved

DMA and External Memory

DMA

DMA data bus addressing = CPU data bus addressing to read and write

Peripherals (13) are equipped with DMA



External Memory

Can access external SPI flash and external SPI SRAM.

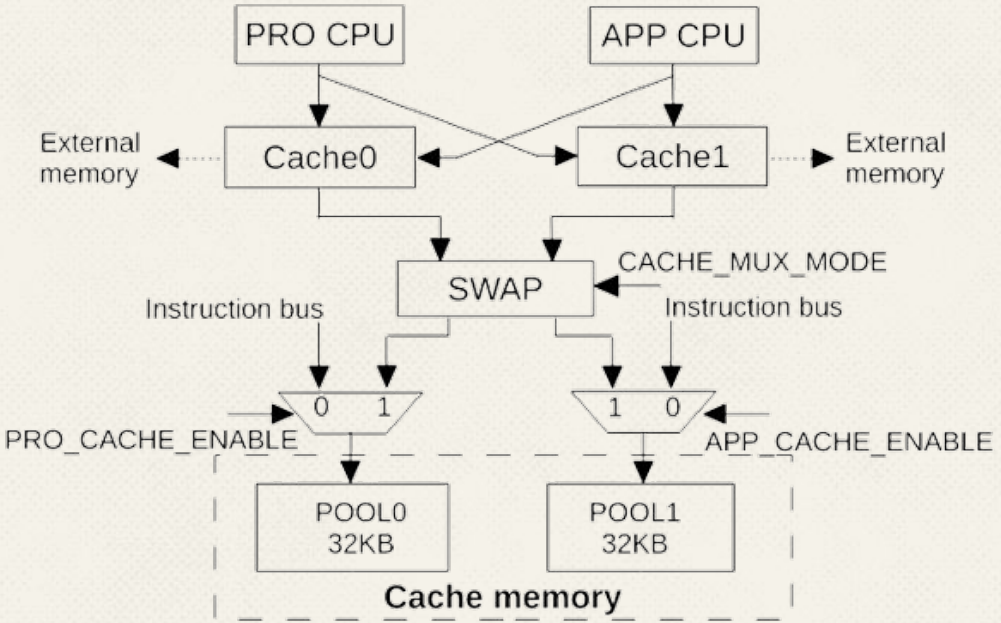
When CPU accesses external memory through the Cache and MMU

Cache map the CPU's address to an external physical memory address (in the address space defined by MMU settings)

Bus Type	Boundary Address		Size	Target	Comment
	Low Address	High Address			
Data	0x3F40_0000	0x3F7F_FFFF	4 MB	External Flash	Read
Data	0x3F80_0000	0x3FBF_FFFF	4 MB	External SRAM	Read and Write
Bus Type	Boundary Address		Size	Target	Comment
	Low Address	High Address			
Instruction	0x400C_2000	0x40BF_FFFF	11512 KB	External Flash	Read

Cache

- ESP32 uses a two-way set-associative cache.
- PRO CPU uses PRO_CACHE_ENABLE and APP CPU uses APP_CACHE_ENABLE to enable the Cache.
- CACHE_MUX_MODE (2 bits) can be set to select POOL0 or POOL1 or select both.
- Cache can also be used by the instruction bus (not used for PRO CPU or APP CPU).
- The cache data is written to the external SRAM memory.
- If the FLUSH function is used, the external memory is not written to.



CACHE_MUX_MODE	POOL0	POOL1
0	PRO CPU	APP CPU
1	PRO CPU/APP CPU	-
2	-	PRO CPU/APP CPU
3	APP CPU	PRO CPU

Bibliography

- https://www.espressif.com/sites/default/files/documentation/esp32_technical_reference_manual_en.pdf
- https://docs.espressif.com/projects/esp-idf/en/latest/esp32/hw-reference/esp32/get-started-devkitc.html
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