deti universidade de aveiro
departamento de eletrónica, telecomunicações e informática

Assignment 1 – Hamming codes

Arquiteturas de Alto Desempenho

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Gr5 TP2

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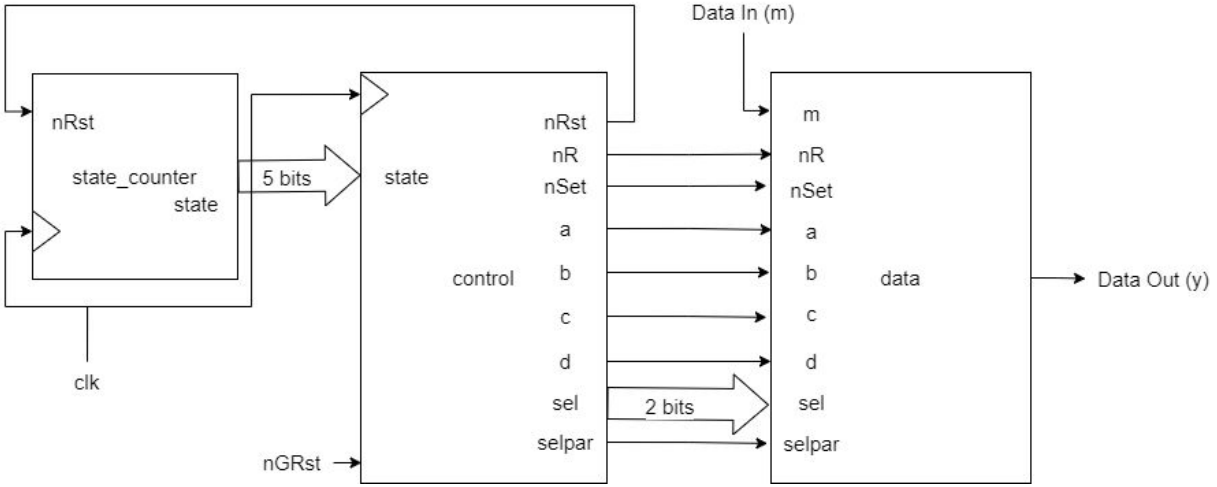
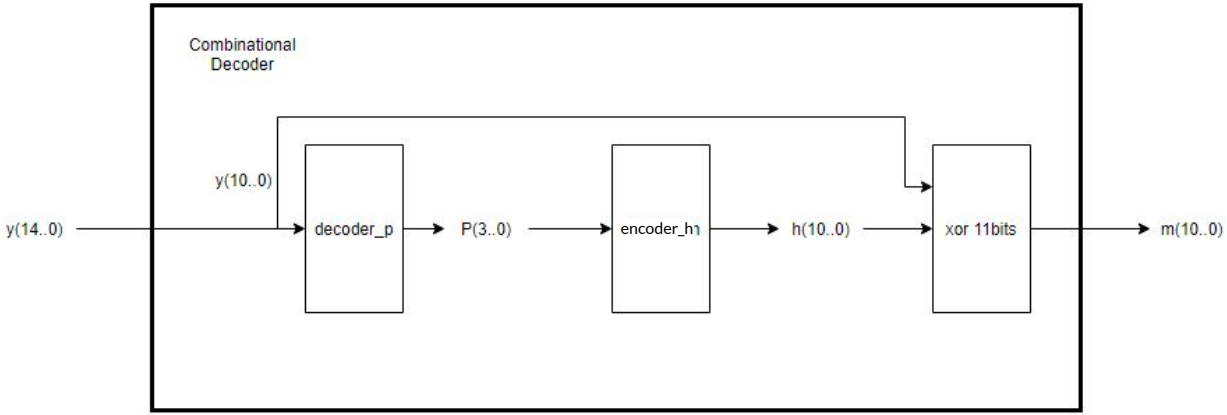


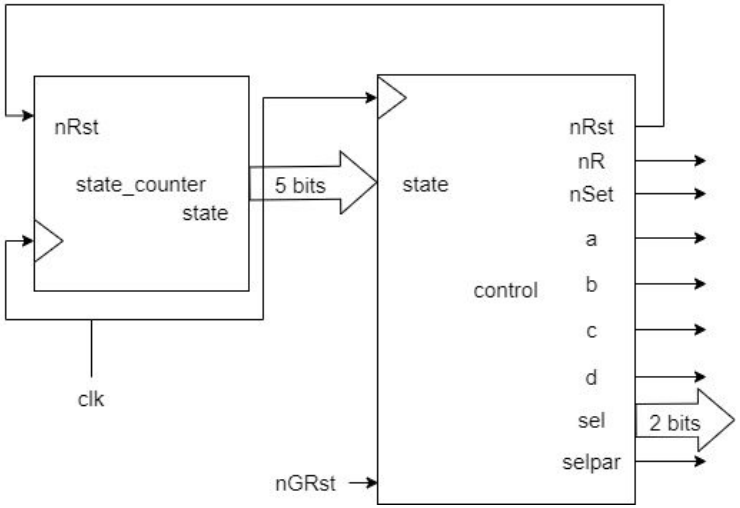
Encoder



Decoder

Encoder

Control Path



C4	C3	C2	C1	C0	nR	a	b	c	d	Sel1	Sel0	Selpar	nSet	nRst
0	0	0	0	0	1	1	1	0	0	0	0	0	1	1
0	0	0	0	1	1	1	0	1	0	0	0	0	1	1
0	0	0	1	0	1	1	0	0	1	0	0	0	1	1
0	0	0	1	1	1	0	1	1	0	0	0	0	1	1
0	0	1	0	0	1	0	1	0	1	0	0	0	1	1
0	0	1	0	1	1	0	0	1	1	0	0	0	1	1
0	0	1	1	0	1	1	1	1	0	0	0	0	1	1
0	0	1	1	1	1	1	1	0	1	0	0	0	1	1
0	1	0	0	0	1	1	0	1	1	0	0	0	1	1
0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
0	1	0	1	0	1	1	1	1	1	0	0	0	1	1
0	1	0	1	1	1	0	0	0	0	0	0	1	1	1
0	1	1	0	0	1	0	0	0	0	0	1	1	1	1
0	1	1	0	1	1	0	0	0	0	1	0	1	1	1
0	1	1	1	0	1	0	0	0	0	1	1	1	1	1
0	1	1	1	1	1	0	0	0	0	0	0	0	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	1	0

$nR = \overline{C4}$

$a = \overline{C4}.\overline{C2}.\overline{C0} + \overline{C3}.C2.C1 + \overline{C4}.\overline{C3}.\overline{C2}.\overline{C1}$

$b = \overline{C3}.C1.C0 + \overline{C3}.C2.\overline{C0} + \overline{C4}.\overline{C3}.\overline{C1}.\overline{C0} + C3.\overline{C2}.\overline{C1}.C0 + C3.\overline{C2}.\overline{C1}.C0$

$c = \overline{C3}.\overline{C2}.C0 + \overline{C3}.\overline{C1}.C0 + \overline{C2}.\overline{C1}.C0 + C3.\overline{C2}.\overline{C0} + \overline{C3}.C2.C1.\overline{C0}$

$d = \overline{C2}.C1.\overline{C0} + \overline{C3}.C2.\overline{C1} + \overline{C3}.C2.C0 + C3.\overline{C2}.\overline{C1}$

$Sel1 = C3.C2.\overline{C1}.C0 + C3.C2.C1.\overline{C0}$

$Sel0 = \overline{C4}.C3.C2.\overline{C0}$

$Selpar = \overline{C4}.C3.C2.\overline{C1} + \overline{C4}.C3.C2.\overline{C0} + C3.\overline{C2}.C1.C0$

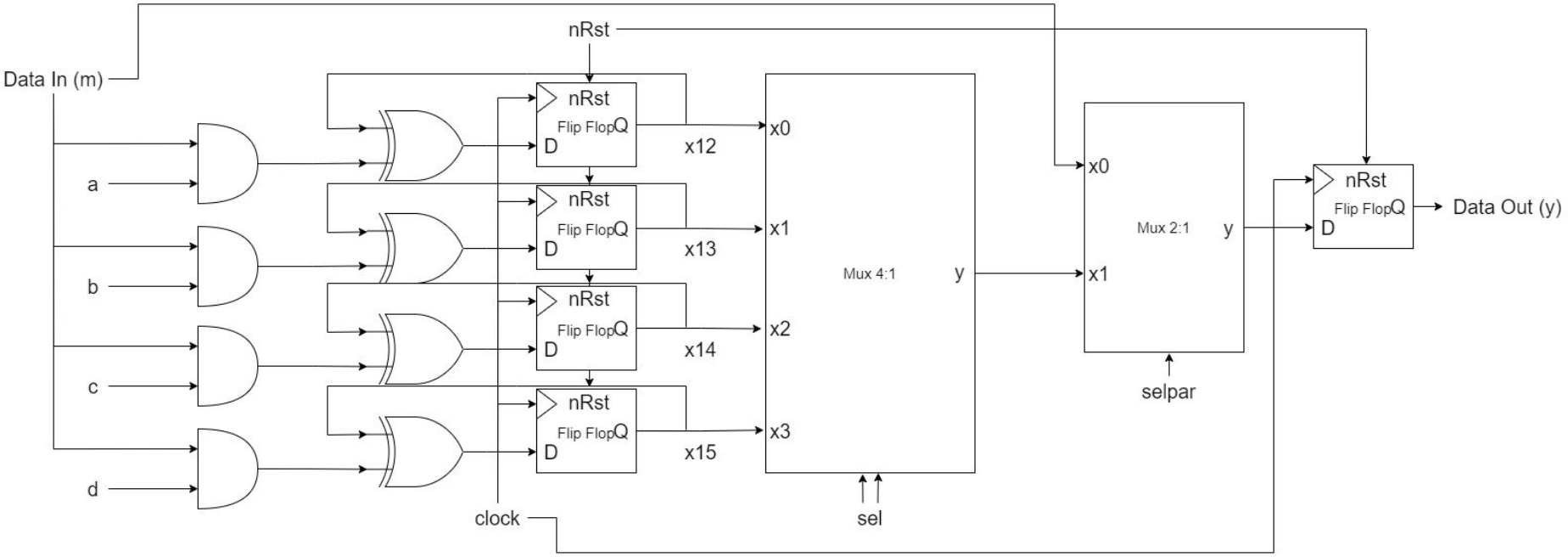
$nRst = \overline{C4}$

16 OR gates
57 AND gates

16 OR gates
37 AND gates

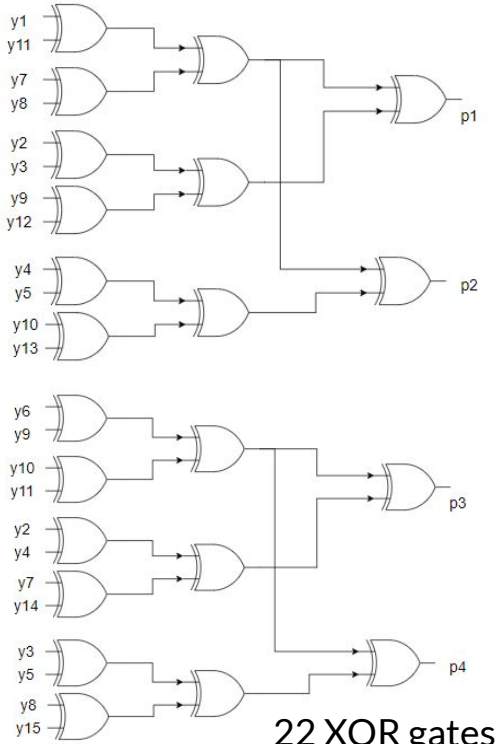
Encoder

Data Path



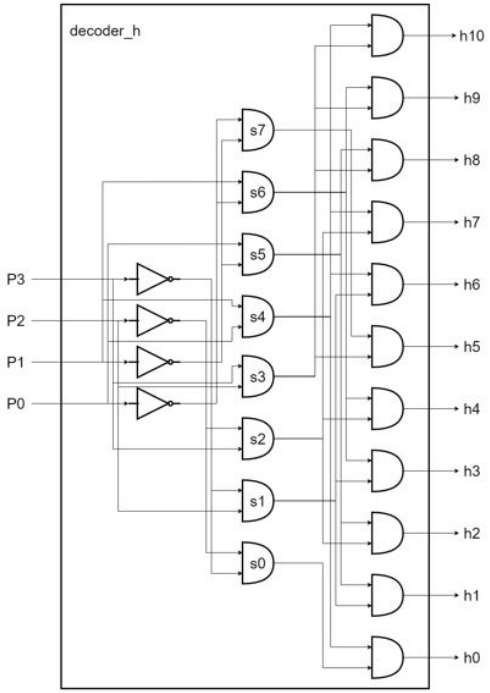
Decoder

decoder_p



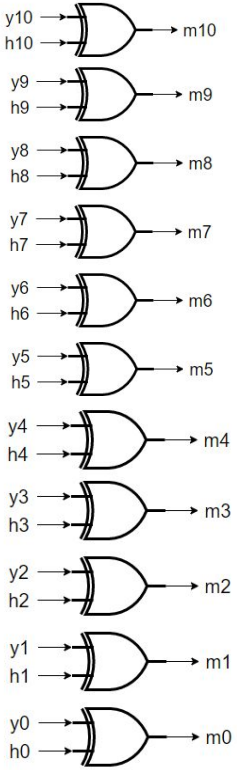
22 XOR gates
3 delays

encoder_h



19 AND gates
2 delays

xor_11_bits



11 XOR gates

Truth Table

encoder_h

$S0 = \overline{P3}.\overline{P2}$

$S1 = \overline{P3}.P2$

$S2 = P3.\overline{P2}$

$S3 = P3.P2$

$S4 = P1.P0$

$S5 = \overline{P1}.P0$

$S6 = P1.\overline{P0}$

$S7 = \overline{P1}.\overline{P0}$

$H0 = S0.S4$

$H1 = S1.S5$

$H2 = S2.S5$

$H3 = S1.S6$

$H4 = S2.S6$

$H5 = S3.S7$

$H6 = S1.S4$

$H7 = S2.S4$

$H8 = S3.S5$

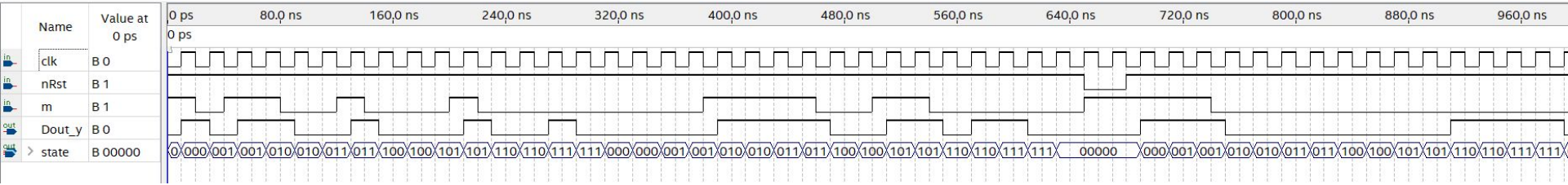
$H9 = S3.S6$

$H10 = S3.S4$

P3	P2	P1	P0	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	1
0	1	0	1	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	0	1	0	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0

Conclusions

Encoder



Decoder