busGrant

address data array with addr form cpuReqReg

!busGrant

read dataArray and write it to cacheRdData, assert cache done

!(cacheCs && cacheRead)

–

cacheCs && cacheRead

save request in cpuReqReg, perform a cache lookup, use addr from cacheAddr

wait bus grant complete

idle

busGrant

assert busReq, request bus write, use addr and data from victimReg

!busGrant && !victimRegDirty

read busData and output correct word to cacheRdData, assert cacheDone, write cache block into tag and data arrays, use addr from cpuReqReg, set from victimReg, and data from busData

tagHitEn

read dataArray and write it to cacheRdData, assert cache done

hit test

wait bus grant writeback

!busGrant

assert busReq

wait bus grant access

!tagHitEn

save victim data and addr in victimReg

!busGrant

assert busReq

!busGrant && victimRegDirty

write the cache block from the bus into the tag array, use the addr and set from victimReg as the set in the cache.

wait bus complete access

busGrant

assert busReq, request bus read, use addr from cpuReqReg

busGrant

–

Cache controller -
Read state machine

!(cacheCs && cacheWrite)
−

cacheCs && cacheWrite

save request in cpuReqReg,
perform a cache lookup,
use addr from cacheAddr

idle

hit test

tagHitEn

assert cacheDone,
write to tag and data arrays,
set tagDirty, use addr and data
from cpuReqReg,
use set from tagArray

!busGrant

assert cacheDone

wait bus
complete

busGrant

assert busReq,
request bus write word,
read addr and data from
cpuReqReg

busGrant
−

wait
bus
grant

!tagHitEn
−

!busGrant

assert busReq

Cache controller -
Write state machine