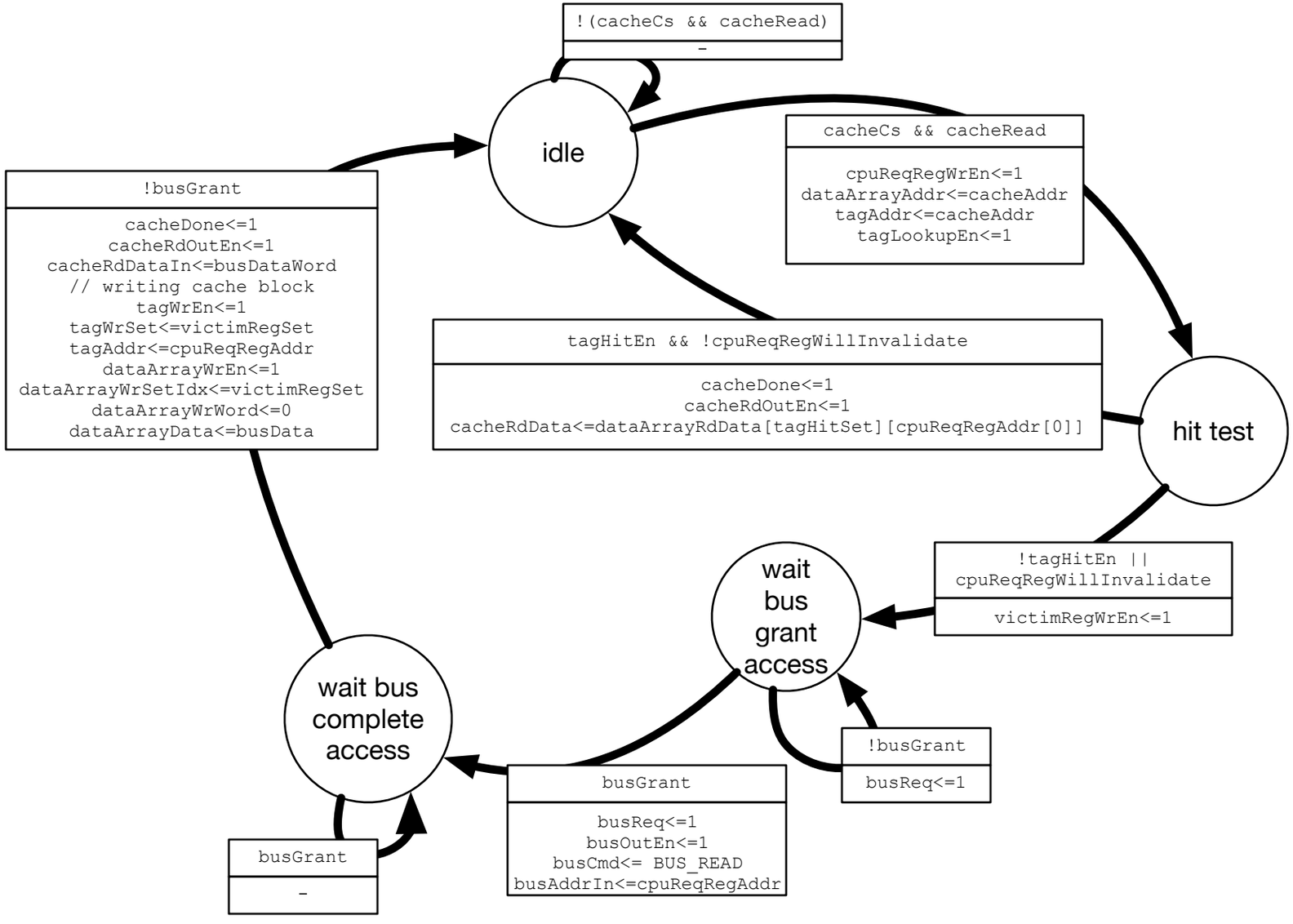



```
Default values (internal flags):
cpuReqRegWrEn<=0
victimRegWrEn<=0
tagLookupEn<=0
tagWrEn<=0
tagWrSetDirty<=0
dataArrayWrEn<=0
dataArrayWrWord<=0
busOutEn<=0
cacheRdOutEn<=0

Default values (outputs):
cacheDone<=0
busReq<=0
```

Cache controller read state machine

Inputs and outputs

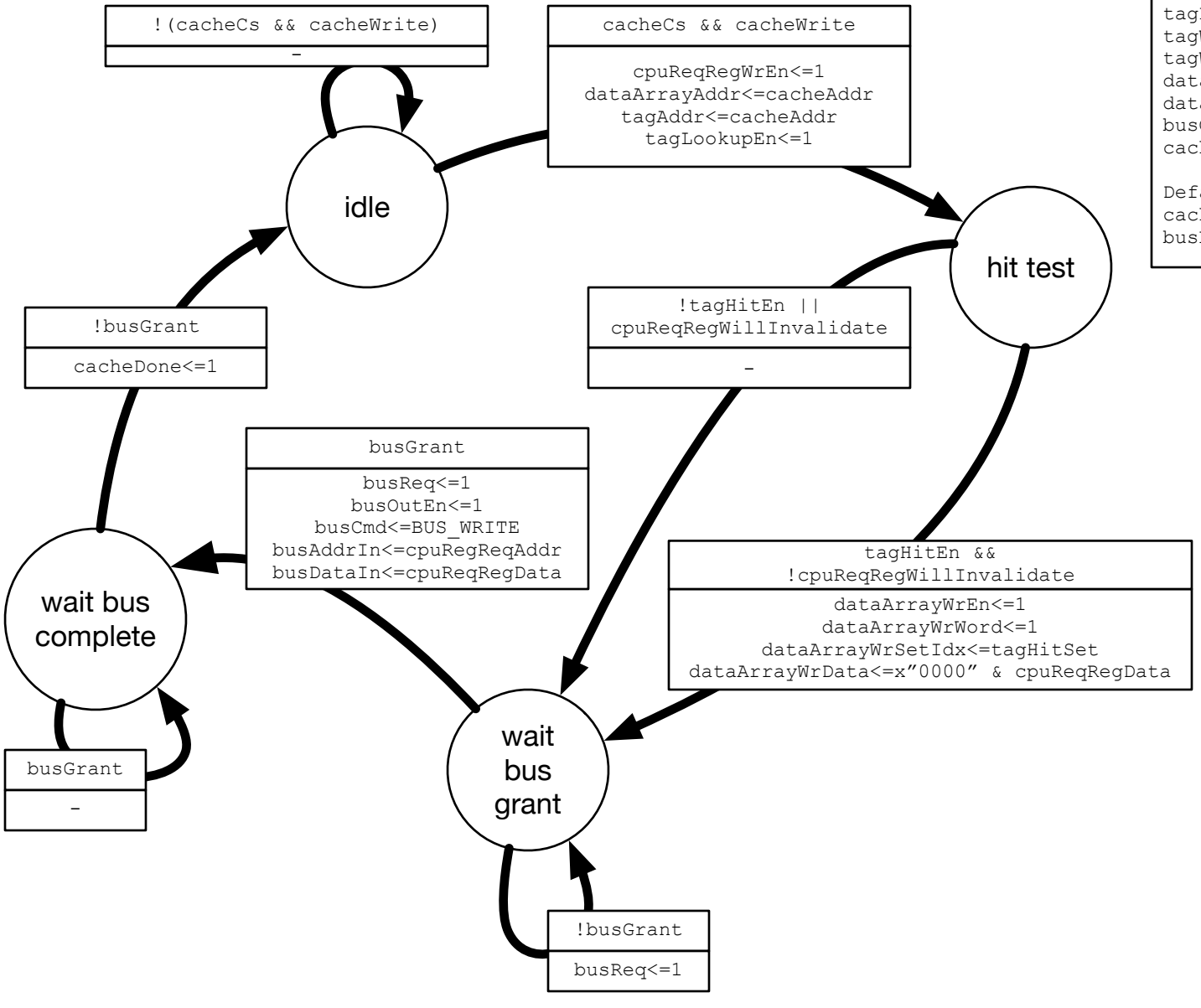
Cache:

inputs_cpu: cacheCs, cacheRead, cacheWrite, cacheAddr, cacheWrData,

outputs_cpu: cacheRdData, cacheDone

outputs_bus: busReq, busAddr, busData

inputs_bus: busGrant, busData




```
Default values (internal flags):
cpuReqRegWrEn<=0
victimRegWrEn<=0
tagLookupEn<=0
tagWrEn<=0
tagWrSetDirty<=0
dataArrayWrEn<=0
dataArrayWrWord<=0
busOutEn<=0
cacheRdOutEn<=0

Default values (outputs):
cacheDone<=0
busReq<=0
```

Cache controller write state machine

Inputs and outputs

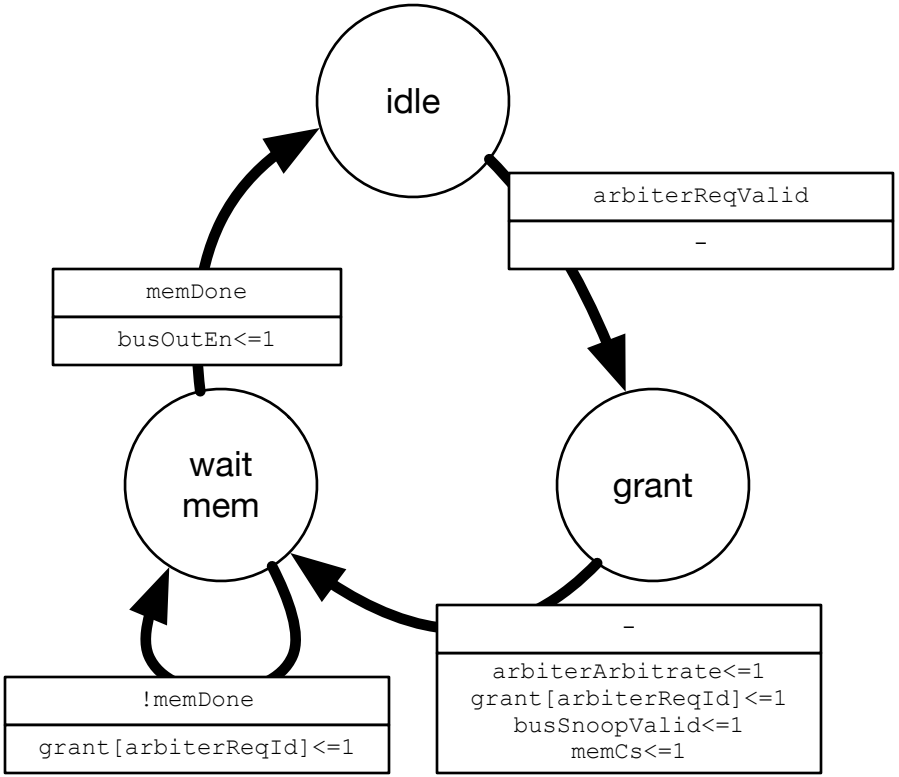
Cache:

inputs_cpu: cacheCs, cacheRead, cacheWrite, cacheAddr, cacheWrData,

outputs_cpu: cacheRdData, cacheDone

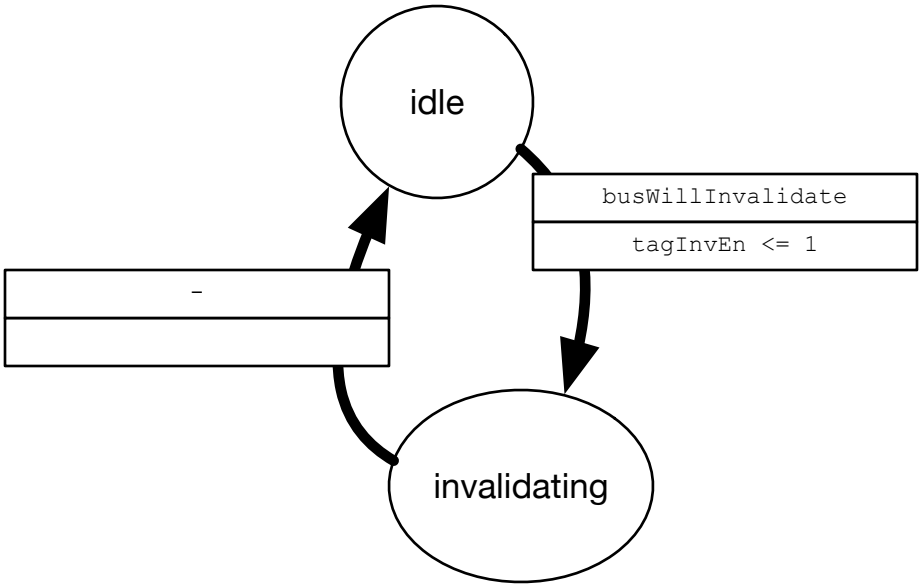
outputs_bus: busReq, busAddr, busData

inputs_bus: busGrant, busData




```
Default values (internal flags):
arbiterArbitrate<=0
busOutEn<=0
Default values (outputs):
busGrant<=0
memCs<=0
busSnoopValid <= 0
```

Bus controller state machine:
inputs_cache: busReq[ ], busAddr, busData, busCmd
outputs_cache: busData, busGrant[ ]
outputs_mem: memCs, memRead, memWrite, memWriteWord, memWrData
inputs_mem: memDone, memRdData




```
Default values (outputs):
tagInvEn <= 0
```

Cache snoop state machine

Cache controller datapath

Control
cacheCs
cacheRead
cacheWrite

Control
busAddr
Control
cacheAddr
cpuReqRegAddr

TagArray
tagInvEn
tagInvAddr
tagLookupEn
tagWrEn
tagWrSet
tagAddr
tagHitEn
tagHitSet
tagVictimSet

Control
VictimReg
victimRegWrEn
victimRegSetIn
victimRegSet
Control

Control
DataArray
dataArrayAddr
dataArrayWrEn
dataArrayWrWord
dataArrayWrSetIdx
dataArrayWrData
dataArrayRdData

cpuReqRegAddr[0]
busDataWord
Control
RdDataTriStateBuffer
cacheRdOutEn
cacheRdDataIn
cacheRdData
cacheRdData

x“0000” & cpuReqRegData
busData
busGrant

Control

Control
CpuReqReg
currReqWillInvalidate
cacheAddr
cacheWrData
cpuReqRegWrEn
cpuReqRegWasInvalidatedIn
cpuReqRegAddrIn
cpuReqRegDataIn
cpuReqRegWasInvalidated
cpuReqRegAddr
cpuReqRegData

BusTriStateBuffer
busOutEn
busCmdIn
busAddrIn
busDataIn
busCmd
busAddr
busData
busReg
busCmd
busAddr
busData

cpuReqRegAddr[0]
busData
busDataWord

Control
busCmd
“BUS_WRITE”
busSnoopValid
busGrant
busWillInvalidate <=
(busCmd == BUS_WRITE) &&
busSnoopValid && !busGrant
busWillInvalidate

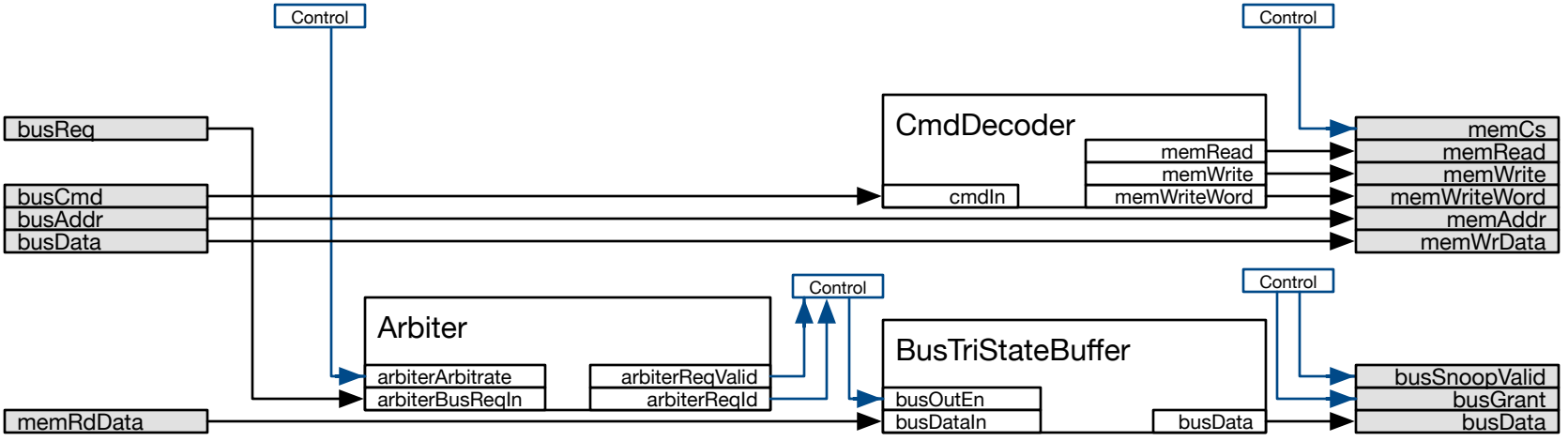
cacheAddr
busAddr
busWillInvalidate
currReqWillInvalidate <=
(cacheAddr == busAddr) &&
busWillInvalidate
currReqWillInvalidate

cpuReqRegAddr
cpuReqRegWasInvalidated
cpuReqRegWillInvalidate <=
((cpuReqRegAddr == busAddr) &&
busWillInvalidate) ||
cpuReqRegWasInvalidated
cpuReqRegWillInvalidate

Legend

Breaks a signal in half

Multiplexer



Bus controller datapath