

Default values (internal flags):

```

cpuReqRegWrEn<=0
victimRegWrEn<=0
tagLookupEn<=0
tagWrEn<=0
tagWrSetDirty<=0
dataArrayWrEn<=0
dataArrayWrWord<=0
busOutEn<=0
cacheRdOutEn<=0

```

Default values (outputs):

```

cacheDone<=0
busReq<=0

```

Cache controller read state machine

Inputs and outputs

Cache:

inputs_cpu: cacheCs, cacheRead, cacheWrite, cacheAddr, cacheWrData,

outputs_cpu: cacheRdData, cacheDone

outputs_bus: busReq, busAddr, busData

inputs_bus: busGrant, busData

Default values (internal flags):

```
cpuReqRegWrEn<=0
victimRegWrEn<=0
tagLookupEn<=0
tagWrEn<=0
tagWrSetDirty<=0
dataArrayWrEn<=0
dataArrayWrWord<=0
busOutEn<=0
cacheRdOutEn<=0
```

Default values (outputs):

```
cacheDone<=0
busReq<=0
```

Cache controller write state machine

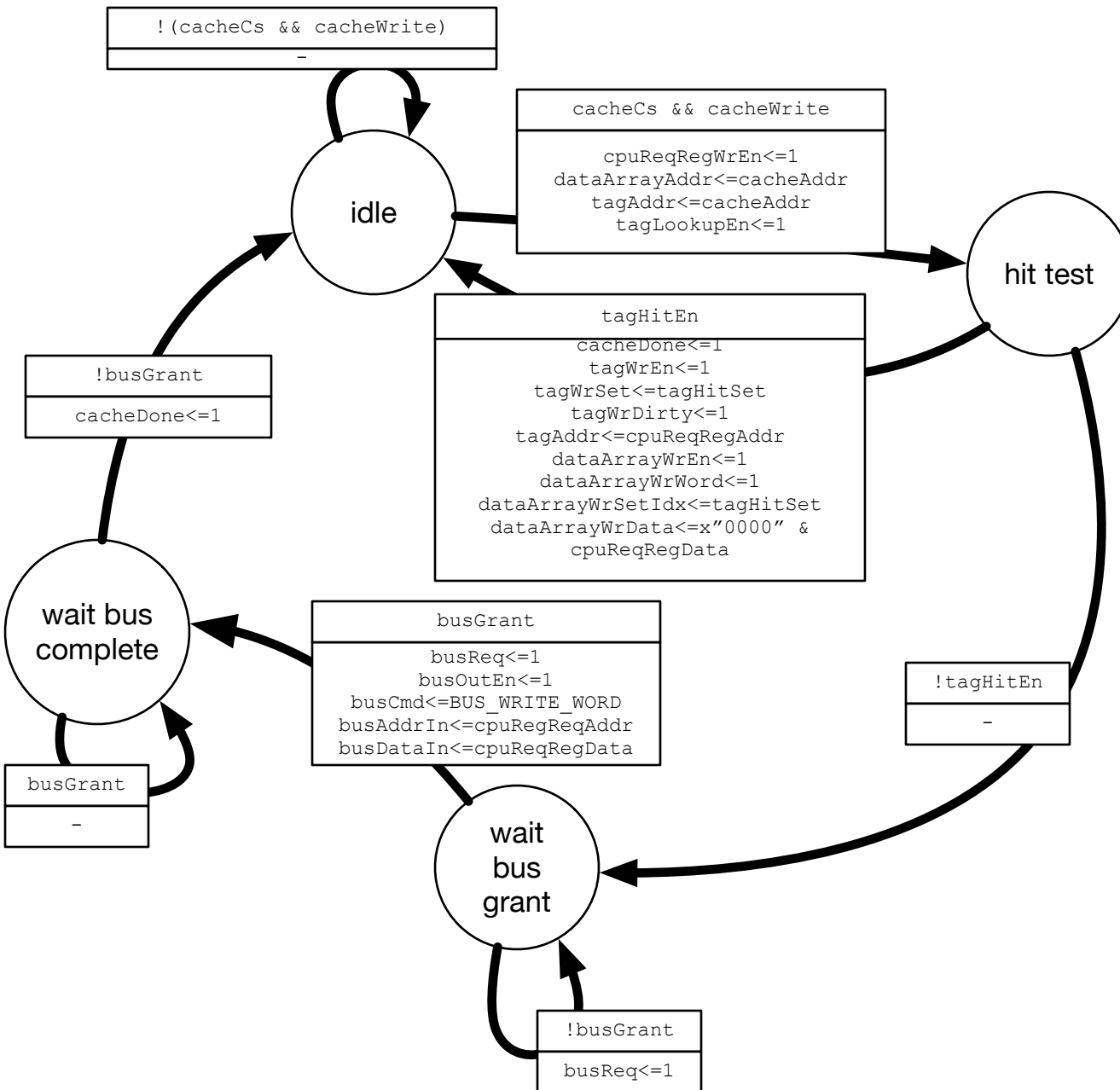
Inputs and outputs

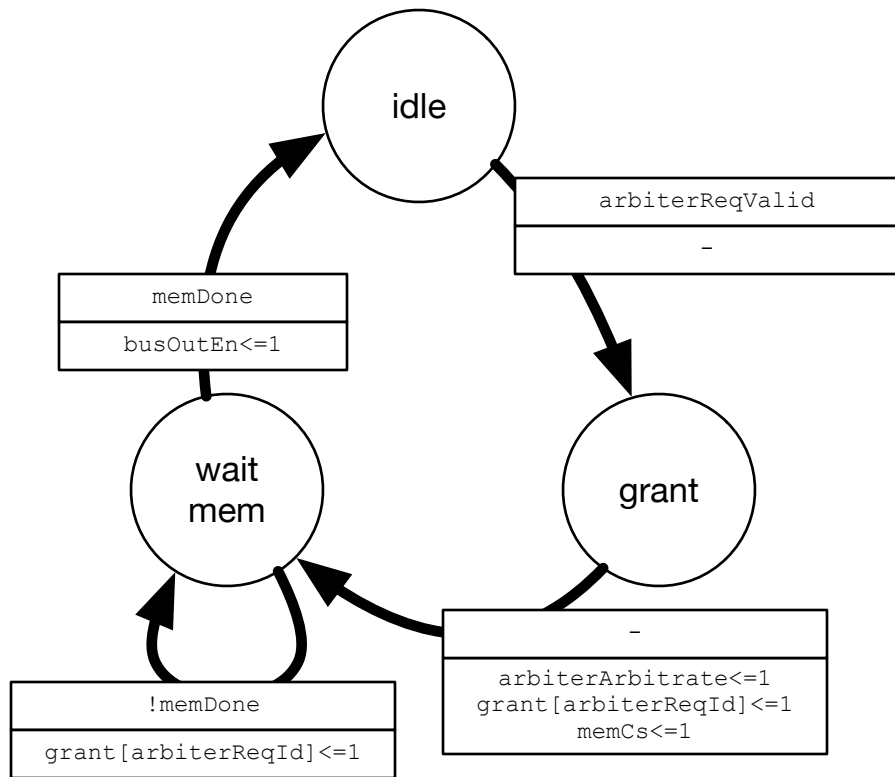
Cache:

inputs_cpu: cacheCs, cacheRead, cacheWrite, cacheAddr, cacheWrData,
outputs_cpu: cacheRdData, cacheDone

outputs_bus: busReq, busAddr, busData

inputs_bus: busGrant, busData





Default values (internal flags):
 arbiterArbitrate<=0
 busOutEn<=0

Default values (outputs):
 busGrant<=0
 memCs<=0

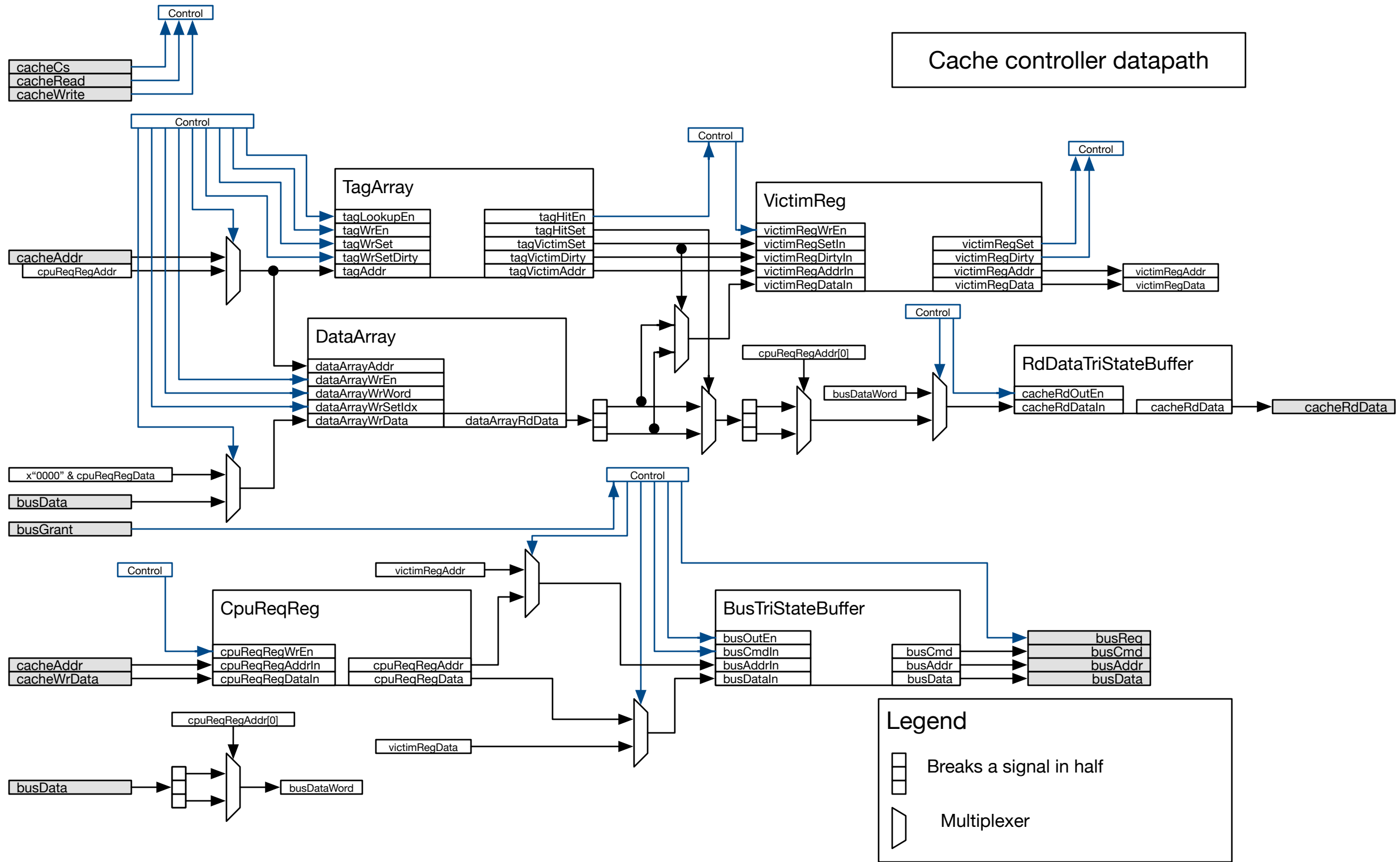
Bus controller state machine:

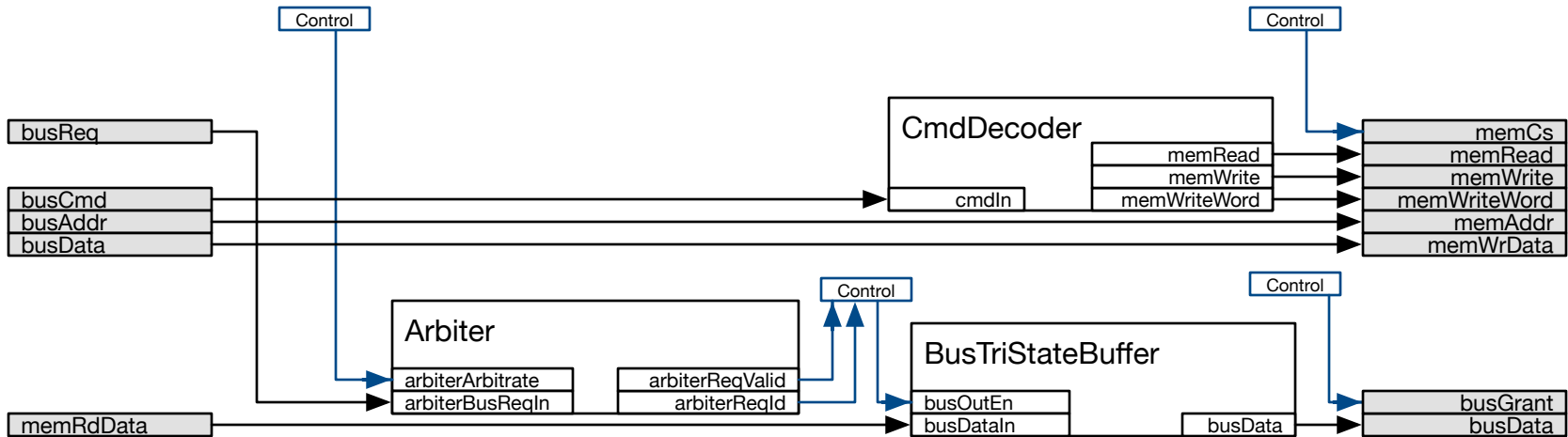
inputs_cache: busReq[],
 busAddr, busData, busCmd

outputs_cache: busData,
 busGrant[]

outputs_mem: memCs,
 memRead, memWrite,
 memWriteWord, memWrData

inputs_mem: memDone,
 memRdData





Bus controller datapath