

Default values (internal flags):

```

cpuReqRegWrEn<=0
victimRegWrEn<=0
tagLookupEn<=0
tagWrEn<=0
tagWrSetDirty<=0
dataArrayWrEn<=0
dataArrayWrWord<=0
busOutEn<=0
cacheRdOutEn<=0

```

Default values (outputs):

```

cacheDone<=0
busReq<=0

```

**Cache controller write state machine**

**Inputs and outputs**

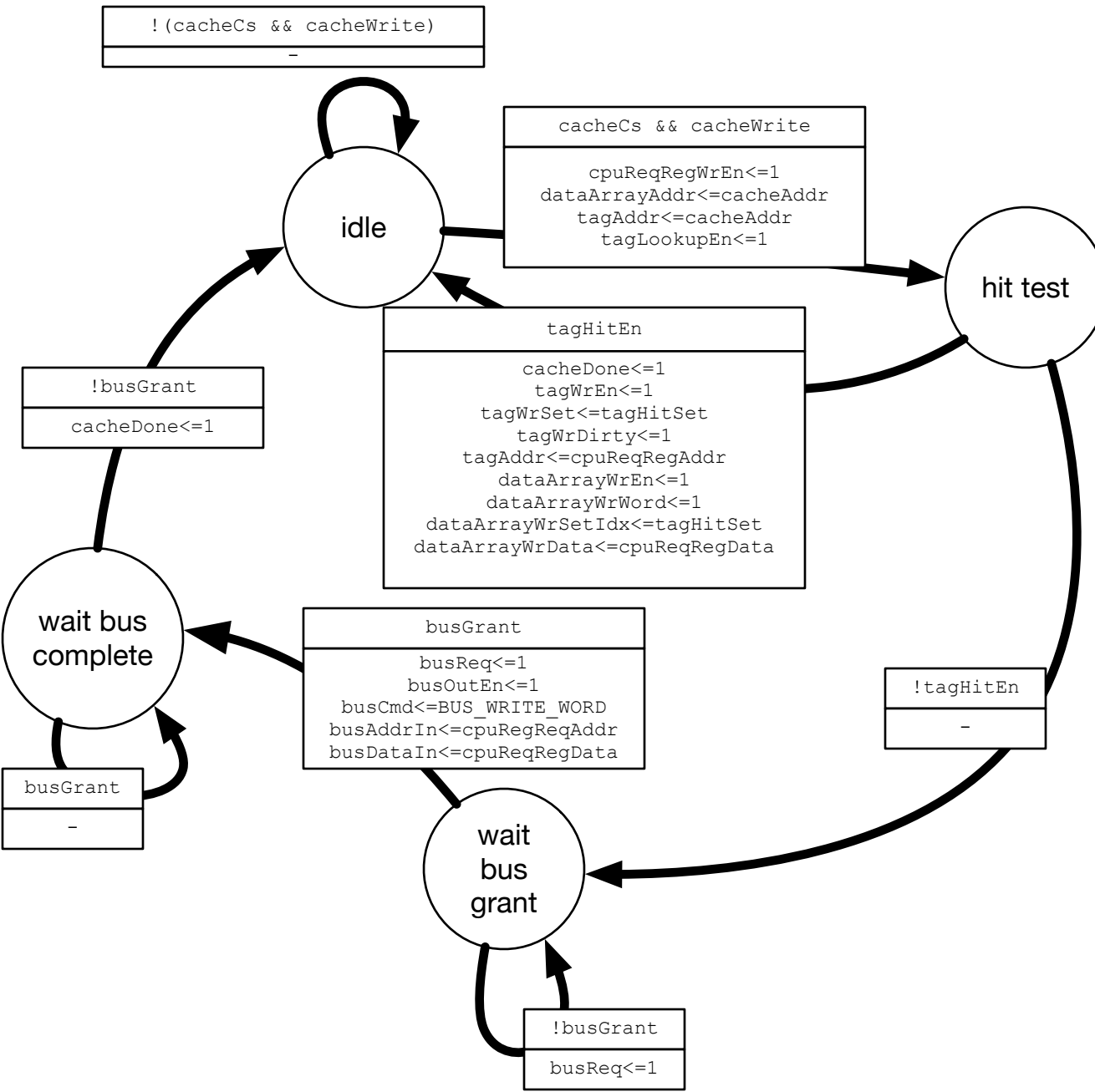
Cache:

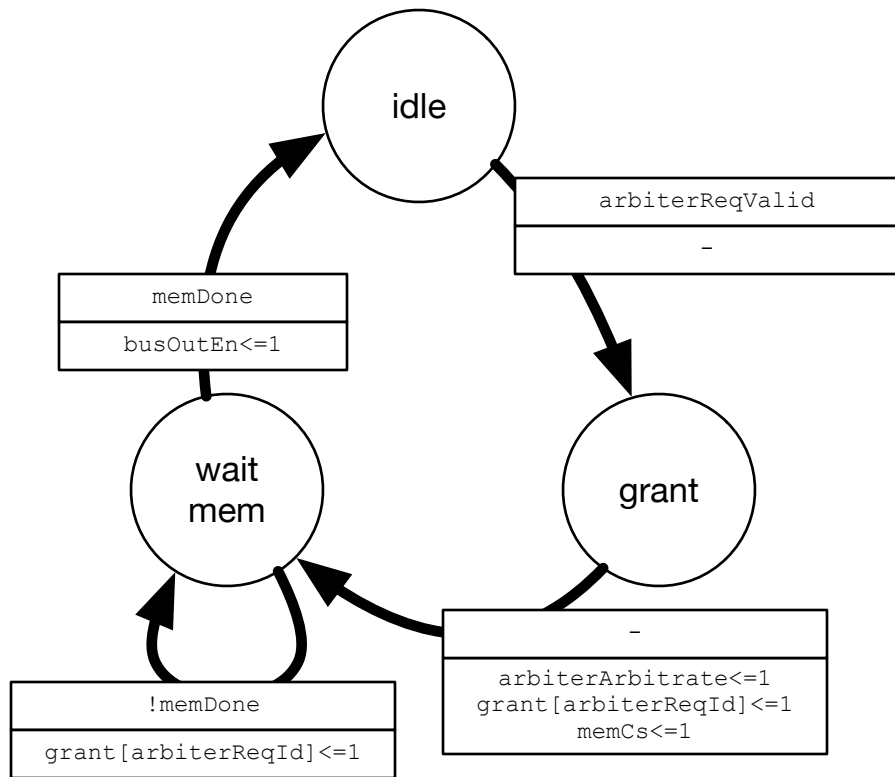
**inputs\_cpu:** cacheCs, cacheRead, cacheWrite, cacheAddr, cacheWrData,

**outputs\_cpu:** cacheRdData, cacheDone

**outputs\_bus:** busReq, busAddr, busData

**inputs\_bus:** busGrant, busData





Default values (internal flags):  
 arbiterArbitrate<=0  
 busOutEn<=0

Default values (outputs):  
 busGrant<=0  
 memCs<=0

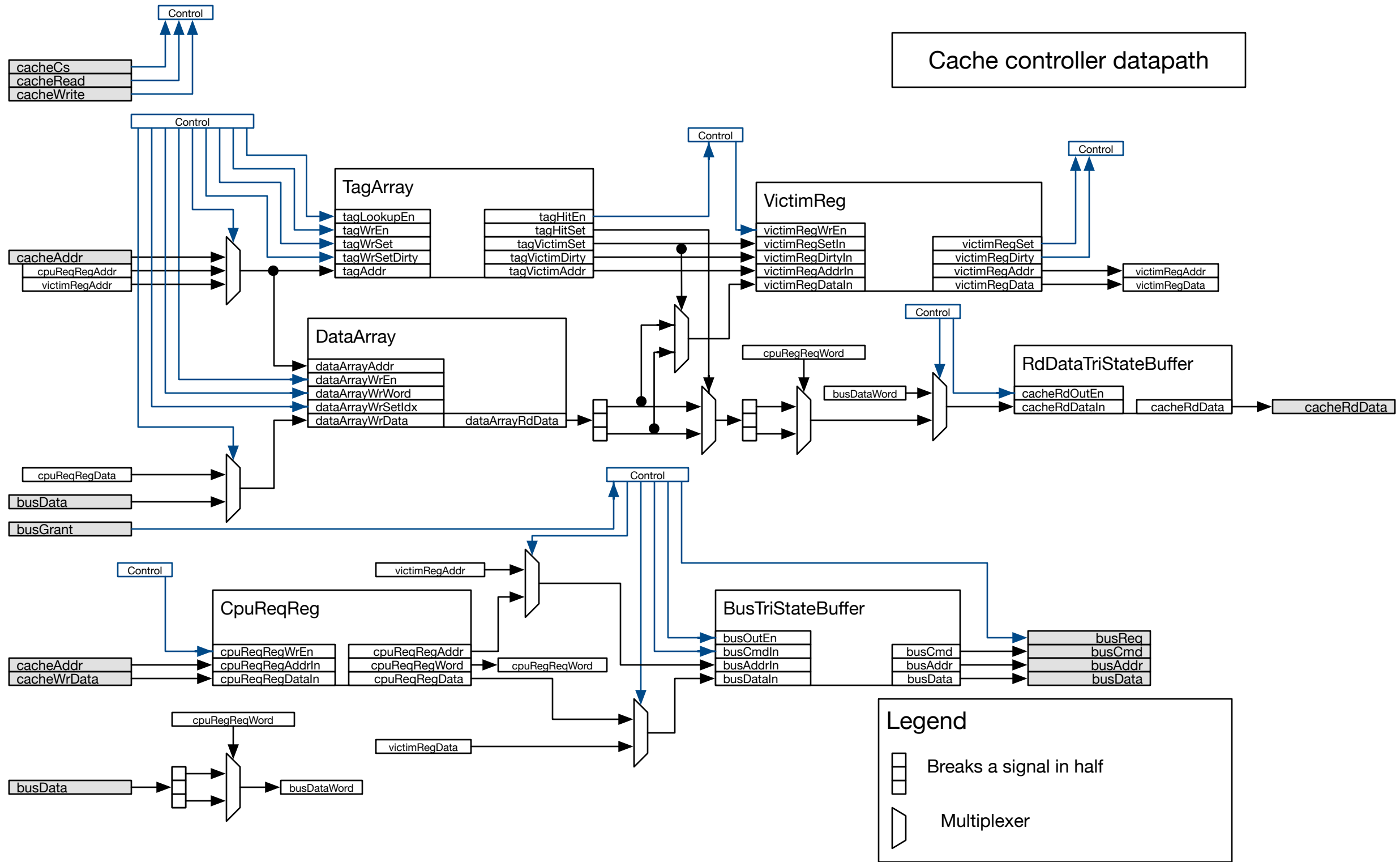
### Bus controller state machine:

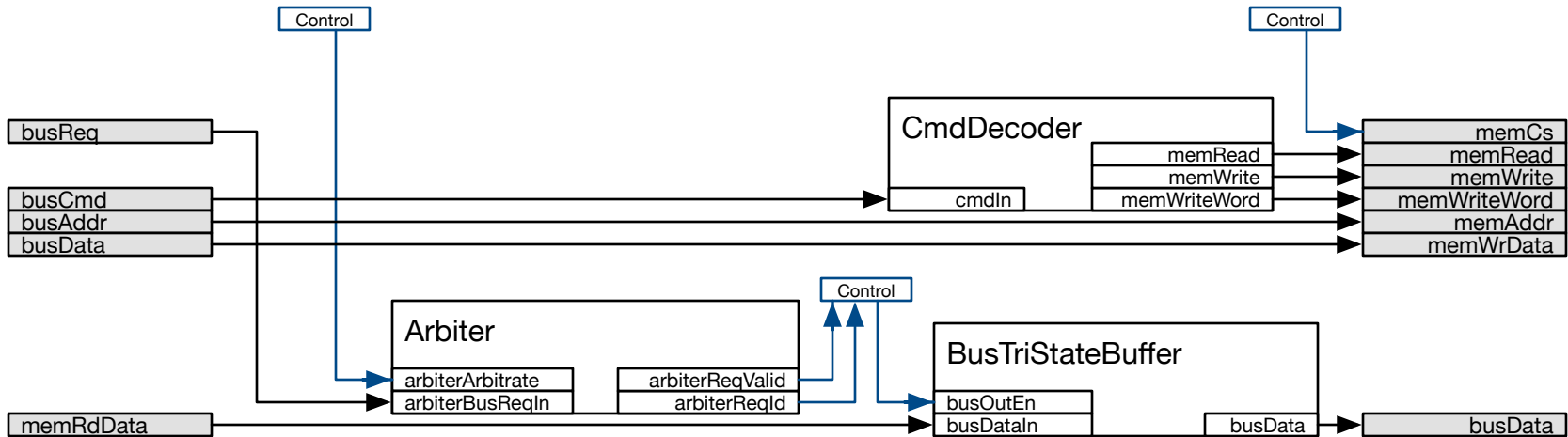
**inputs\_cache:** busReq[ ],  
 busAddr, busData, busCmd

**outputs\_cache:** busData,  
 busGrant[ ]

**outputs\_mem:** memCs,  
 memRead, memWrite,  
 memWriteWord, memWrData

**inputs\_mem:** memDone,  
 memRdData





Bus controller datapath