1.EmPowerSoC Tool

1.1 Introduction

We have built an open-source EDA tool, EmPowerSoC**,** that can be used for power estimation of SoC. It has been developed alongside the existing QFlow open-source tool chain as indicated below which is currently being used for implementation of RTL to GDSII flow.

The main highlights of the EmpowerSoC tool are**:**

1. It can be used by researchers to calculate the most importantaspect of designing a SoC – Power Dissipation. EmpowerSoC brings together the features of various open-source tools along with an additional feature of estimating power dissipation. It saves a lot of effort and time and its user-friendliness makes it an indispensable tool for the researchers.

2. Power estimation is done by extracting transistor level netlists of thebuilding blocks on an automated basis.

3. In EmpowerSoC, the user has the flexibility to calculate both active andstandby power dissipation. Standby power (leaking power) is the power which is dissipated from the SoC while it is not active i.e. in sleep/standby mode. It is a major contributor to power dissipation and becomes an essential design parameter while designing a SoC. Active power, in contrast to Standby Power, is the power which is dissipated while the SoC is active i.e. while performing a particular task.

4. EmpowerSoC comes with an intuitive and user-friendly GUI which iseasy to use and also allows the user to open multiple instances and show the results simultaneously.

5. EmpowerSoC is backed by comprehensive documentation which is easyto understand and self-explanatory. The Installation Procedure and Tutorials have been presented in a lucid manner and guides the users how to start using the tool.

The emerging trend in applications for the ever increasing functionality, performance and integration within SoC is leading to designs that dissipate

power in huge amounts and hence it has become essential to keep an eye at the amount of power dissipation while designing a SoC. This makes the EmpowerSoC an indispensable tool for the researchers who wish to put forward new low power SoC designs.

1.2 Motivation

Power analysis is an important consideration while designing a SoC. The Power computation of Very Large Scale Integrated Circuits (VLSI) are far beyond human ability because of their complexity. So to analyse power in these circuits we have to use professional computer aided tools. Most of such tools are proprietary which makes them less accessible to the vast majority of students. We have built an open source tool, EmpowerSoC which can be used for estimation of Power consumption of a circuit. This tool can be used by students as well as professionals, and it provides an alternate to the costly proprietary software.

Through this project, we wanted to familiarise ourselves with the VLSI design flow and learn more about the effort that goes behind building an Electronic Design Automation tool. We wanted to learn more about the various open source VLSI tools available and understand their functioning.

1.3 LITERATURE SURVEY:

Qflow tool chain : Qflow is an open source tool chain that can be used for the complete RTL to GDSII flow. It takes the Verilog source code as input and can generate the physical layout. It provides an alterative to the commercial proprietary Electronic Design Automation softwares by companies like Cadence and Synopsys. It is helpful for startup companies, students and small businesses who cannot afford to do purchase these softwares for integrated circuit design.

Qflow tool chain consists of the following-

Yosys : It is an open source RTL synthesis tool. Yosys provides a basic set of synthesis algorithms for processing the synthesizable Verilog code and also for converting Verilog to simple RTL Verilog format.

Graywolf : Graywolf is the tool that takes care of placement. Placement is an essential step in physical design flow. It is used for placing and assigning locations to various circuit subsystems within the chip.

Qrouter : Qrouter takes care of Routing. Routing is the next step after placement in the VLSI design flow. Qrouter is used for connecting the placed subsystems within the chip using wires.

Opentimer/OpenSTA : OpenSTA is an open source tool that is used for performing static timing analysis. STA is an important step in VLSI design flow. OpenSTA uses standard file formats to verify the timing of a design.

Magic : Magic is an open source layout tool. It is popular and easy-to-use VLSI layout tool. It can perform Design Rule Checking(DRC), Parasitic Extraction etc. After the verification, the data is converted to the industry standard GDSII format.

Ngspice : Ngspice is used for electronic circuit simulation. It supports all kinds of circuits. Using Ngspice we can perform DC, transient and AC analysis. There is also an option to view the output waveform.

1.4 Power Dissipation in CMOS

The power Dissipation in CMOS circuits is mainly of 2 types- Dynamic Power and Static Power.

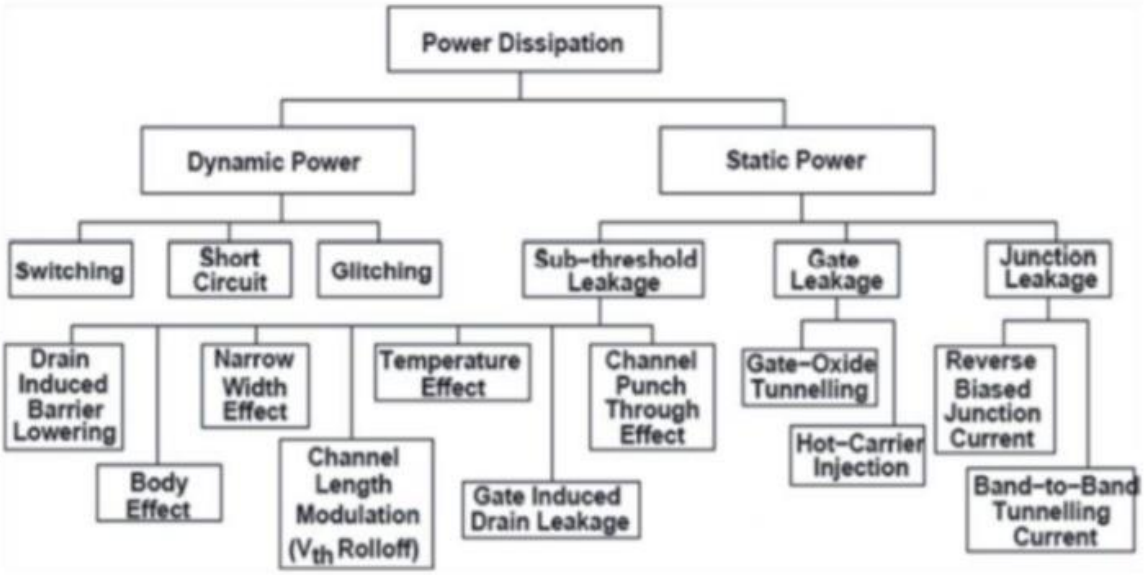

Figure-1 Different Types of Power Dissipation

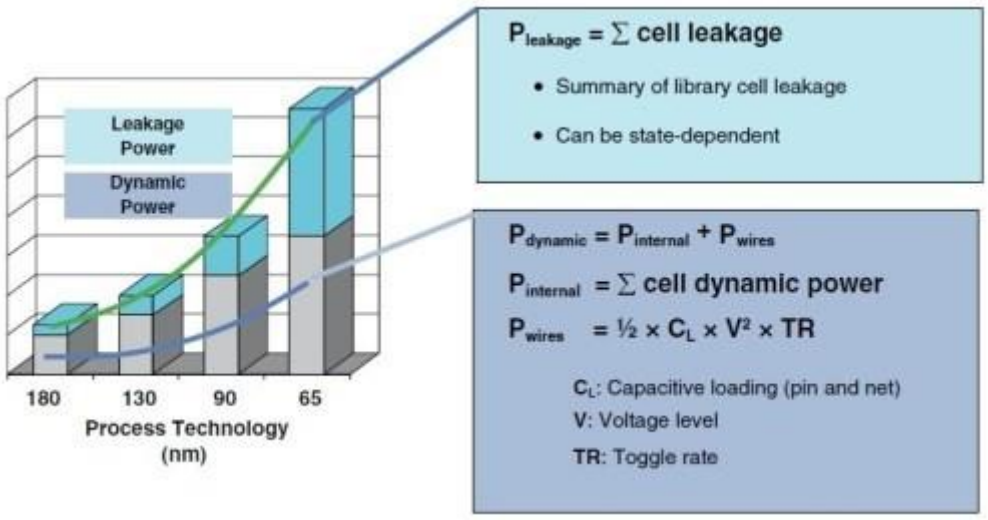

Figure-2 Power Dissipation

Dynamic Power is the power consumed when the circuit is in active state. It consists of Switching Power dissipation, short circuit Power Dissipation and Glitching Power dissipation. Switching power dissipation consists of the power that is dissipated in the parasitic capacitors and resistors while charging and discharging. Short circuit Power dissipation consists of the

power that is dissipated during switching when a path exists from VDD to Ground for current to flow. Glitching power dissipation occurs when the input signals to a particular logic block reach at the input of a gate at different times.

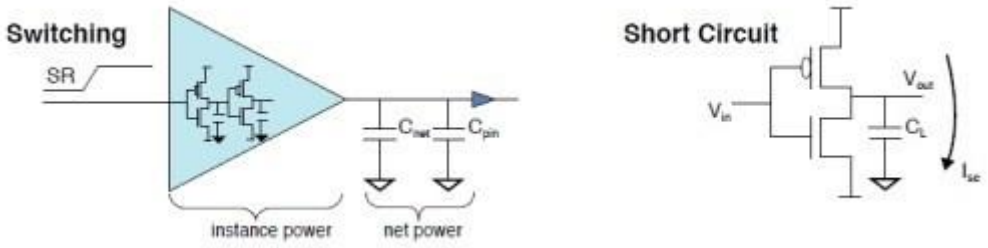

Figure-3 Short-Circuit and Switching Power

Static Power mainly consists of the power dissipated due to leakage current. Static power dissipation is a constant factor in CMOS circuits and is not dependent on Switching. Below 90nm technology, it has become an important contributor to the power dissipation, The main causes of static power dissipation are Sub threshold leakage, gate leakage, and Junction leakage.

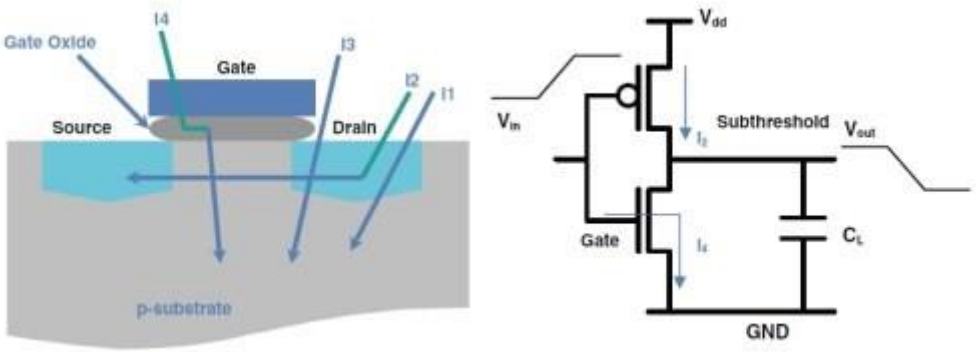

Figure-4 Leakage Power

2. Work done till date on EmPowerSoc

2.1 Tool Flow

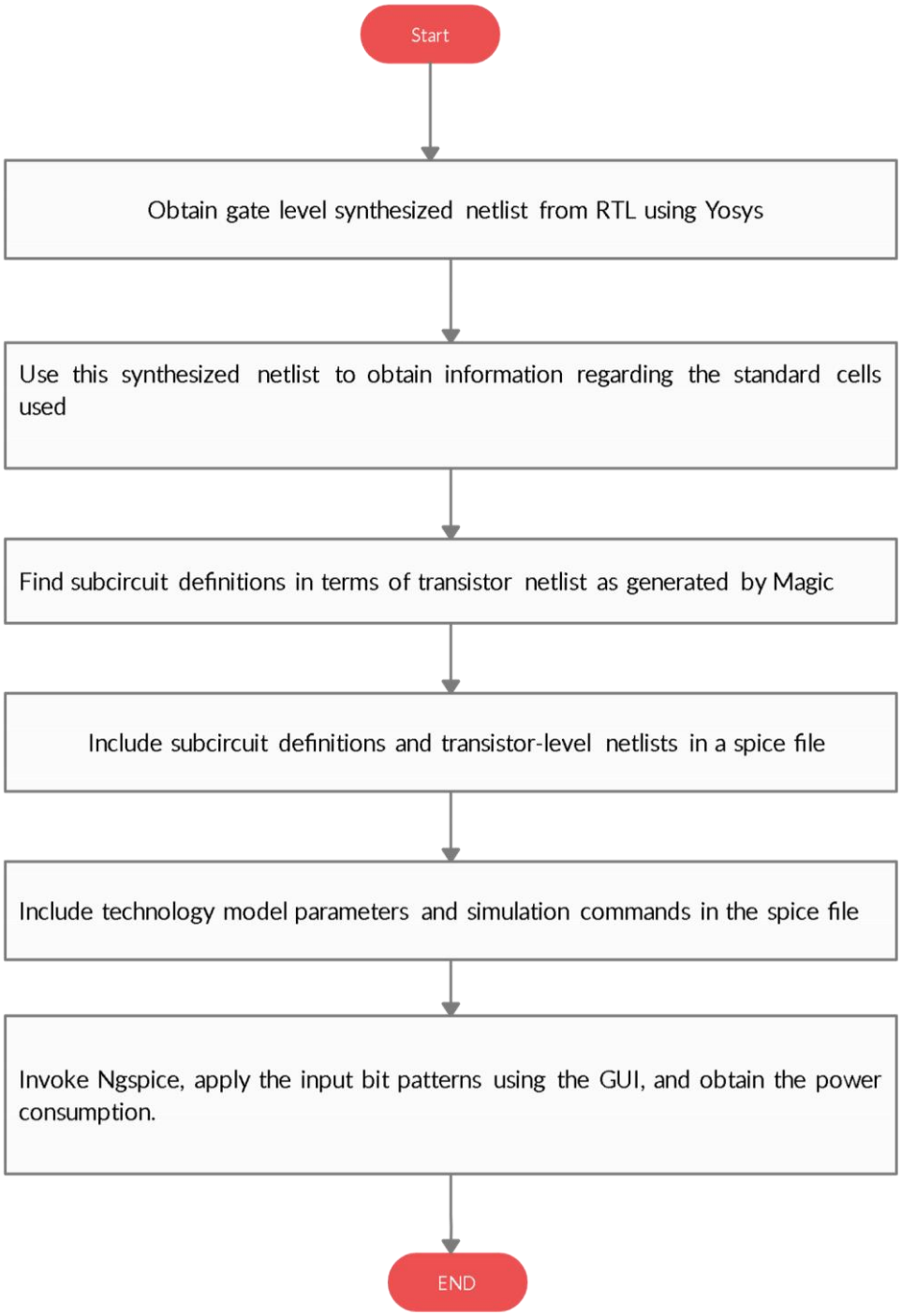

Figure-5 Flow chart of EmpowerSoC

The entire automation was created using scripting in Python and Perl programming languages on the Linux operating system.

Some important files used for the automation are-

1. .ys : Synthesis file containing information about standard cells

2. BLIF (Berkeley Logic Interchange Format)

The BLIF file is used to convert any digital circuit in text format, as any digital circuit can be visualised as a directed graph of combinational and sequential logic nodes which can be represented in form of text by using various .net commands.

3. .ext :
.ext files can be extracted with the help of Magic tool. It contains the environmental information (scaling, timestamps, etc.), and the layout of different subcells and logic gates used in the cell. This can be used to extract the gate level netlist of any ASIC Design.

4. .spice : Transistor level netlists for the standard cells. These files are usedby Ngspice for simulation.

5. .mag : This is the layout file. It is used to extract the .ext files for thesub_cells of our model.

While developing an open-source tool, a GUI had to be created for smooth functioning of the tool. For creating the GUI of EmPowerSoC, we used the PyQt5 distribution of Python language. PyQt5 can be used for developing highresolution GUI applications and is a cross- platform toolkit. PyQt5 also consists of a set of developer tools which makes developing GUI applications even more fluent and easily. We used the Qt Designer(Developer tool) for designing the layout for our tool.
After designing the layout, the entire backend was done using python and Perl scripting. The entire flow was then connected using the backend scripting.

2.2 Methodology used for power calculation

Power can be considered in active mode and standby mode. Active power is the power consumed while the chip is active, the inputs and outputs are changing and is doing useful work. It mainly consists of the switching power.
Whereas, the standby power is the power consumed when the device is in sleep mode or when the input and output nodes are stable and no useful work is being done.

We have calculated the Average Active Power consumption by taking the product of average current drawn from the supply during active mode of operation and supply voltage. Similarly, average Standby Power consumption is calculated as the product of average leakage current when the inputs are not changing(standby mode of operation) and supply voltage.

2.3 TOOL GUI

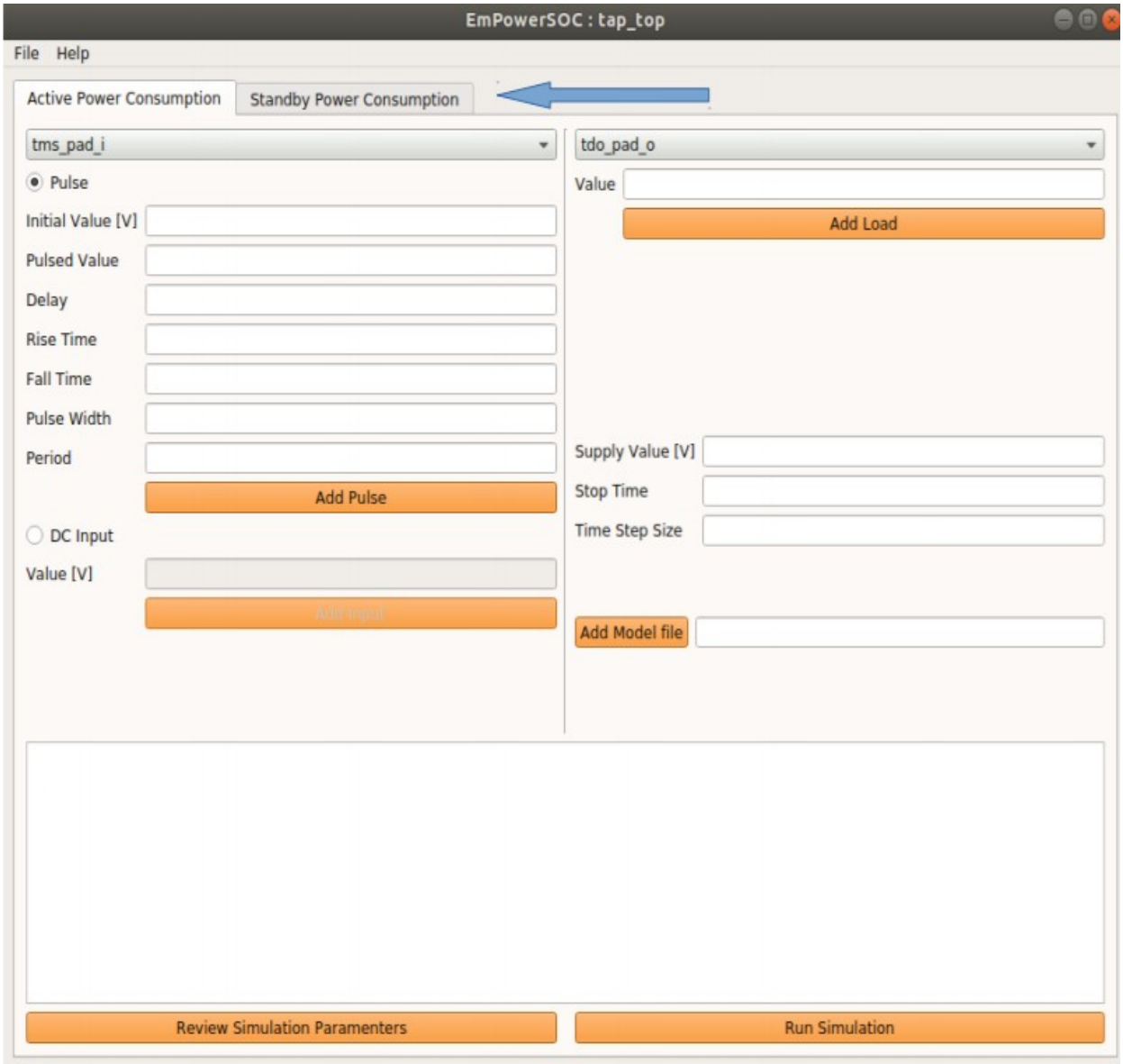

Figure-6 GUI of the tool

2.4 Installation procedure

Requirements:

- Qflow tool chain
- Python 3 and PyQt
- Perl

Guidelines:

- Install Qflow using : https://github.com/kunalg123/vsdflow. The VSD team has provided a script to install Qflow and all its dependencies.
- Download the EmPowerSoc debian package.

To install the package-Open terminal and change directory to the location where the package is downloaded and run the following command-

- sudo gdebi <package_name>
- Or, you can install the package using GUI installer. ○ Now, EmPowerSoc is ready to be used.

2.5 Result

Table-1 Active Power Consumption values for different modules

Module Type	Total_q	Energy_avg	Power_avg_abs	Power_avg_uw
Inverter	**-1.782e-13**	**3.207e-13**	**3.207e-05**	**3.207e+01**
3-bit UpCounter	**-1.312e-12**	**2.362e-12**	**2.362e-04**	**2.362e+02**
Jtag	**-2.496e-10**	**4.493e-10**	**1.123e-02**	**1.123e+04**

3. REFERENCES

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2. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design”Wiley.
3. http://opencircuitdesign.com/qflow/ - QFlow Documentation

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Akshat Jain
Naveen Dugar
Nimesh Shahdadpuri
Sagar Yadav
Kunal Ghosh

Division of Electronic and Communication Engineering
NSIT New Delhi, India