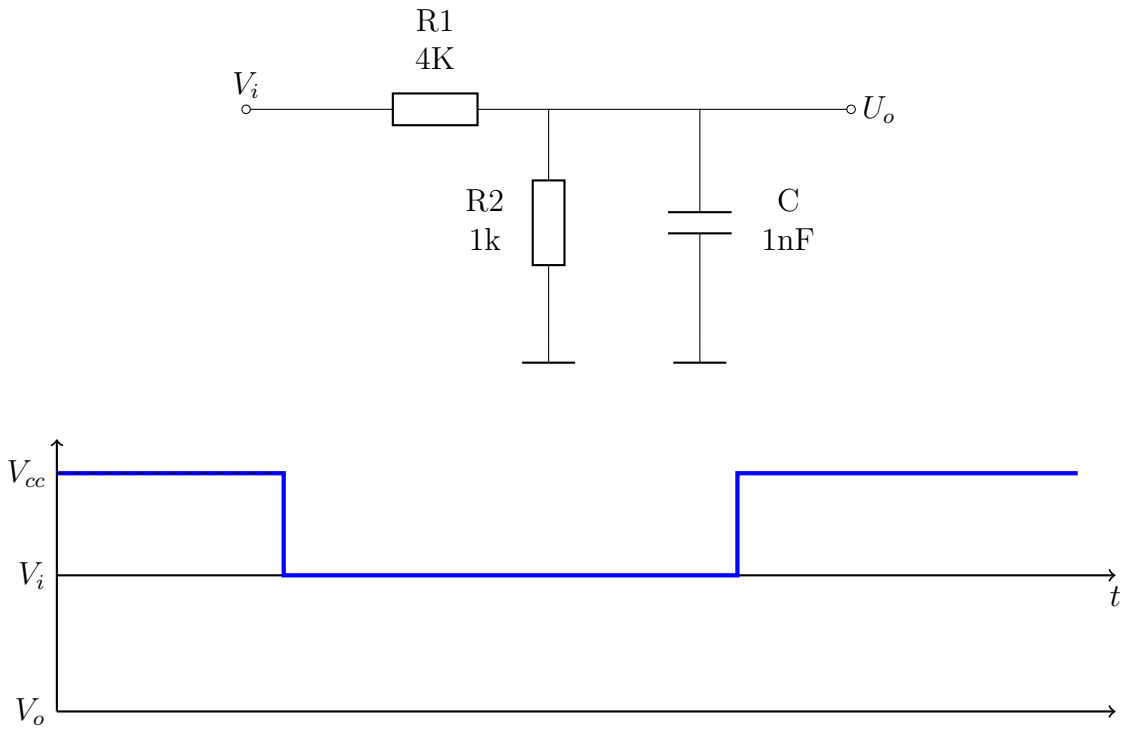
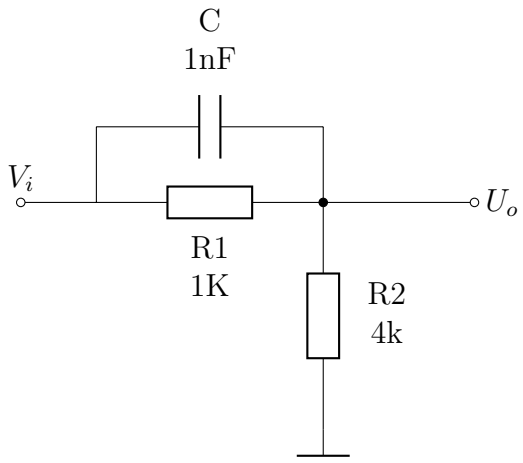
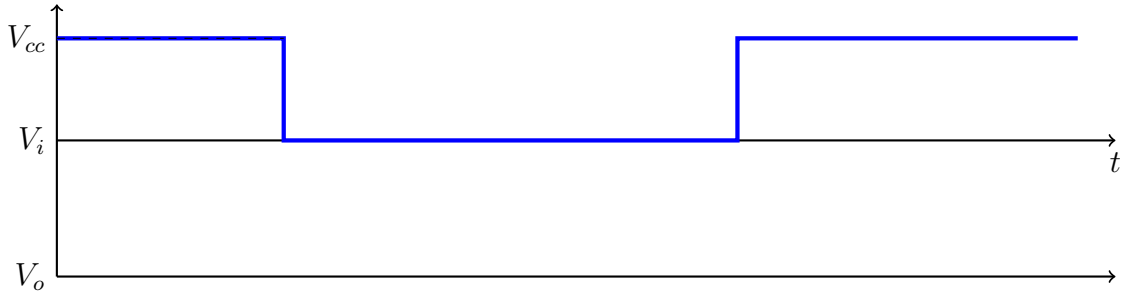
Plot the output signal for the following circuit and calculate the moments when the output signal crosses $0.1V_{cc}$ and $0.9V_{cc}$ (if they do), relative to the input signal edges. Assume $V_{cc} = 5V$. The duration of the input pulse is long enough for all the voltages to stabilize.

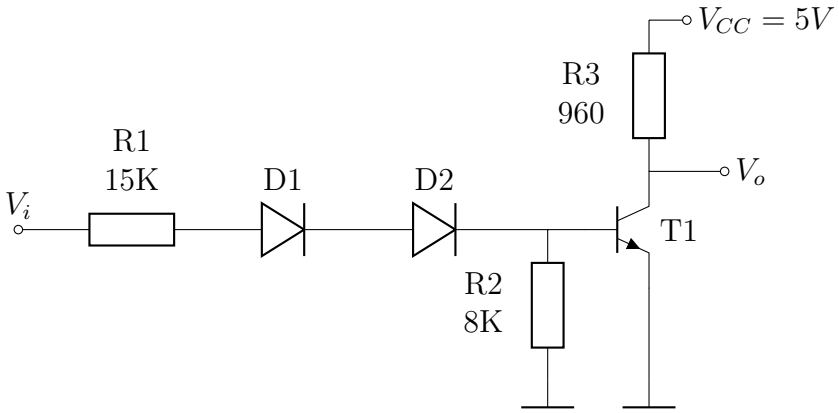


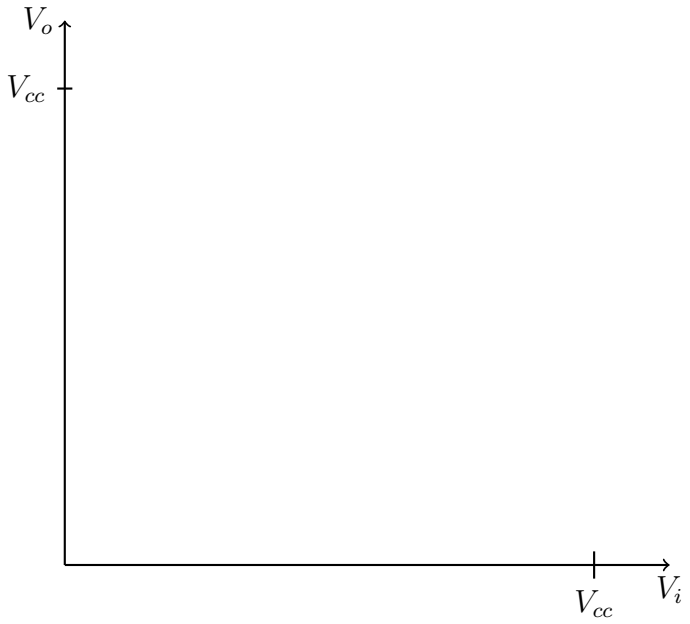
Plot the output signal for the following circuit and calculate the moments when the output signal crosses $0.1V_{cc}$ and $0.9V_{cc}$ (if they do), relative to the input signal edges. Assume $V_{cc} = 5V$. The duration of the input pulse is long enough for all the voltages to stabilize.



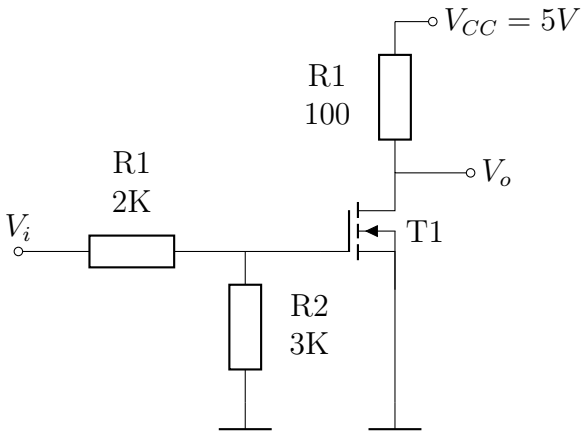
For the digital gate below, please determine the static dependency $V_o(V_i)$. Calculate $V_{OL}$, $V_{IL}$, $V_{IH}$, $V_{OH}$, $MZL$, $MZH$. Calculați factorul de supracomanda pentru T1. Se cunosc $U_D = 0.6V$, $U_{BE} = U_{BE0} = 0.8V$, $U_{CEsat} = 0.2V$, $\beta = 100$.



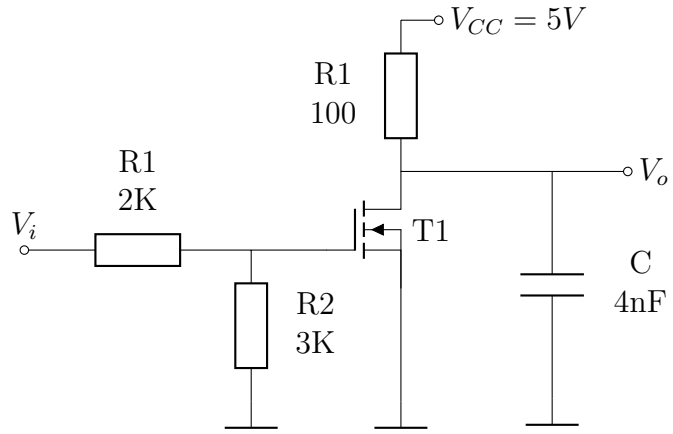
In the circuit below, assume the simplified Resistor-Saturation model for the MOSFET transistor, with $K = 0.1A/V^2$ and $V_T = 1V$.

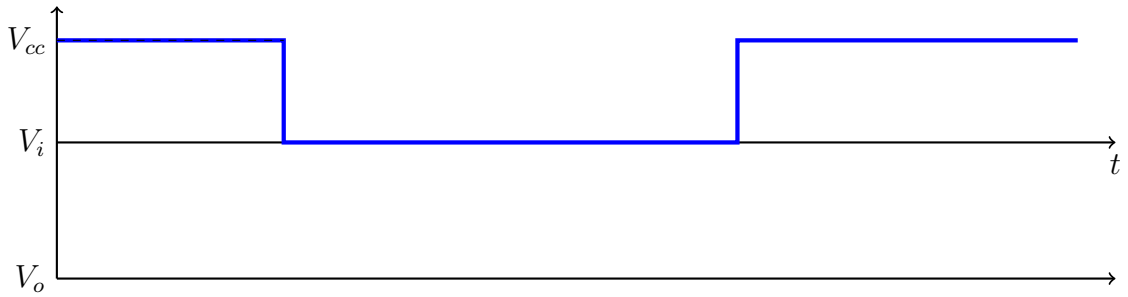
1. Calculate $V_i$ such that the MOSFET is both in the linear region and in the saturation region
2. Calculate the $V_o$ for the following cases:
   (a) $V_i = 2V$
   (b) $V_i = 5V$



Plot the output signal for the following circuit and calculate the moments when the output signal crosses $0.1V_{cc}$ and $0.9V_{cc}$ (if they do), relative to the input signal edges. Assume $V_{cc} = 5V$. The duration of the input pulse is long enough for all the voltages to stabilize.

Assume the simplified Resistor-Saturation model for the MOSFET with $K = 0.1A/V^2$ and $V_T = 1V$. Ignore the input capacitance of the MOSFET.



Design a CMOS circuit which implements $\overline{A}B \vee C$. All variable represent digital input signals. The only components you are allowed to use are MOS transistors. Try to minimize the number of transistors used. Explain briefly your design and how it works.