MediaTek
HSPA Smartphone Solution

MT6573 / MT6513 (2G)

Design Notice V1.4

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Revision History

Rev.	Date	Author	Description
V0.1	2011.01.13	CK Cheng	First version release and pre-release
V0.2	2011.01.26	CK Cheng	Modify Download, PMU, audio, speech, LCM, MT6620 part
V0.3	2011.02.16	CK Cheng	Modify P.27 Bootrom USBDL Trigger Criteria. Modify P.37 FsourceP bootstrap description . Add P.55 for VDDK_DVFS cap. Modify PMU P.149, P.150 typo. Add VPA ground design notice. (P116)
V0.4	2011.04.28	Jerome Chen	1. Add UART IO voltage description on P.35 2. Correct GPIO176 power domain to DVDD_NML on P.61 3. Add power inductor selection guide and QVL on P.117~118 4. Correct LCM RGB SPI IF pin definition on P.192
V0.5	2011.05.12	Jerome Chen	1. Modify UART IO voltage description on P.35 2. Add LCM CPU IF timing constraint on P.192
V0.6	2011.05.24	Jerome Chen	1. Delete MT6620 Combo Module Application note (Please refer to MT6620 design notice) 2. Update Touch Panel Hardware Application Note on P.233~246
V0.7	2011.06.11	Jerome Chen	1. Update High Speed Memory Layout Rule(LPDDR) on P.63~89 2. Update VPA power inductor selection guide and QVL on P.117~121 3. Update MSDC layout guide on P.235
V0.8	2011.06.13	Jerome Chen	1. Update VPA power inductor selection guide and QVL on P.117~120
V0.9	2011.07.01	Jerome Chen	1. Update VPA power inductor, diode, and capacitor selection guide on P.117~121 2. Update BC1.1 design notice on P.144~147 3. Update Audio design notice on P.179~184
V1.0	2011.08.25	Zhiyong jia	1. Add MIPI LCM power connection guide on P.192 2. Add MCLK for Camera MIPI connection on p.200

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Revision History

Rev.	Date	Author	Description
V1.0	2011.08.25	Zhiyong jia	3. PMU part, modify VPA output component on p.95 4. Update charging design notice on p.126~P.133 5. Add Gas Gauge customer support model on p .145 6. Add Gas Gauge Layout guide on p.149
V1.1	2011.09.25	Zhiyong jia	1. Add Emmc design notice and remove SDIO2 mux and SDIO3 on p.226 2. Add eMMC application circuit on p230~p232 3. Modify layout guideline on p233 4. Add eMMC 153b & 169b package compatibility on p234 5. Add speaker pseudo input to avoid TDD on p180 6. Update BC1.1 mixed unify flow on P.139
V1.2	2011.11.01	Zhiyong jia	1. Modify eMMC application circuit on p235~p236 2. Del Audio application notice on original p170, p184~p185 3. Add ACCDET with EINT solution on p183~p187 4. Add Gauge design guide on p146
V1.3	2011.12.05	Zhiyong jia	1. Add VDDK_MDVFS bypass cap layout rules with highest priority on p.116
V1.4	2012.01.05	Zhiyong jia	1.Remove Power management part on p15 & p16 2.Modify sub camera direction on p205

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Outline

- MT6573 Introduction
  - General description, block diagram
  - Firmware upgrade, image layout, engineer mode
- MT6573 Hardware Design Notice
  - Bootstrap, pin-mux, schematic notice
  - High speed memory layout rule
  - Power management unit
  - Audio / speech
  - USB / MSDC
  - Peripherals: touch panel / sensors
- Case Study

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Strength of MT6573 Smartphone Platform

Dual SIM

One-stop Service: Analog TV BT/FM/Wi-Fi/GPS

Video Telephony

FWVGA Video Playback
Video Streaming

Full HTML Browser Better Performance

MT6573

ARM11 650 MHz AP
Rel. 6 HSPA Modem
Integrated PMIC

8M Camera

FWVGA Video Record
Face Detection / Smile Shot

3D Acceleration

Launcher , Live Wallpaper
Gallery, Games

Tier 1 Performance

Audio/Speech/Modem
Low Power

Turnkey Solution

Android latest version
IOT, FTA, CTS 100% Pass

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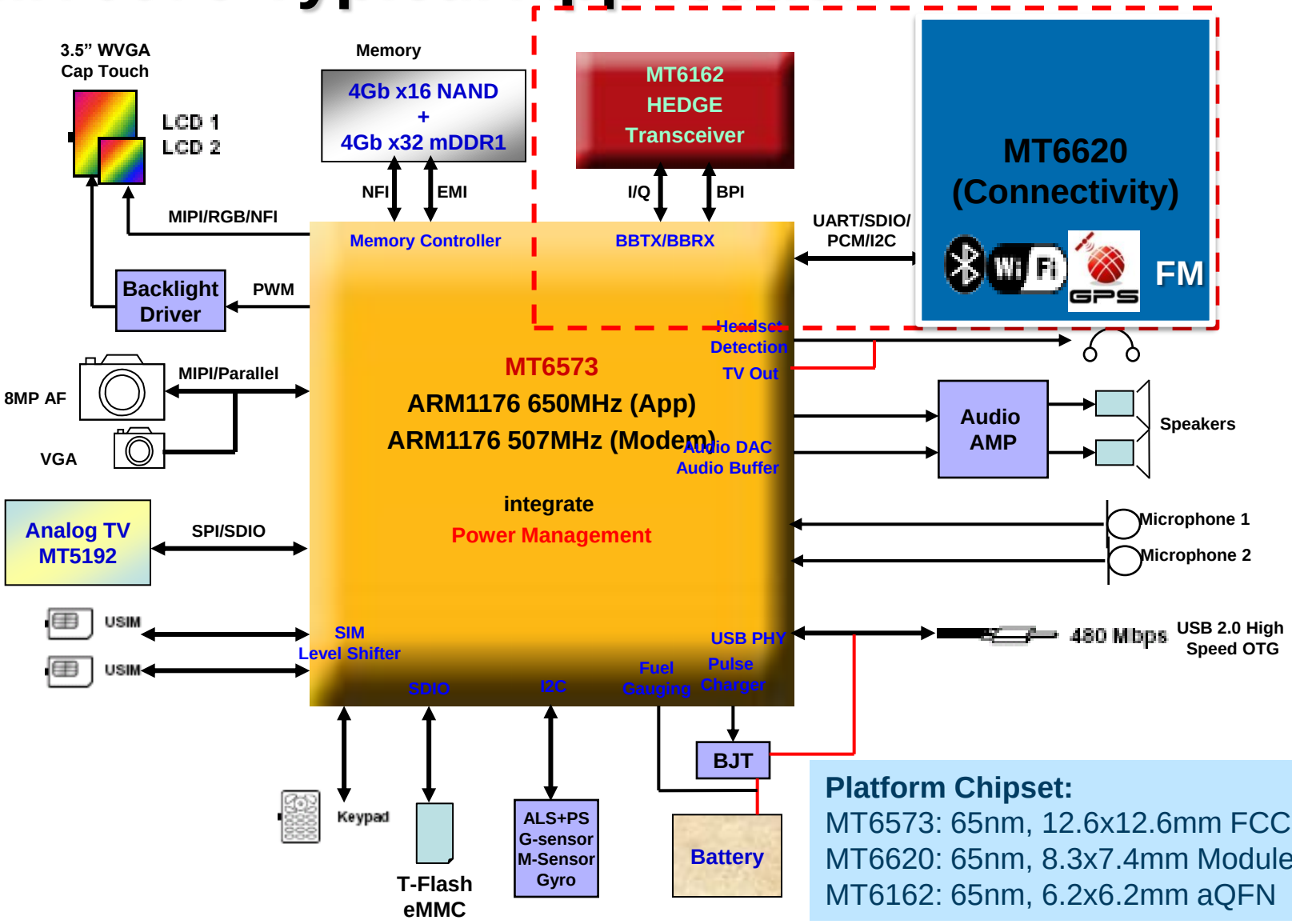
MT6573 Typical Application



Platform Chipset:

MT6573: 65nm, 12.6x12.6mm FCCSP
MT6620: 65nm, 8.3x7.4mm Module
MT6162: 65nm, 6.2x6.2mm aQFN

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MT6516 / MT6573 Feature Comparison

	Mediatek MT6516	Mediatek MT6573
Package	15x15mm 564-pin, BGA, 0.5mm, 65nm	12.6x12.6mm 518 balls, BGA, 0.4mm, 65nm
Apps Processor	ARM926EJS@ 416 MHz w/ 32KB/32KB I/D cache	ARM1176JZFS@ 650 MHz w/ 32KB/32KB I/D cache 128KB L2, DVFS support
Modem Processor	ARM7EJ-S @ 104 MHz , 104MHz DSP	ARM1176JFS@ 507 MHz, 280MHz DSP
Modem	GPRS, EDGE class12	EDGE class12, HSDPA Cat8 7.2Mbps, HSUPA Cat6 5.76Mbps
Memory	104MHz-mDDR, 128MB x 4, NAND (NFI)	200MHz-mDDR, 256MB x 4, NAND (NFI)
Camera / TV-out	5MP Bayer/YUV, 10bit parallel, MIPI CSI-2	8MP Bayer/YUV, 10bit parallel, MIPI CSI-2 CVBS TV out
Display	WVGA, 24-bit color, MIPI DSI, CPU/RGB I/F	FWVGA, 24-bit color, MIPI DSI, NFI, CPU/RGB I/F
Audio	64-Poly, MP3,AAC,HE-AAC, WMA,G.711,G.723.1,G.729,AWB+,3D effect	64-Poly, MP3,AAC,HE-AAC, WMA,G.711,G.723.1,G.729,AWB+,3D effect Dual mic, Digital mic support
Video Decode	MPEG4/H.264: D1 @ 30fps	MPEG4/H.264: FWVGA @ 30fps
Video Encode	MPEG4: D1 30 fps	MPEG4: FWVGA @ 30fps, H.264 CIF @ 30fps
Video Telephony	NA	3G-324M: QCIF 15 FPS, 64kbps
Video Streaming	QVGA Video Streaming	MPEG4/H.264 to D1, 30 fps
Peripherals	UARTx4, SIMx2, R-touch, PCMx1, I2Sx2, I2Cx3, SPIx1 SDIOx3, Key Matrix 8x8 USB 2.0 HS OTG int. PHY x 1	UARTx4, SIMx2, R-touch, PCMx1, I2Sx2, I2Cx2, SPIx1 SDIOx4 , Key Matrix 8x8 USB 2.0 HS OTG int. PHY x 1, USB FS host x 1
Power Management	External PMIC MT6326	Integrate PMU, 5 bucks, 20 LDOs, LED driver, pulse charger, gas gauge

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MTK HSPA Smartphone Feature Overview

HSPA Smartphone Platform:

MT6573 + MT6162 + MT6620

MT6573 Features:

- App. Processor: ARM1176JZF-S **650 MHz**
  - Dedicated 32KB I-Cache and 32KB D-Cache
  - DVFS 1.0 ~ 1.35V, step 25mV support
  - ARM™ TrustZone® Security
- Modem Processor: ARM1176JZ-S **507 MHz**
  - HSDPA, Downlink 7.2Mbps (Category 8)
  - HSUPA, Uplink 5.76Mbps (Category 6)
  - UMTS Band 800/850/900/1700/1900/2100/AWS
  - EDGE Qual-Band 850/900/1800/1900
- PMU/R-touch panel driver integrated
- Supports up to FWVGA (864x480) LCM
  - 24bit CPU/RGB IF, 2-lane MIPI DSI I/F
- MFlexVideo driven multimedia engine
  - MPEG-1/2/4, DivX, H.264, VC1/WMV9 **FWVGA 30fps decode**
  - MP4/H.263 FWVGA 30fps encode.
  - QCIF Video Telephony
- Camera ISP: 8MP
  - MIPI/Parallel I/F, EIS, face detection
- Advanced DSP acoustic functionality
  - AEC and noise reduction
- Supports QWERTY keypad
- Multi-memory system with more flexibility for phone design, which supports
  - NAND-boot , eMMC boot
  - NAND data storage
  - LPDDR SDRAM 200MHz
- Integrate DC couple headphone driver
- Integrate dual microphone / digital microphone I/F
- Integrated fuel gauge.
- Supports SD, MMC, Memory Stick, Memory Stick Pro, SDIO cards
- Supports dual SIM
- Built-in USB 2.0 (High-speed/OTG), IrDA
- Package size: 12.6x12.6 mm^2 , 518 balls TFBGA with 0.4 mm pitch

Hardware Function Configuration

Basic blocks

AP+MD BB (MT6573)	2G+3G RF (MT6162)	WiFi+BT+FM +GPS (MT6620)	Audio Amp BL Driver	LCM FWVGA
USB 2.0 High Speed OTG	Memory card MMC/SD	R-type Touch Panel	Dual SIM	Memory NAND / DDR

Optional blocks

Dual Microphone	C-type Touch Panel	Dual Camera VT call	E-Campass	IrDA
ATV (MT5192)	CMMB MBBMS	Proximity /Light Sensor	Motion Sensor	Gyroscope

- **MediaTek IC**
- **Built-in MediaTek BB IC**
- **External IC** (Decided by customers)
- **External IC** (Qualified list provided by MTK)

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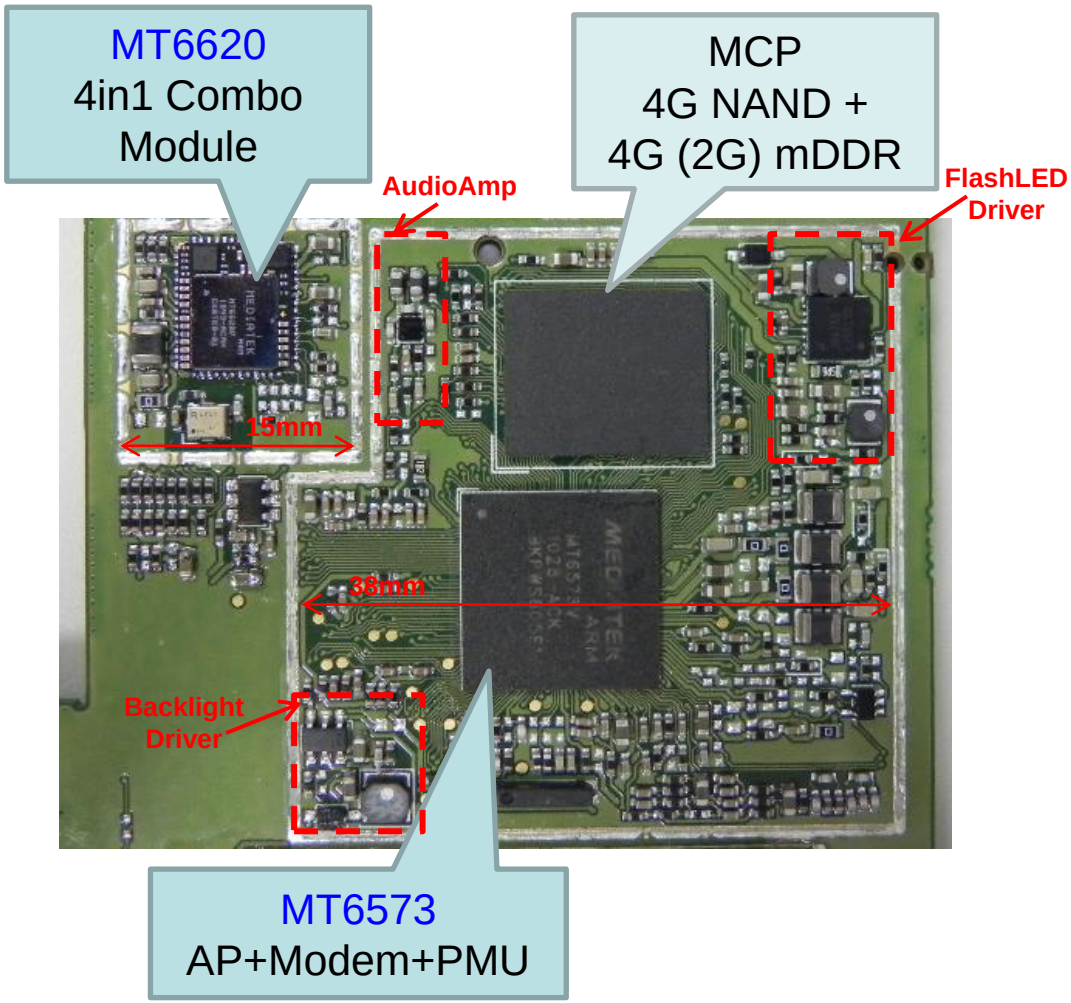
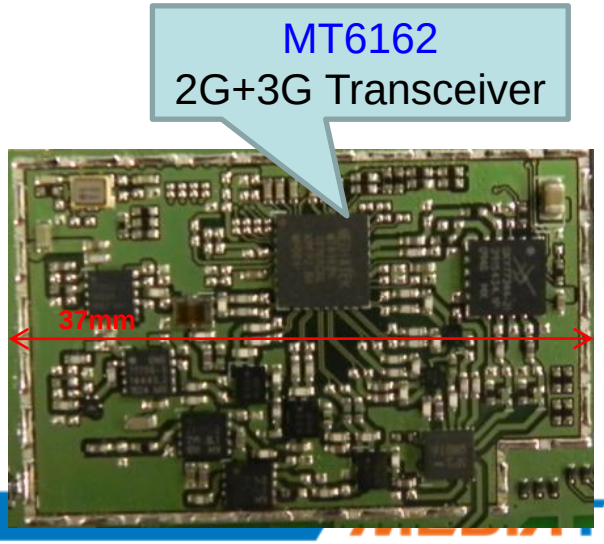
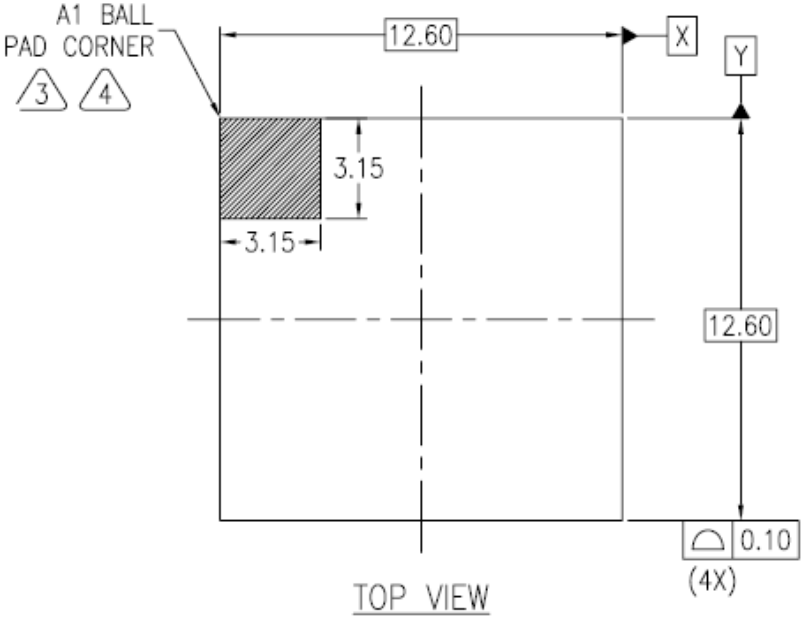
PCB Snapshot (6L HDI1)

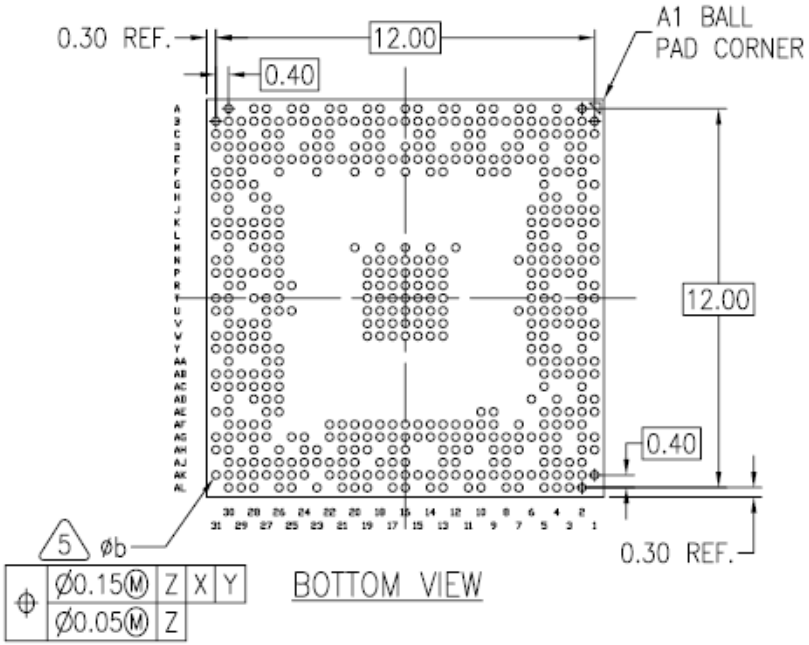


- 6 layer (1-4-1) design to reduce cost and PCB manufacture time.
- 0402 components used.
- Baseband core placement area <1300 mm^2
- Connectivity core placement area < 225mm^2
- RF placement area < 800mm^2 (4+4 band)



MT6573/MT6513 Package





Body Size		Ball Count	Ball Pitch		Ball Dia.	Package Thk.
X	Y	N	eE	eD	b	A (MAX)
12.6	12.6	518	0.4	0.4	0.3	1

Outlines and Dimension of FCCSP 12.6mm*12.6mm, 518-ball, 0. 4 mm pitch Package

Please refer to our "SMT Application Notes" for 0.4mm pitch BGA SMT yield improvement

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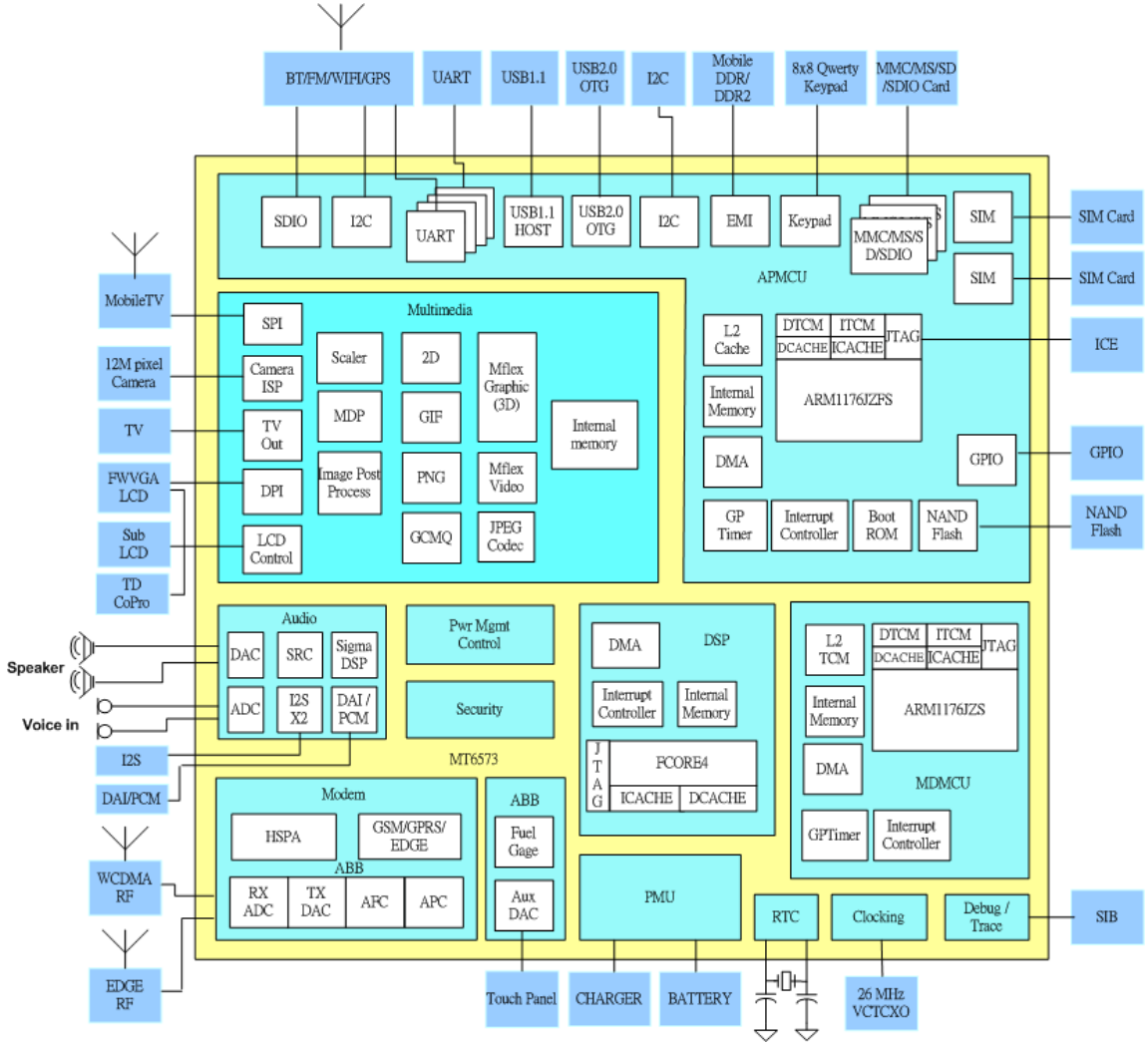
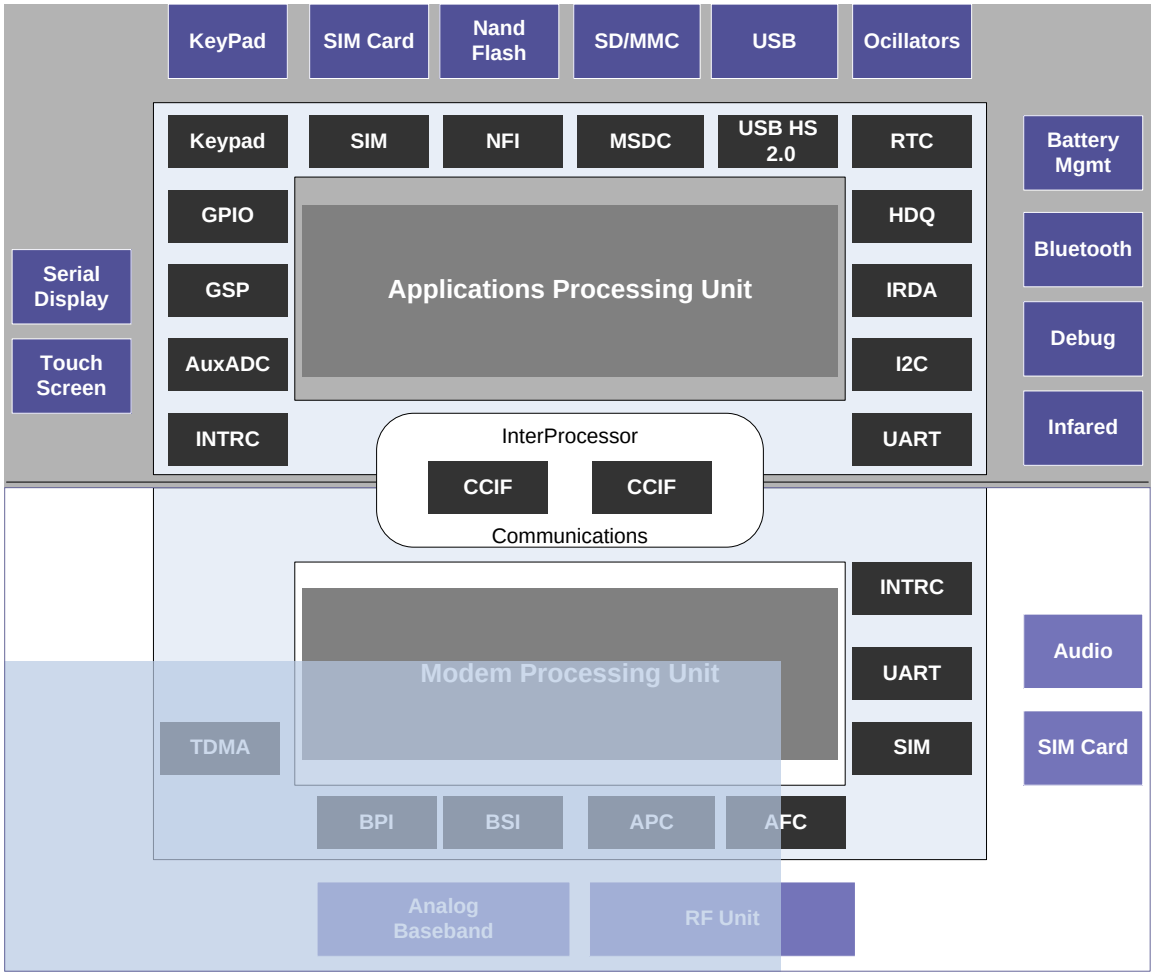
MT6573 SoC Block Diagram



Inter-Processor Communication

AP Peripherals

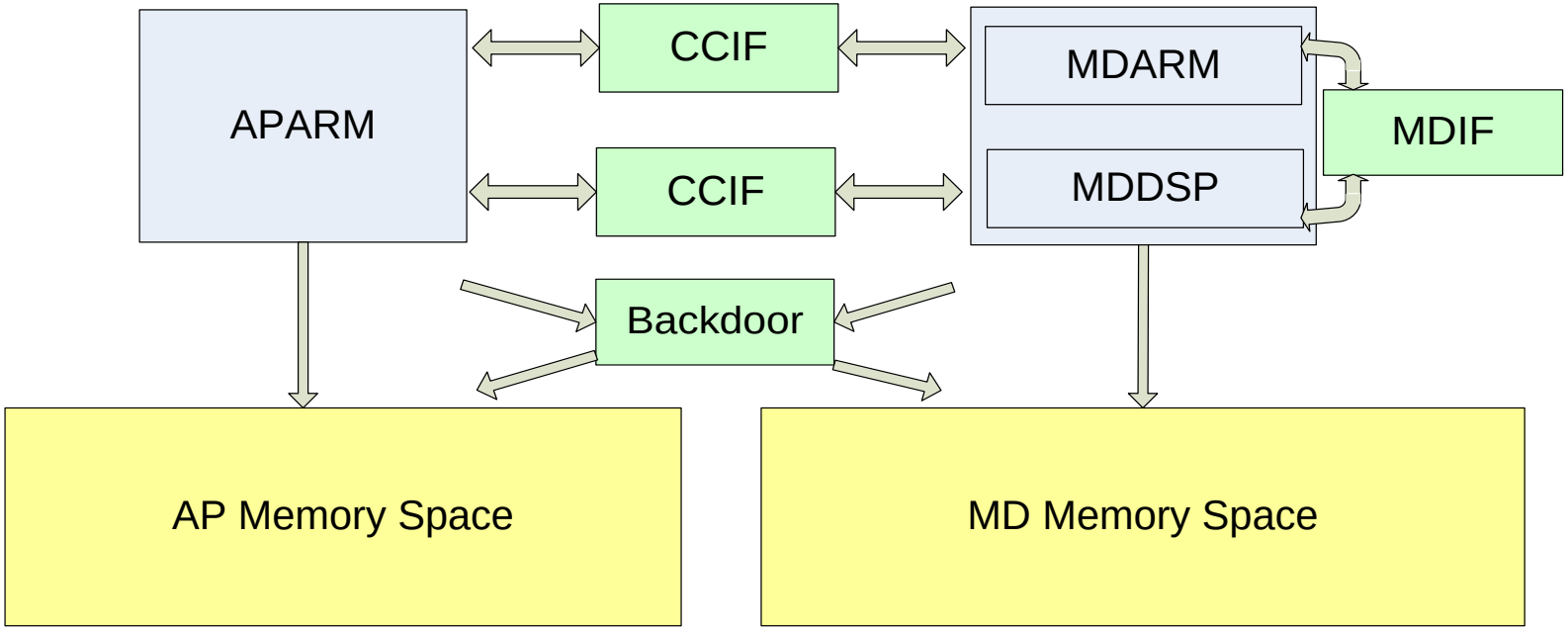
- ACCDET
- AP_DMA
- AUXADC
- CCIF
- CIRQ_EINT
- EFUSEC
- GPTIMER
- HDQ_ONE_WIRE
- I2C
- IRDA_FRAMER
- KP
- LMU
- MSDC
- NIF
- OSTIMER
- PWM
- RGU
- RTC
- SEJ
- SIMIF
- TOPSM
- TRNG
- UART
- USB11, USB20



MD Peripherals

- AFC
- CIRQ_WOE
- DIVIDER
- DUAL_BPI
- DUBL_BSI
- GPTIMER
- LMU
- LOG_ACC
- MDIF
- MD_DMA
- OSTIMER
- PFC
- TDMA
- WCDMA_TIMER

Inter-Processor Communication



- CCIF & MDIF
  - Inter-core communication
  - Used for message passing, data pointer passing and interrupt initiating
  - Backdoor can't do it
- Backdoor
  - Inter-memory space communication
  - A mean for AP/MD to see the entire MD/AP memory space
  - CCIF & MDIF can't do it

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MT6573 Firmware Download

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NAND Partition Layout for Android (1/2)

- **Pre-loader**
  - Pre-loader image
  - Handles all the download and secure boot procedures
- **U-boot**
  - Second loader image
  - Handles most hardware initializations and bring-up entire Linux kernel
- **Boot**
  - Linux kernel image and it's root file system
- **Recovery**
  - Recovery kernel image and it's root file system
  - Handles all the system recovery and firmware update functionalities
- **System (Android)**
  - Android system image
- **Logo**
  - Boot-up logo image

Index	Partition	Type
1	PRELOADER	Raw data
2	NVRAM	YAFFS2
3	SECCFG	Raw data
4	UBOOT	Raw data
5	BOOT	Raw data
6	RECOVERY	Raw data
7	SECSTATIC	YAFFS2
8	MISC	Raw data
9	SYSTEM	YAFFS2
10	CACHE	YAFFS2
11	LOGO	Raw data
12	APANIC	Raw data
13	USER	YAFFS2

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NAND Partition Layout for Android (2/2)

- **NVRAM**
  - Stores the hardware related information, such as calibration data, MAC address, IMEI … etc.
- **Cache**
  - For Android internal used
  - Store Android internal cache data or web cache data
- **Misc**
  - Used for the recovery procedure (power loss)
- **User**
  - Used for Android system to store user data such as user contacts, settings, installed applications … etc.
- **SECCFG and SECSTATIC**
  - Reserved for the security platform used
- **Apanic**
  - Used to store the kernel panic debug messages

Index	Partition	Type
1	PRELOADER	Raw data
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8	MISC	Raw data
9	SYSTEM	YAFFS2
10	CACHE	YAFFS2
11	LOGO	Raw data
12	APANIC	Raw data
13	USER	YAFFS2

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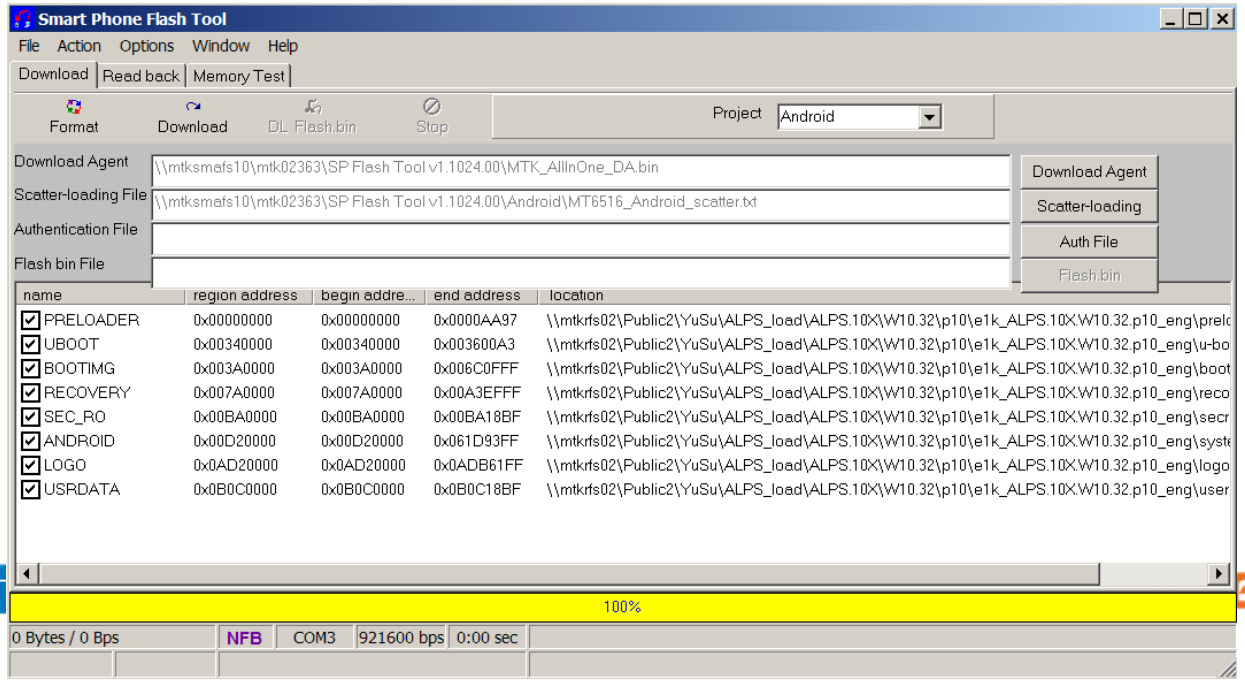
Software Package Download

- **Download Ports**
  - UART1 / USB FS: DA / pre-loader image download
  - USB HS: U-Boot, boot, recovery, sec_ro, system, logo, user data images download
- **Download Agent**
  - The agent on target to perform the download procedure upon tool request
- **Scatter-Loading File**
  - Describe the start address of each partition to download to



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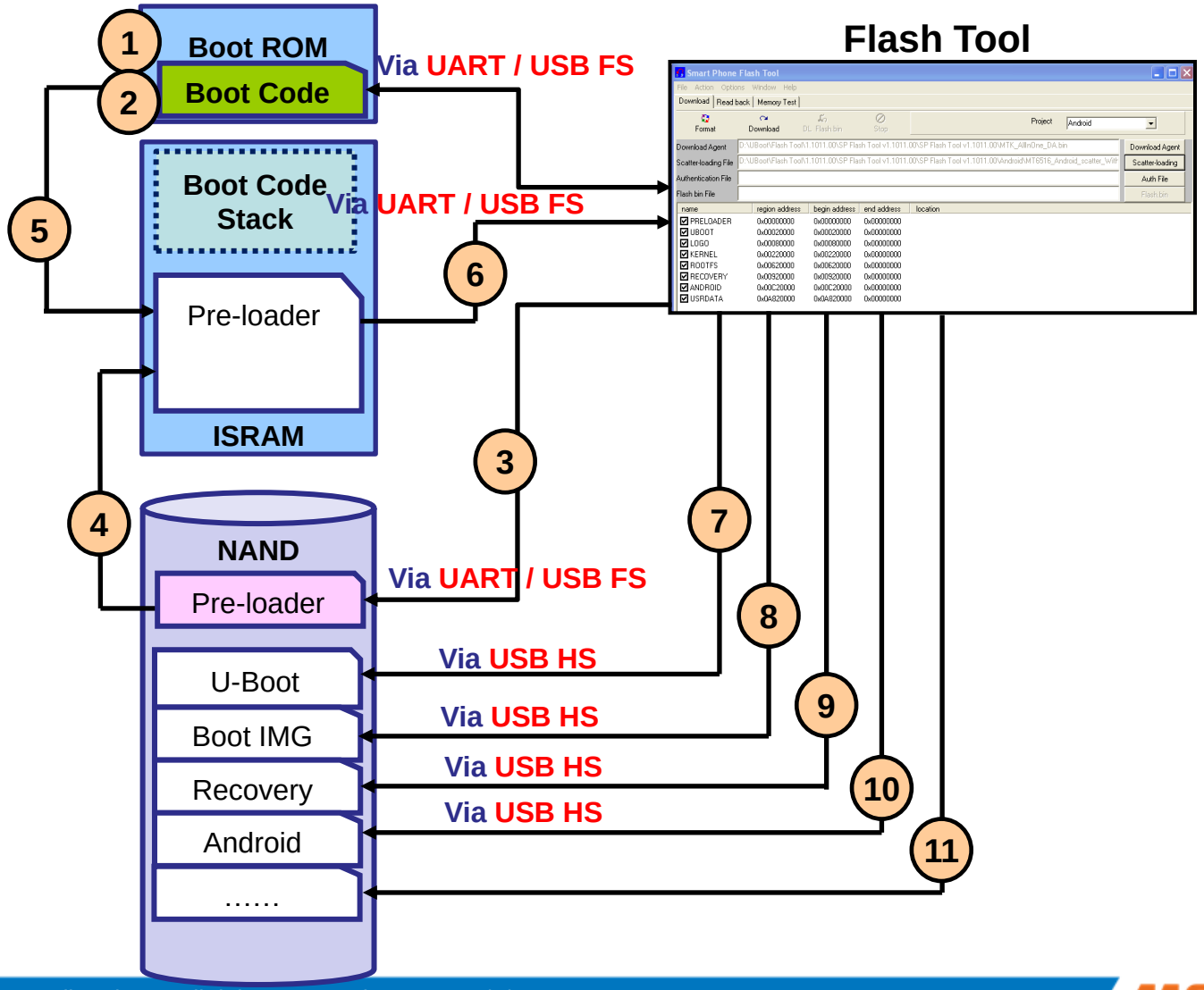
Software Package Download



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USB Download Feature Introduction

	MT6516	MT6573
Format NAND Flash	UART1	UART1 / **USB FS**
Download DA / Pre-Loader	UART1	UART1 / **USB FS**
Download Bootloader / Image	USB HS	USB HS
USB Download w/o Battery	X	**O**

- Format NAND Flash
  - Format command between bootrom and flashtool.
- Download DA / Pre-Loader
  - Loading download agent to internal SRAM and flash pre-loader to NAND.
- Download Bootloader / Image
  - Bootloader and OS image download to NAND flash.
- USB Download w/o Battery
  - Target can perform USBDL without attaching battery. (Using VBUS power from USB)

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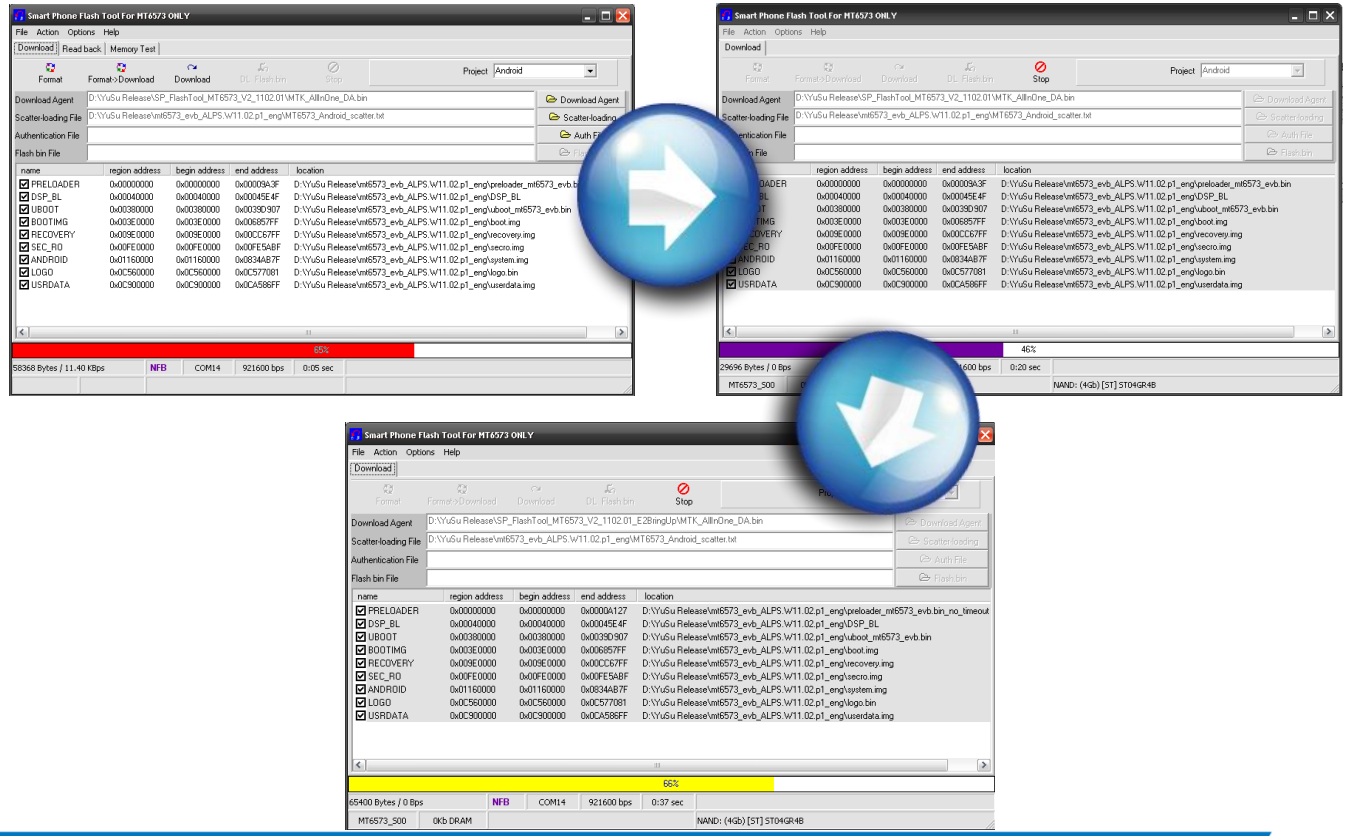
Download Procedure

- Red progress bar: Downloading DA through BootROM.
- Purple progress bar: Downloading preloader through DA.
- Yellow progress bar: Downloading other images through preloader.



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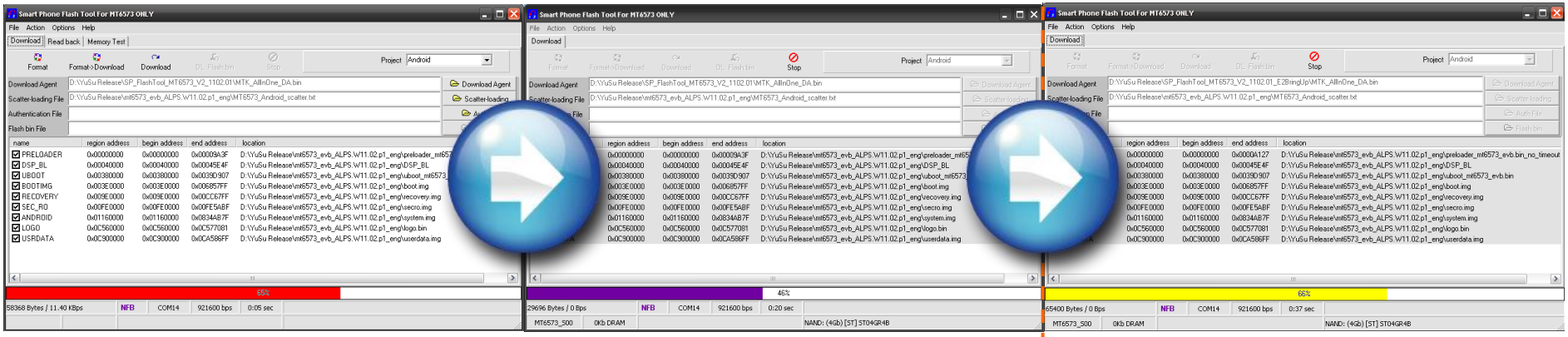
Download Methods

- 1ST and 2nd stage supports USB download from 6573 E2.
- 6573 E2 supports both UART and USB download in 1st and 2nd stage.

1st and 2nd stage: UART/USB

3rd stage USB



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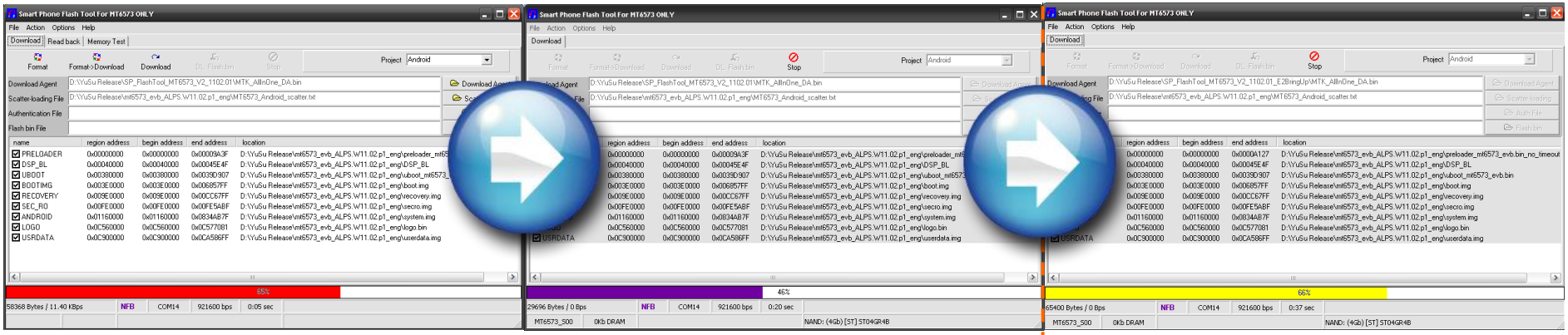
BootROM USB Auto-Detection Mechanism

- BootROM will initialize USB if charger is detected and wait for a configurable time until timeout.
- Timeout is default 30s, and can be overriden by preloader header settings.
- Current preloader timeout settings is 0s, that is, USB will not be initialized.
- Timeout will be 30s if preloader is absent, and will be 0s if preloader is present.

1st and 2nd stage: UART/USB

3rd stage USB



Will enter USBDL mode automatically when power on with USB cable connected and preloader not present.

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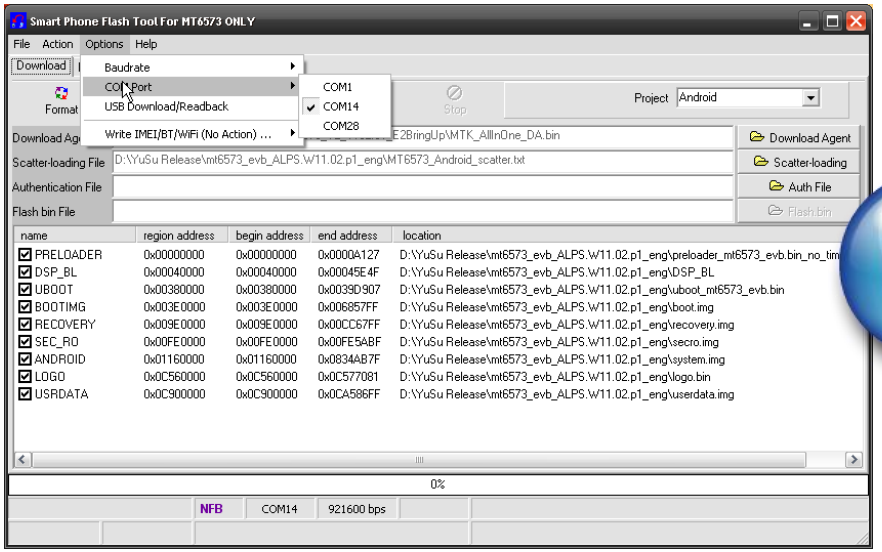
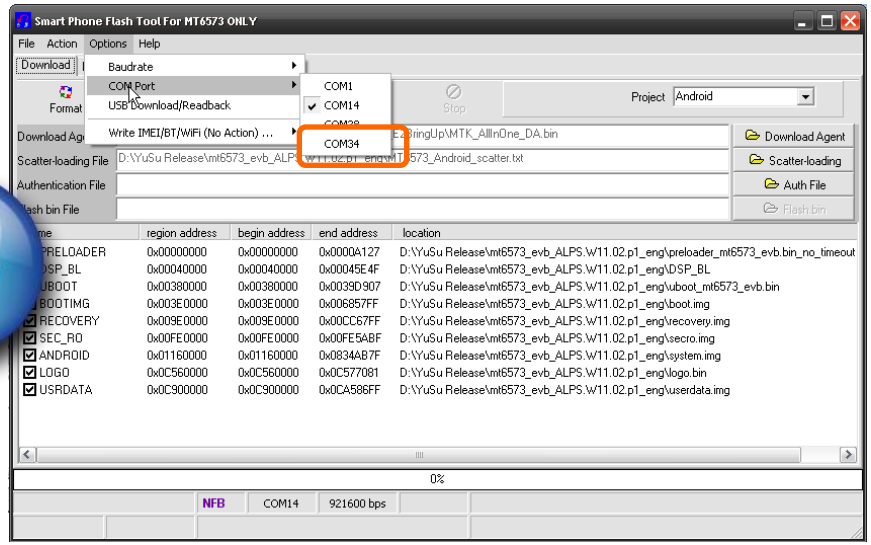
Download Method(USBDL)

- Power on with USBDL key pressed and USB cable not connected.
- Connect USB cable to PC then a new COM port will appear.
- Choose the COM port and press “Download” to start downloading.





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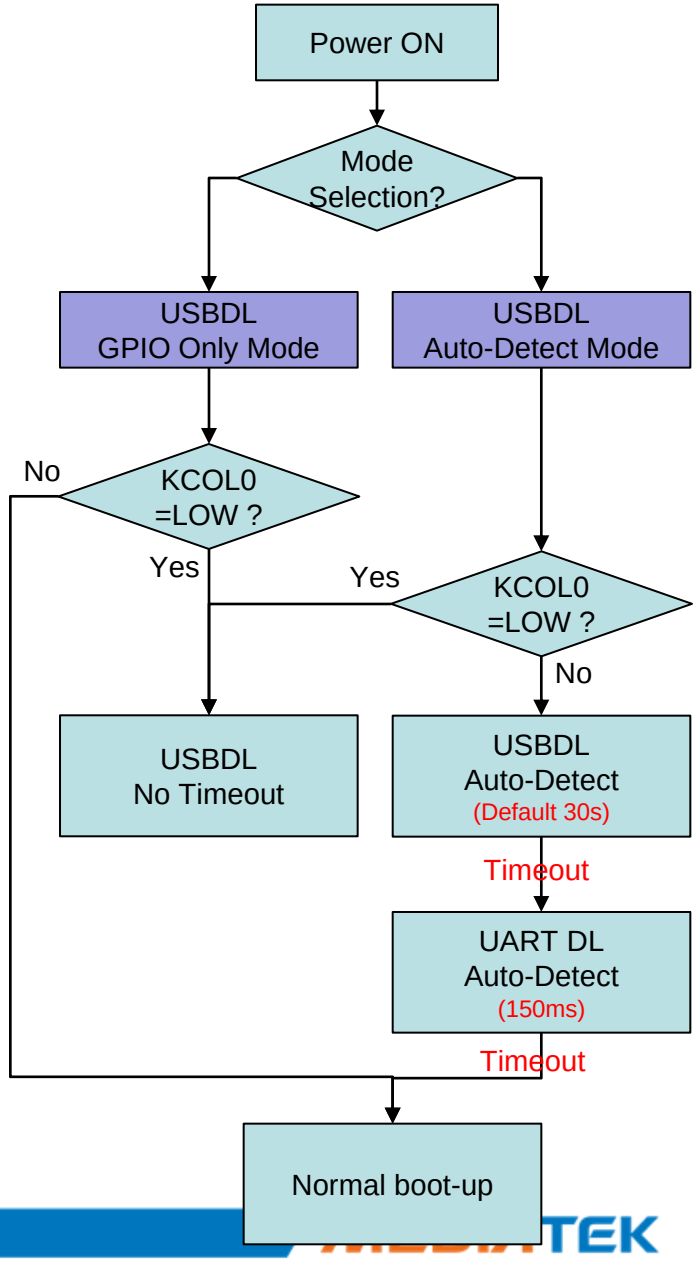
Bootrom USBDL Flow

- How to enter bootrom USB download mode?
  - Auto-Detect Mode (default setting)
  - GPIO Only Mode (key matrix KCOL0 tie to GND)

- Bootrom USBDL mode selection is according to EFUSE setting by default
  - Default is auto-detect mode with 30s timeout
  - Boot-loader's configuration can override this setting



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Bootrom USBDL Trigger Criteria

	USB Cable	USBDL w/o Battery	USBDL No Timeout	USBDL Auto-Detect
KCOL0=LOW	Plugged	Activated	Activated	X
KCOL0=LOW (By shorting KCOL0 and KROW0)	Plugged	Activated	Activated	X
Other condition	Plugged	X	X	Activated
Other condition	Un-Plugged	X	X	X

- As long as KCOL0=LOW, target enters USBDL mode without timeout
- Native USBDL w/o Battery can only be triggered by KCOL0 + KROW0
- If KCOL0=HIGH and USB cable is not plugged in, Native USBDL Auto-Detect will be skipped

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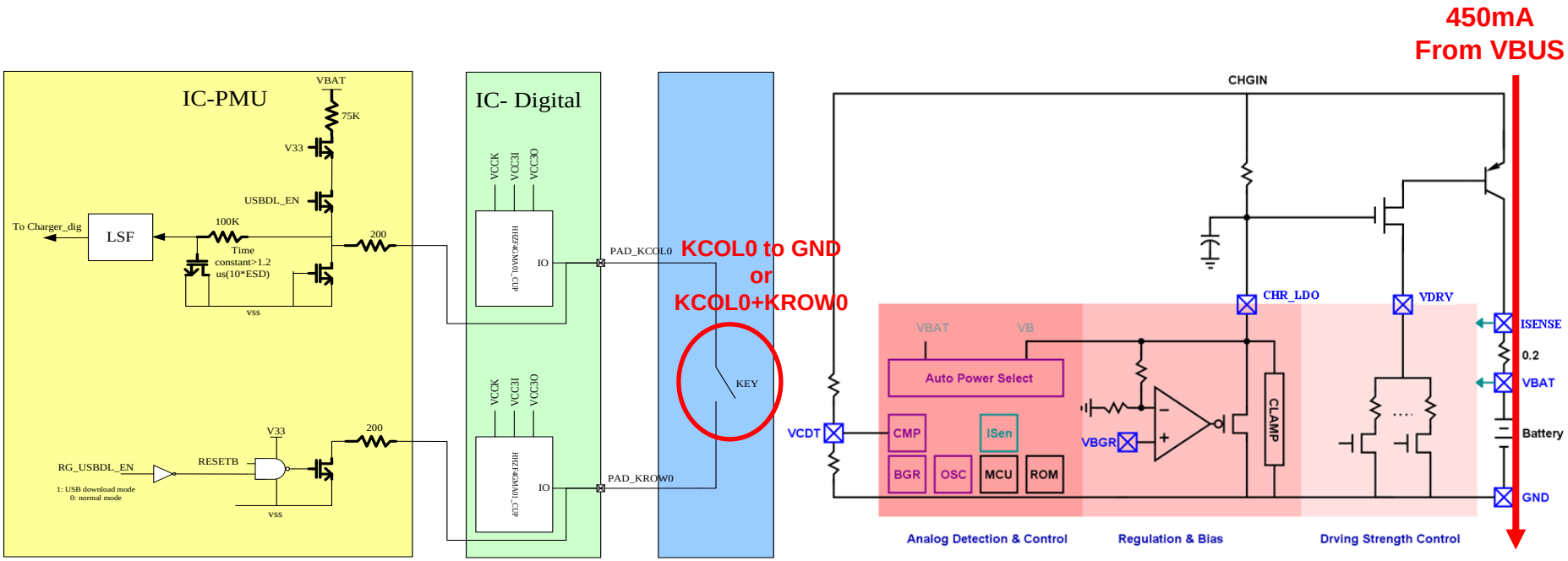
Force Charger Mode for USBDL

- Set charger to 450mA (0.2 ohm Rsense) when detect DL key pressed (KCOL0+KROW0, or KCOL0 to GND). Use this power (USB port) as source in factory D/L stage.
- If false triggered, software can disable this function when detect in normal power on.
- 8 seconds timeout for security concern.

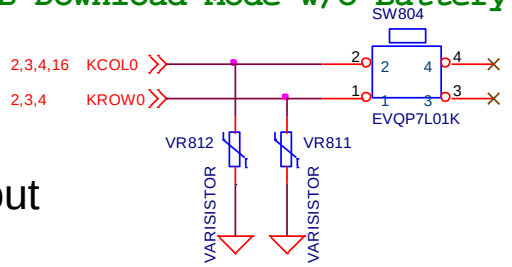


Application Scenarios

- KCOL0 and KROW0 as on board key switch (usually side key, camera or volume up/down)
  - Can enter USBDL and USBDL w/o battery without test fixture on PCBA stage or assembly done.
  - User may enter this mode occasionally. (prevent by timeout setting)

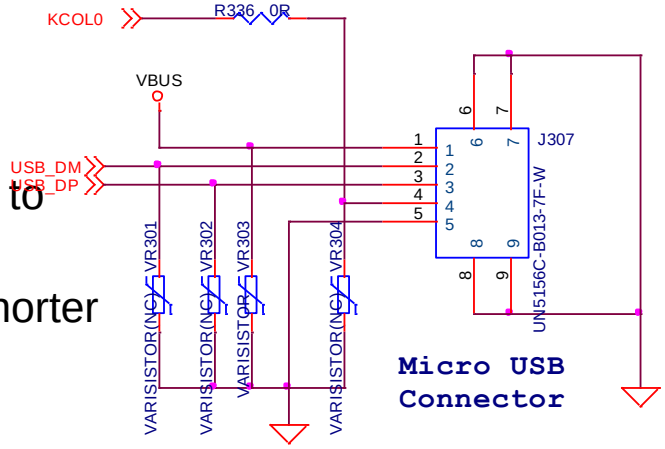
Function Key

USB Download Mode w/o Battery



- KCOL0 as test point.
  - Test fixture needed.

- KCOL0 connect to USB connector ID pin
  - Use special cable for production line. (ID pin short to ground)
  - Use OTG cable will boot-into USBDL mode (set shorter timeout)
  - Con only use on non-OTG project.



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Customization Settings (by request)

- Pre-Loader
  - Auto detection mode timeout. (default is 30s)

- EFUSE (By Request)
  - Mode select: disable auto detect mode.
  - PID / VID – Can customize USB PID/VID in bootrom USB driver by Efuse.

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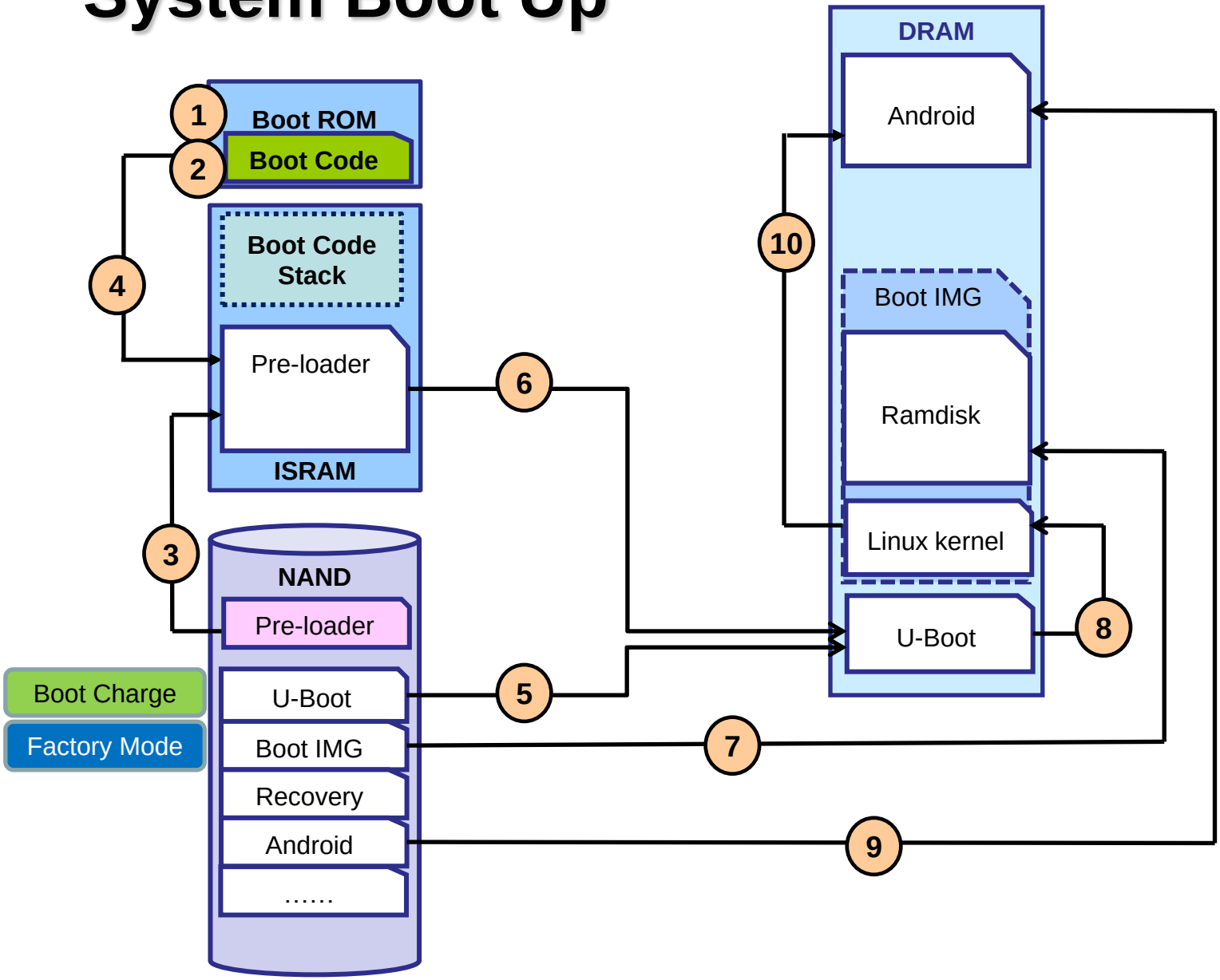
System Boot Up



Confidential B

MT6573 Factory Mode & Engineer Mode Notice

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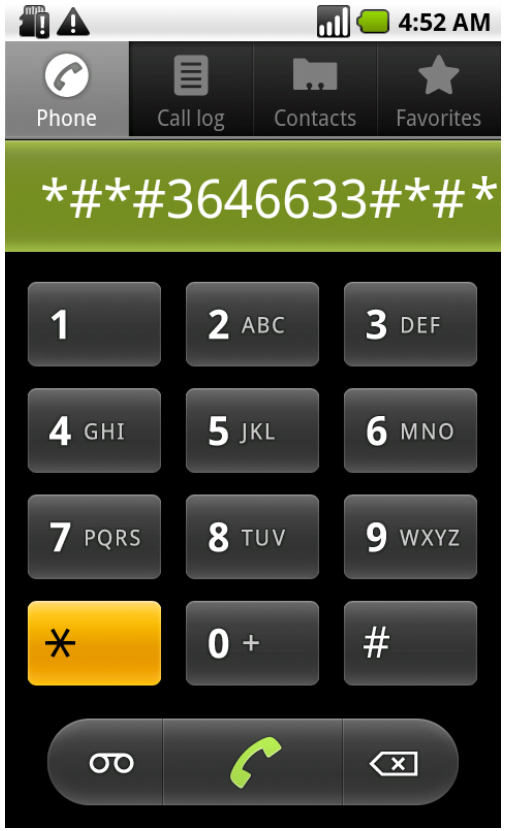
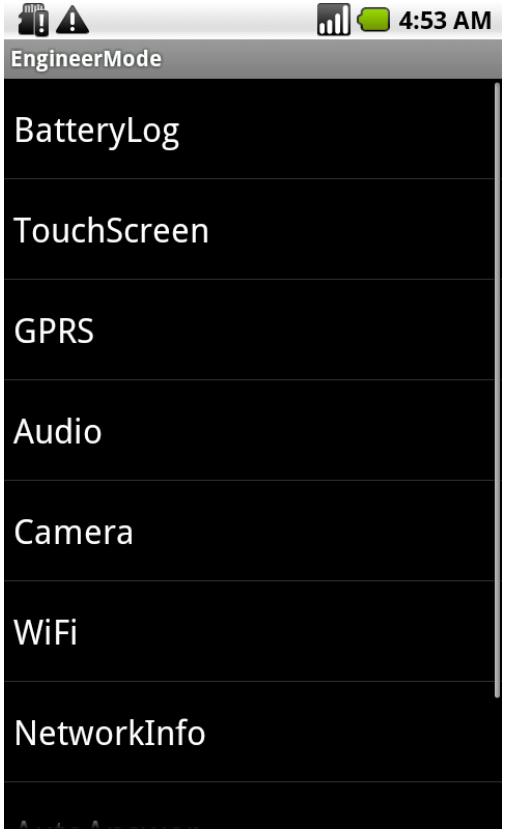
Engineering Mode in Android 2.x

– Enter phone menu and then dial ***#*#3646633#*#***





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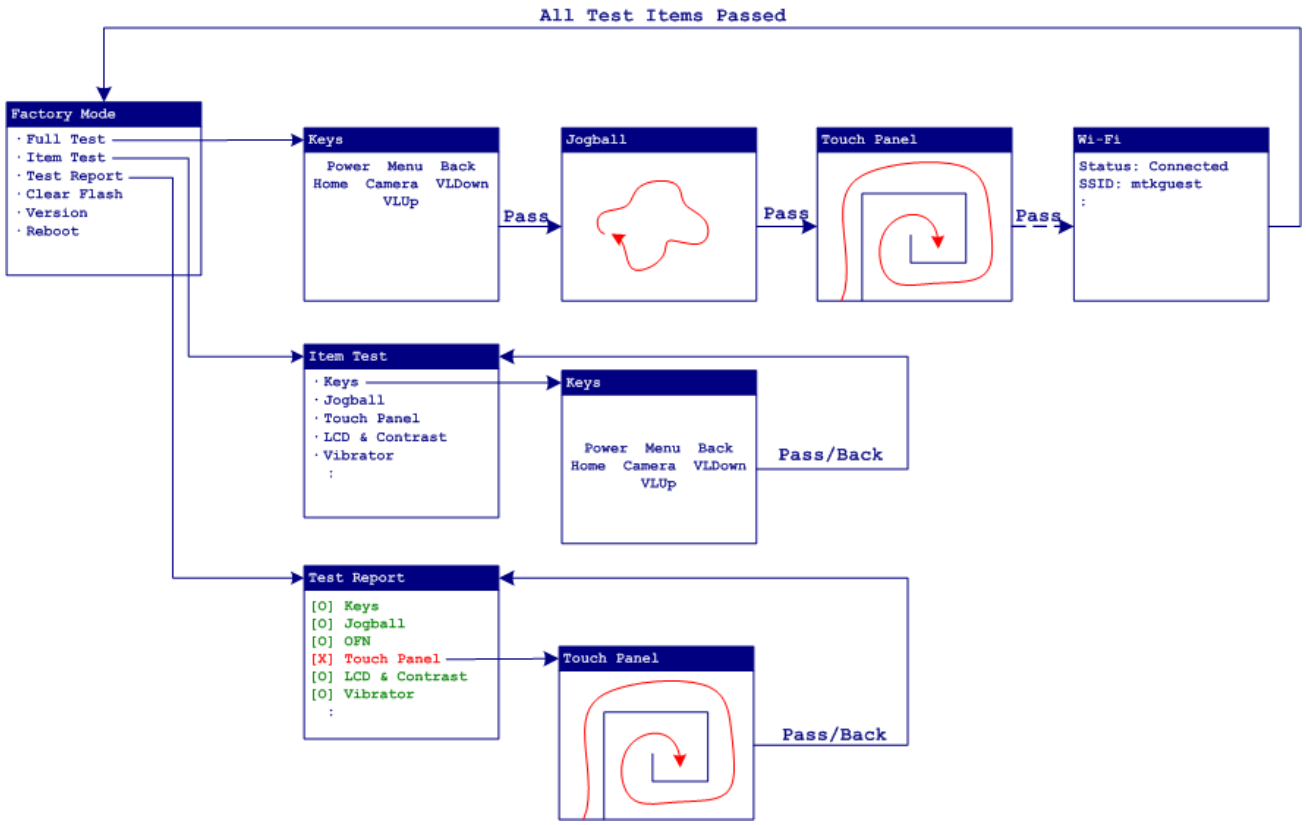
Factory Mode in Android 2.x

- Press **volume down key** + **power key** to boot up



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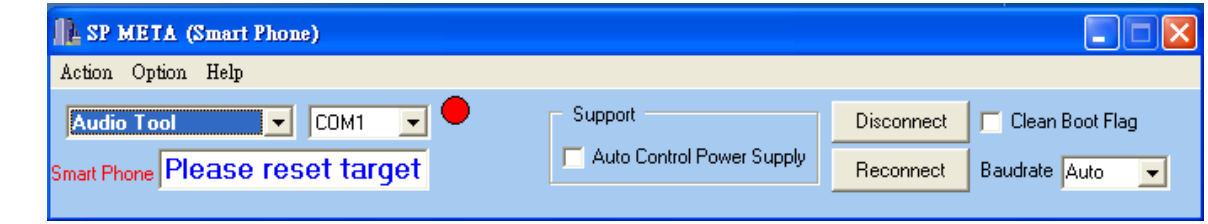
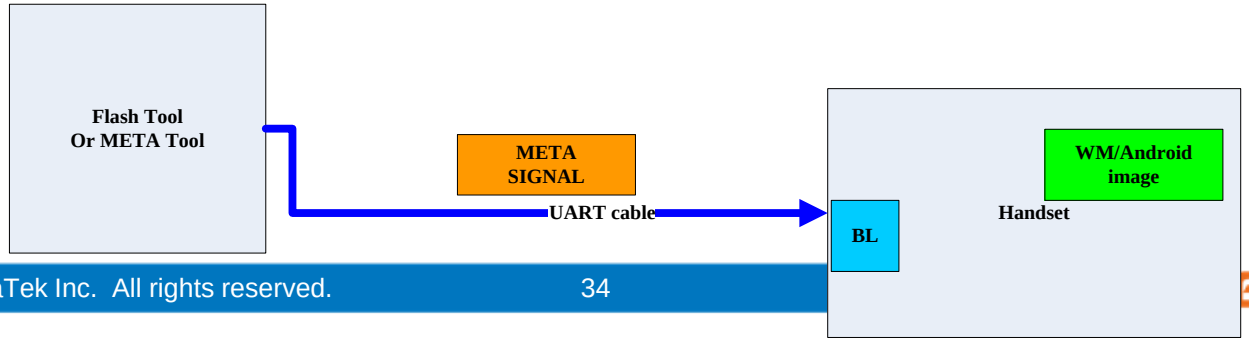
AP/MAUI META Tool

- Install Smartphone META tool.
- How to enter META mode (UART1 / USB)
  - If target have not been in META mode, click “Reconnect” button, then connect phone;
  - Phone will power on and enter into META mode automatically
- UART can support Auto baud rate
  - UART IO voltage of MT6573 is 1.8V
  - Suggest to use 1.8V level shifter, 1.8V UART-to-USB IC on test fixture side. (Please refer to “Important Notification for MT6573 UART Interface” guideline)
- Please refer to META user manual in detail.





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Confidential B

Design Notice –
Schematic Design Notice

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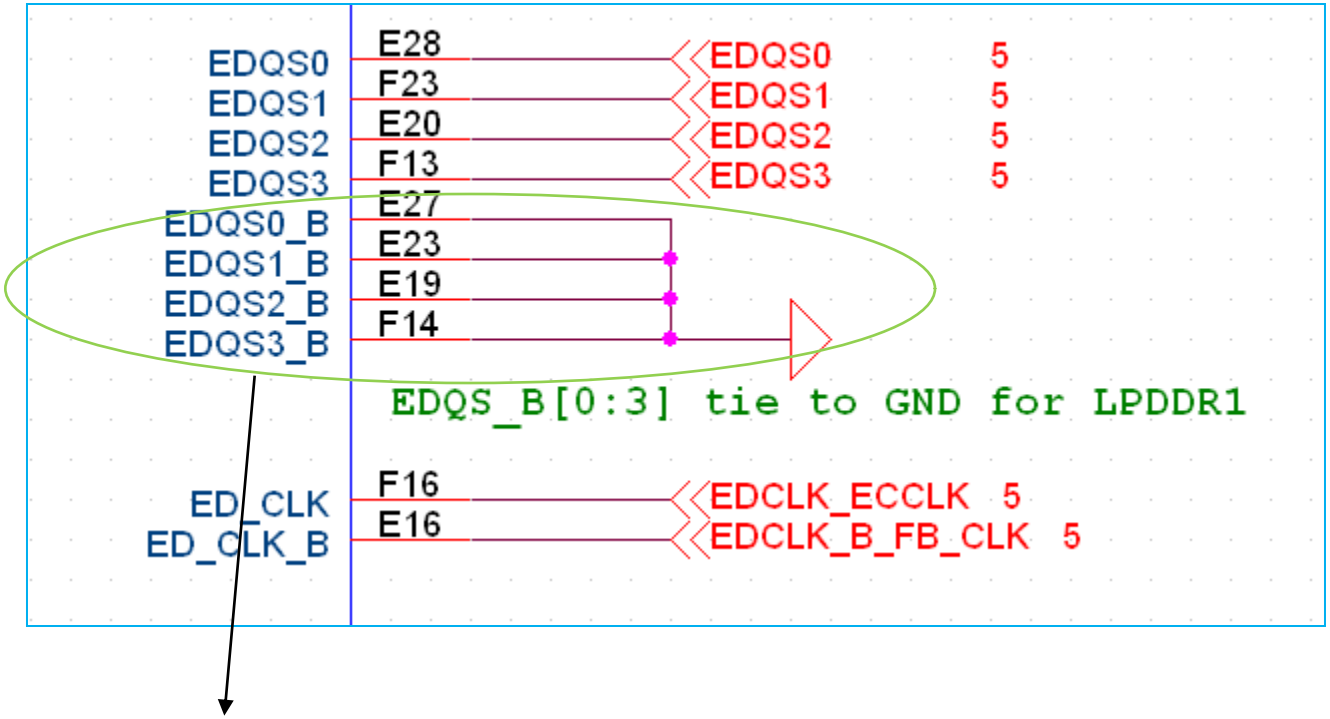
Schematic Notice (1/18)

Pin \ H\L	H(DVDD)	L(GND)	Description
TESTMODE	Enable	Disable	Test mode selection
FSOURCE_P	Enable	Disable	eFuse power (2.8V)
ICORE	Enable	Disable	Test mode selection
PMU_TESTMODE	Enable	Disable	PMU test mode selection
KCOL1	NAND Boot	NOR Boot	Boot selection
EVREF	-	LPDDR1	EMI setting
XLPDDR2	LPDDR2	LPDDR1	EMI setting

Set TESTMODE, ICORE, PMU_TESTMODE to 0V (GND)
Set FSOURCE_P to 0V (GND)
Set KOL1 weakly pull-up to 1.8V
Set EVREF, XLPDDR2 to 0V (GND)

Schematic Notice (2/18)



EDQS_B[0:3] tie to GND for LPDDR1

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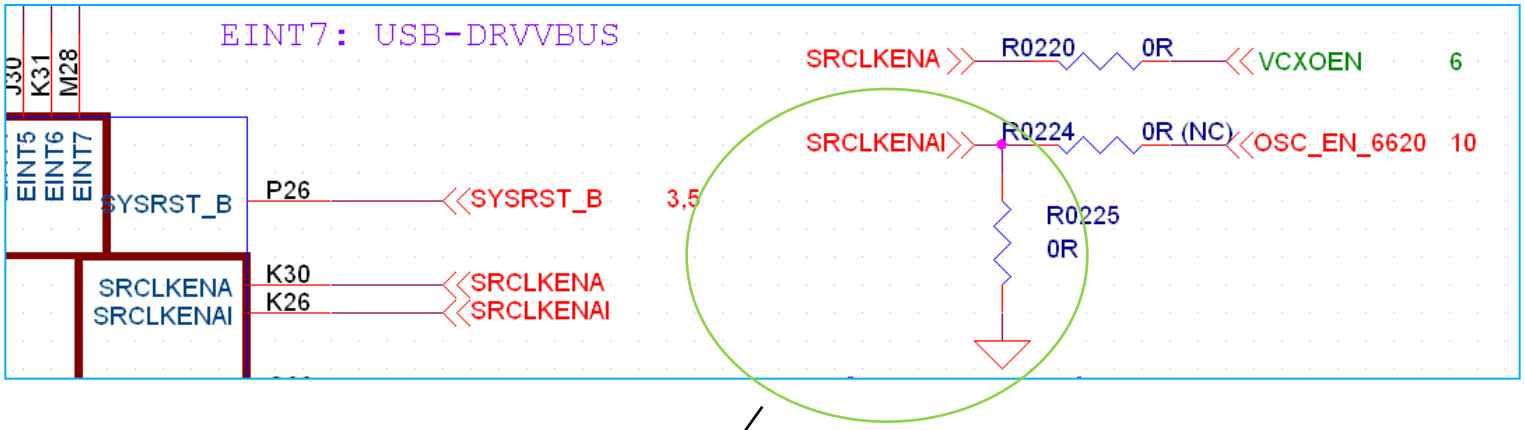
Schematic Notice (3/18)



SRCLKENAI (input) tie to GND if not used; otherwise, system can not go into sleep mode

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Schematic Notice (4/18)

Net	PU/PD	Aux Func.0	Aux Func.1
KCOL6	PU/PD	GPIO36	I1:KCOL6
KCOL7	PU/PD	GPIO35	I1:KCOL7
KCOL5	PU/PD	GPIO37	I1:KCOL5
KCOL4	PU/PD	GPIO38	I1:KCOL4
KCOL2	PU/PD	GPIO40	I1:KCOL2
KCOL3	PU/PD	GPIO39	I1:KCOL3
KROW7	PU/PD	GPIO43	I1:KROW7
KROW6	PU/PD	GPIO44	I1:KROW6
KCOL1	PU/PD	GPIO41	I1:KCOL1
KCOL0	PU/PD	GPIO42	I1:KCOL0
KROW4	PU/PD	GPIO46	I1:KROW4
KROW5	PU/PD	GPIO45	I1:KROW5
KROW0	PU/PD	GPIO50	I1:KROW0
KROW1	PU/PD	GPIO49	I1:KROW1
KROW3	PU/PD	GPIO47	I1:KROW3
KROW2	PU/PD	GPIO48	I1:KROW2

Default reset state of KROW[0:7] & KCOL[2:7] is PD (pull-down)
Default reset state of KCOL[0:1] is PU (pull-up)
Default reset state of KROW[1:7] & KCOL[2:7] is Aux Func. 0 (GPIO)
Default reset state of KROW[0] & KCOL[0:1] is Aux Func. 1 (Keypad)
Don’t use KROW[0] & KCOL[0:1] for GPIO usage

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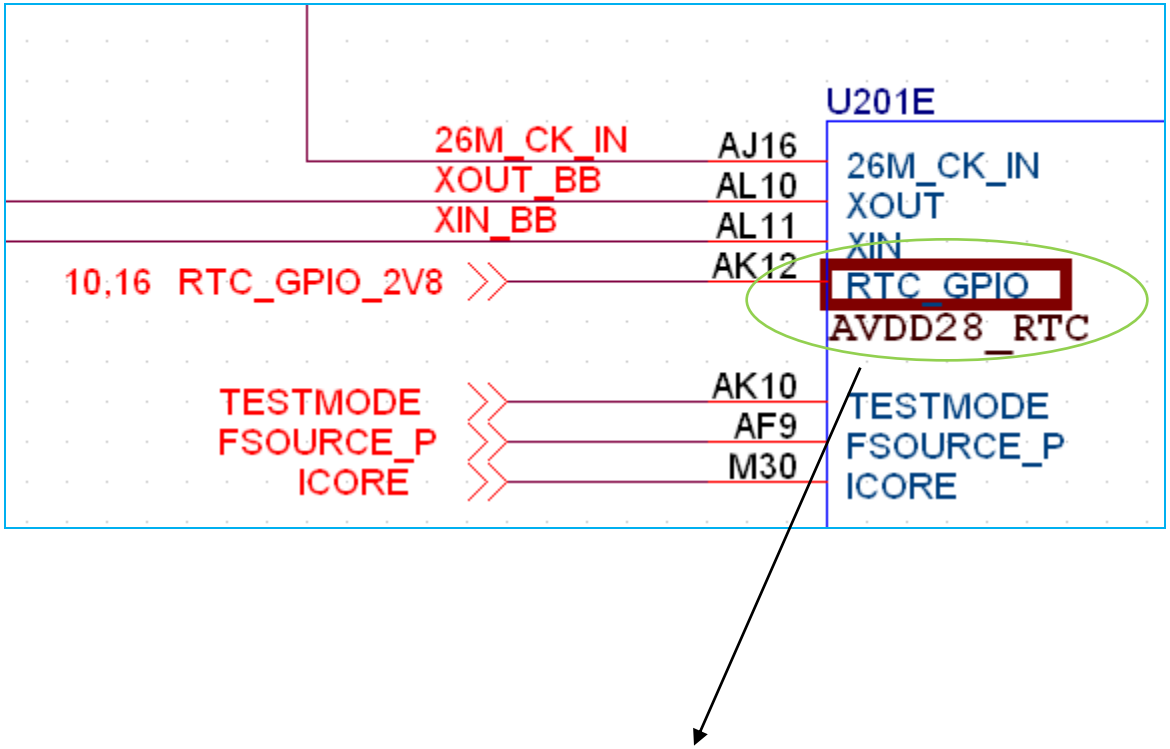
Schematic Notice (5/18)



RTC_GPIO belongs to 2.8V VRTC power domain;
it can be used to export 32kHz clock or 2.8V GPIO usage

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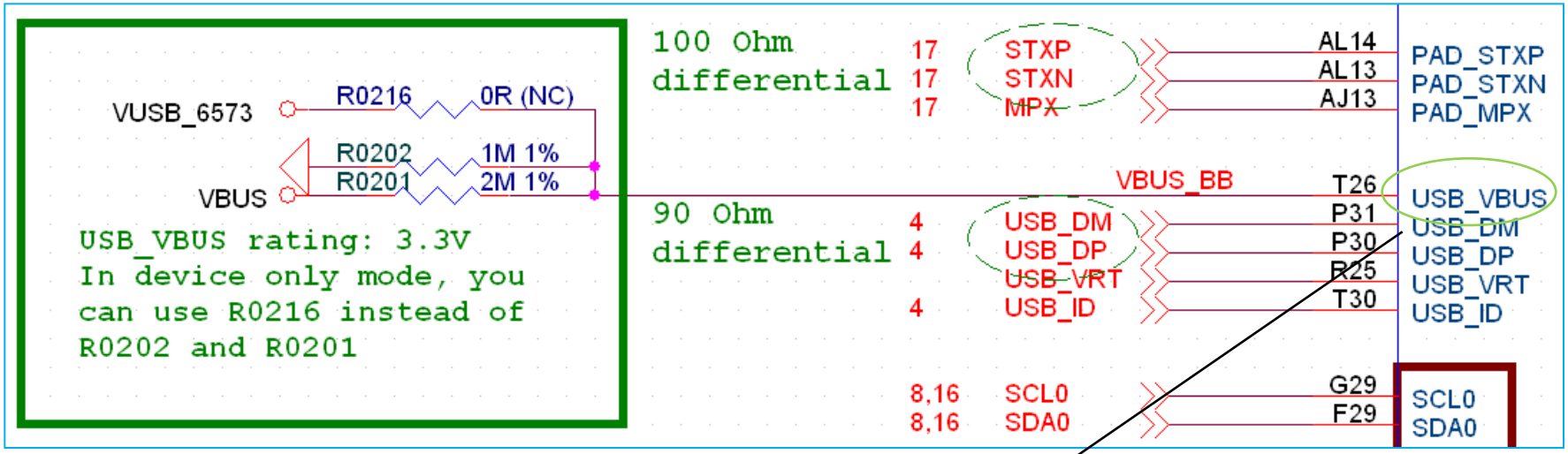
Schematic Notice (6/18)



You can use R0216 instead of R0201 and R0202 in device only mode

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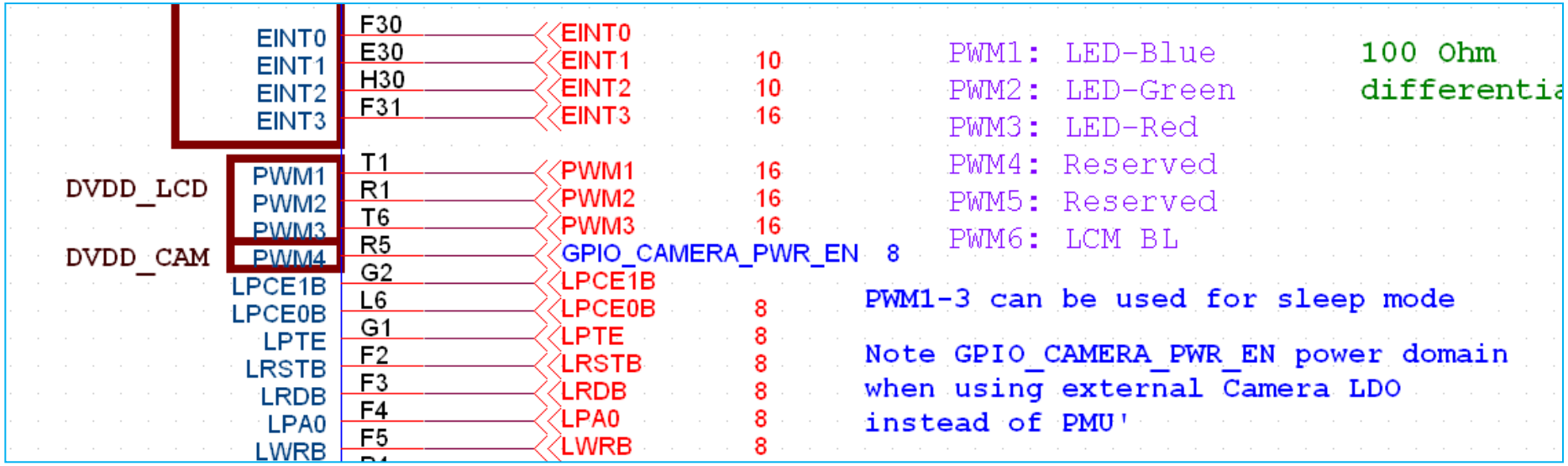
Schematic Notice (7/18)



PWM[1:3] can be used for sleep mode blinking;
PWM4 belongs to DVDD_CAM power domain

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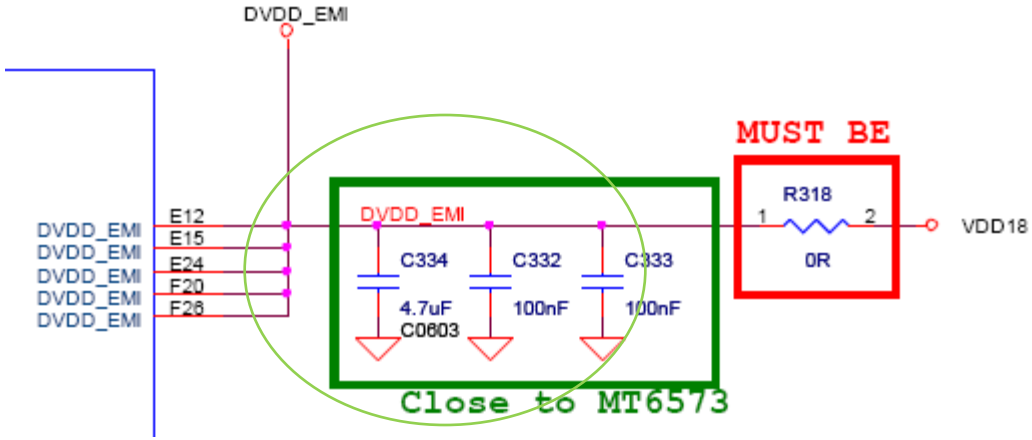
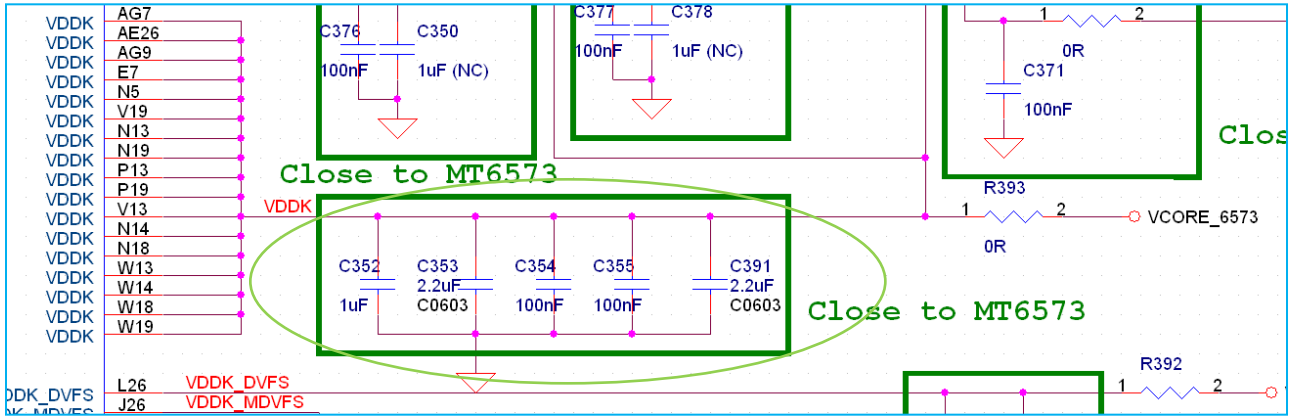
Schematic Notice (8/18)





Keep enough capacitors on DVDD_EMI and VDDK as above; put them as close as possible to MT6573

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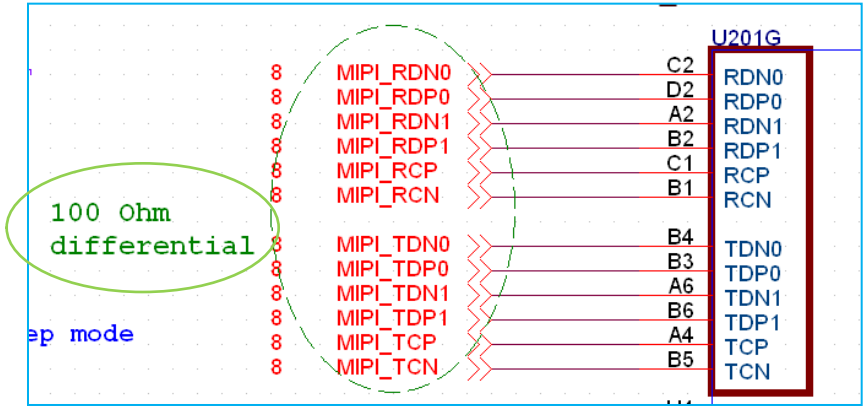
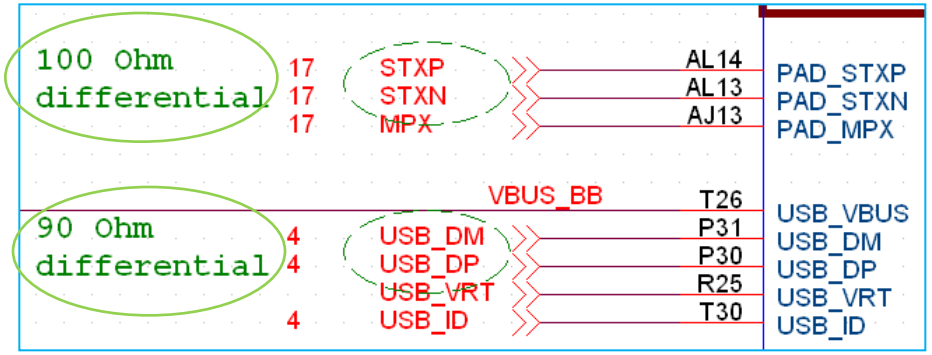
Schematic Notice (9/18)





MIPI: 100 Ohm differential signal impedance control
SATA: 100 Ohm differential signal impedance control
USB: 90 Ohm differential signal impedance control

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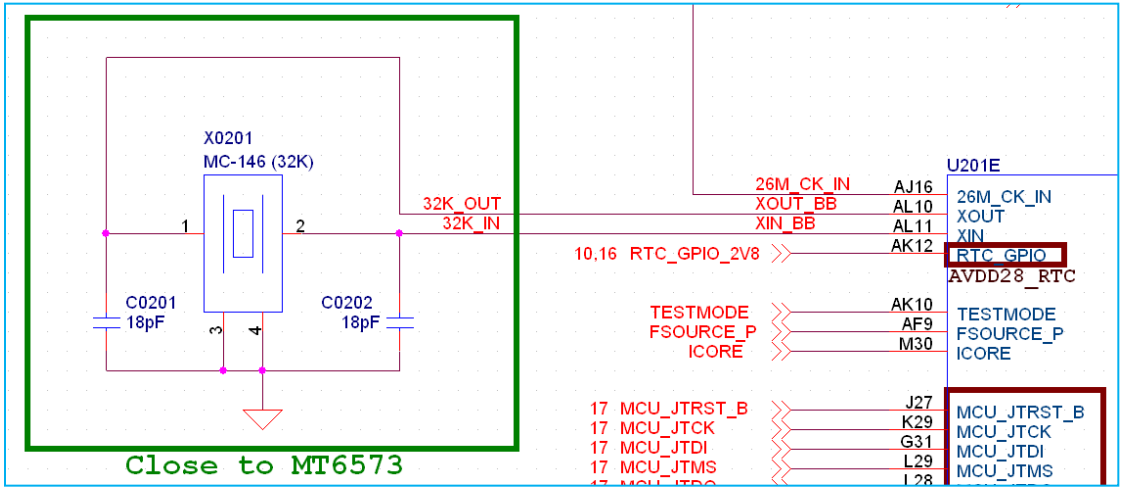
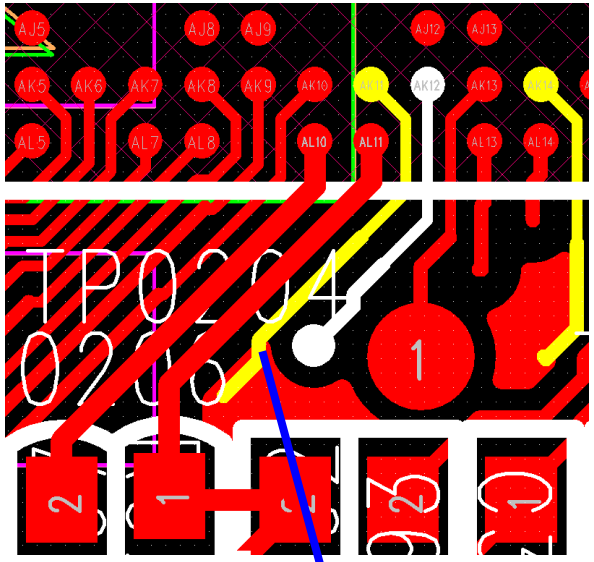
Schematic Notice (10/18)





Separate XIN and RTC_GPIO (white line) by GND (yellow line)

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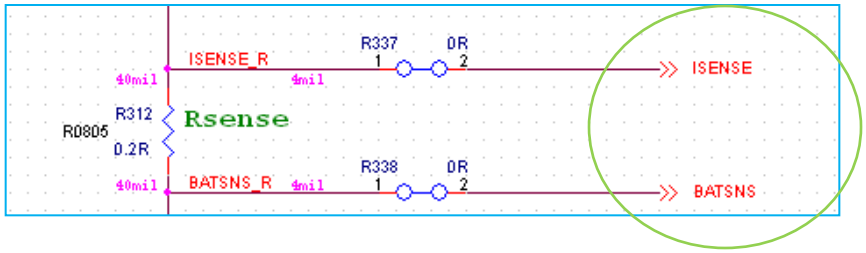
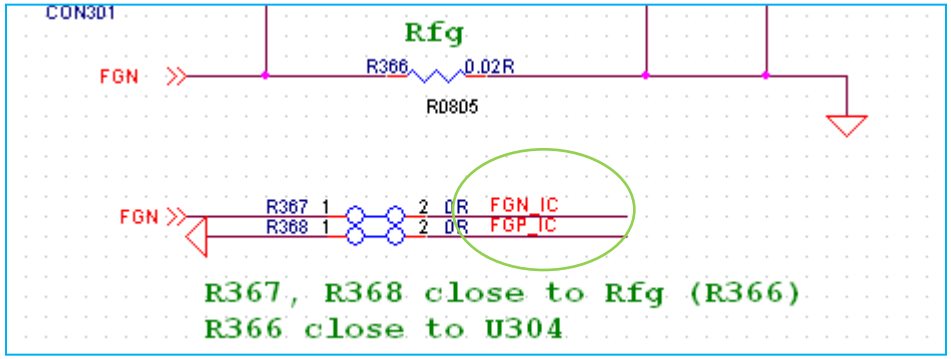
Schematic Notice (11/18)





Keep differential routing for ISENSE and BATSNS to Rsense
Keep differential routing for FGP and FGN to Rfg

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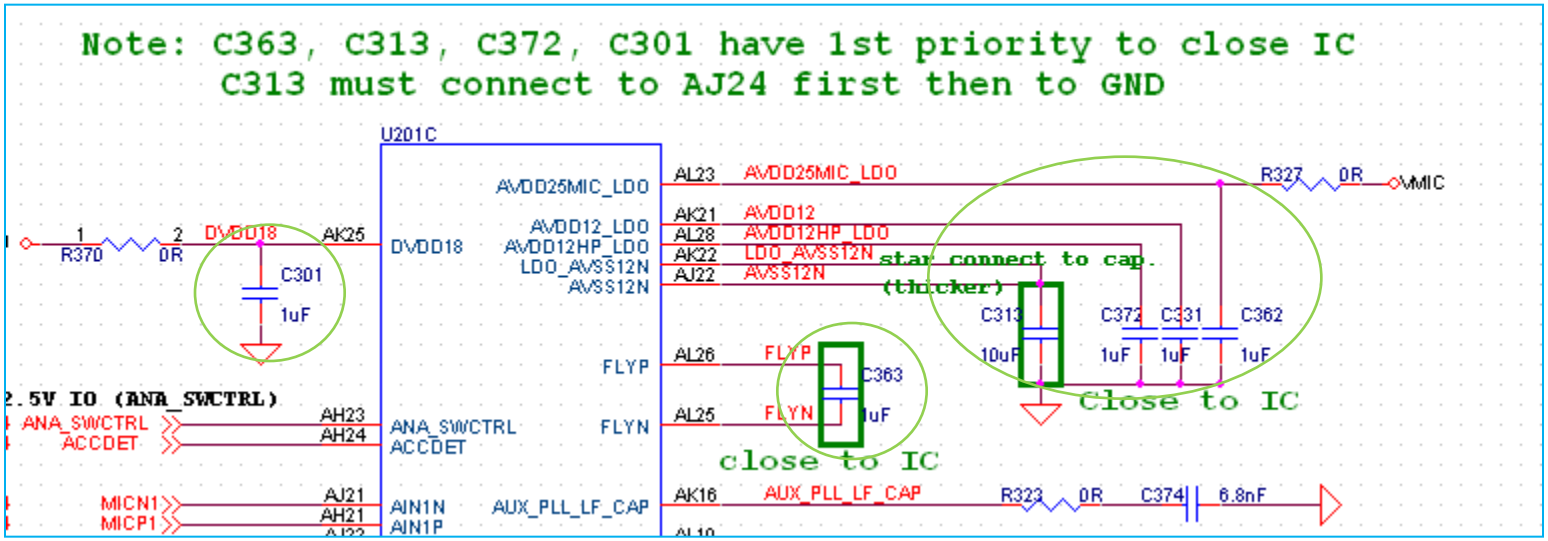
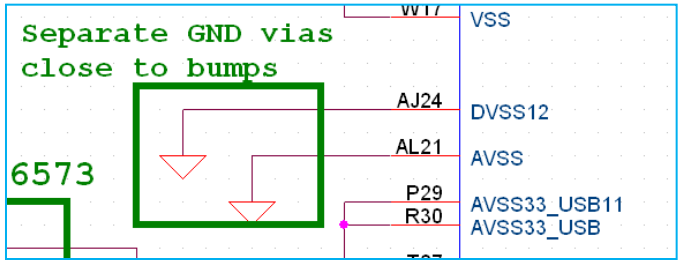
Schematic Notice (12/18)



Keep C363, C313, C372, C301 as close as possible to MT6573

C313 must connect to AJ24 first then to GND



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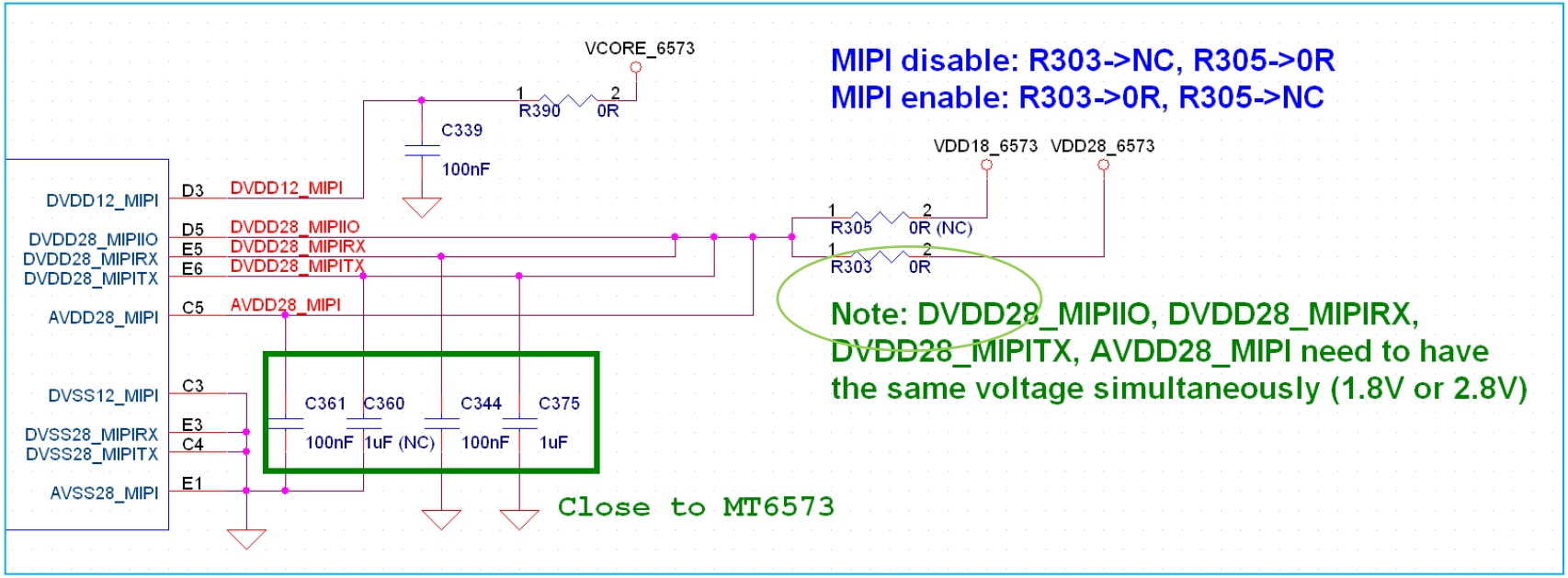
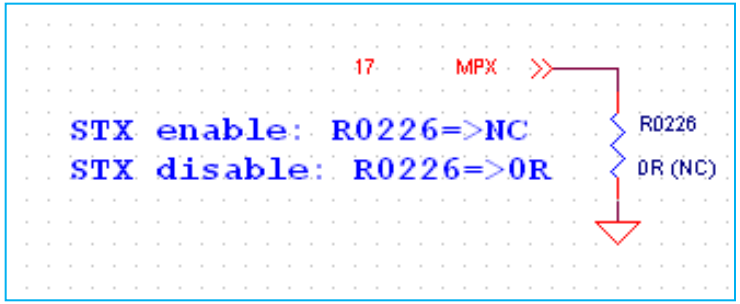
Schematic Notice (13/18)

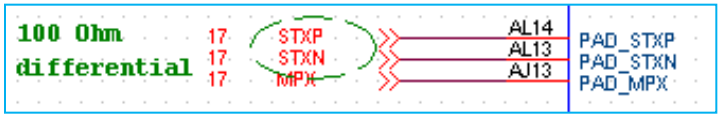


DVDD28_MIPIIO, DVDD28_MIPIRX, DVDD28_MIPITX, AVDD28_MIPI need to have the same voltage simultaneously

	2.8V	1.8V
MIPI TX (LCM)	V	X
MIPI RX (Camera)	V	X
GPIO	V	V

Schematic Notice (14/18)





Tie PAD_MPX to GND if not used

Keep PAD_STXP and PAD_STXN as floating if not used

Note:

PAD_STXP, PAD_STXN, PAD_MPX are used for internal debug purpose

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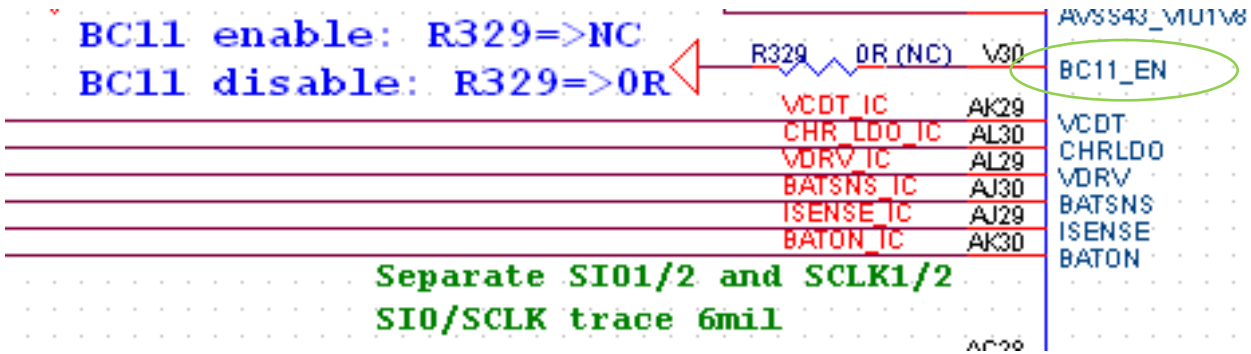
Schematic Notice (15/18)



BC11_EN:

BC11 charger enable: floating

BC11 charger disable: tie to GND

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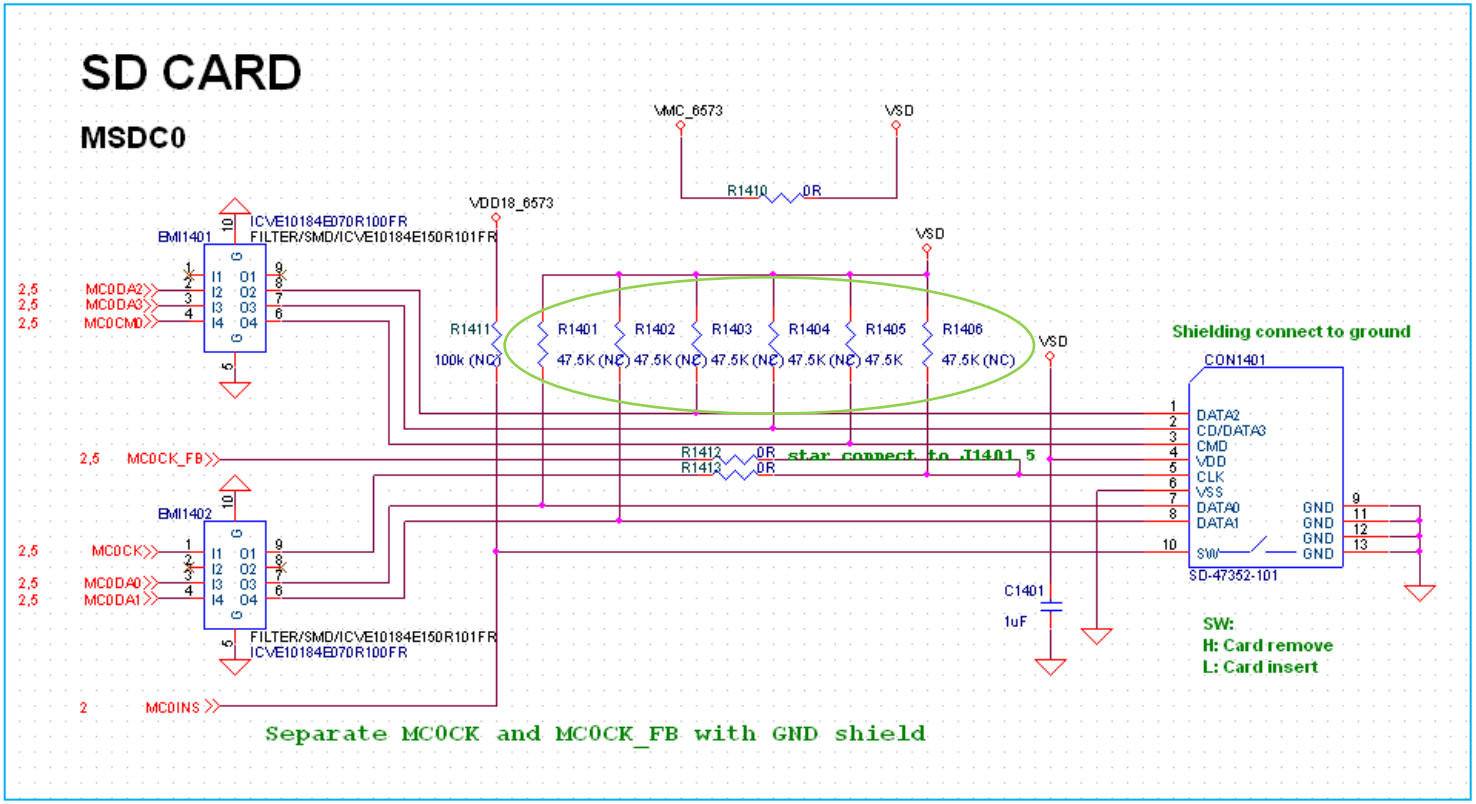
Schematic Notice (16/18)



For better interoperability and stability, please reserve 47k Ohm in each memory card interface line

For memory card hot plug function, please connect to MC0INS with internally pull-up

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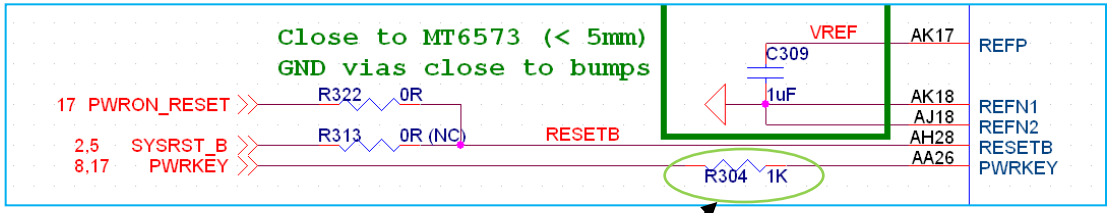
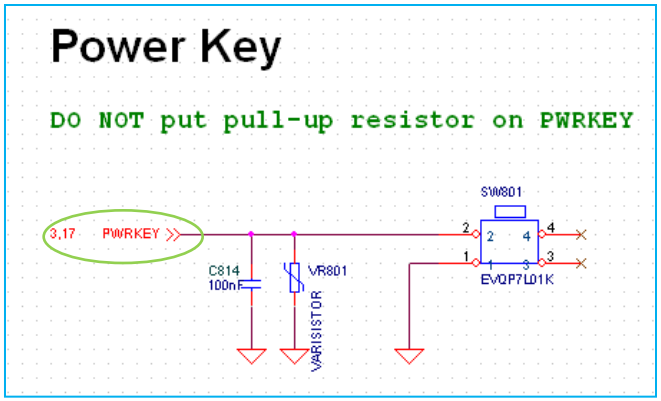
Schematic Notice (17/18)





Add a 1k Ohm resistor to avoid ESD damage

DO NOT put pull-up resistor on PWRKEY

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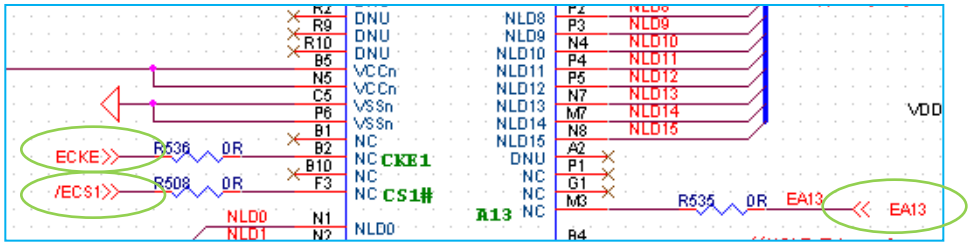
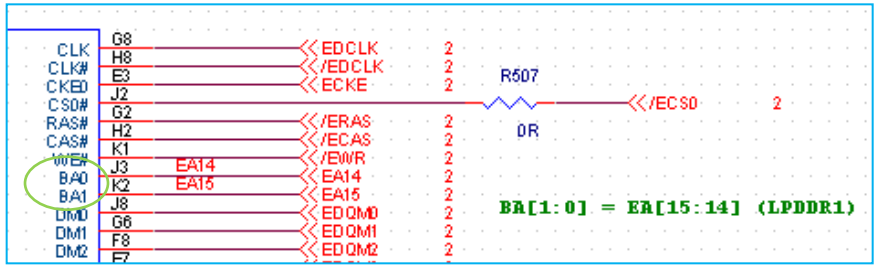
Schematic Notice (18/18)





Connect EA13 (MT6573 A25) to A13 of MCP (M3)
Connect EA[14:15] (MT6573 D24, A21) to BA[0:1] of MCP (J3, K2)

137-ball FBGA dual die:
connect ECKE (MT6573 C14) to CKE1 of MCP (B2)
connect ECS1_B (MT6573 B25) to CS1# of MCP (F3)
For compatibility for single and dual die, 0 Ohm is recommended to be reserved as shown above

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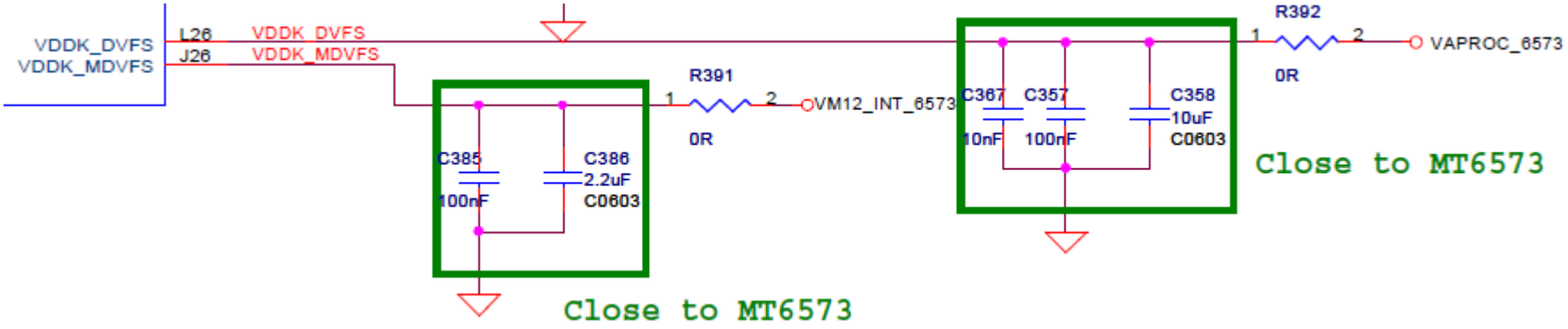
Schematic Notice



- VDDK_DVFS is power to APMCU.
- VDDK_MDVFS is power to internal SRAM.

- C358 > 10uF for better transient response.
- Put C367, C357, C358 as close as possible to processor.

(dominate CPU highest clock)

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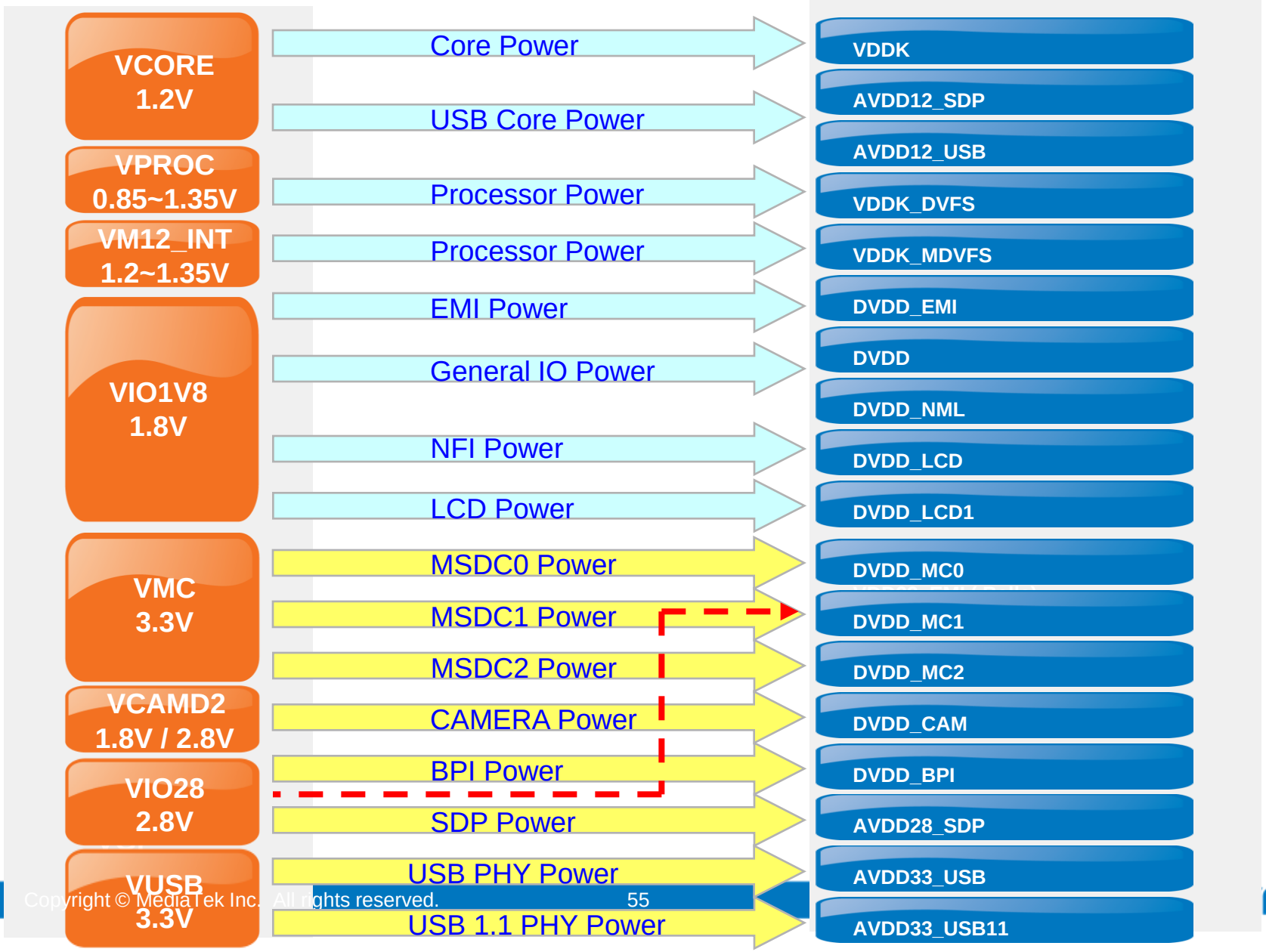
Reference Power Distribution



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Default UART Dispatch Notice

UART1	Download Bootloader, META Link, Production Line Test Point
UART2	User Define
UART3	User Define, Default Use for MT6620
UART4	Data log for Debugging, Boot-Up Selection and Setting.
USB Port	Download Image file, Mass Storage

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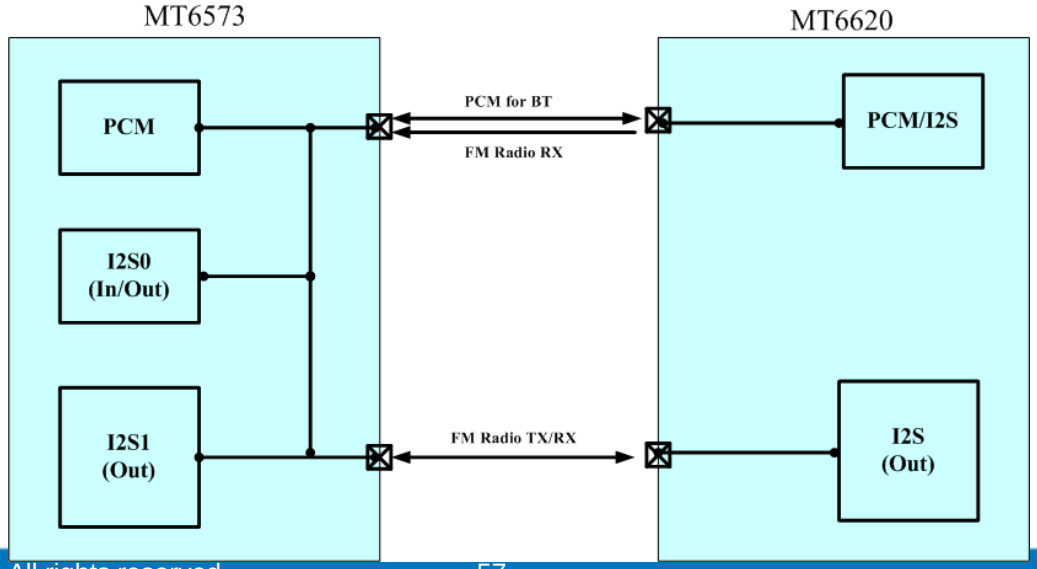
I2S Design Notice

	INPUT	OUTPUT	Application
I2S0	V	V	FM RX, FM TX, mATV, HDMI, External Codec…
I2S1	X	V	FM TX, HDMI, External DAC

- I2S0 default mux with PCM and connect to MT6620 for pin and net saving.
- I2S1 can be mux as I2S0 if input is required.



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MT6573 Reference Phone PCB 6-layer Define

Layer	Define	Via	Stackup		
			S/M	min10	30
L1	Signal			20~48	40
			pp (1080)	65+/-15	66
L2	Signal			20~48	32
			pp (2116)	130+/-20	128
L3	GND			Hoz	15
			core	381+/-38	381
L4	Signal			Hoz	15
			pp (2116)	130+/-20	128
L5	GND, Signal			20~48	32
			pp (1080)	65+/-15	66
L6	GND			20~48	40
			S/M	min10	30
设计板厚:			1.003	(mm)	1003
成品板厚:			1.0+/-0.1	(mm)	

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MEDIATEK

Design Notice – GPIO Selection

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Design Notice – GPIO selection (1/2)

1. Pull-Up / Pull-Down selection :

- Choose GPIO with suitable PU/PD after reset state for application
  - Ex : As for “enable pin of audio amplifier”, please choose GPIO with **PD** after reset state
  - Ex : As for “enable pin of external LDO”, please choose GPIO with **PD** after reset state

2. Power domain of IO supply selection :

- Choose GPIO with suitable power domain of IO supply for application
  - GPIO [0:6] DVDD_NML
  - GPIO [7:9] VSIM2
  - GPIO [10:25] DVDD_BPI
  - GPIO [26:52] DVDD
  - GPIO [53:61] DVDD_MC0
  - GPIO [62:69] DVDD_MC1
  - GPIO [70:75] DVDD_MC2
  - GPIO [76:91] DVDD_CAM
  - GPIO [92:93] DVDD_LCD1
  - GPIO [94:98] DVDD_CAM
  - GPIO [99:141] DVDD_LCD1
  - GPIO [142:153] DVDD28_MIPIIO
  - GPIO [154:175] DVDD_LCD
  - GPIO [176:202] DVDD_NML

3. Please choose suitable GPIO for peripheral IC :

- Please choose GPIOs with matched direction, pull-up/pull-down, data inversion, data output, gpio mode after reset state for peripheral IC application

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Design Notice – GPIO selection (2/2)

Notice of Drv_Tool usage

After enable "InPull En", you can change the PU/PD value by changing "InPull SelHigh".
(Only valid when GPIO is input mode)

"InPull En" can enable/disable PU/PD, then GPIO will be the default PU/PD value after reset state.
(Only valid when GPIO is input mode)

"OutHigh" can change the default output level.
(Only valid when GPIO is output mode)

GPIO Setting | GPO Setting | EINT Setting | ADC Setting | KEYPAD Setting | PMIC Setting

	Def.Mode	M0	M1	M2	M3	InPull En	InPull SelHigh	Def.Dir	In	Out	INV	OutHigh
GPIO0	0:GPIO0	✔	☐			✔ PD	✔	IN	✔	☐	☐	☐
GPIO1	0:GPIO1	✔	☐			✔ PD	☐	IN	✔	☐	☐	☐
GPIO2	0:GPIO2	✔	☐			☐ PD	☐	OUT	☐	✔	☐	☐
GPIO3	0:GPIO3	✔	☐			☐ PD	☐	OUT	☐	✔	☐	✔

In above example :
GPIO0 will be PU in input mode
GPIO1 will be PD in input mode
GPIO2 will be Low in output mode
GPIO3 will be High in output mode

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High Speed Memory Layout Rule (DDR)

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MT6573 External Memory Interface

- Mobile DDR 200MHz
  - SDRAM/DDR/DDR2 support up to 256MB per device
  - 32-bit data bus width
  - Memory clock up to 200MHz
  - Self-refresh mode support
  - Low power operation
  - Programmable slew rate for memory controller's IO pads
  - 4 external memory devices supported
  - Advanced bandwidth arbitration control
- NAND Flash / eMMC booting support
  - 1.8V, 8bit / 16bit IO support. 2K/4K page size, 4-bit HW ECC.
  - eMMC 4.4 support.
- Modulated layout provided (6L HDI1 / 8L HDI2)
  - 137 ball NAND + mDDR MCP
  - 6L HDI1 PCB for low cost and 8L HDI2 PCB for thin form factor.

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High Speed Memory Layout Outline

- Memory PCB layout characteristics in the following order:
  1. Placement
  2. Ground/Power plane
  3. Suggested routing order (Signal layout)
  4. Other general layout considerations

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LPDDR signals introduction:

- We can categorize DDR SDRAM interfaces into 4 groups as follows. For MT6276 or MT6573, it support x32 LPDDR.

Group	Signal Name	Description
Data	DQ[0:15] DQS[0:1] DM[0:1]	Data Bus Data Strobe Data Mask
Clock	CLK CLK#	Memory Differential Clock Memory Inverted Differential Clock
Command	A[0:15] BA[0:1] RAS CAS WE	Address Bus Bank Select Row Address Select Column Address Select Write Enable
Control	CKE CS	Clock Enable Chip Select

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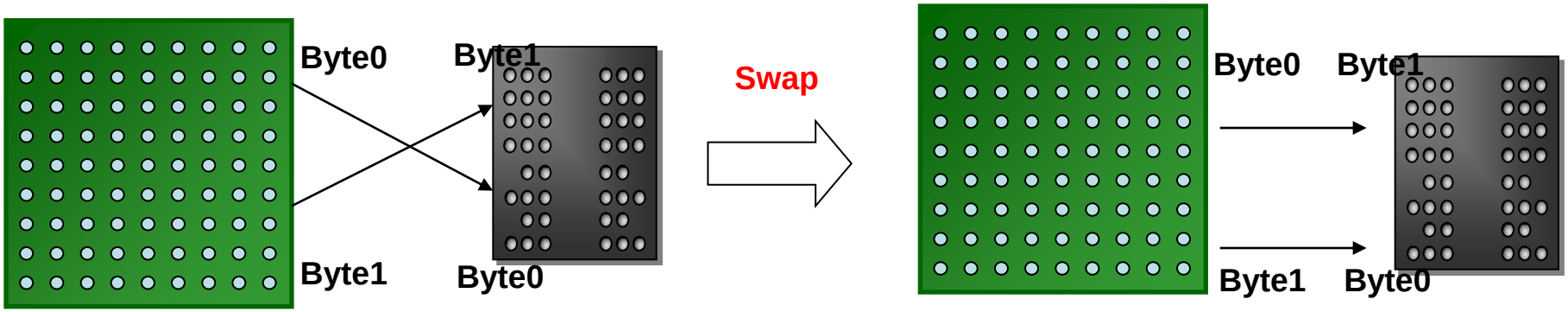
High Speed Memory Layout-Placement

- Placement
  - Memory device must place as close to BB Chip as possible
  - Avoiding extra long trace (Max trace1500mil)
  - Avoiding other high frequency devices place close to Memory
  - Route these traces smoothly, reduce the via counts and avoiding traces interlace if possible
  - You can swap byte in order to reduce traces interlace if there has restriction in placement



  - "Swap byte" means to connect DQS0 from BB chip to memory DQS1 in order to reduce the interlacing of data traces, e.g. DQ[0:7] from BB chip to memory D[8:15].

    Note: Swap the corresponding DQSx ,DMx and DQx at the same time.
  - Different bits (DQx) in the same data byte could also be swapped if needed.

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High Speed Memory Layout-P/G plane

- Ground/Power plane
  - A solid power/ground plane must be provided near all traces routing layers.
  - It will minimize the return current path to get better performance.
  - There are 2 methods for reference:
    1. It is recommended all traces are routed above a solid GND plane, and there is a power plane (memory power domain VMEM) under the GND plane if possible.

       e.g. 6 layers(MT6236/MT6276 reference stack up)-

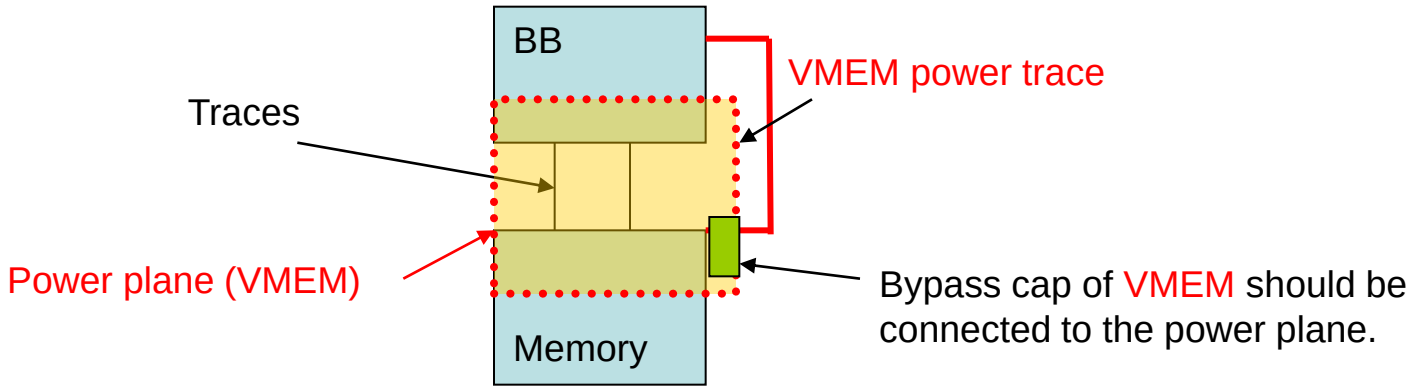
       1st layer : memory traces

       2nd layer: memory traces (strongly recommended - the same group of traces routed on the same layer)

       3rd layer: GND

       4th layer: Power plane (VMEM), it could including some memory traces (need to shielded with Vm plane)

       5th/6th layer: if there is some memory trace in 4th layer, please assign 5th layer as GND plane. If there is no memory trace in 4th layer, 5th/6th don't care.



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High Speed Memory Layout-P/G plane

2. If power plane is a signals' reference plane (return current path), please notice that its area must be cover the entire signal routes in signal layer. In this condition, GND plane is still needed even as 6th layer

Method 1:

Method 2:

Black line: Memory Signal traces Blue line: GND plane Red line: Power plane

Green line: do not care

Note: All power trace bypass capacitors (de-cap) must be placed as close to the memory or BB power pins as possible, and all capacitor's GND should have the shortest and widest trace to the GND plane.

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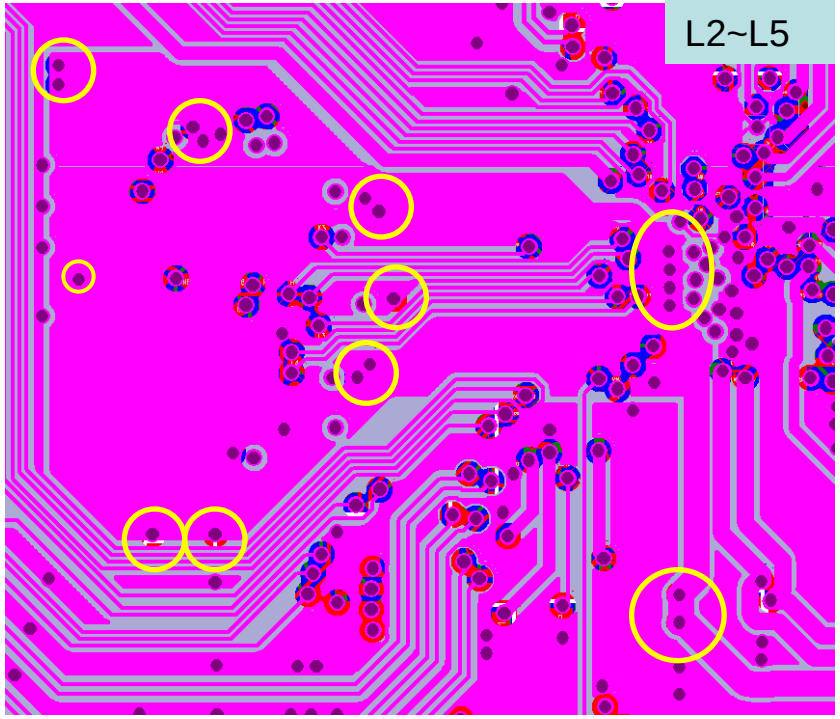
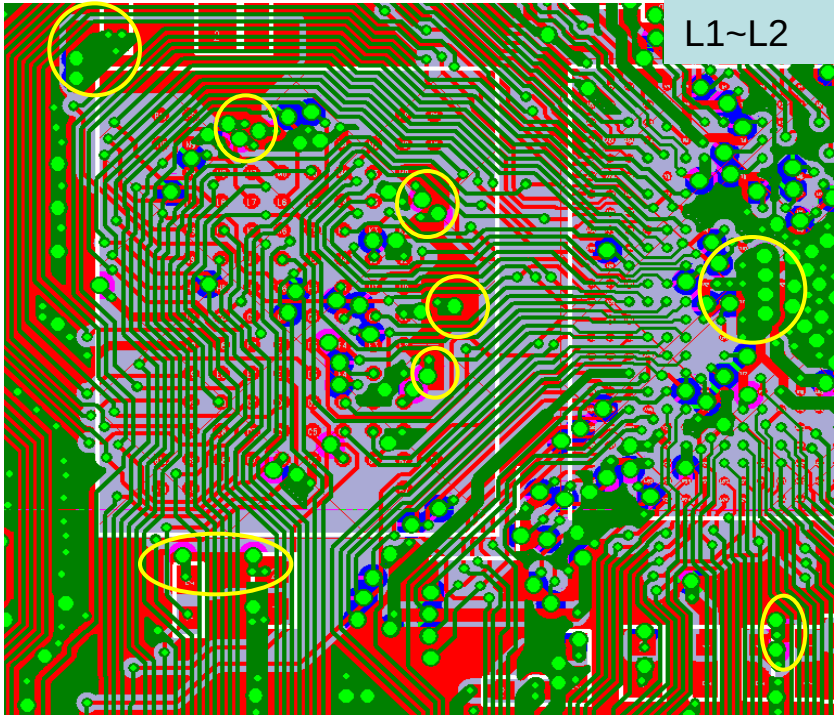
Vm Notice(1/2):

- Vm Via Quantity Suggestion:
  1. blind via(L1-L2): one via per one Vm ball or one de-cap if possible
  2. buried via(L2-L5): more is better (at least 3 via for BB Vm balls)
  3. Please refer to the reference phone layout as below





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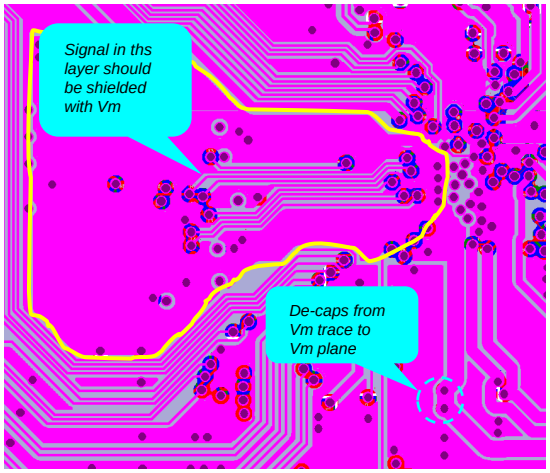
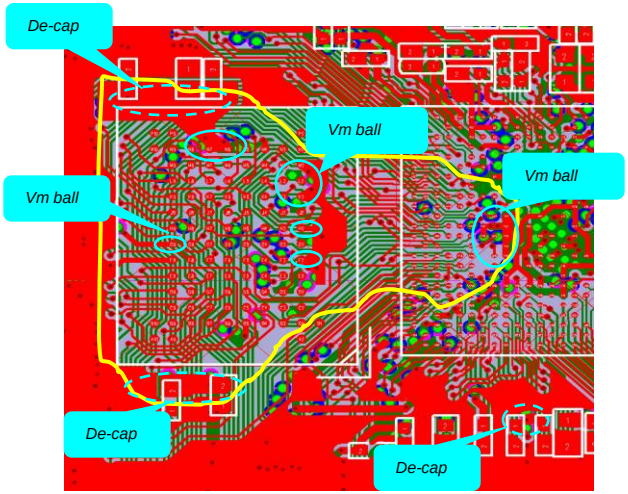
Vm Notice(2/2):

- Vm plane size suggestion:
  - 『 Method 1 』 : must cover all of BB & MCP Vm balls and should cover de-caps (close to Vm balls) if possible, see the two figure.
  - 『 Method 2 』 : it must cover the entire memory signal routes in signal layers, like 『 Method 1 』 GND plane's role.

『 Method 1 』





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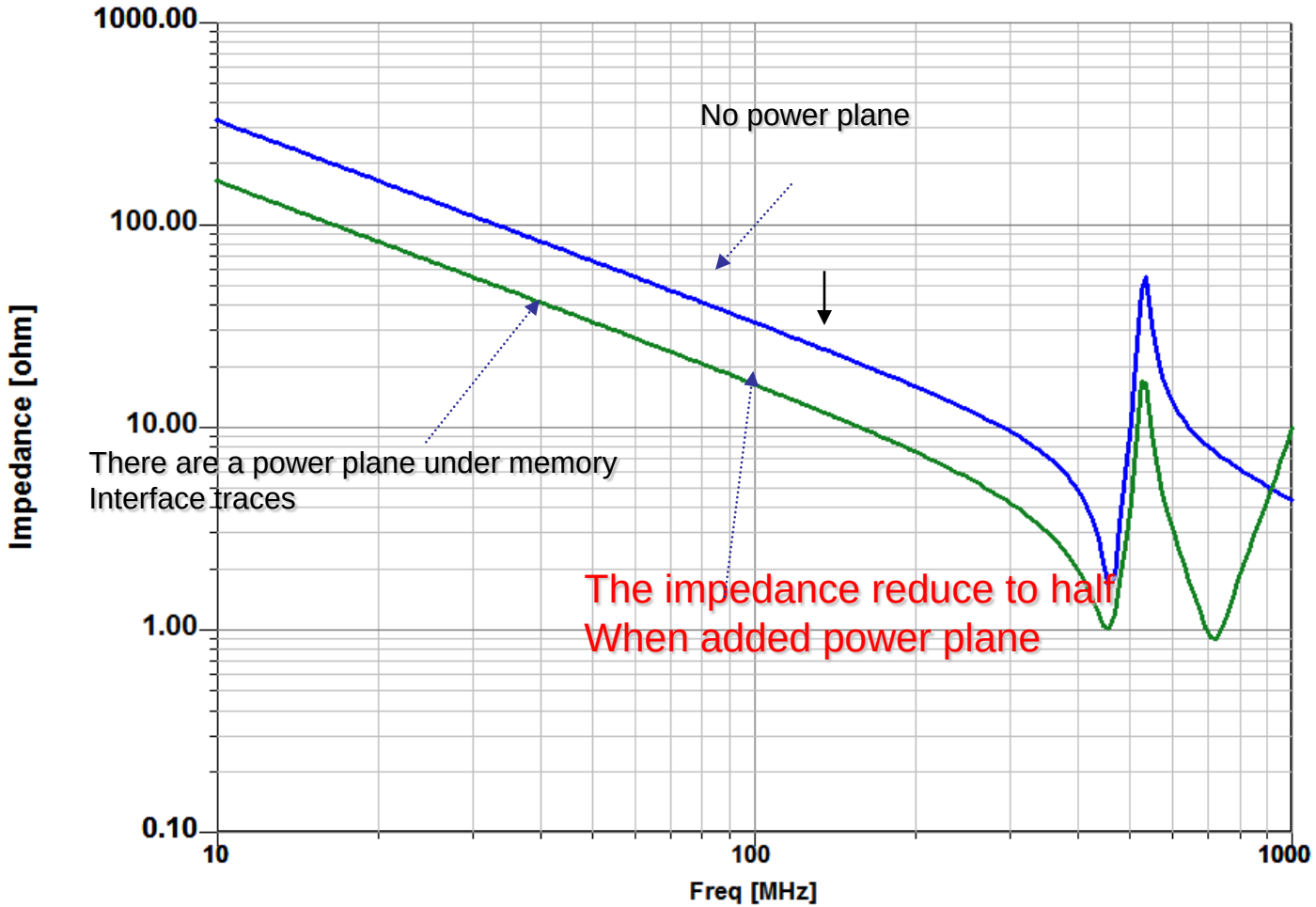
High Speed Memory Layout-P/G plane

- If we take a good power plane under traces, we can get good trace impedance performance.



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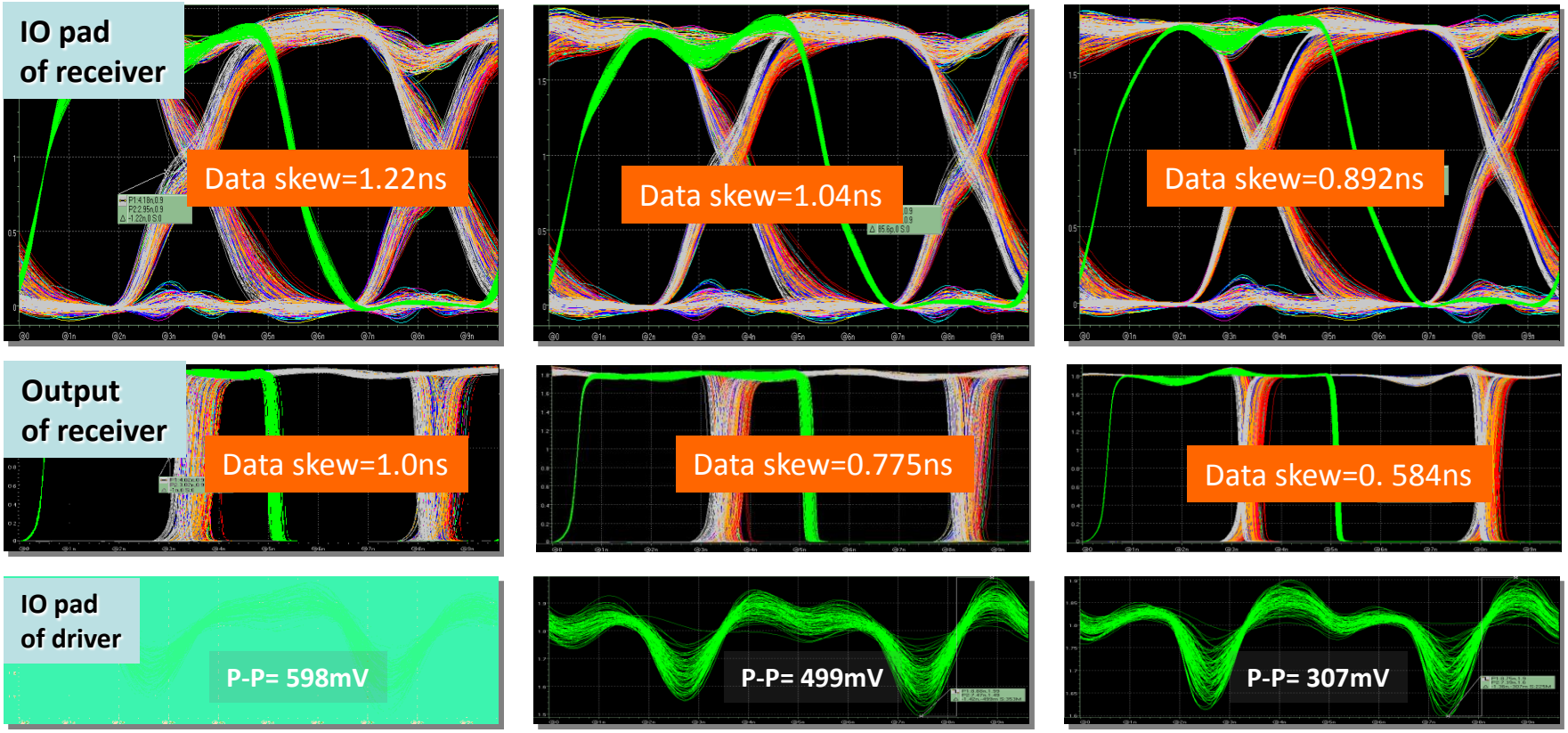
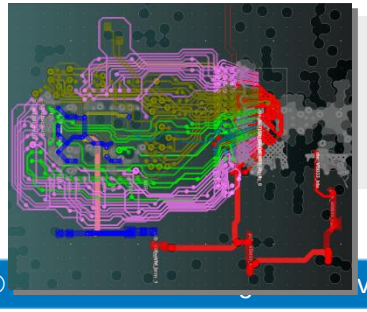
High Speed Memory Layout-P/G plane

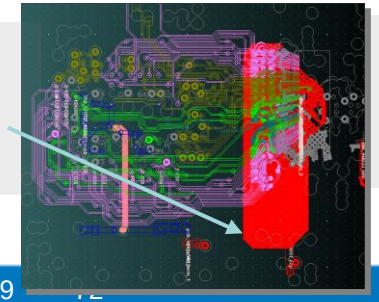
Add a power plane (Vm plane) on PCB to enhance performance (reducing data-skew)



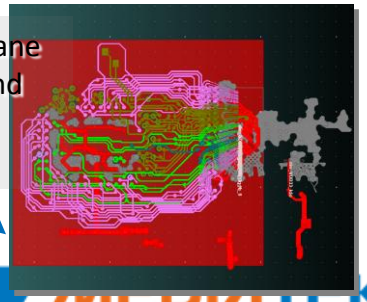
Only power trace
Bad



Added a small power plane under BB chip
Not good

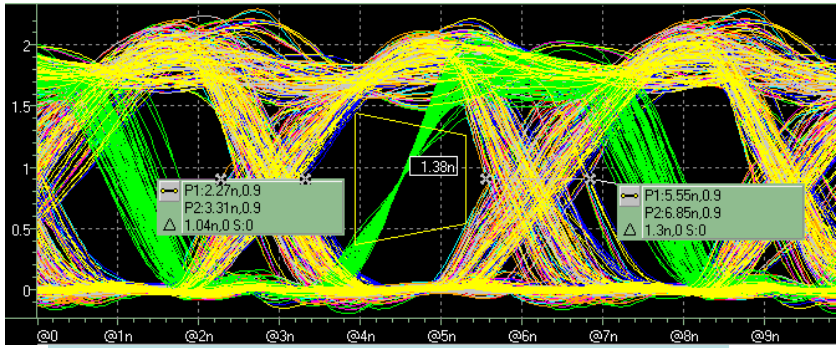


Added power plane under BB chip and DRAM
Must

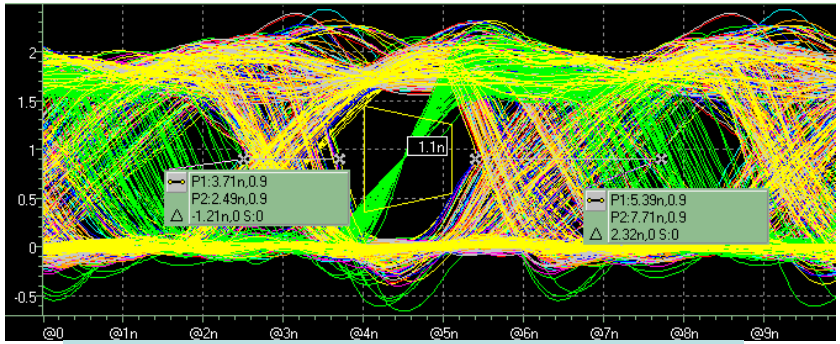


High Speed Memory Layout-P/G plane

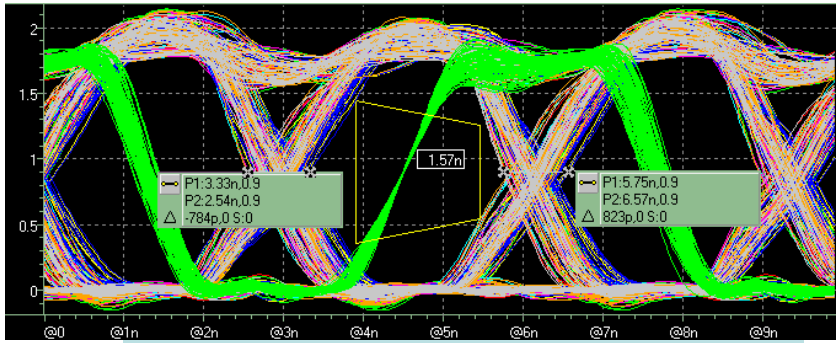
- Data eye simulation result



without power plane, but with short power trace from PMU



without power plane and short power trace from PMU



with power plane & short power trace from PMU

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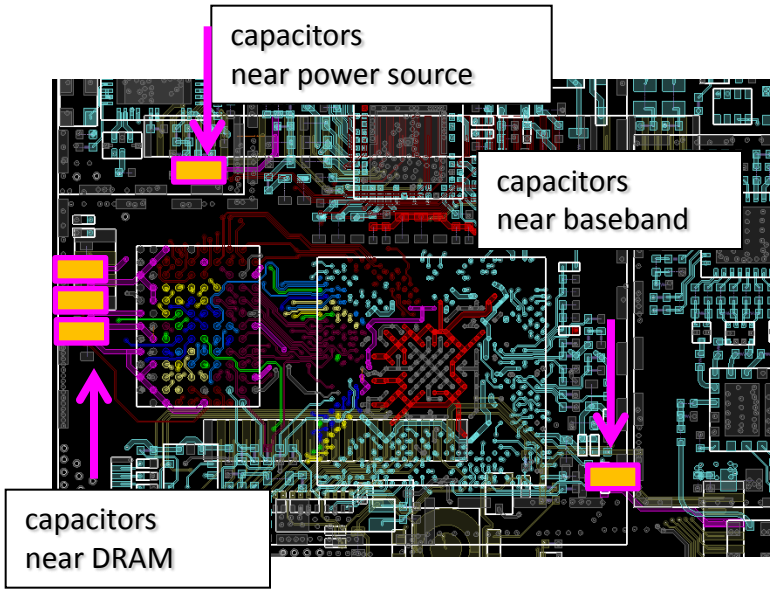
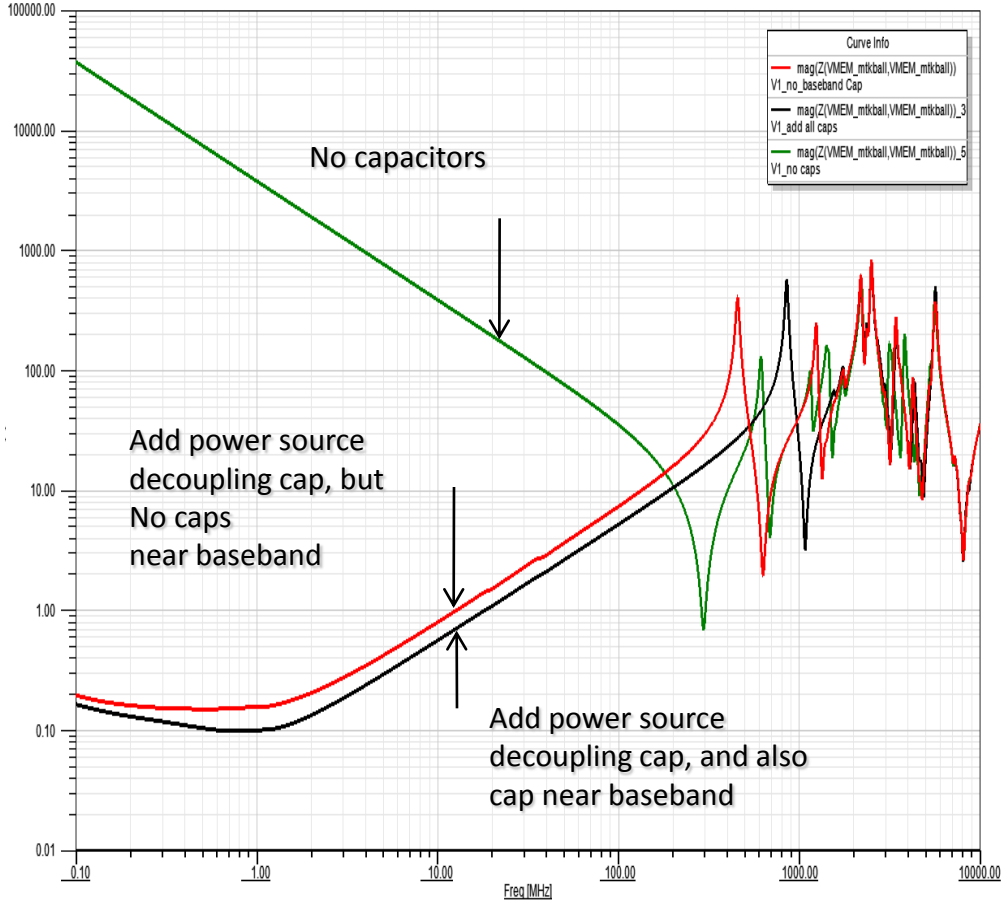
MT6516 Case study of Power Impedance (PDN)





- ***Decoupling capacitors near baseband are necessary*** for high speed mobile DRAM interface.
- ***The difference between the Impedance amplitude, will cause unstable DRAM operation. (In this case : "at -20℃ hang up")***
- Recommend to add decoupling capacitors near baseband & DRAM chip and power source.

→ Vm de-cap "near"IC is important!!

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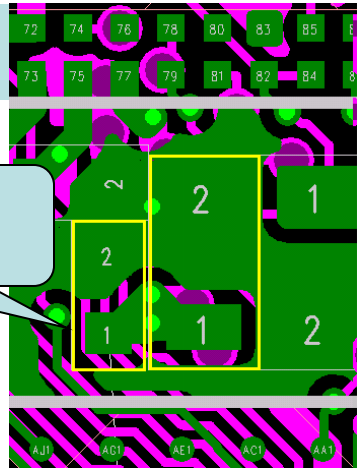
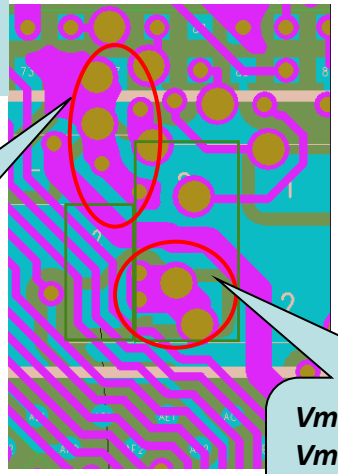
PDN Improvement (1): Vm de-cap via

L1



Vm capacitors near baseband chip

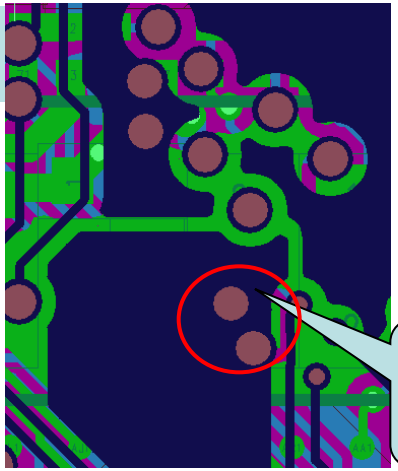
L2



GND via from capacitor GND pad(L1) to GND plane(L3)

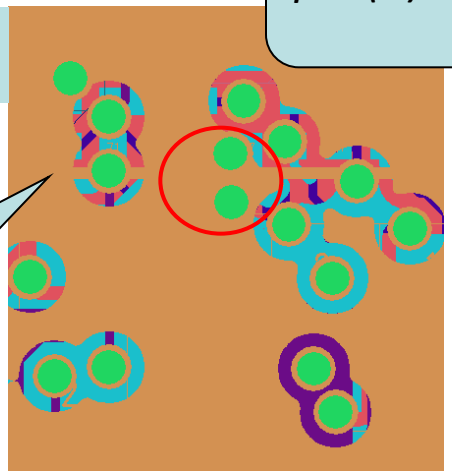
Vm via from capacitor Vm pad(L1) to Vm plane(L7)

L7



Vm plane

L3



GND plane

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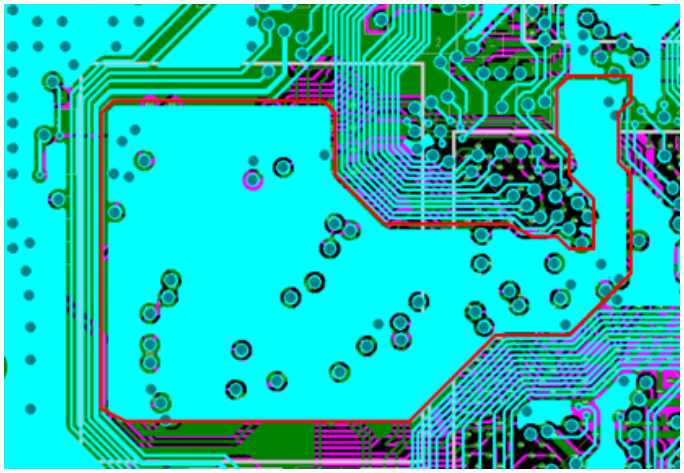
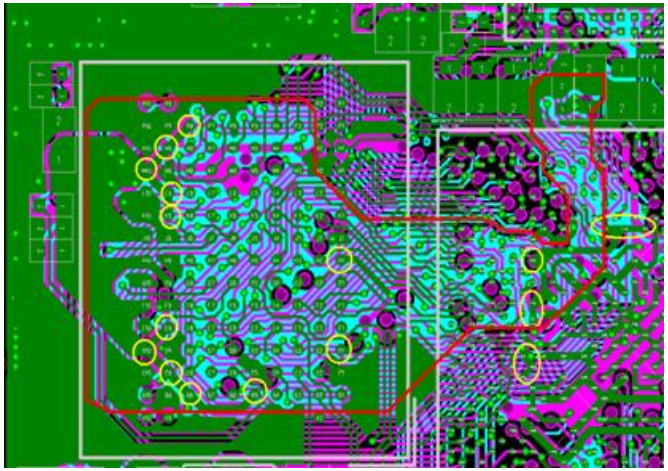
PDN Improvement (2): Vm plane size

- Please notice that the Vm plane size must be cover Vm balls of baseband chip and MCP as possible
  - ***if some Vm balls can't be covered by Vm plane, please check if Vm trace/via quantity between Vm plane to these Vm balls are optimized. (Please try to move other trace and reserve space to increase Vm via quantity)***
- Please notice that the via quantity between Vm plane to Vm balls, must follow the basic rule at least as the previous pages.





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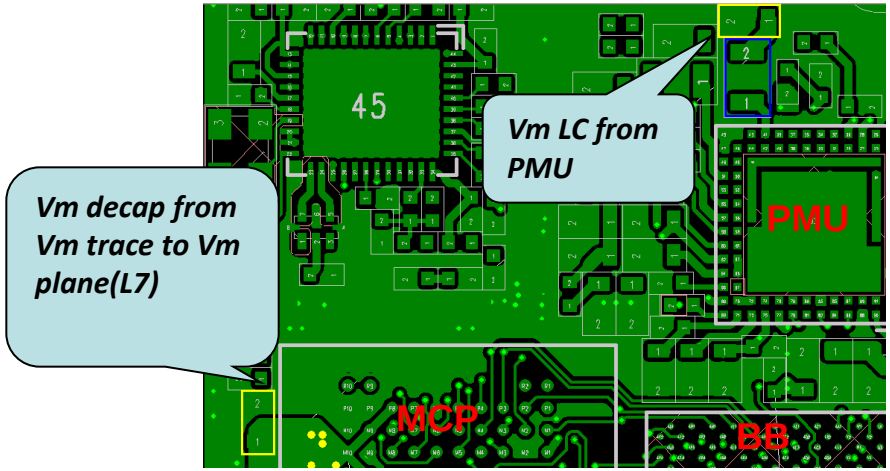
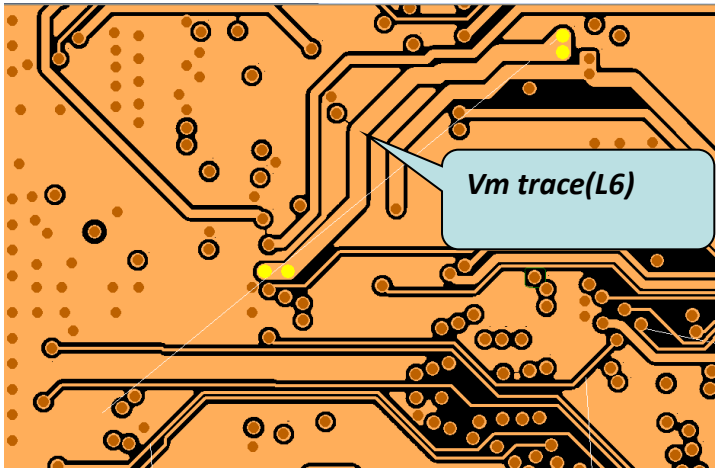
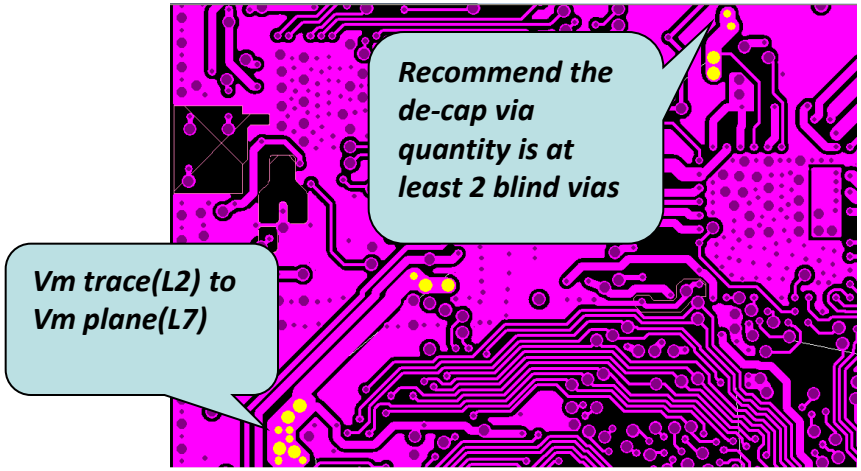
PDN Improvement (3): Vm trace/via







- Please notice that Vm via quantity is optimized (at least 2 buried via) when Vm trace from PMU to Vm plane changes layer no.

  Vm PDN: L1 LC→L6 trace→L2 trace →L7 Vm plane

- Please notice that the decoupling capacitor from Vm trace to Vm plane is needed.

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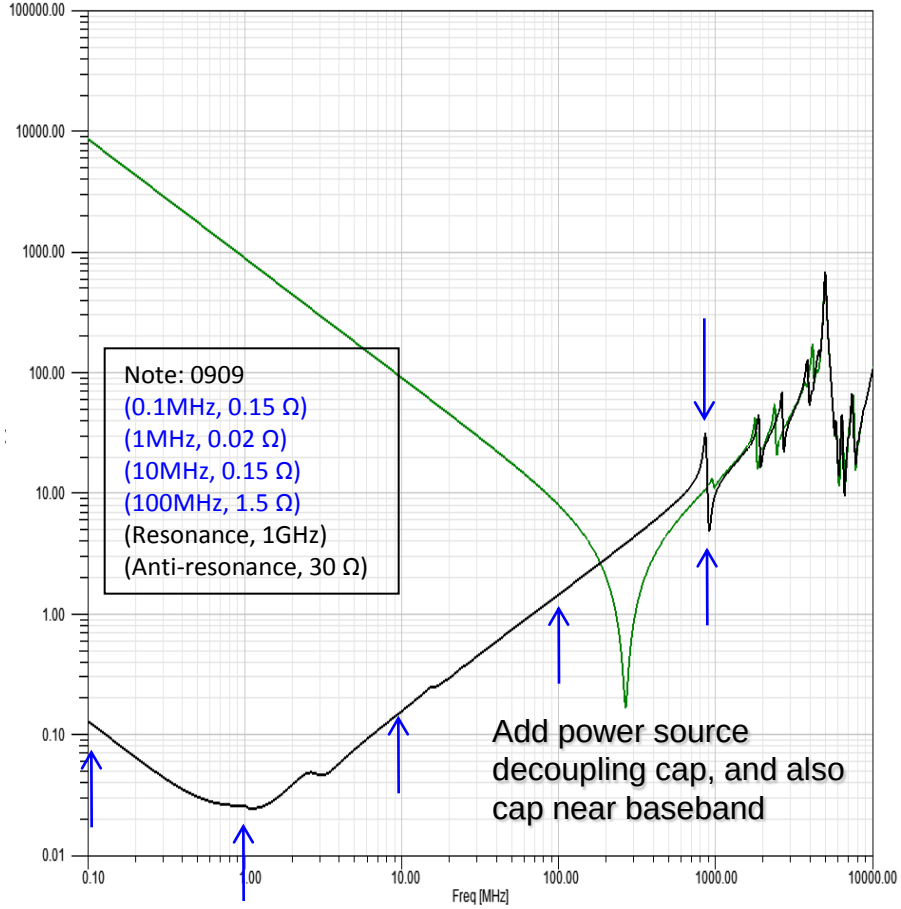
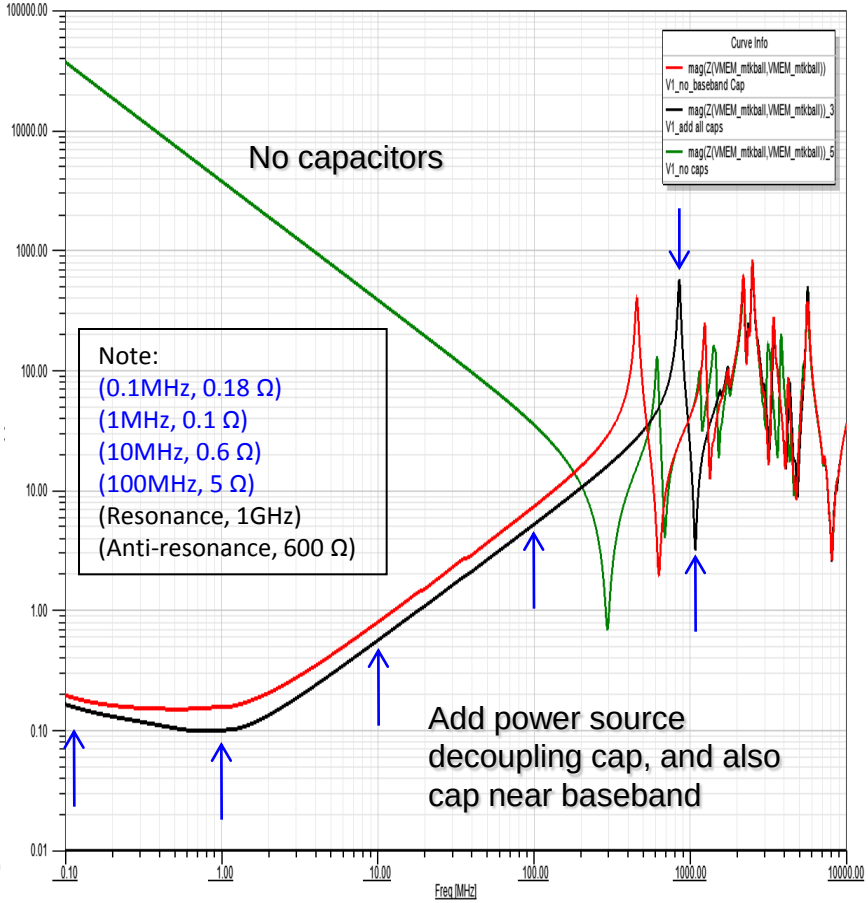
PDN comparison of MTK in-house & customer PCB layout

Improvement PDN (MTK in-house)



Customer's Board (Debug reference)



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PDN comparison table

	0.1 MHz	1 MHz	10 MHz	100 MHz	Resonance	Anti-resonance	Remark
MTK In-house (0909)	0.15 Ω	0.02 Ω	0.15 Ω	1.5 Ω	~1 GHz	30 Ω	(i) Improve power plane (ii) Improve power via
Customer's board	0.18 Ω	0.10 Ω	0.60 Ω	5.0 Ω	~1 GHz	600 Ω	

Note: 0909
(0.1MHz, 0.15 Ω)
(1MHz, 0.02 Ω)
(10MHz, 0.15 Ω)
(100MHz, 1.5 Ω)
(Resonance, 1GHz)
(Anti-resonance, 30 Ω)

Note: customer's
(0.1MHz, 0.18 Ω)
(1MHz, 0.1 Ω)
(10MHz, 0.6 Ω)
(100MHz, 5 Ω)
(Resonance, 1GHz)
(Anti-resonance, 600 Ω)

From simulation/experiment, we know that the small PDN impedance difference will cause unstable dram operation.

Therefore, we must lower the PDN impedance (from Vm source to BB/MCP Vm balls) as possible by following layout rule. That will let system become more robust.

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High Speed Memory Layout- Suggested routing order (Signal layout)

- Layout routing order (priority)
  - Please route traces in the following sequence:
    1. Power/GND plane
    2. Data group
    3. Clock group
    4. CMD/ADDR groups
  - Signal integrity (SI) is highly related to Power/GND plane, and data groups are operating at twice the clock frequency.

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High Speed Memory Layout-
Suggested routing order (Signal layout)

1. Data group (1/2)
   - DQx should be routed in a group and routed in the same layer and reduce via counts if possible.

     e.g.

     D[0:7] is aligned to DQS[0],

     D[8:15] is aligned to DQS[1].

Group	Signal Name	Description
Data	DQ[0:15] DQS[0:1] DM[0:1]	Data Bus Data Strobe Data Mask

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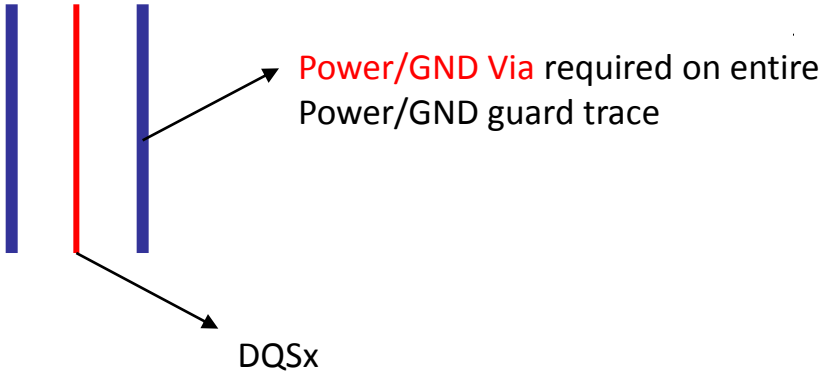
High Speed Memory Layout-
Suggested routing order (Signal layout)

1. Data group (2/2)
   - All different data group: (Max. trace length - Min. trace length) < 300mil “per byte” as possible.
   - To control/minimize the data-skew in 50ps for MT6276/MT6573 is necessary.
   - To reduce the crosstalk on DQSx , Power/GND guard is required.



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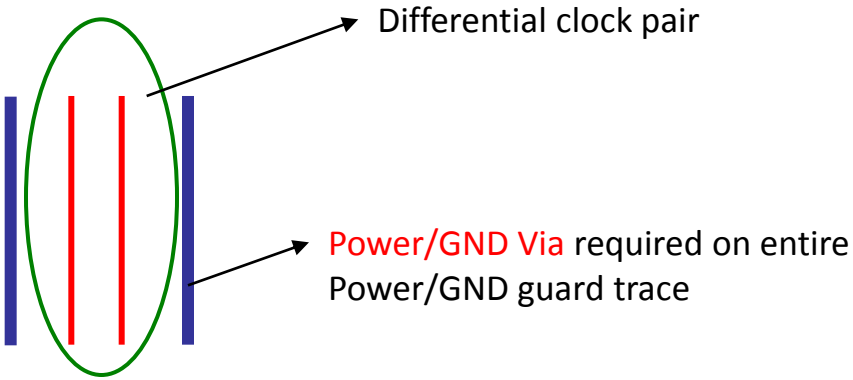
High Speed Memory Layout-
Suggested routing order (Signal layout)

2. Clock group
   - Every trace must have solid Power/GND plane near the entire route.
   - Route these 2 clock traces in parallel and keep equal trace length.
   - Within a clock pair:
     (Max. trace length – 50 mil) < Trace length < (Max. trace length),



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High Speed Memory Layout-
Suggested routing order (Signal layout)

3. Control/Command groups
   - Every trace must have solid power and ground plane near the entire route.
   - Within CMD/ADDR group:
     |Max. (CMD/ADDR trace length) – Min. (CMD/ADDR trace length)|
     < 600 mil as possible

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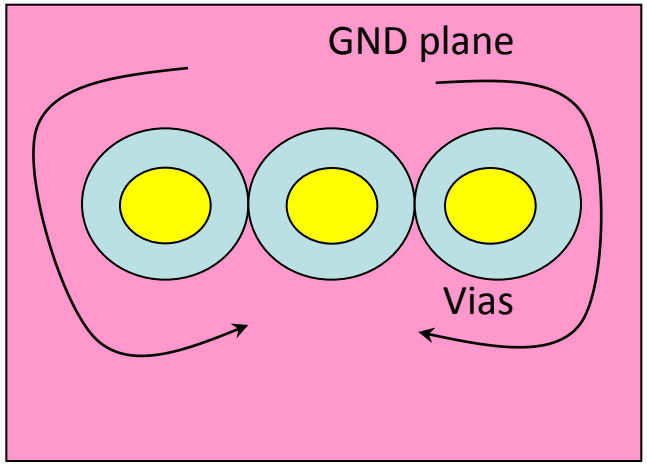
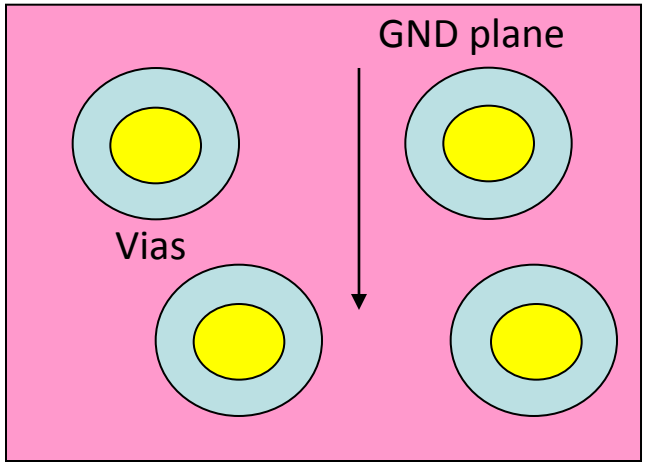
High Speed Memory Layout – Other general layout considerations

- All bypass capacitors must be placed as close to the devices' power balls as possible, and GND of all capacitors should keep the shortest trace route to the GND plane.
- Avoid other sensitive traces near the memory traces.
- Increase traces' spacing as possible.
- On the GND plane, do not block the GND return currents, as shown in the left figure.



Bad current return path



Good current return path

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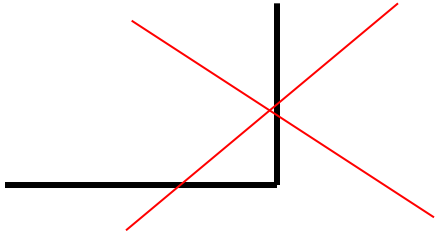
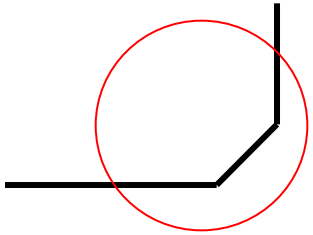
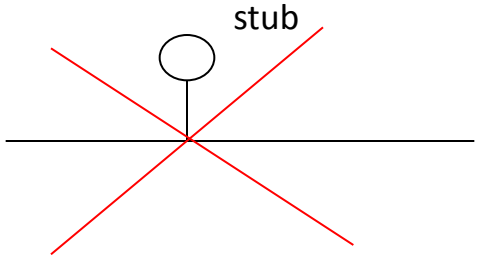
High Speed Memory Layout – Other general layout considerations

- When it becomes necessary to turn 90°, make two 45° turns or an arc instead of making a single 90° turn. By making two 45° turns or an arc, it reduces reflections on the signals with impedance discontinuities minimized.





- Avoid creating unnecessary stubs on data lines, if a stub is unavoidable, please keep the stub as short as possible.



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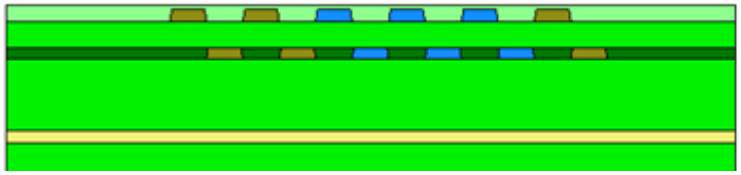
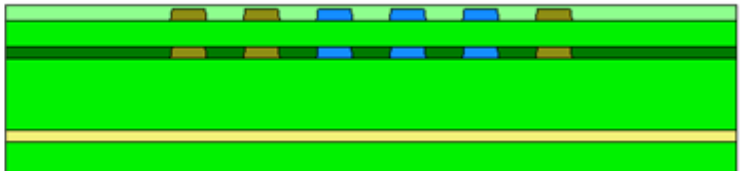
High Speed Memory Layout – Other general layout considerations

- If two adjacent layers are signal layers, please avoid routing signal trace in Overlap method as the following picture.

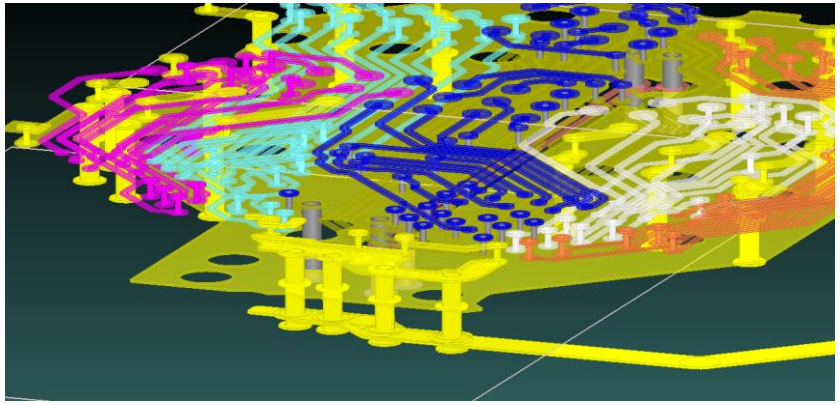


Interleave (O)



Overlap (X)

- Please check if the power via quantity(power plane to power pins) is optimized.



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Layout check list & priority

- Layout review list & priority: (Placement➔ PI➔ SI)
  - Placement: MCP must be put close to BB EMI pin group area. (NFI don't care)
  - Power: Solid power plane/via(1)plane size: to cover BB/MCP Vm pins(2)BB Vm buried/blind via quantity >= 3 (Notice the GND plane/via quantity, too)
  - De-caps must be close to BB/MCP Vm pins
  - The signal traces must have 『Solid』 reference plane, it can be Power/GND plane.
  - Differential ECLK & EDQSx must have Power/GND guard trace.
  - For MT6573/MT6276, please follow the trace length limitation ("package + PCB" trace length, please refer to module layout SOP document).
  - MT6236/MT6516/MT6268 ED/EA trace length limitation, to do your best is fine.
- Vcore layout **must be** also taken care of, like "PDN improvement(3)" page of the slide, except power plane.

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Confidential B

Design Notice - PMU

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Content

- MT6573 Introduction
  - General description
  - Block diagram
  - Buck/LDO list
- Comparison
- Function Description
- Reference design
- Appendix

MT6573 PMU – General Description

- The MT6573 built-in high performance power management IC.
- Highly integrated functions fulfill all power requirement in smart phone system
  - Buck converter x 5 (AP core, MD core, IO/memory, RF, PA)
  - LDOs
    - Analog LDO * 4
    - Digital LDO * 9
  - Charger controller
    - AC/USB
    - Pulse-Charger
  - Driver
    - Keypad back-light * 1
  - Gas Gauge

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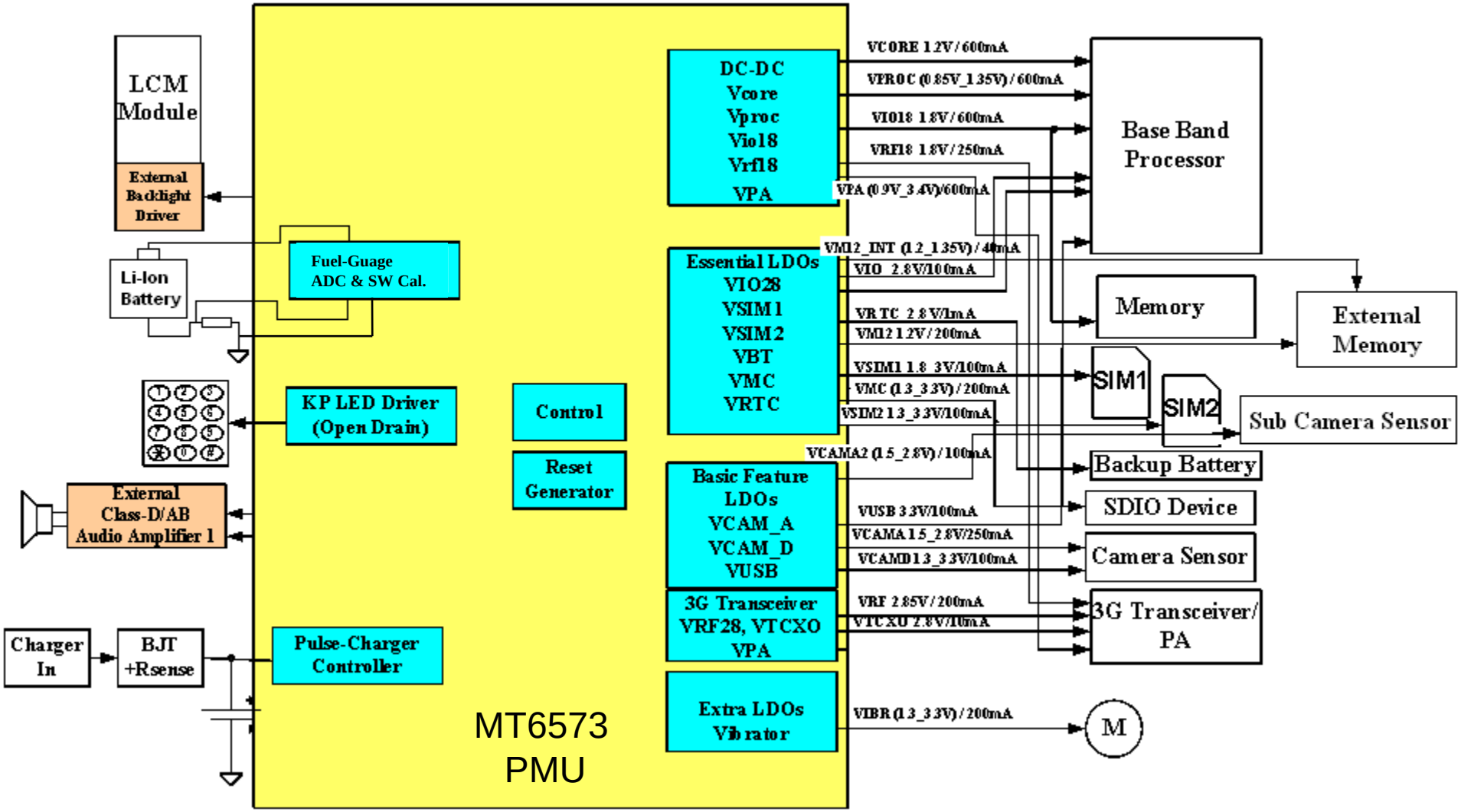
MT6573 Introduction – Block Diagram



MT6573 Regulators List

Vcore/Vio18/Vproc/VRF18/Vpa need near-end bypass cap

Regulator	Output Voltage (V)	Output Current (mA)	Output Components	Notes
VCORE	**0.8~1.3V**	600	2.2uH + 4.7uF	
VIO18	1.8V	600	2.2uH + 4.7uF	
VPROC	**0.85~1.35V**	600	2.2uH + 4.7uF	
VRF18	1.8V	250	2.2uH + 4.7uF	
VPA	0.9~3.4V	800	4.7uH + 2.2uF	4.7uH (Rated current base on inductor change > 1A
VIO28	2.8V	100	1uF	Far-end bypass cap
VRF28	2.85V	200	2.2uF+1uF	Far-end bypass cap
VSIM	1.8/3V	100	1uF	Far-end bypass cap
VTCXO	2.8V	10	1uF	Far-end bypass cap
VSIM2	1.3/1.5/1.8/2.5/2.8/3.0/3.3V	100	1uF	Far-end bypass cap
VUSB	3.3V	100	1uF	Far-end bypass cap
VM12	1.2V	200	1uF	Far-end bypass cap
VM12_INT	1.2~1.35V	40mA	1uF	Far-end bypass cap
VCAM_A	1.5 / 1.8 / 2.5 / 2.8V	250	2.2uF	Far-end bypass cap
VCAMA2	1.5 / 1.8 / 2.5 / 2.8V	100	1uF	Far-end bypass cap
VCAM_D	1.3/1.5/1.8/2.5/2.8/3.0/3.3V	100	1uF	Far-end bypass cap
VCAMD2	1.3/1.5/1.8/2.5/2.8/3.0/3.3V	100	1uF	Far-end bypass cap
VMC	1.3/1.5/1.8/2.5/2.8/3.0/3.3V	200	1uF	Far-end bypass cap
VIBR	1.3/1.5/1.8/2.5/2.8/3.0/3.3V	200	1uF	Far-end bypass cap
VRTC	2.8V	1.0	0.1uF	Backup battery

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MT6573 PMU Spec Summary

Function	MT6326 PMIC	MT6573 PMU
Buck Converter	4	5
LDO	19	20 (Include internal LDOs)
Driver	1. Keypad LED 2. Vibrator 3. B/L driver 4. Flash light driver 5. USB OTG switch	1. Keypad LED 2. Vibrator use LDO
Audio	1. Class-D Amplifier x 2 2. Audio Switch	X
Others	1. Analog switch	1. Dual SIM L/S
Charger	1. Linear Charger	1. Pulse Charger 2. Gas Gauge

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- MT6573 Introduction
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- Function Description
  - Power on Timing
  - Buck
  - Driver
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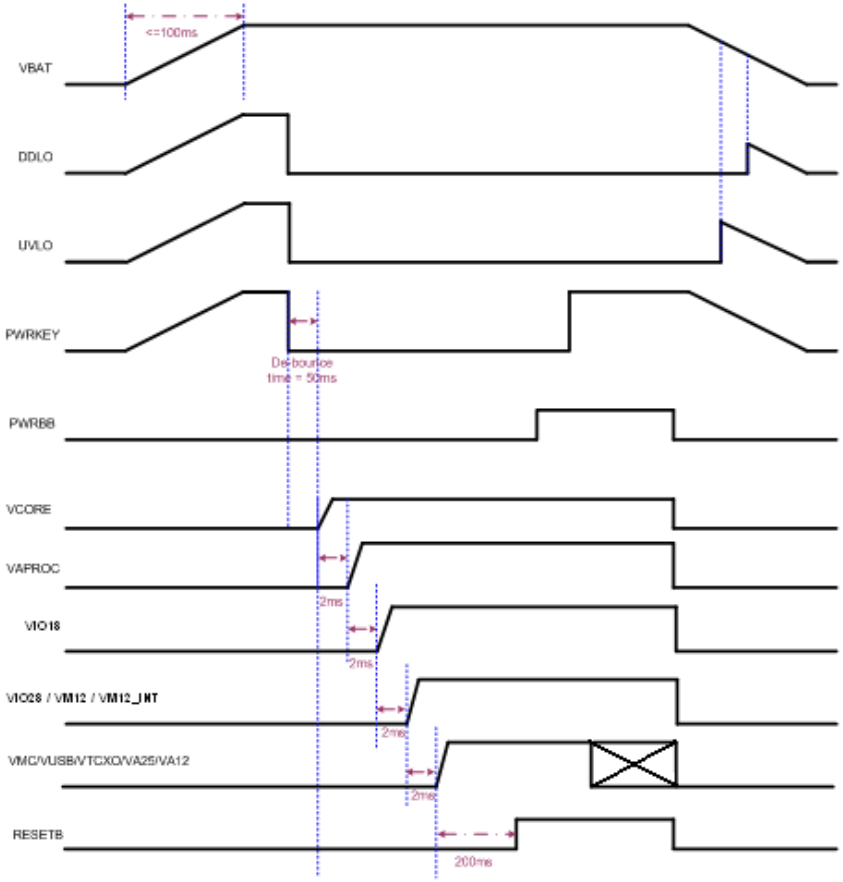
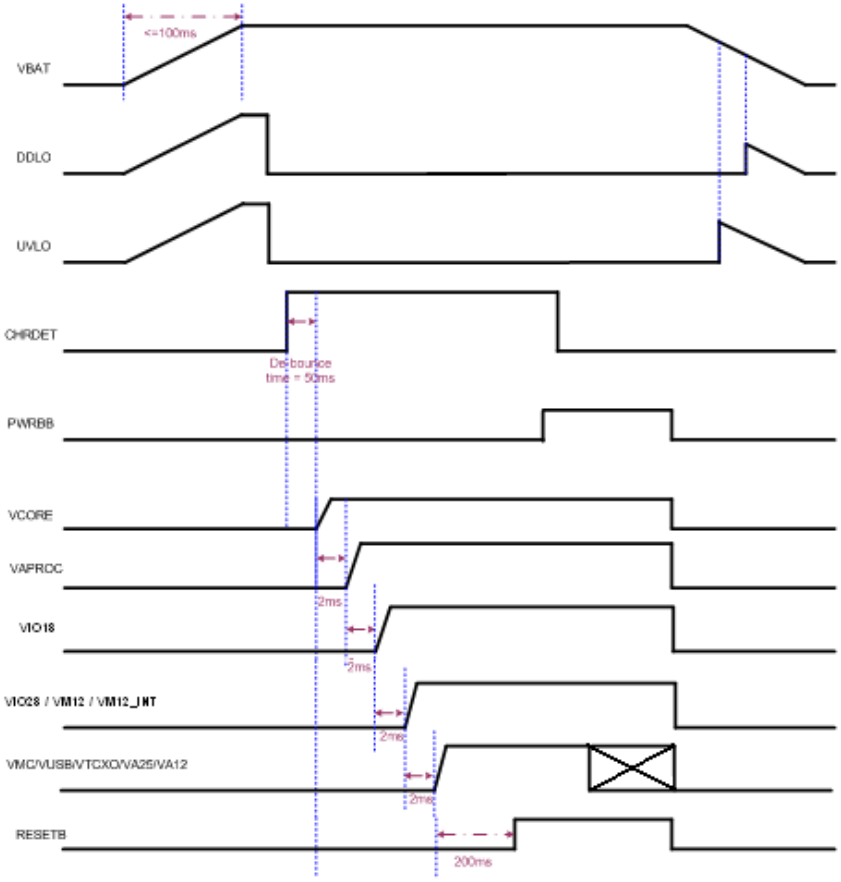
Function Description - Power On/OFF Timing Control

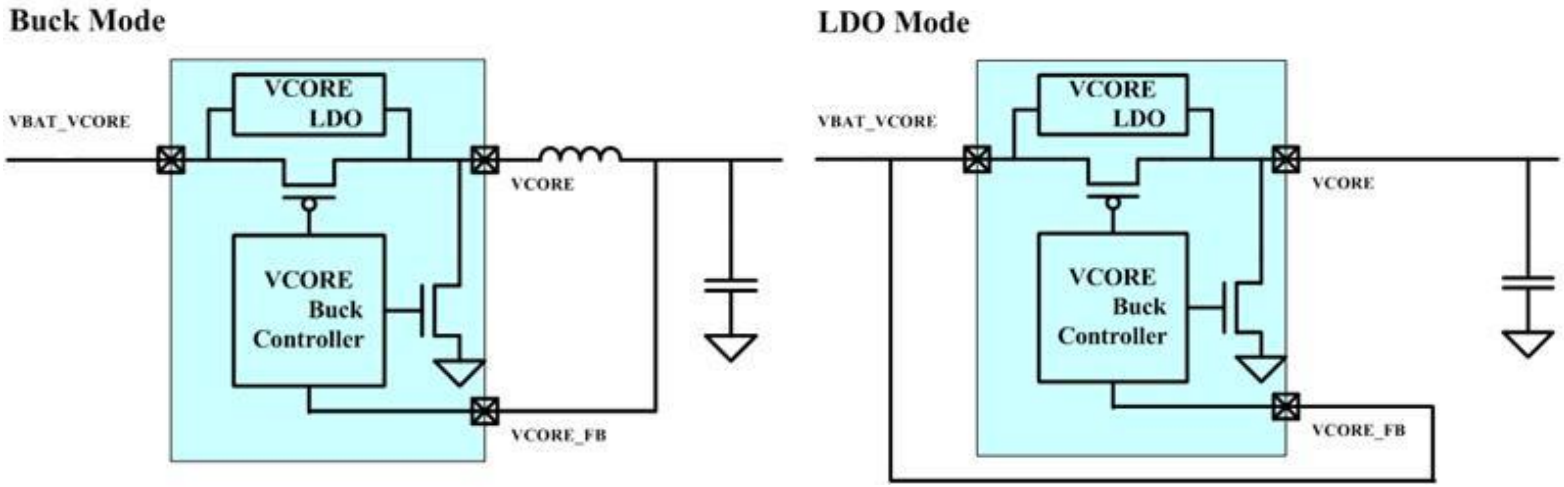


Press PWRKEY



Charger Plug-in

Function Description - Buck Converter (VRF18) With LDO Mode



- V_{RF18} also provide LDO mode for lower cost requirement.
  - VRF18 (Buck/LDO: 250/100mA)
- Buck mode: VRF18_FB connect to the output capacitor.
- LDO mode: VRF18_FB connect to VBAT.

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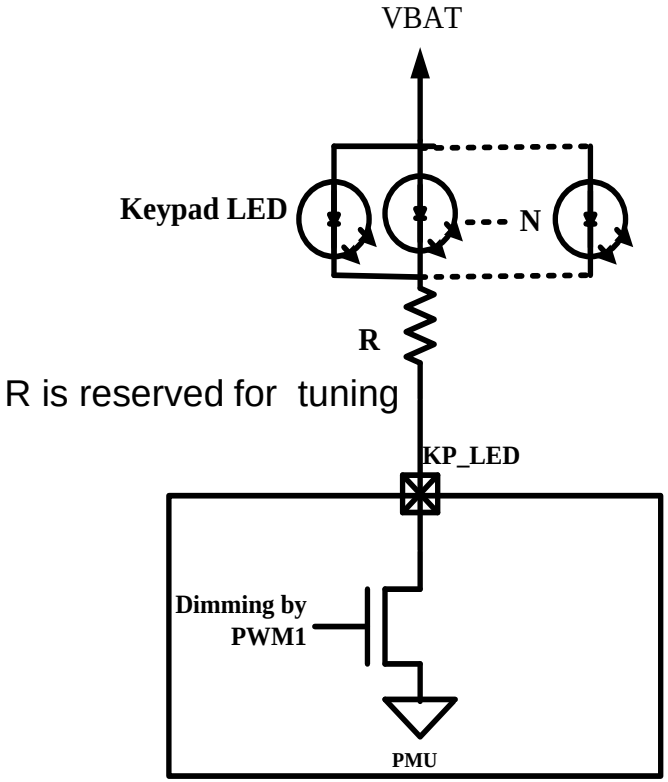
Function Description - KP_LED Driver



KPLED_MODE KPLED enable mode select

0 Pwm mode, controlled by hardware **PWM1** output signal

1 Register control mode (see the KPLED_EN to turn-on)

Content

- MT6573 Introduction
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  - **Schematic**
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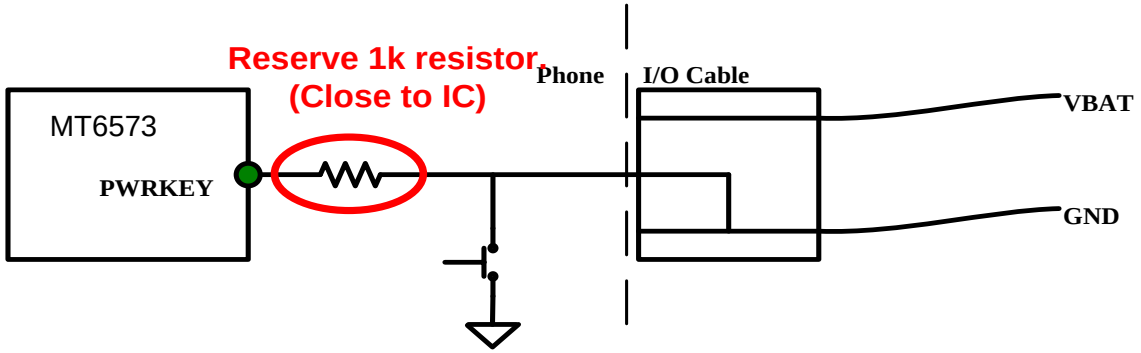
Typical Application

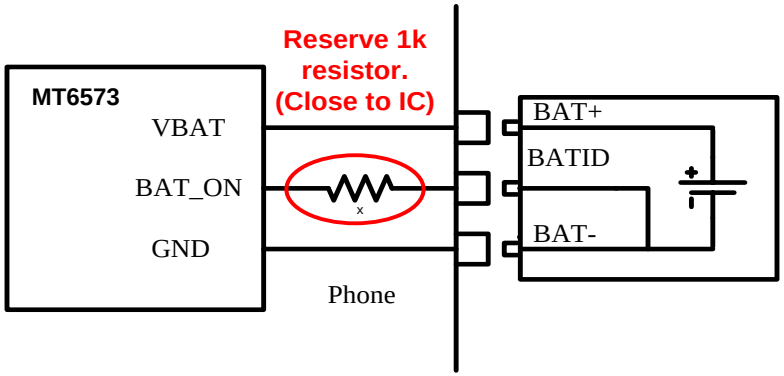
MT6573 Features		Vout	I_max	Application
LDO	VMC	SW Setting	200	Memory Card
	VSIM2	SW Setting	100	SIM2
	VIBR	SW Setting	200	Vibrator
	KP_LED	150mA		KEYPAD
	Backlight	x		External backlight Driver
Audio Amplifier	Class D			External Audio Amplifier

Reference design - Schematic
IC Protection: PWRKEY and BAT_ON

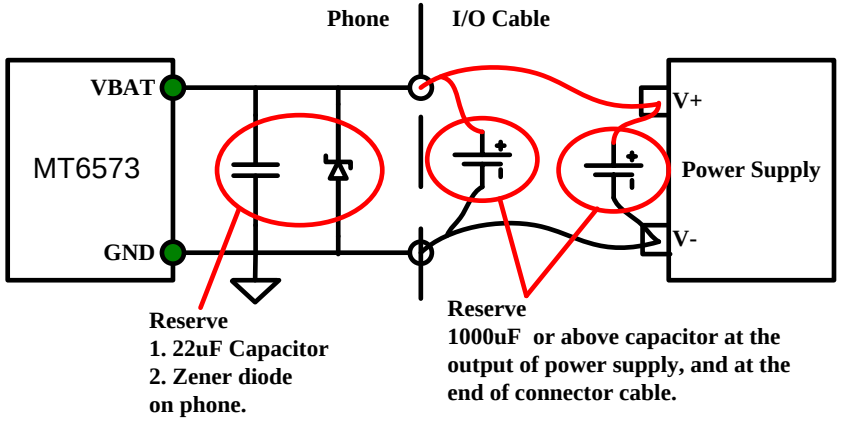


Please reserve 1k resistor on phone PCB to protect **PWRKEY** no matter if PWRKEY connect to any I/O connector or not.

Please reserve 1k resistor on phone PCB to protect **BAT_ON** pin if BAT_ON is used to detect battery.



Reference design - Schematic
IC Protection: VBAT



MT6573 has lower VBAT voltage rating. (Max. 4.3V.) Some protection should reserve to prevent the damage by voltage surge.

•Design notice in Phone side:
1. At least 22uF capacitor.
2. Add Zener diode (5.1V/500mW) to protect the IC against low frequency voltage surge. Put it between battery connector and MT6573.
Notice: If using IO connector or test point to supply VBAT for download, manufacture, or repair, should let VBAT trace passing zener diode and 22uF capacitor before entering IC.
Notice: Using 5.1V zener will introduce some leakage when VBAT = 4.2V.
•Design notice in Power Supply side:
Add 1000uF (or above) capacitor at the output of the power supply to reduce the voltage bounce caused by long power cable. And the power cable should be as short as possible. Also add 1000uF (or above) capacitor at the end of power cable (near phone side).

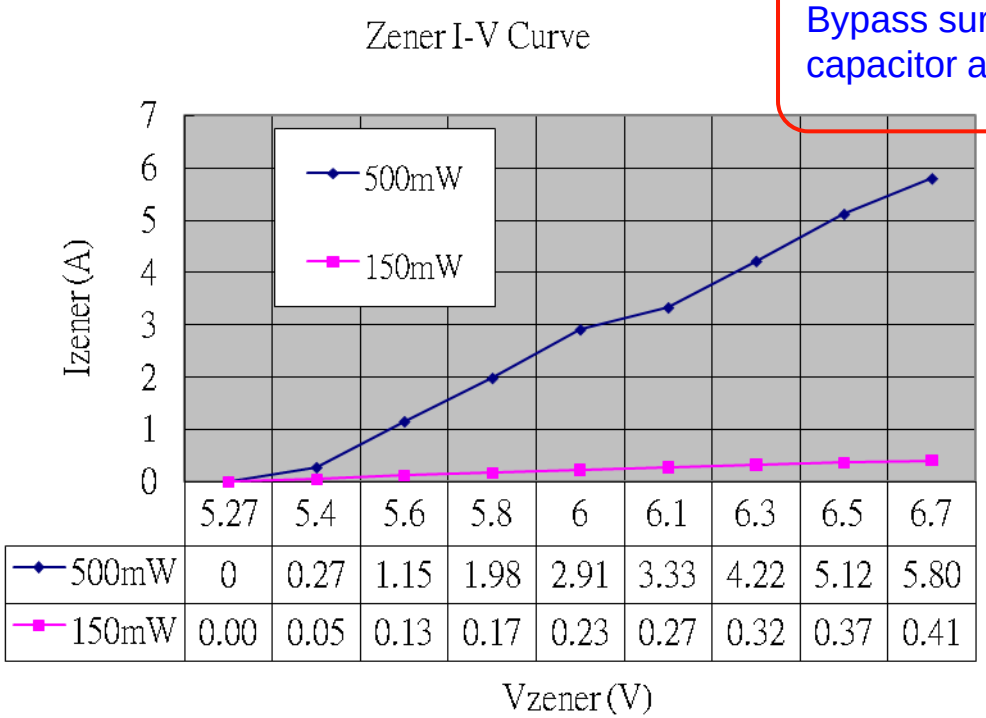
Zener Diode Selection Guideline

Selection Guideline

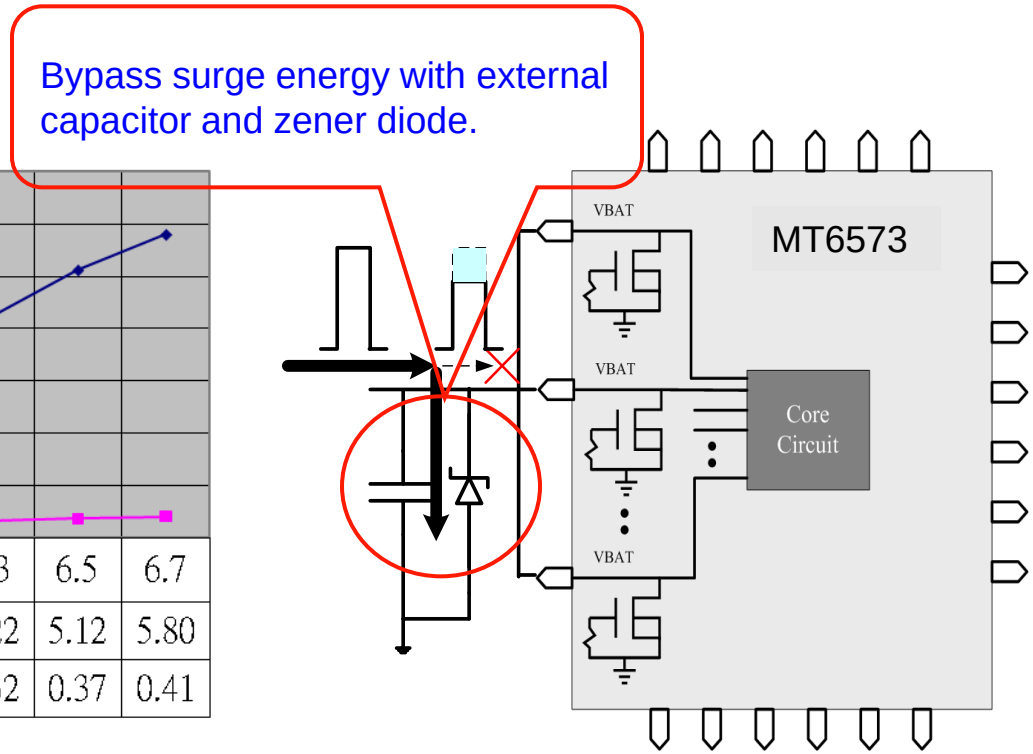
- 500mW zener diode has lower Z_{ZT} than 200mW and can sink more exceptional surge voltage/current.
- MT6573 must selcet 5.1V/500mW zener to enhance VBAT pin protection.
- Ir<100uA @Vr=4.2V, Ta=25°C, Using 5.1V zener will introduce some leakage when VBAT = 4.2V. Large Ir current will introduce more leakage current.

500mW Zener diode

- Change Zener diode to 5.1V/500mW
  - 150mW zener has similar current sink capability, can only release part of the external pulse energy.
  - 500mW zener can share more than 90% of external energy.



	5.27	5.4	5.6	5.8	6	6.1	6.3	6.5	6.7
500mW	0	0.27	1.15	1.98	2.91	3.33	4.22	5.12	5.80
150mW	0.00	0.05	0.13	0.17	0.23	0.27	0.32	0.37	0.41



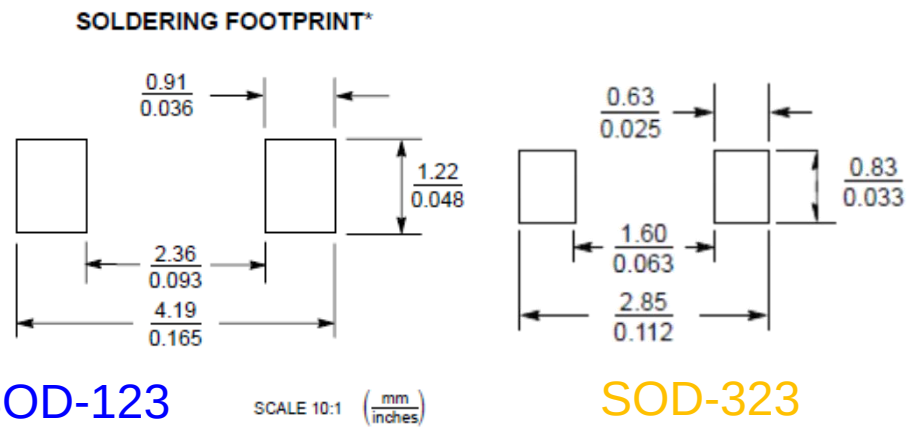
Zener Diode Validation List

- For design in,please notice the parts shipping delivery time.
- The latest validation list, please access the MTK BBS web.

Item	Vendor	Part number	Power (Watts)	Package	IR(uA) @VR=4.2V	Contact Window
1	On semi	MMSZ5231BT1G	**500mW**	SOD123	9	Tony Kao, 886-2-23761153 886-987-265-997 Email: tony.kao@onsemi.com
2	JIANGSU CHANGJIANG (长电科技)	MMSZ5231B	**500mW**	SOD123	72	Mr. Chan 0510-86858061 13601525970 E-mail: cyz@cj-elec.com
3	Prisemi	PZ3D4V2H	**500mW**	SOD323	11.5	欧新华 Mobile:18602108386 Tel: +86-21-60870158-8018 Email: ken.ou@prisemi.com
4	Prisemi	PZ5D4V2H	**500mW**	SOD523	4.85	
5	Vishay	MMSZ4689-V	**500mW**	SOD123	7	Mike_Wang 886-911313660 mike.wang@Vishay.com
6	Crownpo	CDZ55C5V1SM	**500mW**	0805	10.2	陳富榮Sam 138-12888205 Email: sam@sh-selmag.com

Co-Layout

- For 2nd source parts concern, co-layout is flexible to select parts vender.
- SOD-123 and SOD-323 are most popular package of 500mW Zener and can co-layout . For thermal dissipation concern, SOD-123 and SOD-323 are fist choice and then SOD-523.
- For safety operation area, please notice the steady state power rerating and should exposed pad to a large copper.

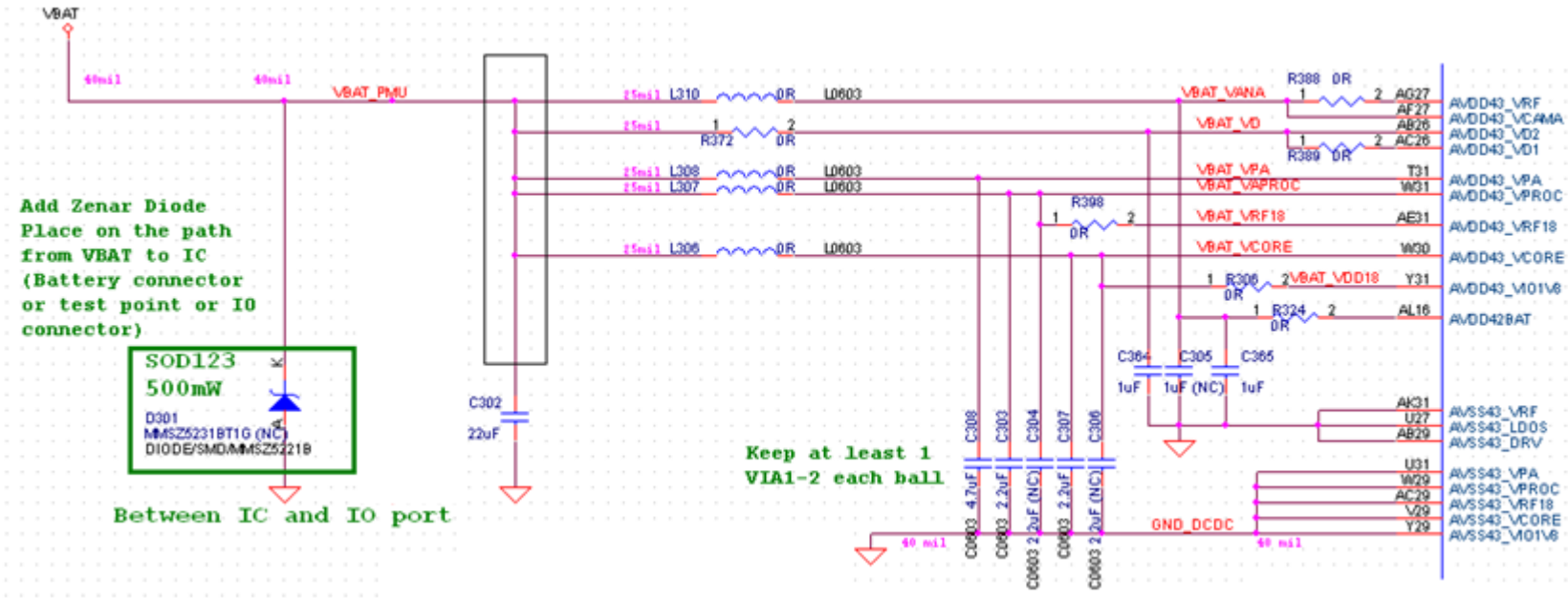


SOD-123

SOD-323

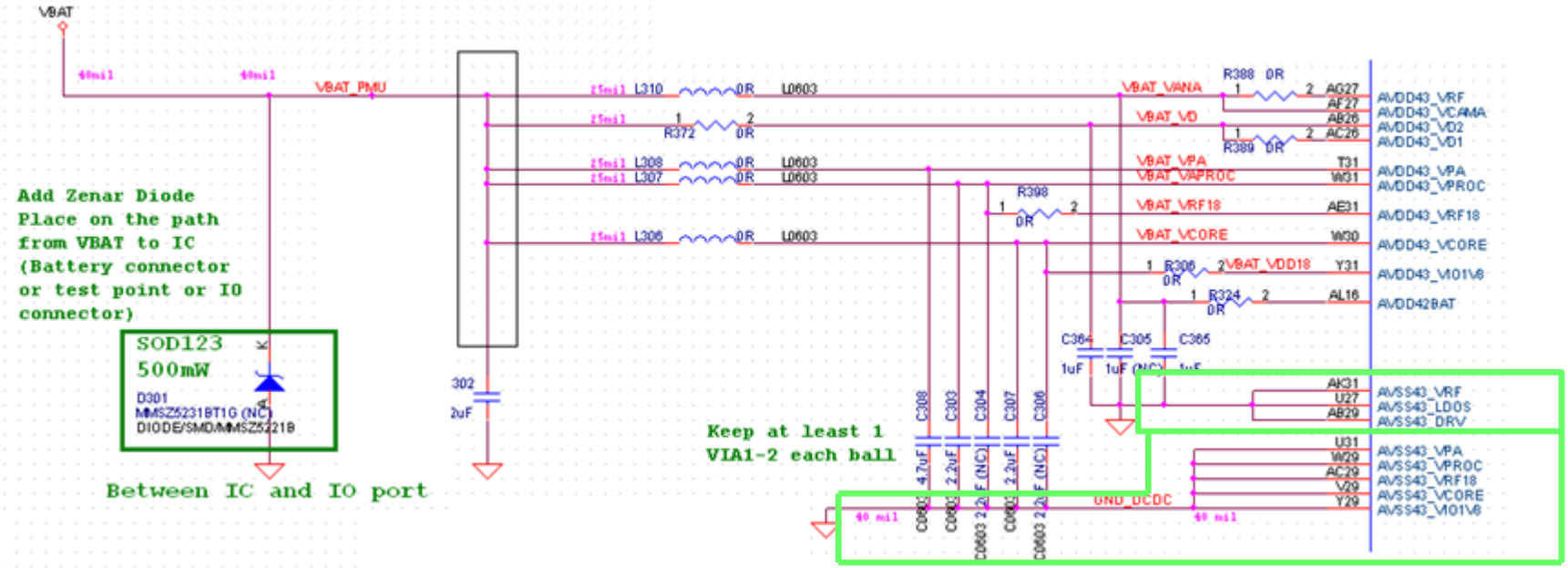
SOD-123/ SOD-323

Reference design - Schematic
VBAT Input Filter 1/2



- VBAT input should reserve enough filter to prevent interference to RF performance.
- All bypass cap. should be as close to MT6573 IC as possible
- Bead selection: Rated Current > 1000mA, DCR < 0.10ohm

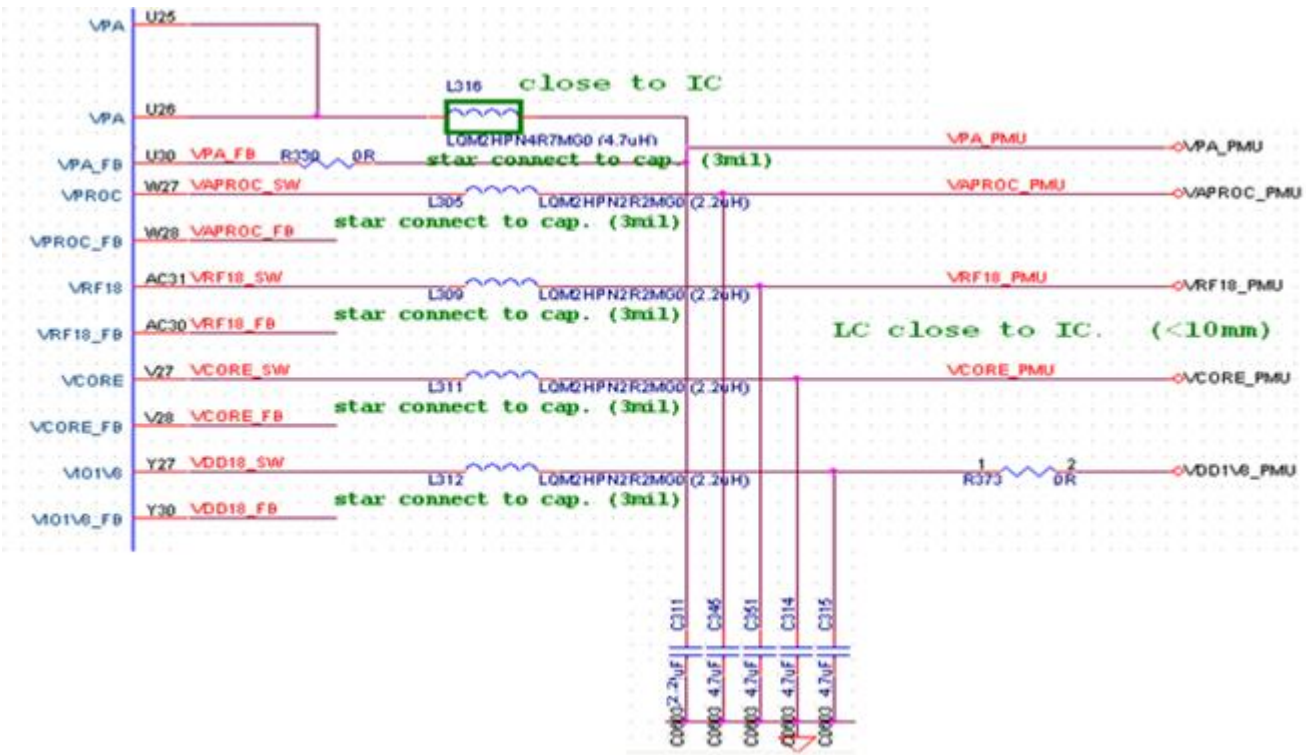
Reference design - Schematic
VBAT Input Filter 2/2



- VBAT input GND pin must first connect to input capacitor GND pin and then connect to system GND through VIA.

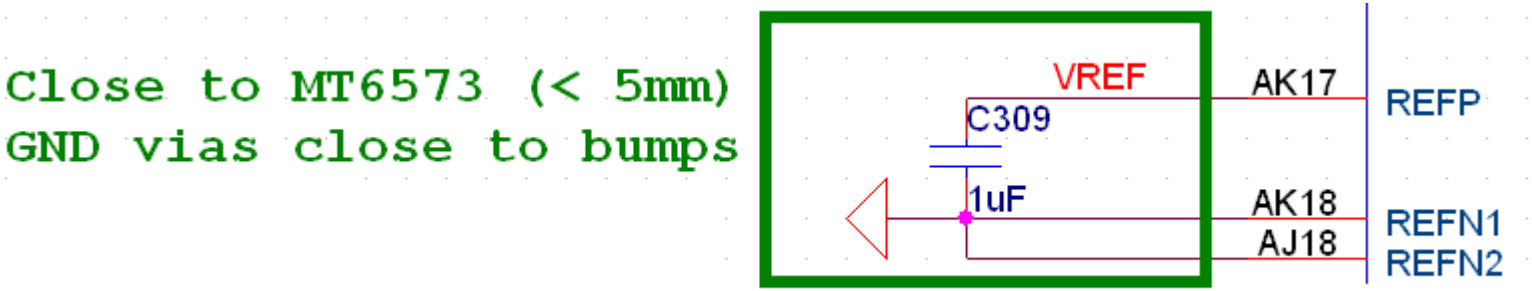
Reference design - Schematic

Output Capacitor: $V_{PA}/V_{PROC}/V_{RF18}/V_{CORE}/V_{IO18}$



- Put enough capacitors both at $V_{PA}/V_{CORE}/V_{PROC}/V_{IO18}/V_{RF18}$ to obtain good system stability.

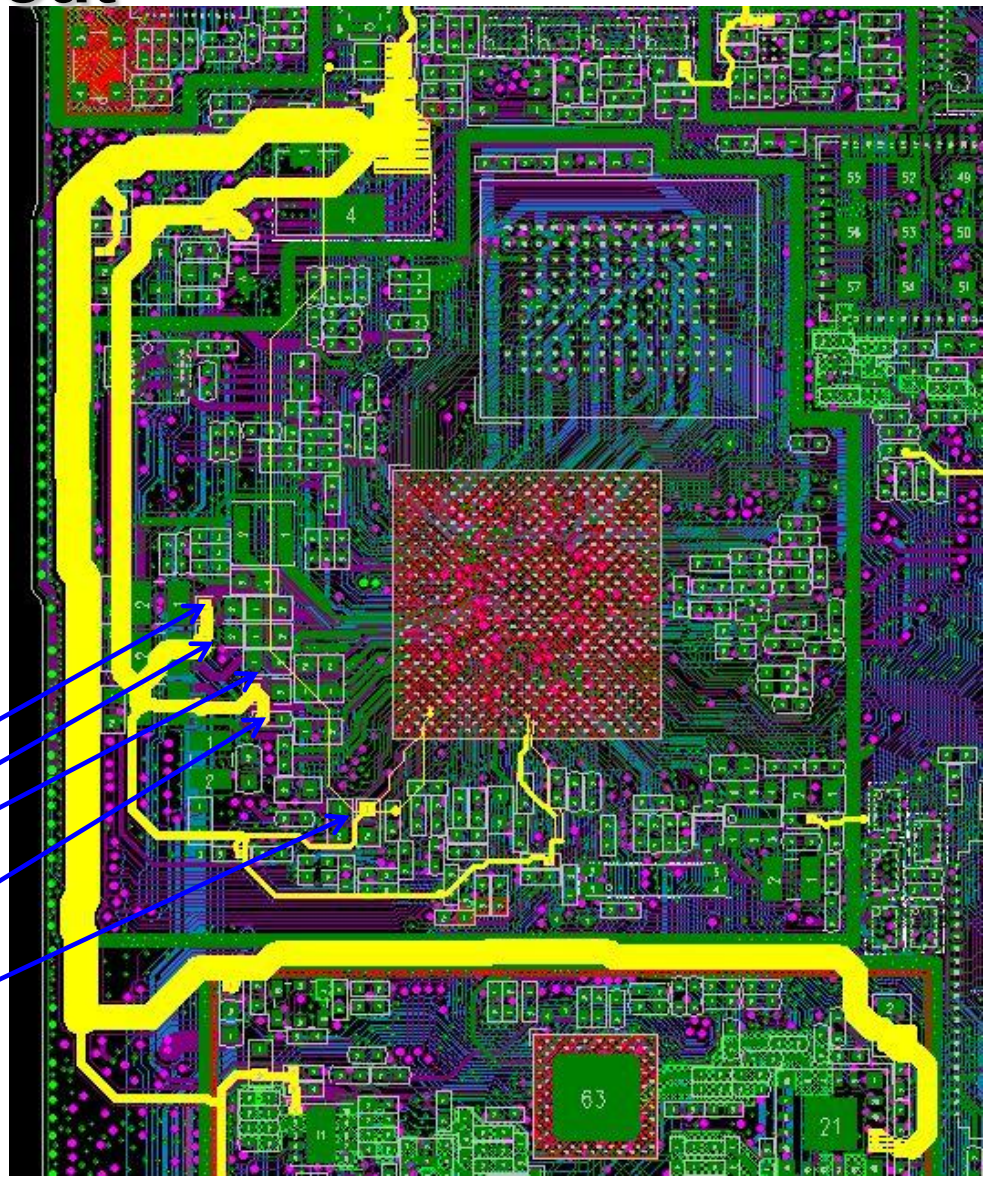
Reference design - Schematic
Bypass Capacitor for VREF



- Place 1uF/X5R for VREF and should be as close to MT6573 IC as possible
- REFN1/2 pins must first connect to input capacitor GND pin and then connect to system GND through VIA.

Reference design - Layout VBAT Traces

- Star-connect different VBAT group to BATTERY Connector directly



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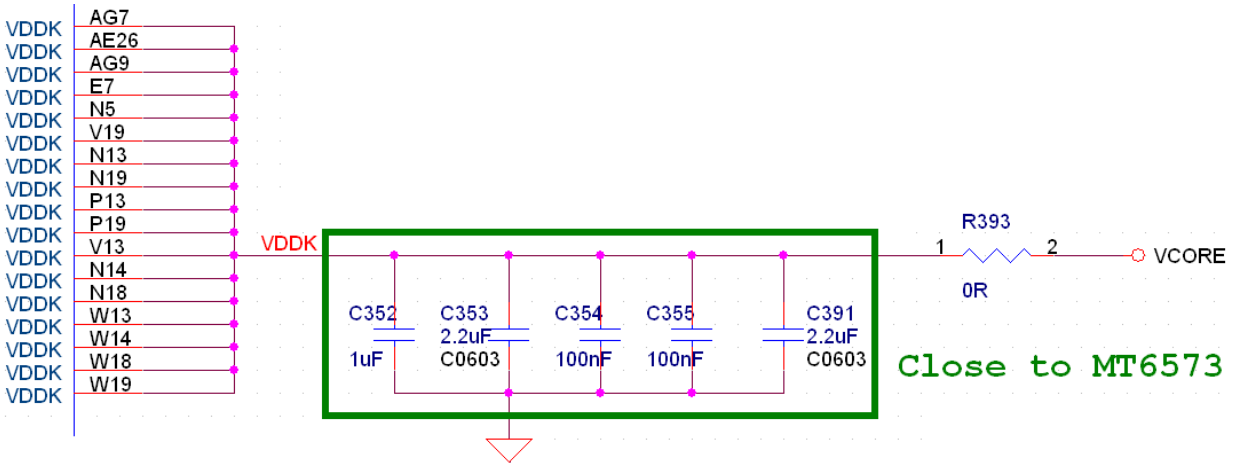
Reference design – Schematic

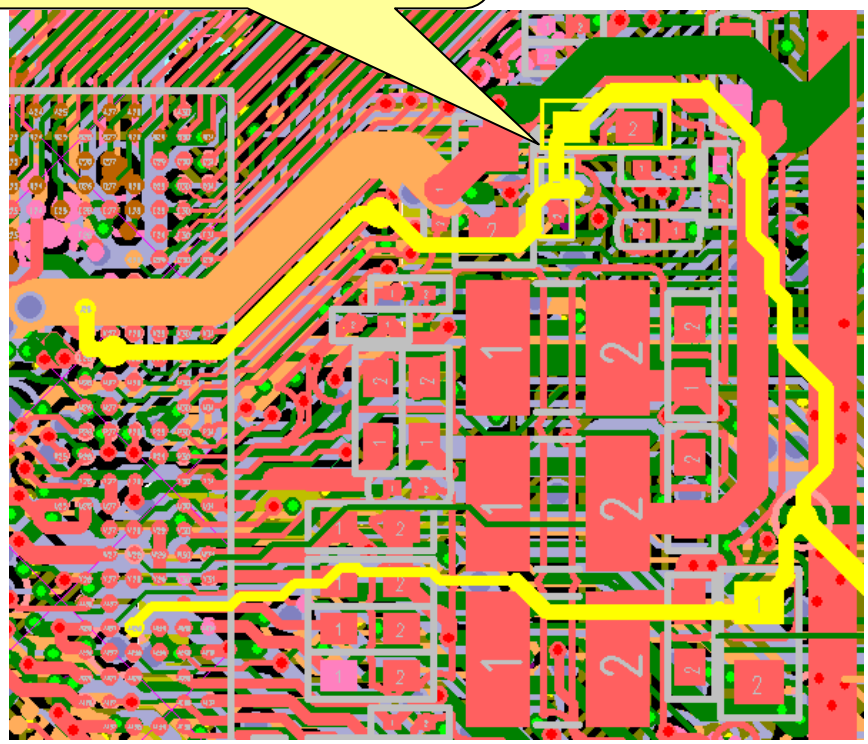
Bypass Capacitor for VCORE (near to Base-band)

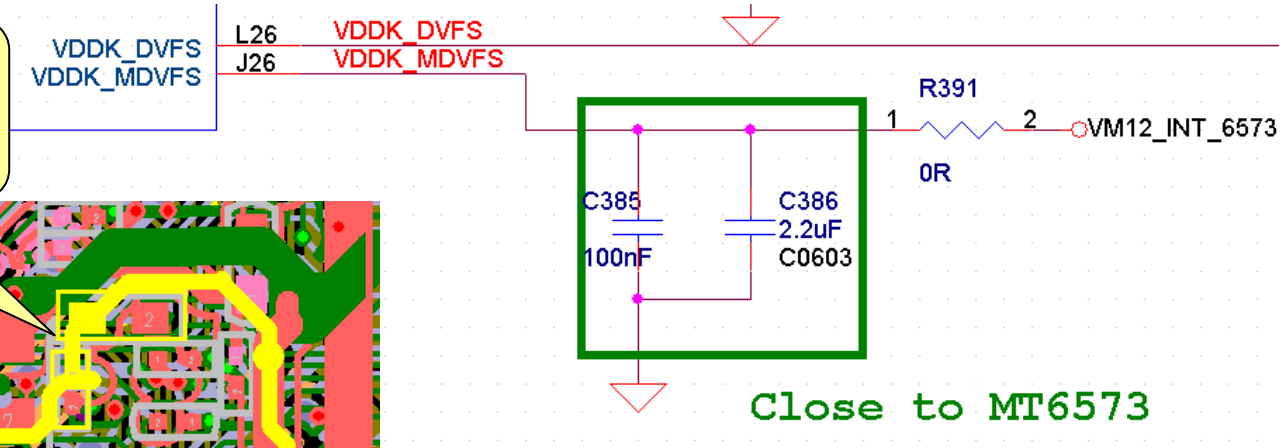


- Reserve enough bypass capacitors both at VCORE to obtain good system stability.

VM12_INT Layout Notice (Important!)

Please put de-cap (C385, C386) for VDDK_MDVFS as close as possible to main chip. And make sure power trace passing through capacitor before enter chip!





VM12_INT is for internal SRAM power ball J26 (VDDK_MDVFS), layout quality and de-coupling cap is important to system stability ! Please make sure capacitor on trace is effective.

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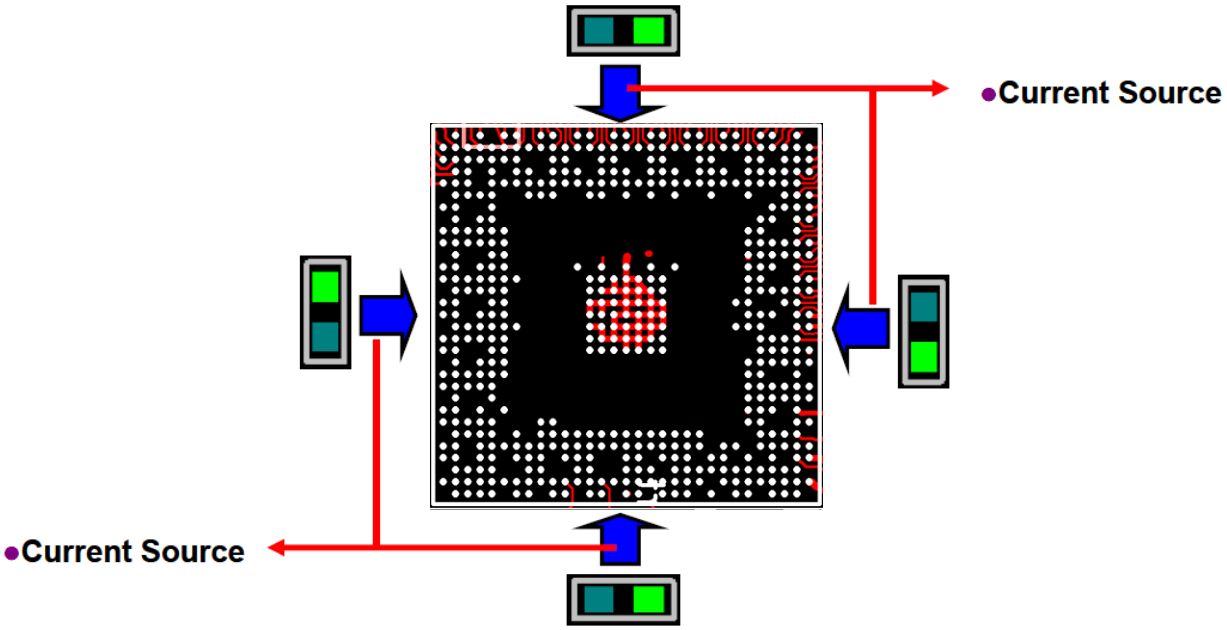
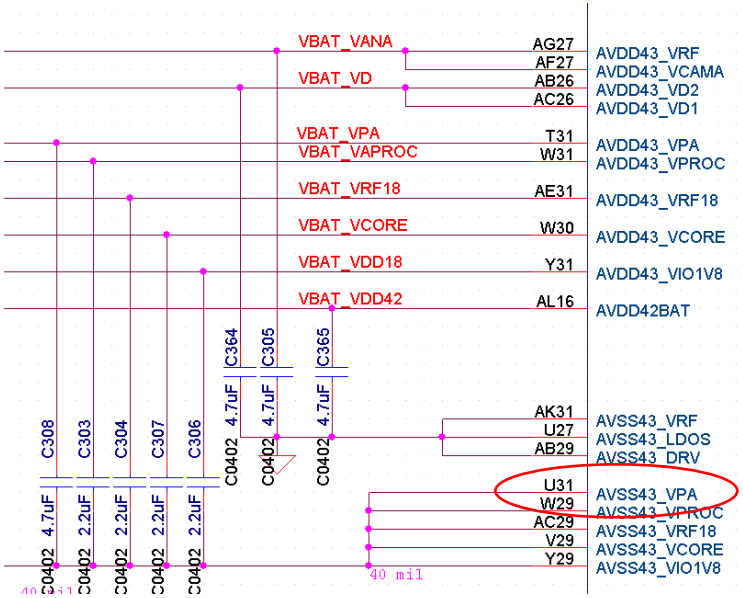
Reference design – Layout
Bypass Capacitor for VCORE (near to Baseband)

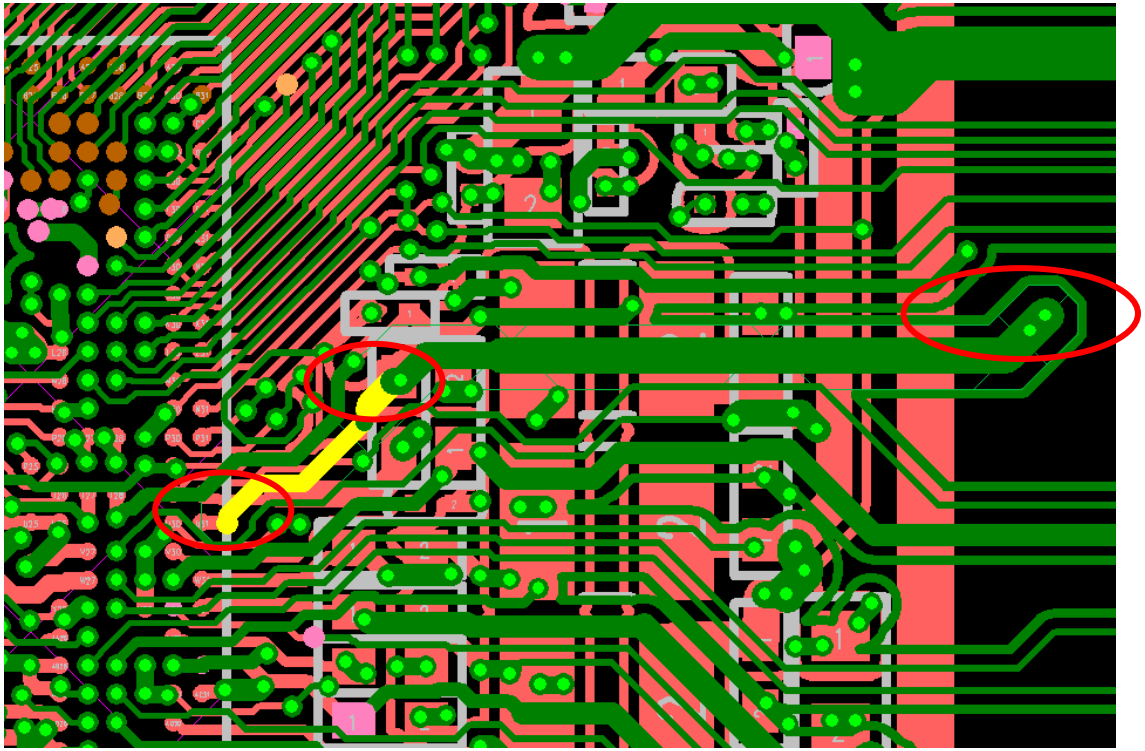


- Due to MT6573 has many Vcore (VDDK) balls, and those balls scatter around the package of MT6573. Put bypass capacitors around MT6573 to increase system reliability.

Reference design - Layout VPA GND Traces

- Star connect ball U31 (VPA ground) to input cap (C308) and go together for a distance then to main ground plate for the purpose of avoiding coupling internal circuit.





MTK Inductor Recommended Parts

- Only for VPA Application Notice.

Part Number	Manufacture
LQH3NPN4R7MJ0	Murata
NRH3012T4R7	Taiyo Yuden
VLS3012ET-4R7M	TDK
LVS303012-4R7M	奇力新

ELECTRICAL CHARACTERISTICS

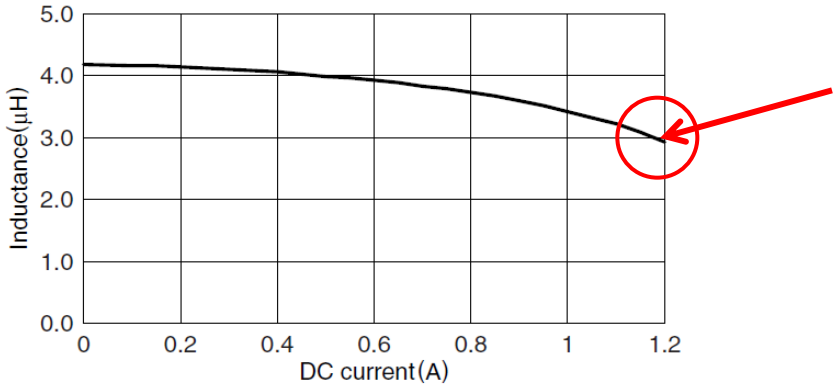
Part No.	Inductance (μH)	Inductance tolerance (%)	Test frequency (MHz)	DC resistance (Ω)		Rated current(A)*		
						Based on inductance change		Based on temperature rise
				max.	typ.	max.	typ.	typ.
VLS3012ET-4R7M	4.7	±20	1.0	0.156	0.130	0.95	1.05	1.30

- Those part has mentioned the rated current on temperature rise.
- DCR also need to consider for efficiency improving.

MTK Inductor & Capacitor Limitation

- VPA's Inductor Limitation.

TYPICAL ELECTRICAL CHARACTERISTICS
INDUCTANCE vs. DC SUPERPOSITION CHARACTERISTICS
VLS3012ET-4R7M



The inductor's value at DC current is 1.2A should be kept at or above 3uH is needed.

- VPA Total Capacitors Limitation.

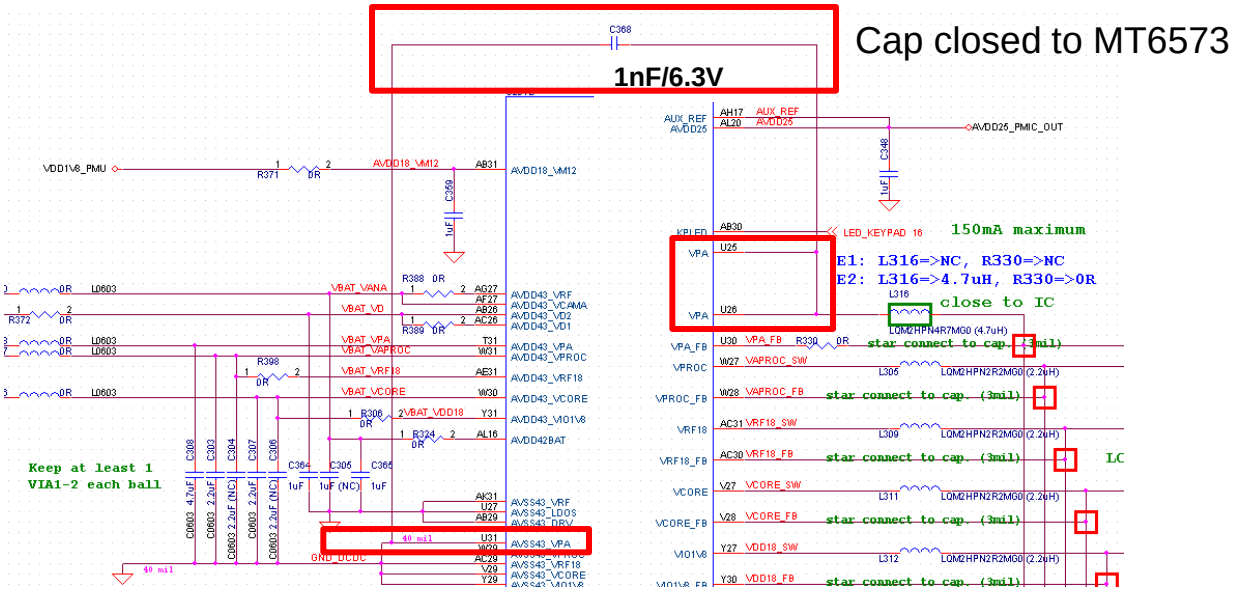
2.2uF (PMU-side) + 2.2uF (PA-side) < C_{total} < 2.2uF (PMU-side) + 2.2uF (PA-side) + 0.1uF x 4pcs

Bypass Capacitor Applied on VPA

- Only for VPA Application Notice.
- Low cost solution

  1) To enhance voltage rating of VPA, add a 1nF/6.3V capacitor between VPA and AVSS43_VPA is recommended.

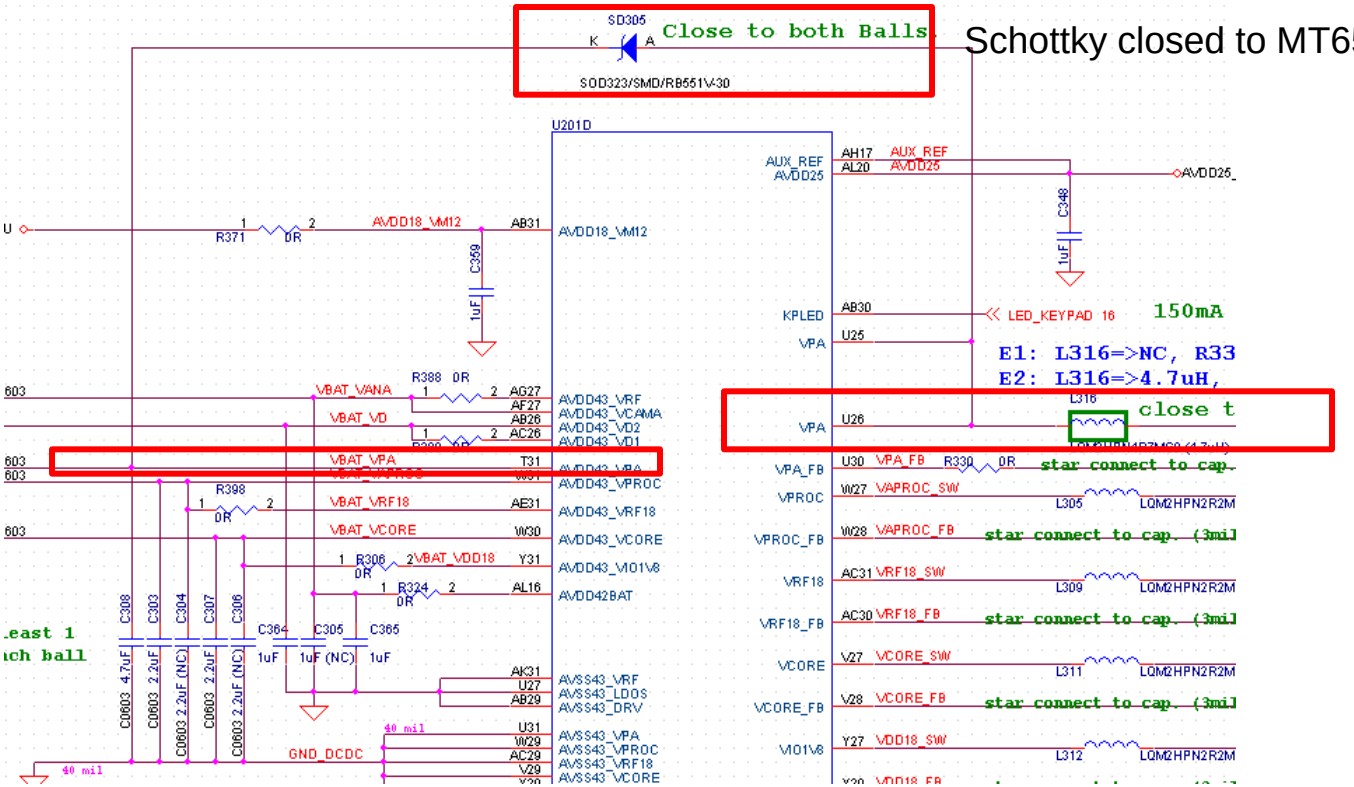
  2) The trace should be >8mil to reduce parasitic ESL.



Or … Schottky Diode Applied on VPA

- Only for VPA Application Notice.

  1) To enhance voltage rating of VPA, add a schottky diode between VBAT_PA & VPA is recommended.
  2) The trace should be >8mil to reduce parasitic ESL.



MTK Schottky Recommended Parts

- Only for VPA Application Notice.

Part Number	Manufacture
RB551V-30	ROHM

●**Absolute maximum ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Reverse voltage (repetitive peak)	V_{RM}	30	V
Reverse voltage (DC)	V_R	20	V
Average rectified forward current	Io	500	mA
Forward current surge peak (60Hz· 1cyc)	I_{FSM}	2	A
Junction temperature	Tj	125	°C
Storage temperature	Tstg	−40 to +125	°C

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_F1	-	-	0.36	V	I_F=100mA
	V_F2	-	-	0.47	V	I_F=500mA
Reverse current	I_R	-	-	100	μA	V_R=20V

- Should be consider the current rating on “Forward current surge peak”, over 2A is recommended.
- Forward voltage is less than 0.5V

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Design Notice - Pulse Charging

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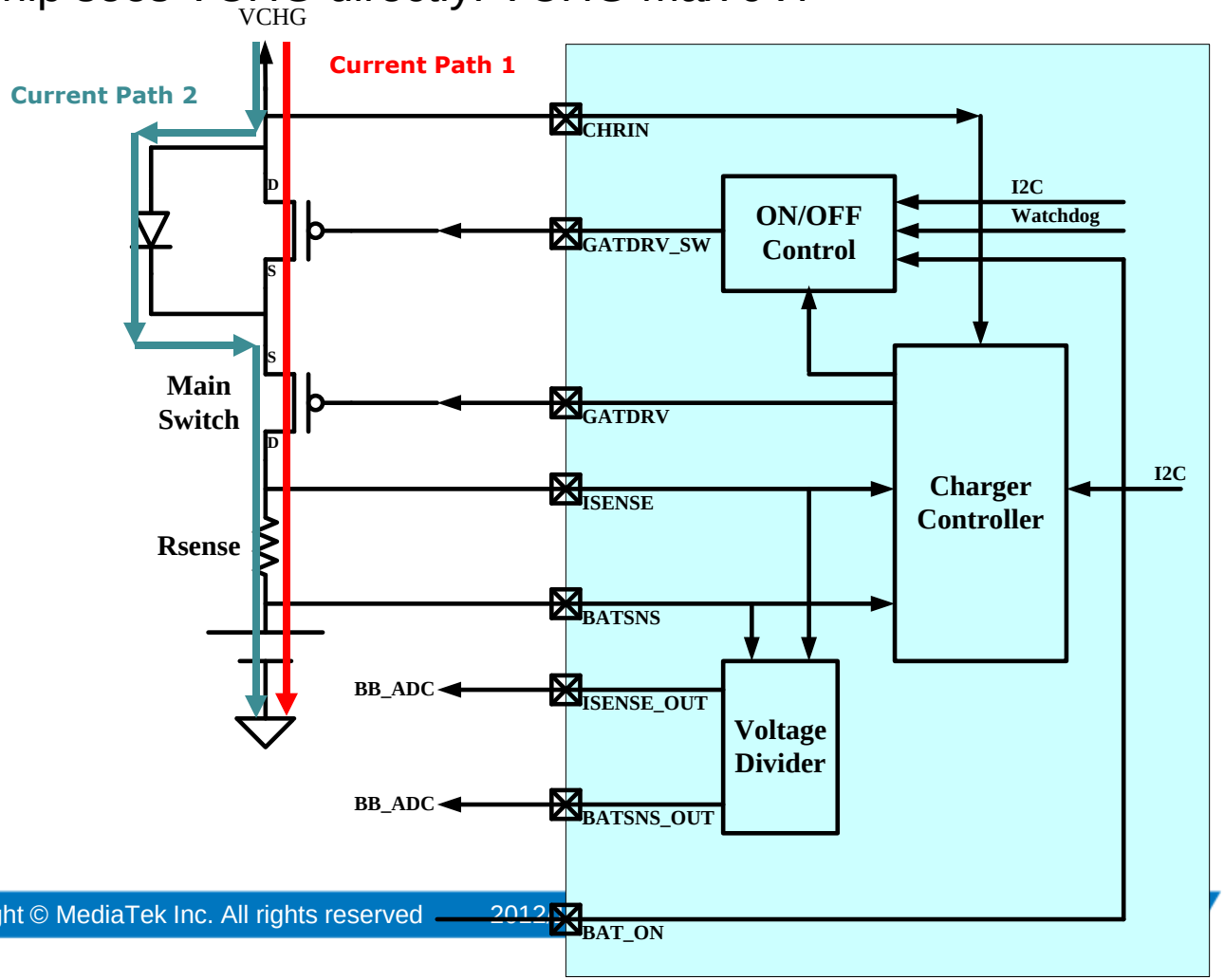
Linear Charger Hardware (MT6326)

- Software control enable/disable.
- Hardware control charge full by CV.
- Chip sees VCHG directly. VCHG max 9V.



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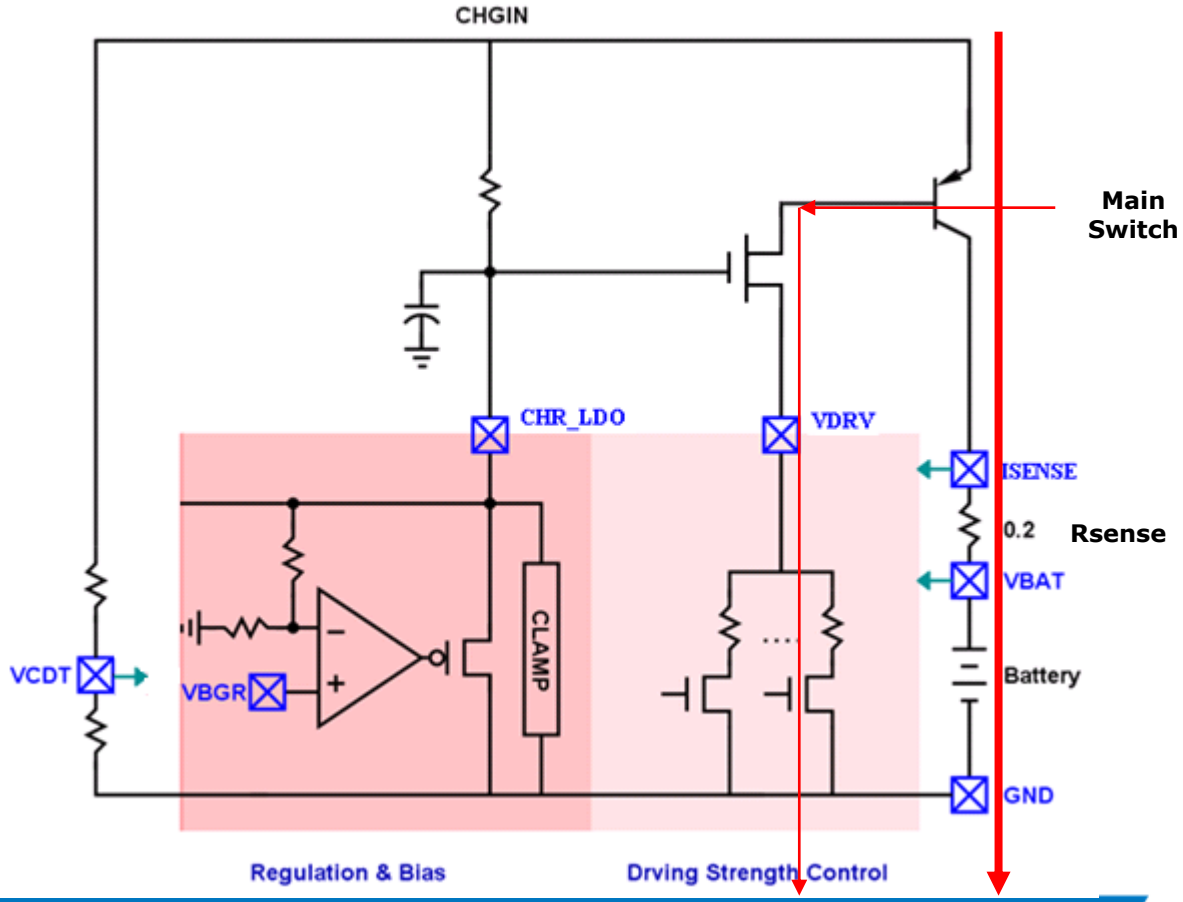
Pulse Charger Hardware

- Software control enable/disable, and detect charge full.
- Hardware protect by OV and watchdog timer.
- Chip doesn't see VCHG directly, VCHG max. 30V.



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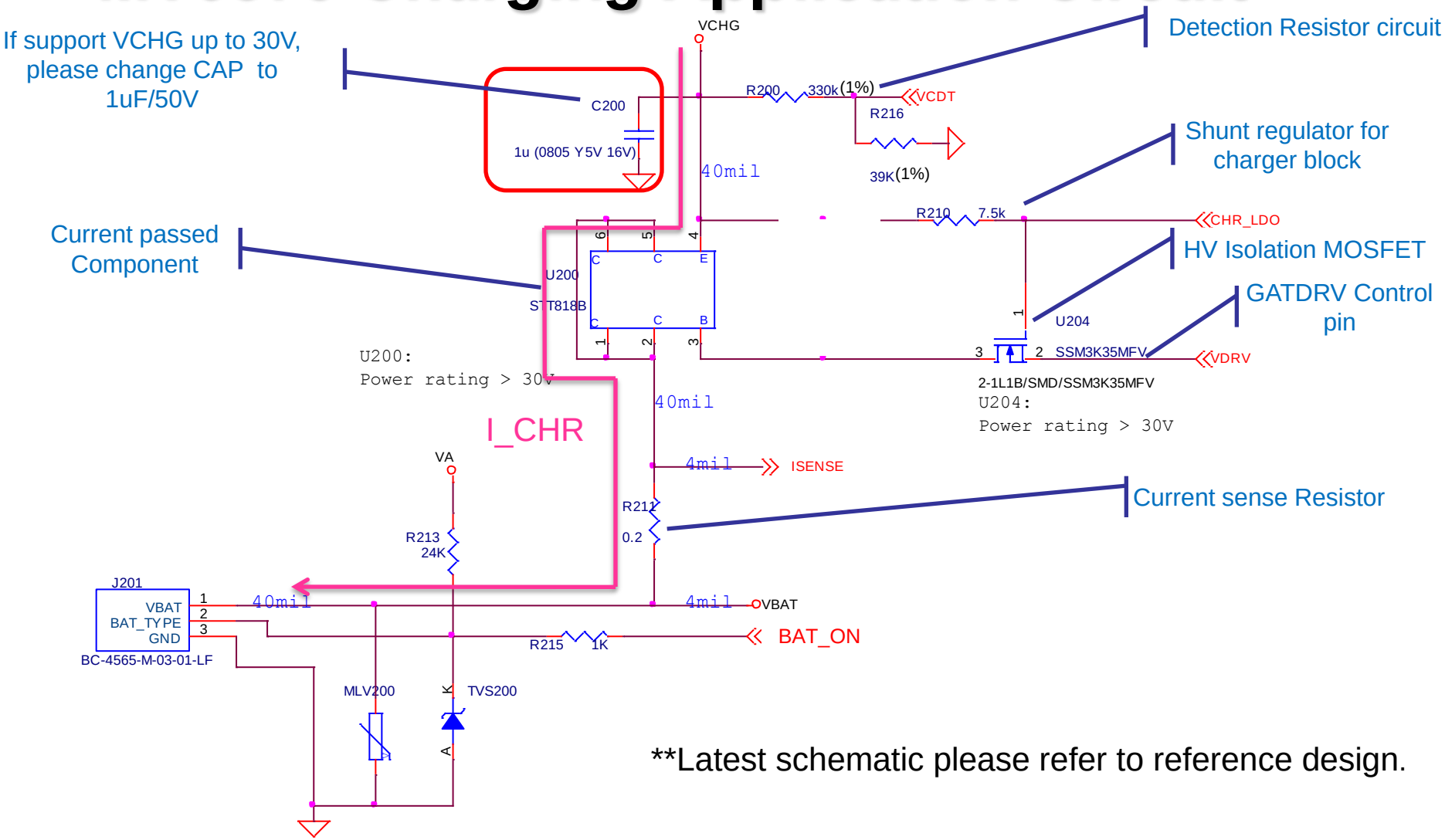
MT6573 Charging Feature Comparison

Chip Feature	MT6326	MT6573
Charging type	CC-CV	Pulse Charging
Maximum charger input voltage	9V	30V
Support battery type	Li-ion	Li-ion
VCHG OVP	7V	10.5V(Maximum) (Default HW protection is 7V)
CV	4.2V	4.2V comparator
CC	160mV/R	160mV/R
Pre_ charge	25mV/R	70mA(USB)/200mA(AC)
Battery OVP	4.3V	4.35V
Watchdog timer	Yes	Yes
Pre-charge safety timer	NO	35 minutes
Passed element	P-MOSFET +SD	BJT+ N-MOSFET
Pre-charge/CC overlap	Yes	Yes

MT6573 Charging Application Circuit



**Latest schematic please refer to reference design.

BJT Validation List

- For design in, please notice the parts shipping delivery time.
- The latest validation list, please access the **MTK BBS web**.

Item	Vendor	Part number	Power (Watts)	Package	hFE (min)	hFE (max)	Ic	Contact Window
1	ST	STTB818	**1.2**	SOT23-6L(TSOP6)	100	NC.	3A	Peter lui peter.liu@st.com 02-23762971
2	On semi	NSS35200MR6T1G	**1**	TSOP6	100	400	2A	Tony Kao, tony.kao@onsemi.com 886-2-23761153 886-987-265-997
3	NXP	PBSS5350D	**0.7**	SC-74(SOT-457)	200	NC.	3A	Mag Cheng mag.cheng@nxp.com "+886-987-49186 +886-2-8170-9076 (Direct)
4	Presemi	PT236T30E2	**1.2**	SOT23-6L(TSOP6)	100	NC.	3A	Ken ou ken.ou@prisemi.com

- Must take the power dissipation into consideration.
- The calculation of the power dissipation is introduced in following pages.

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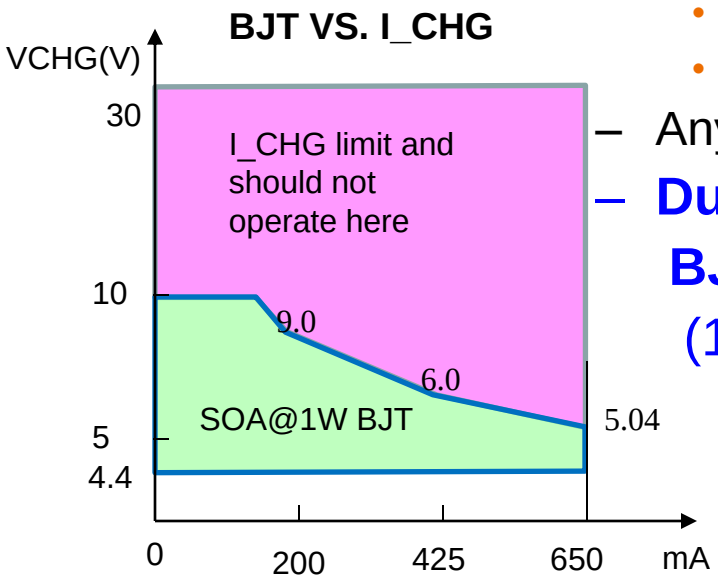
BJT Power Dissipation and Charge Current

- Charger BJT selection
  - Max. charger operate voltage 10V
  - Max. battery charge current (0.72C for Li-ion 900mAHr)
  - Max. power dissipation of external BJT (1W),Duty=8/(8+1)
    - **BJT Pd=(Vchg-3.3V)*Ichg*Duty**
    - (Vchg-3.3)*0.65*0.88 < 1 ➔ Vchg < 5.04V, (I=0.65A)
    - (Vchg-3.3)*0.425*0.88 < 1 ➔ Vchg < 6.0V, (I=0.425A)
    - (Vchg-3.3)*0.20*0.88 < 1 ➔ Vchg < 9.0V (I=0.20A)
  - Any charging time VCHG > VBAT + 0.2 ➔ VCHG > 4.4 V
  - **Due to pre-charge has no charger OVP and then BJT Pd must be large than 0.75W.**
    (10V-2.5V)*100mA=0.75W



Pulse Charging

- Feature
  - Maximum input voltage up to 30V
    (30V is system endurable voltage , not chargeable voltage)
  - Meet 2010 China charger standard
  - CC mode current control
  - Constant current pre-charging
  - Charger OVP and battery OVP
  - Pre-charge/CC safety timer
  - Watchdog timer

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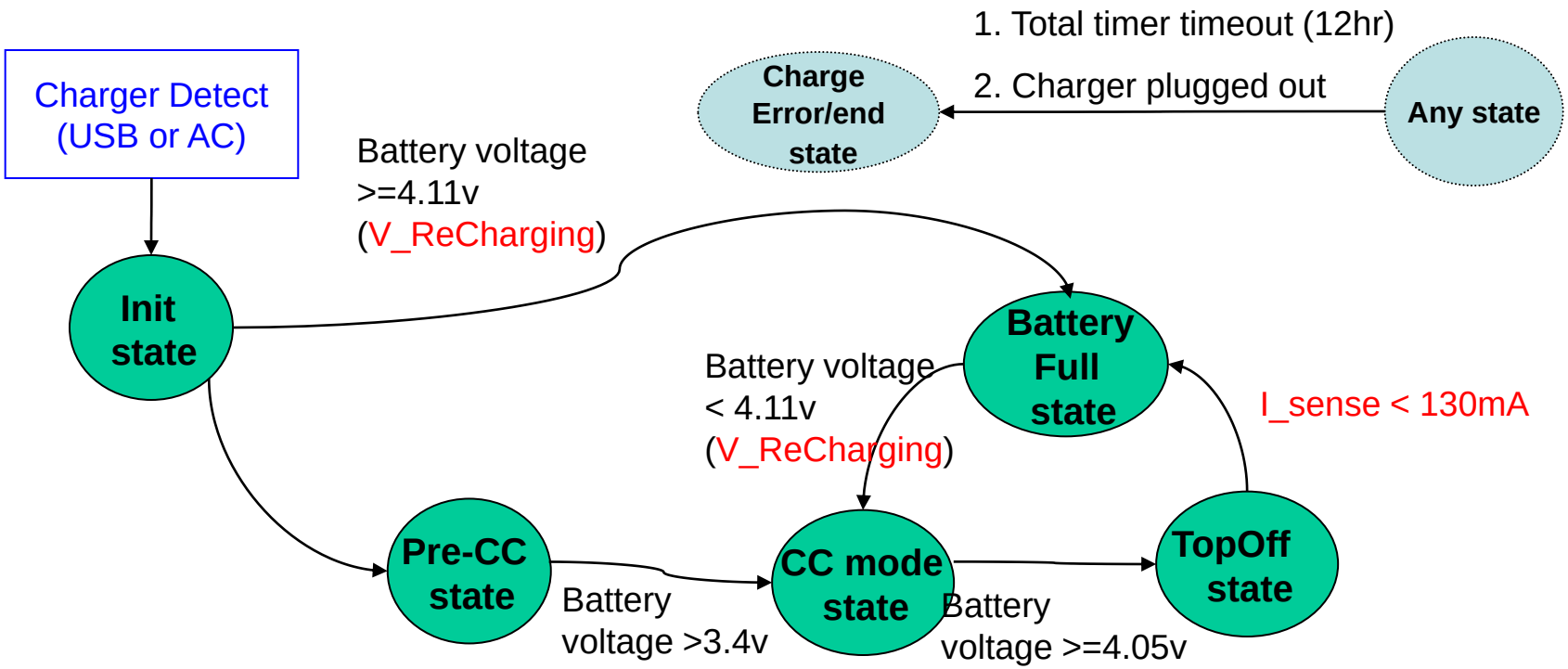
Design Notice – Charge Current Setting

		MT6326	MT6573
Sense Resistor		0.2 Ohm	0.2 Ohm
Pre-Charge(mA)		125	70
CC(mA)	0	62.5	70
	1	90	200
	2	150	400
	3	225	450
	4	300	550
	5	450	650
	6	650	700
	7	800	800

Charging State



Init	CC Mode	CV Mode	Battery Full
1. Init the safety timers 2. Check the VBAT, decide to enter Pre-CC/CC mode or battery full state	1. Do Charger Protection 2. If (1) fail 1) Charger Voltage >6.0V 2) Battery Temperature >50C , stop charging 3. If (2) pass, do charging algorithm: charging 9s and stop charging 1s.	1. Do Charger Protection 2. If (1) fail 1) Charger Voltage >6.0V 2) Battery Temperature >50C , stop charging 3. If (2) pass, do charging algorithm: charging 10s	1. Battery percentage always display 100% Note : When recharging, the battery percentage is still 100%.

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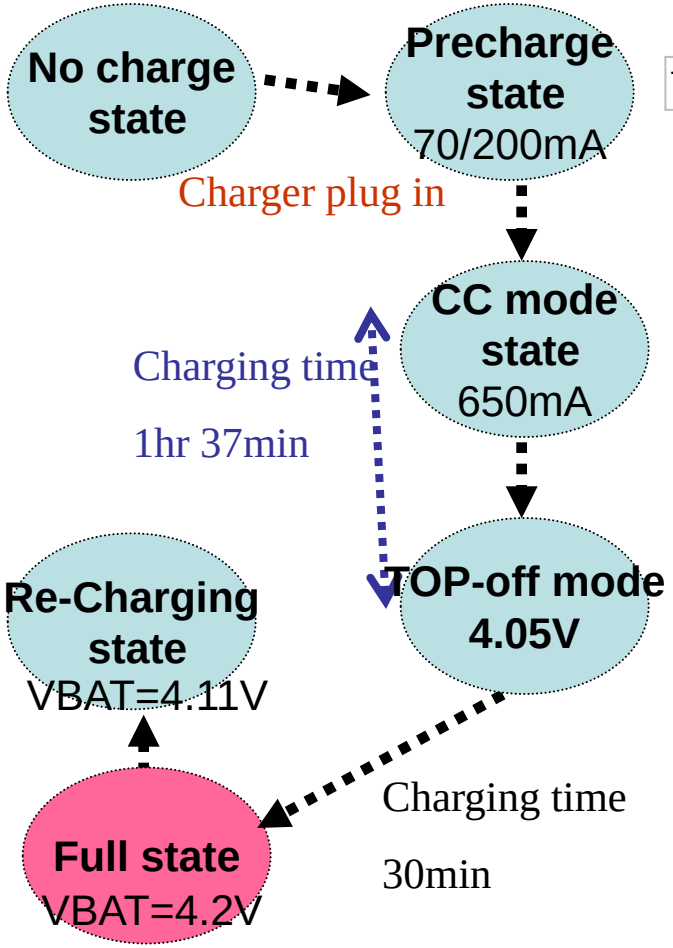
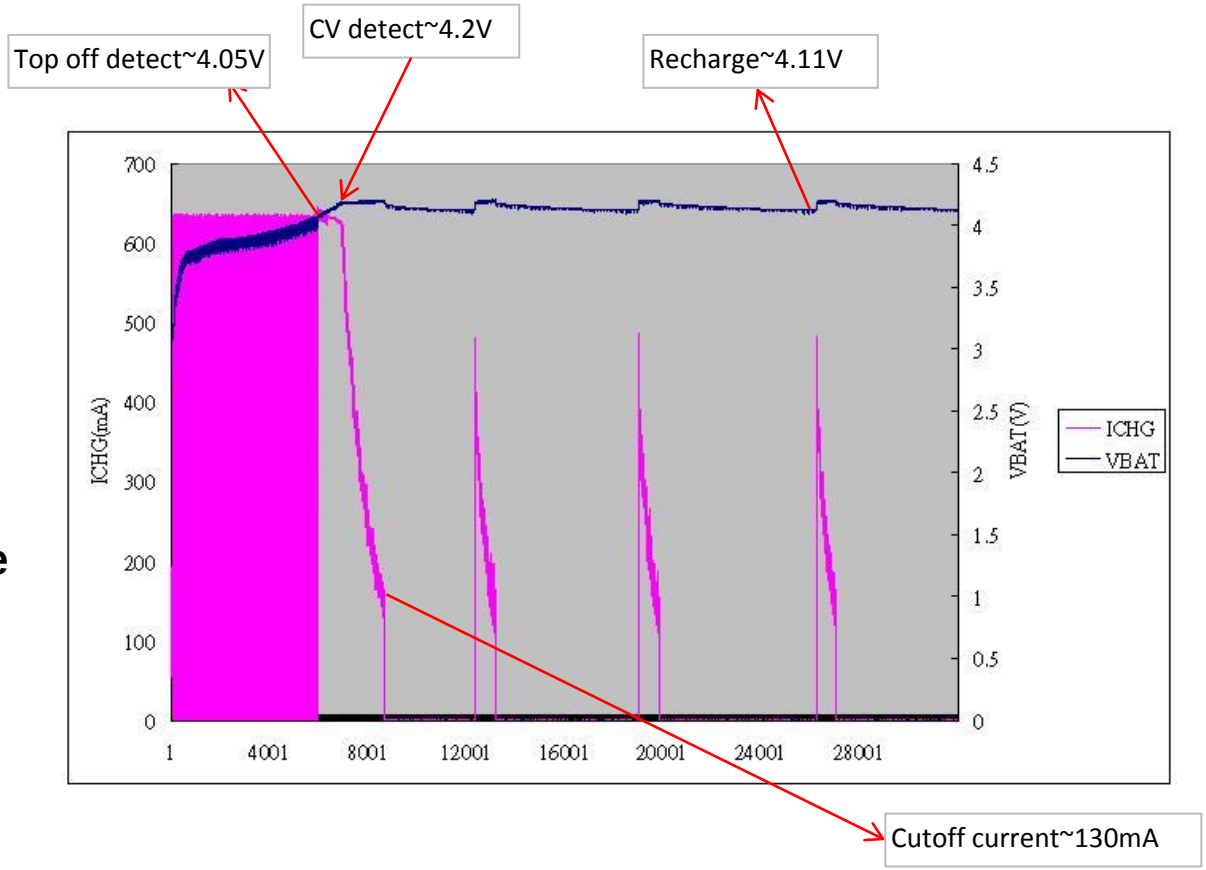
Pulse Charge Charging Curve



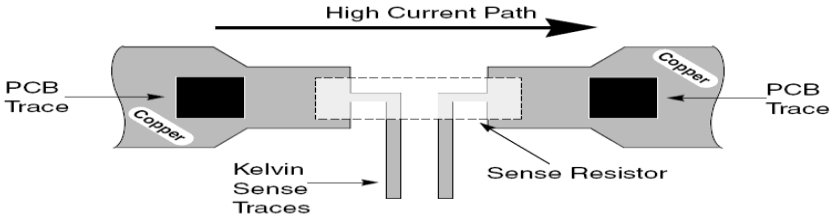


Component Selection Glide

- U200 (BJT):Current passed Component
  - h_{FE} (DC Current Gain) is 100~300 (Typical 200 @-20~80 ^{0}C) at Ic=0.5A
  - For thermal dissipation concern, the U200 power dissipation must be large than 1W.
  - VCE(Collector-Emitter Voltage) ≥30V
  - Ic >0.8A (Depend on application)
- U204 N-MOS
  - Vgs threshold <1.5V @Id=0.1mA
  - VDS>30V (Depend on application)
  - RDS (ON) <10 ohm @ID = 10 mA, VGS = 2.5 V
- C200 (VCHG input cap)
  - If want to support VCHG up to 30V, please change CAP to 1uF/50V.

Charger Layout Notice:

- C216 CHR_LDO decouple cap close to IC.
- R211 (Current sense resistor)close battery connector and trace is 40mil(star connect to connector)
- The exposed pad of the U200(Current passed component) should connect to a large copper ground plane to get good thermal performance.
- ISENSE and BATSNS should be connected as the below figure.
- The trace from Rsense to battery connector should not share with other VBAT traces.
- ISENSE/BATSNS should be routed as differential traces which are away from noisy signals.



Introduction – Battery Charging 1.1 (BC1.1)

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BC1.1 vs. YDT1591-2006

	USB-IF BC1.1	YDT1591-2006
Define Items	Dedicate Charger Charging Host Portable Charging Device Accessory Charger Adapter	Dedicate Charger
Output Voltage	DC: 4.75~5.25V	DC: 4.75~5.25V
Output Current	500~1500mA	300~1800mA
DP/DM	DP / DM short	DP / DM short
Interface	USB A/Micro USB AB	USB A
Others	Detail define detection mechanism.	Only define DP/DM as dedicate charger case.

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Apply BC1.1 to Fast Charging Time

- Define three types of charging ports in BC1.1
  - Standard Downstream Port

    I_{CHG_MAX}=500mA and support USB2.0 communication.
  - Charging Downstream Port

    I_{CHG_MAX}=1.5A and support USB2.0 *Low/Full-speed* communication.

    I_{CHG_MAX}=900mA and support USB2.0 *High-speed* communication.

    I_{CHG_MAX}=560mA and support USB2.0 communication during *chirp*.
  - Dedicated Charging Port

    I_{CHG_MAX}=1.8A but can't support USB2.0 communication.

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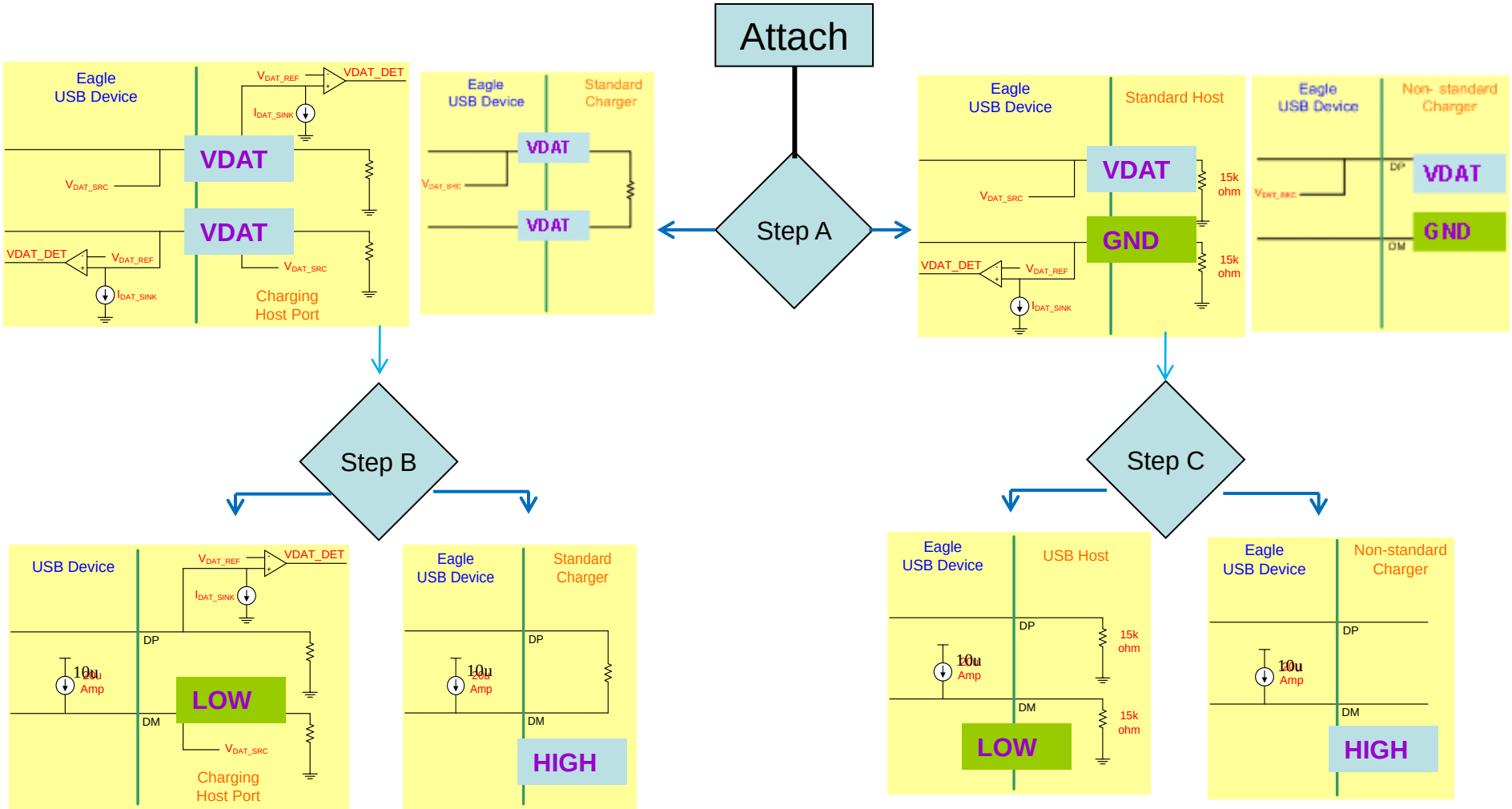
Mixed Unify Flow



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Enable Pin for BC1.1

- Ball naming “BC11_EN”
  - If let this ball floating (internally pull-up)

    BC1.1 “Dead Battery Provision” function will be **enabled**.

  - Pull this ball to GND by a resistor (suggest)

    BC1.1 “Dead Battery Provision” function will be **disabled**.
    Charging port detection still work normally.

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MT6573 Application Notice-- Gas gauge

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Gas gauge Introduction

- What is Gas gauge?
  - For precise battery capacity estimate

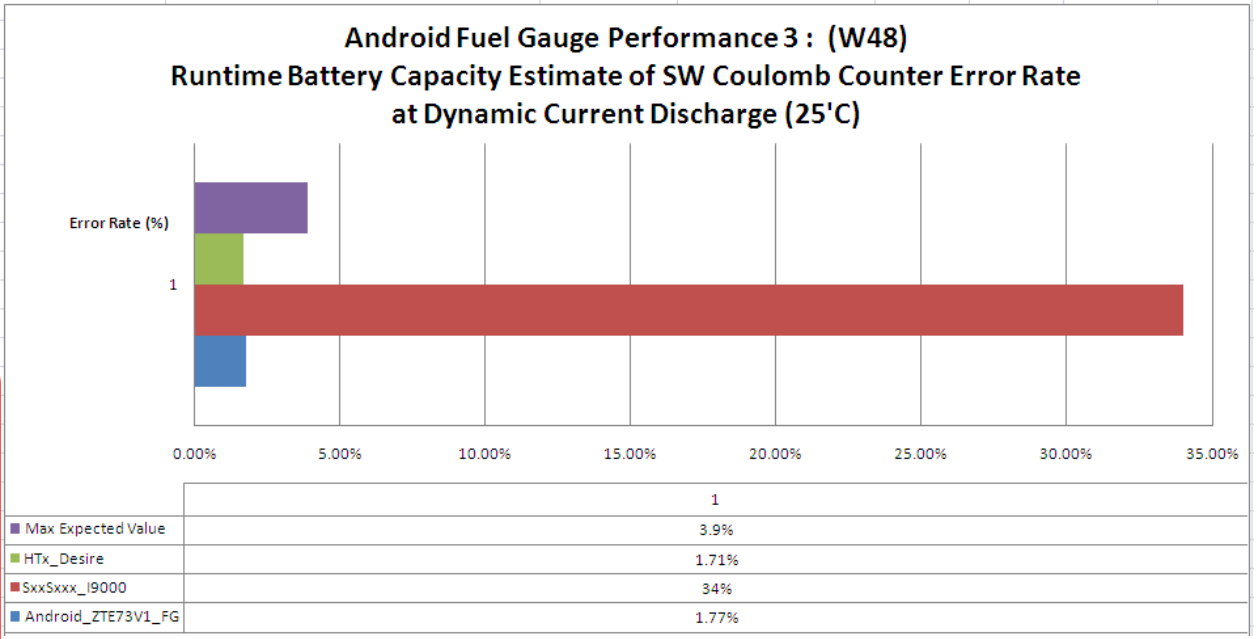
NO

YES

Gas gauge benchmark

- The total discharge error rate of MT6573 is closed to HTx Desire

	Fuel Gauge Style	Cost (US)
HTx Desire	Battery-side FG	~ 0.5
SxxSxxx I9000	NA	NA
Mxtx Milestone	NA	NA
MTK MT6573	Phone-side FG	< 0.01



KPI	Target	NT (25'C)	Max Error
Total Error Rate D%=100%~0%	MT6573	Done	1.96%
	SxxSxxx I9000	Done	34.00%
	Mxtx Milestone	Done	55.00%
	HTx Desire	Done	1.71%

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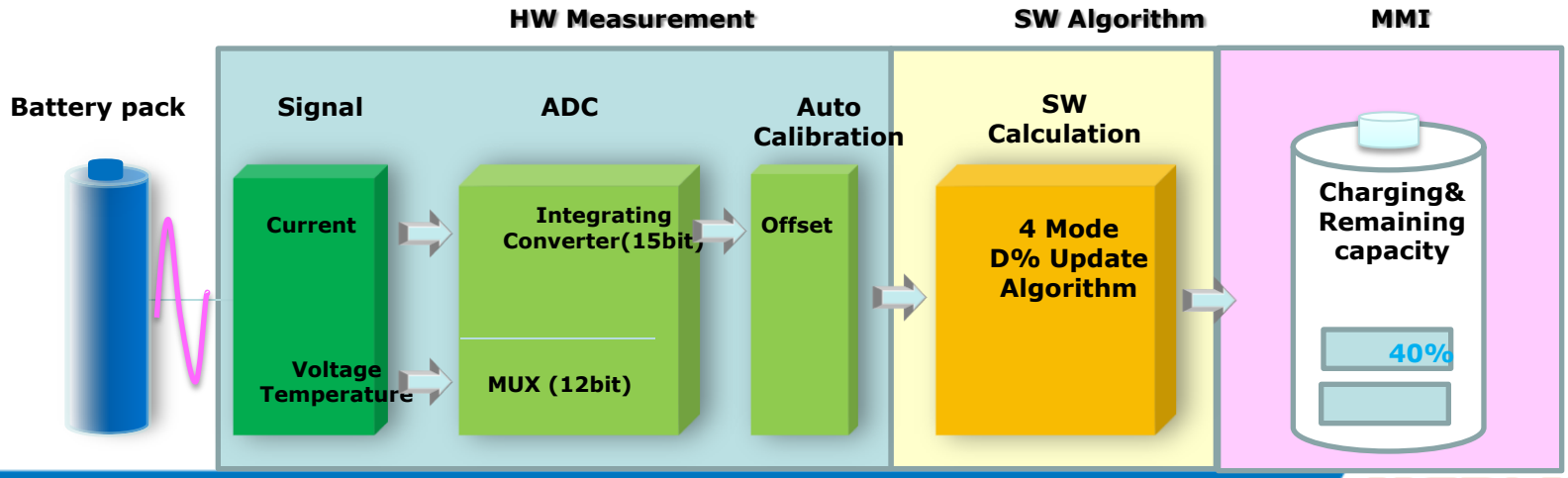
MT6573 Fuel Gauge System

- System-side Li-Ion battery fuel gauge SOC
  - Precise Battery Fuel Gauging
  - Battery Low/High Interrupt Warning
  - Battery current measurement
  - Temperature Reporting



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Fuel Gauge Customer Support

Case of Customer Support		Customers	Pros	Cons	Effort
No Use Fuel Gauge		1. For Cost down (remove Rfg) 2. Do not case the battery percentage	Remove Rfg (< 0.01US)	Battery percentage error rate = 30%~50%	None
Use MTK Fuel Gauge	**Use default ZCV Table**	1. Need precise battery percentage 2. Can not get the battery ZCV table	1. Battery percentage error rate < 20% 2. Cost is cheaper than the Fuel Gauge IC (0.6~0.9US)	Need Use default ZCV Table	Need Rfg (< 0.01US)
	MTK SA measure ZCV Table for each customer	**1.Need precise battery percentage 2. Can get the battery ZCV table**	**1. Battery percentage error rate <10% 2. Cost is cheaper than the Fuel Gauge IC (0.6~0.9US)**	**Need 20 days for creating the ZCV table**	**1. Need Rfg (< 0.01US) 2. Need provide the battery packet and SPEC to MTK SA for creating the ZCV table. (same as the flow of Gas Gauge IC vender)**

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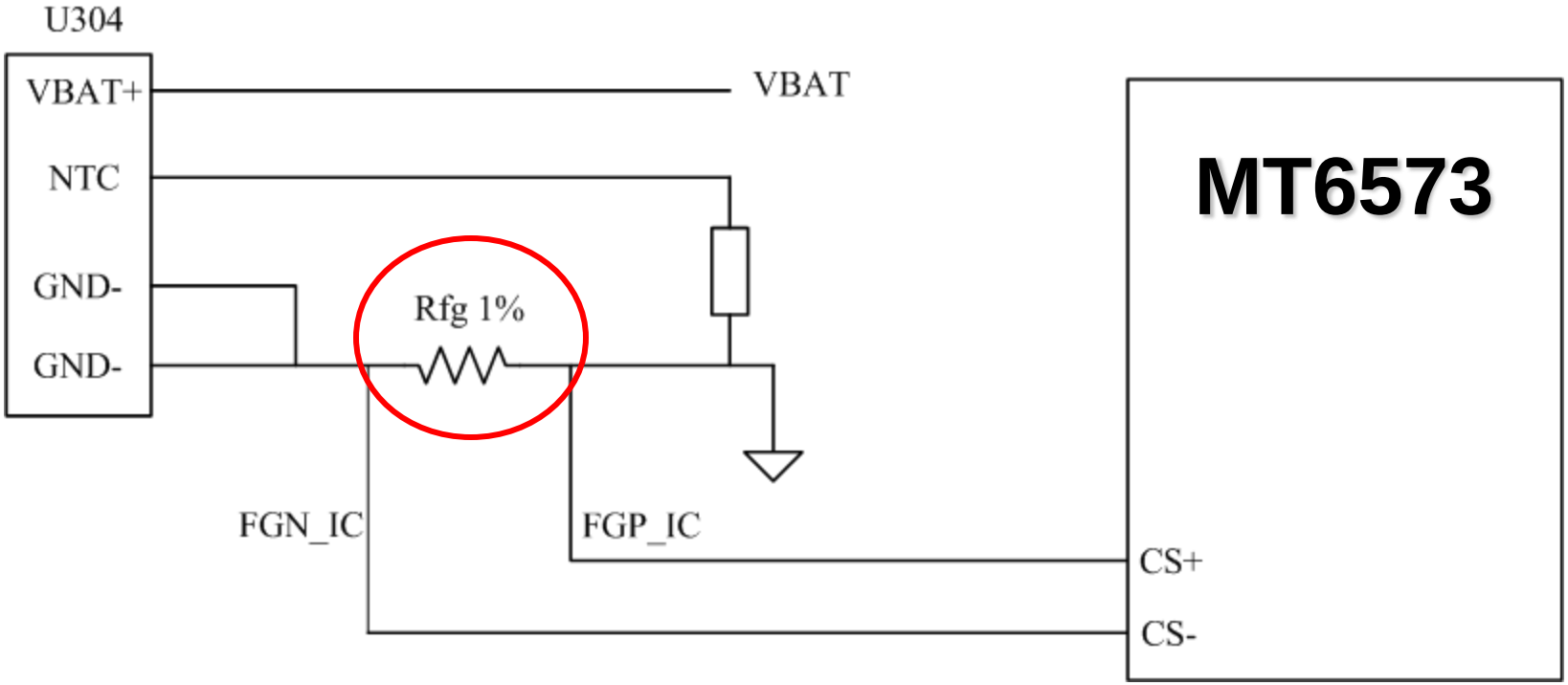
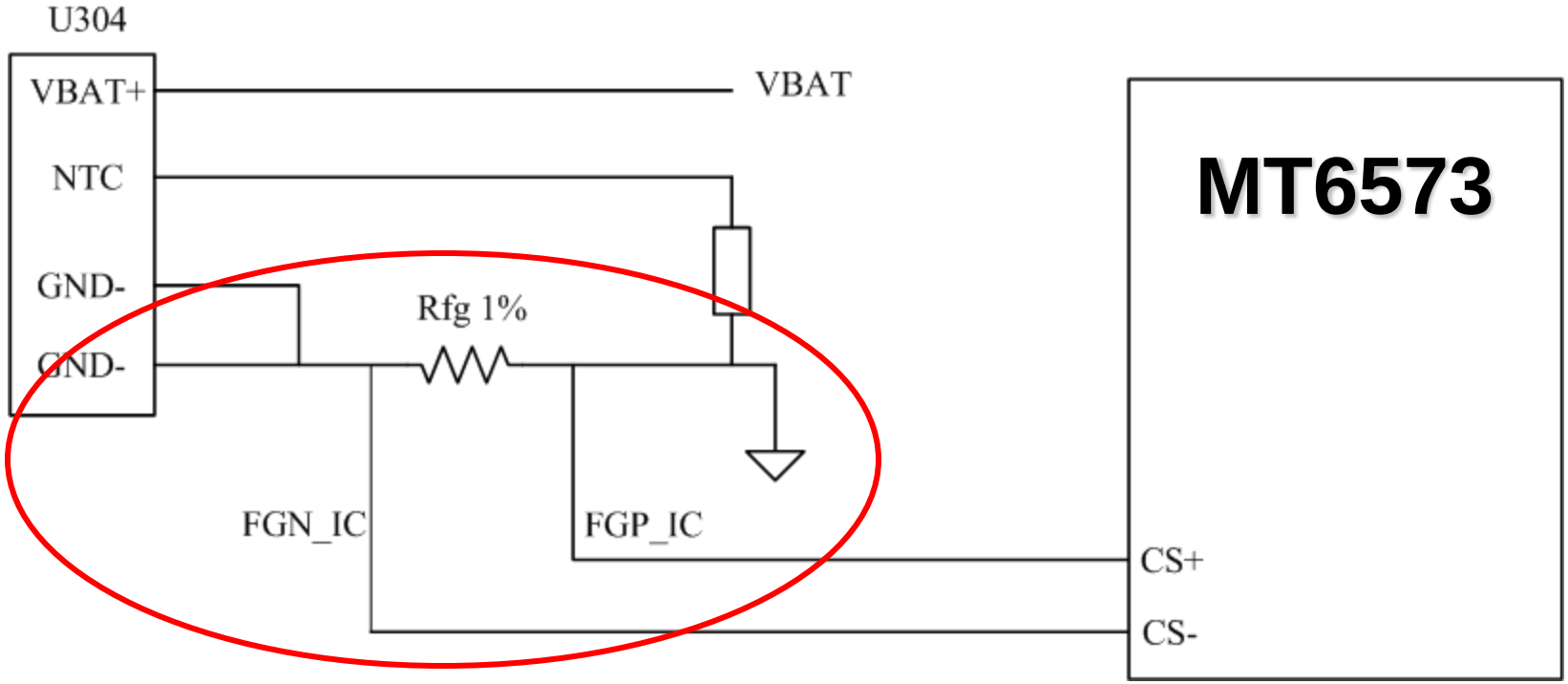
Gas gauge Application Circuit

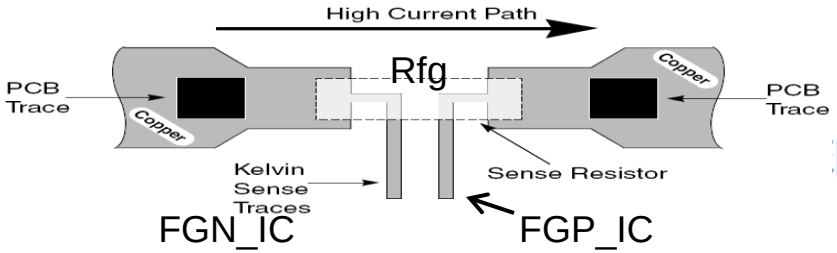


- Sense resistor Rfg need **20m~50m Ω 1% 1206 package** in series with the battery negative terminal to ground
- Please **must have NTC temp sense resistance for gas gauge**
- If you want to disable Gauge function, please short FGP and FGN to system GND directly.

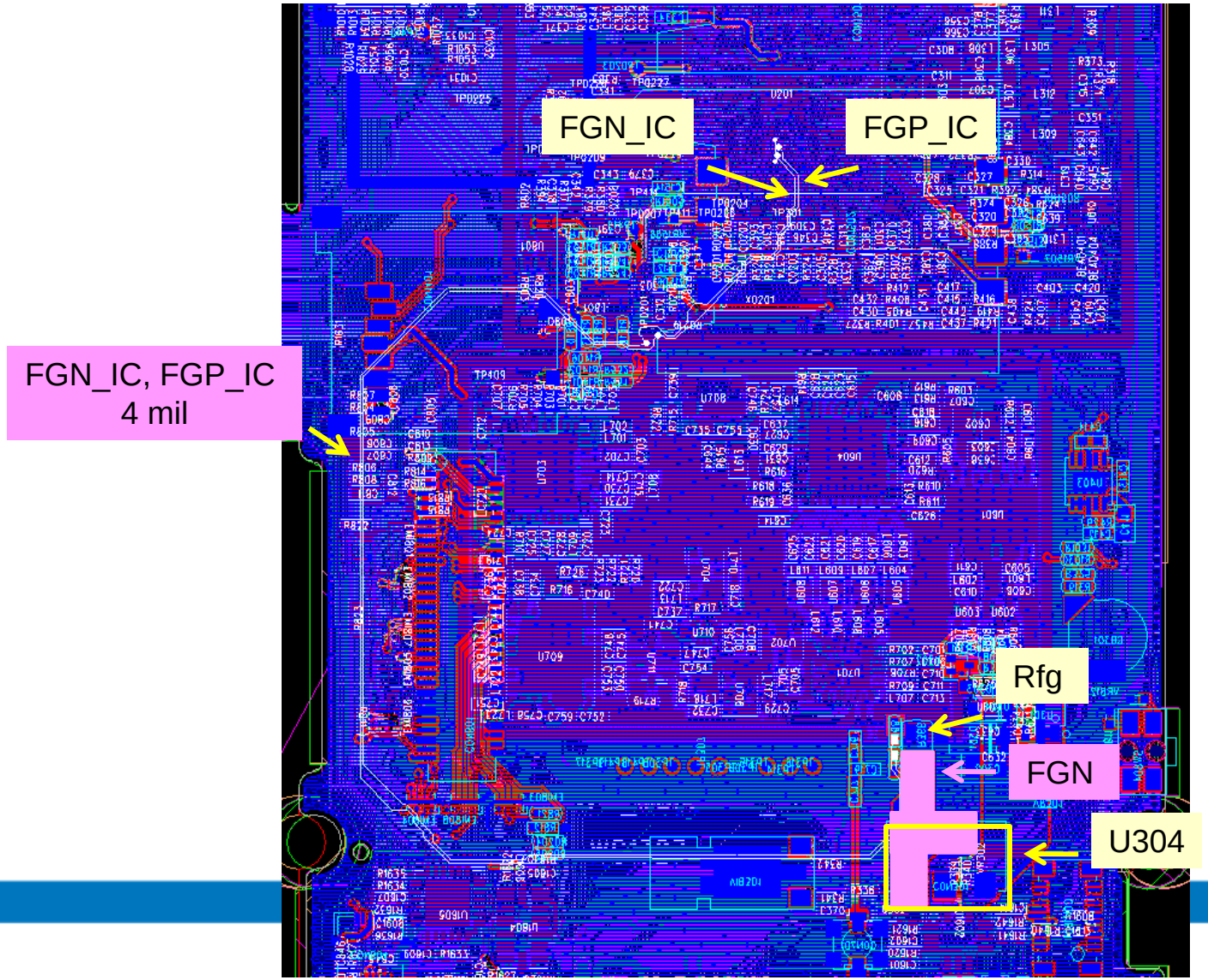
Gas gauge PCB Layout design note



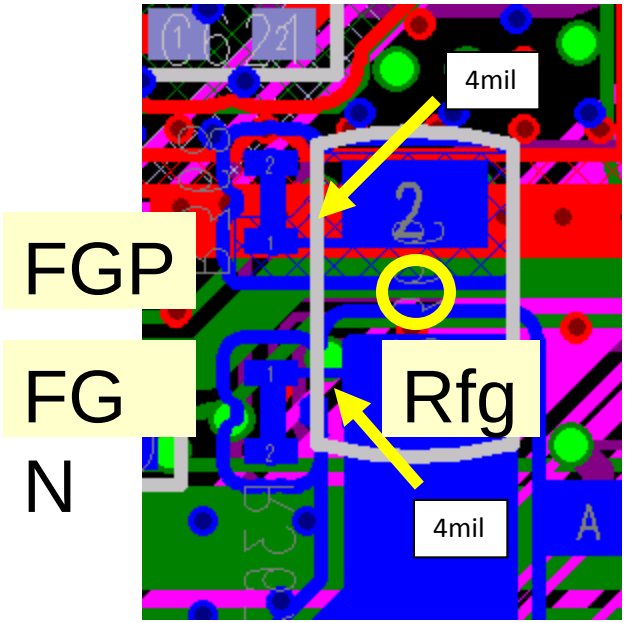
- Rfg PCB layout closed to U304
- FGN_IC/FGP_IC use 4mil differential line from MT6573 CS-/CS+ connect to Rfg



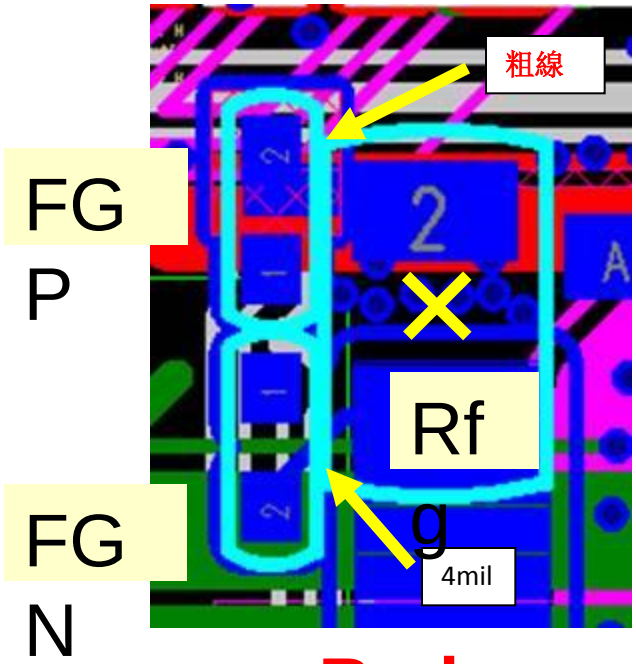
Reference design - Layout FGN_IC/FGP_IC



Reference design - Layout FGN_IC/FGP_IC



Good



Bad

Confidential B

MT6573 Design Note- Speech

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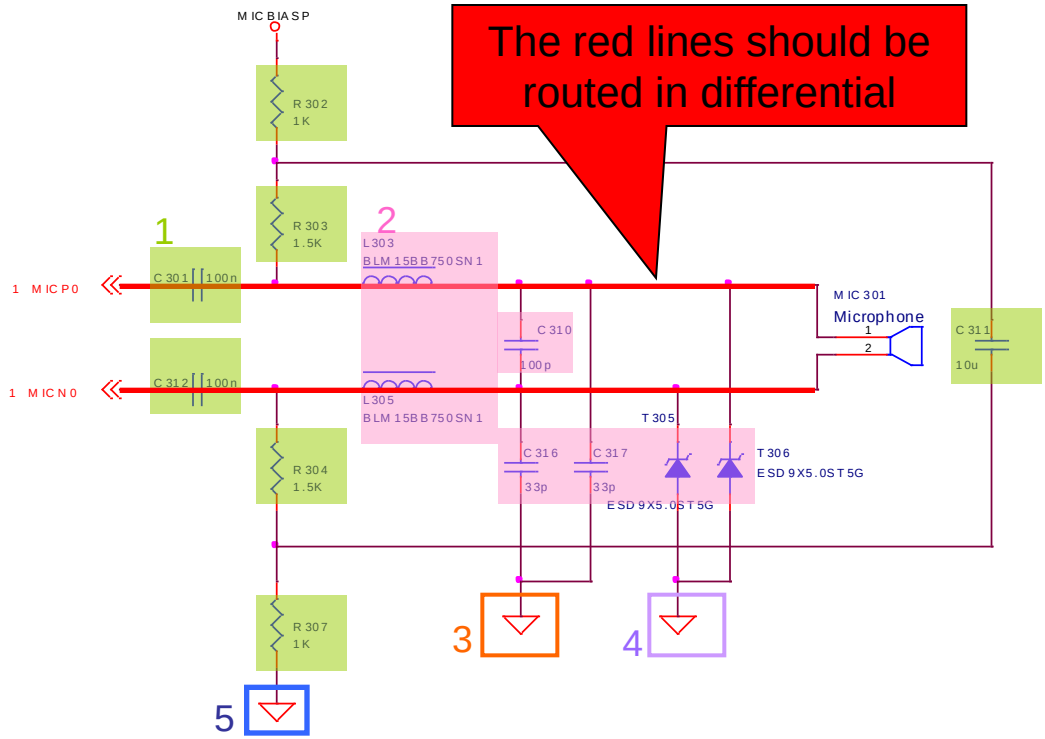
Agenda

- Microphone circuit application note
  - Analog microphone / Digital microphone
- 2-mic application circuit
  - Analog microphone / Digital microphone
- SW setting of digital/ analog microphone
- Critical component placement/ layout rule
- 2-in-1 speaker application note
- Gain range and setting in NVRAM database

ECM analog microphone application note

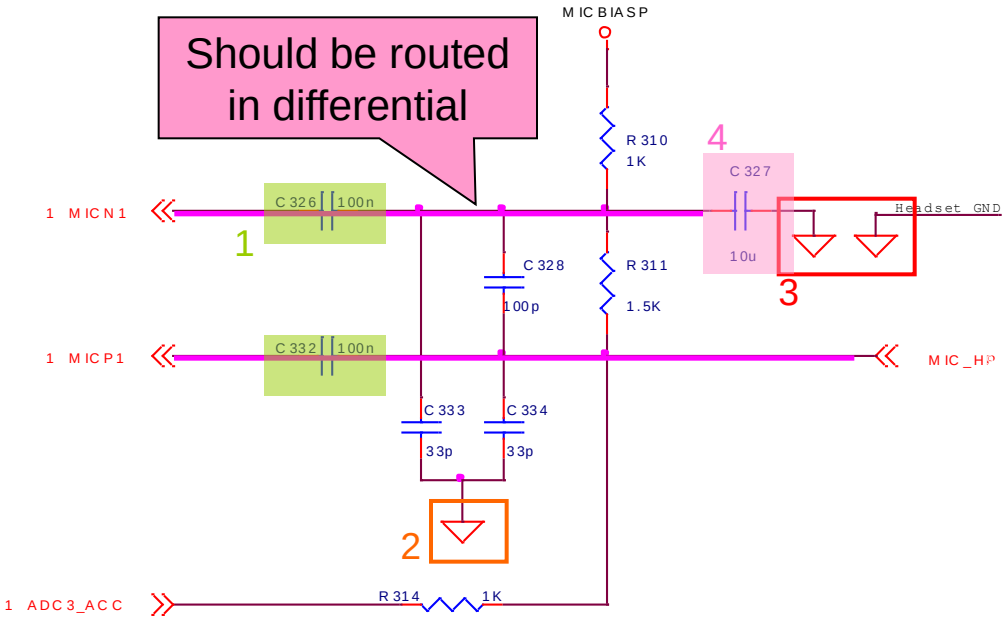
- Layout consideration-Normal mode



1. R302, R303, R304, R307, C311, C301 and C312 should be put **close to the BB chip**
   - R302, R303, R304, R307, C311 should be put as close as possible
2. L303, L305, C310, C316, C317, T305 and T306 should be **close to the microphone**
3. GND of **C316 and C317** should be connected **together** and then to the GND
4. GND of **T305 and T306** should be connected **together** and then to the GND
5. GND of **R307**should connect to the **main GND by a single via**

ECM analog microphone application note

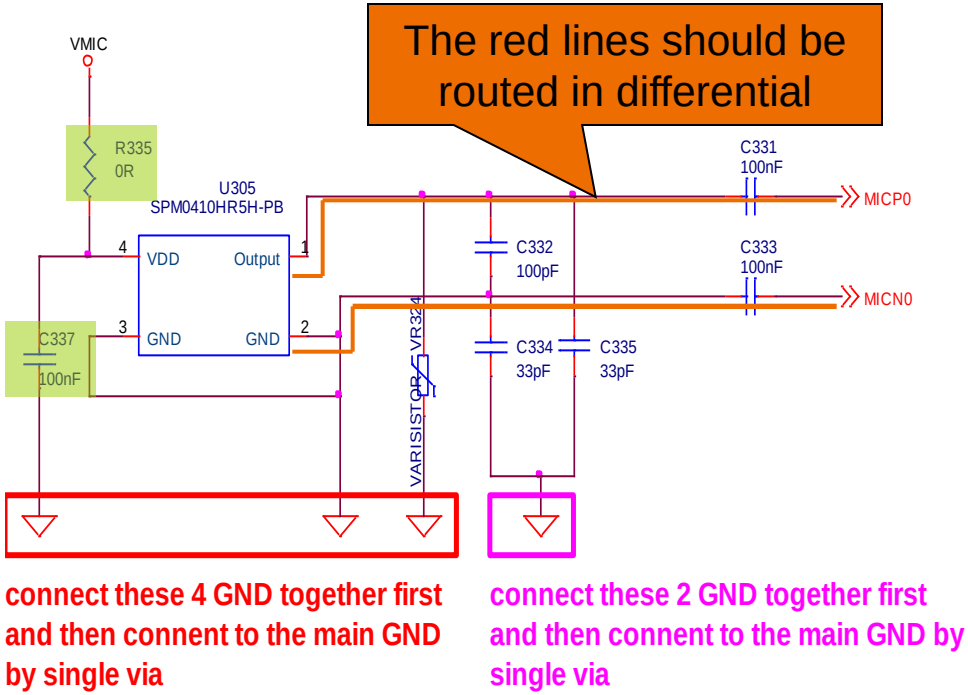
- Layout consideration-Headset mode



1. **C326, C332, R311, R310** should be put **close to BB**
2. The **GND of C333 and C334** should **connect together and then connect to the GND**
3. The **GND of C327 and headset** should **connect together and then to the main GND by single via**
4. **C327** should be put **close to microphone**

MEMS analog microphone application note

- Layout consideration-Normal mode

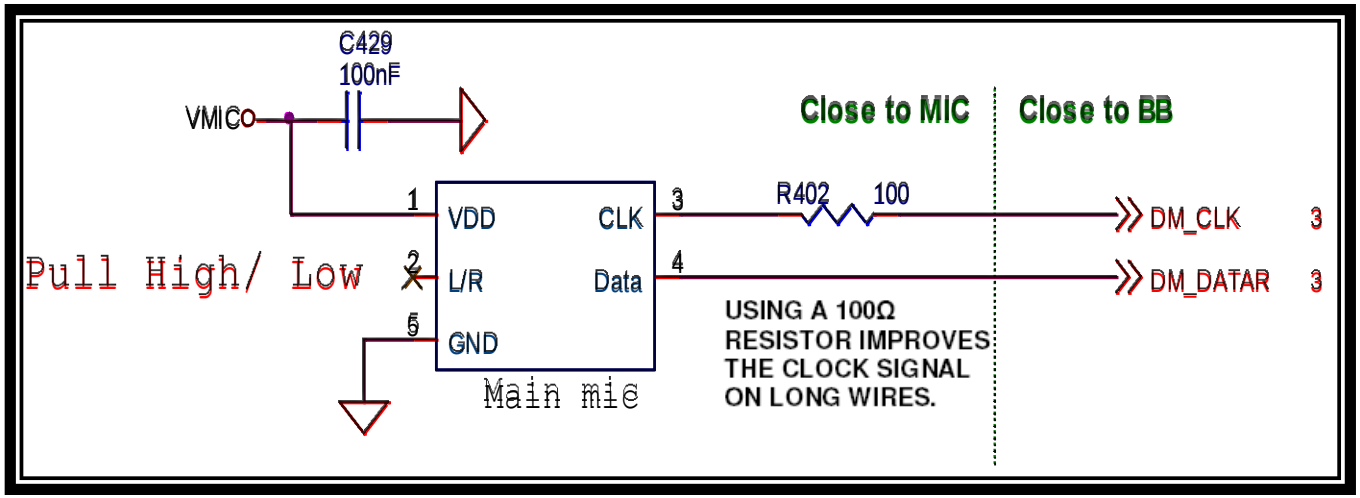


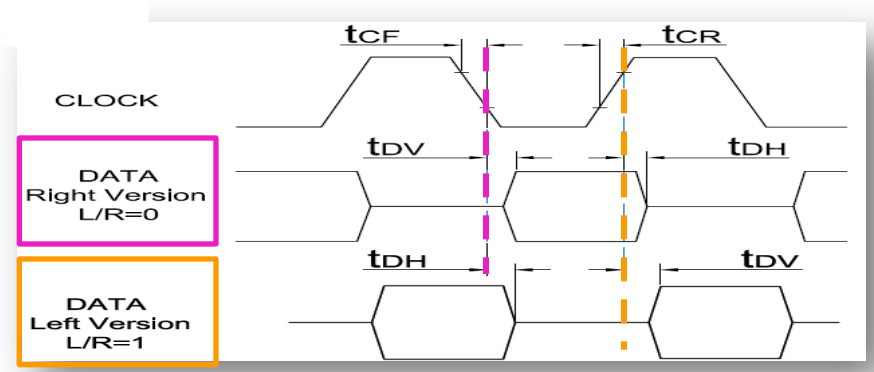
connect these 4 GND together first and then connent to the main GND by single via

connect these 2 GND together first and then connent to the main GND by single via

1. R335, C337 construct a low-pass filter which is used to filter out the noise on the VMIC if necessary
2. R335, C337, VR324, C332, C334 and C335 should be **close to the microphone**
3. GND of **C337 / VR324 and MEMS mic** should be connected **together** and then to the main GND
4. GND of **C335 and C334** should be connected **together** and then to the main GND

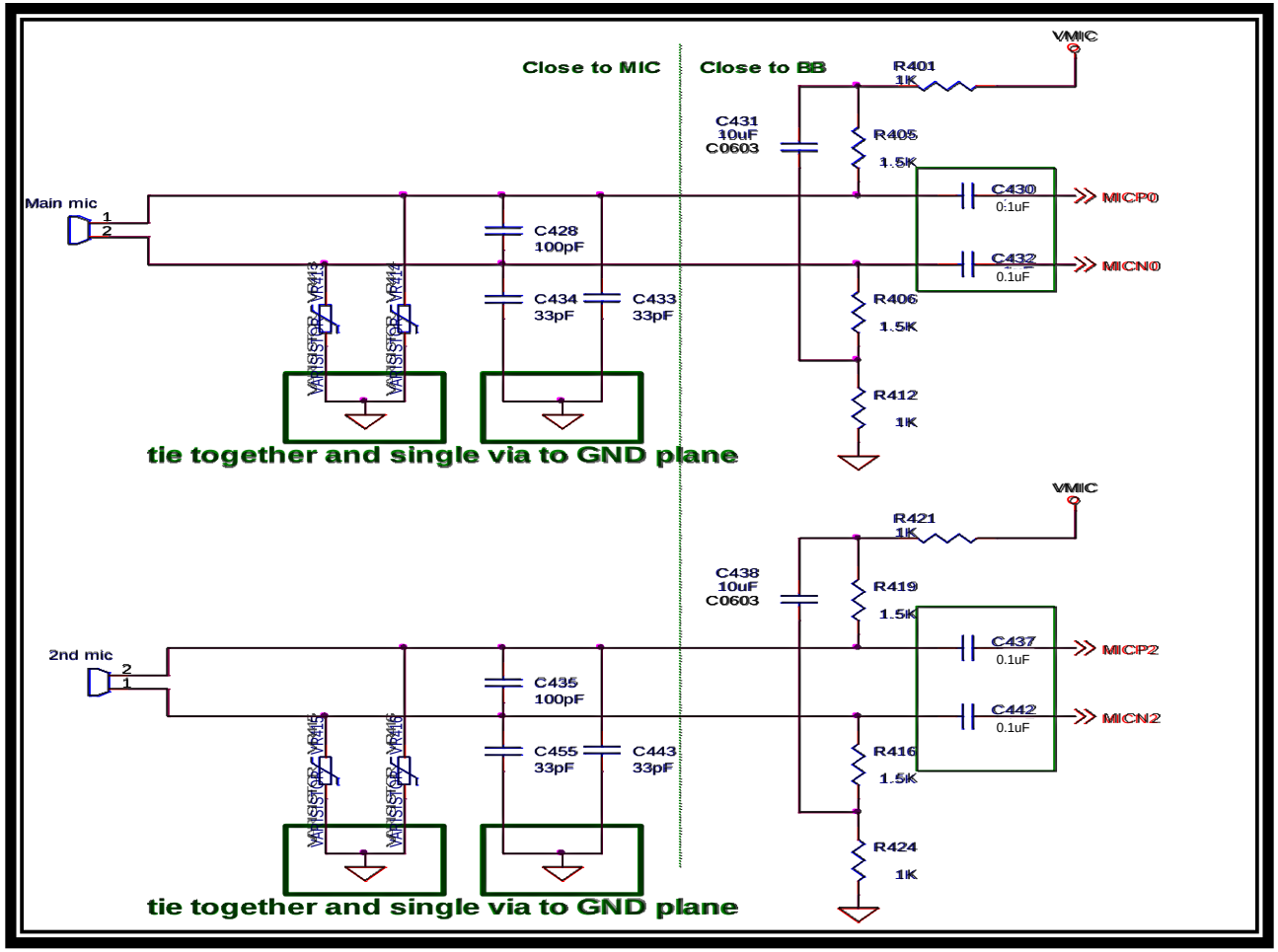
Digital microphone application note



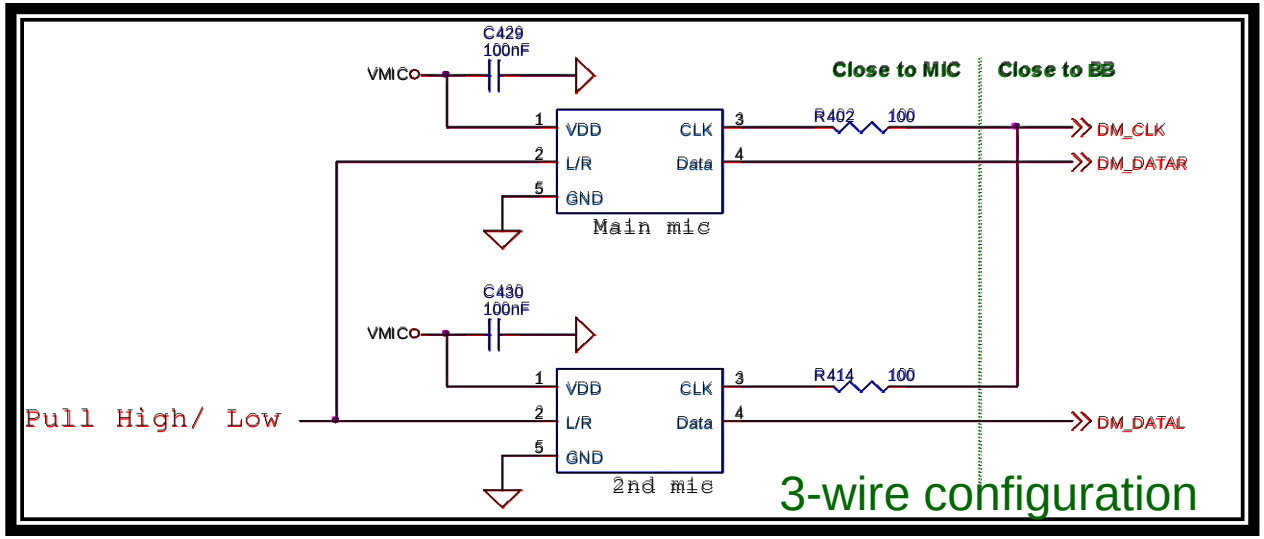


Abbreviation	Description
t_{CR}	Clock rise time
t_{CF}	Clock fall time
t_{DH}	Time from CLOCK Transition to DATA Become High Impedance
t_{DV}	Time from CLOCK Transition to DATA Become Valid

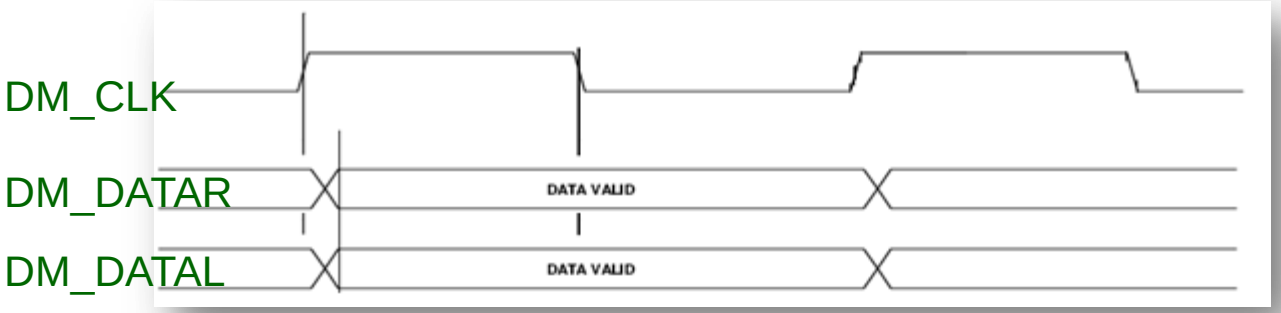
2-mic connectivity- Analog mic



2-mic connectivity- Digital mic



If L/R= High



SW setting of digital/ analog microphone

- How to enable digital/ analog microphone
  - alps\mediatek\config**{project folder}**\ ProjectConfig.mk
    - Digital Mic compile option
    - DIGITAL_MIC_SUPPORT = TRUE(digital) or FALSE(analog)
- How to enable 2-mic support
  - alps\mediatek\config**{project folder}**\ ProjectConfig.mk
    - Dual-Mic compile option
    - DUAL_MIC_SUPPORT = TRUE(dual-mic) or FALSE(single-mic)

Analog/ Digital microphone pin mux

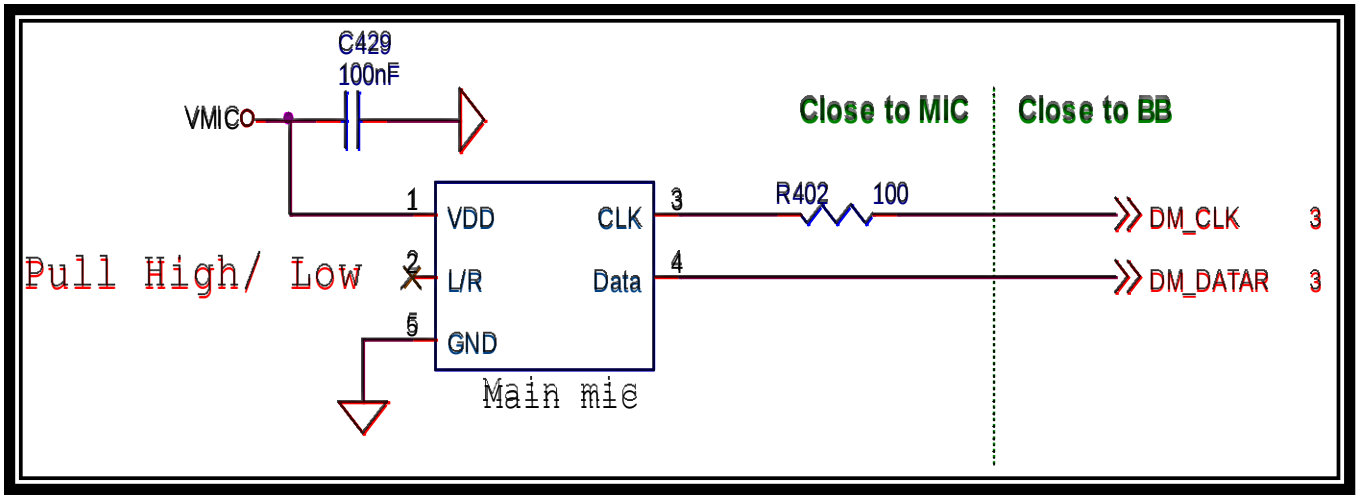
	Pin mux	
	Analog mic	Digital mic
Main mic	AU_VIN0_P	DM_CLK
	AU_VIN0_N	DM_DATAR
Headset mic	AU_VIN1_P	
	AU_VIN1_N	
2nd mic	AU_VIN2_P	
	AU_VIN2_N	DM_DATAL

Note
1. Headset mic only support analog mic
2. Main/ 2nd mic should be set to support the same mic type

		DUAL_MIC_SUPPORT	
		TRUE	FALSE
DIGITAL_MIC_SUPPORT	TRUE	Dual digital mic	Single digital mic
	FALSE	Dual analog mic	Single analog mic

PDM IF (digital microphone IF)spec

Symbol		min	typ	max	unit
DCLK	DMIC Clock Frequency		1.625	3.25	MHz
DTY	DMIC Clock Duty Cycle	40		60	%
CRT	DMIC Clock rise time (CL=80pF)		10		ns
CFT	DMIC Clock fall time (CL=80pF)		10		ns
IC	Input Capacitance		45		pF

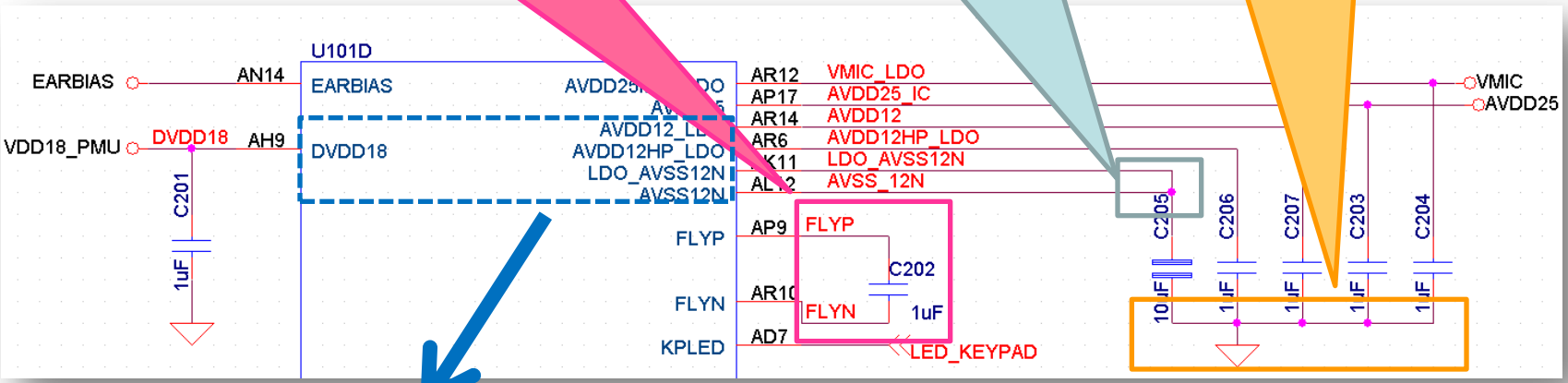


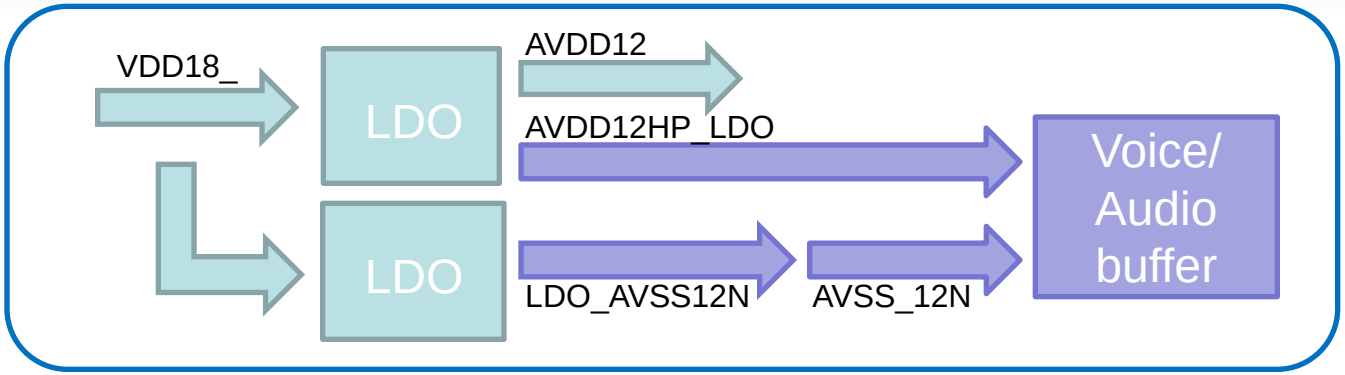
Critical component placement/ layout rule

C202 should be close to pin AP9 and AR10

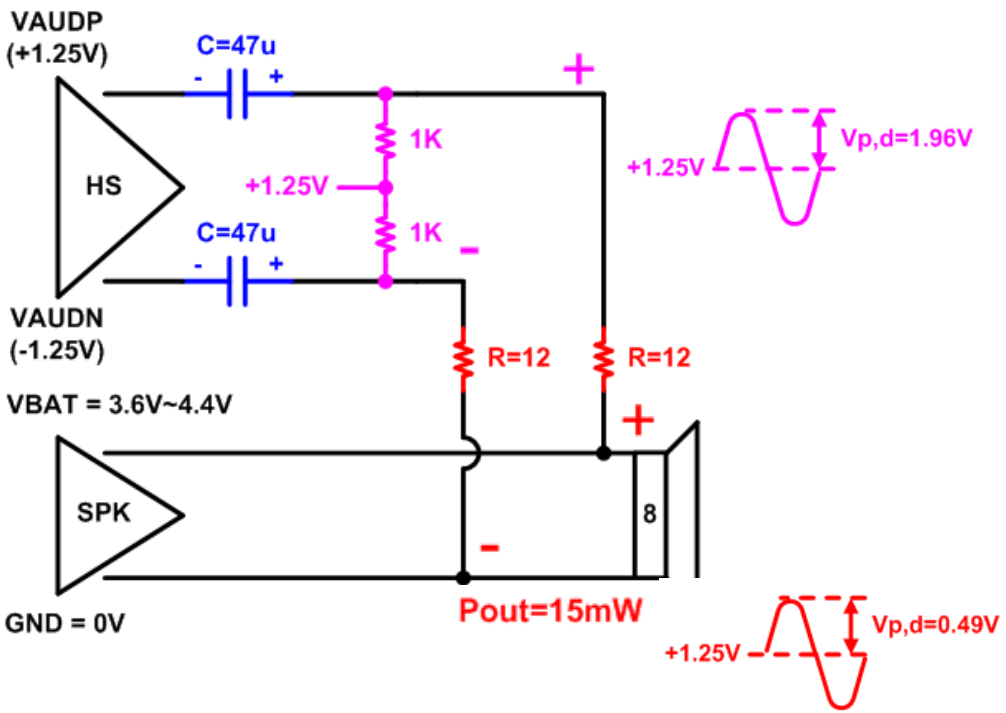
Star connection to the cap C205, 3mil

Connect the cap's GND to the **main GND**





2-in-1 application circuit



- 2 resistor 12Ω are used to construct the equivalent 32Ω load at HS
- 2 47uF capacitor are needed to do DC block and form high-pass filter with resistor 12Ω which impact the low-frequency response
  - To avoid leakage current form SPK amp output to VAUDP/VAUDN)
- Need bias resistor 1KΩ and bias voltage +1.25V to build DC
  - To avoid the leakage current, due to the reference voltage of SPK amp is GND but the HS output is DC-coupled signal)

For 2-in-1 application, not only HW should be modified but also SW,

- alps\mediatek\config**{project folder}**\ ProjectConfig.mk
- 2-in-1 speaker compile option
- 2IN1_SPEAKER_SUPPORT = TRUE (2 in 1 speaker) or FALSE (not 2 in 1 speaker)

Gain range and setting in NVRAM database

DL PGA (Voice/ Audio buffer)

Gain range	NVRAM setting	Gain range	NVRAM setting	Gain range	NVRAM setting
8dB	160	-6dB	104	-20dB	48
7dB	156	-7dB	100	-21dB	44
6dB	152	-8dB	96	-22dB	40
5dB	148	-9dB	92	-23dB	36
4dB	144	-10dB	88	-24dB	32
3dB	140	-11dB	84	-25dB	28
2dB	136	-12dB	80	-26dB	24
1dB	132	-13dB	76	-27dB	20
0dB	128	-14dB	72	-28dB	16
-1dB	124	-15dB	68	-29dB	12
-2dB	120	-16dB	64	-30dB	8
-3dB	116	-17dB	60	-31dB	4
-4dB	112	-18dB	56	-32dB	0
-5dB	108	-19dB	52		

UL PGA

Gain range	NVRAM setting	Gain range	NVRAM setting	Gain range	NVRAM setting
49dB	252	27dB	164	5dB	76
48dB	248	26dB	160	4dB	72
47dB	244	25dB	156	3dB	68
46dB	240	24dB	152	2dB	64
45dB	236	23dB	148	1dB	60
44dB	232	22dB	144	0dB	56
43dB	228	21dB	140	-1dB	52
42dB	224	20dB	136	-2dB	48
41dB	220	19dB	132	-3dB	44
40dB	216	18dB	128	-4dB	40
39dB	212	17dB	124	-5dB	36
38dB	208	16dB	120	-6dB	32
37dB	204	15dB	116	-7dB	28
36dB	200	14dB	112	-8dB	24
35dB	196	13dB	108	-9dB	20
34dB	192	12dB	104	-10dB	16
33dB	188	11dB	100	-11dB	12
32dB	184	10dB	96	-12dB	8
31dB	180	9dB	92	-13dB	4
30dB	176	8dB	88	-14dB	0
29dB	172	7dB	84		
28dB	168	6dB	80		

Component selection guide for WB-AMR application

	WB (100Hz~8KHz)	NB (100Hz~4KHz)
SLR	8+/-3dB	8+/-3dB
SFR	Within the mask (refer to the nest slide)	Within the mask (refer to the nest slide)
RLR	2+/-3dB	2+/-3dB
RFR	Within the mask (refer to the nest slide)	Within the mask (refer to the nest slide)
TCLw	>46dB	>46dB
IDL_SND	-64dBm0(A)	-64dBm0(P)
IDL_RCV	Nominal: -57dBPa(A) Maximum: -54dBPa(A)	Nominal: -57dBPa(A) Maximum: -54dBPa(A)
DIS_SND/ DIS_RCV	Above the mask	Above the mask

Component selection guide for WB-AMR application

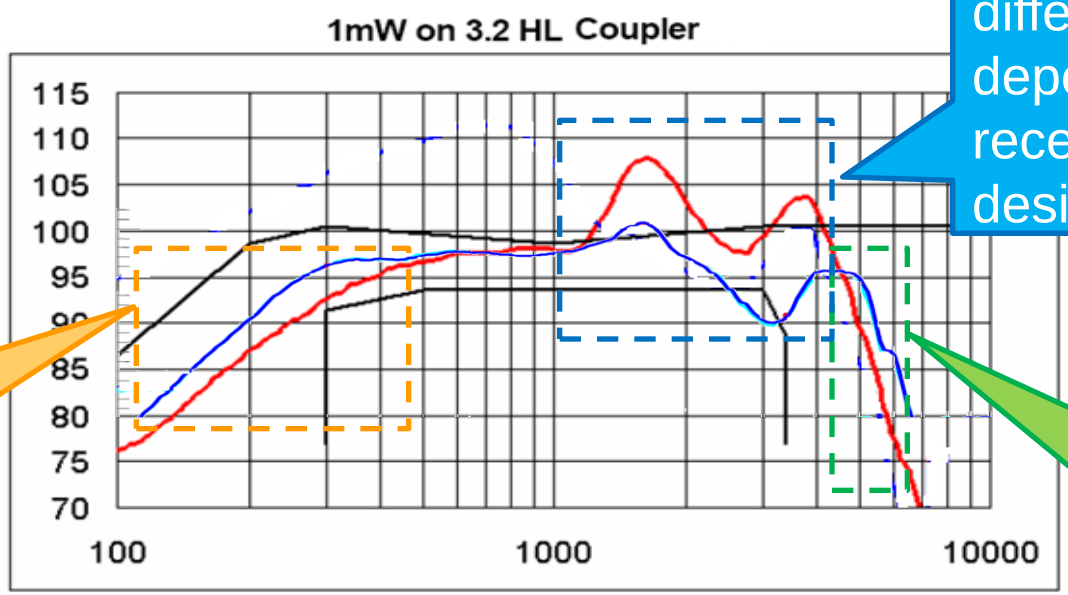
W

NB

Note only high frequency content is extended but also the low frequency part

Component selection guide for WB-AMR application

- WB receiver is needed for the WB-AMR application
  - It has better frequency response at low/high frequency parts
  - Vendor who has WB receiver
    - NXP: RA 12 x 8 x 2 (dimension- 8x12x2.0)
    - Pioneer: DV12-004 (dimension- 8x12x2.1)



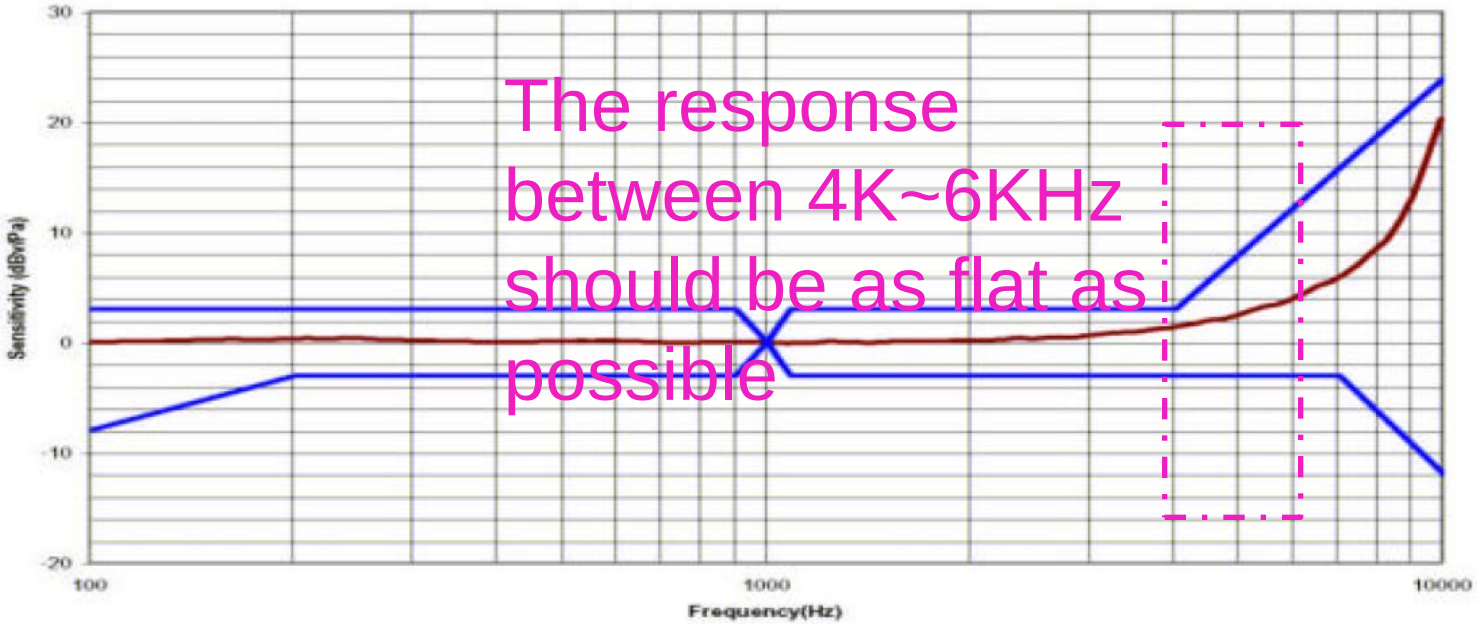
How large the difference is depends on the receiver opening design

Low frequency response is better

High frequency response is better

Component selection guide for WB-AMR application

- WB microphone is needed for the WB-AMR application
  - The frequency response below 6KHz should be as **flat** as possible



MEDIATEK

Design Notice – Audio

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Introduction of ACCDET and DC couple Audio

- ACCDET
  - 3 level Interrupt with two comparator(EINT only 2 level)
  - Not general purpose IO and no internal pull up , need external power source to generate DC voltage for measurement

- MTK DC couple Audio
  - +/- 1.25 V power domain so , audio buffer will broken when pull up voltage high than 1.25+0.3
  - GND reference , and 0V output when audio Buffer turn on

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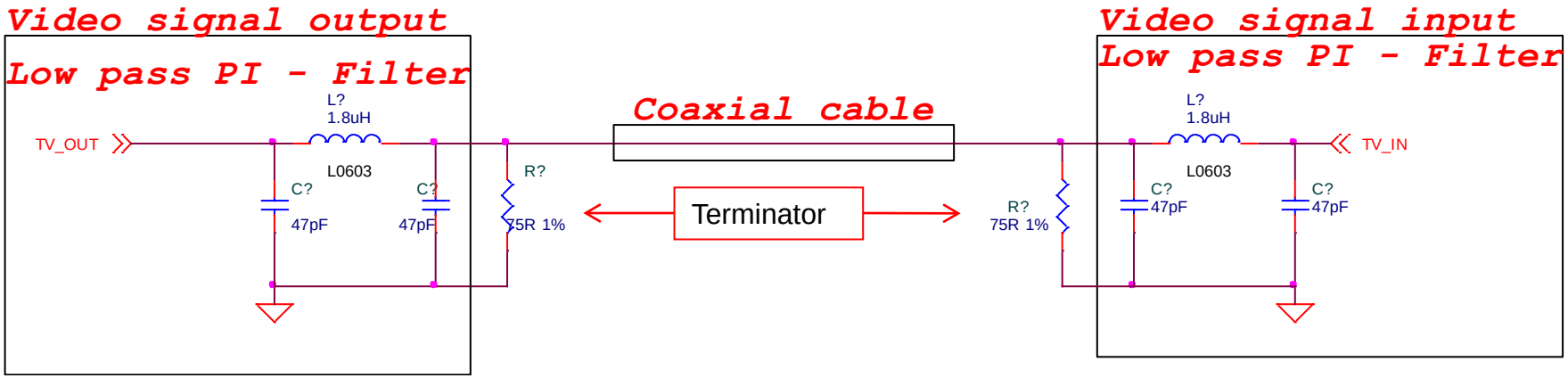
Introduction of earphone and TV cable

- Earphone cable
  - The resistance is 16/32 ohm at earphone receiver (L/R channel)
  - The equivalent resistance around 6~13K of earphone microphone

- TV cable
  - High impedance at TV Line_In or floating at cable only (L/R channel)
  - 37.5 ohm loading when cable connect to TV
  - 75 ohm loading at PCBA internal



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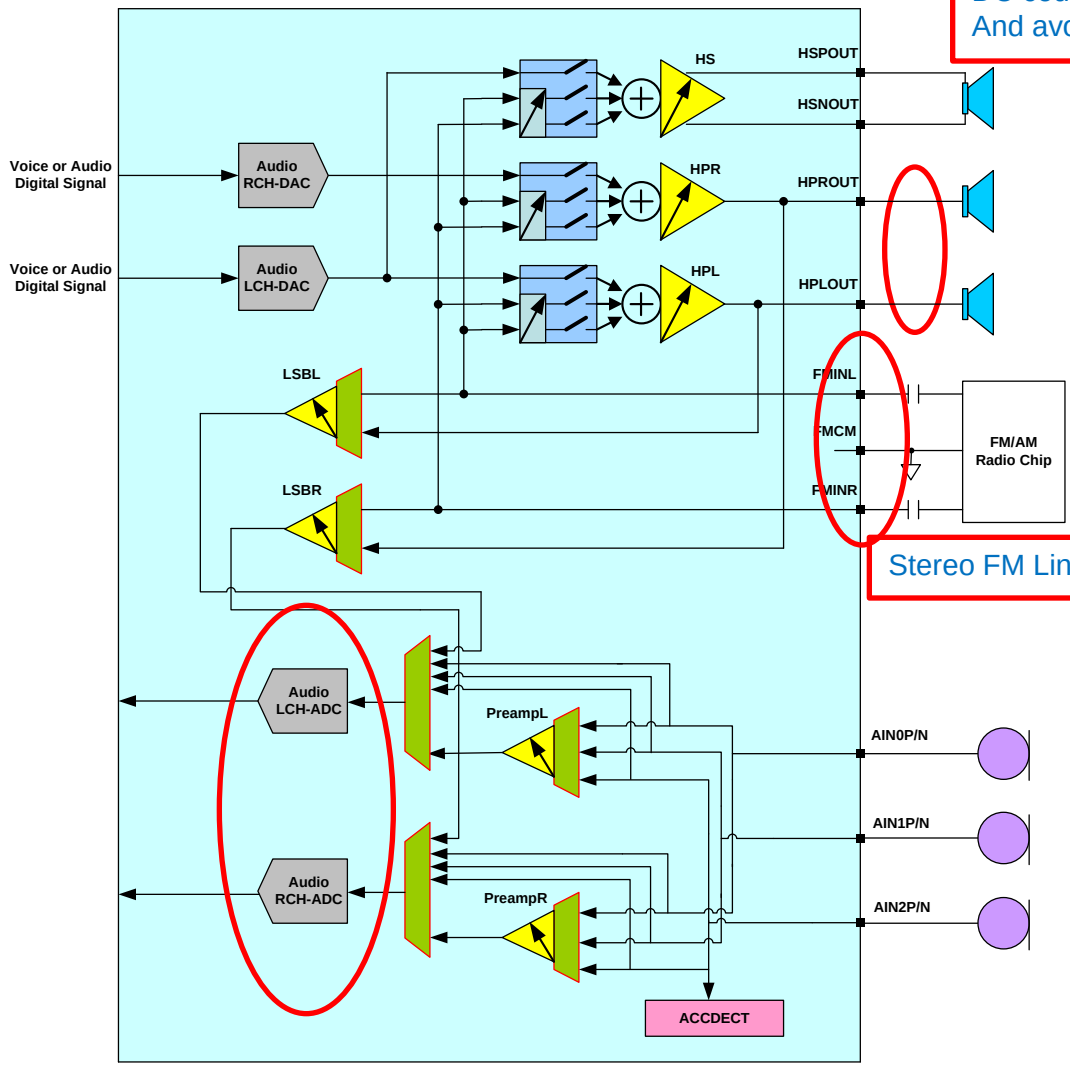
Design Notice – Audio (1/6)

- **Audio Block diagram :**

DC couple Audio to save DC block cap.
And avoid power on POP

Audio DAC replace
Voice DAC



Stereo FM Line in

Dual ADC with spared
PGA support

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Design Notice – Audio (2/6)

- **MT6251/6276/6573 compare:**
  - **MT6573 is the DC couple Audio in Mediatek solution**
  - **The output range is +/- 1.2V at Audio buffer output**
  - **Build in Negative charge pump(NCP) to generate negative power for DC couple audio required**
  - **DO NOT connect 1.8/2.8V power domain circuit to Audio buffer output**
  - **DO NOT USE TVS Diode for ESD protection at Audio Buffer output (replaced by VCE)**

		MT6251	MT6276	MT6573
MIC	gain range (dB)	-20 ~ +43	-14 ~ +49	-14 ~ +49
	Digital Mic support	x	v	v
	gain step size	1dB	1dB	1dB
voice buffer 0	gain range (dB)	-32 ~ +8	-32 ~ +8	-32 ~ +8
	gain step size	1dB	1dB	1dB
	Engineer mode range	0 ~ 255	0 ~ 255	0 ~ 255
audio buffer	gain range (dB)	-32 ~ +8	-32 ~ +8	-32 ~ +8
	gain step size	1dB	1dB	1dB
	Engineer mode range	0 ~ 255	0 ~ 255	0 ~ 255
SPK AMP	Amp Type	ClassAB/D	x	x
	gain range (dB)	12/18dB	x	x
	gain step size	x	x	x
FM	gain range (dB)	x	x	-30~24
	Stereo	x	x	v

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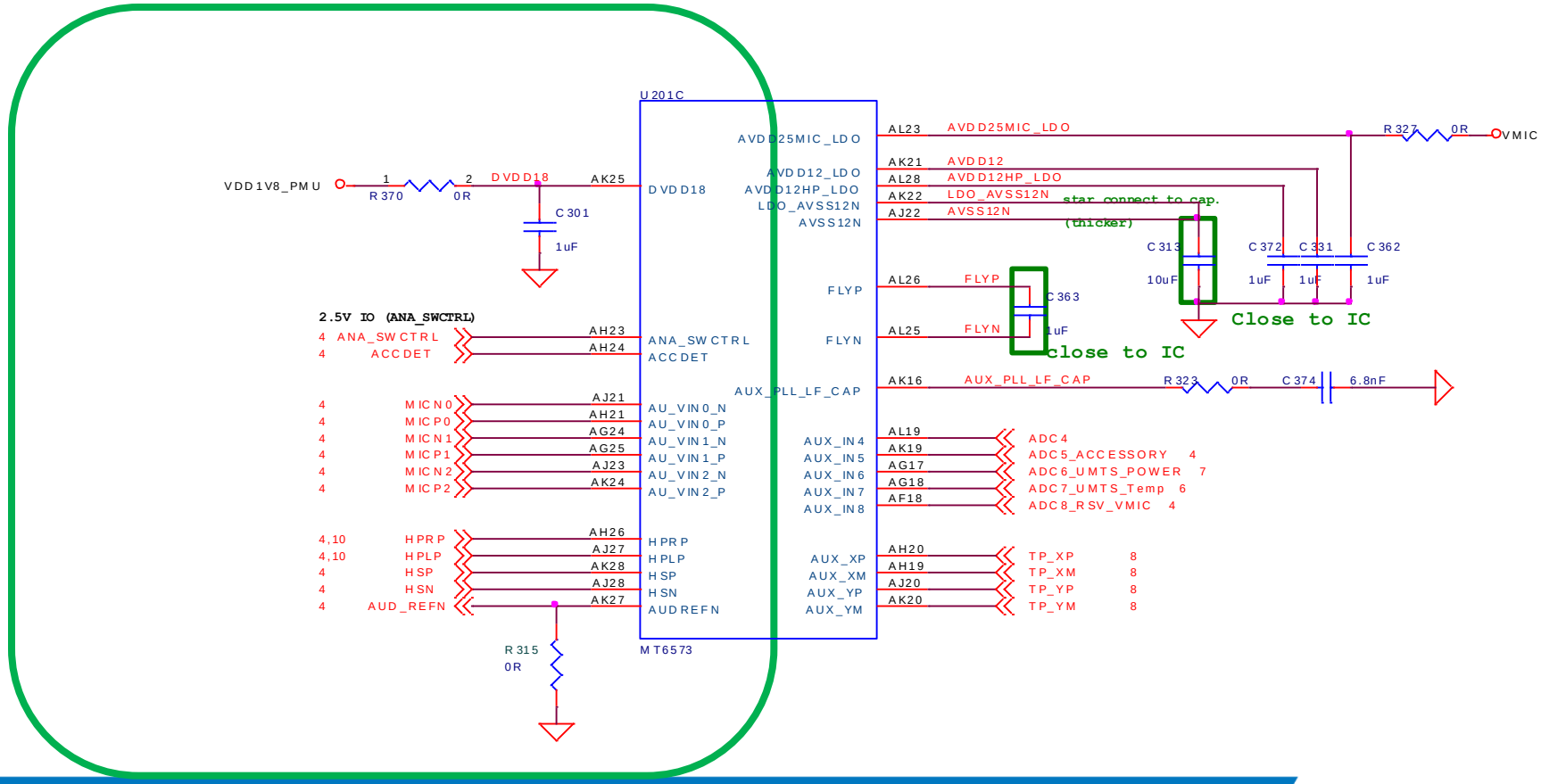
Design Notice – Audio (3/6)

- **Audio Signal schematic and layout :**
  - The signal of Audio block should shielding by GND
  - Pin AK27 is the reference point of DC couple Audio , direct connect to Main GND (Like AUVCM at MT6253)



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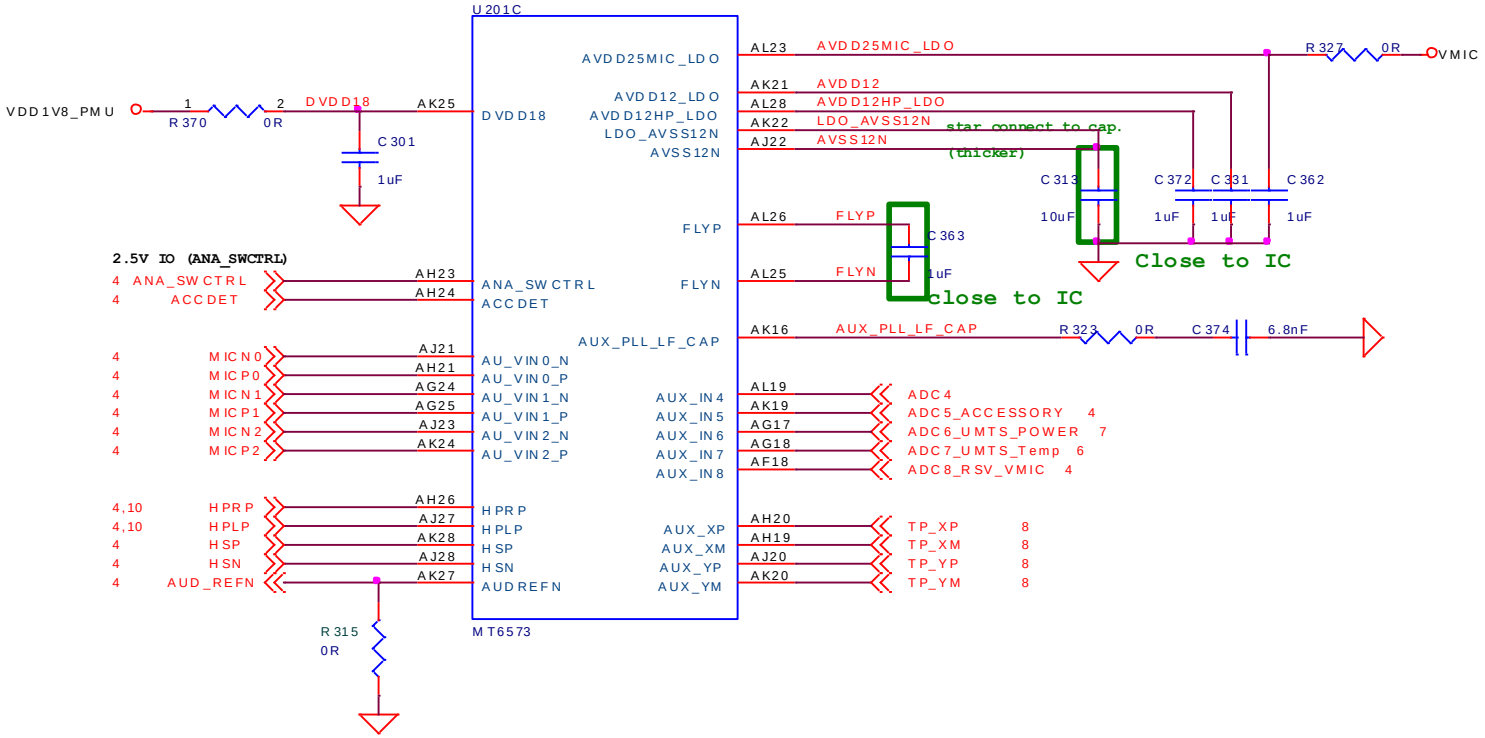
Design Notice – Audio (4/6)

- **Audio Power schematic and layout :**
  - C363 is the Flying capacitor for generate -1.25V to DC couple Audio
  - Pin AK22 is the -1.25V output for Pin AJ22 (DC couple Audio buffer)
  - Star connection from C313 to Pin AK22 and AJ22 is required
  - ADC8_RSV_VMIC (pin AF18) is the spare MicBias for headset Microphone



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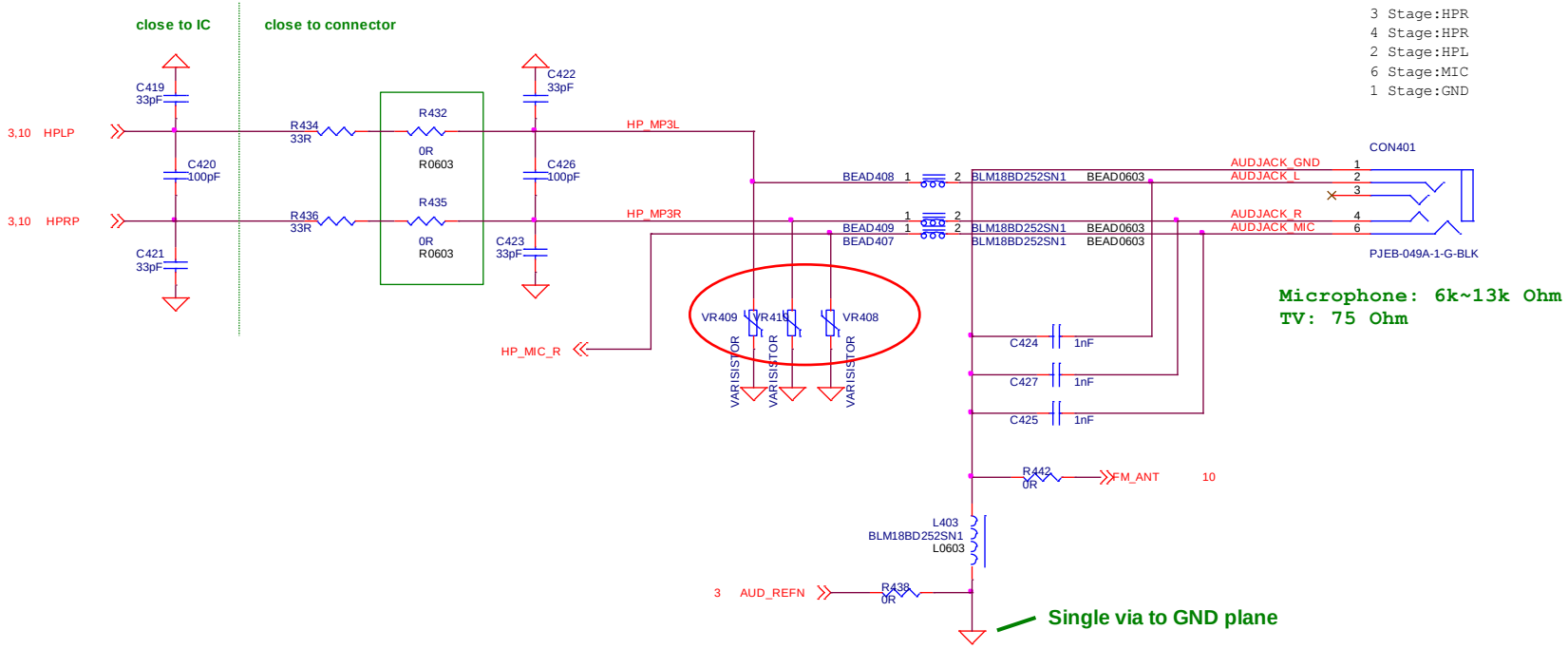
Design Notice – Audio (5/6)

- **DC couple Earphone :**
  - No need extra DC block cap.
  - USE VARISTOR FOR ESD PROTACTION IN DC COUPLE AUDIO

Earphone RECEIVER

Audio Jack



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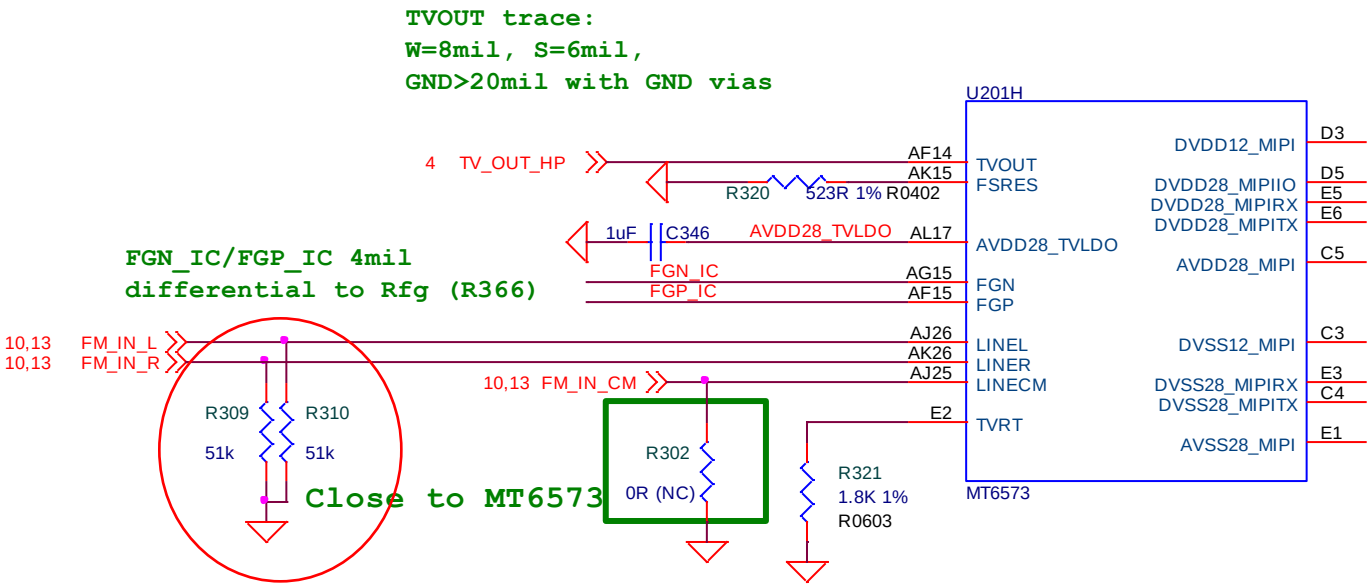
Design Notice – Audio (6/6)

- **Audio Line in:**

  - For Line In playback app. Need Pull low resistor to generate default DC voltage



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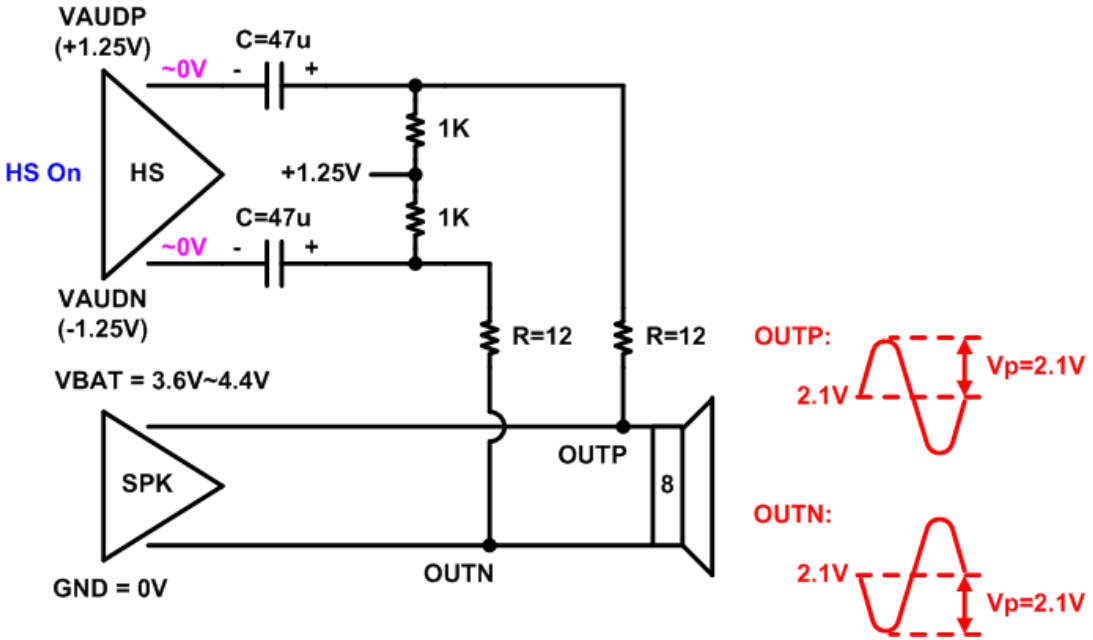
2-in-1 Loudspeaker Support

- Class-AB
  - **Adding two "47uF cap." between (HS buffer , SPK output)** to block DC voltage
  - **Adding two "1k resistor" and pull up to VAUDP(+1.25V) to build up DC voltage**
- Class-D
  - Two analog switch still need to replace 12ohm resistor



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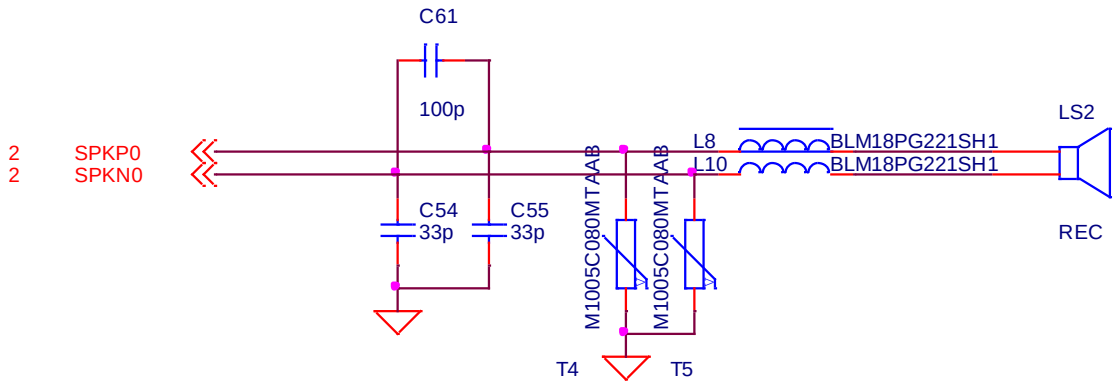
Design Notice – SPK Amp

- **External Class-AB/D Audio Amplifier :**
  - The trace width of SPK_P and SPK_N should be greater than 25 mil for 8ohm SPK
  - The Net of SPK_P and SPK_N should be shielded by GND
  - Please select Bead for Amp output filter which R_{DC} < 0.1ohm and Rated Current > 1.1A

LOUD SPEAKER



Vendor	P/N	Rdc(ohm)	Rate current(mA)
Murata	BLM18PG221SH1	0.1	1400
	BLM15PD800SN1	0.07	1500
	BLM18KG221SN1	0.05	2200
	BLM18KG331SN1	0.08	1700
	BLM18SG221TN1	0.04	2500
	BLM18SG331TN1	0.07	1500
	BLM18EG221SN1	0.05	2000
TDK	MPZ1608S221A	0.05	2200
	MPZ1608S331A	0.08	1700
	MPZ1608Y221B	0.1	1500

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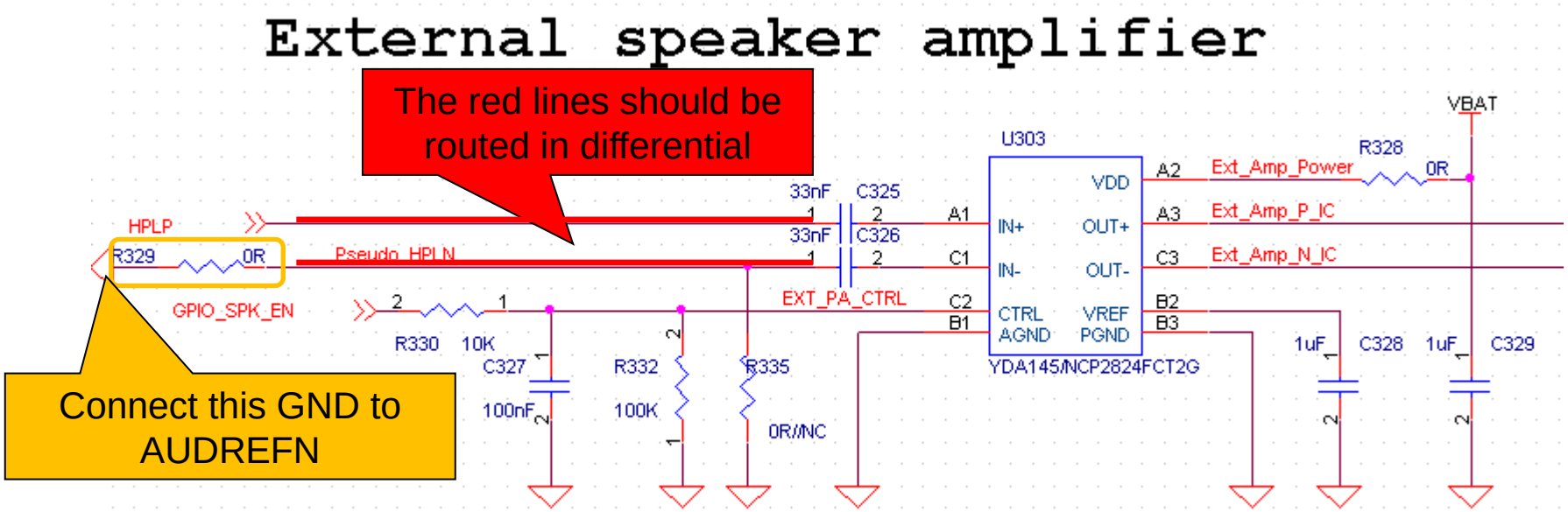
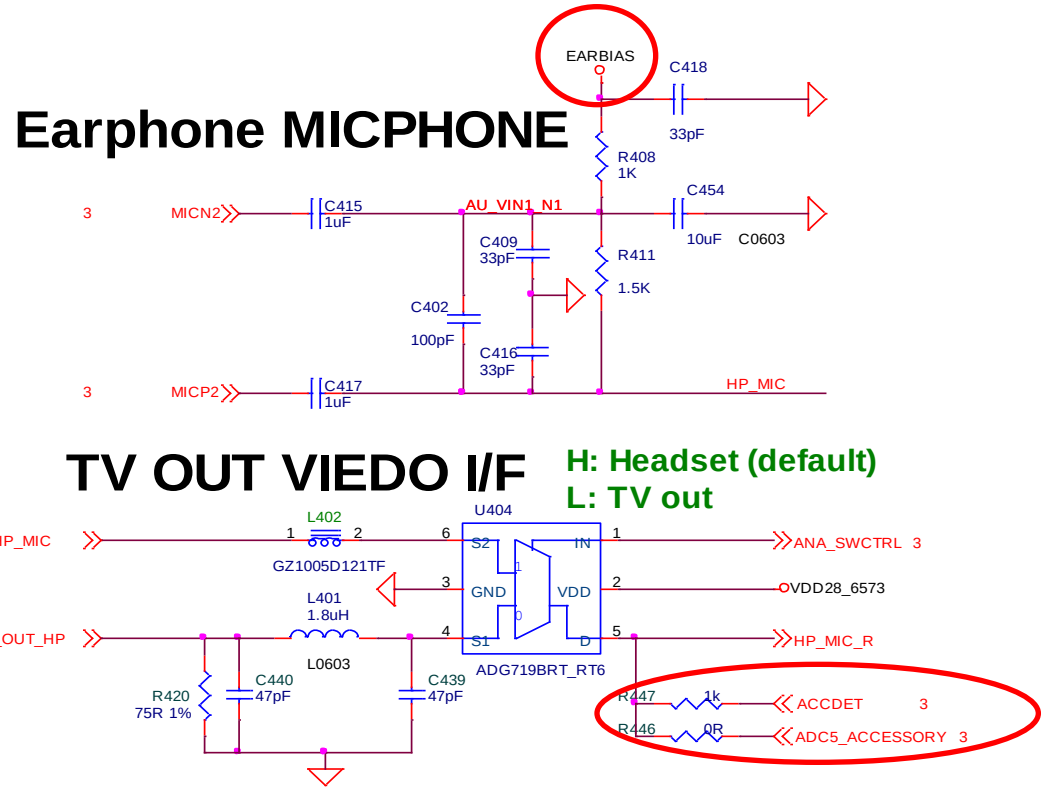
External Speaker Amplifier application note

- Connect R329 GND Pin to AUDREFN pin of BB Chip
- Pseudo_HPLN of R329 must layout as differential line with HPLP
- External Speaker Amplifier PSRR > 60dB @ Frequency<1KHz



Accessory detect at DC couple solution – 1

- Solution in MT6573(With TV out)
  - Analog switch is needed for earpiece/TV_cable share connector
  - ACCDET and AUXADC connect to HP_MIC near connector side
  - EARBIAS is the extra microphone bias for earpiece and named ADC8_RSV_VMIC4 at MT6573



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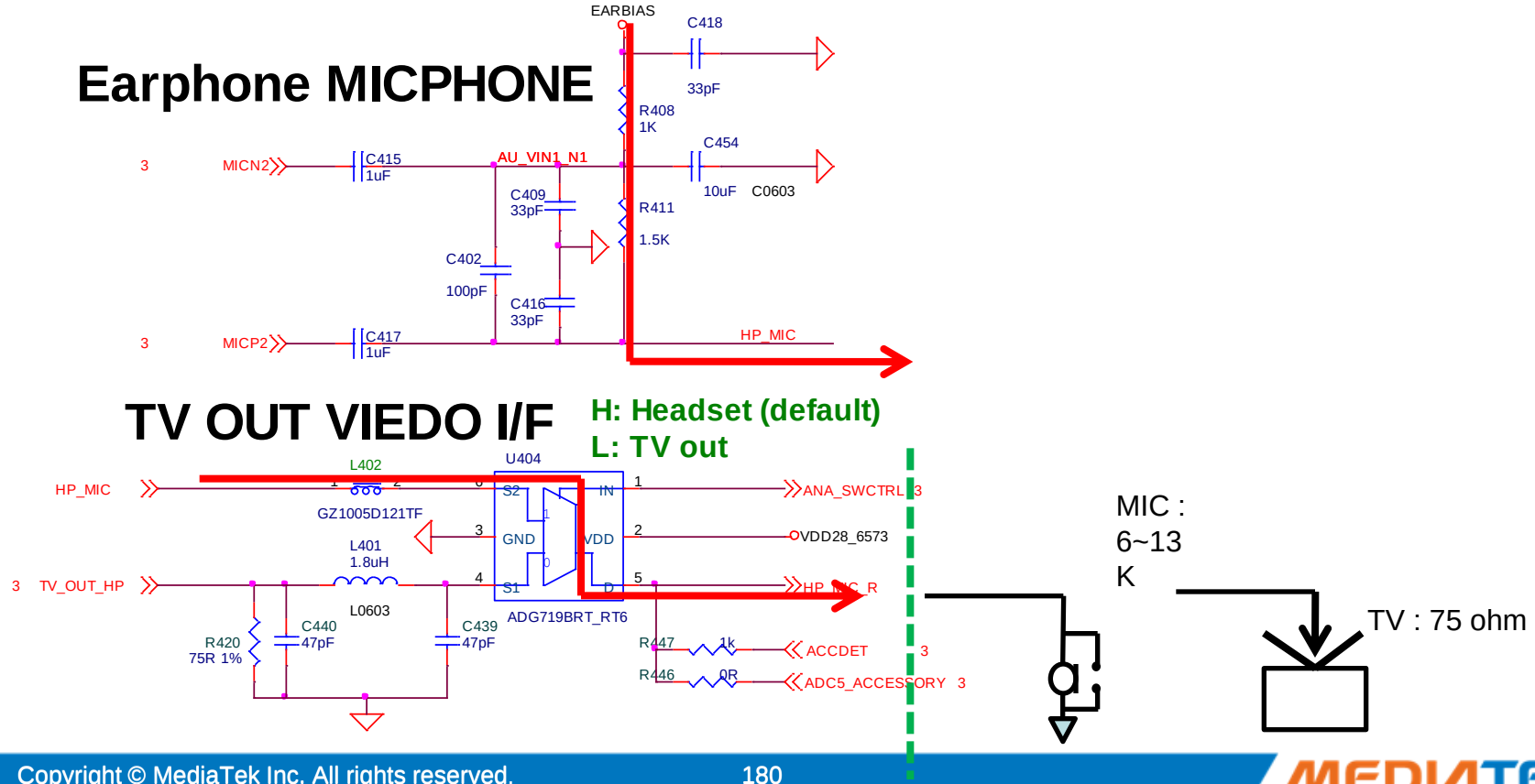
Accessory detect at DC couple solution – 1

- Case 1 detection of plug in earpiece or not
  - check AB value of ACCDET
    - 11 : no device plug in — High than 1.7V
    - 01 : earpiece plug in — 0.4V~1.7V
    - 00 : Enter double check status — under 0.4V



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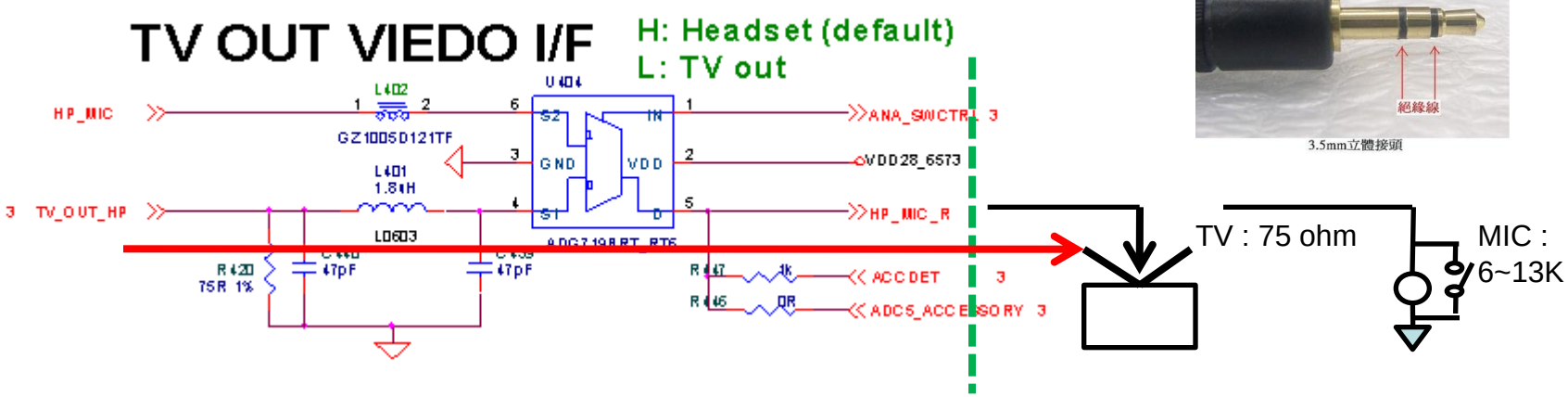
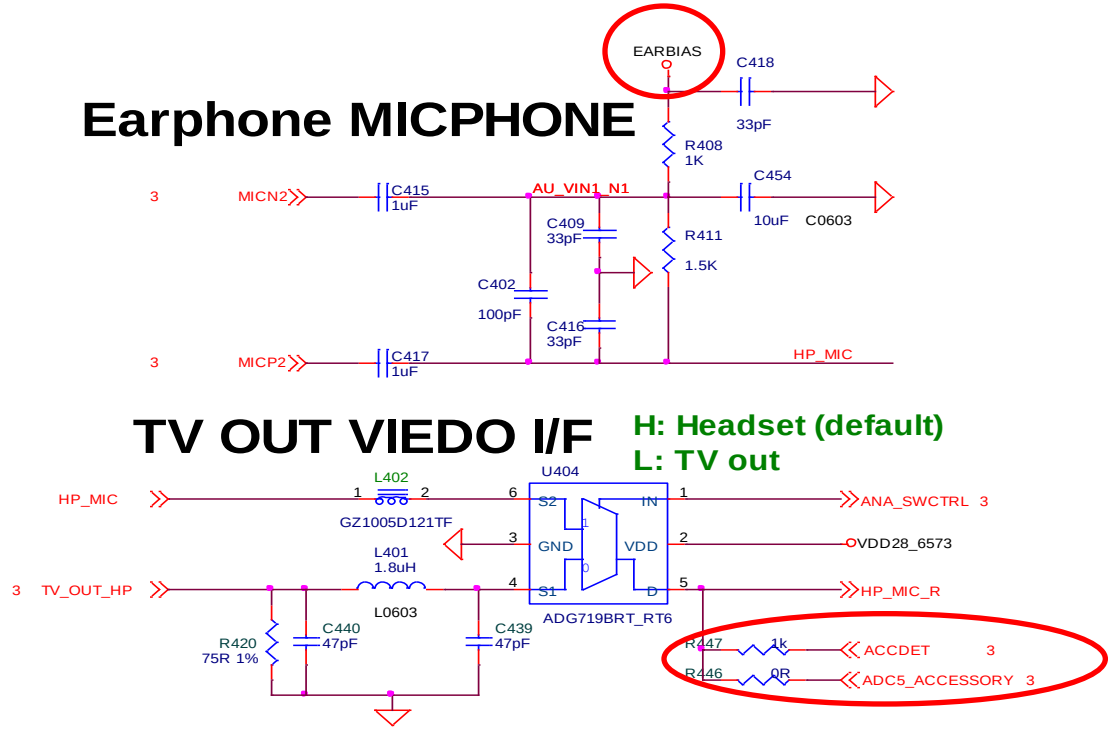
Accessory detect at DC couple solution – 1

- Double check status
  - Switch to TV path first
  - TV DAC output All white signal at VBI interval
  - Check AB value of ACCDET again
    - 11 : Earpiece plug in and in hook switch release High than 1.7V
    - 01 : TV Cable plug in and connect to TV 0.4V~1.7V
    - 00 : Earpiece plug in and Hook switch pressed under 0.4V
      or Normal 3.5mm earpiece (without microphone)



Current Accessory detect solution

- Structure
  - ACCDET connect to HP_MIC
  - EARBIAS for earpiece microphone bias



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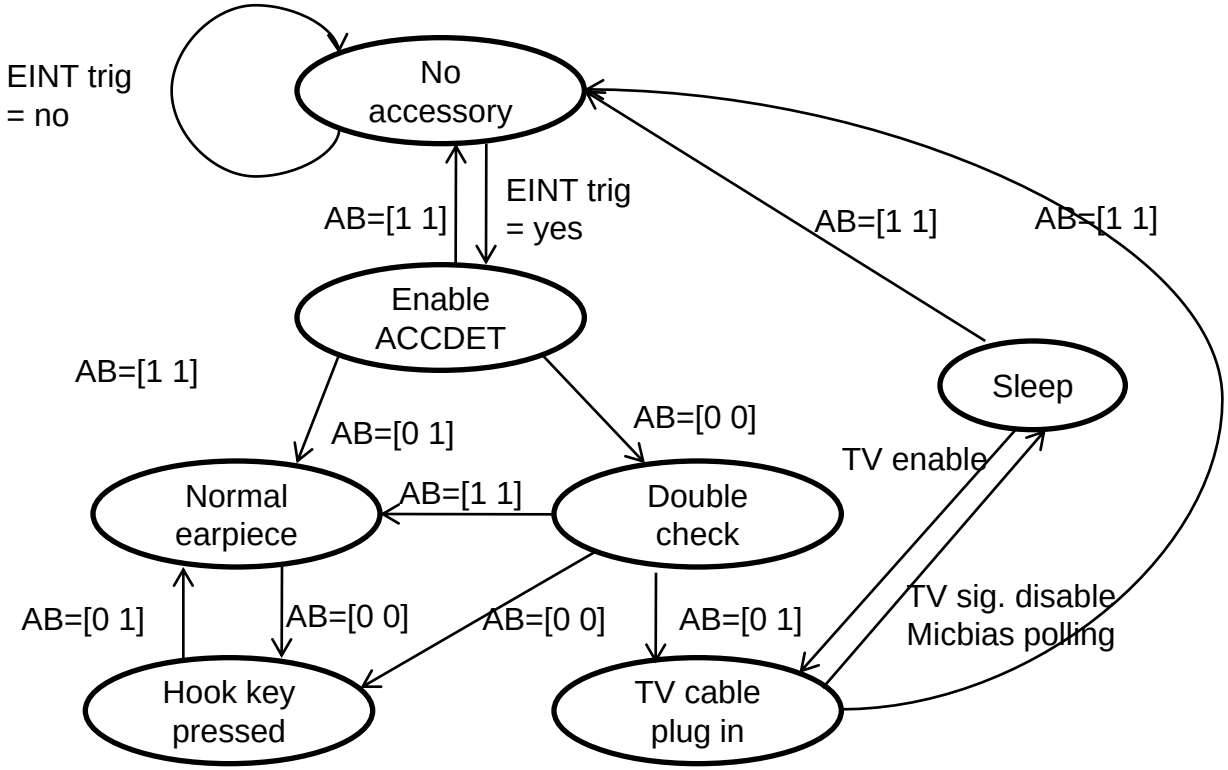
Updated Accessory detect solution - Structure

- Advantage
  - When using 2.5/3.5mm standard earphone jack , detect state machine will start after plug in finished.
  - There is no noisy sound cause by detect behavior during plug in 2.5/3.5mm standard earphone jack.
  - Delay time of EINT trig ACCDET is custom setting (default 1000ms)



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Updated Accessory detect solution – SW setting

- Structure
  - Please use the earphone jack which with switch pin
  - The other EINT pin connect to the switch pin through 47K ohm
  - ACCDET connect to HP_MIC through 1K ohm

- SW setting of EINT+ACCDET
  - Complier Option : accdet_custom.h

New detection method enable

```
#define ACCDET_EINT // if define ACCDET_EINT we can use EINT to adjust headset plug in

#ifdef ACCDET_EINT
#define ACCDET_DELAY_ENABLE_TIME 1000 //delay 1000ms to enable accdet after EINT
//#define ACCDET_EINT_HIGH_ACTIVE //defaule is active if not define ACCDET_EINT_HIGH_ACTIVE
#endif
```

Delay time of EINT trig ACCDET

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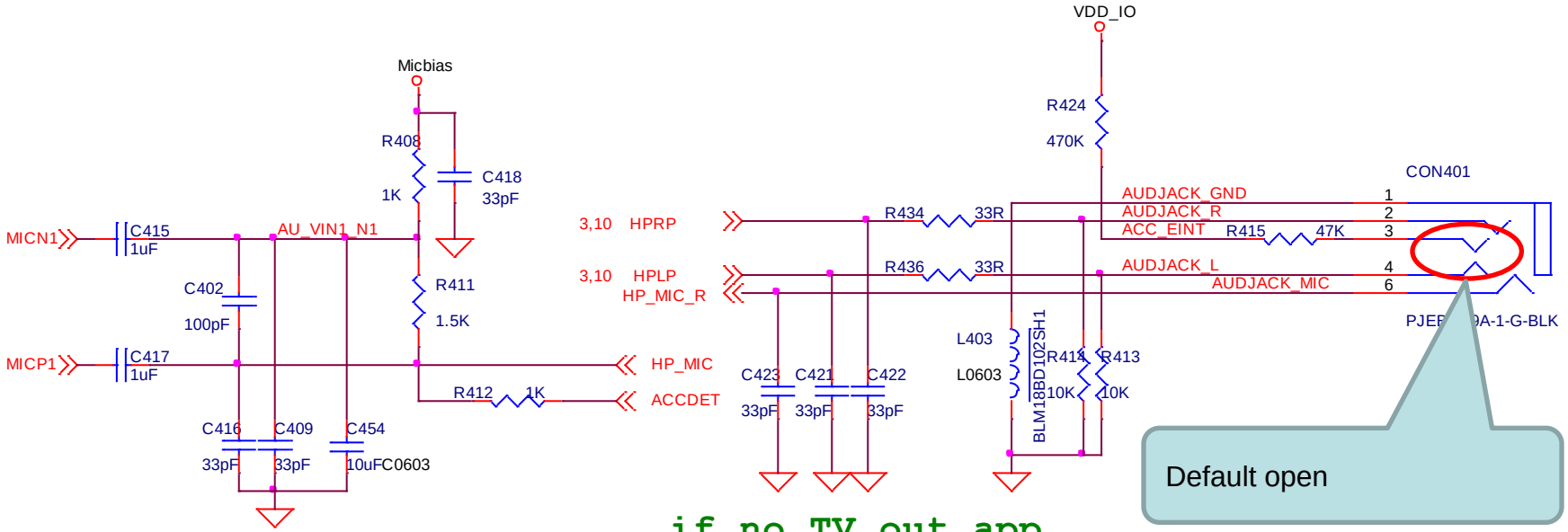
Updated Accessory detect solution – Circuit of default open earphone Jack

- User scenario
  - ACCDET trigged by “EINT high to low” modified by Drv tool
  - Didn’t use internal Pull up or Pull low at used EINT

EINT_ACCDET Default high
Plug in ==> Low



if no TV out app.
can remove pull low resistor

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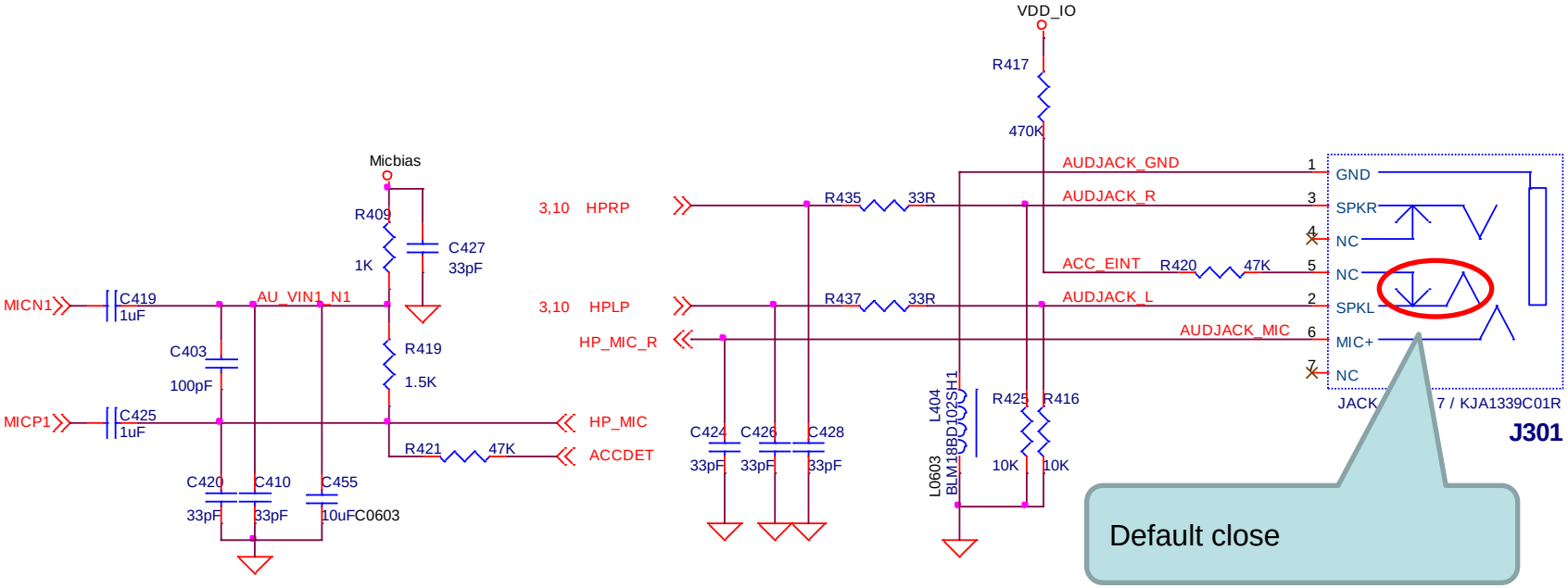
Proposed Accessory detect solution – Circuit of default Short earphone Jack

- User scenario
  - ACCDET trigged by “EINT low to high” modified by Drv tool
  - Didn’t use internal Pull up or Pull low at used EINT



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Internal Use

MT6573 LCM Design Notice

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LCM Design Note – Overview

- Display Resolution
  - Support HVGA(320x480) and up to WVGA(480x800) / FWVGA(480x864)
- Interface
  - Supports CPU 8/9/16/18/24 bit interface
  - Supports RGB565/666/888 interface
  - Supports MIPI DSI command/video mode, 2-Lane interface
  - Dedicated HW tearing free control pin for CPU and MIPI DSI interface
- IO Power
  - Support 1.8v/2.8v/3.3v IO level LCM (DVDD_LCD1, “Ball-N3”)
    - Beware below signals share the same IO voltage as LCM (PWM1, 2, 3, SCL1, SDA1 (I2C1), Serial & parallel LCD interfaces)

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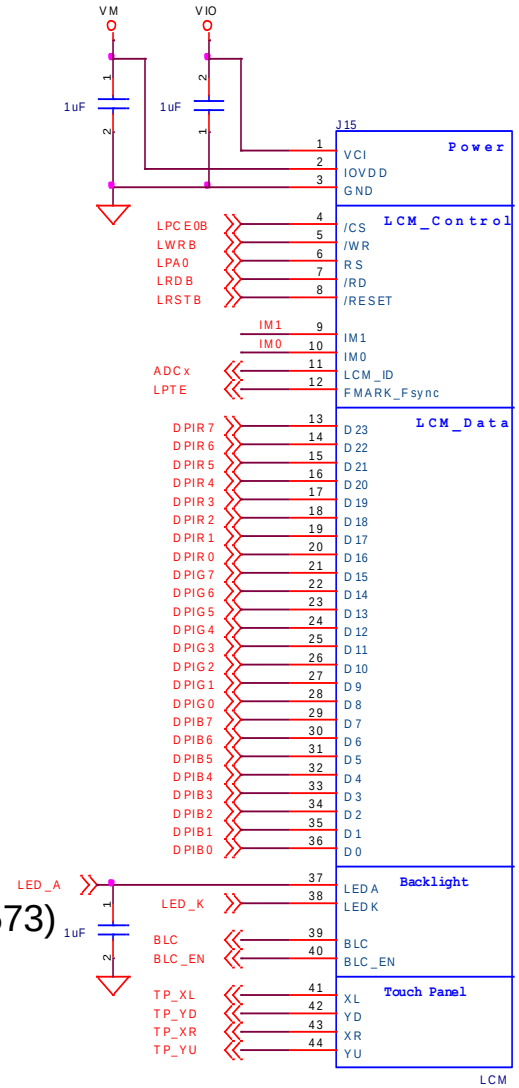
LCM Design Note

- LCM side design notice
  - Power
    - VCI : connect to 2.8v for LCM analog power
    - IOVDD : connect to 1.8v depends on LCM IO level
      - LCM IO level should follow NAND flash bus power level
  - LCM Control
    - All LCM control pin are reserved at BB side
    - IM[1:0] : Interface Mode should reference IOVDD level
    - LCM_ID pin connect to Aux_ADC
  - LCM Data
    - All LCM data pin are reserved at BB side
    - For 8 bit interface, some LCM use lower byte D[7:0], some use D[23:16]. Be sure data pin connect to the correct LCM pins.
  - Touch Panel
    - Connect to dedicated 4-wire R-type TP pin
  - CABC
    - BLC pin connect to backlight driver (external component for MT6573)
  - System performance
    - EMI filter on LCM control pin & dadtabus is optional (Trade-off between performance & cost). It could reserve at 1st version SMT.



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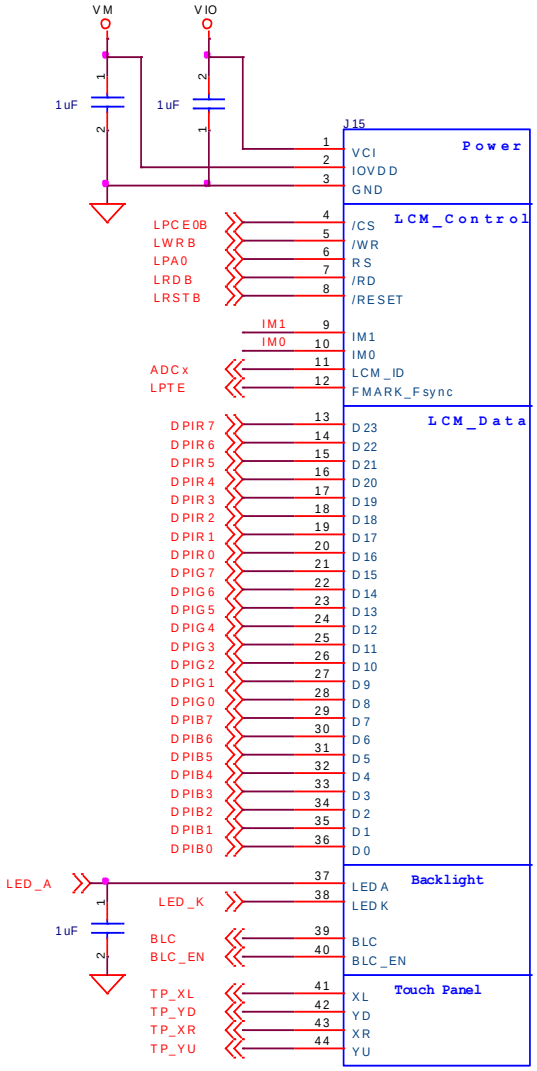
LCM Design Note – CPU Interface

- BB side design notice

MT6573 (Pin definition)		LCM side
LPCE0B	L6	/CS
LWRB	F5	/WR
LPA0	F4	RS
LRDB	F3	/RD
LRSTB	F2	/RESET
DPIR[7:0]	M4, N2, M2, N4, M6, K3, M5, M1	D[23:16]
DPIG[7:0]	L2, K2, K1, K4, L5, K5,J1, K6	D[15:8]
DPIB[7:0]	J2, J3, J4, J5, H2, H5, G5, H4	D[7:0]
LPTE	G1	FMARK / F_Sync



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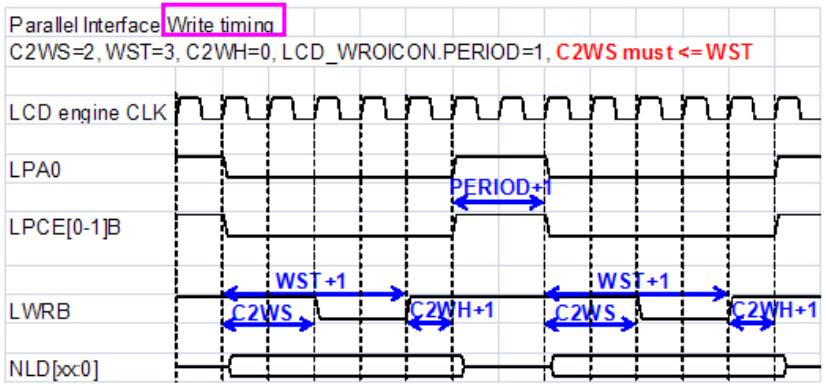
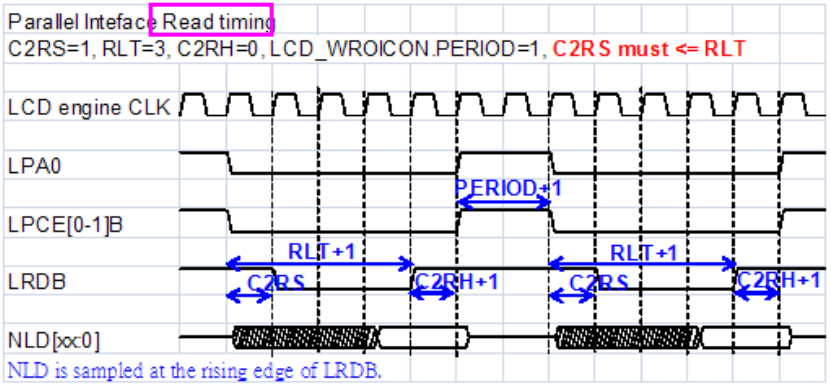
LCM Design Note – CPU Interface

- All control signals timing are reference LCM engine CLK 122.88MHz (1T=81.3ns)
- CPU IF control timing is well controlled by setting C2WS, C2WH and WST value based on “LCM engine CLK”

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2RH				C2RS						RLT					
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			C2WH		C2WS						WST					
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0





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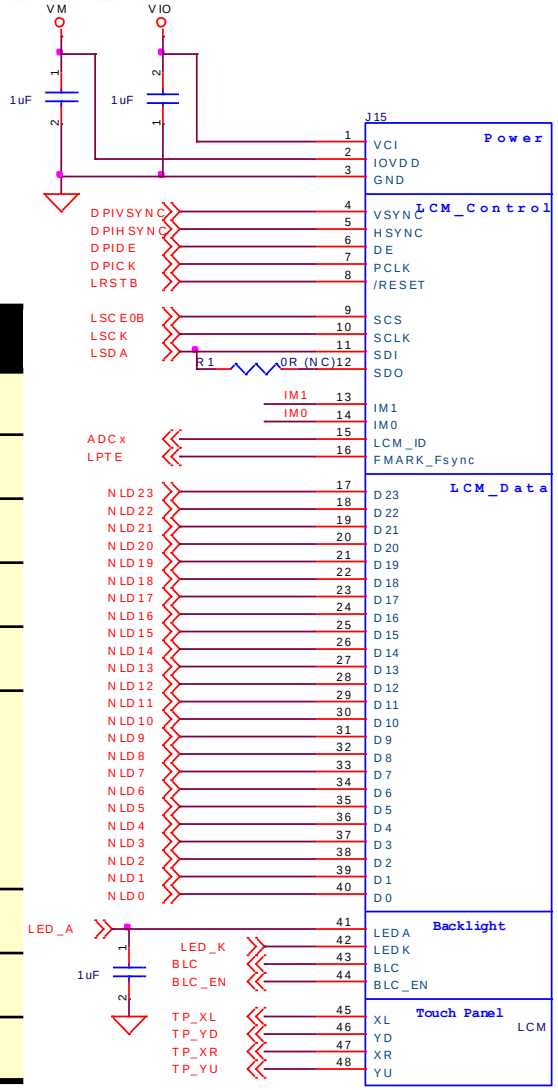
LCM Design Note – RGB Interface

- BB side design notice
  - RGB interface control pin are dedicated
  - RGB data pin are share with CPU interface
  - No need for LPTE for tearing free
  - SPI Interface is used for system initialization
    - BB LSDA connect to LCM SDI or SDA
    - If LCM has SDO pin, leave it floating or connect to LSDA through a 0ohm

MT6573 (Pin definition)		LCM side
DPIVSYNC	N7	VSYNC
DPIHSYNC	N6	HSYNC
DPIDE	P6	DE
DPICK	P5	PCLK
LRSTB	F2	/RESET
DPIR[7:0]	M4, N2, M2, N4, M6, K3, M5, M1	R[7:0]
DPIG[7:0]	L2, K2, K1, K4, L5, K5,J1, K6	G[7:0]
DPIB[7:0]	J2, J3, J4, J5, H2, H5, G5, H4	B[7:0]
LSCE0B	P3	SCS
LSCK	P2	SCLK
LSDA	R6	SDI



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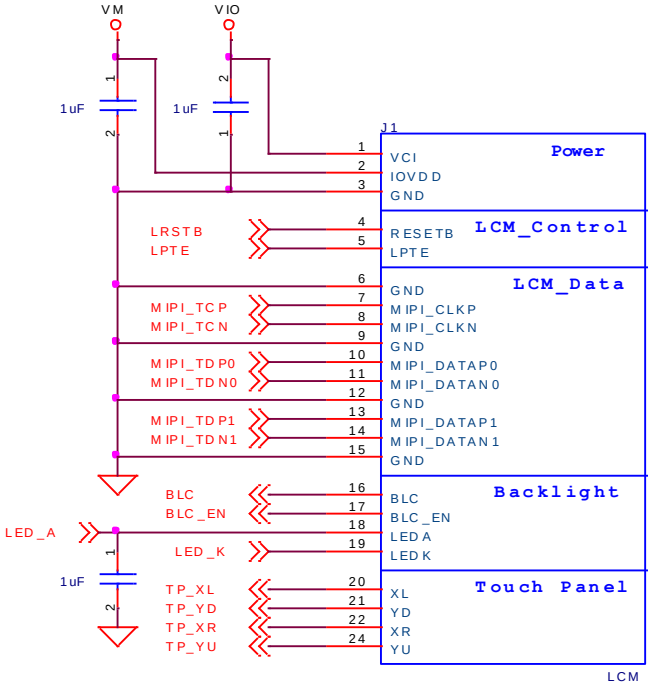
LCM Design Note – MIPI DSI Interface

- BB side design notice
  - MIPI DSI Interface do good to system design simplicity
  - MIPI DSI clk/data are differential pair and trace layout should meet 100ohm differential impedance
    - MIPI_TCP / MIPI_TCN
    - MIPI_TDP0 / MIPI_TDN0
    - MIPI_TDP1 / MIPI TDN1

MT6573 (Pin definition)		LCM side
TCP	A4	MIPI_CLKP
TCN	B5	MIPI_CLKN
TDP0	B3	MIPI_DATAP0
TDN0	B4	MIPI_DATAN0
TDP1	B6	MIPI_DATAP1
TDN1	A6	MIPI_DATAN1
LRSTB	F2	/RESET
LPTE	G1	FMARK / F_Sync



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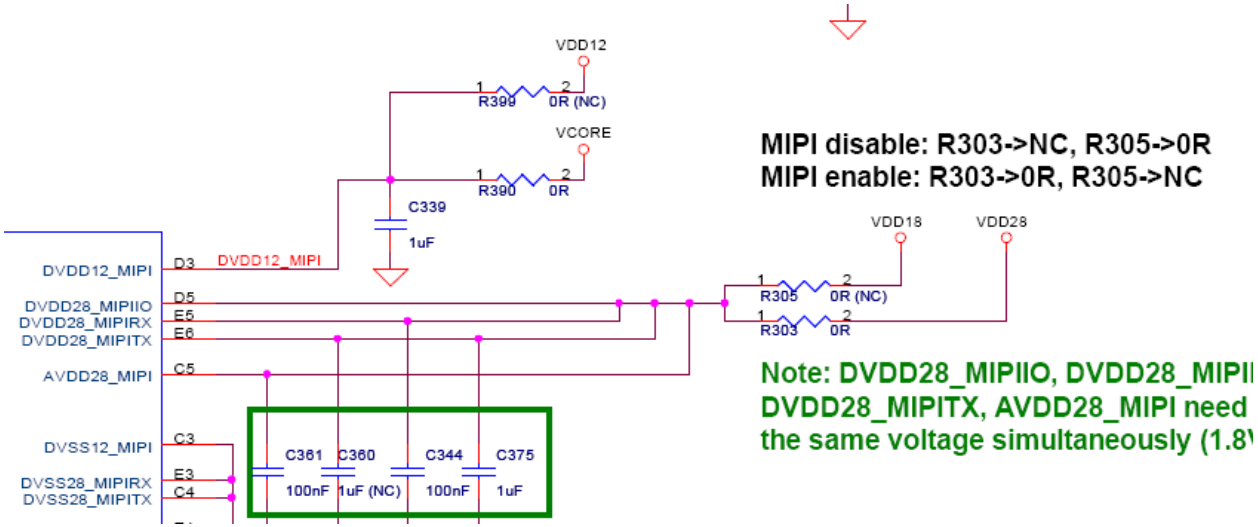
LCM Design Note – MIPI DSI Interface

- TVRT (pin E2) must connect 1.8K to GND for MIPI PHY reference current circuit
- MIPI Power domain
  - DVDD12_MIPI connect to 1.2v
  - DVDD28_MIPIIO (pin D5), DVDD28_MIPITX (pin E6), DVDD28_MIPIRX (pin E5), and AVDD28_MIPI (pin C5) connect to 2.8v
- By pass cap for MIPI power domain need to close to BB chip



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MT6573 LCM Mode selection

- MT6573 provide 4 modes for LCM pin mux solution for CPU/RGB Interface
  - MIPI DSI Interface are dedicated pins (no mux with CPU/RGB Interface)
- Mode Description
  - Mode 0 : RG565/666/888 Interface + NAND16bit + TD16bit
  - Mode 1 : RGB565 + NAND16bit + TD16bit
    CPU18 + NAND16bit + TD16bit
  - Mode 2 : CPU24 + NAND16 + TD16bit
  - Mode 3 : CPU24 + NAND16 + TD 16bit
- Customer Suggestion
  - RGB Interface → Suggest them use mode 0
  - CPU Interface → Suggest them use mode 3

	lcd_io_sel	NLD																DPI																											
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	B0	B1	B2	B3	B4	B5	B6	B7	G0	G1	G2	G3	G4	G5	G6	G7	R0	R1	R2	R3	R4	R5	R6	R7
16-bit CPU/16-bit		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	b0	b1	b2	b3	b4	b5	b6	b7	g0	g1	g2	g3	g4	g5	g6	g7	r0	r1	r2	r3	r4	r5	r6	r7
Nand + 24-bit	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15																								
18-bit CPU/16-bit		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	b2	b3	b4	b5	b6	b7	g2	g3	g4	g5	g6	g7	r2	r3	r4	r5	r6	r7				
Nand + 18-bit	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15																								
24-bit CPU/16-bit		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	g0	g1	g2	g3	g4	g5	g6	g7								
Nand + 8-bit	2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15																								
16-bit Nand + 24-bit CPU	3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
IO driving group		NLD0								NLD1								DPI0		DPI1						DPI2								DPI3		DPI4		DPI5			

: Nand IF
: CPU IF
: RGB IF

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Internal Use

Content Adaptive Backlight Control (CABC)

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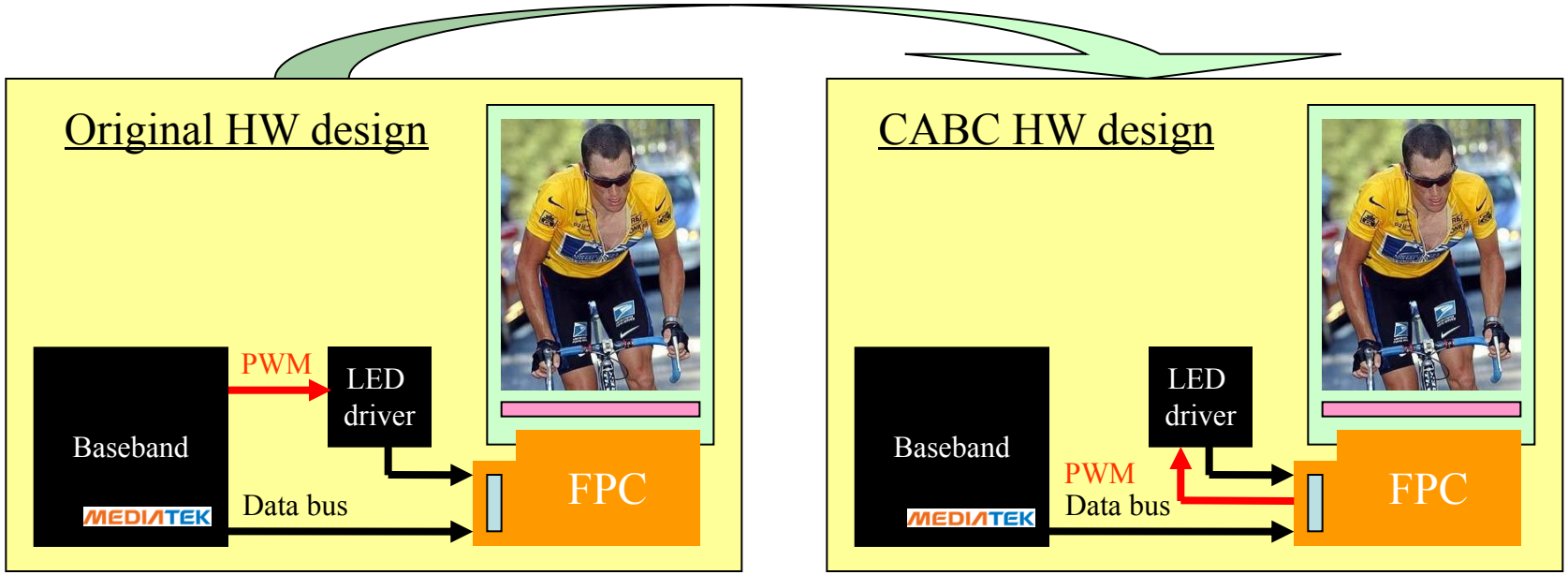
LCM Design Note – CABC

- **CABC applies a content based PWM control method for LCM backlight brightness control which reduce power 0%~50%**
- **LCM Selection Guide**
  - **LCD driver IC should support PWM output for backlight LED driver control (with BL_PWM or BL_EN pin)**



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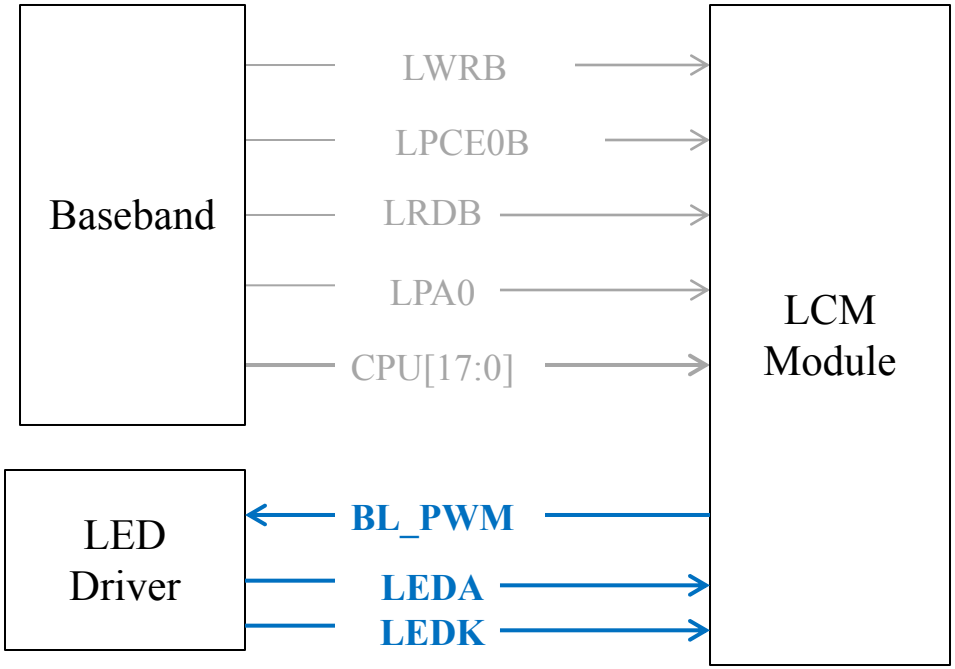
LCM Design Note – CABC

- CABC Connection Guide (ex. CPU18bit + CABC)



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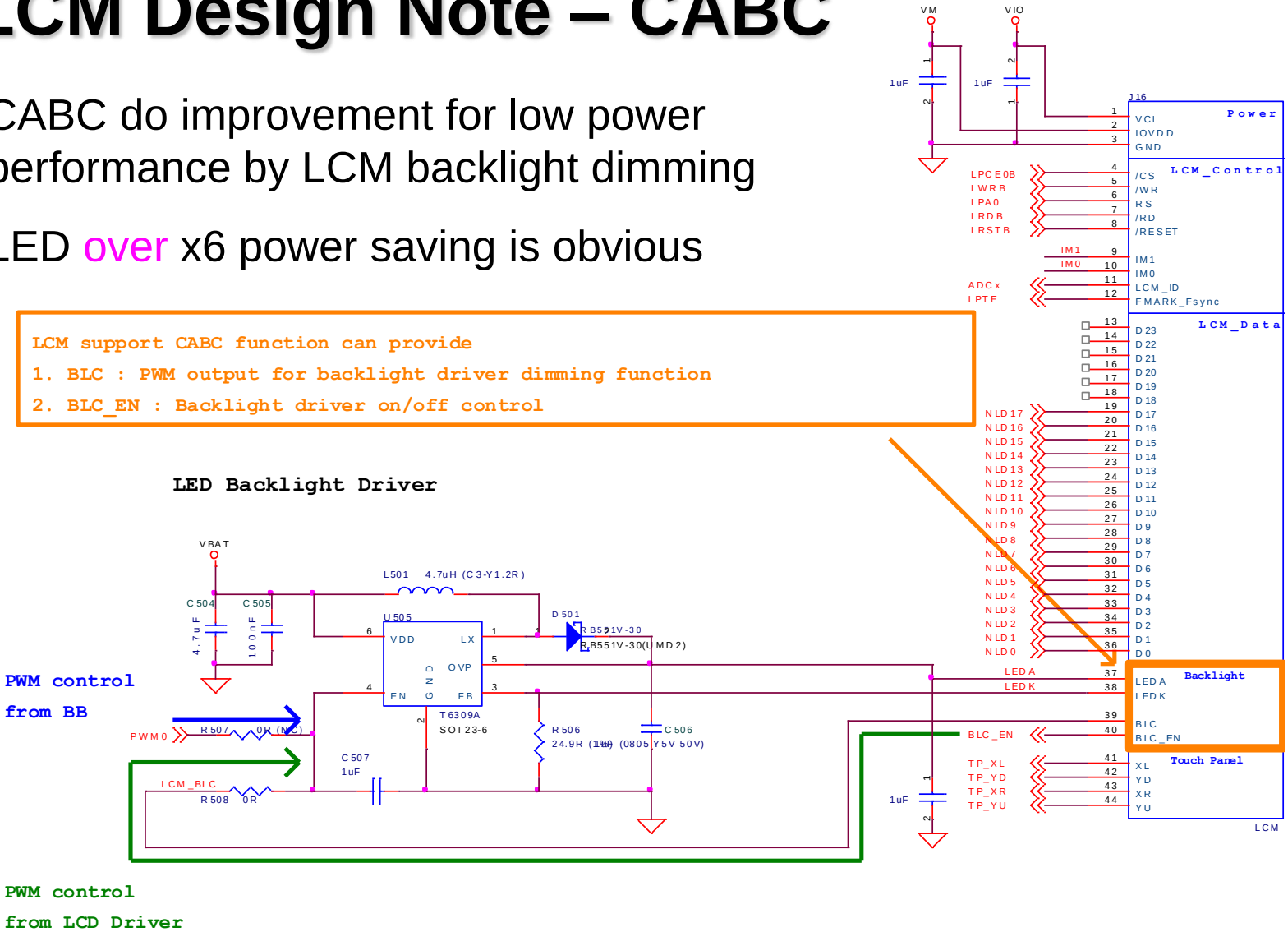
LCM Design Note – CABC

- CABC do improvement for low power performance by LCM backlight dimming
- LED over x6 power saving is obvious

LCM support CABC function can provide
1. BLC : PWM output for backlight driver dimming function
2. BLC_EN : Backlight driver on/off control



Confidential B

MT6573 Camera Design Notice

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Parallel Image Sensor Interface

BB Chip (Pin definition)	Camera side
VCAMA(AF28)	AVDD
VCAMD(AF30)	DVDD
VCAMA2(AG28)	AF_VDD
VCAMD2(AD28)	DOVDD
CMVREF	VSYNC
CMHREF	HSYNC
CMPCLK	PCLK
CMMCLK	MCLK
SDA1	SIOD
SCL1	SIOC
CMRST	RESETB
CMPDN	PWDN
CMDAT0~CMDAT9	DATA0 ~ DATA9

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MIPI CSI-2 Image Sensor Interface

BB Chip (Pin definition)	Camera side
RDP1	MDP1
RDN1	MDN1
RCP	MCP
RCN	MCN
RDP0	MDP0
RDN0	MDN0
SDA1	SIOD
SCL1	SIOC
CMRST	RESETB
CMPDN	PWDN
CAM_STROBE	STROBE
CMMCLK	MCLK

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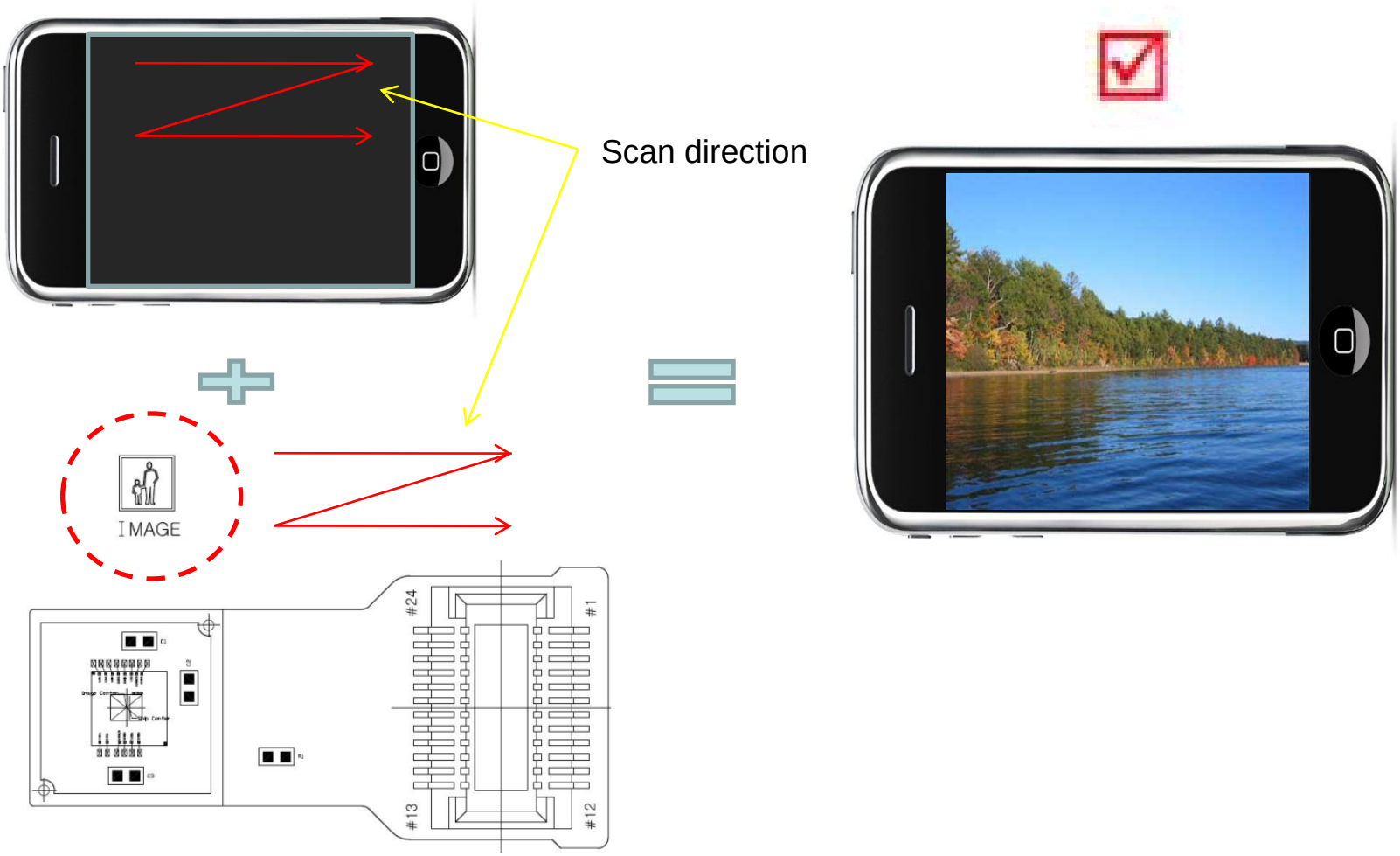
Sensor Module Selection



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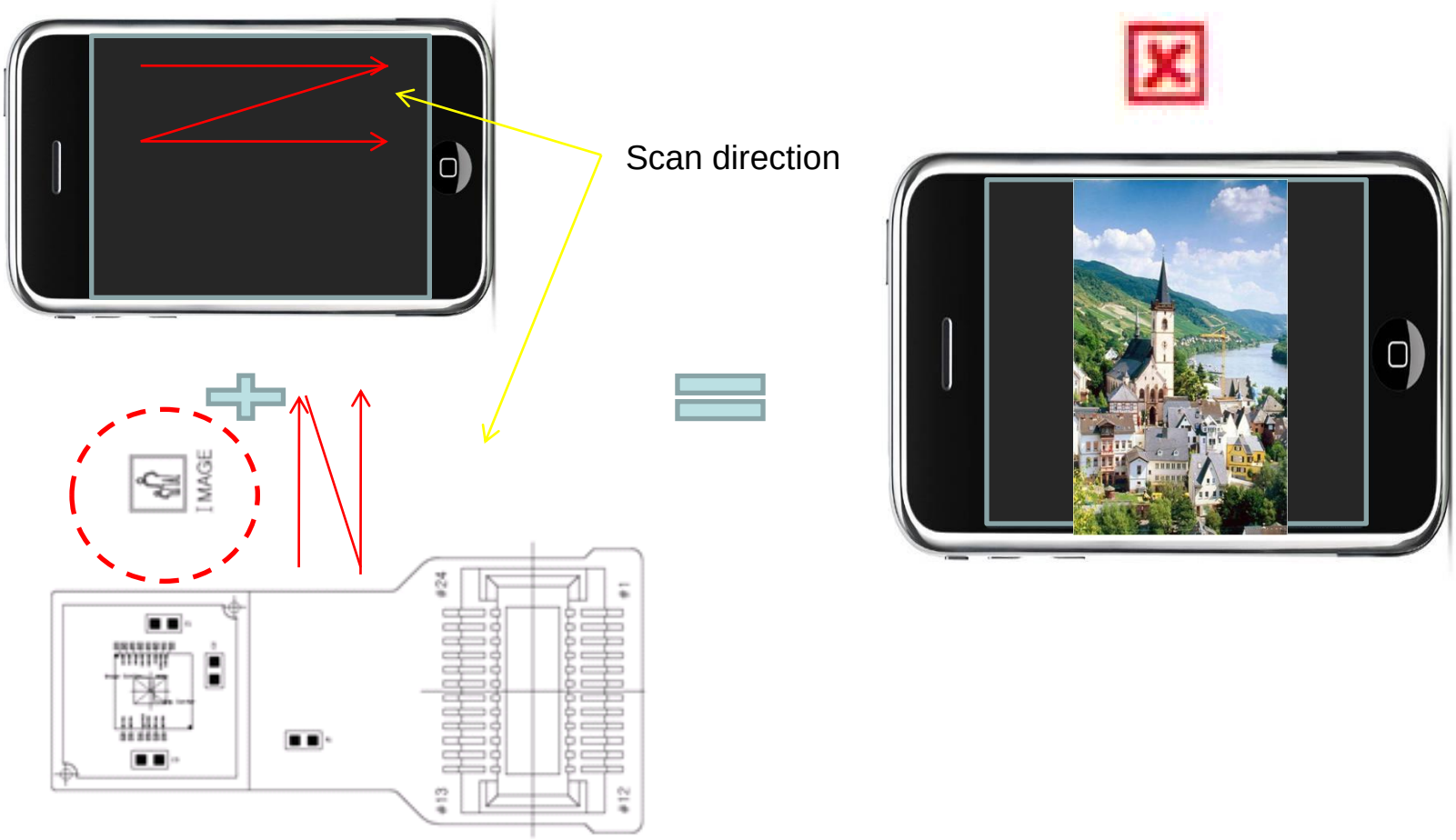
Sensor Module Selection



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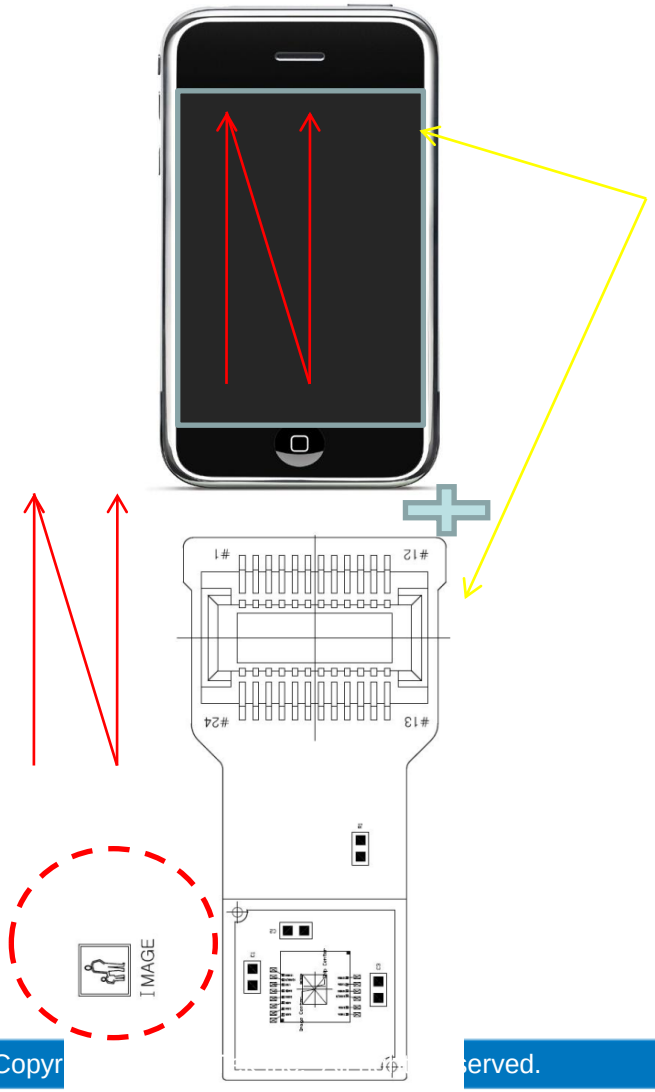
Sub camera placement

Sub camera is proposed to video call. (VT mode)

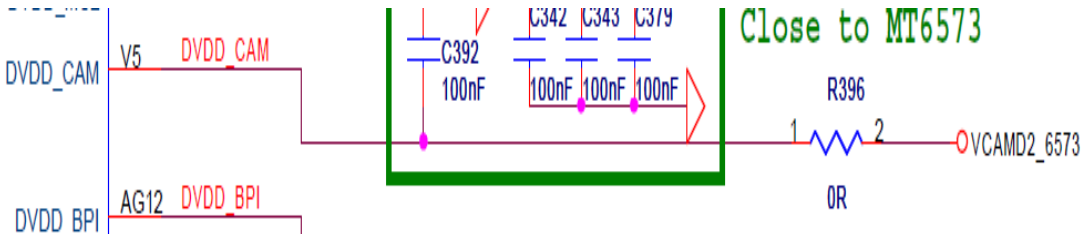


Be careful the scan direction

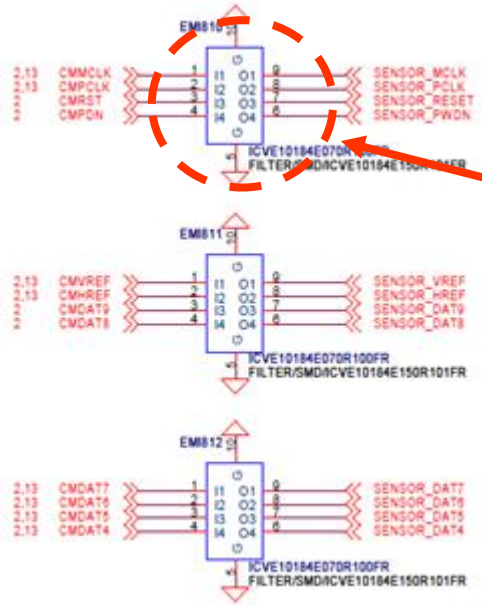
Both front- and rear-facing cameras, if present, MUST be oriented so that the long dimension of the camera aligns with the screen's long dimension.

Recommend by ICS

Camera Reference Circuit



Sensor's IO level is defined by DVDD_CAM. (VCAMD2_6573)



For Parallel Sensor :

EMI filter cap. max. loading is 30pf

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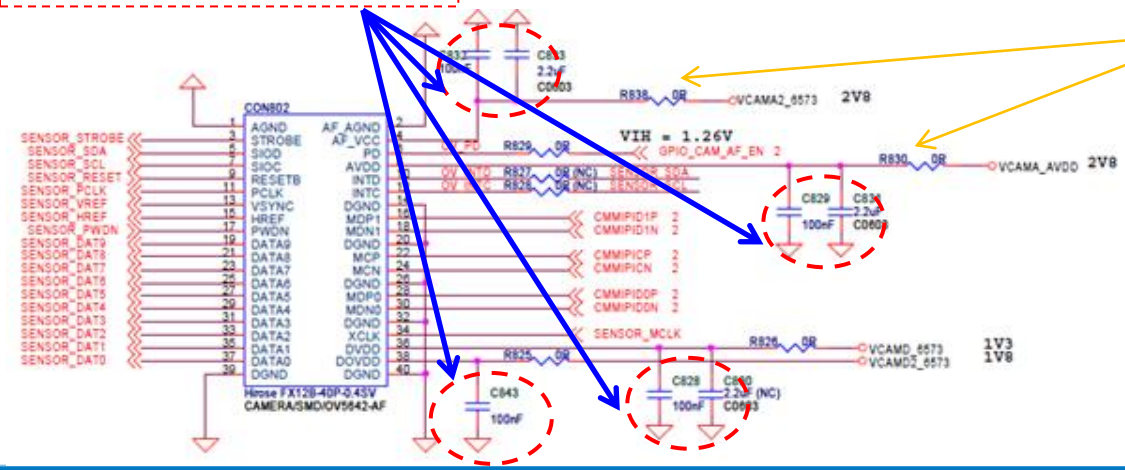
Camera Reference Circuit

LDO output capability

Analog LDO	VTCXO	2.8	10	
	VCAMA	1.5/1.8/2.5/2.8	250	
	VCAMA2	1.5/1.8/2.5/2.8	100	
Digital LDO	VM12	1.2	200	
	VM12_INT	1.2 ~ 1.35	40	
	VIO28	2.8	100	
	VSIM	1.8/3.0	100	
	VUSB	3.3	100	
	VCAMD	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	
	VCAMD2	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	
	VSIM2	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	
	VMC	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	

Must be reserved de-couple caps and placed near by connector

Reserve bead on sensor AVDD and AF_VDD path



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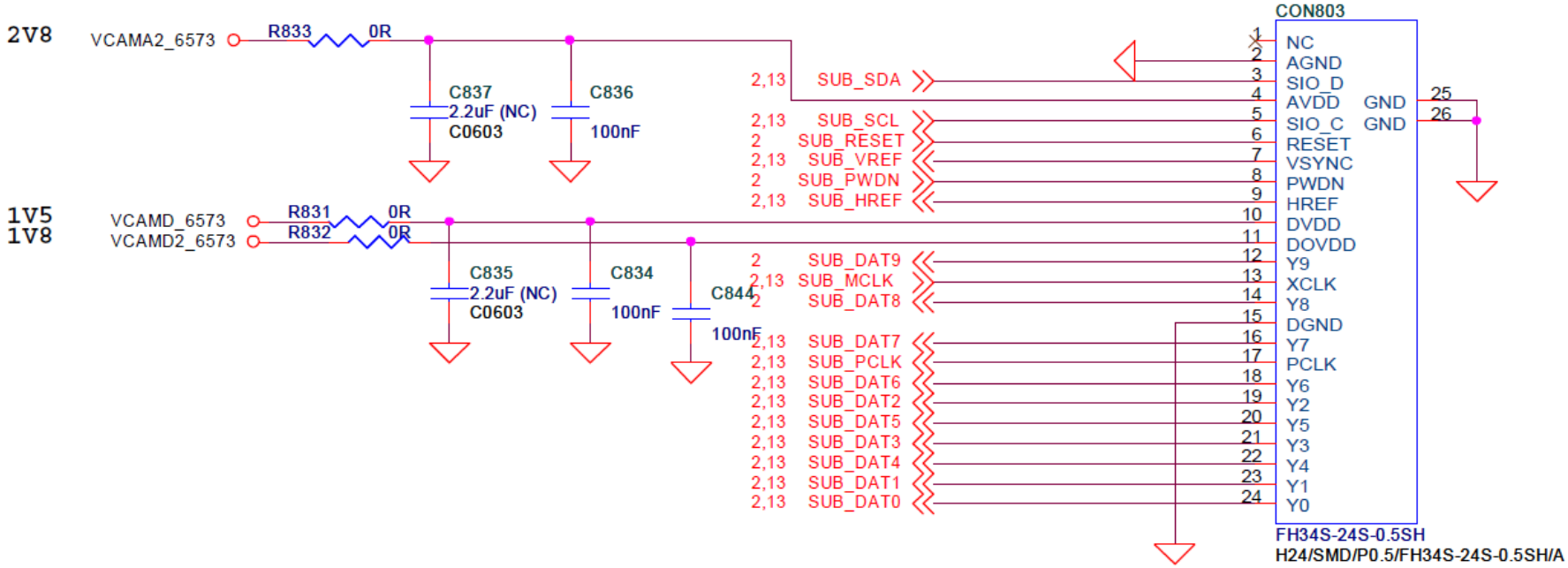
Camera Reference Circuit

Sensor output format is RAW8, please connect sensor output to CMDAT[2:9] . (please confirm with sensor output also)
Sensor output format is RAW10, please connect sensor output to CMDAT[0:9]
Sensor output format is YUV / JPEG, please connect sensor output to CMDAT[2:9]



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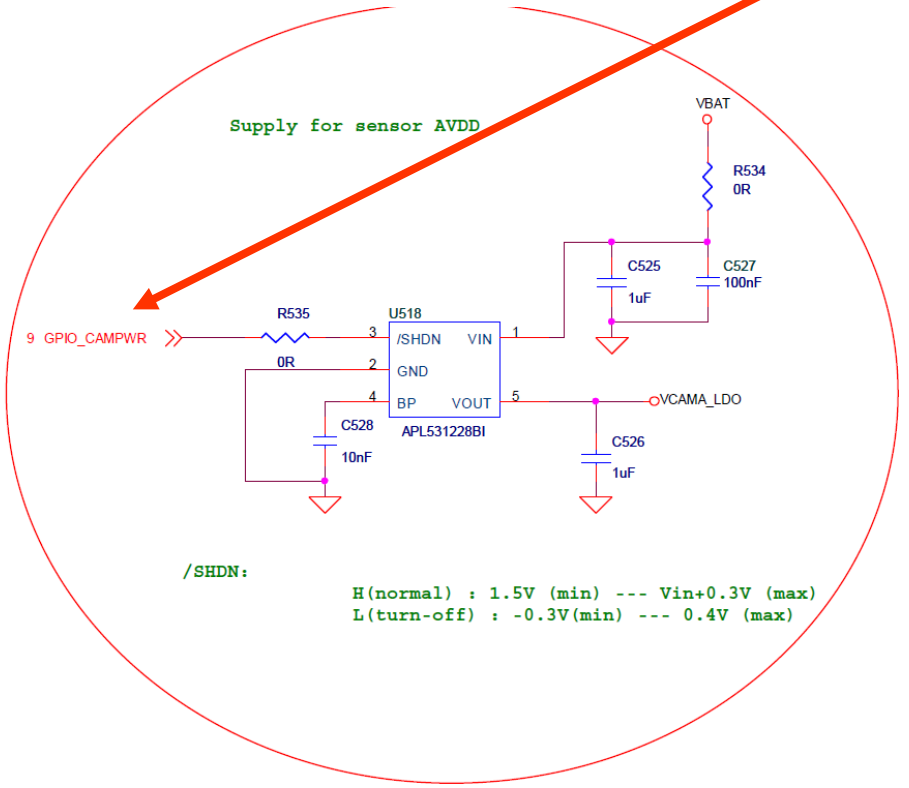
Camera Reference Circuit

[External LDO circuit]



External LDO circuit:

Used GPIO_CAM to control LDO SHDN pin.

Default is Low. (turn-off output)

Sensor power- on sequence:

Normally, the power-on sequence is DOVDD->AVDD->DVDD

Sensor power-off sequence:

The power-off sequence is DVDD -> AVDD-> DOVDD

Don't use VCAMA or VCAMD to instead of GPIO to control LDO SHDN pin.

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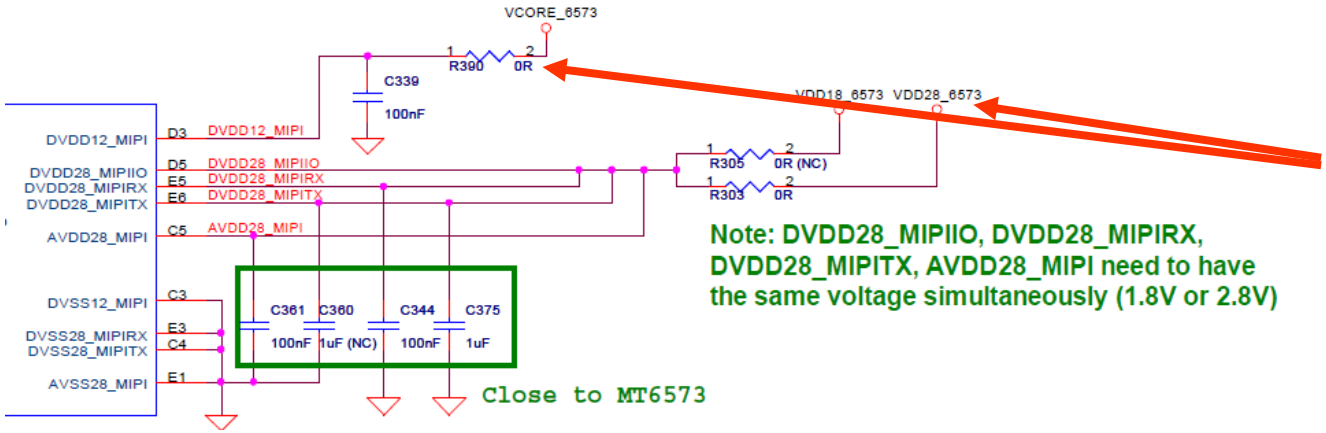
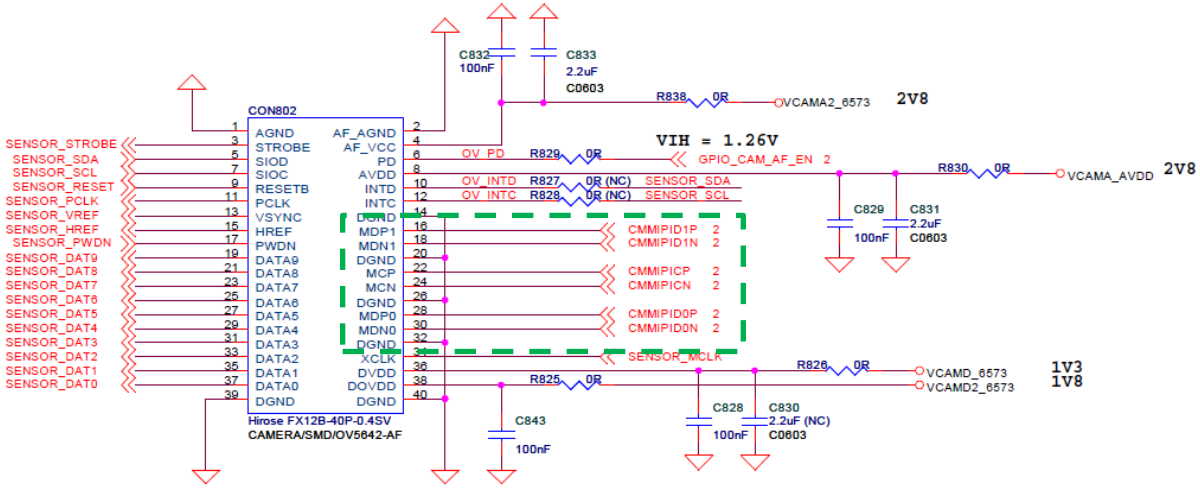
Camera Reference Circuit

[MIPI CSI2 circuit]



MIPI CSI2 I/F:

MIPI disable:
R303->NC, R305->0R
MIPI enable:
R303->0R, R305->NC



MIPI CSI2 trace:

a. 100 ohm differential pair
b. Ground shielding.
3. Routing lengh < 3”

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Camera Reference Circuit

[External LDO: software configuration]

Modified camera_hw.c

Turn-on camera function:
Set GPIO73 to high after VCAMA & VCAMD configure.

Turn-off camera function:
Set GPIO73 to low before VCAMA & VCAMD configure.

Step1:

```
#define MODULE_V2_SPECIAL_POWER                    (73)

#define set_reset_high_main \
        { \
                GPIO_WriteIO(1, MODULE_RESET_PIN_main); \
                GPIO_ModeSetup(MODULE_RESET_PIN_main, 0); \
        }

#define set_reset_Low_main \
        { \
                GPIO_WriteIO(0, MODULE_RESET_PIN_main); \
                GPIO_ModeSetup(MODULE_RESET_PIN_main, 0); \
        }

#define set_reset_high_sub \
        { \
                GPIO_WriteIO(1, MODULE_RESET_PIN_sub); \
                GPIO_ModeSetup(MODULE_RESET_PIN_sub, 0); \
        }

#define set_reset_Low_sub \
        { \
                GPIO_WriteIO(0, MODULE_RESET_PIN_sub); \
                GPIO_ModeSetup(MODULE_RESET_PIN_sub, 0); \
        }

#define set_special_power_high \
        { \
                GPIO_WriteIO(1, MODULE_V2_SPECIAL_POWER); \
                GPIO_ModeSetup(MODULE_V2_SPECIAL_POWER, 0); \
        }

#define set_special_power_low \
        { \
                GPIO_WriteIO(0, MODULE_V2_SPECIAL_POWER); \
                GPIO_ModeSetup(MODULE_V2_SPECIAL_POWER, 0); \
        }
```

Step2:

```
// Compact Image Sensor Module Power ON/OFF
void cis_module_power_on(kal_bool on)
{
  const kal_uint8 camera_id = get_isp_oper_camera_id();

DRV_WriteReg32(0x610D0714 , (DRV_Reg32(0x610D0714)|0x10));
  if(on==KAL_TRUE)
  {
    pmic_adpt2_set_vcamd(PMIC_ADPT_VOLT_1_5); /* DVDD, OV3640 spec: 1.5V */
  pmic_adpt2_vcamd_enable(KAL_TRUE);
    pmic_adpt2_set_vcama(PMIC_ADPT_VOLT_2_8); /* AVDD, OV3640 spec: 2.8V */
  pmic_adpt2_vcama_enable(KAL_TRUE);

set_special_power_high;

    if (CAM_MAIN_CAMERA == camera_id)
    {
      #fdef OV3640_HW_SCCB //hw sccb
                GPIO_ModeSetup(SCCB_SERIAL_CLK_PIN, 1);
                GPIO_ModeSetup(SCCB_SERIAL_DATA_PIN, 1);
      #else//config sw SCCB
                GPIO_ModeSetup(SCCB_SERIAL_CLK_PIN,0);
                GPIO_ModeSetup(SCCB_SERIAL_DATA_PIN,0);
      #endif
```

```
    pmic_adpt2_vcamd_enable(KAL_FALSE);

set_special_power_low;
    pmic_adpt2_vcama_enable(KAL_FALSE); \\ for InfiV5/6/5  fonch board use this power' cenf mu it off
```

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Camera Design Note – Dual Camera

- For dual camera solution, CCM must support HW Reset, Power down function
  - When power down, CCM output could set to high-Z
- Dual camera use independent RESET, PWDN control pin for main/sub sensor switching
  - BB CMPDN, CMRST → Main camera
  - For sub camera, use CAMERA power domain GPIO
- Dual camera share pins of
  - VSYNC
  - HSYNC
  - MCLK
  - PCLK
  - CAMDAT[9:0]
  - I2C
- For 8bit YUV sensor, connect to CMDAT[9:2]
- Layout notice
  - All signal need well shielded by GND plane especially CMMCLK, CMPCLK
  - EMI filter could add close to connector. Be careful that heavy loading for sensor may cause PCLK fail to work.
  - Total bus capacitor loading should be < 30pF

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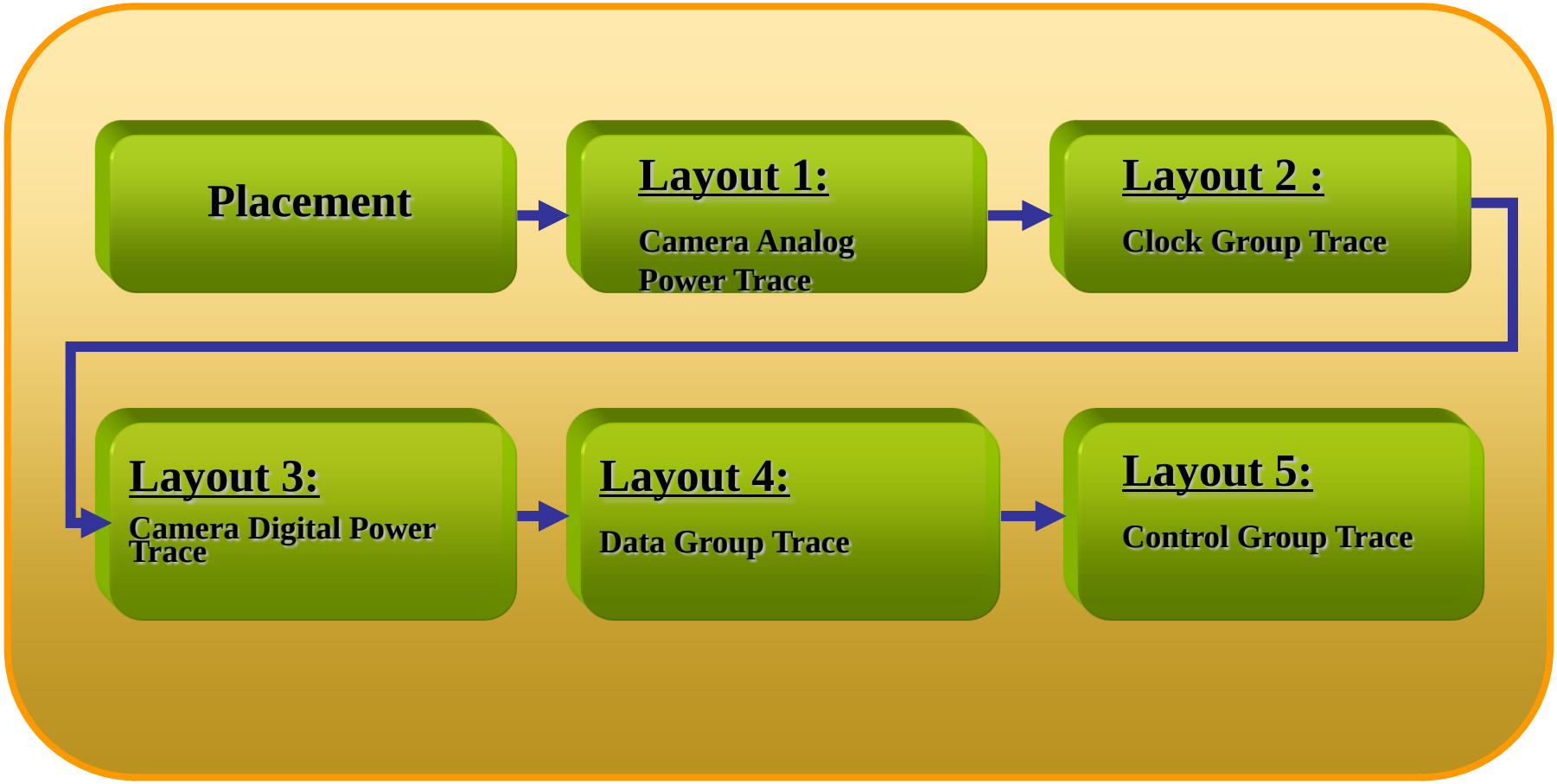
PCB Design Flow



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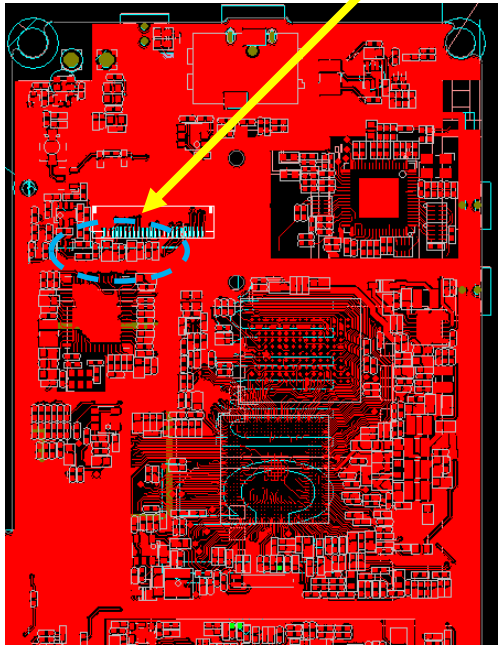
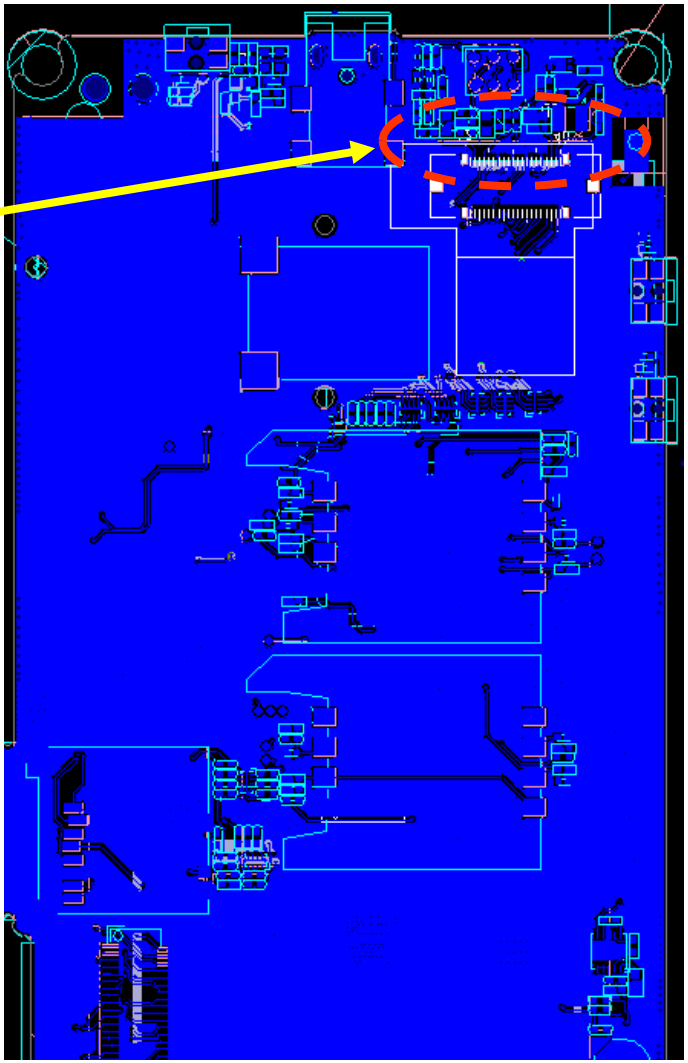
Design Notice – Image Sensor

- **PCB Component Placement recommend :**

➢To minimize RF radiation interference, do not place the sensor module near or beneath the antenna.

➢The sensor module's power supplies(inductors , beads , resistors , capacitors) should be placed as close as possible to the connect





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Design Notice – Camera

- **General Routing recommend :**

➢With minimum trace lengths, route high-speed clock and high-speed data differential pairs first.

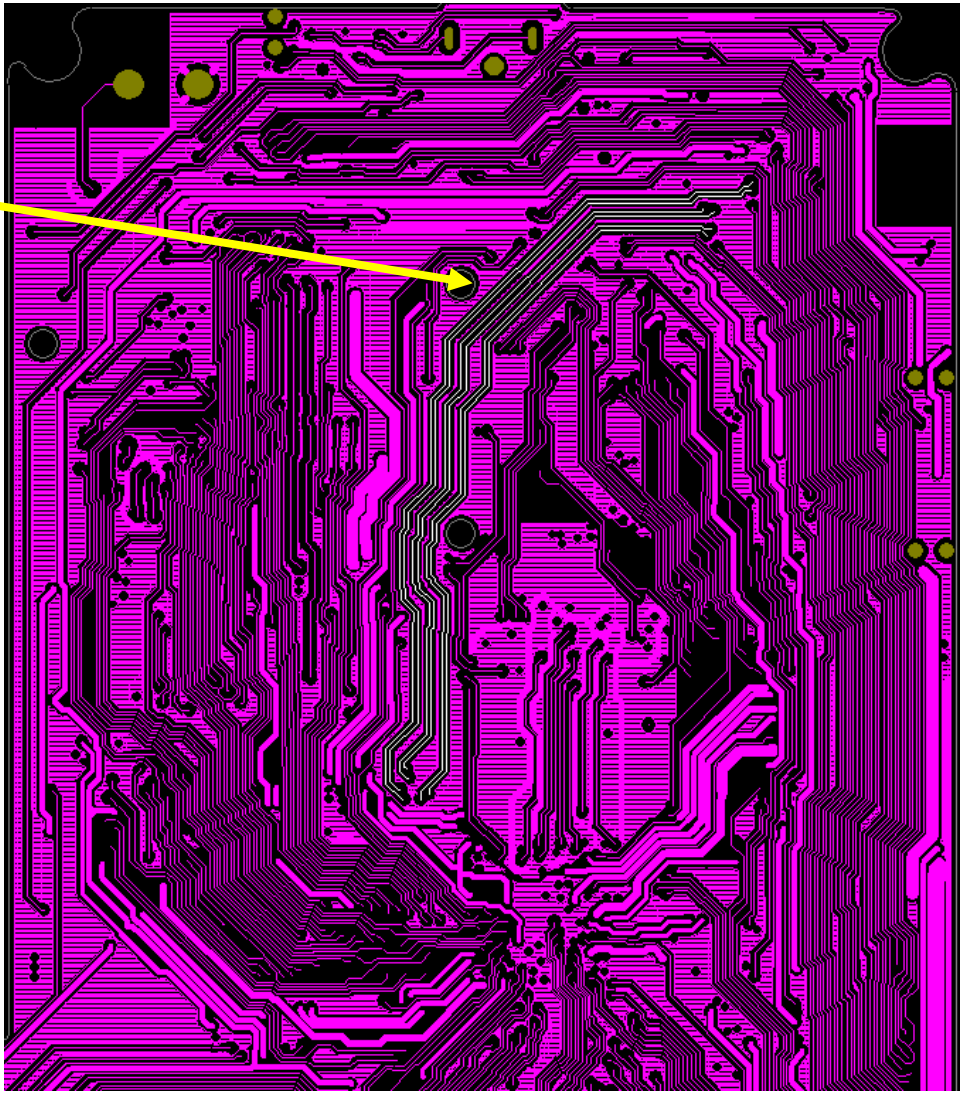
➢Route signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.

➢When it becomes necessary to turn 90˚, use two 45˚ turns or an arc instead of making a single 90˚ turn. This reduces reflections on the signal by minimizing impedance discontinuities.

➢Do not route signal traces under crystals, oscillators, clock synthesizers, magnetic devices.

➢Route all traces over continuous planes

➢Keep all signals clear of the core logic set.



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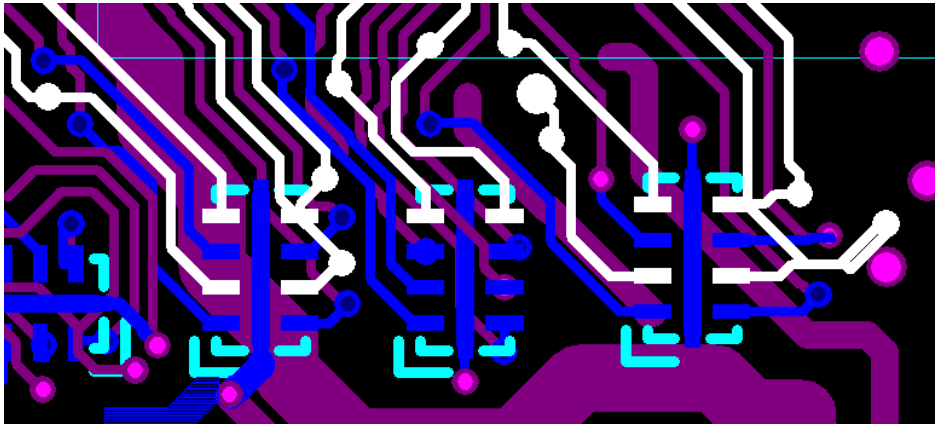
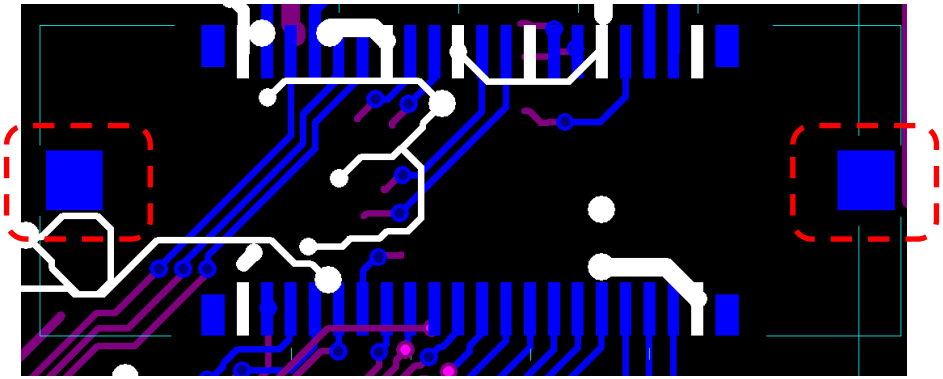
Design Notice – Camera

- **General Routing recommend :**



1.EMIF shall be placed as close as camera connector.

2.Don't routing the trace to cross EMIF input and output. (L1 & L2)



3.Reduce the routing trace on top layer.
4.Don't routing the unrelated signal on L2 pad.
(GND signal is OK)
5.The support pins of module connector must be connect to system GND.

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Design Notice – Camera

- **PCB Layout Design Notice**

This section states the layout recommendations for the MIPI CSI signals. Refer to below tables for the routing guidelines. Multiple vias shall be drilled in the ground guard to minimize the inductance of grounding path.

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
PP material	1080
Main trace patterns and impedance (MIPI-CSI)	**Target impedance: Z_{diff} = 100 Ω ± 15%.** W = 4-mil, S = 7-mil, and Ground Space = 10-mil (GSSG pattern, 20-mil ground guard width).
Maximum length	**MIPI CSI: 3 inches.**
Length matching in PCB	Pair to pair (within one connector): 100 mils.
Remark	Route the differential pair straight and symmetrically on the same layer with equal trace width and space.

Adobe Acrobat Document

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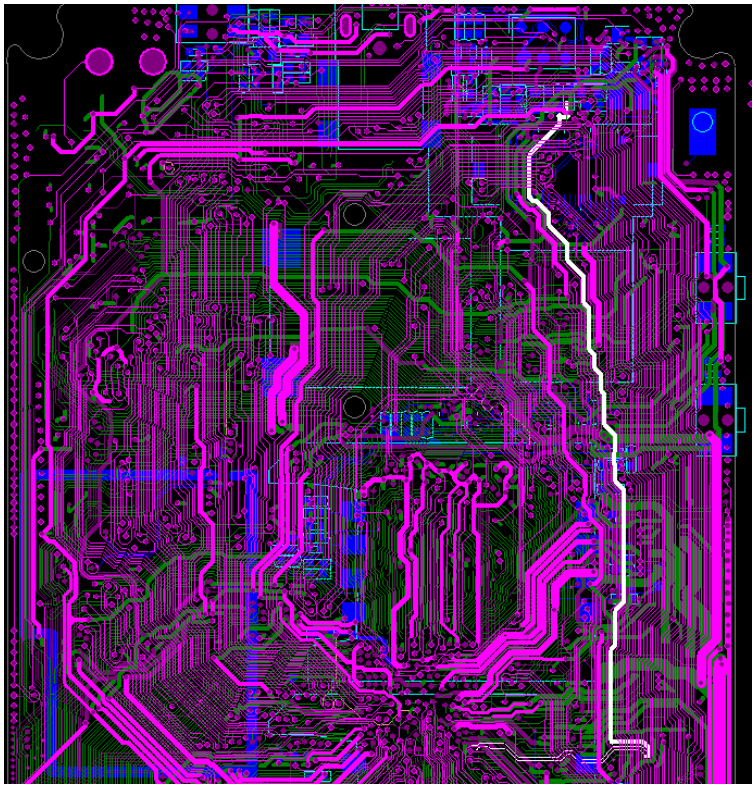
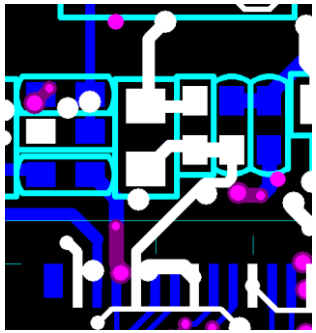
Design Notice – Camera

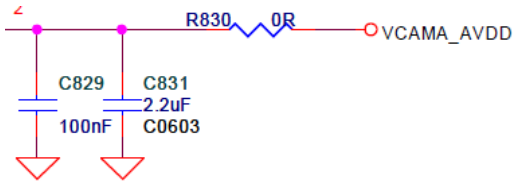
- **Analog Power Routing (Must be!!)**

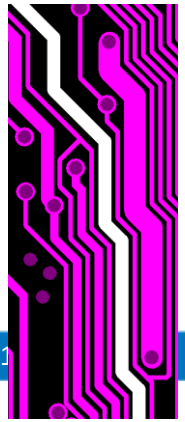
This section states the layout recommendations for the image sensor Analog power routing. Refer to below table for the routing guidelines. Analog Power shall be routed surround with ground plane.

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Analog Power)	W ≥ 12-mil, S = 4-mil with GND trace.
Remark	Analog power must be routed surround with ground plan. De-couple cap shall connect to main ground directly.









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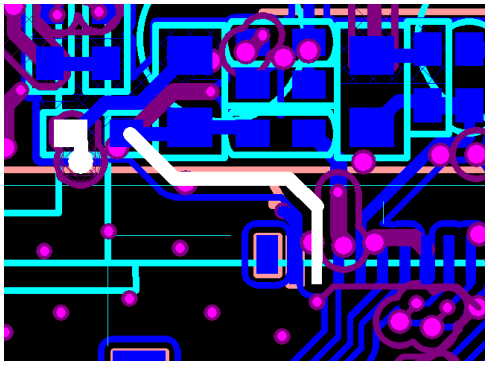
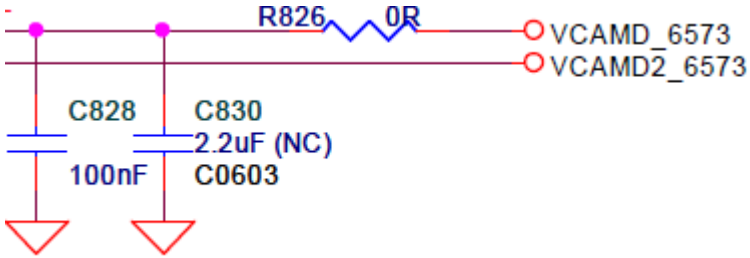
Design Notice – Camera

- **Digital Power Routing** (Must be!!)

This section states the layout recommendations for the image sensor digital power routing. Refer to below table for the routing guidelines. Digital Power shall be routed surround with ground plane.

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Digital Power)	W ≥ 12-mil, S = 4-mil with GND trace.
Remark	Digital power shall be routed surround with ground plan. De-couple cap shall connect to main ground directly.





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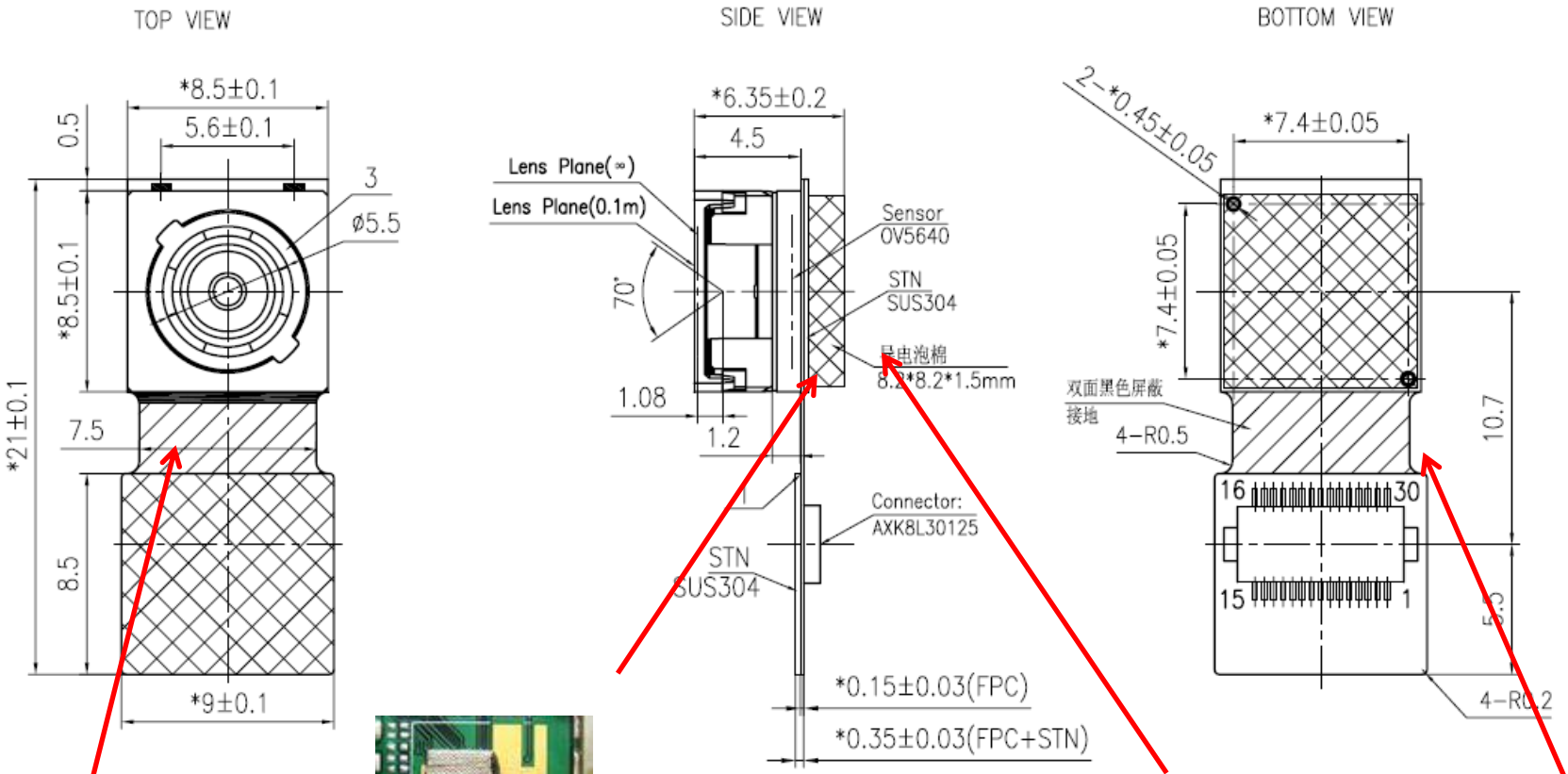
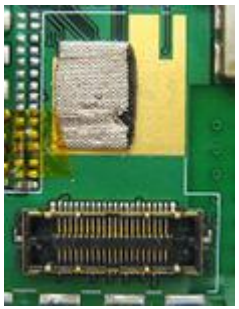
Camera module notice.



Shielding film
Have to connect
module ground.



Open the
soldering mask
for module
conductive

Double-side gummed.
Electric and connect
with module ground.

Shielding film
Have to connect
module ground.

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Confidential B

MT6573 USB Design Notes

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MT6573 USB Port Introduction

	Port 1	Port 2
Spec	USB 2.0 High Speed OTG. 480Mbps.	USB 1.1 Full Speed Host. 12Mbps.
Power	1.2V (share with vcore) and 3.3V (VUSB from PMU)	3.3V (VUSB from PMU) or 1.8V/3V from VSIM
Applications	Firmware Download META Link ADB Mass Storage USB OTG Charger Detection	IC-USB USB Host to ext. Modem (please check with marketing for feature ready date)

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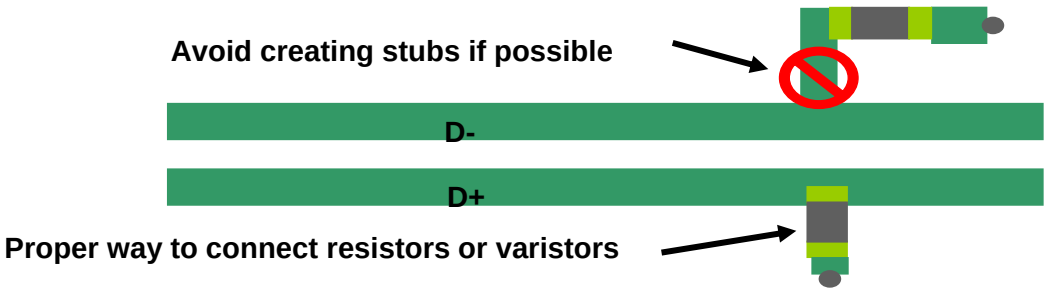
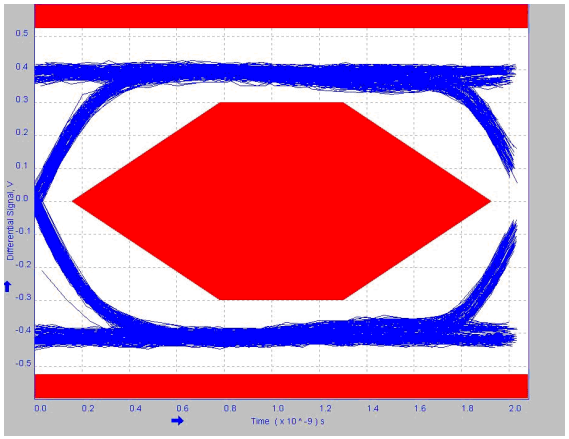
USB 2.0 High Speed General Routing Notice

- Avoid creating unnecessary stubs on data lines, if a stub is unavoidable (for example: ESD issue), please keep the stub as short as possible.



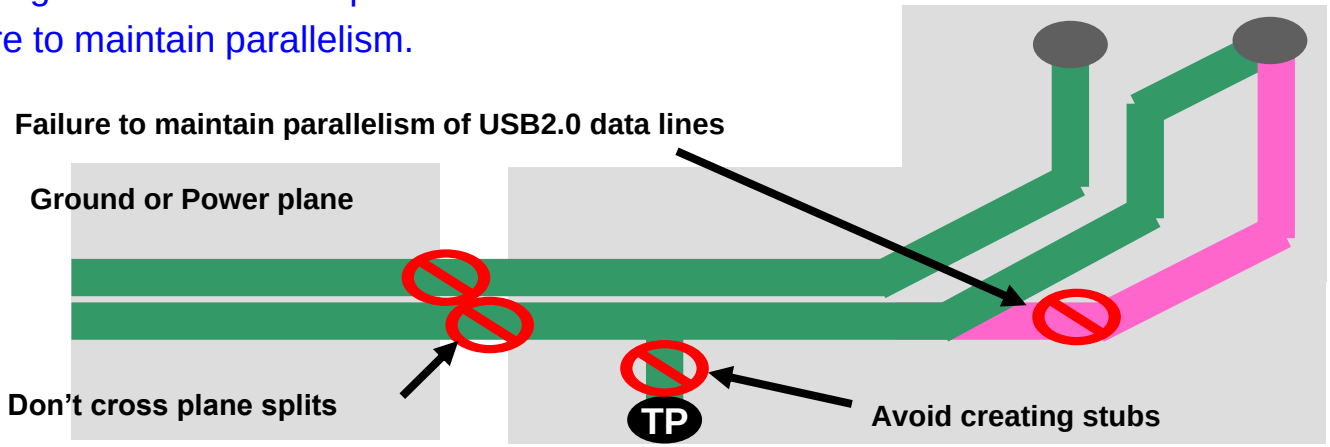


Poor Routing Techniques:

Cross a plane split.

Creating a stub with a test point.

Failure to maintain parallelism.



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Pin Definition

- USB2.0 pin out description.
  - General pins

Ball	Name	Type	Description
T28	AVDD12_USB	Power	1.2V analog power for USB HS PHY. (share with Vcore)
R29	AVDD33_USB	Power	3.3V analog power for USB HS PHY. (from PMU VUSB LDO)
T26	USB_VBUS	Input	USB OTG VBUS detection. Use 2M ohm and 1M ohm to divide 1/3 of USB 5V for VBUS valid detection.
P31	USB_DM	IO	D- for USB port 1. (HS OTG)
P30	USB_DP	IO	D+ for USB port 1. (HS OTG)
T30	USB_ID	Input	USB ID detection. Connect to ground on USB cable for A device.
R25	USB_VRT		USB vbias, put 5.1k ohm (1%) to ground.
M28, T6	DRVVBUS	Output	To control 5V external charge pump on/off for OTG application.
R26	ACDD33_USB11	Power	3.3V analog power for USB FS PHY. (from PMU VUSB LDO)
P28	USB11_DM		D- for USB port 2. (Full Speed Host)
P27	USB11_DP		D+ for USB port 2. (Full Speed Host)

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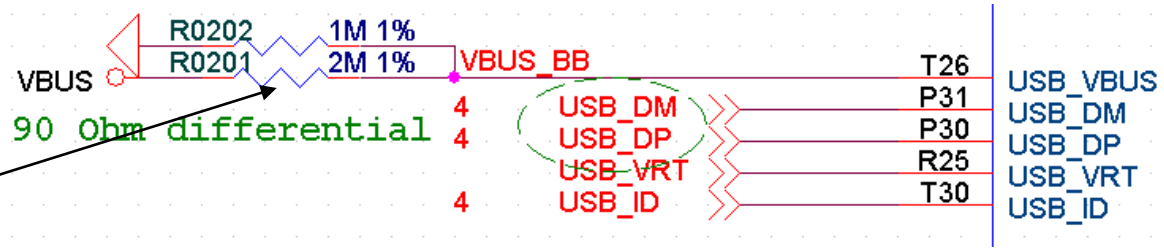
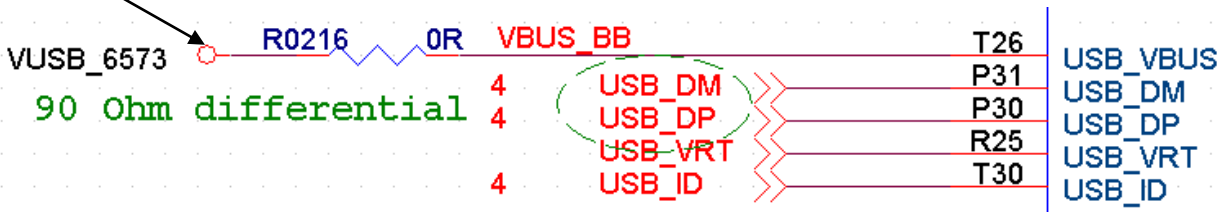
USB Download for OTG Projects

- Don't left USB_VBUS floating even if you are using device mode only! Or USB download may fail to initialize.

●Normal connection, can apply on OTG or device mode. VBUS=5V, beware VBUS can't exceed 10V.



●Device mode only application, for saving external BOM, you can connect VUSB(3.3V) to USB_VBUS to make sure USB can work properly in boot-rom stage.



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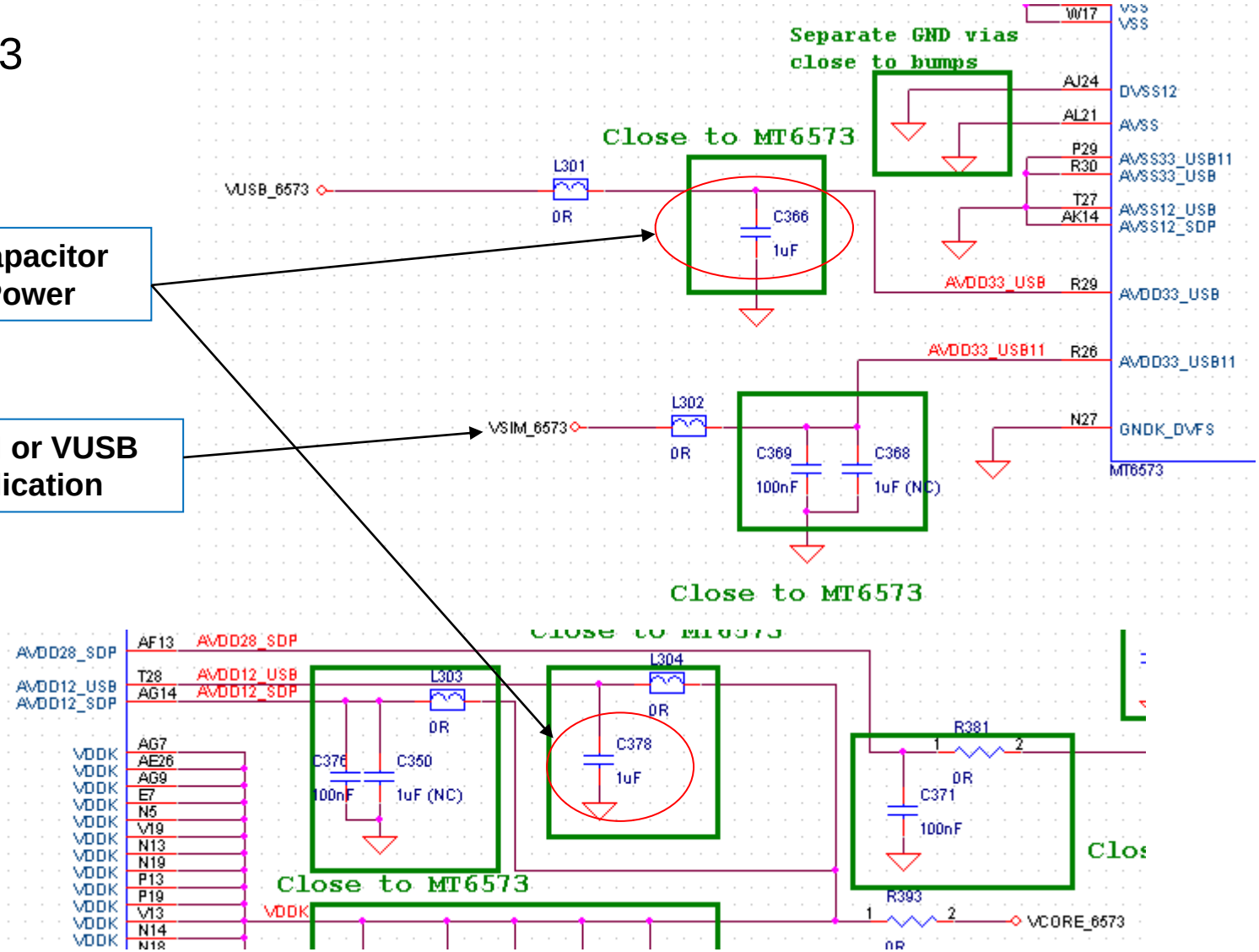
Schematics Design for USB2.0

- MT6573

Reserve bypass capacitor for USB 1.2, 3.3V Power

Connect to VSIM or VUSB depends on application



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Internal Use

MT6573 MSDC Design Notice

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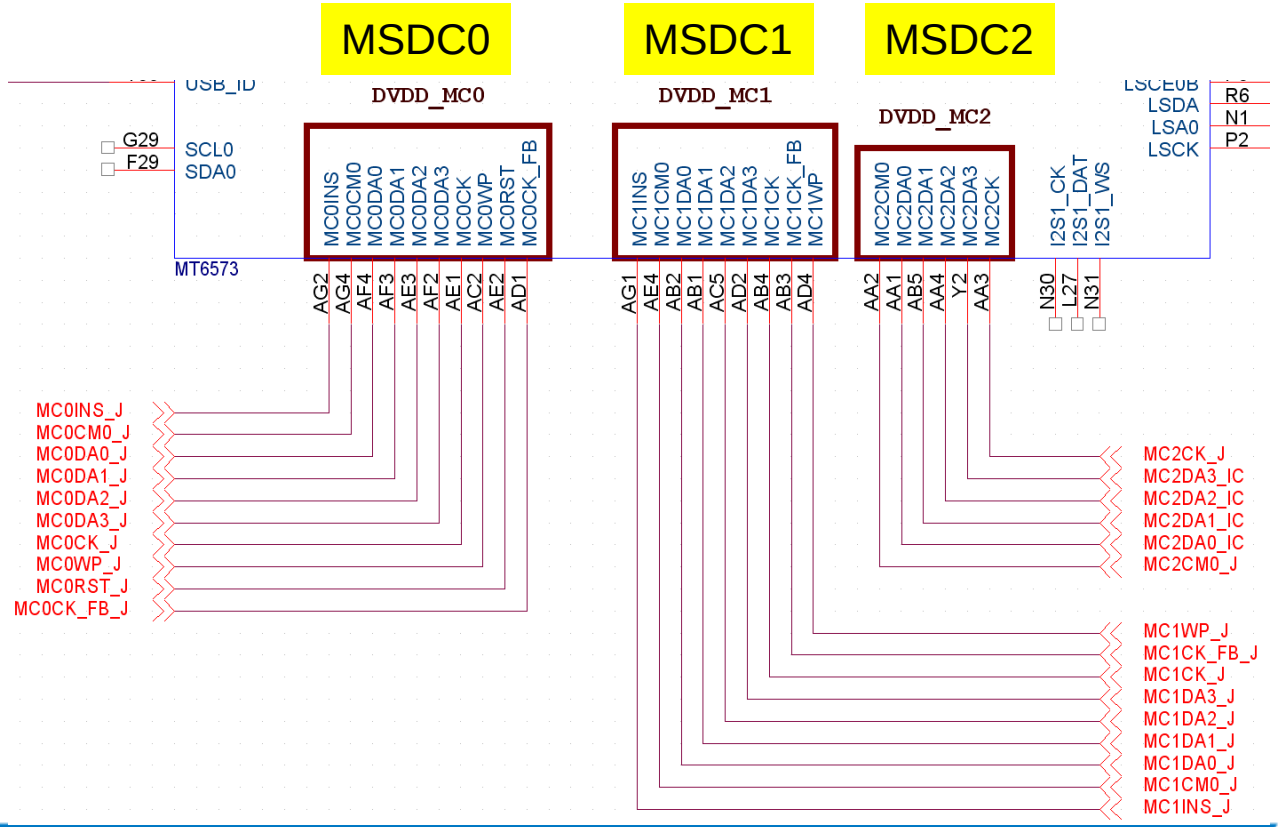
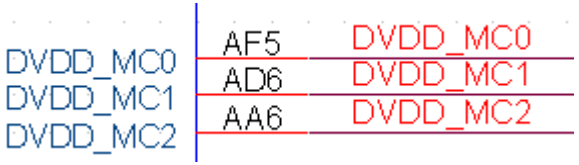
MT6573 MSDC HW Configuration

3 HW MSDC modules in MT6573



MT6573 MSDC Power Configuration



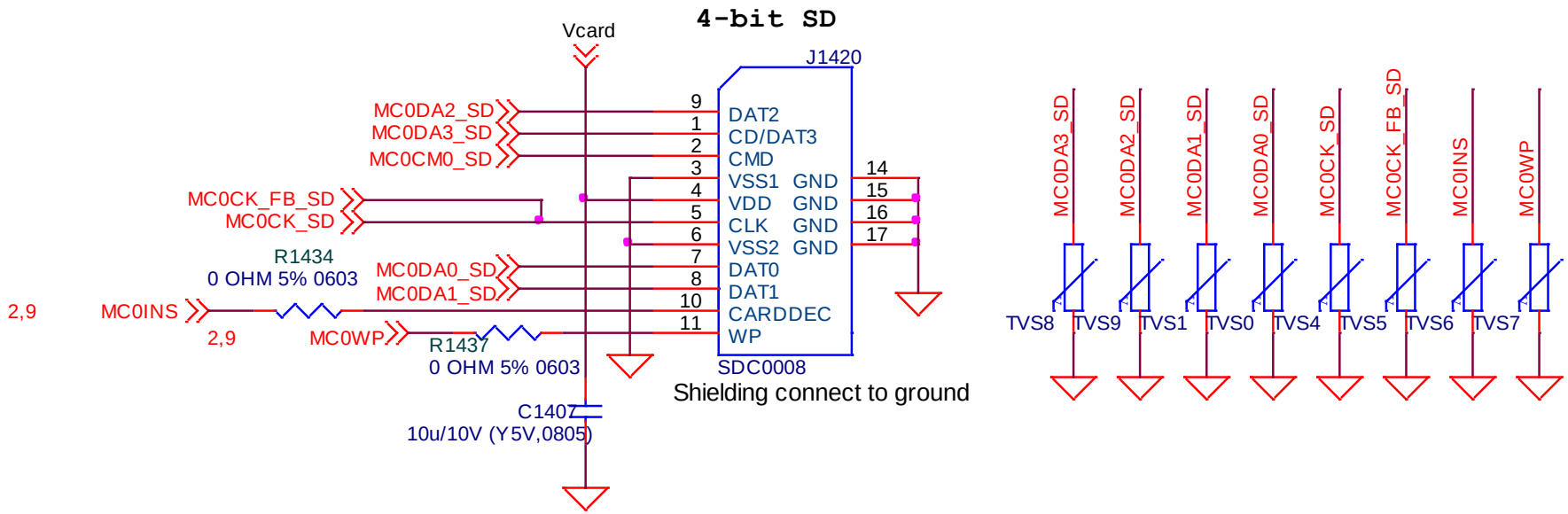
Power for MSDC0/1/2

MT6573 MSDCs Difference

1. PU Resistors
   - There are internal PU resistors for MSDC0/1/2
2. Feedback Clock
   - MSDC0/1: external feedback clock
   - MSDC2: internal feedback clock
3. Suggested MSDC Utilization Priority
   - MSDC0/1 > MSDC2

Example Circuit for SD Card

1. Add ESD protection device on CMD/CLK/DAT/MCINS/MCWP with Cap < 15pF
2. Provide 3.3V to Vcard and MT6573 related module
   - DVDD_MC0/1/2
3. Current supply requirement to SD card application: >= 200mA



MT6573 eMMC Application Note

- Only MSDC0 supports eMMC boot (HW reset pin)
- Only MSDC0/1 have dedicated MCINS pin for hot plug
- eMMC 8-bit mode is not supported
  - 8-bit mode performance is same as 4-bit mode (internal buffer sync limitation)
- MT6620 is suggested to use MSDC1 (FB_CLK)

	Application	MSDC0	MSDC1	MSDC2	Note
1	T-Flash x 1 + MT6620	T-Flash	MT6620	x	
2	T-Flash x 1 + MT6620 + eMMC	eMMC	MT6620	T-Flash	1. support eMMC boot 2. T-Flash can use EINT as MCINS
3	T-Flash x 2 + MT6620	T-Flash	MT6620	2nd T-Flash	2nd T-Flash can use EINT as MCINS

MT6573 eMMC & T-Flash Power Requirement

200mA, 3.3V is required for each T-Flash and eMMC

- MT6573 VMC LDO (default on, 3.3V, 200mA max) is suggested for eMMC boot
- If eMMC and T-Flash are both used, need one external LDO for T-Flash card
- eMMC VCC & VCCQ are connected together to 3.3V
- For extra large capacity eMMC, more current may be required

ex, Samsung eMMC 4.41 consumes

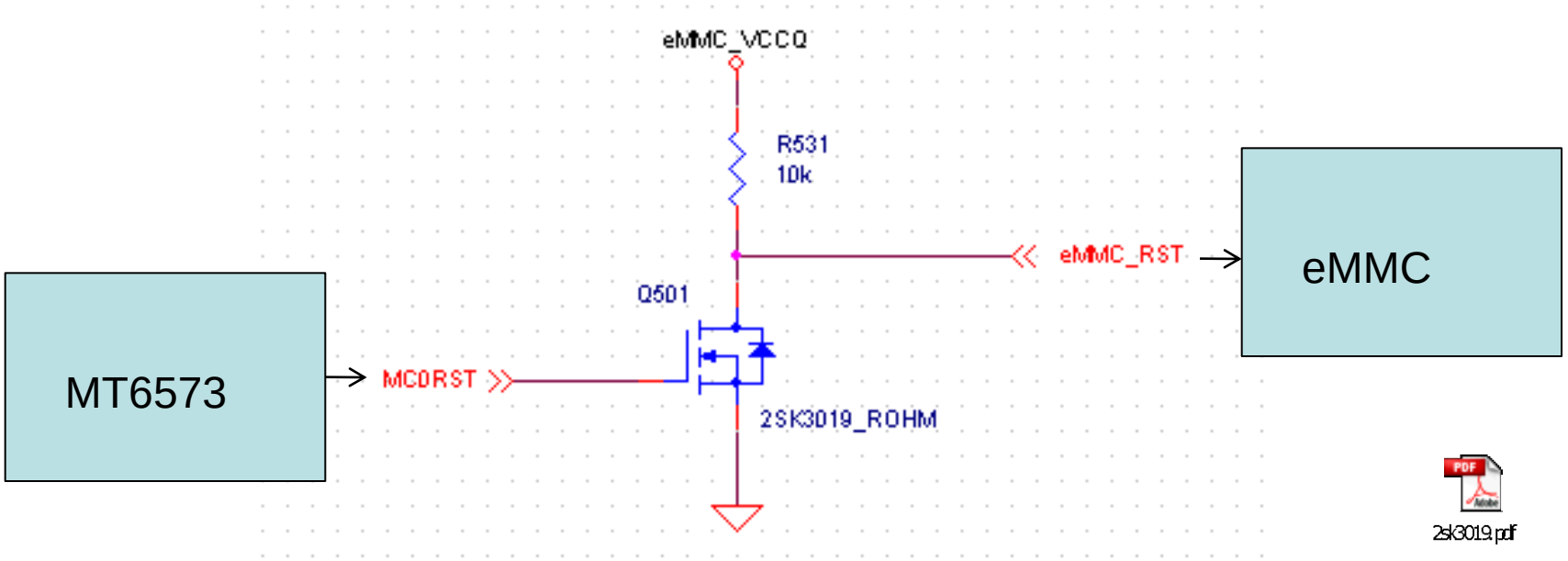
- 50mA for each NAND die
- 100mA for eMMC controller

If Samsung16GB eMMC is used (4GB/die), 50mA x 4 + 100mA = 300mA is required

Vendor	Capacity	Part No.	Current Consumption
SanDisk	4 8	SDIN5C1-4G SDIN5C1-8G	200mA RMS
Micron	4	MTFC4GBMREK-IT	4/8 GB, Typical current consumption - Standby current: 70µA - Active current (RMS): 70mA
Samsung	4	KLM4G1FE3A-A001	4GB NAND: 50mA, 4 dies max. controller: 100mA
Hynix	4	H26M31001FPR (26nm)	4/8/16/32GB <= 200mA
	8	H26M42001FMR (26nm)	4/8/16/32GB <= 200mA

Add NMOS and Pull-up Resistor for MC0RST

- Add a NMOS and pullup resistor between MT6573 MC0RST and eMMC RST



2sk3019.pdf

- 2SK3019 NMOS, or other similar parts is also fine for this

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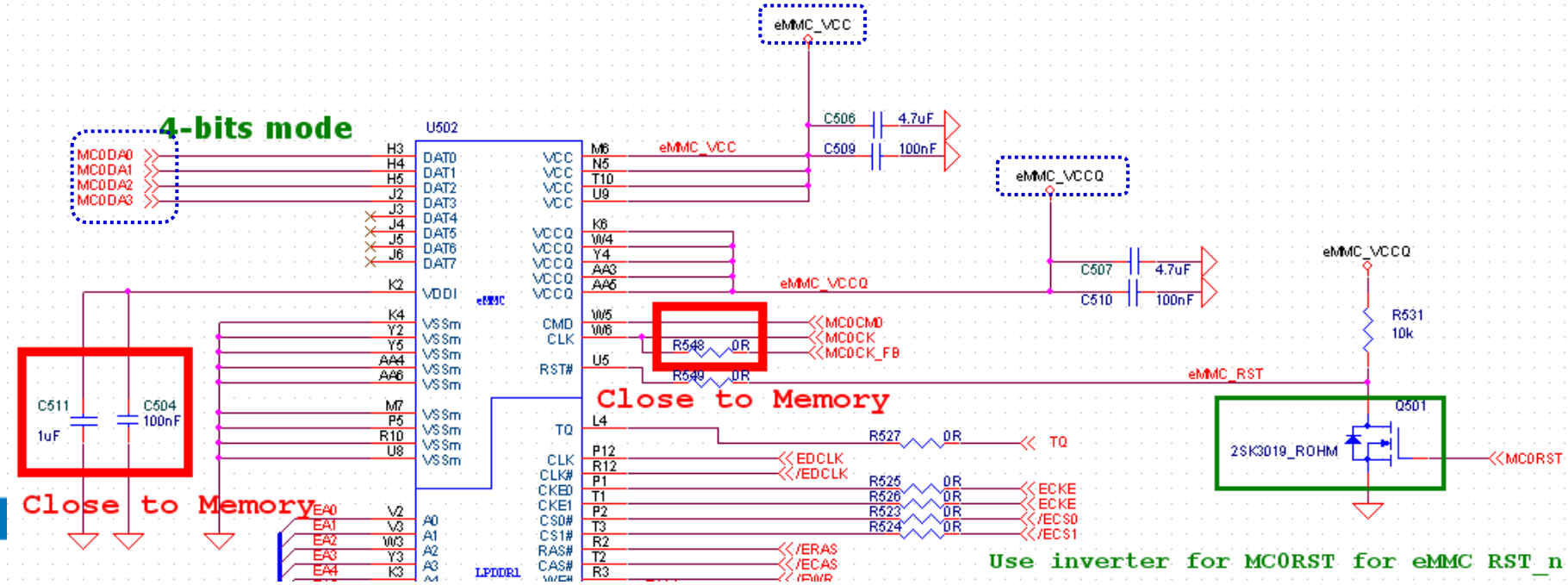
MT6573 eMMC Application Circuit

- eMMC 4-bit mode is preferred
- MT6573 VMC LDO (default on, 3.3V, 200mA max) is suggested for eMMC boot
- eMMC VCC & VCCQ are connected together to 3.3V
- Check eMMC spec for VDDi cap
- Add one NMOS & 10K ohm PU resistor

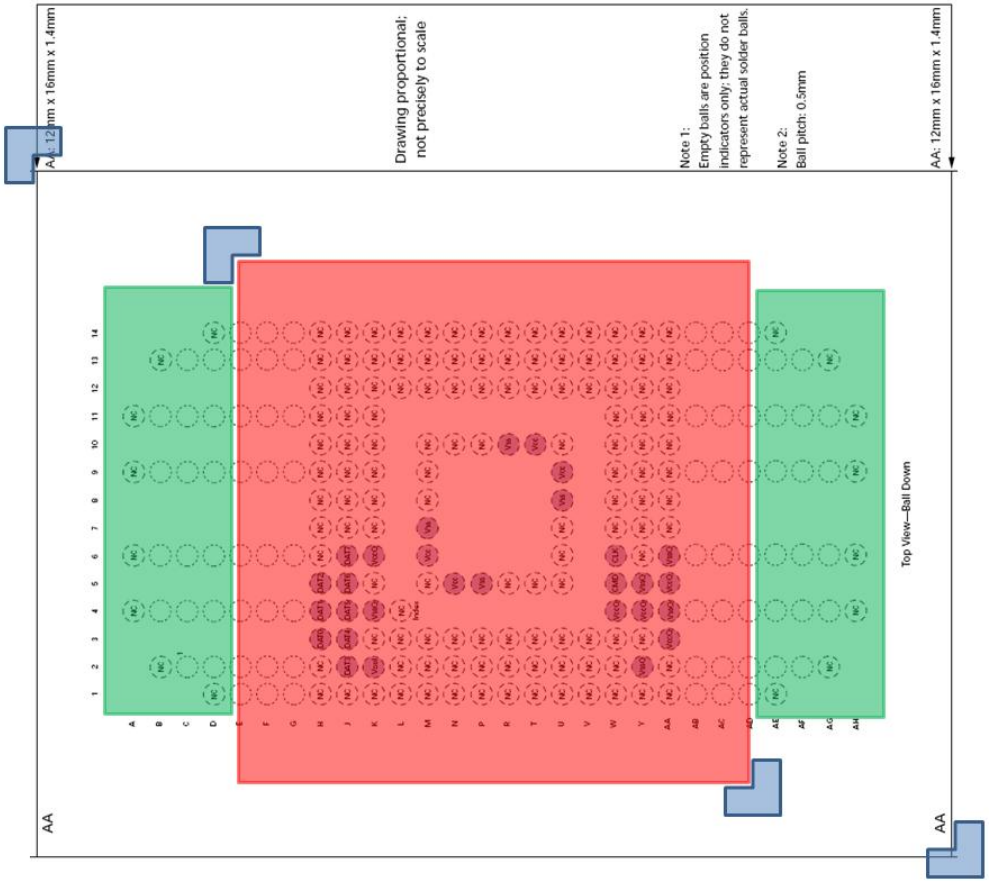


Layout Guidelines

1. DAT, CMD, CLK in a group
2. If this criteria can not be followed，the priority is ((DAT + CLK_FB) + CMD/CLK)
3. Both CLK and CLK_FB must be grounded in both sides to reduce interference
4. CLK_FB start point must be as close to device as possible (T-card socket or eMMC chip)
5. Keep total trace length < 150mm
6. Keep trace difference of DAT, CMD, CLK, CLK_FB to be < 500mil

eMMC 153b & 169b Package Compability

- Suggest to use 169b layout footprint
  - 153b can be put on 169b



Internal Use

Touch Panel
Hardware Application Note

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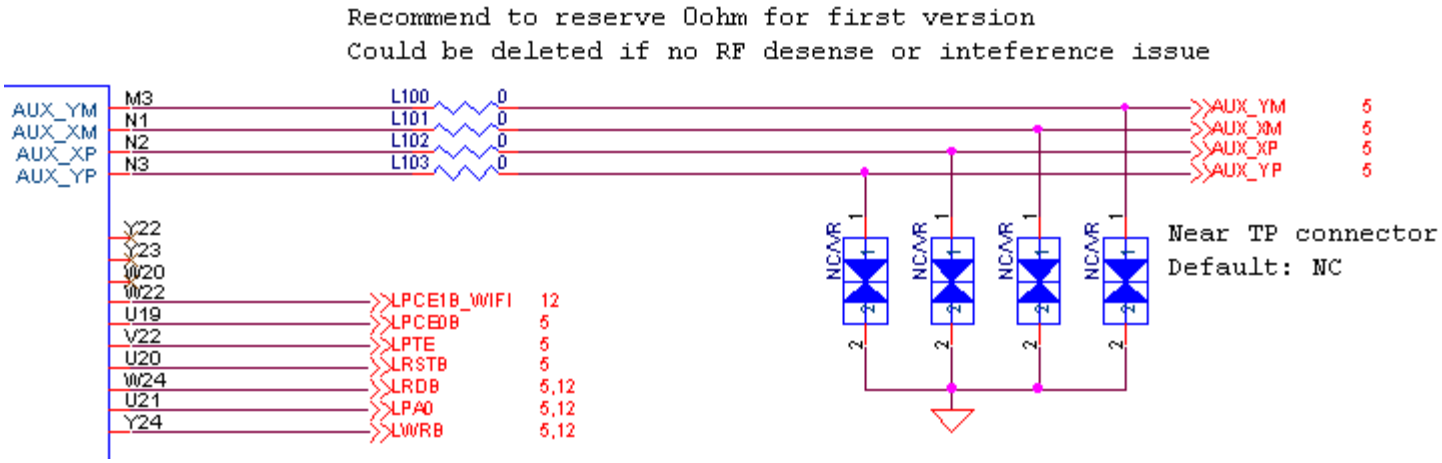
Design Notice – Resistive Touch Panel Hardware Connection

- Recommend to reserve 0ohm and varistors in the first version.
- For RF desense issue, replace 0ohm with adequate beads.
- For ESD issue, mount adequate varistors.
- Otherwise, these components can be removed in later versions to save BOM cost.

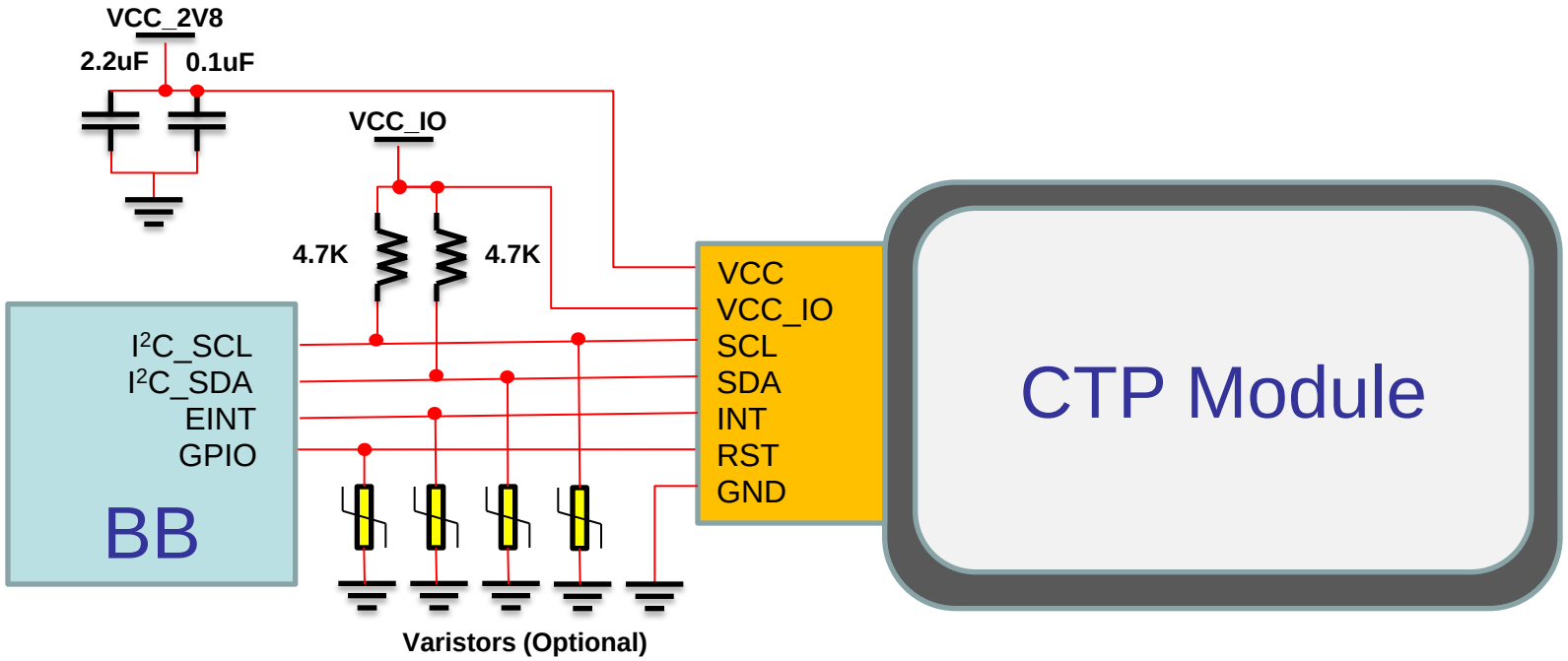


Design Notice – Resistive Touch Panel Suggested Requirements for Sensor

- For better user experience for using resistive touch panel (RTP) on smart phone, we recommend to use the sensor which satisfies the following specifications:
  - Activation force: <35g
    - Lower activation force gives better user experience on manipulating smart phone UI with finger.
  - Terminal resistance: 200ohm~700ohm (as small as possible)
    - Larger resistance will cause longer measurement time and may degrade touch response
  - Chattering time: <10ms
    - Longer chattering time may degrade touch response
  - Linearity: <1.5%
    - Larger value may degrade line smoothness and point accuracy

Design Notice – Capacitive Touch Panel Hardware Connection

- Only capacitive touch panel (CTP) with I²C I/F is supported.
- The CTP shall be compatible with 1.8V I/O and 2.8V analog power
- MT6573 I2C is recommended to connect CTP and its clock stretch function shall be enabled.



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Design Notice – Capacitive Touch Panel Suggested Requirements for Module

- **CTP module which fulfills the following requirements is recommended:**
  - Mutual-capacitance type controller
    - For better recognition of multi-touch gestures supported by Android
  - SITO or DITO glass sensor
    - Glass sensor is typically more stable and reliable than film sensor over wide temperature range.
  - COF design
    - CTP controller is mounted on FPC in order to avoid RF or other noise on PCB coupling to sensing channels
  - 1.8V I/O power (include I^2C) and 2.8V analog power shall be supported by the controller
  - In-situ firmware update via I^2C is recommended
  - The operating clock frequency and scanning frequency are adjustable:
    - It will need to do frequency hopping in case CTP interferes with FM, ATV or other wireless components.

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Notices – System Design

- If CTP cannot use HW I^2C due to power domain issue (shared with camera module), using GPIO to simulate SW I^2C is recommended.
- **Extra LDO with enable signal is suggested to supply the power of the controller** if it is necessary to cut off its power for max power saving when phone is in sleep mode.
- Most CTP controllers are easily interfered by RF signals. It is recommended to **put CTP controllers away from RF antenna area** and use **EMI shielded FPC** for cable connection.
- The driving signal from CTP controller is typically around 1MHz. The harmonics (less than 200MHz) may affect some channels of FM and ATV. It is recommended to **put FM and ATV components and antenna away from CTP panel and its controller**. Or ask controller vendor to reduce driving strength if FM/ATV are desensed by CTP.
- In case that CTP interferes with FM or ATV, it is necessary to implement **frequency hopping (FH)** to move noise away from the interested channel. Thus, the CTP controller must have the capability of changing its operating clock frequency and scanning frequency. The TP driver shall control FH accordingly.

Notices – Touch Performance

- Touch performance can be defined as three main factors. The major parameters of CTP module affected the three factors are listed below:

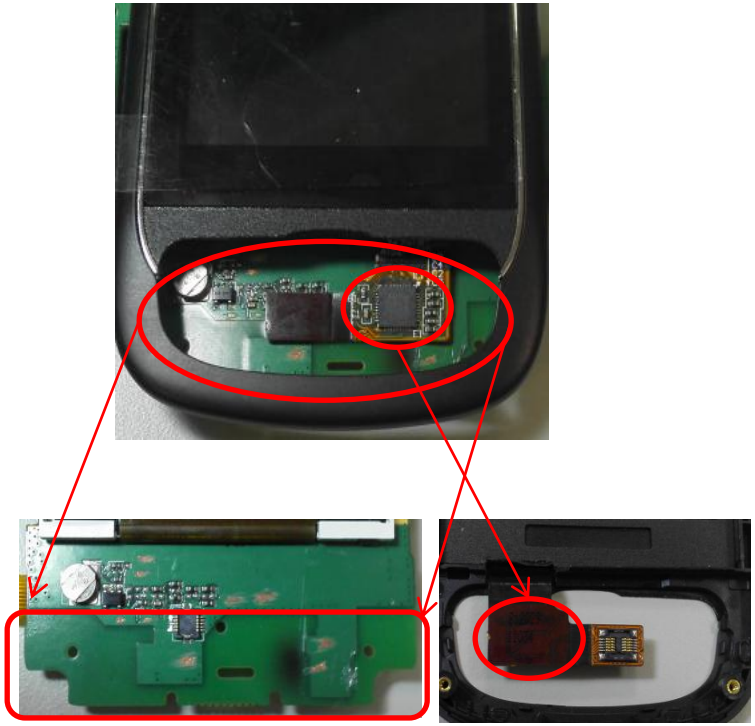
Factors	Major Parameters	What is affected?
Response	Report rate	Lower report rate will report few points which causes curve polygonal if draw it fast and may miss points if quick tapping.
	Latency of first touch from low power state	Larger latency may cause TP failing to sense the first touch when TP is in idle or sleep mode.
Accuracy	Sensor pattern	Diamond pattern is common but have average accuracy. Some controller vendors have proprietary sensor pattern for better accuracy.
	Sensor pitch	Smaller sensor pitch will have better accuracy and narrow finger separation distance. However, more sensor channels and larger boarder area are necessary for smaller pitch. 5mm is common in use for finger touch. The theoretical minimum distance between two fingers will 2.5x sensor pitch, i.e. 12.5mm.
	SNR	Some controllers have higher SNR. It helps to combat strong noise and sense smaller touch area to have better touch accuracy. Mutual-cap is generally have better SNR.
Power consumption	Active current	Mutual-cap controller usually has larger power consumption in active mode (20~40mw) due to much more sensor nodes than self-cap (10~15mW).
	Sleep/Idle current	Some controllers can have low power state or idle state which still perform touch sense but at lower speed to reduce power consumption.

Notices – Selection of CTP Controller

- **CTP is sensitive to common mode noise from AC charger**. It is recommended to use **AC charger which complies with national regulation** for phone charger and **use CTP controller which can combat noise from AC charger**.
- It is necessary to check if the controller will deactivate I^2C bus once its power is cut-off. If it is the case, other devices on the same I^2C bus cannot communicate with host.
- In general, self-capacitance-sensing CTP controller can only report two coordinates simultaneously, lower SNR and has ghost point issue. We suggest to **use mutual-capacitance-sensing CTP controller** for higher SNR, better accuracy and true multi-finger touch.
- MTK can provide **HW/SW requirements of CTP controller and recommended module test specification for CTP module**. The major parameters of CTP controllers are defined in the requirements and the test methods to verify the module test are also proposed. Customer can request module maker to produce module based on these documents to ensure quality and performance. Please consult MTK contact window to apply for these documents.

Case Study – RF Interferes CTP due to Bad Placement

- Issue:
  - CTP outputs random touch points while RF TX power is emitted (during establish phone call or search network etc.)
- Root cause:
  - CTP controller is placed in the RF antenna area. Strong RF noise couples to CTP sensing signals and power to cause false touch signal.
- Solution:
  - Place CTP controller as away from RF antenna as possible. If RF antenna is at bottom. It is recommended to put CTP controller on the top.
  - Shield CTP signal with metal film on FPC
  - Use the controllers which have better immunity to RF noise.

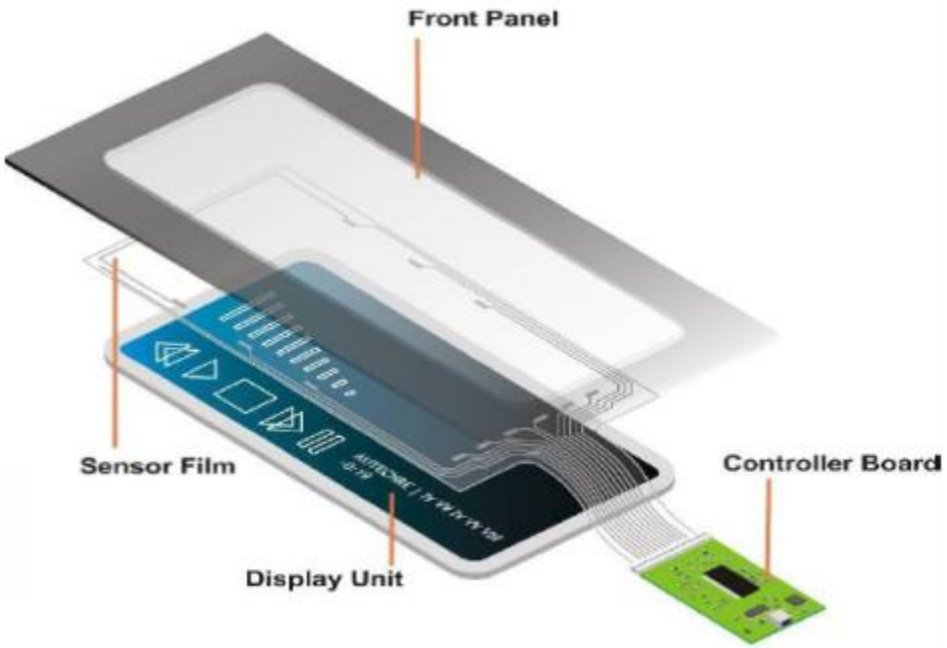


RF antenna area

CTP signals are not well shielded on the bottom side

Introduction of Capacitive Touch Panel

- A CTP module is consist of
  - Cover lens
  - Glass or film sensor
  - CTP controller



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Types of CTP Controller

- Two types of CTP controller:
  - **Self capacitance:** measure self capacitance change on each sensing line
  - **Mutual capacitance:** measure mutual capacitance change between driving lines and sensing line

	Self capacitance	**Mutual capacitance**
Performance	Good	Excellent
Scan rate	Fast	Average
Power consumption	Low	Average
Multi-touch capability	Yes, but can only support two-finger touch with ghost point issue	Yes, may support 2~10 fingers.
Chip Cost	Average (<$2)	High (>$2)

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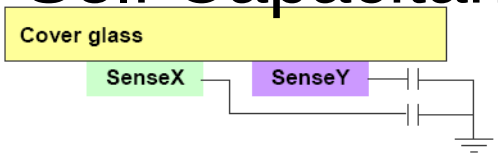
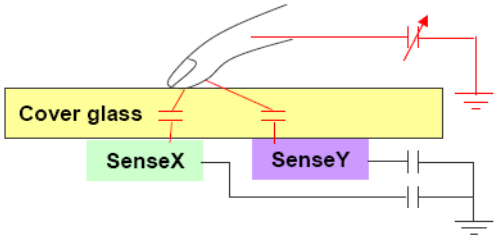
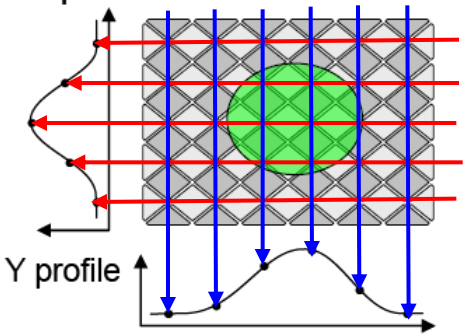
Comparison of Controller

Self Capacitance

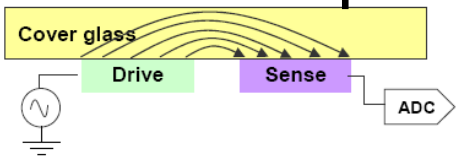


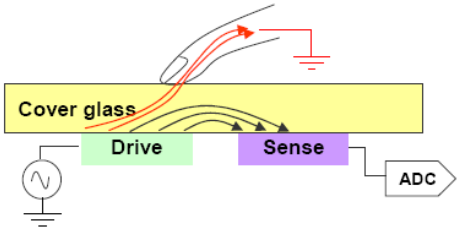


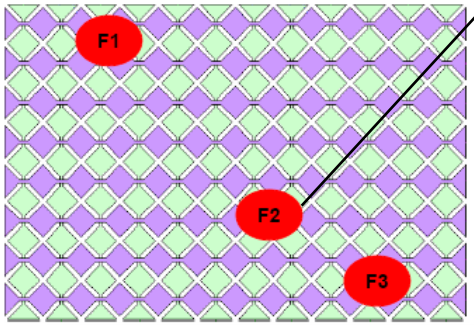
- 2 sets of traces: X-axis, Y-axis
- Finger location computed by curve fitting capacitance profiles for X and Y axes

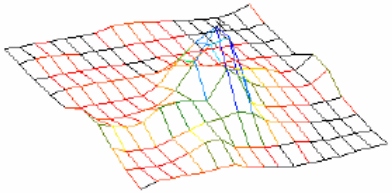


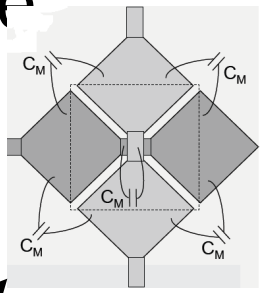
Mutual Capacitance

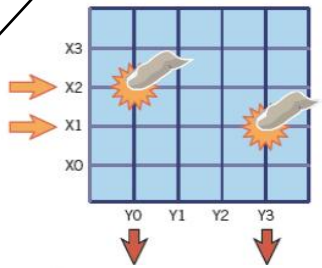










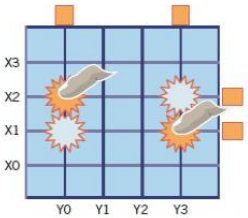


Result:
X2 * Y0 = 1
X1 * Y3 = 1

Conclusion:
X2,Y0 = 1
X1,Y3 = 1

4 * 4 = 16 sensors

Ghost points issue



Result:
X3 & X0 = 0
X2 & X1 = 1
Y0 & Y3 = 1
Y1 & Y2 = 0

Conclusion:
X2,Y0 = 1
X2,Y3 = 1
X1,Y0 = 1
X1,Y3 = 1

4 + 4 = 8 sensors

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CTP Sensor Structure

Cover Lens with print (C.G.)
Optical Adhesive (PSA)
Dual sides ITO Glass (ITO-G)

DITO (Double-sided ITO) G/G

CG
PSA
Dual layer ITO Glass

SITO (Single-sided ITO) G/G

CG
Film on PET
Film on PET

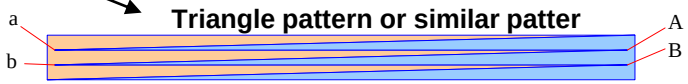
G/F/F

CG
Dual layer ITO Glass
Preservation Film

Single Glass

CG
Single layer on Glass/Film

Single-layer



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Comparison Between Sensor Types

△ Average
○ Good
◎ Excellent

	DITO	SITO	G/F/F	SG	SL G/F
Transparency	○~◎	○	△	◎	◎/○
ITO resistance	◎	◎	△	◎	◎/△
Pattern rule	◎	◎	△	◎	◎/△
Thinness	△	△	○~◎	◎	◎
Weight	△	△	○	◎	◎
Impact endurance	○	○	◎	△	△/◎
Touch performance	◎	◎	○~◎	◎	△
Yield rate	△	○	△	◎	◎
Maturity	◎	◎	◎	△	△
Cost	△	○	○~◎	○~◎	◎
Major Drawback	yield rate, cost, weight	cost, weight	transparency, boarder area	fragile, limit on hole/logo	touch accuracy

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Ambient Light & Proximity Sensor Design Notice

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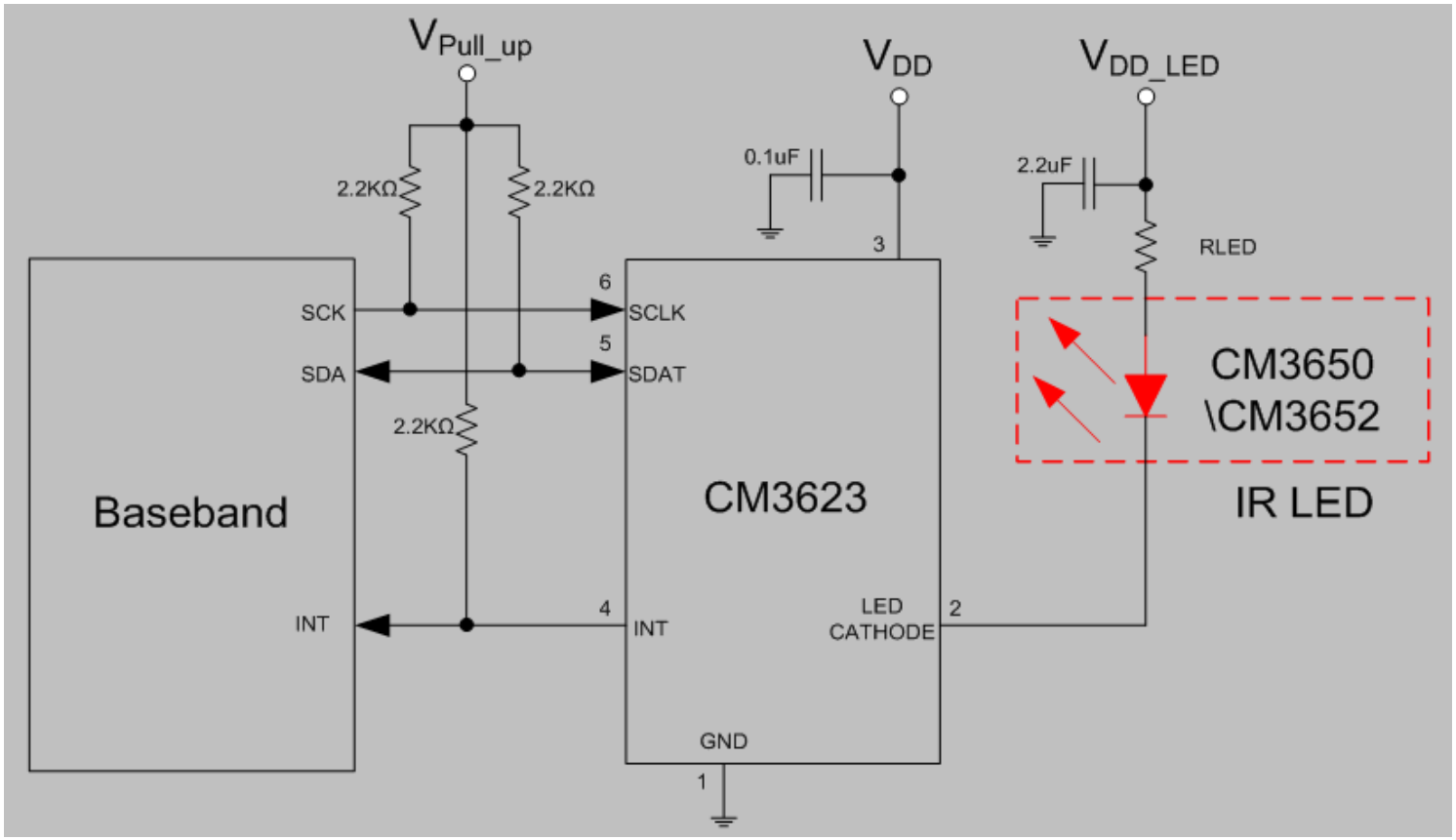
HW Connection Suggestion

- Vdd: 2.5~3.6V
- Vpull_up: 1.8~3.3V
- RLED & Vdd_led: refer to p.12



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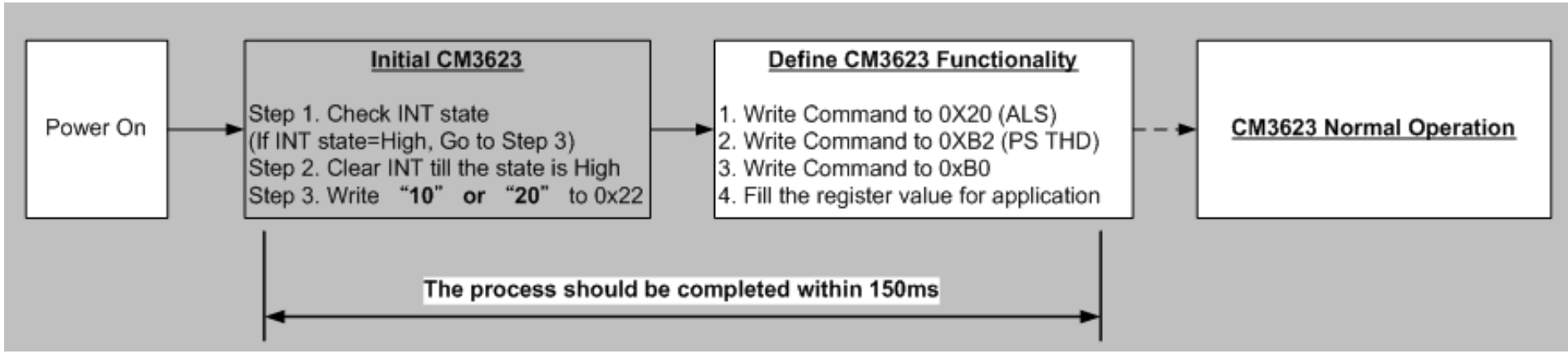
CM3623 Initialization & I2C Address

- Plz refer to CM3623 data sheet for more detail
- 2 different part no. to avoid I2C address conflict



SLAVE ADDRESS			OPERATION
Ordering Part Number	CM3623OP	CM3623OP-AD	
ALS	0x20	0x90	Write Command to CM3623
	0x21	0x91	Read MSB 8 bits of CM3623 ambient light data
	0x23	0x93	Read LSB 8 bits of CM3623 ambient light data
PS	0xB0/0xB2	0xF0/0xF2	Write Command to CM3623
	0xB1	0xF1	Read 8 bits of CM3623 proximity data
Initialization Address	0x22	0xF2	CM3623 initialization usage

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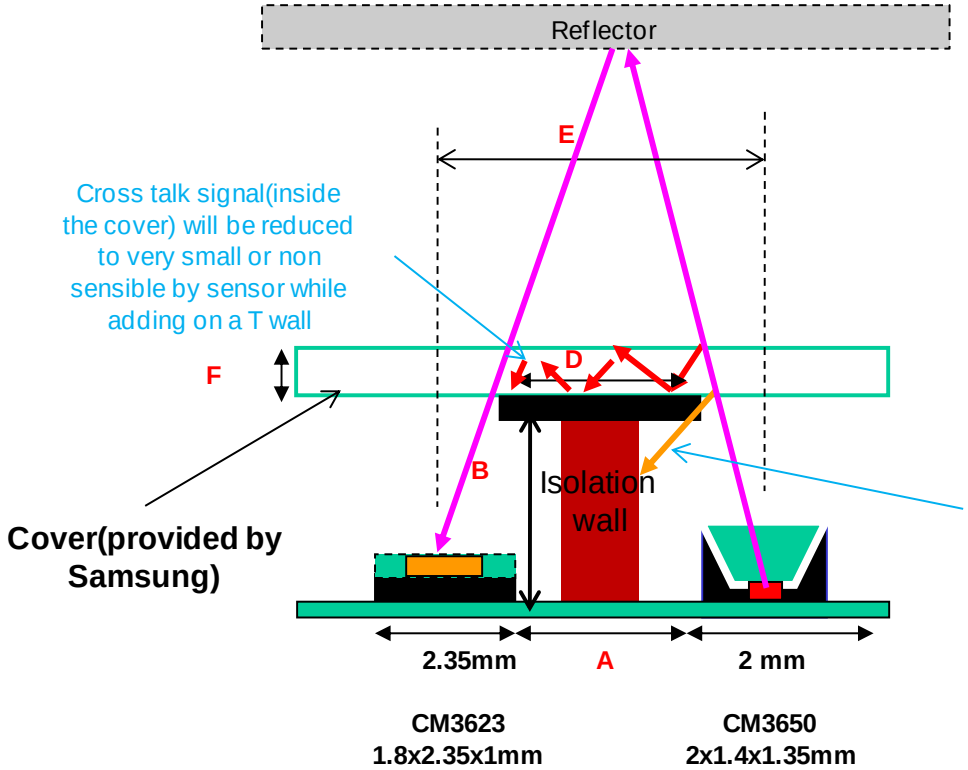
Mechanical Lens Design Suggestion without Light Pipe

CM3623+CM3650 ME design recommendation

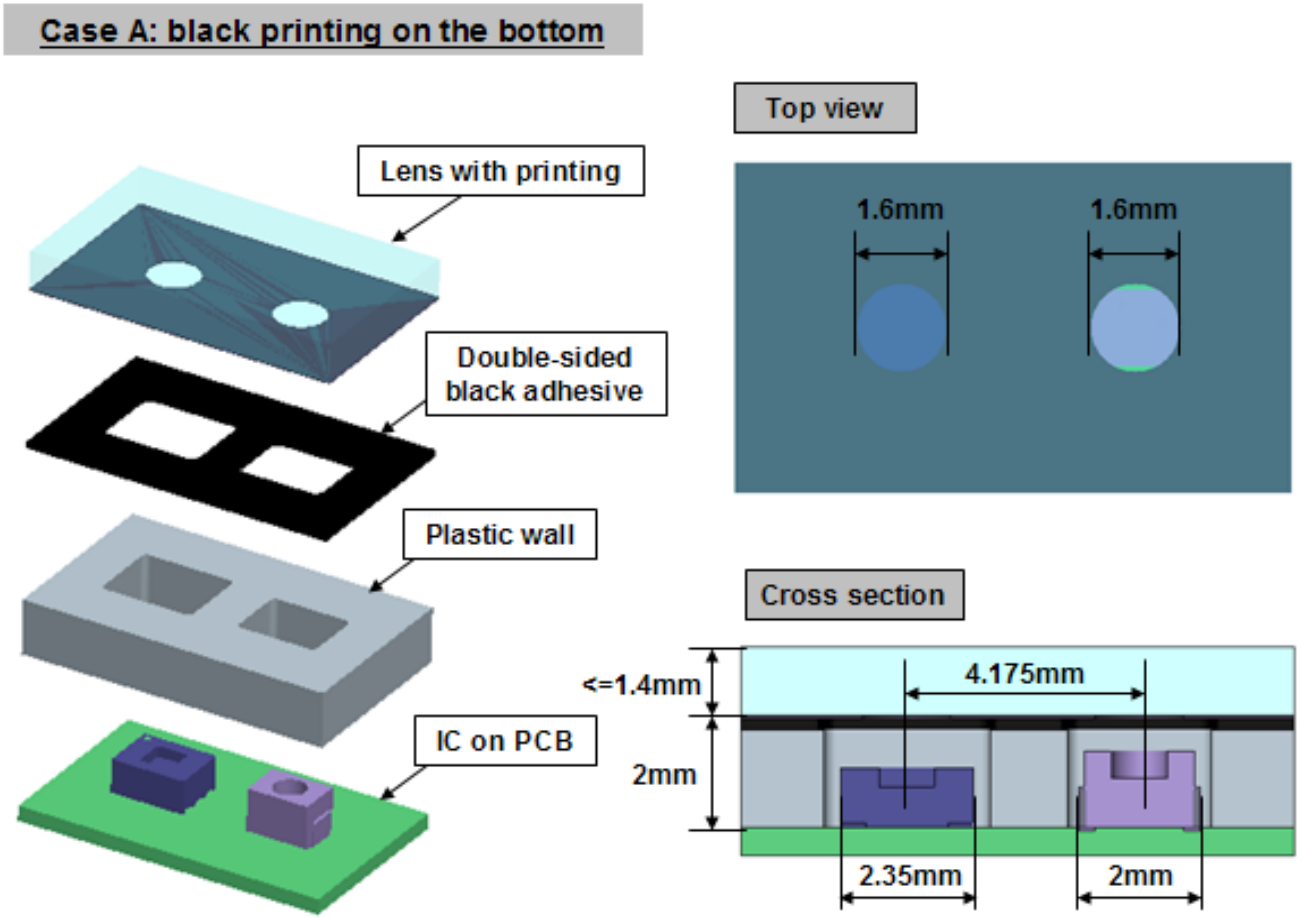


A: distance in between sensor and IR LED (edge to edge)
B: height of isolation wall
D: width of T wall(black tape instead)
E: distance in between the center of sensor and center of IR LER
F: thickness of window(cover)
Note: Isolation wall should put in the middle in between sensor and IE LED

A=2 mm, B=2 mm, D=2.575mm, E=4.175mm, F<=1.4mm

To achieve maximum detection performance, it is recommended that the transmittance of lens is above 55% for IR (850nm) and above 10% for visible light (550nm)

Mechanical Design Suggestion – CM3623+CM3650



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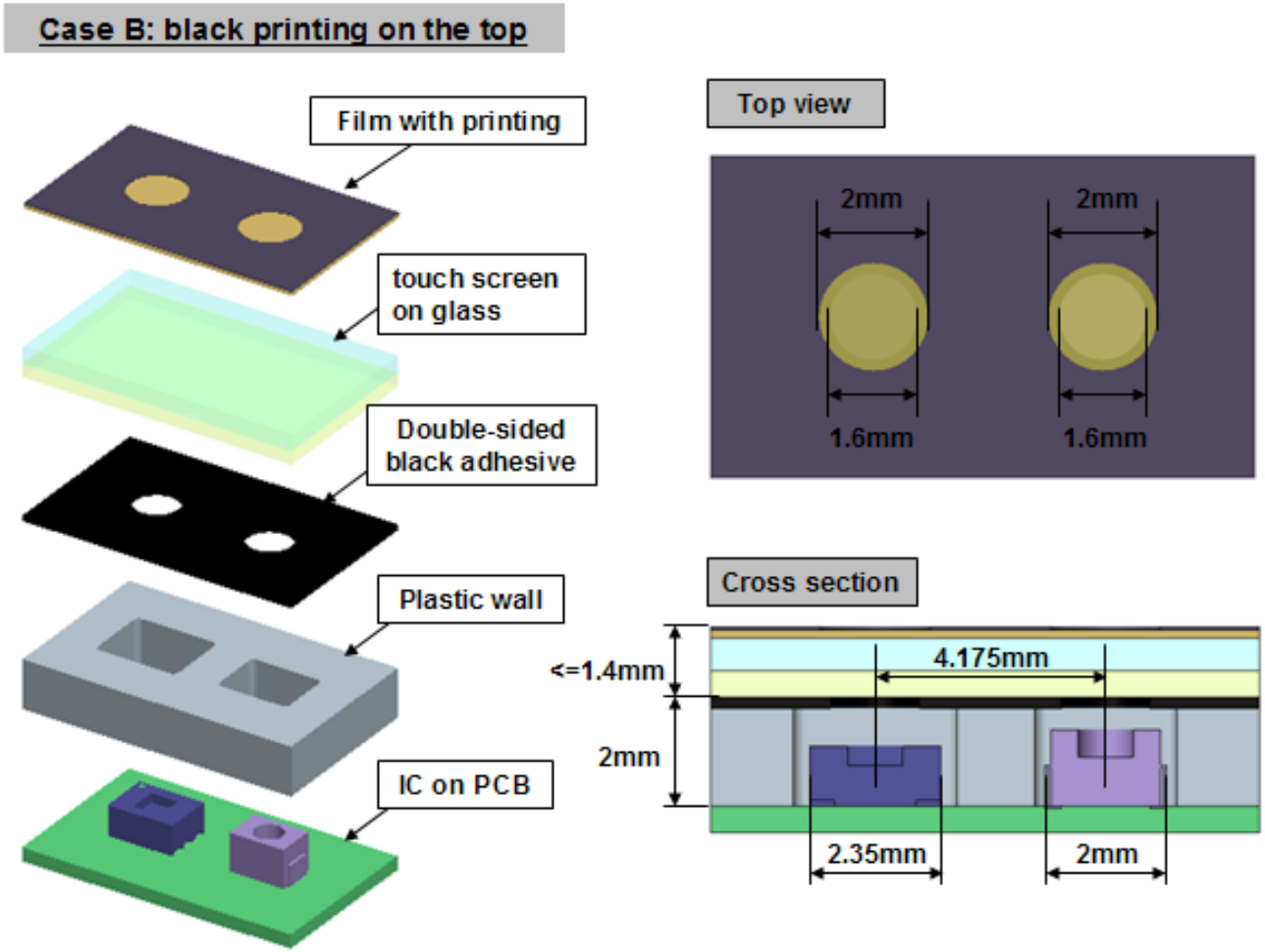
Mechanical Design Suggestion – CM3623+CM3650



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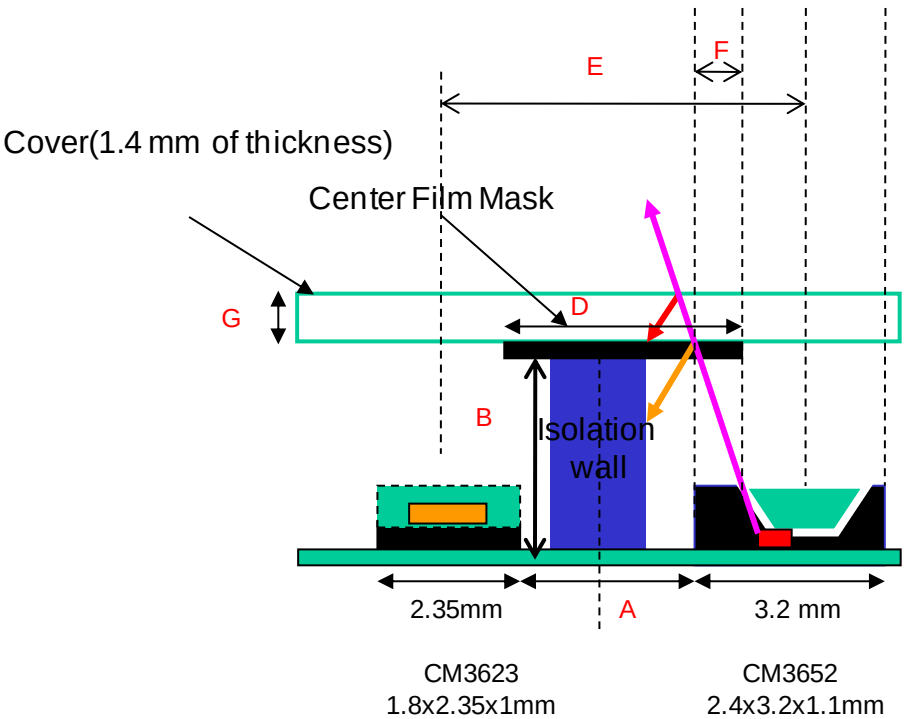
Mechanical Lens Design Suggestion without Light Pipe

CM3623+CM3652 ME design recommendation

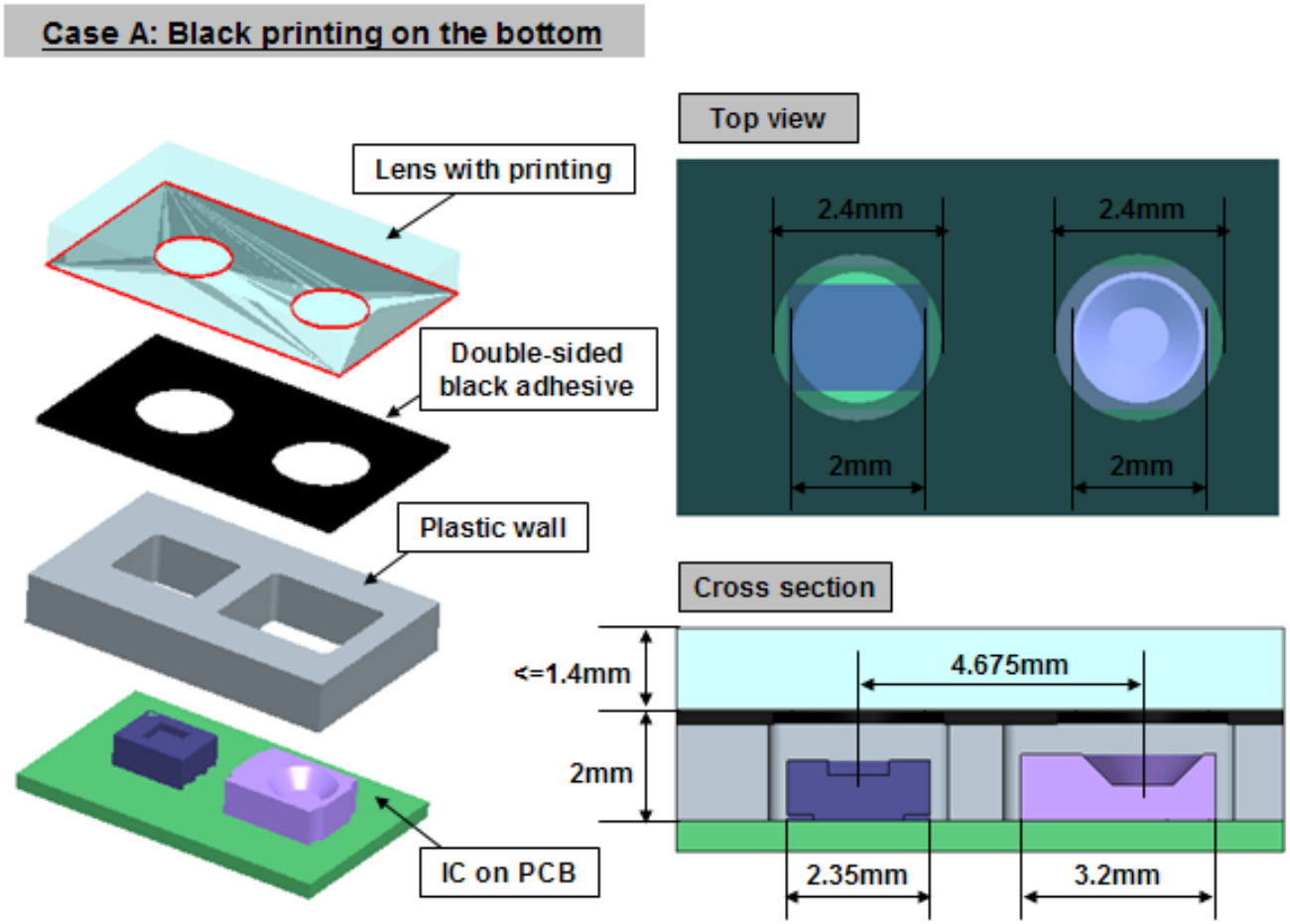


A: distance in between sensor and IR LED (edge to edge)
B: height of isolation wall
D: width of T wall
distance from edge of bowl-shaped IR-LED to left-middle side of center of isolation wall
E: distance in between the center of sensor and center of IR LER
F: edge of IR LED to edge of bowl-shaped
G: thickness of window(cover)

A=1.5 mm, B=1.8 mm, D=2.475mm, E=4.675mm , F=1 mm, G<=1.4mm

To achieve maximum detection performance, it is recommended that the transmittance of lens is above 55% for IR (850nm) and above 10% for visible light (550nm)

Mechanical Design Suggestion – CM3623+CM3652



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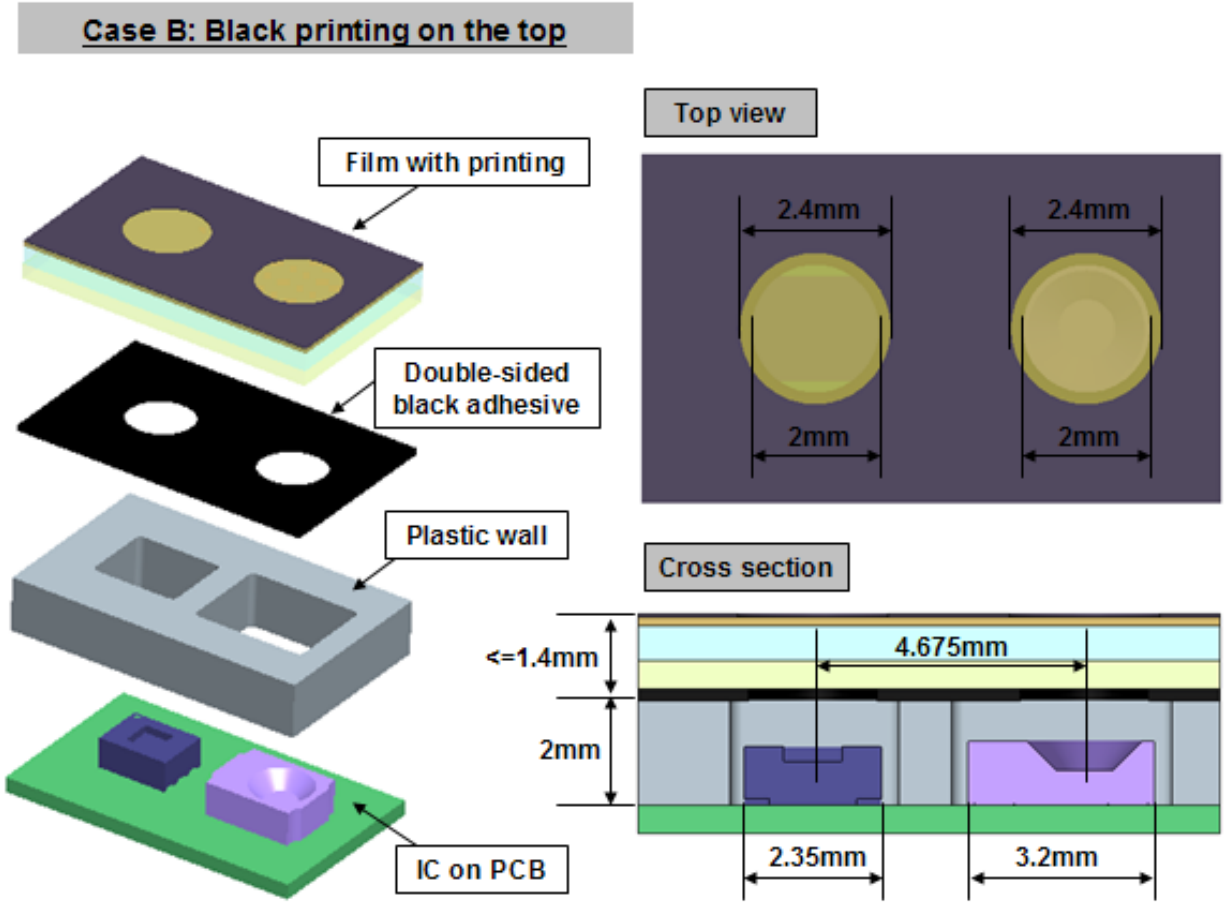
Mechanical Design Suggestion – CM3623+CM3652



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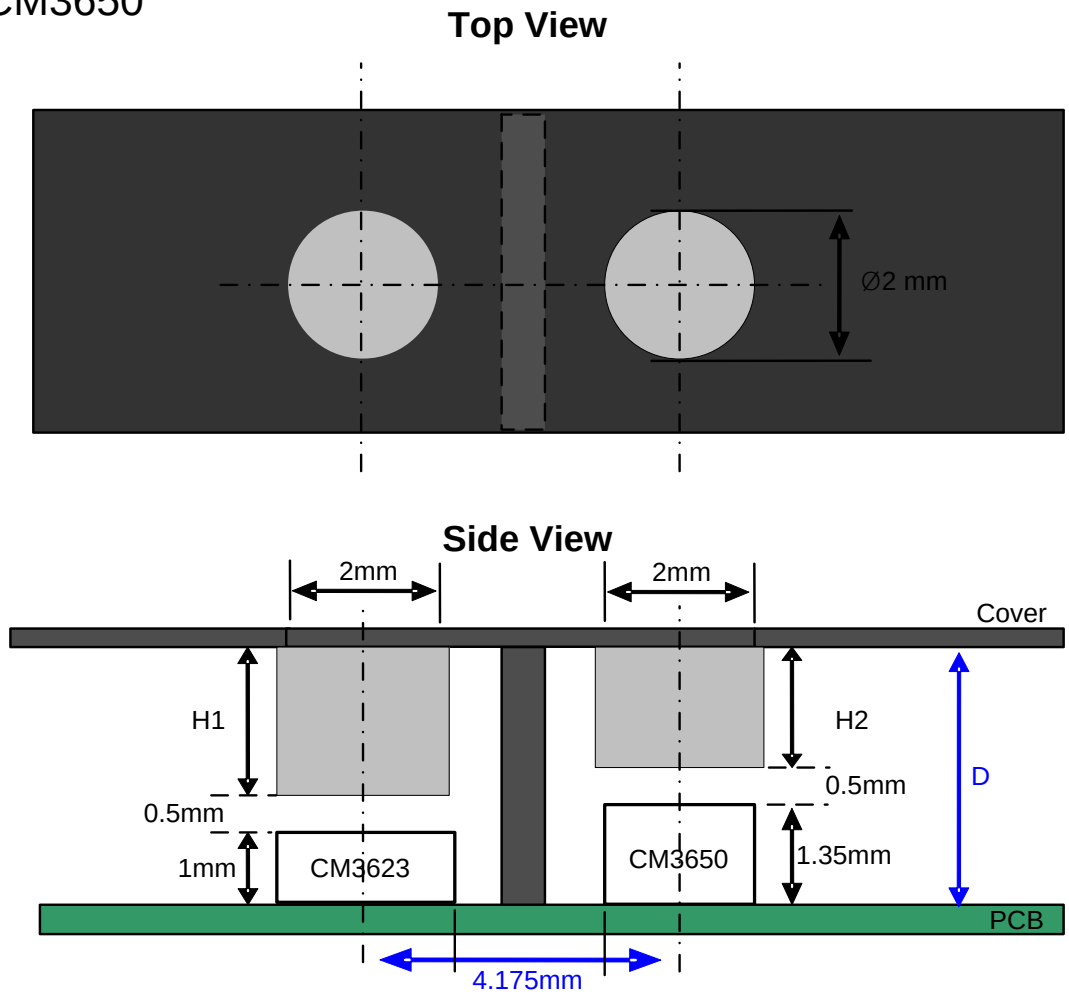
Mechanical Lens Design Suggestion with Light Pipe

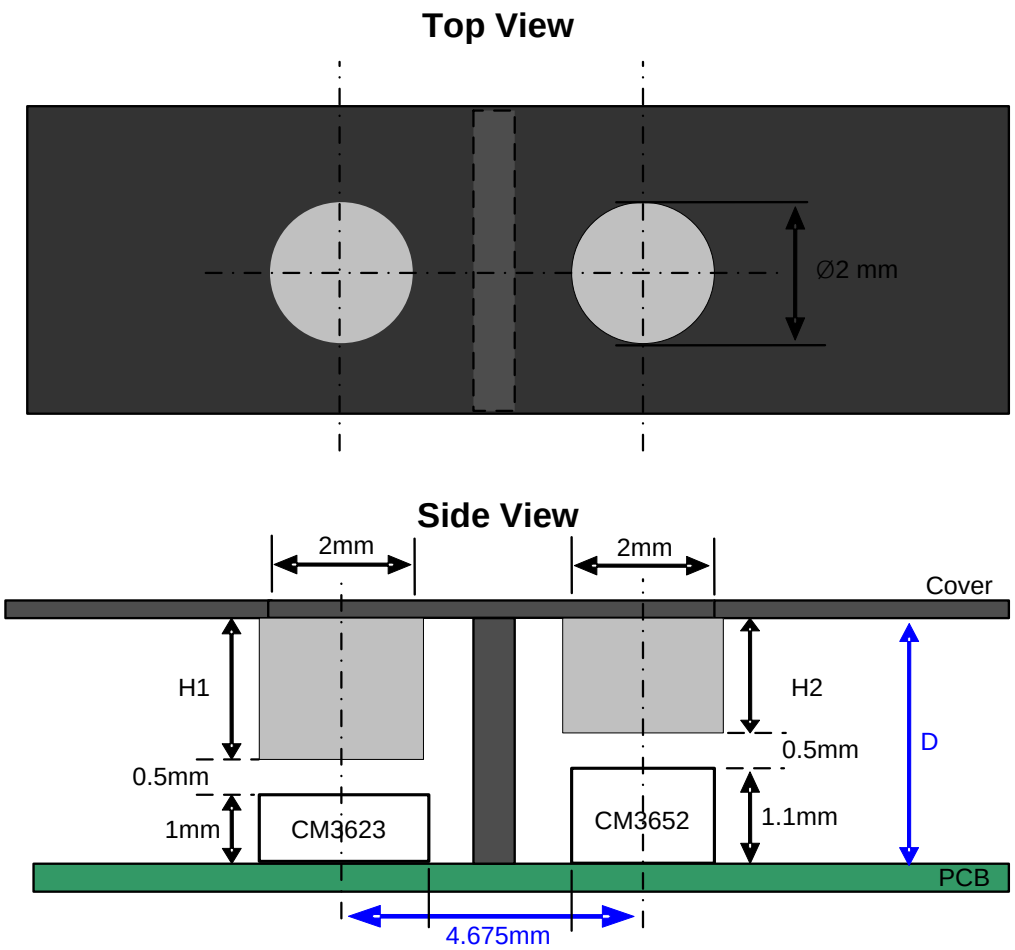
– CM3623+CM3650



Note: The T-Bar design is important in mechanical design. It can isolate the light leakage from CM3650

Mechanical Lens Design Suggestion with Light Pipe

– CM3623+CM3652

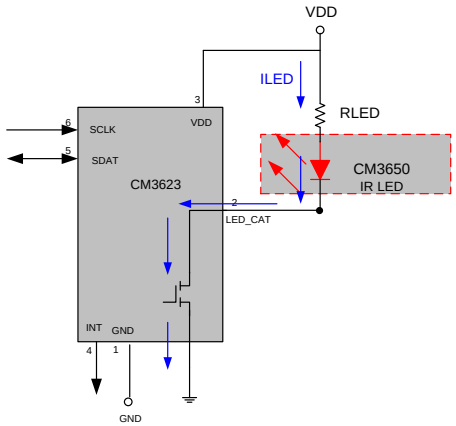
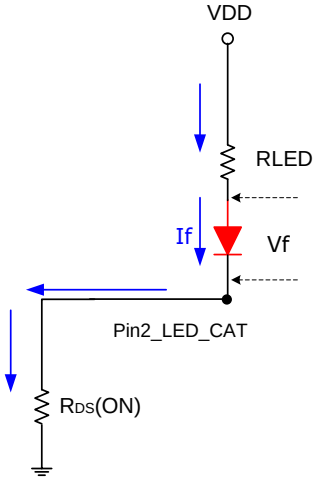


Note: The T-Bar design is important in mechanical design. It can isolate the light leakage from CM3652

R_{LED} Calculation

R_{LED} calculation should consider followings to obtain the realistic value for the application:

1) Operation voltage (VDD)
2) Forward current (If)
3) Forward voltage (Vf)

PS circuit	ILED path schematic drawing
	 **Note:** RDS(ON) = 1.5Ω (typ.)

After these 3 conditions have been confirmed, RLED can be calculated by using Vf – If chart of LED and the below equation:

$$R_{LED} = \frac{V_{DD} - V_F - (RDS_{ON} \times I_F)}{I_F} (\Omega)$$

For example:

If VDD is 2.85 V, and we need to adjust the If to 150mA, The Vf value by checking Vf – If chart is 1.75V, then R_{LED} is:

$$R_{LED} = \frac{2.85\ V - 1.75\ V - (1.5\Omega \times 150\ mA)}{150\ mA} = 5.83\ (\Omega)$$

Confidential B

Gravity (G) Sensor Design Notice

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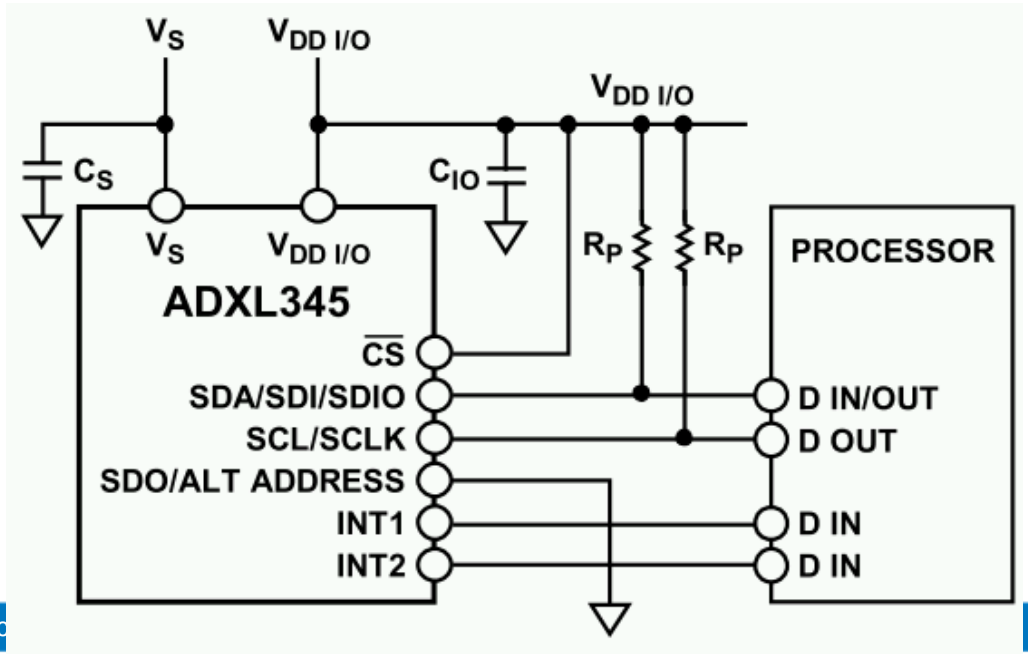
HW Connection Suggestion – ADXL345

- Vs: 2.0 ~ 3.6V
- Vdd i/o: 1.7 ~ Vs
- The 7-bit I2C address for the device is 0x53, followed by the R/W bit
- Users can select an alternate I2C address by connecting the SDO/ALT ADDRESS pin to high. The I2C address is then 0x1D, followed by the R/W bit
- INT1 & INT2 can be used simultaneously for various activities detection
- Put Rs (resistor series with power, up to 100 ohm) and Cs>2.2uF for noise injection.



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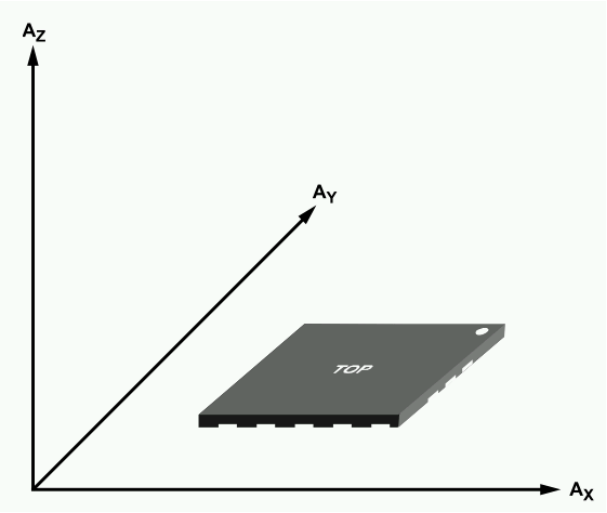
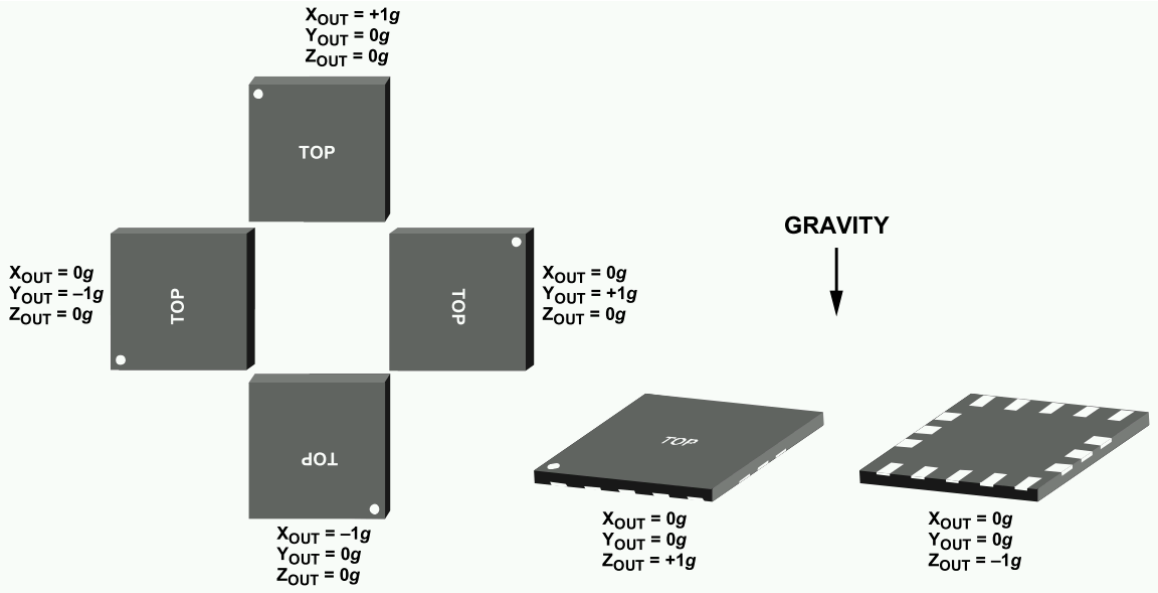
Component Placement & Orientation Notice



Sensing Axes of ADXL345



Output Response vs. Orientation to Gravity

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Confidential B

Magnetic Sensor Design Notice

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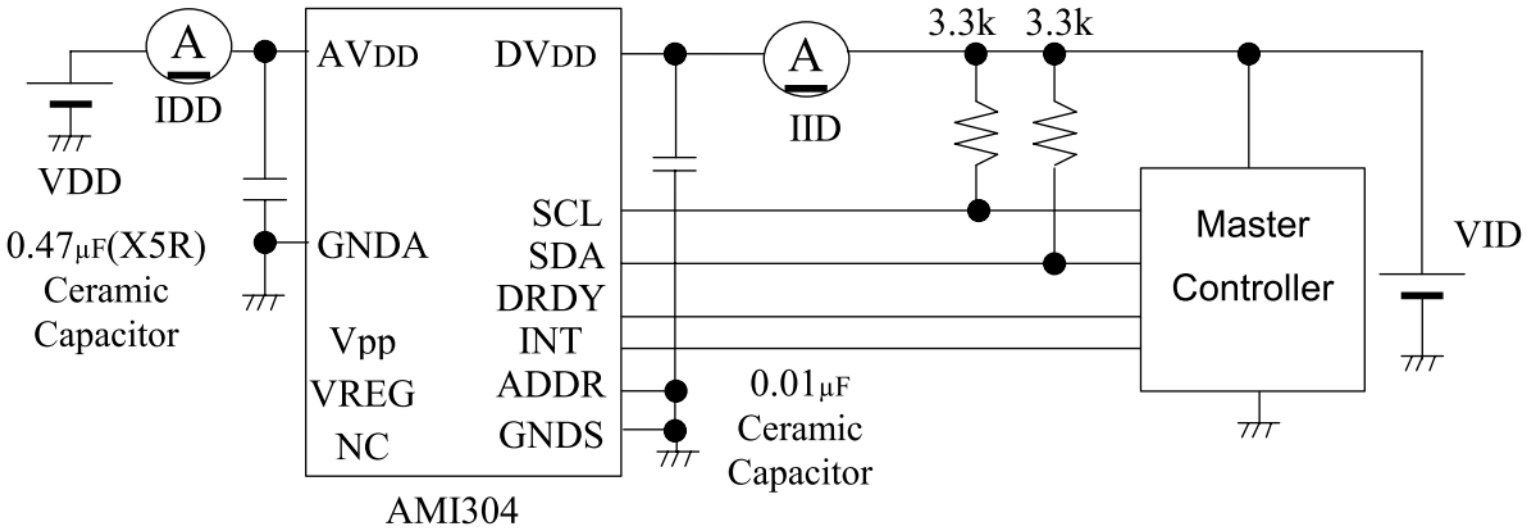
HW Connection Suggestion – AMI304

- Pin 1 (DVDD): 1.7 ~ AVDD
- Pin 3 (AVDD): 2.4 ~ 3.6V
- Pin 11 (DRDY): inform controller the data is ready to be read
- Pin 9 (INT): inform controller an abnormal magnetic field appears. This HW feature can be replaced by SW algorithm
- Pin6 (ADDR): 2 different I2C address selection
- Refer to AMI304 datasheet for more detail



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Component Placement Notice

When placing this sensor on PCB, the following guidelines should be taken

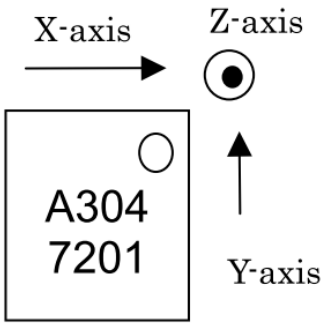
- **Keep a minimum distance of 15mm from the components with magnet**

  Ex: mic, speaker, vibrator, transformer, magnetic switch…etc.

- **Keep a minimum distance of 15mm from the components with magnet-conductive material (Iron, Cobalt, Nickel). They could be:**

  1. **Memory/SIM card socket, metal connector, screw, nut, spring**
  2. **IC with lead frame, battery, SAW filter, antenna, power amplifier, inductor**
  3. **EMI shielding case, LCD rear case**

- **Keep a minimum distance of 15mm from power ICs or PCB traces of 100mA or greater**
- **Do not cover the magnetic sensor with any material that can block the magnetic field**



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Thanks

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