PCB Design Guidelines for MT6575

V1.2

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Version Change History

Version	Release date	Change description	Editor
V1.2	2012/01/17	First English version	Charles Chen
		Revised p.72、p.74：update MT6329 BUCK/SPEAKER GND design recommendation.	

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Outlines

- **Brief of MT6575**
- **Packaging**
  - MT6575 POD
  - MT6575 Footprint
  - MT6575 floor planning
- **General guidelines**
  - PCB stack-up recommendation
  - Common Rules and Via Type
  - Placement Notes
  - MT6575 Fan-out recommendation
- **Design guidelines for high-speed digital signals**
  - PDN design for CPU
  - LPDDR2
  - LPDDR1
- **Others**
  - RF - USB - HDMI - MIPI - Charger
  - 32K Crystal - Audio - SIM Card -T-CARD - Camera
  - **MT6620**(BT/FM/WiFi/GPS) –**MT6329**

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Brief of MT6575

- MT6575 is the next-generation 3.75G smart-phone solution of MediaTek with ARM CA9 and 1.0GHz CPU.

Dual SIM

One-stop Service:
Analog TV
BT/FM/Wi-Fi/GPS

Video Telephony
720p Video Playback
Video Streaming

Full HTML Browser
Better Performance

MT6575
CA9 1GHz AP
Rel. 6 HSPA Modem
Use External PMIC

8M Camera
FWVGA Video Record
Face Detection / Smile Shot

3D Acceleration
Launcher ,Live Wallpaper
Gallery,Games

Tier 1 Performance
Audio/Speech/Modem
Low Power

Turnkey Solution
Android latest version
IOT, FTA, CTS100% Pass

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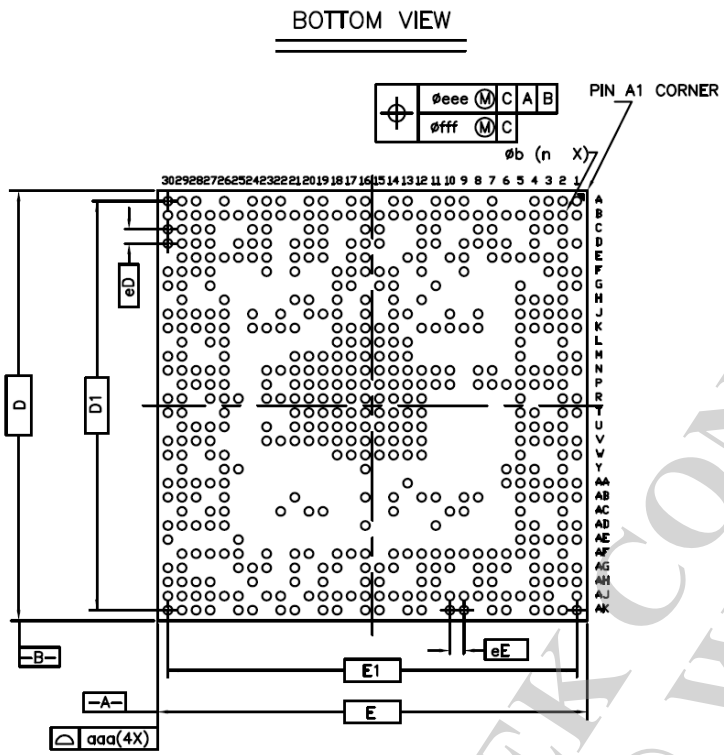
MT6575 POD



		Symbol	Common Dimensions
Package :			TFBGA
Body Size:	X	E	12.200
	Y	D	12.200
Ball Pitch :	X	eE	0.400
	Y	eD	0.400
Total Thickness :		A	1.200 MAX.
Mold Thickness :		M	0.700 Ref.
Substrate Thickness :		S	0.260 Ref.
Ball Diameter :			0.250
Stand Off :		A1	0.110 ~ 0.210
Ball Width :		b	0.200 ~ 0.300
Package Edge Tolerance :		aaa	0.100
Mold Flatness :		bbb	0.100
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.050
Ball Count :		n	537
Edge Ball Center to Center :	X	E1	11.600
	Y	D1	11.600

- Package info.
  - Body size: 12.2mmx12.2mmx1.2mm max
  - Ball pitch: 0.4mm
  - Ball diameter: 0.25mm normal
  - Ball counts: 537

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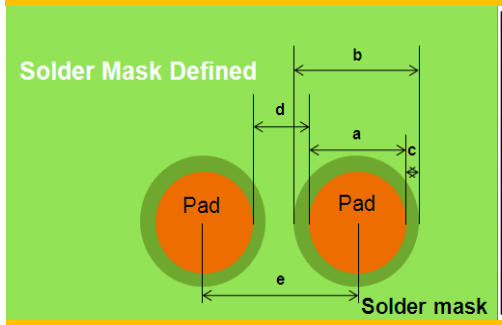
MT6575 Footprint

- Due to many PWR/GND pins around central area may connected by wider traces, it is recommend to implement "**Solder Mask Defined + Copper Defined**" for MT6575 PCB footprint design to reducing SMT risk caused by deformed pads.

Figure1, solder mask defined for central red pins is recommended. Pad size:0.325mm, solder mask:0.25mm.



Solder Mask Defined PCB land pad and Solder mask opening rule			
Solder mask opening	a	0.25mm	9.8mil
Land pad size	b	0.325mm	12.8mil
Solder mask on pad	c	0.038mm	1.5mil
Webbing between pads	d	0.15mm	6mil
Ball pitch	e	0.4mm	15.8mil

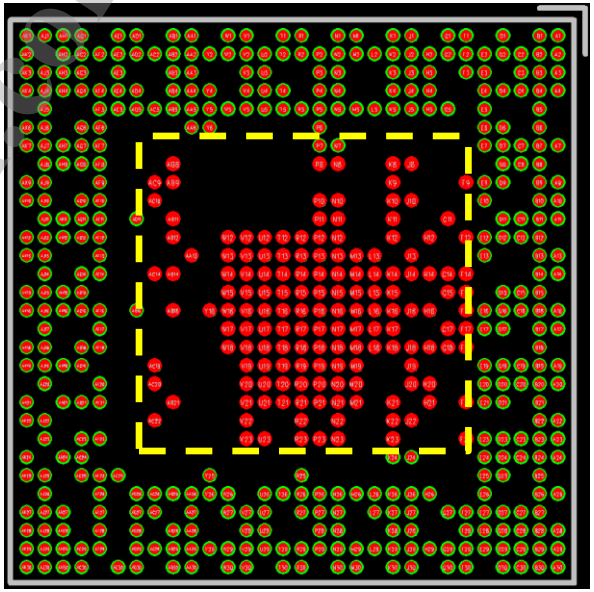
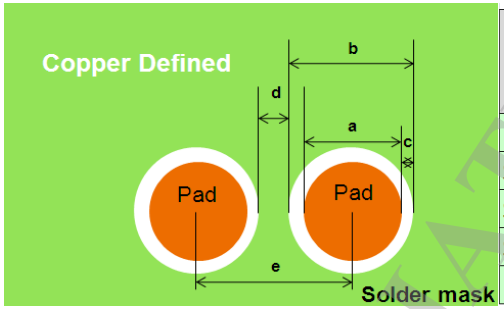


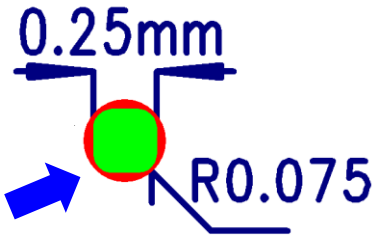
Figure 1

Figure1, copper defined for pins out of yellow frame is recommended. Pad size:0.25mm, solder mask:0.325mm.



Copper Defined PCB land pad and Solder mask opening rule			
Land pad size	a	0.25mm	9.8mil
Solder mask opening	b	a+0.075mm	a+3mil
Solder mask clearance	c	0.038mm	1.5mil
Solder dam	d	0.075mm	3mil
Ball pitch	e	0.4mm	15.8mil

- Recommend stencil opening➔0.25mm square with 0.075R angle.



Recommend to adopt 0.1/0.25mm(drill/land) laser via size underneath MT6575 for better SMT yield.

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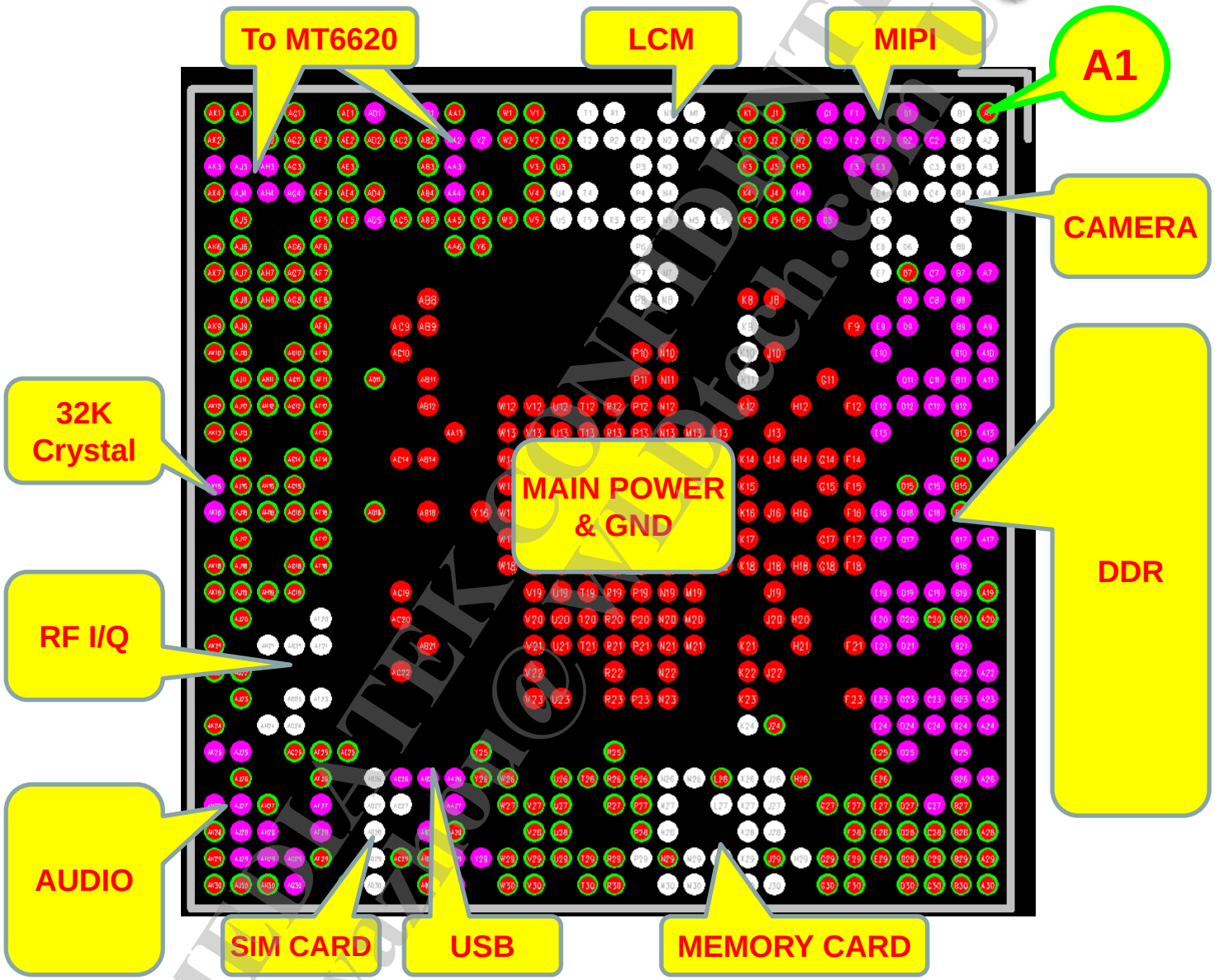
MT6575 Floor Planning



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MT6575 PCB Stack-up Recommendation

- The total thickness of the PCB is recommended to be less 1.0mm±10%。
- Please follow the recommended layer definition, the thickness and material of pre-preg/core to achieve the optimal electrical performance.
- Regarding the ”Layer definition”, we only define LPDDR1/2. The layers with “N/A” can be defined by the system H/W designers and it is recommended to use those layers to reinforce the power/ground plans of LPDDR1/2.
- For the other signal buses, please follow the PCB design guidelines in this document.
- The stack-up recommendations include:
  - 10 layers with HDI-2 (stacked via)
  - 10 layers with HDI-2 (stagger via)
  - 10 layers with HDI-1
  - 8 layers with HDI-1
  - 8 layers with HDI-2 (stagger via)
  - 10 layers with HDI-2 (stacked via)

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10 layers with HDI-2 (stacked via)

10L HDI-2 (2-6-2), 1.0mm

Layers	Stackup	Theoretic thickness (mm)	Theoretic thickness (mils)	Material	ER	Layer definition Signal/Power/Ground (S/P/G) LPDDR1/2	Layer definition Signal/Power/Ground (S/P/G) LPDDR1/2
SR		0.030	1.2	SR	3.5		
L1		0.035	1.4	Copper		S	S
		0.070	2.8	Prepreg (1080)	3.7		
L2		0.030	1.2	Copper		S	P
		0.070	2.8	Prepreg (1080)	3.7		
L3		0.030	1.2	Copper		P	S
		0.080	3.2	Prepreg (1080)	3.7		
L4		0.015	0.6	Copper		G/S	P
		0.076	3.0	core	4.1		
L5		0.015	0.6	Copper		P	G/S
		0.105	4.1	Prepreg (2116)	3.9		
L6		0.015	0.6	Copper		G	G
		0.076	3.0	core	4.1		
L7		0.015	0.6	Copper		N/A	N/A
		0.080	3.2	Prepreg (1080)	3.7		
L8		0.030	1.2	Copper		N/A	N/A
		0.070	2.8	Prepreg (1080)	3.7		
L9		0.030	1.2	Coper		N/A	N/A
		0.070	2.8	Prepreg (1080)	3.7		
L10		0.035	1.4	Copper		N/A	N/A
SR		0.030	1.2	SR	3.5		
	Total	1.0 mm ±10%					

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10 layers with HDI-2 (stagger via)

10L HDI-2 (1-1-6-1-1), 1.0mm/0.9mm

Layers	Stackup	Proposal 1 (1.0 mm)		Proposal 2 (0.9 mm)		Material	ER	Layer definition Signal/Power/Ground (S/P/G)
		Theoretic thickness (mm)	Theoretic thickness (mils)	Theoretic thickness (mm)	Theoretic thickness (mils)			LPDDR1/2
SR		0.030	1.2	0.030	1.2	SR	3.5	
L1		0.035	1.4	0.035	1.4	Copper		S
		0.070	2.8	0.050	2.0	Prepreg (1080)	3.7	
L2		0.030	1.2	0.030	1.2	Copper		S
		0.070	2.8	0.050	2.0	Prepreg (1080)	3.7	
L3		0.030	1.2	0.030	1.2	Copper		P
		0.080	3.2	0.070	2.8	Prepreg (1080)	3.7	
L4		0.015	0.6	0.015	0.6	Copper		G/S
		0.076	3.0	0.076	3.0	core	4.1	
L5		0.015	0.6	0.015	0.6	Copper		P
		0.105	4.1	0.105	4.1	Prepreg (2116)	3.9	
L6		0.015	0.6	0.015	0.6	Copper		G
		0.076	3.0	0.076	3.0	core	4.1	
L7		0.015	0.6	0.015	0.6	Copper		N/A
		0.080	3.2	0.070	2.8	Prepreg (1080)	3.7	
L8		0.030	1.2	0.030	1.2	Copper		N/A
		0.070	2.8	0.050	2.0	Prepreg (1080)	3.7	
L9		0.030	1.2	0.030	1.2	Coper		N/A
		0.070	2.8	0.050	2.0	Prepreg (1080)	3.7	
L10		0.035	1.4	0.035	1.4	Copper		N/A
SR		0.030	1.2	0.030	1.2	SR	3.5	
	Total	1.0 mm ±10%		0.9 mm ±10%				

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10 layers with HDI-1

10L HDI-1 (1-8-1), 1.0mm

Layers	Stackup	Theoretic thickness (mm)	Theoretic thickness (mils)	Material	ER	Layer definition Signal/Power/Ground (S/P/G) LPDDR1/2
SR		0.030	1.2	SR	3.5	
L1		0.035	1.4	Copper		S
		0.070	2.8	Prepreg (1080)	3.7	
L2		0.031	1.2	Copper		S
		0.070	2.8	Prepreg (1080)	3.7	
L3		0.015	0.6	Copper		P
		0.100	3.9	core	4.1	
L4		0.015	0.6	Copper		G/S
		0.070	2.8	Prepreg (1080)	3.7	
L5		0.015	0.6	Copper		P
		0.100	3.9	core	4.1	
L6		0.015	0.6	Copper		G
		0.070	2.8	Prepreg (1080)	3.7	
L7		0.015	0.6	Copper		N/A
		0.100	3.9	core	4.1	
L8		0.015	0.6	Copper		N/A
		0.070	2.8	Prepreg (1080)	3.7	
L9		0.031	1.2	Coper		N/A
		0.070	2.8	Prepreg (1080)	3.7	
L10		0.035	1.4	Copper		N/A
SR		0.030	1.2	SR	3.5	
	Total	1.0 mm ±10%				

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8 layers with HDI-1

8L HDI-1 (1-6-1), 1.0mm/0.8mm

Layers	Stackup	Proposal 1 (1.0 mm)				Proposal 2 (0.8 mm)				Layer definition Signal/Power/Ground (S/P/G)
		Theoretic thickness (mm)	Theoretic thickness (mils)	Material	ER	Theoretic thickness (mm)	Theoretic thickness (mils)	Material	ER	LPDDR1/2
SR		0.030	1.2	SR	3.5	0.030	1.2	SR	3.5	
L1		0.030	1.2	Copper		0.025	1.0	Copper		S
		0.076	3.0	Prepreg (1080)	3.7	0.069	2.7	Prepreg (1080)	3.7	
L2		0.030	1.2	Copper		0.025	1.0	Copper		S
		0.109	4.3	Prepreg (2116)	3.9	0.069	2.7	Prepreg (1080)	3.7	
L3		0.015	0.6	Copper		0.015	0.6	Copper		P
		0.127	5.0	Core	4.1	0.102	4.0	Core	4.1	
L4		0.015	0.6	Copper		0.015	0.6	Copper		G/S
		0.127	5.0	Prepreg (2116)	3.9	0.114	4.5	Prepreg (2116)	3.9	
L5		0.015	0.6	Copper		0.015	0.6	Copper		P
		0.127	5.0	Core	4.1	0.102	4.0	Core	4.1	
L6		0.015	0.6	Copper		0.015	0.6	Copper		G
		0.109	4.3	Prepreg (2116)	3.9	0.069	2.7	Prepreg (1080)	3.7	
L7		0.030	1.2	Coper		0.025	1.0	Coper		N/A
		0.076	3.0	Prepreg (1080)	3.7	0.069	2.7	Prepreg (1080)	3.7	
L8		0.030	1.2	Copper		0.025	1.0	Copper		N/A
SR		0.030	1.2	SR	3.5	0.030	1.2	SR	3.5	
	Total	1.0 mm ±10%				0.8 mm ±10%				

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8 layers with HDI-2 (stagger via)

8L HDI-2 (2-4-2), 0.9mm

Layers	Stackup	Theoretic thickness (mm)	Theoretic thickness (mils)	Material	ER	Layer definition Signal/Power/Ground (S/P/G) LPDDR1/2	Layer definition Signal/Power/Ground (S/P/G) LPDDR1/2
SR		0.030	1.2	SR	3.5		
L1		0.030	1.2	Copper		S	S
		0.061	2.4	Prepreg (1080)	3.7		
L2		0.030	1.2	Copper		S	P
		0.060	2.4	Prepreg (1080)	3.7		
L3		0.031	1.2	Copper		P	S
		0.123	4.8	Prepreg (2116)	3.9		
L4		0.014	0.6	Copper		G/S	P
		0.140	5.5	Core	4.1		
L5		0.014	0.6	Copper		P	G/S
		0.123	4.8	Prepreg (2116)	3.9		
L6		0.031	1.2	Copper		G	G
		0.060	2.4	Prepreg (1080)	3.7		
L7		0.030	1.2	Coper		N/A	N/A
		0.061	2.4	Prepreg (1080)	3.7		
L8		0.030	1.2	Copper		N/A	N/A
SR		0.030	1.2	SR	3.5		
	Total	0.9 mm ±10%					

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8 layers with HDI-2 (stacked via)

8L HDI-2 (2-4-2), 0.9mm

Layers	Stackup	Theoretic thickness (mm)	Theoretic thickness (mils)	Material	ER	Layer definition Signal/Power/Ground (S/P/G) LPDDR1/2	Layer definition Signal/Power/Ground (S/P/G) LPDDR1/2
SR		0.030	1.2	SR	3.5		
L1		0.030	1.2	Copper		S	S
		0.061	2.4	Prepreg (1080)	3.7		
L2		0.030	1.2	Copper		S	P
		0.060	2.4	Prepreg (1080)	3.7		
L3		0.031	1.2	Copper		P	S
		0.123	4.8	Prepreg (2116)	3.9		
L4		0.014	0.6	Copper		G/S	P
		0.140	5.5	Core	4.1		
L5		0.014	0.6	Copper		P	G/S
		0.123	4.8	Prepreg (2116)	3.9		
L6		0.031	1.2	Copper		G	G
		0.060	2.4	Prepreg (1080)	3.7		
L7		0.030	1.2	Coper		N/A	N/A
		0.061	2.4	Prepreg (1080)	3.7		
L8		0.030	1.2	Copper		N/A	N/A
SR		0.030	1.2	SR	3.5		
	Total	0.9 mm ±10%					

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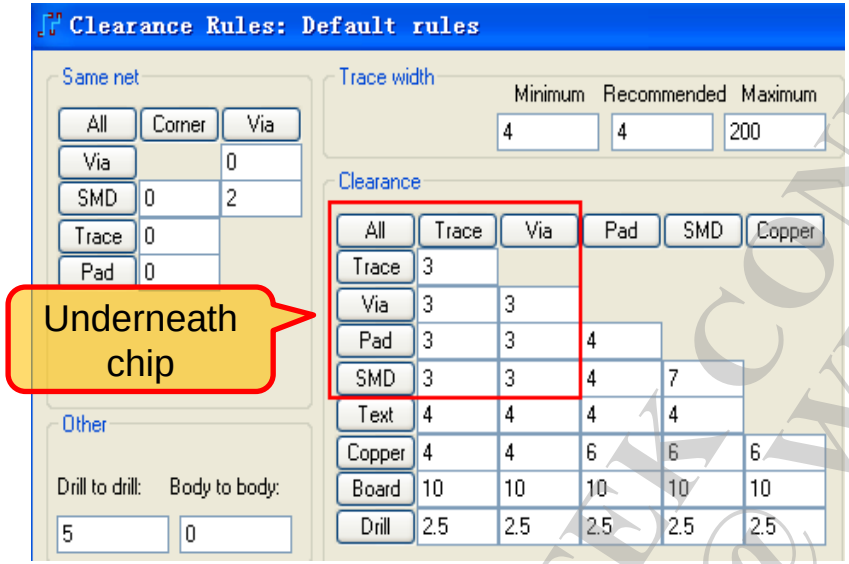
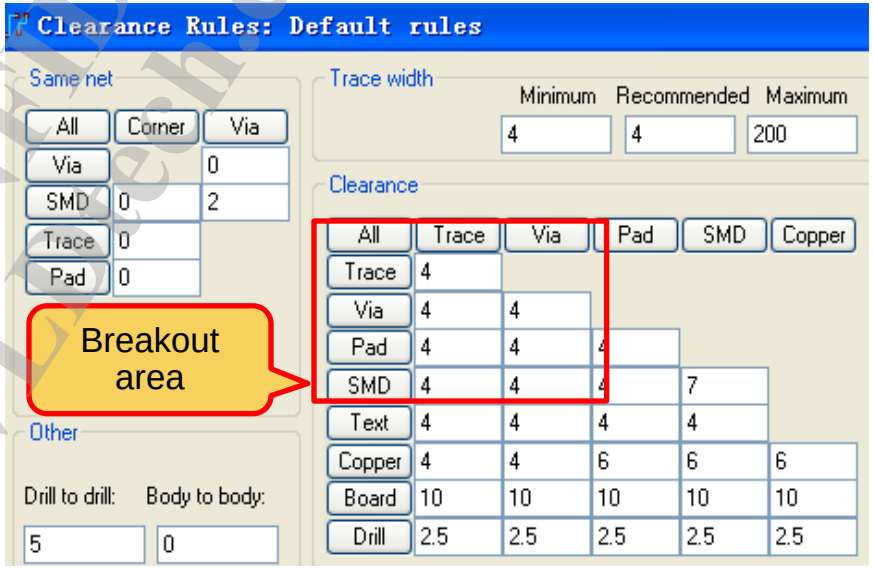
Design Rules and Via Type

- **The min. trace width/spacing:**
  - Underneath MT6575: 3/3 mils
  - Breakout area: 4/4 mils





- **Via type:**
  - Blind Via (underneath MT6575)➔ 4/10 mil
  - Blind Via (outside MT6575) ➔ 4/12 mil
  - Buried Via➔12/20mil
  - Through Via➔12/20 mil

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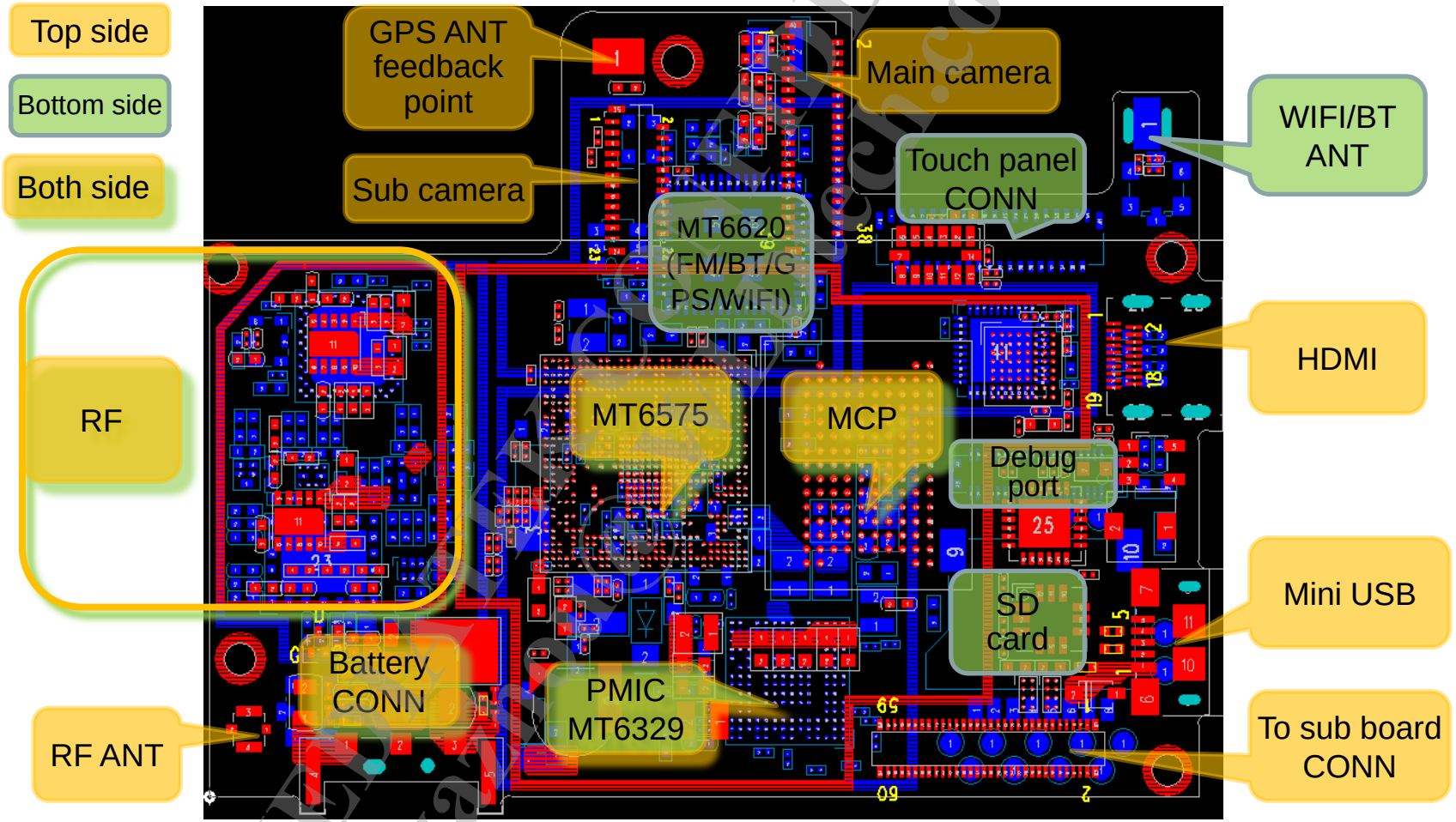
Placement Notes

- Below is 10 layer HDI+1 reference board placement. LCM, SIM card, Audio Jack, Mic, Speaker etc. are allocated on the sub-board.
- Components should be placed according to schematic and mechanism. RF devices could be placed on both side according to the limitation of mechanism, board size, impedance control, etc.



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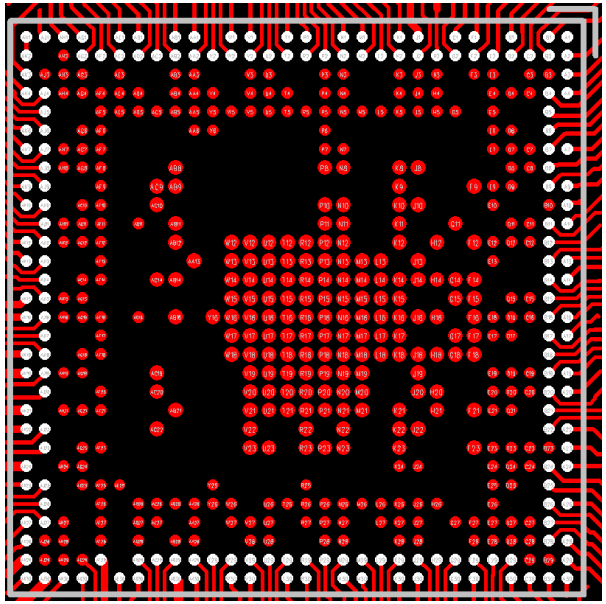
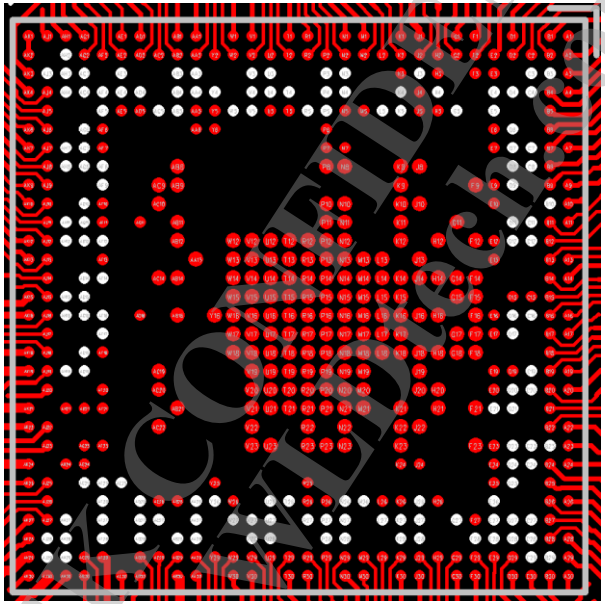
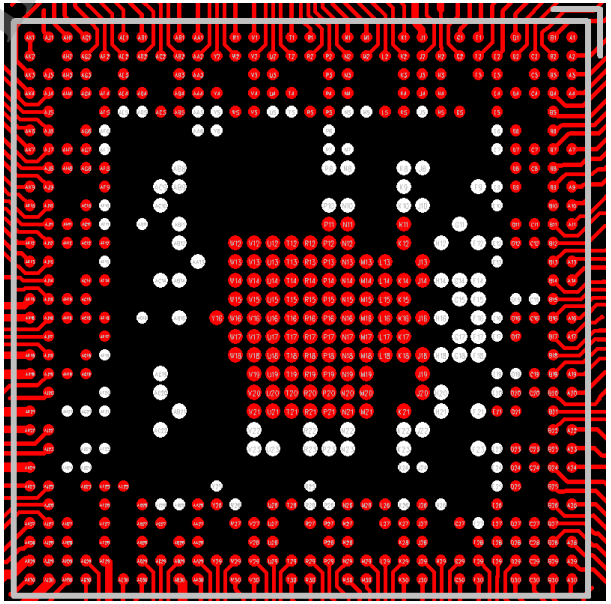
MT6575 Fan-out Recommendation







Fan out by top layer for 1st & 2nd rows.

Fan out by layer 2 for 3rd to 5th rows.
Blind via (4/10mil) must be placed at the center of ball pads.

Other balls could be fanned out by inner layers, and keep GND plane as solid as possible.

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PDN design for CPU

- For the high-end smart phones, CPU with high-speed operation up to GHz or above, the instantaneous current and power consumption can't be handled by conventional PCB design concepts. Therefore, PCB with a good PDN (power delivery network) design is a must to ensure the proper functioning of high-speed CPU.
- A complete PDN design contains the whole path from the VRM output to power input of the main chip, including the power transmission and the relevant return path. Good PDN design on PCB requires to optimize the relevant power trace, the allocation of the power and ground via (PWR / GND via), and the allocation of its decoupling capacitors. The following PCB guidelines is to regulate the PCB layout to achieve the best PDN design.

MT6575 ball list for VDDK_DVFS(VPROC), VDDK(VCORE) and VDDK:

Ball	#	Signal Name	Description
M20, N20, P20, R20, T20, U20, V20, M21, N21, P21, R21, T21, V21	13	**VDDK_DVFS** (VAPROC_6575)	Provide application processor CPU core power. 1.25V~0.9V (DVFS) Maximum current 1.12A
E25	1	**VDDK_DVFS_OUT** (VPROC_FB)	VDDK_DVFS remote sense
P11, K12, N12, P12, R12, T12, U12, V12, W12, L13, M13, W13, G14, H14, J14, W14, K15, V15, K16, V16, K17, V17, G18, H18, J18, U18, V19	27	**VDDK** (VCORE_6575)	Provide logic power and modem MCU core power. 1.25V/0.9V Maximum current 1.0A

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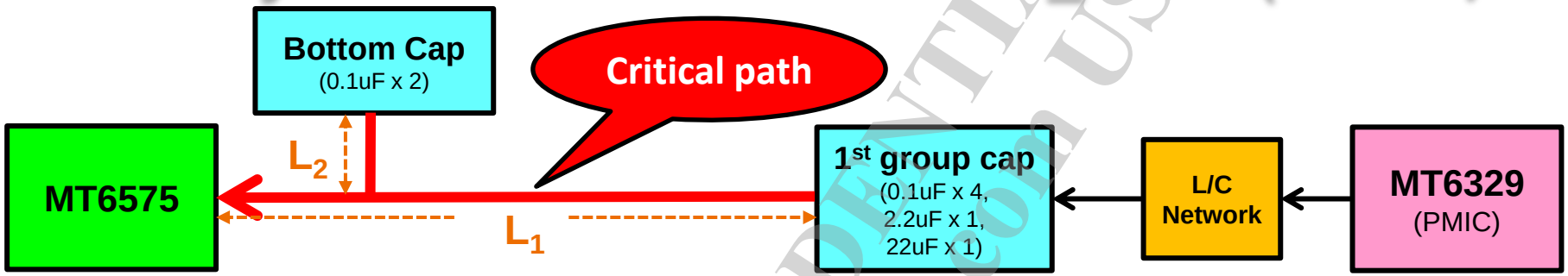
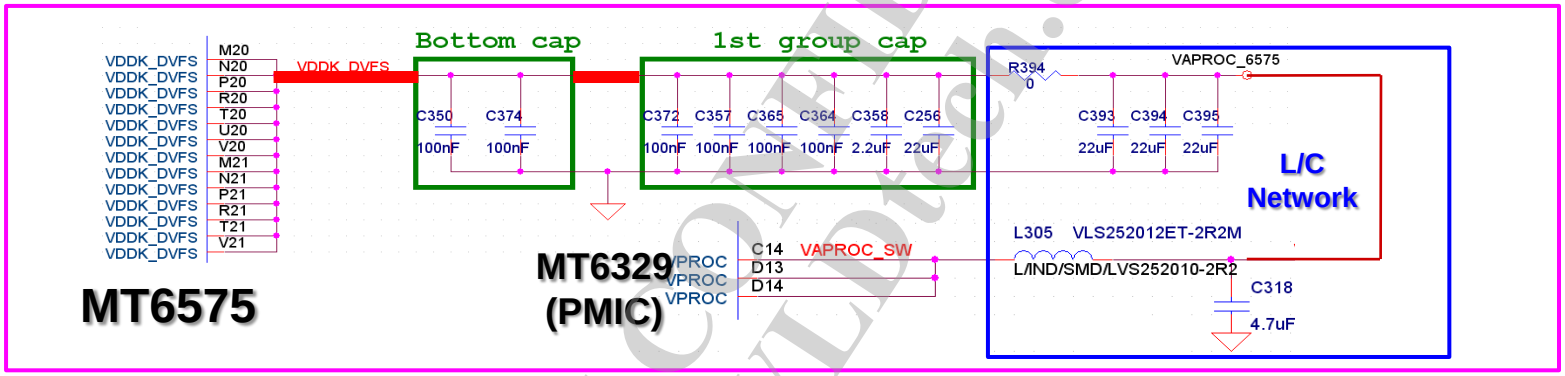
PCB Layout Guidelines for VDDK_DVFS(VPROC)





1. The PDN network starts from MT6329 (PMIC) output pins, through the LC low-pass filter, which produces the DC power, and then passes the first capacitor group (1st group cap) to supply power for high-speed CPU.
2. The "critical path" is defined as the path from the "1st group cap" to the VDDK_DVFS of MT6575. The trace routing on the PCB requires to follow the following PCB layout guidelines.
3. There are four 0.1uF, a 2.2uF, and a 22uF decoupling capacitors for "1st group cap ".
4. Please allocate two 0.1uF decoupling capacitors for "Bottom cap", and make them as close to VDDK_DVFS as possible.
5. L_1 is defined as the wide power trace between "1st group cap" area to MT6575VDDK_DVFS ("critical path"), and its PCB guideline is as follows:
   1) If there are three power planes for CPU, it is recommended that L_1: trace length ≤ 650mil; trace width ≥ 40mil, and make them as parallel traces (suggestion 1 , * Note 1).
   2) If there are two power planes for CPU, it is recommended that L_1: trace length L ≤ 650mil; trace width: layer-1 ≥ 40mil, layer-2 ≥ 80mil, and make them as parallel traces (suggestion 2 , * Note 2).
6. L_2 is defined as the path between the "Bottom cap" area and the "critical path", and the PCB layout guideline is defined as follows:
   1) Double-sided SMT: please place these two 0.1uF capacitors directly underneath the VDDK_DVFS balls, and make the capacitors in series with the wide power traces by vias (make L_2 as short as possible).
   2) Single-sided SMT: please make these two 0.1uF capacitors as close to the MT6575 as possible (make L_2 as short as possible).

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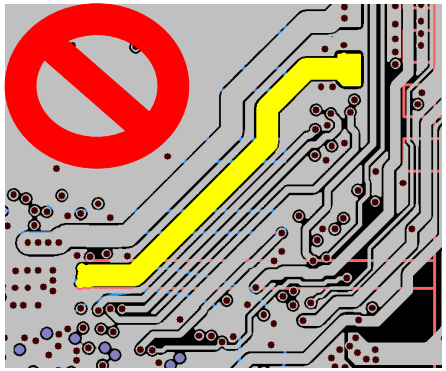
*** Note1、2：detailed examples in next page**

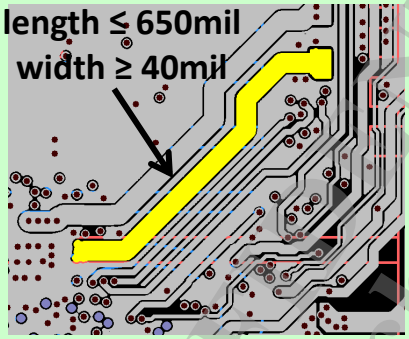
PCB Layout Guidelines for VDDK_DVFS(VPROC) (cont.)

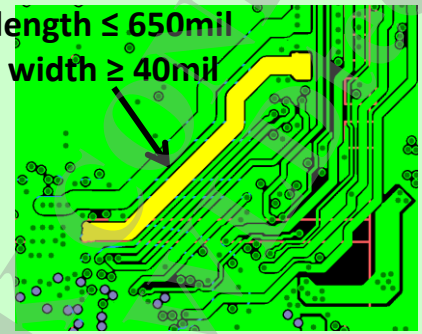
The PCB design examples for wide power traces between "1st group cap" and MT6575VDDK_DVFS :

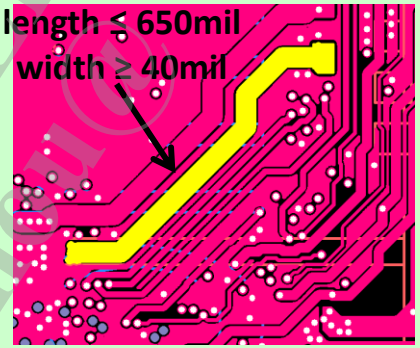


Allocate only one power trace is forbidden !

Suggestion 1

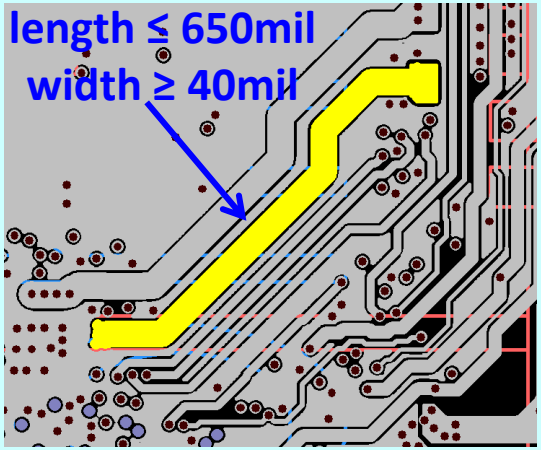


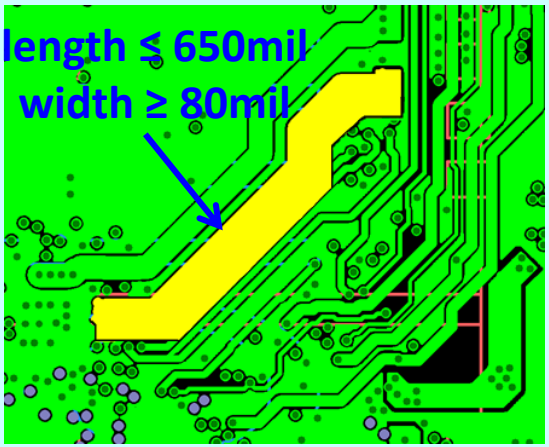




Three parallel traces on three layers

Suggestion 2





Two parallel traces on two layers

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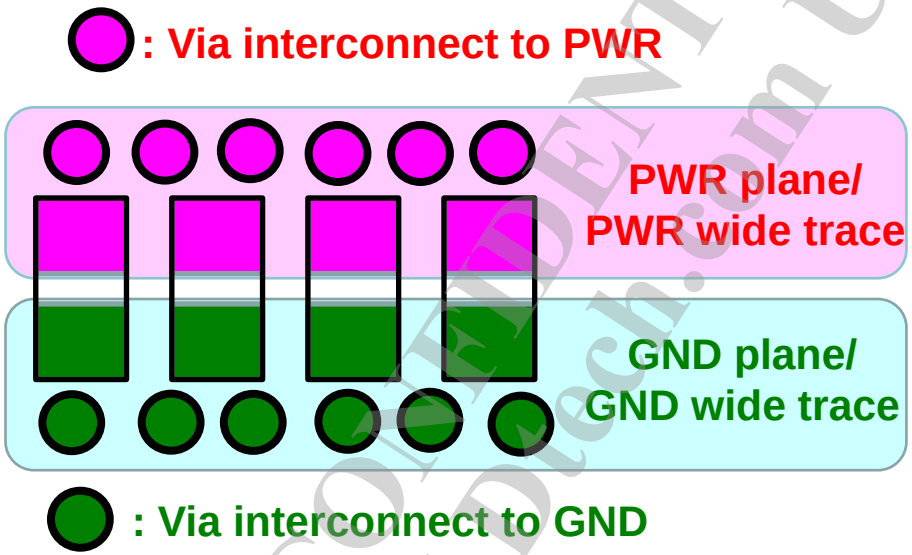
Via Interconnects for CPU PDN



- **Recommendation of PWR/GND via for decoupling capacitors：**

1. The interconnect of vias could easily become the bottleneck of PDN design, so please pay attention to the guidelines for the relevant PWR/GND vias.
2. Next to the decoupling capacitors, allocate PWR and GND vias and connect to the parallel wide power traces.
3. For each decoupling capacitor, it is recommended to allocate one PWR via and one GND via, at least. If there is more spacing, try to allocate more PWR/GND vias.

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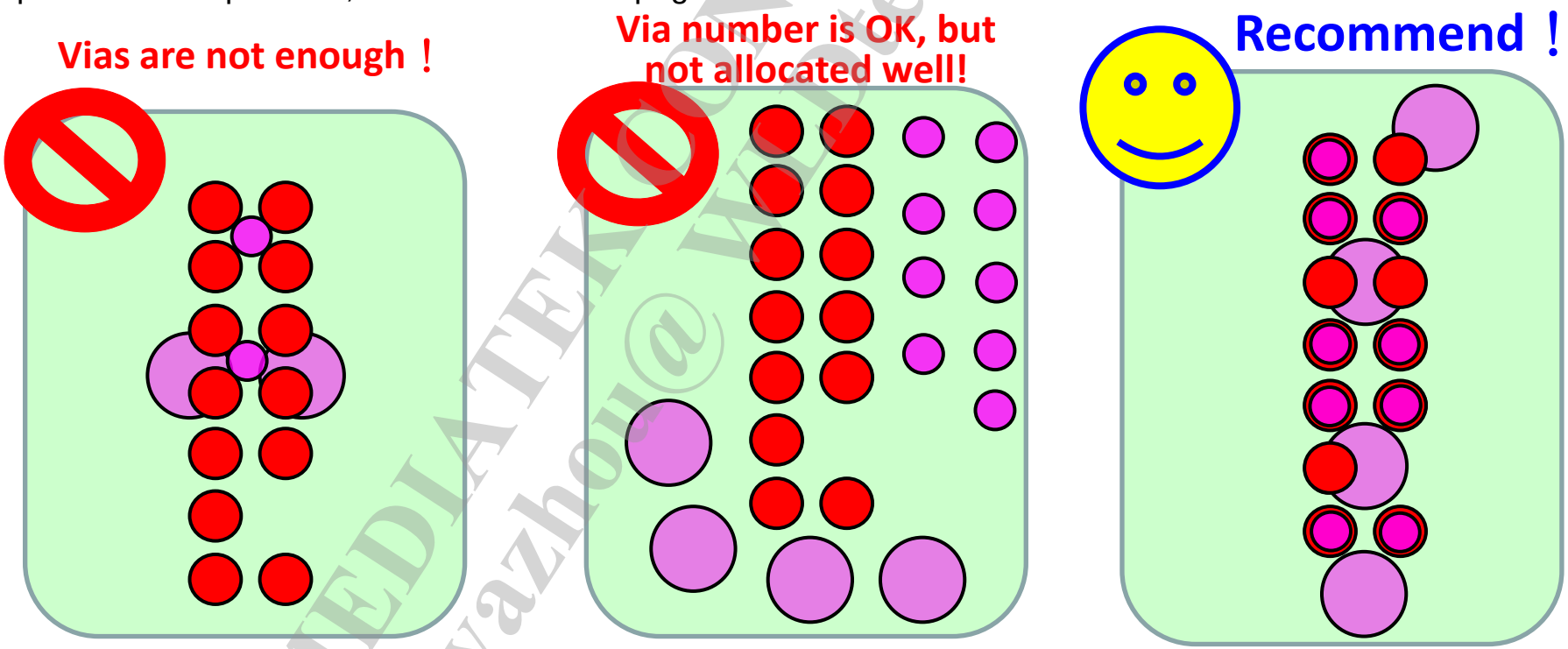
Via Interconnects for CPU PDN (Cont.)

● **Vias guidelines for VDDK_DVFS** (Top view of MT6575 PCB)

1. To allocate enough via holes underneath VDDK_DVFS balls. The minimum requirement of vias is as below: make "DDK_DVFS ball number": “micro vias”: "PTH vias" in a 3:2:1 ratio. Regarding MT6575, The minimum requirement of vias is: 8 micro vias (blind/buried vias) with 4 PTH vias.
2. To allocate as more micro vias as you can, and more than 8 micro vias will be much better. It is recommended to implement "via on ball" design on VDDK_DVFS balls and connect to “wide power trace” and PTH vias. In addition, the PTH vias should be placed within the area averagely, shown as below figures:
3. Besides power vias, pleas also pay attention to the surrounding ground vias and place them as close to the power vias as possible, shown as the next page.



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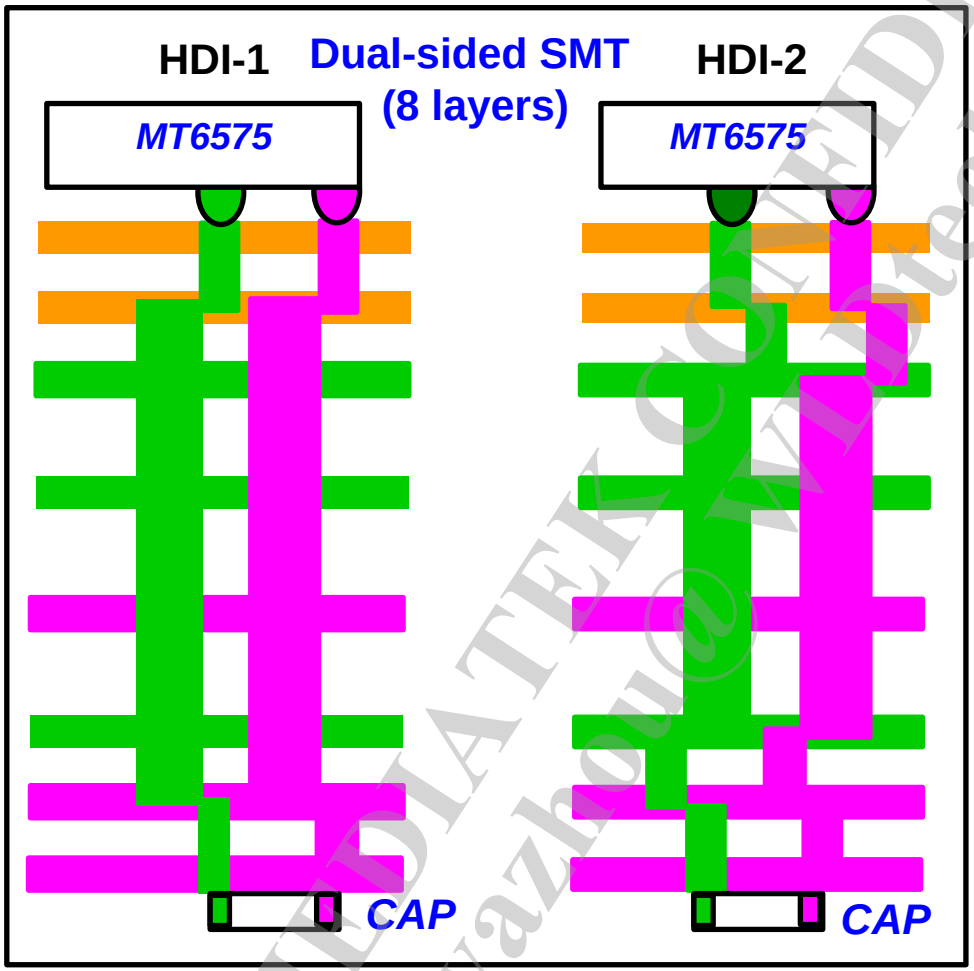
:VDDK_DVFS (PWR balls)

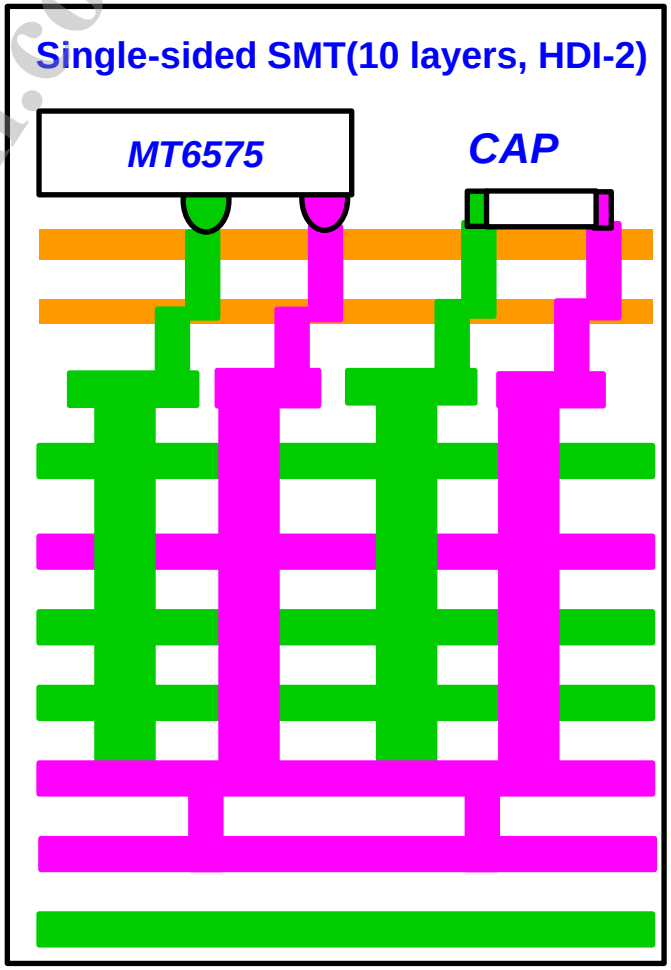
: Micro via (Blind/buried via)

: PTH via

Via Interconnects for CPU PDN (cont.)

1. Besides power vias, please also pay attention to the arrangement of the surrounding ground vias to reduce the inductance of via interconnect, and narrow the "return path“. Make the ground vias as close to power vias as possible, as shown below.
2. The ratio of the GND via vs. PWR via is basically1:1, at least.





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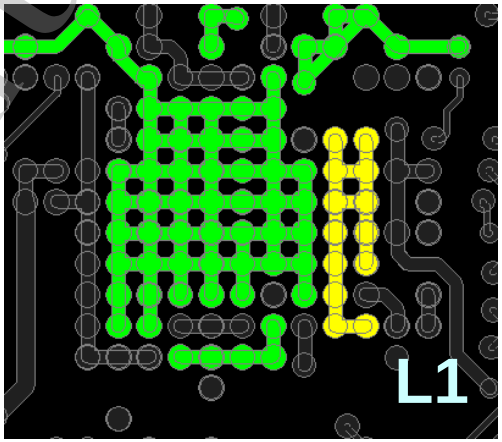
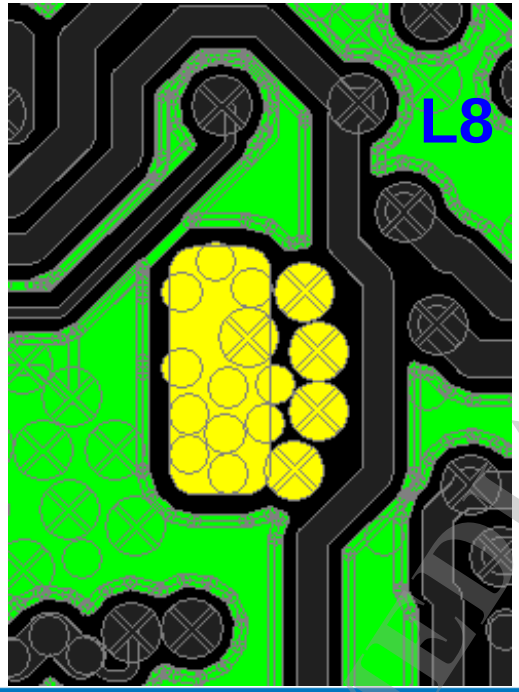
Power GND Signal

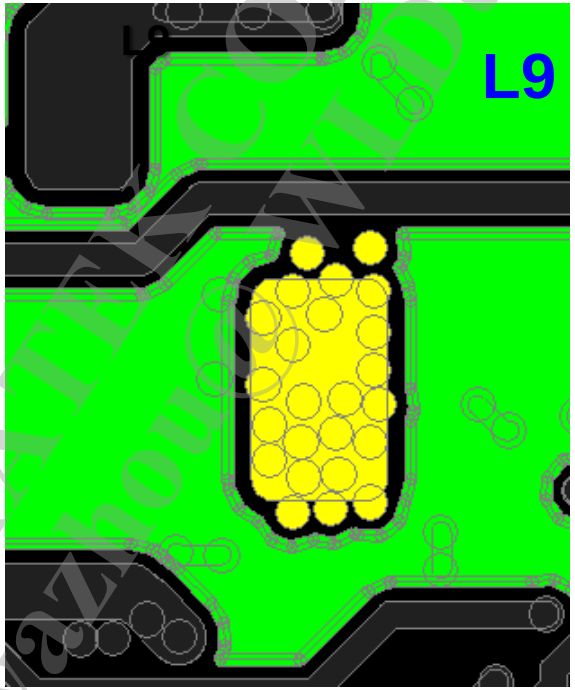
Example of GND/PWR Via Design (Dual-sided SMT)

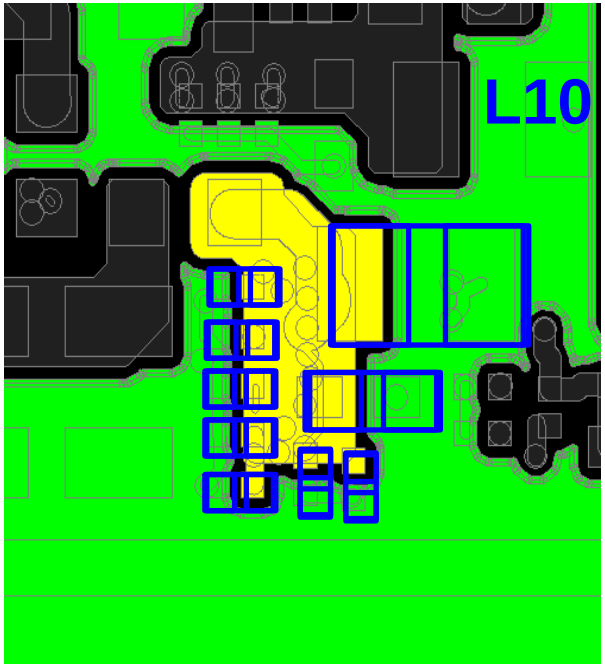
For double-sided SMT, if MT6329 (PMIC), "1st group cap", and "Bottom cap" can be placed just beneath the MT6575, the design can achieve the best PDN design. Besides, please still follow the following specifications:

1. Regarding the PWR and GND via, please make your PCB design in accordance with the instructions of the following pages.
2. It is recommended to allocate 2~3 parallel wide power trace on the way of the interconnect of power via and VDDK_DVFS, shown as below example:









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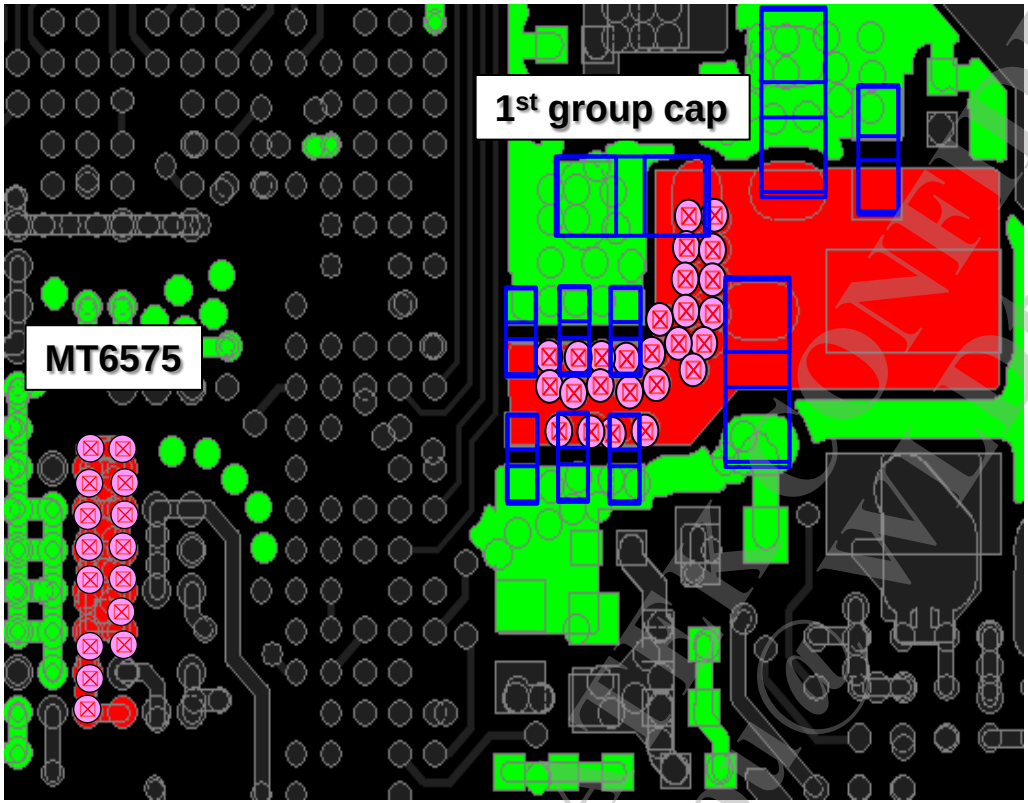
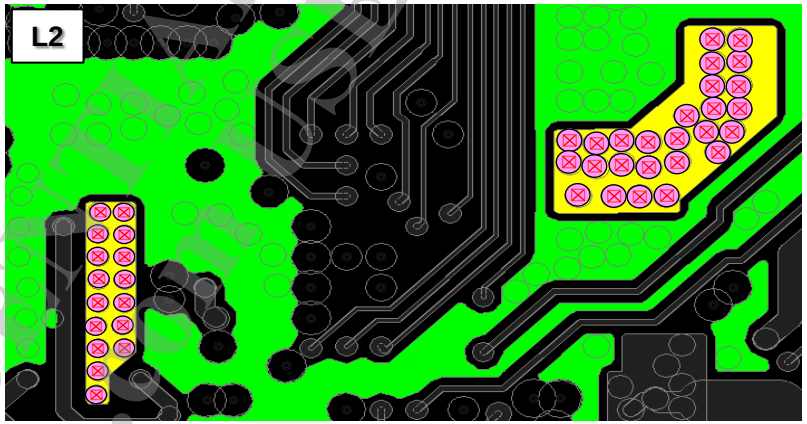
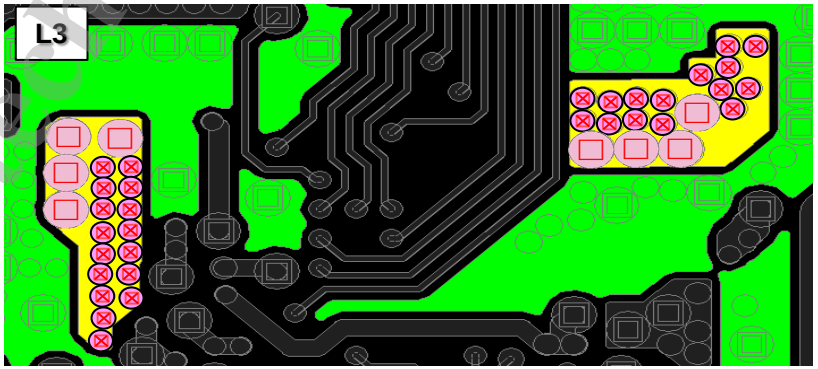
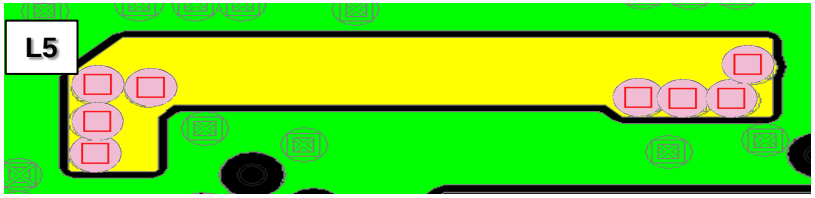
Example of GND/PWR Via Design (single-sided SMT)

L1 (MT6575 and 1st group cap)









:GND balls & vias

: PTH via

: Micro via
(Blind/buried via)

: VDDK_DVFS

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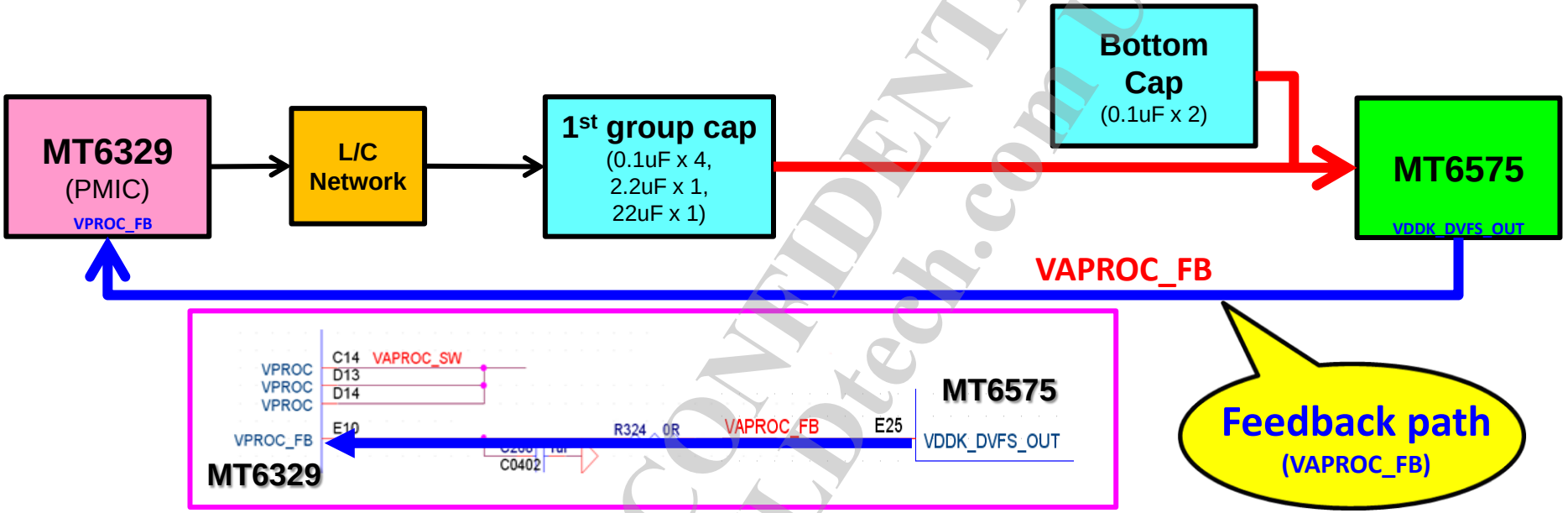
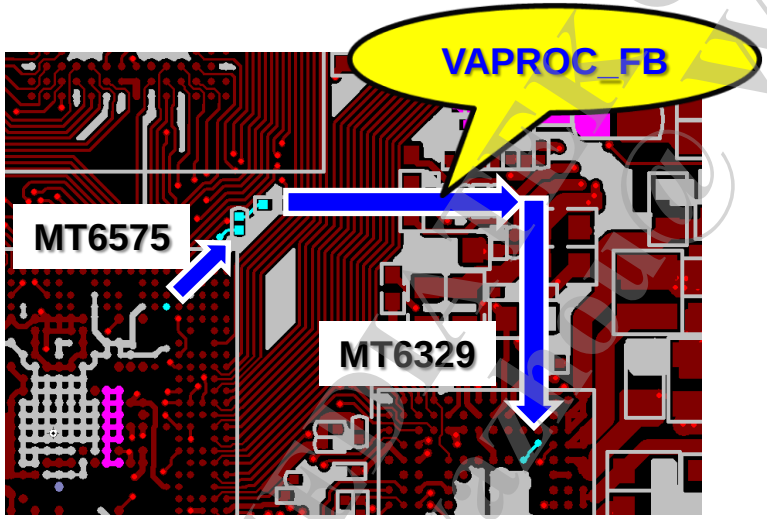
PCB Layout Guidelines for VDDK_DVFS_OUT





There is feedback path, VAPROC_FB, between MT6575 and MT6329 (PMIC). This feedback path is for voltage detection, and, for this path, **ground shielding** is a must to prevent the coupling effect from other signals.

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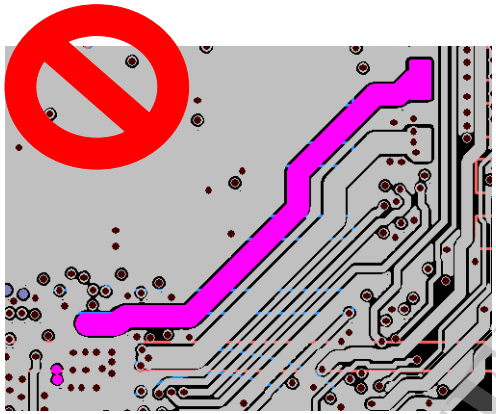
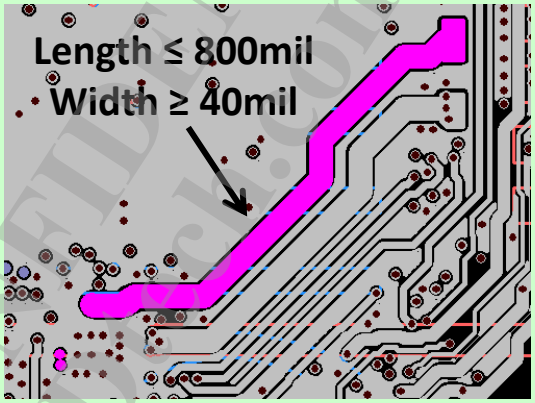
PCB Layout Guidelines for VDDK(VCORE)

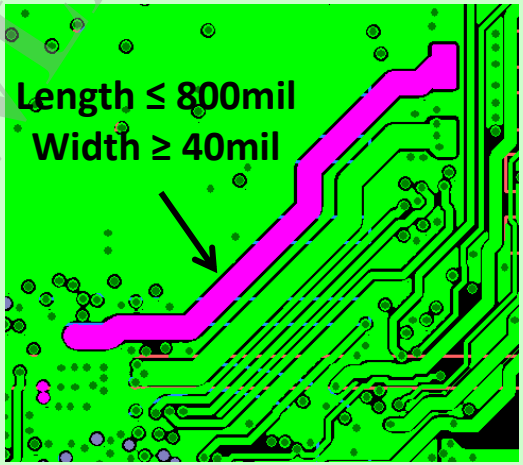
Only one power trace

is not recommended！



Recommend





Two parallel traces on two layers

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Outlines

- Brief of MT6575
- Packaging
  - MT6575 POD
  - MT6575 Footprint design
  - MT6575 floor planning
- General guidelines
  - PCB stack-up recommendation
  - Common Rules and Via Type
  - Placement Notes
  - MT6575 Fan-out recommendation
- **Design guidelines for high-speed digital signals**
  - PDN design for CPU
  - **LPDDR2**
  - LPDDR1
- Others
  - RF - USB - HDMI - MIPI - Charger
  - 32K Crystal - Audio - SIM Card -T-CARD - Camera
  - **MT6620**(BT/FM/WiFi/GPS) **–MT6329**

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MT6575 Ball list for LPDDR2 Interface

Ball	#	Signal Name	Description
C11, A10, D12, B10, C12, B12, B11, D11, A22, D21, D20, B22, E21, C24, A23, A24, D8, C7, B9, B8, A7, D9, A9, C8, D23, C23, D24, B24, A26, D25, B25, C27	32	**ED[0:31]**	Data bus **(DQ)**
A13, C15, A14, B17, A17, B18, D17, C19, B21, B19	1	**EA[0:9]**	Command/Address inputs **(C/A)**
A11, B23, B7, B26	4	**DQM[0:3]**	Data mask**(DM)**
C16 A16 D16	1	**ECKE0** **/ECS0** **/ECS1**	Clock enable**(CE)** Chip select**(CS)**
E12, E20, E9, E24 E13, E19, E10, E23	8	**EDQS[0:3]** **/EDQS[0:3]**	Differential data strobe pair **(DQS)**
E17 E16	2	**EDCLK** **/EDCLK**	Differential clock pair **(CLK)**
F8, G11, F12, F14, F15, G15, F16, F17, G17, F18, F21, F23	12	**DVDD_EMI** (DVDD12_EMI)	Provide LPDDR2 DRAM controller I/O power. 1.2V+/-10% Maximum current 400mA
D19	1	**EVREF**	Reference voltage

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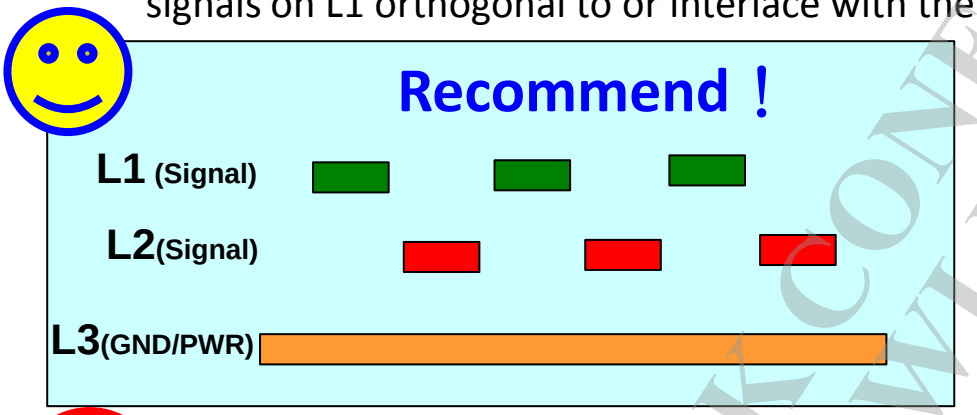
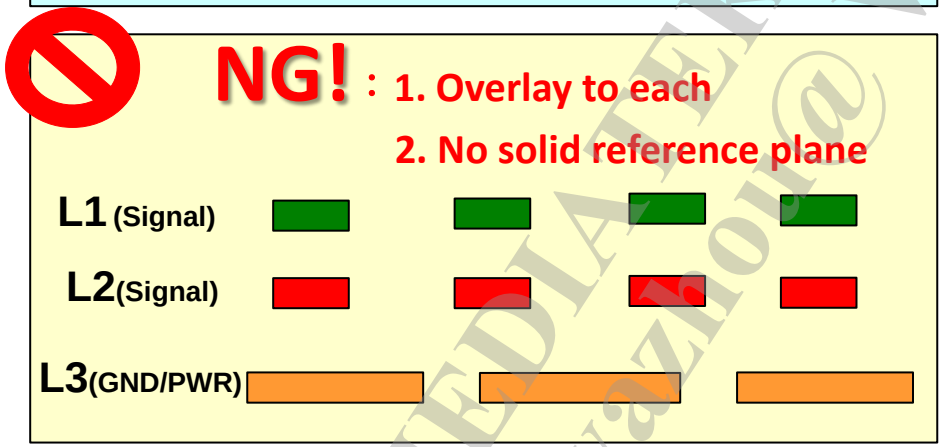
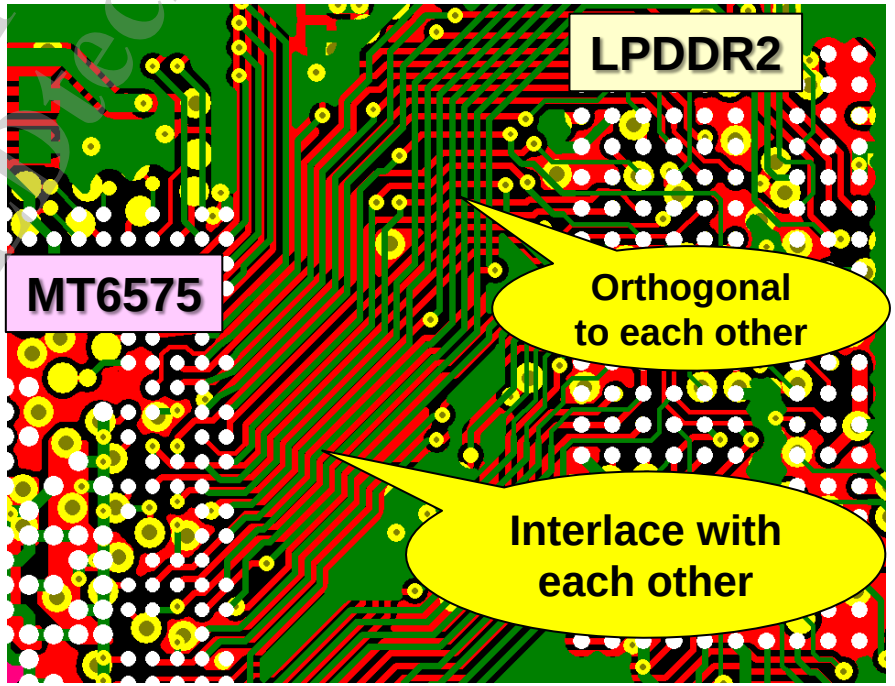
PCB Design Guidelines for DQ, C/A, DM, CE & CS

PCB layout guidelines:

1. Make the routing length of memory bus between MT6575 and LPDDR2 MCP as short as possible.
2. Trace width/spacing:
   1) Underneath MT6575: 3mils/3mils partially.
   2) Others (breakout area): 4mils/4mils.
3. To rout most of the memory signals on L1 & L2 with a solid reference plane. Besides, make the signals on L1 orthogonal to or interlace with the signals on L2, as shown below:







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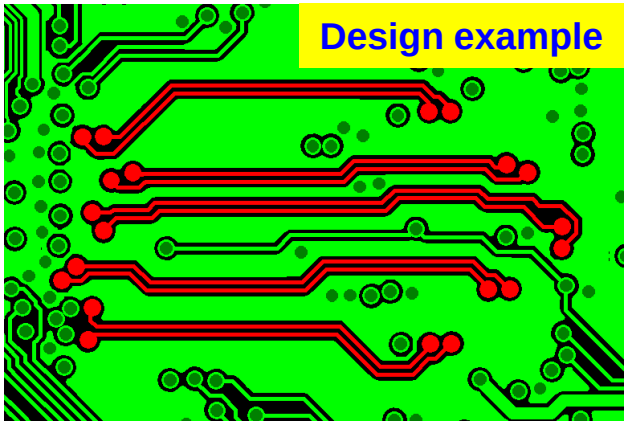
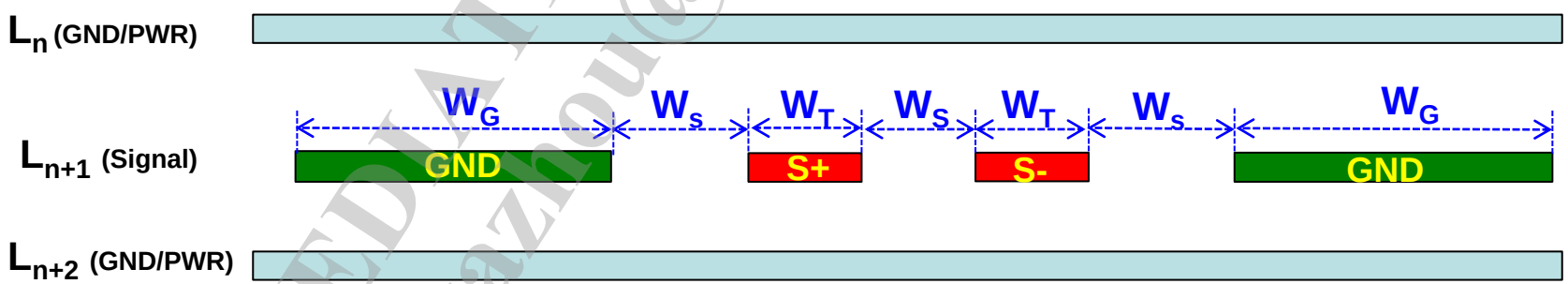
PCB Design Guidelines for DQS, CLK

Ball	#	Signal Name	Description
E12, E20, E9, E24 E13, E19, E10, E23	8	**EDQS[0:3]** **/EDQS[0:3]**	Differential data strobe pair **(DQS)**
E17 E16	2	**EDCLK** **/EDCLK**	Differential clock pair **(CLK)**



PCB layout guidelines:

1. **DQS and CLK are differential pairs, respectively：**
   1) **For each differential pair, make them routing in parallel。**
   2) **Route the differential pairs in inner layer with solid reference planes and ground shielding。**
2. **Trace width/spacing guidelines：W_T=W_S= 4 mils，W_G ≥ 10 mils。**



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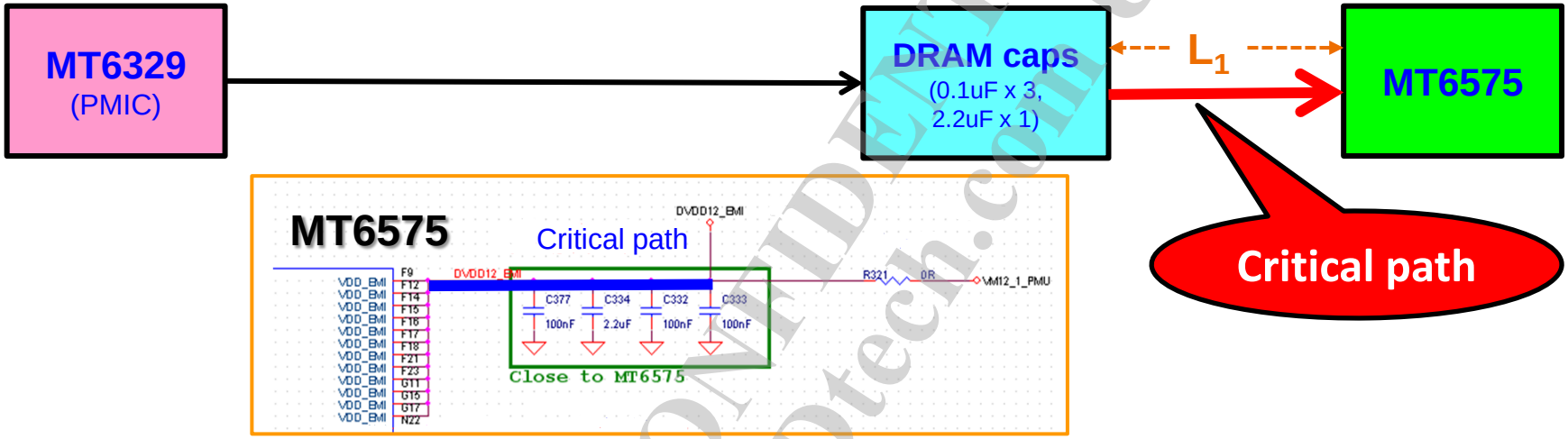
PCB Layout Guidelines for DVDD12_EMI



1. The PDN network stars from the output pin of MT6329 (PMIC) through the decoupling capacitors (DRAM caps), and connect to the MT6575 chip.
2. The “critical path” is defined as the path between the "DRAM caps" and MT6575. It is strongly recommended to follow below PCB layout guideline for this “critical path”.
3. There are three 0.1uF, and one 2.2uF decoupling capacitors for "DRAM caps“, and place them as close to DVDD12_EMI of MT6575 as possible.
4. L_1 is defined as the path between the "DRAM caps" and MT6575 DVDD12_EMI. Make the length of L_1 as short as possible, and no more than 150mil. In addition, other PCB layout guidelines are as follows:
   1) Double-sided SMT: Please "DRAM caps” underneath the balls of MT6575 DVDD12_EMI, and allocate appropriate volume of via. Regarding the critical path, please follow the guidelines in p.35 ~ p.37 and refer to the design example in p.38.
   2) Single-sided SMT: (recommend only for HDI-2 PCB): Allocate the "DRAM caps" as close to MT6575 as possible. Regarding the critical path, please follow the guidelines in p.35 ~ p.37 and refer to the design example in p.39.

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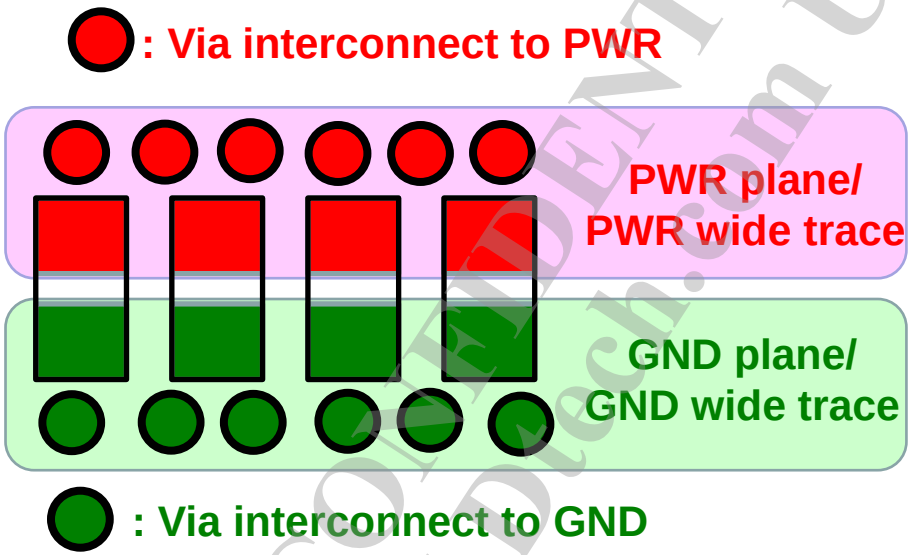
Via Interconnects for DVDD12_EMI



- **Recommendation of PWR/GND via for decoupling capacitors：**

1. The interconnect of vias could easily become the bottleneck of PDN design, so please pay attention to the related layout guidelines.
2. Allocate PWR and GND vias close to the decoupling capacitors and connect to the critical path or DVDD12_EMI of MT6575.
3. For each decoupling capacitor, it is recommended to allocate one PWR via and one GND via, at least. If there is enough space, try to allocate more PWR/GND via.

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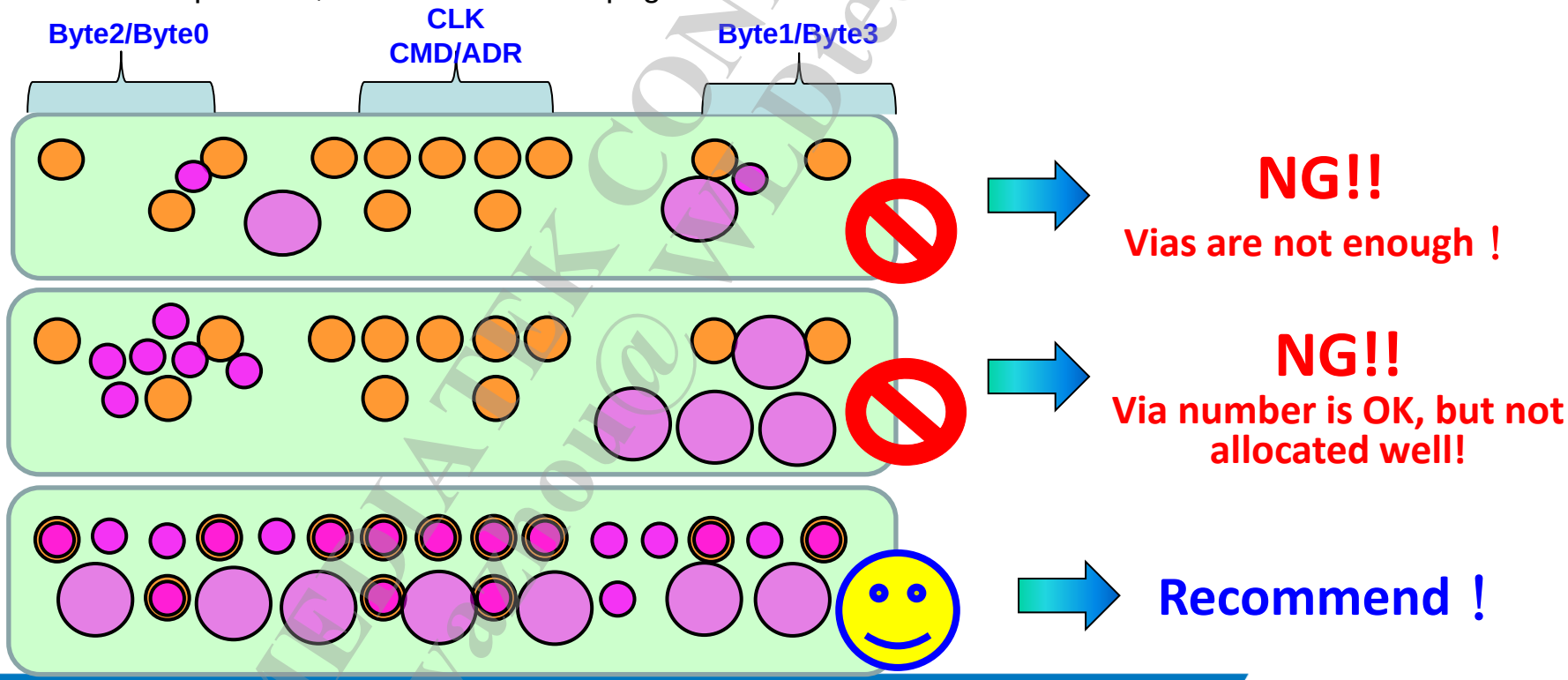
Via Interconnects for DVDD12_EMI (Cont.)

● **Vias guidelines for DVDD12_EMI (Top view of MT6575 PCB)**

1. To allocate enough via holes underneath DVDD12_EMI balls. The minimum requirement of vias is as below: make " DVDD12_EMI ball number": "micro vias": "PTH vias" in a 2:1.5:1 ratio. Regarding MT6575, The minimum requirement of vias is: 9 micro vias (blind/buried vias) with 6 PTH vias.
2. To allocate as more micro vias as you can, and more than 9 micro vias will be much better. It is recommended to implement "via on ball" design on DVDD12_EMI balls and connect with the "critical path" and PTH vias. In addition, the PTH vias should be placed within the area averagely, shown as below figures:
3. Besides power vias, pleas also pay attention to the surrounding ground vias and place them as close to the power vias as possible, shown as the next page.



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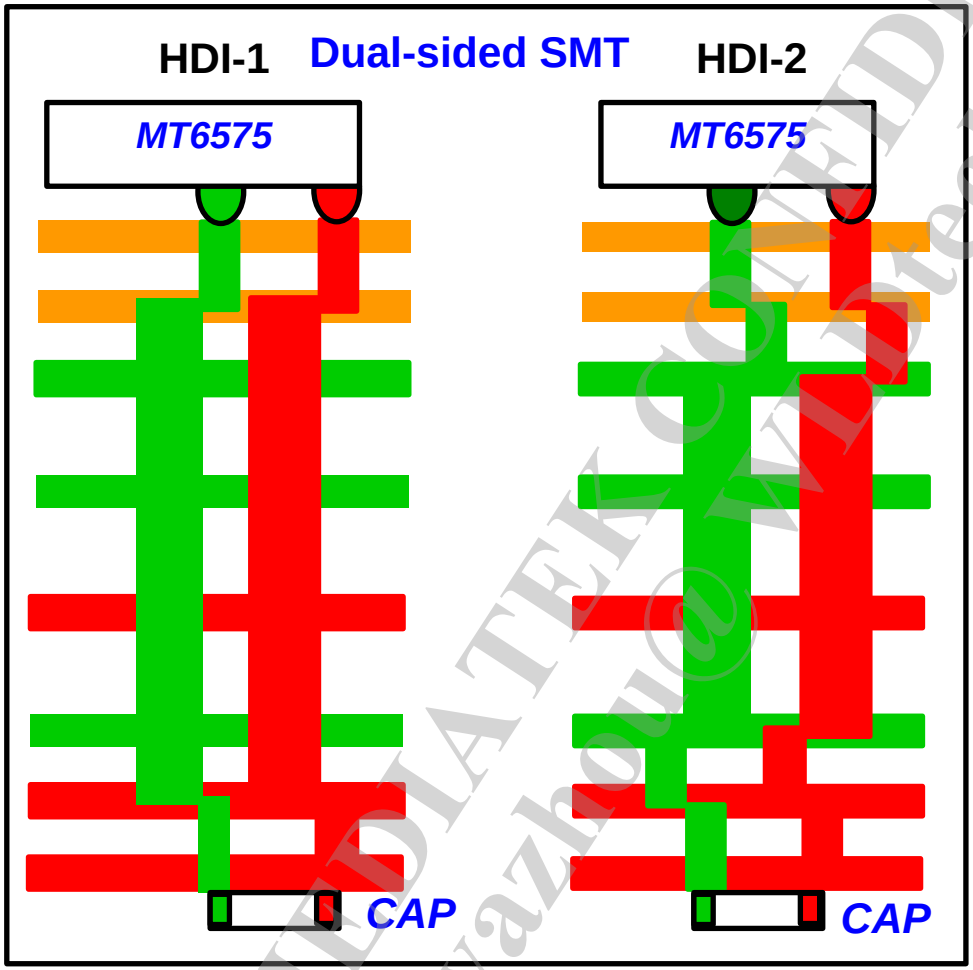
:DVDD12_EMI (PWR balls)

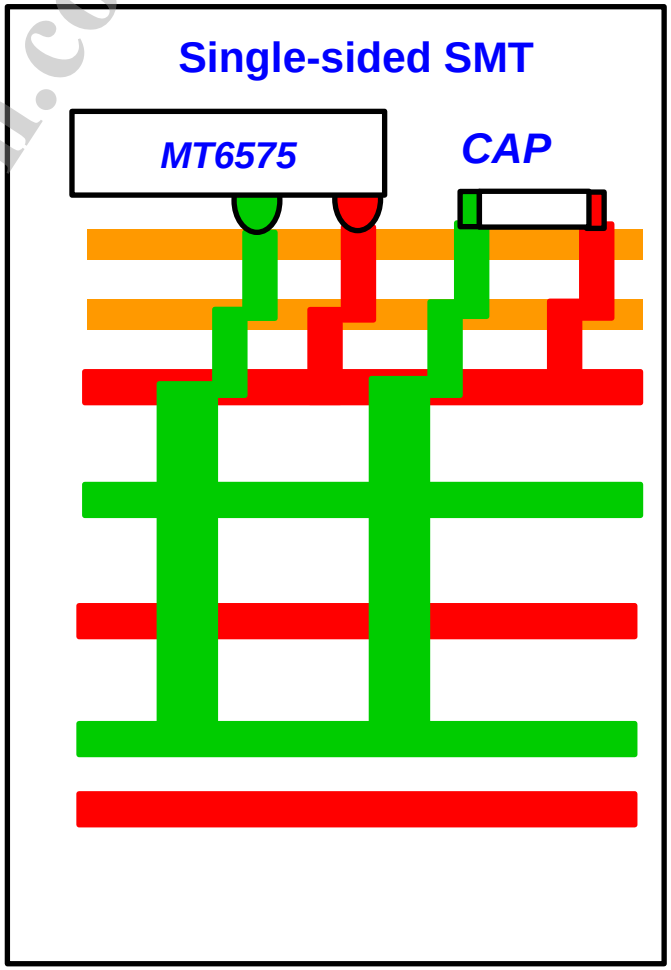
: Micro via (Blind/buried via)

: PTH via

Via Interconnects for DVDD12_EMI (cont.)

1. Besides power vias, please also pay attention to the arrangement of the surrounding ground vias to reduce the inductance of via interconnect, and narrow the "return path“. Make the ground vias as close to power vias as possible, as shown below.
2. The ratio of the GND via vs. PWR via is basically1:1, at least.





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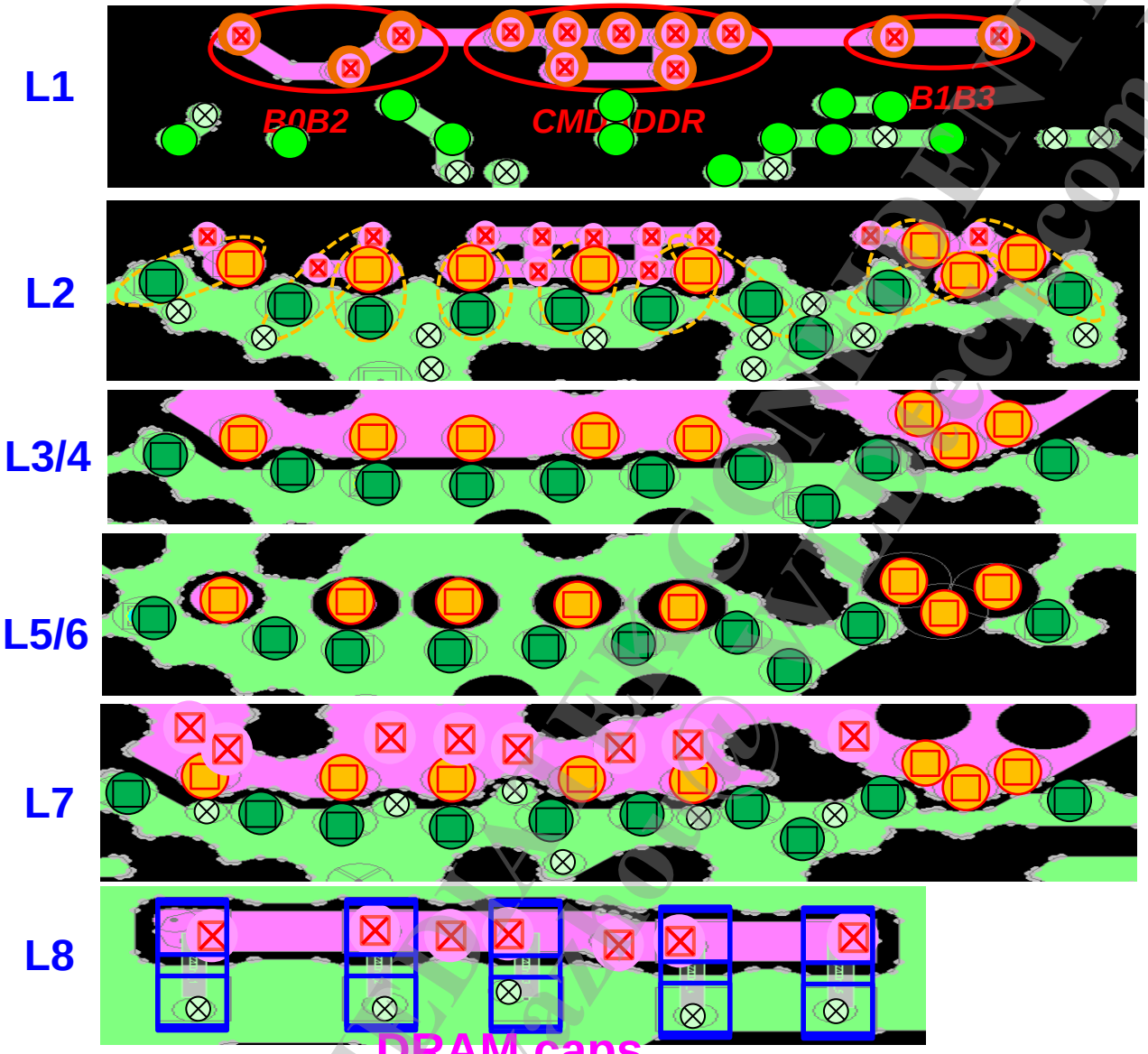
Power GND Signal

Design Example of Via Interconnects for DVDD12_EMI



Dual-sided SMT

: DVDD12_EMI balls

: Micro via
(Blind/buried via)

: PTH via

:GND balls

: Micro via
(Blind/buried via)

: PTH via

: DRAM caps

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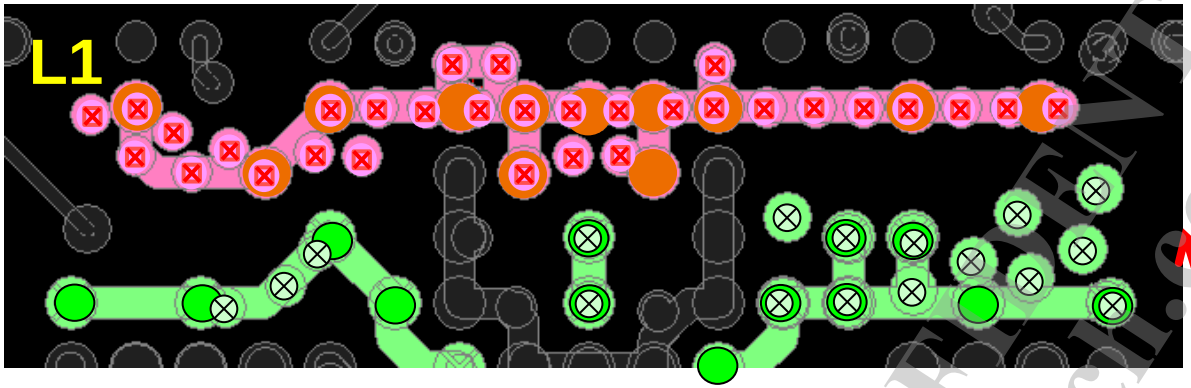
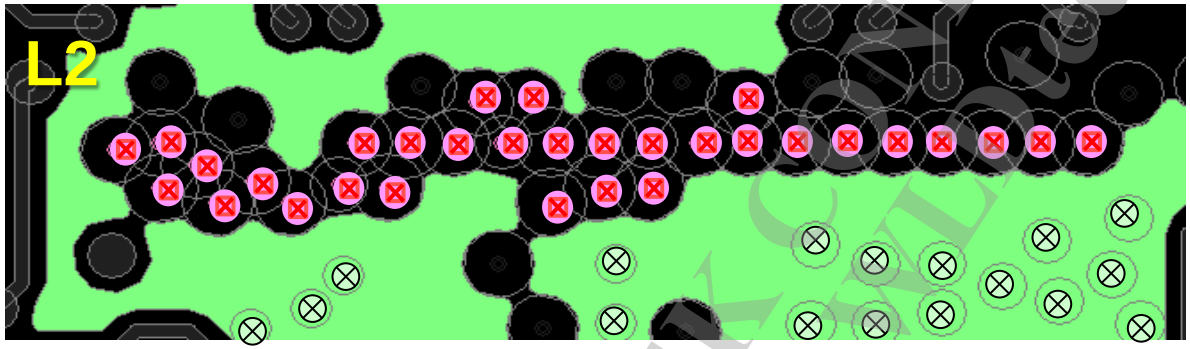
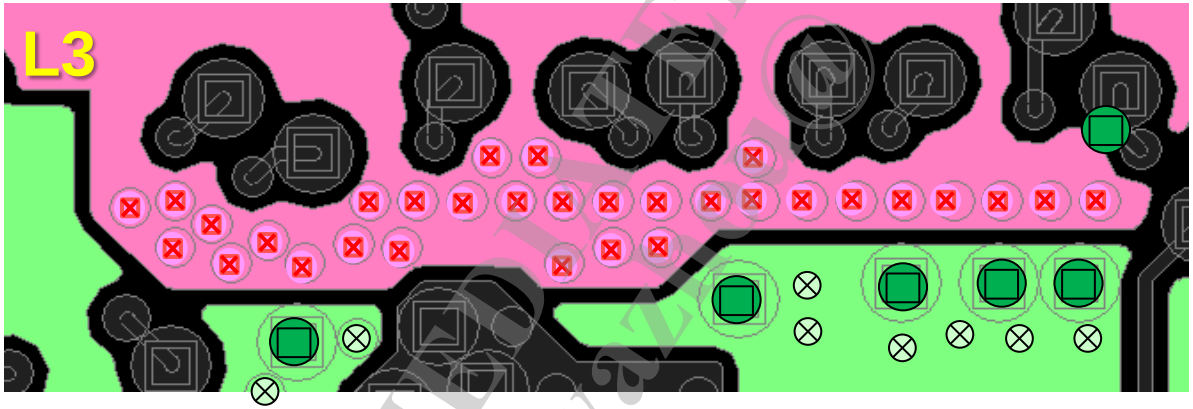
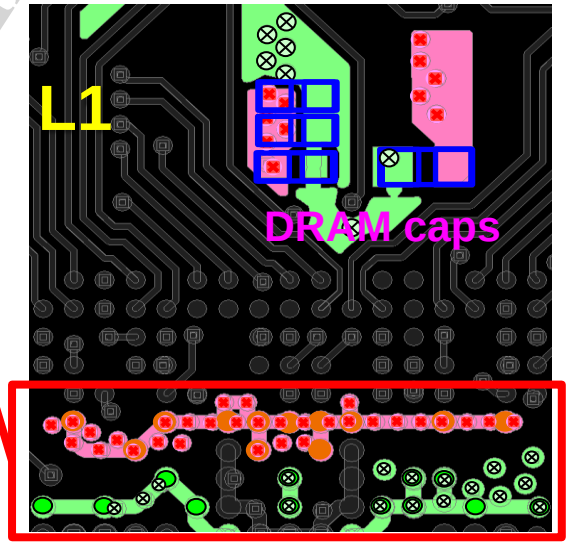
Design Example of Via Interconnects for DVDD12_EMI (cont.)

Single-sided SMT









: DVDD12_EMI balls

: Micro via
(Blind/buried via)

: PTH via

:GND balls

: Micro via
(Blind/buried via)

: PTH via

: DRAM caps

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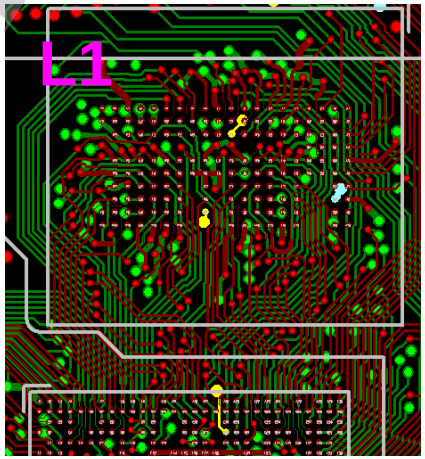
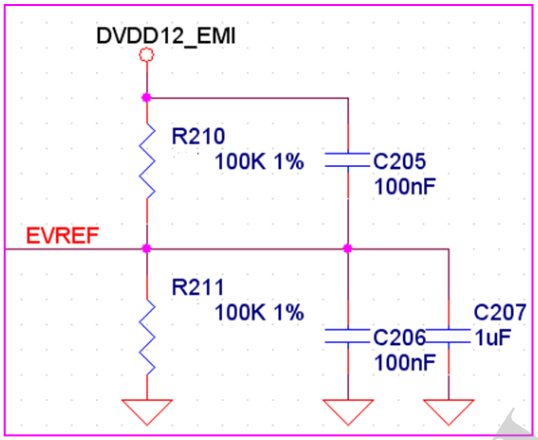
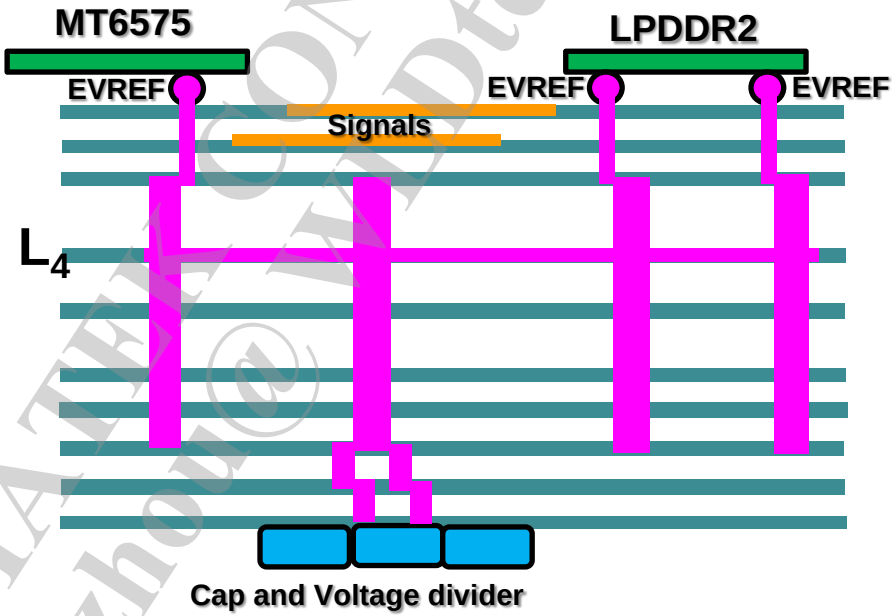
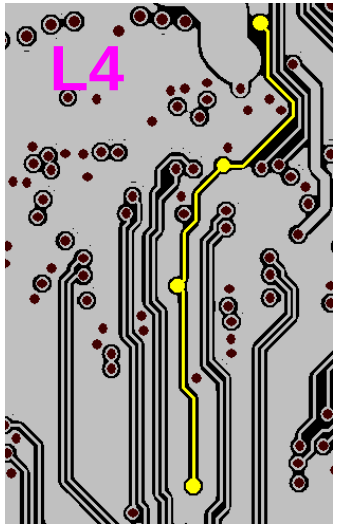
LPDDR2 EVREF Guideline

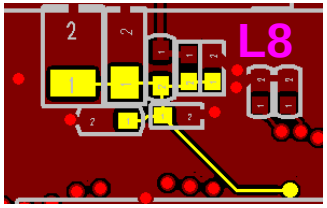
1. The resistor divider for EVREF is 100KΩ 1% resistor.
2. EVREF needs ground shielding and don't make it adjacent to noisy signals, such as EDQ, EDQS, EDCLK, DQM, or EA…etc.











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  - MT6575 floor planning
- General guidelines
  - PCB stack-up recommendation
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  - Placement Notes
  - MT6575 Fan-out recommendation
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  - PDN design for CPU
  - LPDDR2
  - **LPDDR1**
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  - 32K Crystal - Audio - SIM Card -T-CARD - Camera
  - **MT6620**(BT/FM/WiFi/GPS) **–MT6329**

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MT6575 Ball List for LPDDR1 Interface

Ball	#	Signal Name	Description	Grouping
C11, A10, D12, B10, C12, B12, B11, D11, A22, D21, D20, B22, E21, C24, A23, A24, D8, C7, B9, B8, A7, D9, A9, C8, D23, C23, D24, B24, A26, D25, B25, C27	32	ED[0:31]	Data bus	**DQ**
A11, B23, B7, B26	4	DQM[0:3]	Data mask	
E12, E20, E9, E24	8	EDQS[0:3]	Data strobe	**DQS**
C16 D17, A17 C15 A16 B18	6	ECKE0 /ECS0,1 ECAS# ERAS# EWR#	Clock enable Chip select Column select Row select Write enable	**C/A**
B21, A19, B20, C19,B13, B15, B14, A14, D15, A13, B19, D16, B17, C20,	14	EA[0:13]	Address inputs	
A20, B16	2	EBA0,1	Bank address inputs	
E17 E16	2	EDCLK /EDCLK	Differential clock pair	**CLK**
F8, G11, F12, F14, F15, G15, F16, F17, G17, F18, F21, F23	12	DVDD_EMI (DVDD12_EMI)	Provide LPDDR1 DRAM controller I/O power. 1.8V+/-10% Maximum current 400mA	**LPDDR1_PWR**

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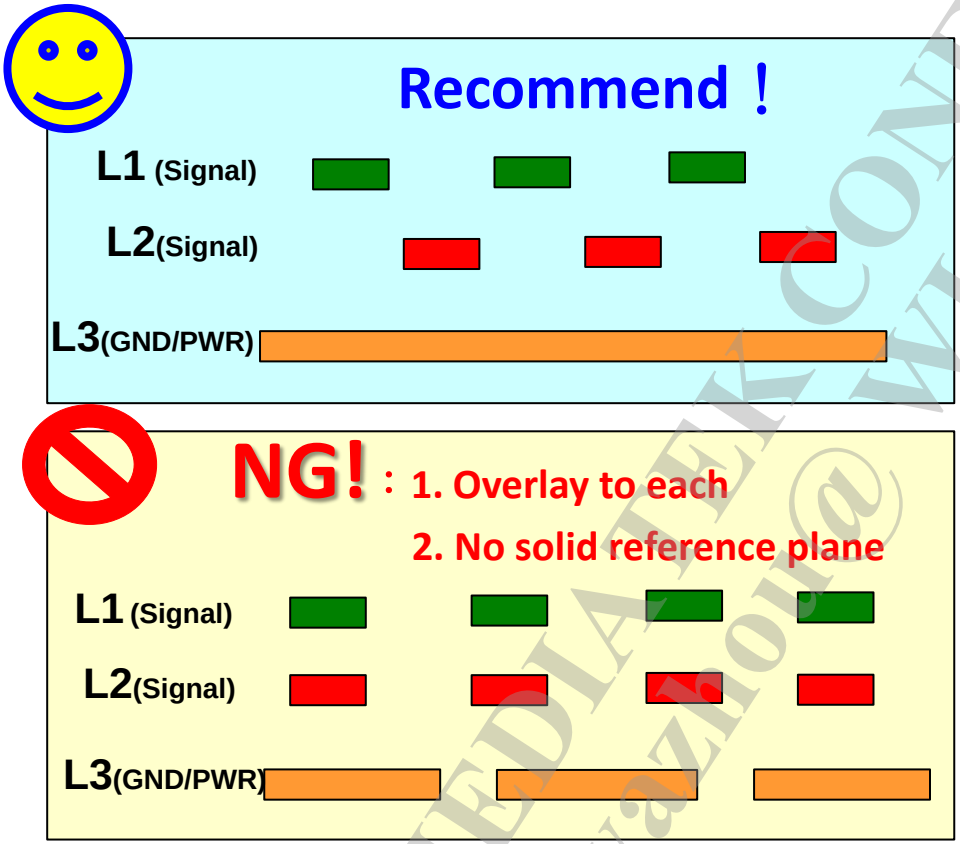
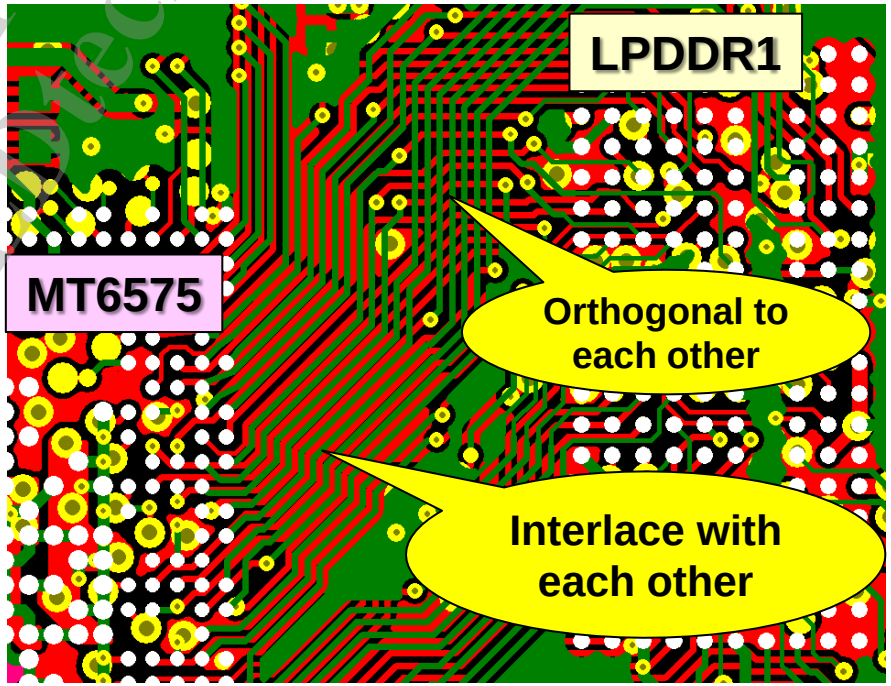
PCB Design Guidelines for DQ, DQS, C/A

PCB layout guidelines:

1. Make the routing of memory bus between MT6575 and LPDDR1 MCP as short as possible.
2. Trace width/spacing:
   1) Underneath MT6575: 3mils/3mils partially.
   2) Others(breakout area): 4mils/4mils.
3. To rout most of the memory signals on L1 & L2 with a solid reference plane. Besides, make the signals on L1 orthogonal to or interlace with the signals on L2, as shown below:





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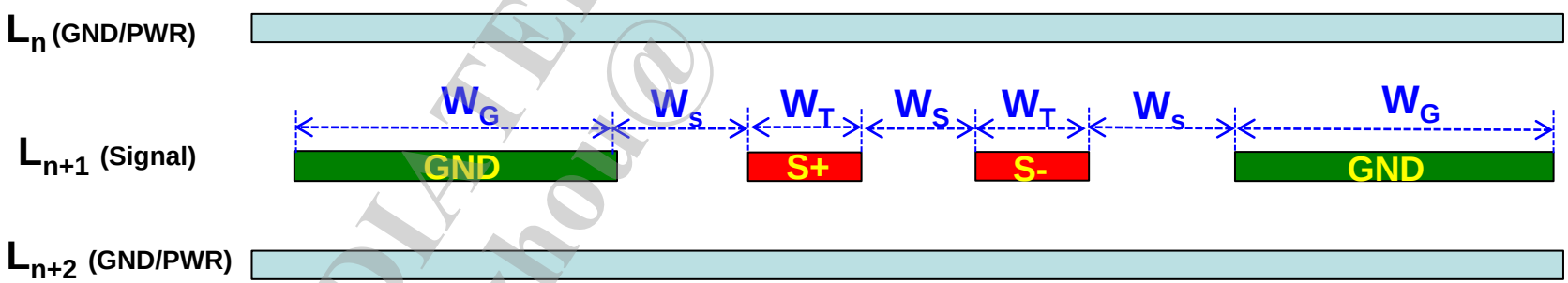
PCB Design Guidelines for CLK

Ball	#	Signal Name	Description	Grouping
E17 E16	2	EDCLK /EDCLK	Differential clock pair	CLK

PCB layout guidelines:

1. CLK is a differential signal pair：
   1) For each differential pair, make them routing in parallel.。
   2) Route the differential pairs in inner layer with solid reference planes and ground shielding。
2. Trace width/spacing guidelines：W_T=W_S= 4 mils，W_G ≥ 10 mils。



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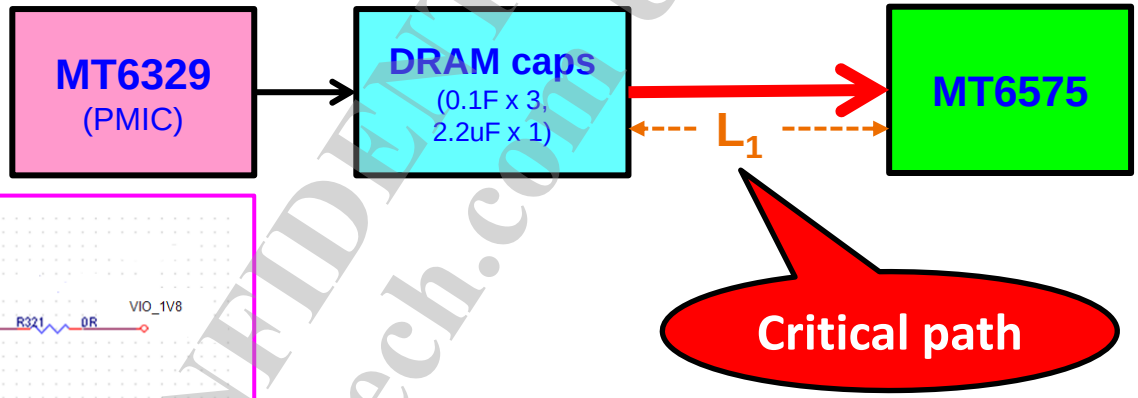
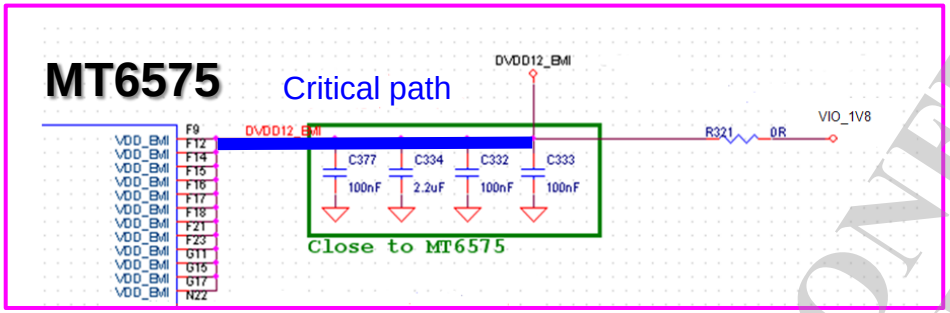
PCB Layout Guidelines for DVDD12_EMI





1. The operating voltage of LPDDR1 is different from LPDDR2. For LPDDR2, it is 1.2V. However, for LPDDR1, DVDD12_EMI = 1.8V.
2. The PDN network stars from the output pin of MT6329 (PMIC) through the decoupling capacitors (DRAM caps), and connect to the MT6575 chip.
3. The critical path is defined as the path between the "DRAM caps" and MT6575. It is recommended to follow below PCB layout guideline.
4. There are three 0.1uF, and one 2.2uF decoupling capacitors for "DRAM caps“, and place them as close to DVDD12_EMI as possible.
5. L_1 is defined as the path between the "DRAM caps" and MT6575 DVDD12_EMI, and try to make the length of L_1 as short as possible. In addition, other PCB layout guidelines are as follows:
   1) Double-sided SMT: Please "DRAM caps” underneath the balls of MT6575 DVDD12_EMI, and allocate appropriate volume of via.
   2) Single-sided SMT: (recommend only for HDI-2 PCB): Allocate the "DRAM caps" as close to MT6575 as possible.
6. Make the relevant PWR/GND vias not too far from DVDD12_EMI balls or "DRAM caps" .

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  - **MT6620**(BT/FM/WiFi/GPS) –**MT6329**

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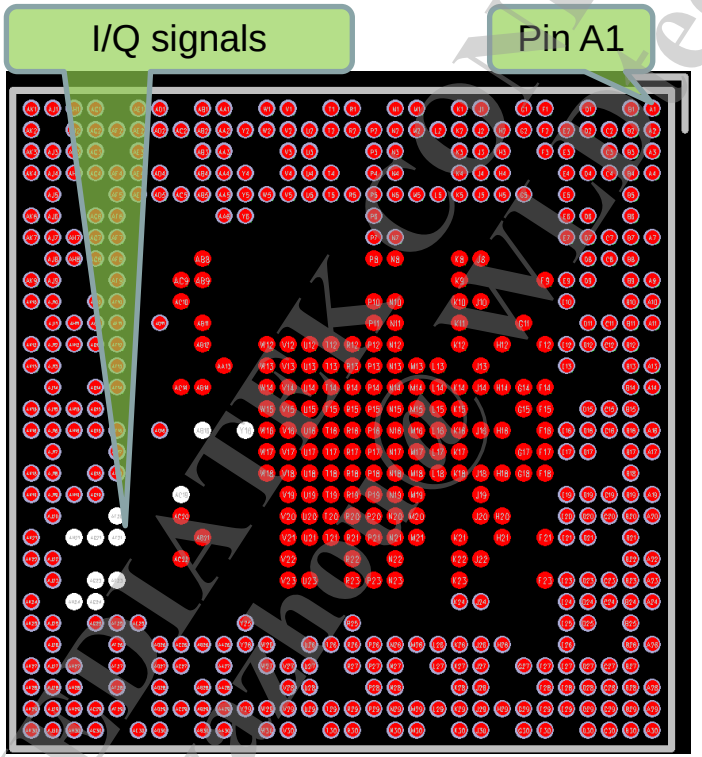
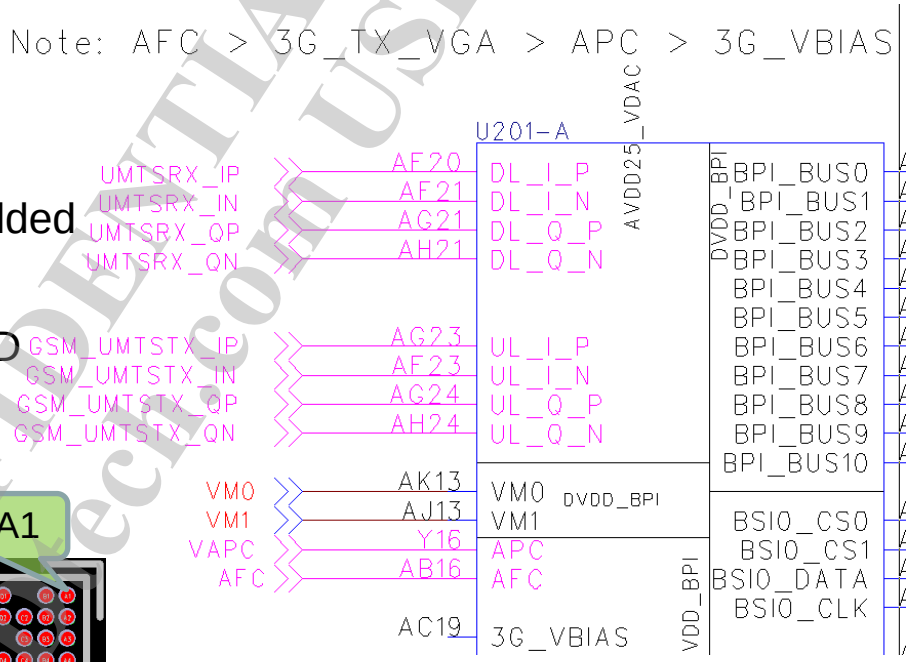
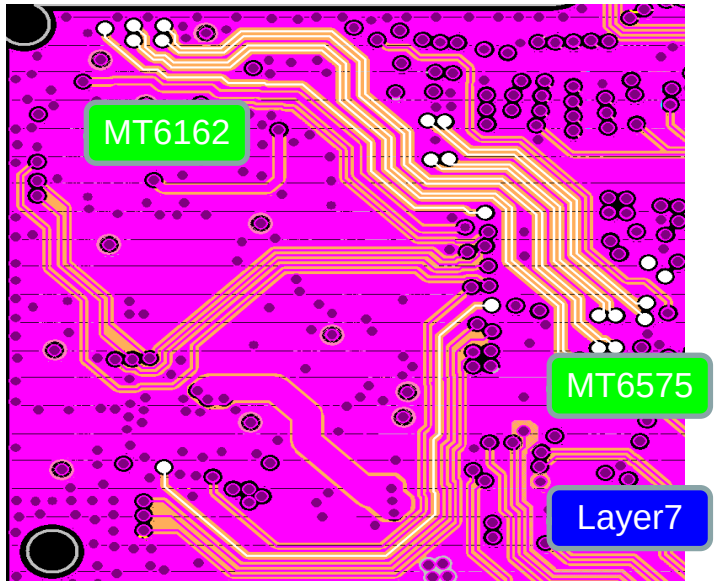
MT6575 RF(1/5)

- Differential pair of I/Q signals must be well shielded by GND(adjacent and up/down layers).
- APC/AFC signals must be well shielded by GND respectively(adjacent and up/down layers).

PCB NET NAME	IC Ball Name
UMTSRX_IP	DL_I_P
UMTSRX_IN	DL_I_N
UMTSRX_QP	DL_Q_P
UMTSRX_QN	DL_Q_N
GSM_UMTSTX_IP	UL_I_P
GSM_UMTSTX_IN	UL_I_N
GSM_UMTSTX_QP	UL_Q_P
GSM_UMTSTX_QN	UL_Q_N
VAPC	APC
AFC	AFC







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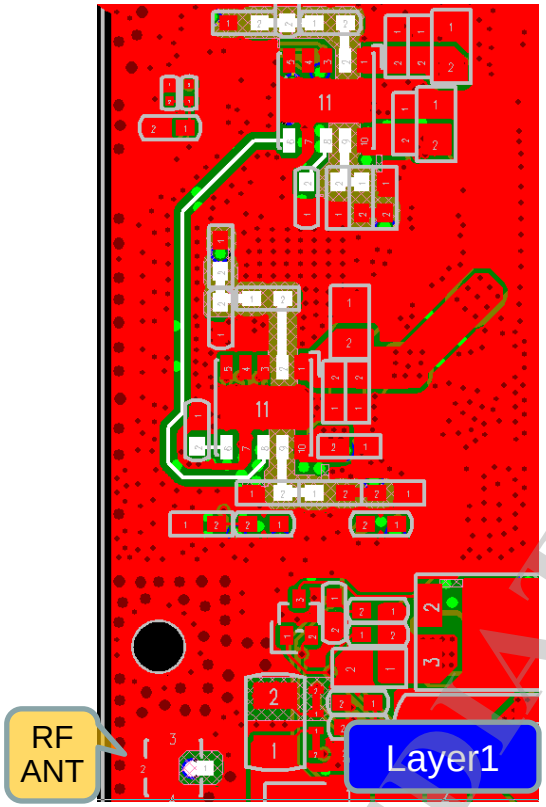
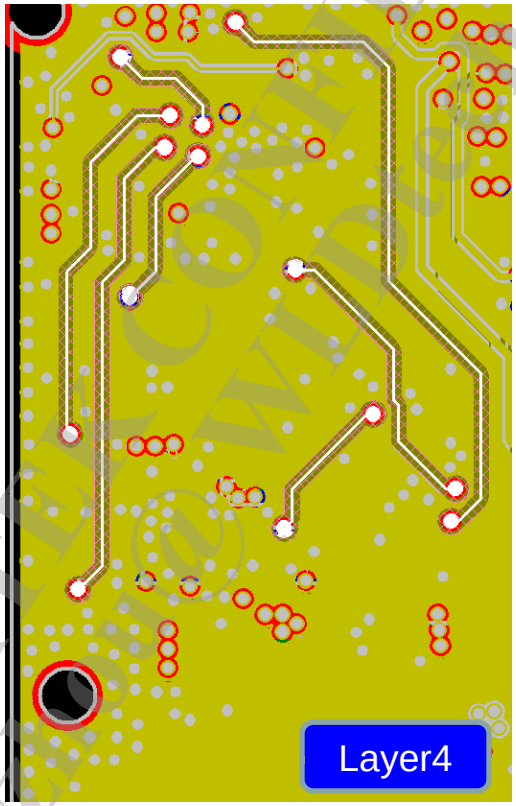
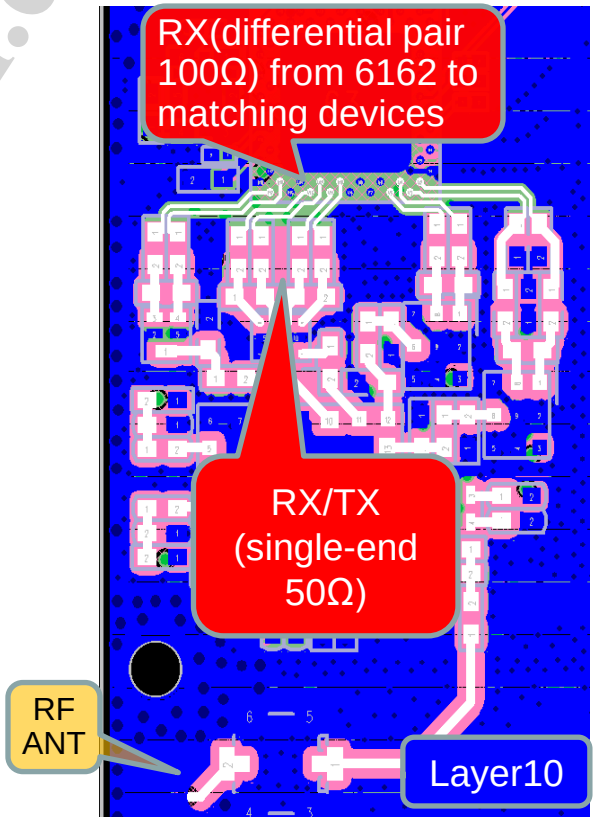
MT6575 RF(2/5)

- Matching circuits of Duplexer/SAW/RX should be placed close to LNA(MT6162); 2G/3G PA should be as far away from LNA as possible; Thermal sensor should be placed close to 3G PA.
- Impedance control is important for RF signals. TX/PDET/CPL(single-end 50Ω) and RX(single-end 50Ω or differential 100Ω).







Please refer to the table 1(next page) in page 50 for RF impedance signals layout.

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MT6575 RF (3/5)

- Table1 is the impedance recommendation of MTK reference PCB design(10L HDI+1), please check the impedance control rule with your PCB vendor for different PCB stack up.

Table1

Layer	Layer denfiniton	50 ohm+/-10%	90 ohm+/-10%	100 ohm+/-10%	50 ohm+/-10%
1	TOP	12MIL---- 48.9OHM(REFL3)	4/5/4MIL---- 88.15OHM(REFL2)	4/8/4MIL---- 95.32OHM(REFL2)	4.5MIL---- 49.03OHM(REFL2)
2	IN1				
3	GND				
4	IN2	4MIL---- 49.82OHM(REFL3/L6)	4/5/4MIL---- 88.3OHM(REFL3/L6)	4/9/4MIL---- 95.91OHM(REFL3/L6)	
5	IN3				
6	GND				
7	IN4	4MIL---- 49.82OHM(REFL5/L8)	4/5/4MIL---- 88.15OHM(REFL5/L8)	4/9/4MIL---- 95.91OHM(REFL5/L8)	
8	GND				
9	IN5				
10	BOTTOM	12MIL---- 48.9OHM(REFL8)	4/5/4MIL---- 88.15OHM(REFL9)	4/8/4MIL---- 95.32OHM(REFL9)	4.5MIL---- 49.03OHM(REFL9)

- 100 ohm：RF signals from MT6162 to the duplexer，MIPI differential pair, HDMI differential pair.
- 90 ohm：USB differential pair
- 50 ohm：all ANT(RF/WIFI/GPS/BT/FM)，RF RX/TX(from matching devices to ANT)

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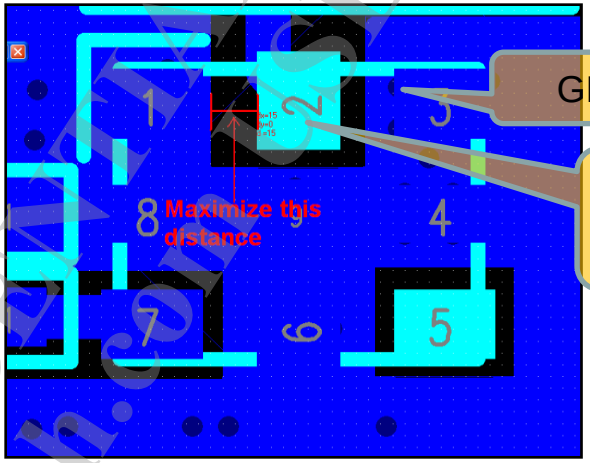
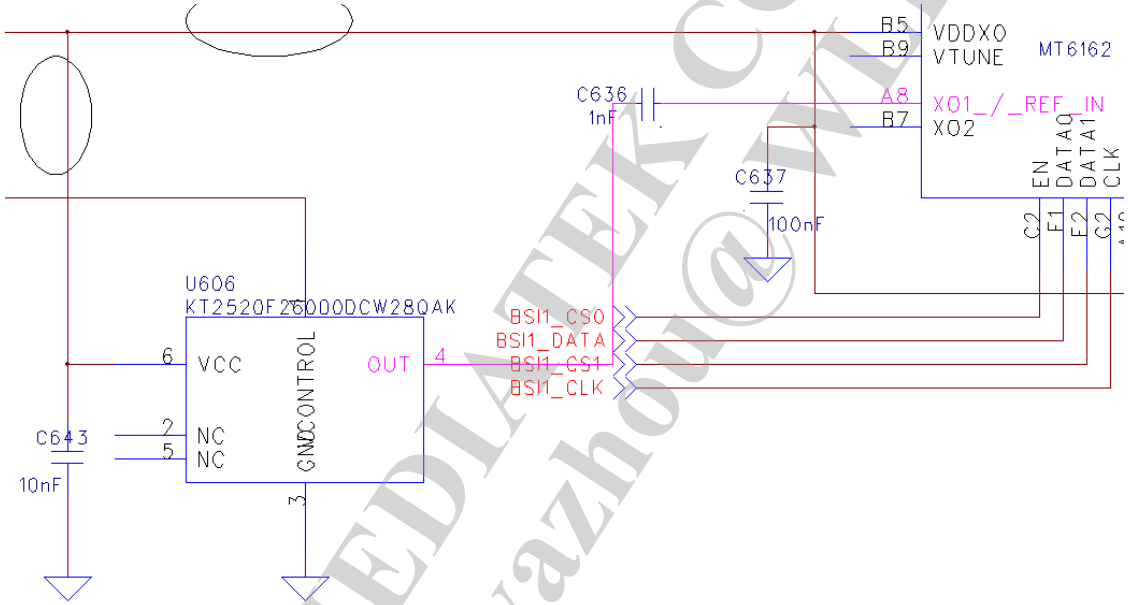
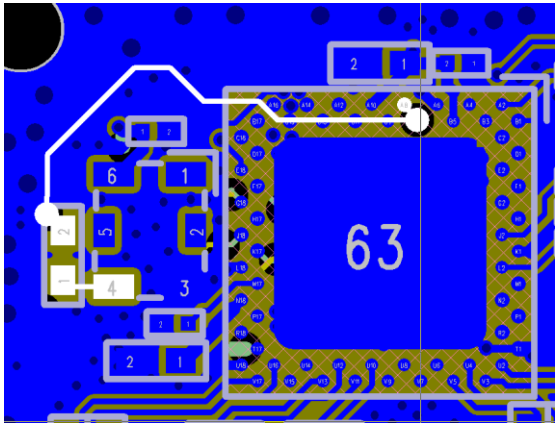
MT6575 RF (4/5)

- The clearance between RF pads/traces and GND should be at least 1 time of RF trace width.
- Solid GND plane within RF shielding case is recommended. More GND vias for the frame of shielding case is recommended.



- Reserve solid reference GND plane underneath 26MHz crystal.
- 26MHz and SYSCLK 26MHz signals must be shielded by GND.(adjacent and up/down layers.





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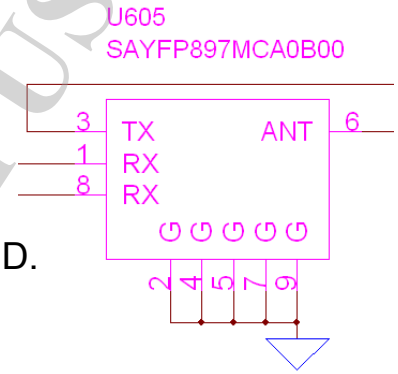
MT6575 RF (5/5)



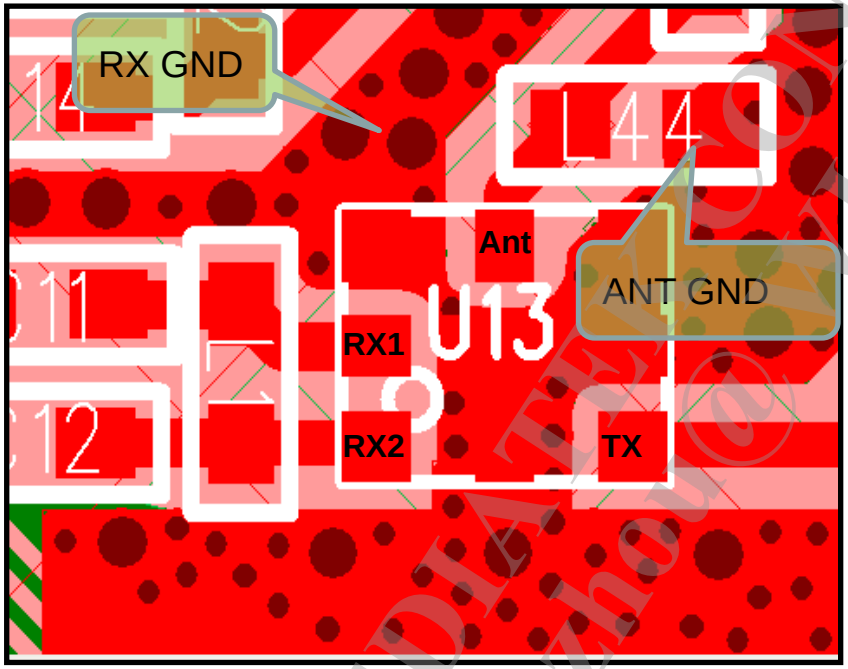
- **Notes for duplexer:**

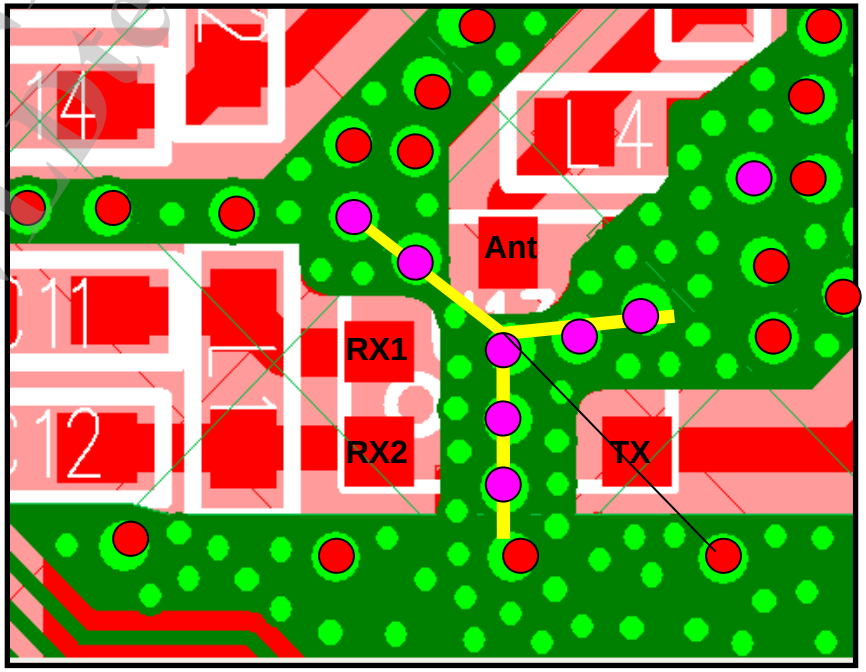
  a. Ensure solid GND plane for duplexer.

  b. GND pin of ANT's matching device should be faraway from RX GND.

  c. Do Not fan out ANT\RX\TX signals in parallel direction.

  d. ANT\RX\TX signals should be well separated by GND, allocate more GND vias on GND plane for better isolation.





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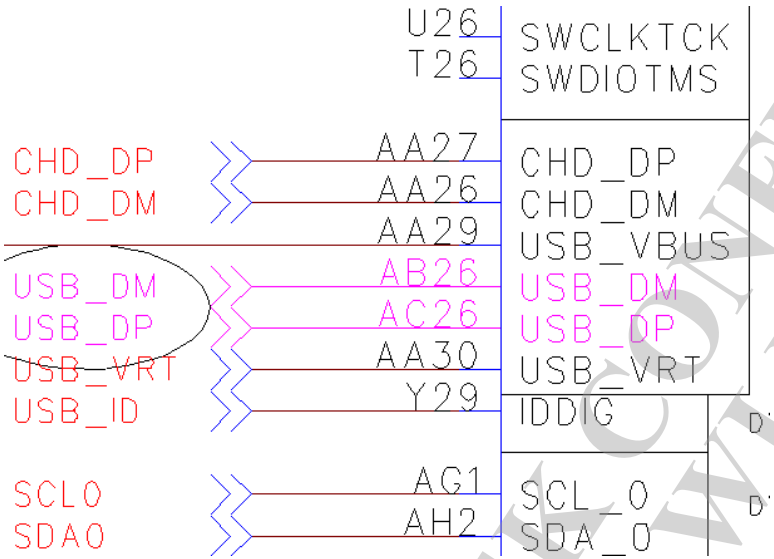
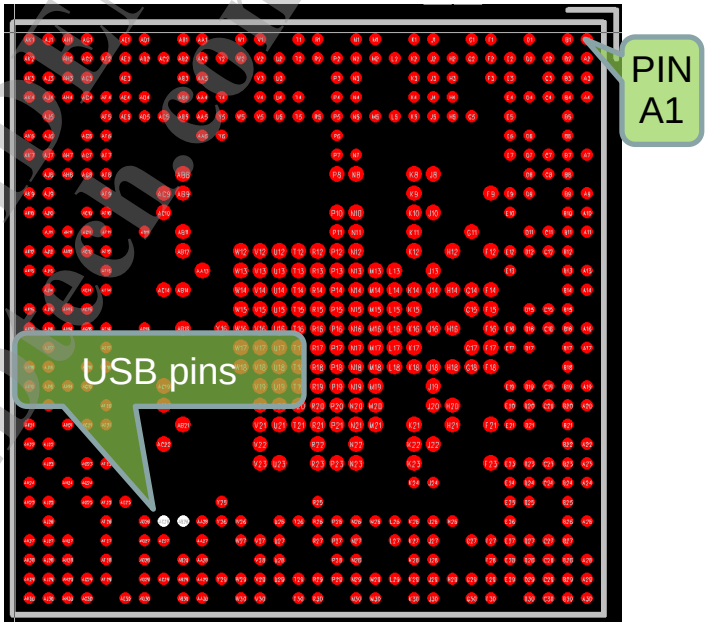
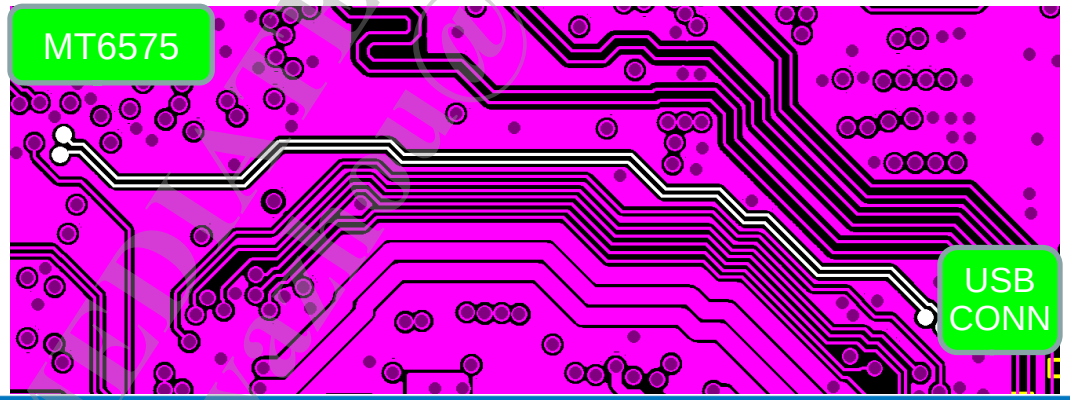
MT6575 USB

- USB signals(diff. pair) should be 90Ω impedance and with GND guard. Place ESD components as close to USB connector as possible.







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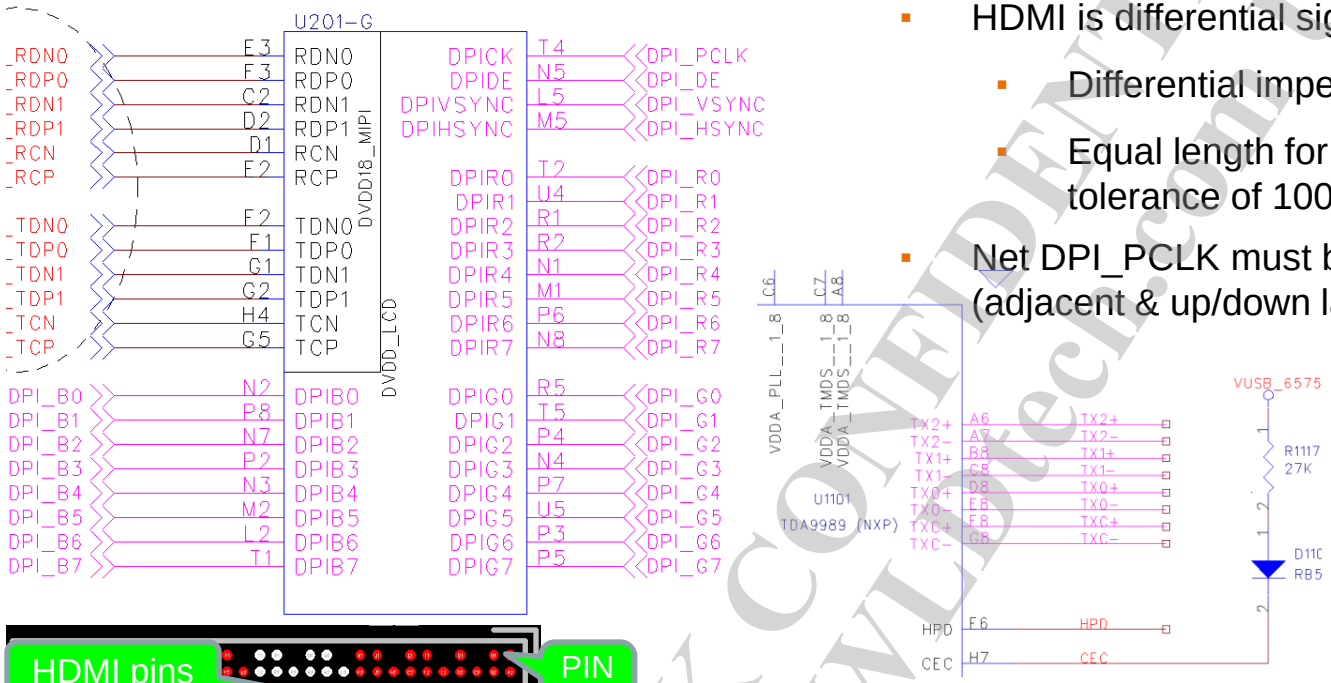
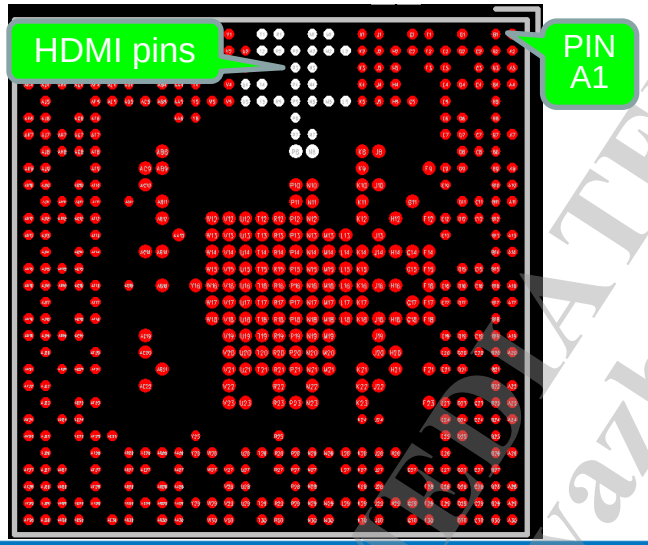
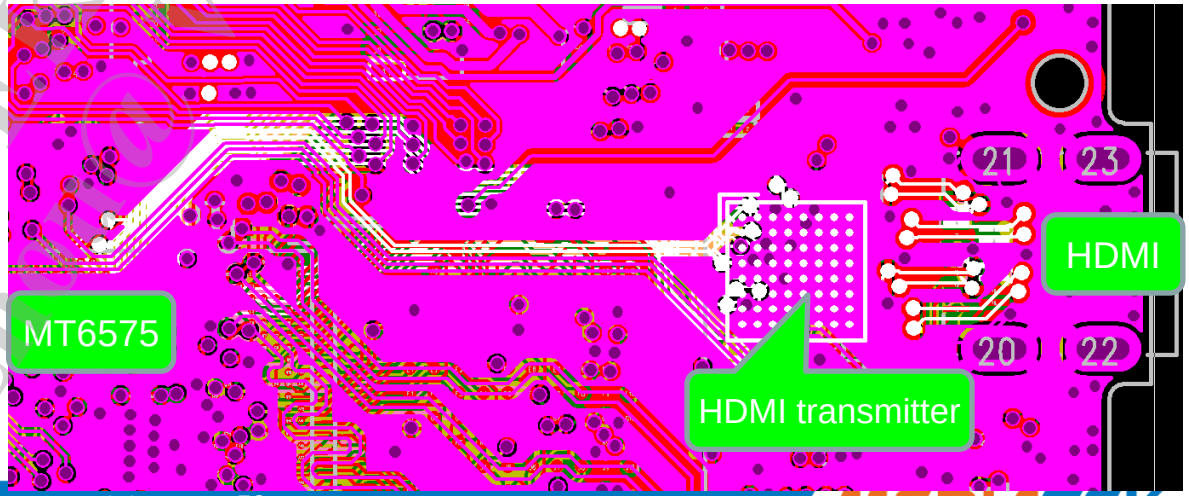
MT6575 HDMI

- HDMI transmitter must be placed within the shielding case to avoid noises from RF.
- HDMI is differential signal:
  - Differential impedance is 100Ω.
  - Equal length for 4 pairs TX signals with the tolerance of 100 mils.
- Net DPI_PCLK must be well shielded by GND (adjacent & up/down layers).







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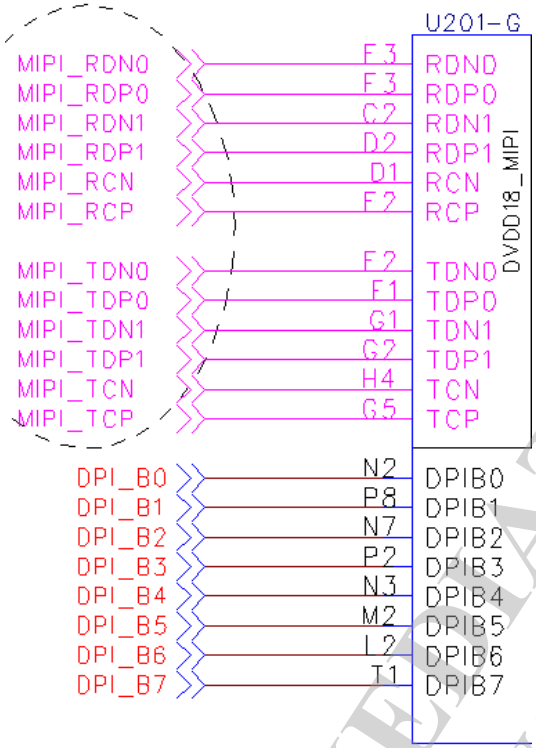
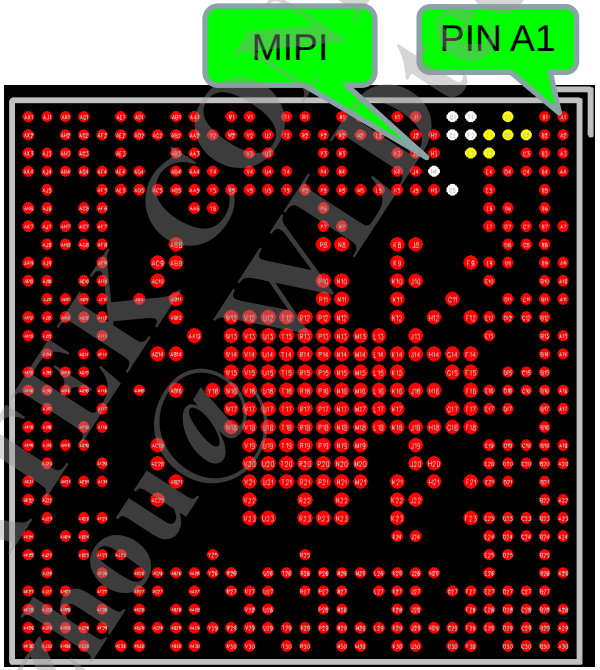
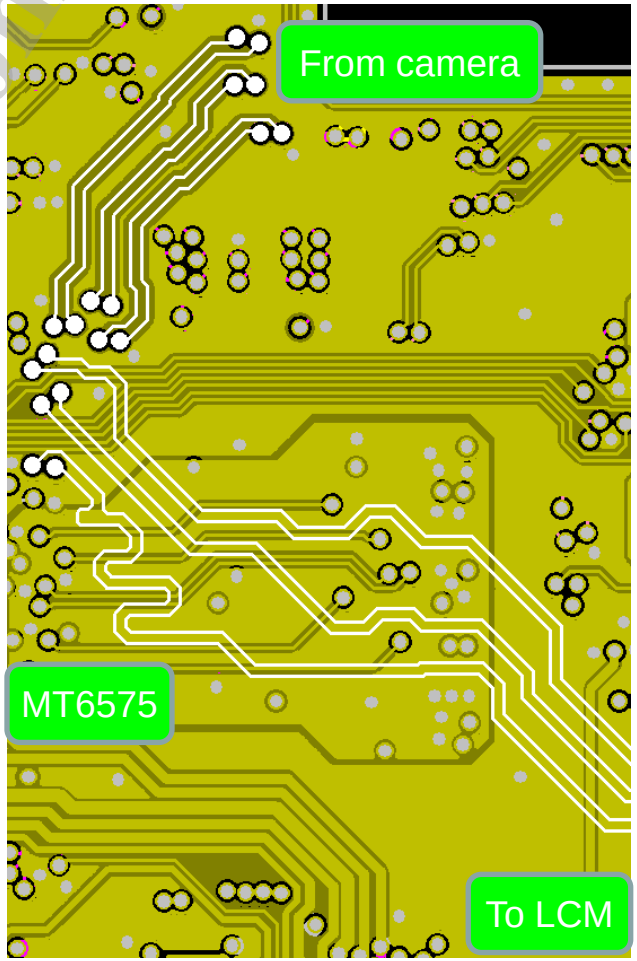
MT6575 MIPI

- Impedance of MIPI differential signals is 100Ω, must be well shielded by GND(adjacent & up/down layers).
- Equal length for same group of RX/TX with the tolerance of 100mil.







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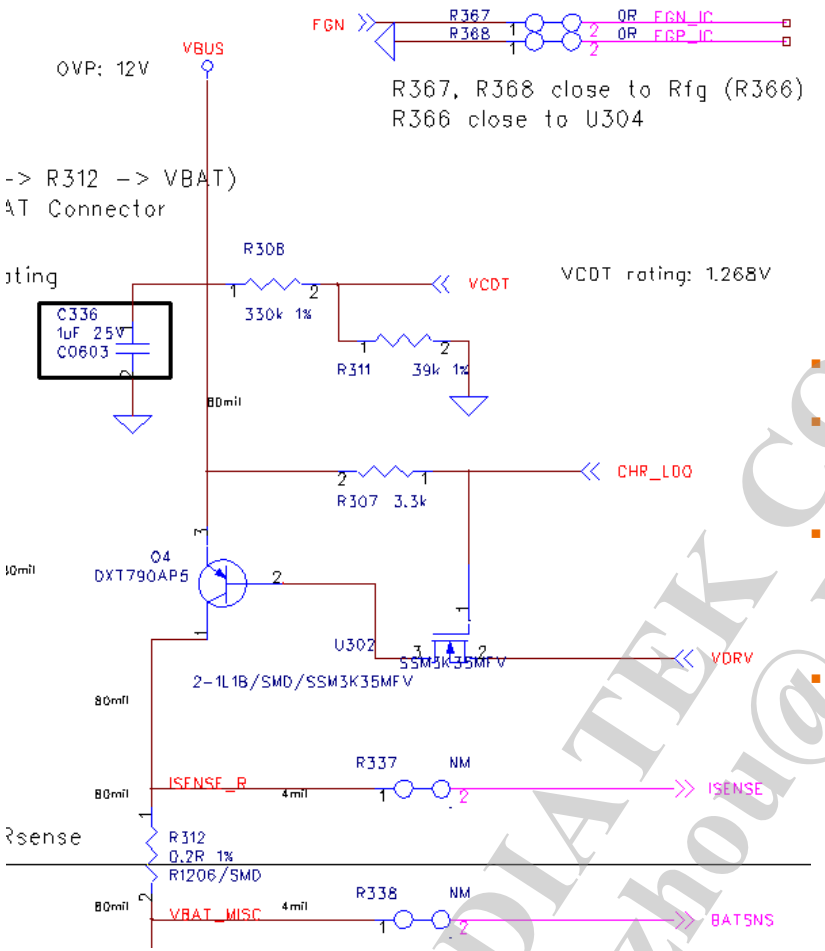
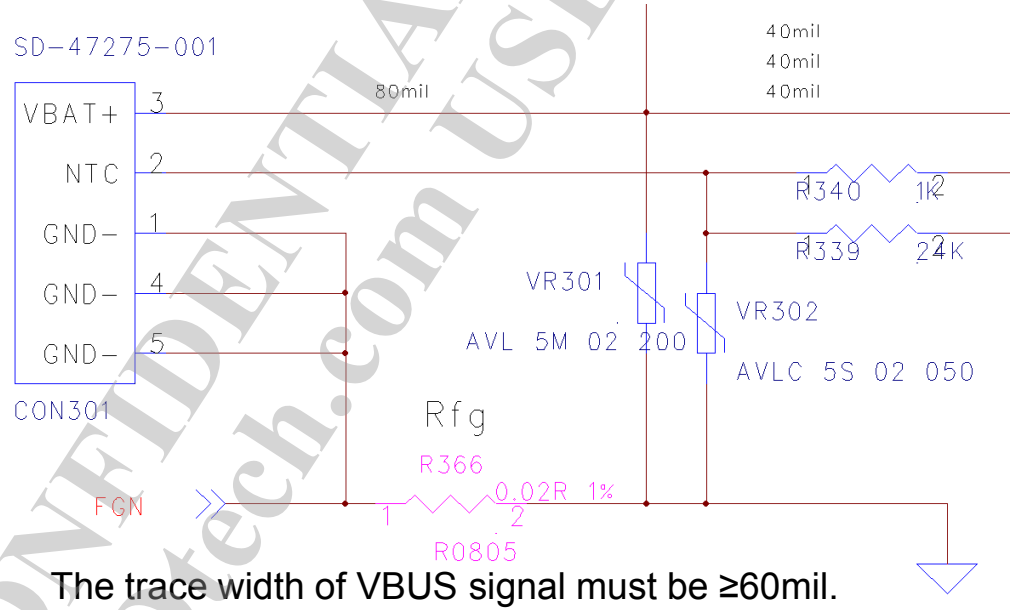
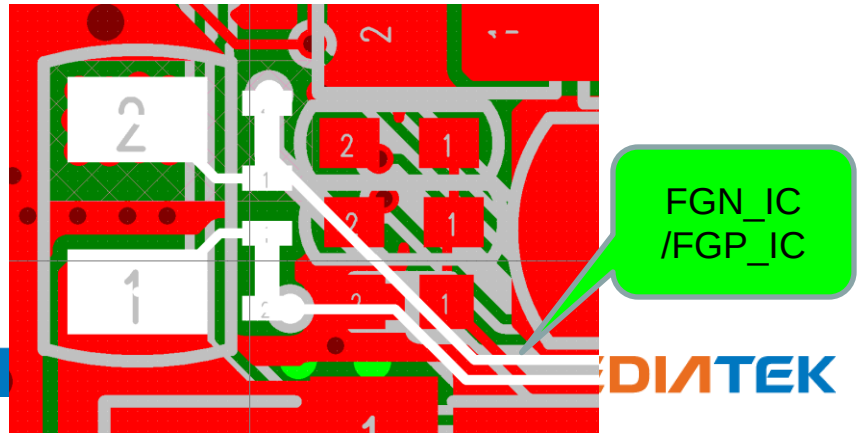
CHARGER





- The trace width of VBUS signal must be ≥60mil.
- All components in this page must be placed close to battery connector(CON301).
- FGN_IC/FGP_IC & ISENSE/BATSNS signals are differential pairs, GND guard is needed(adjacent side, at least).
- GND pin of R336 should be isolated with top layer.



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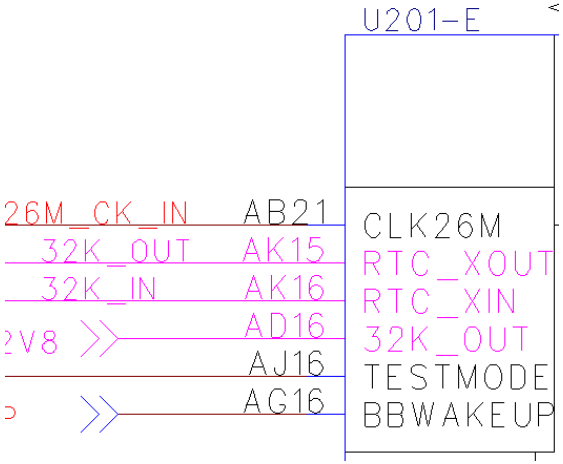
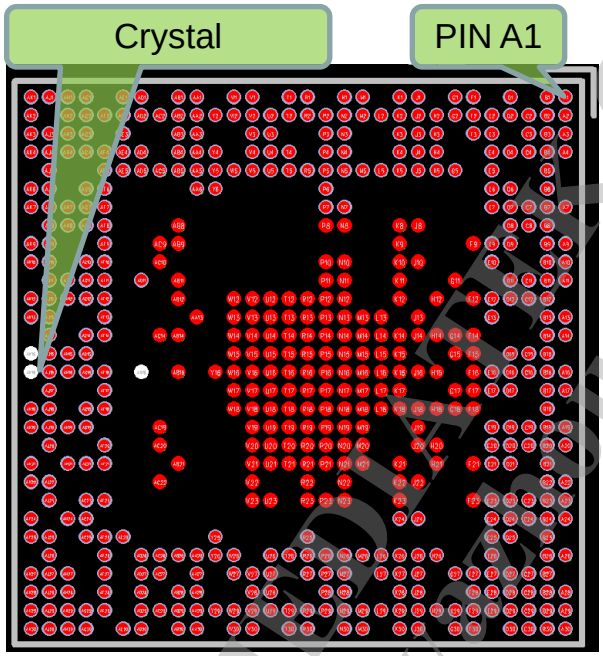
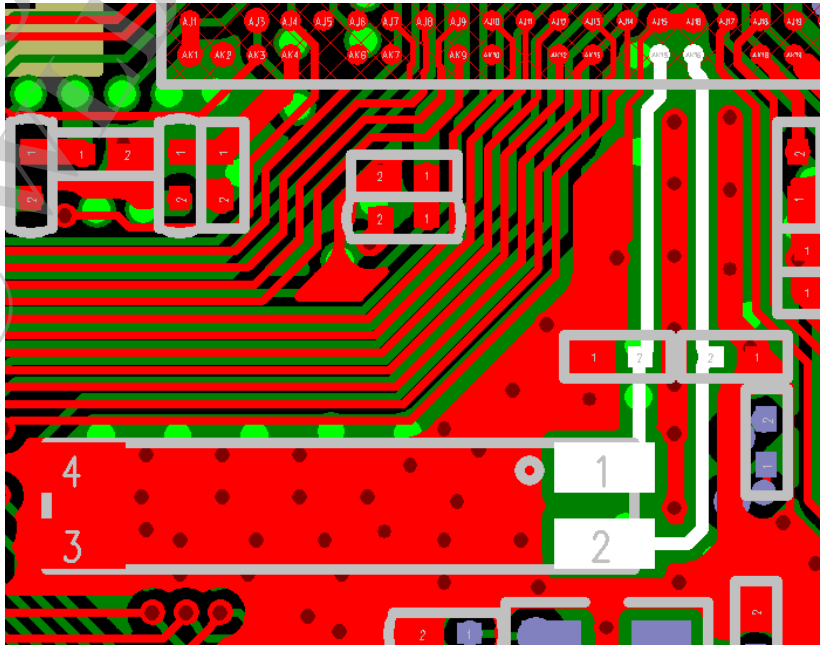
MT6575 32K Crystal



- Place the crystal and capacitors as close to MT6575 as possible, the signals should be shielded by GND.
- Ensure solid GND plane on top & adjacent layers for 32k crystal. It can be placed underneath MT6575 if needed.





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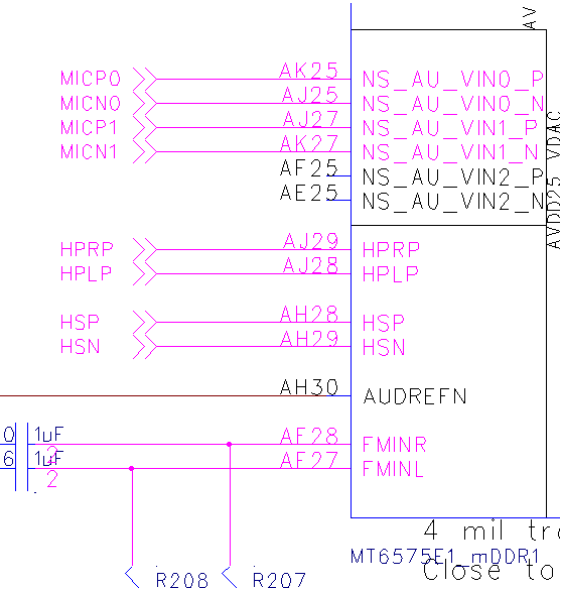
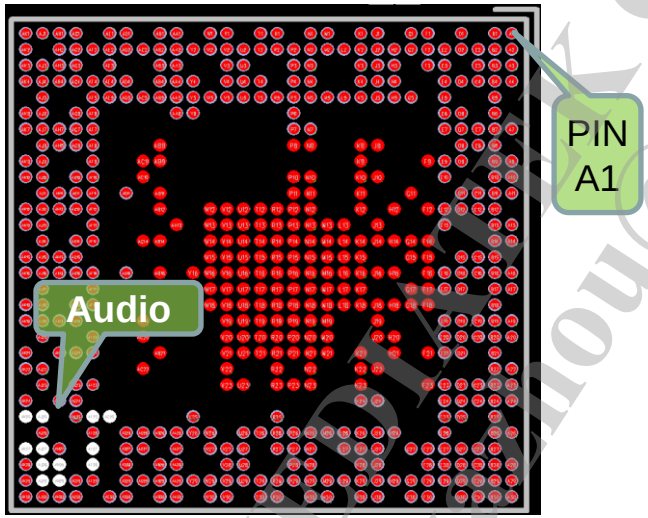
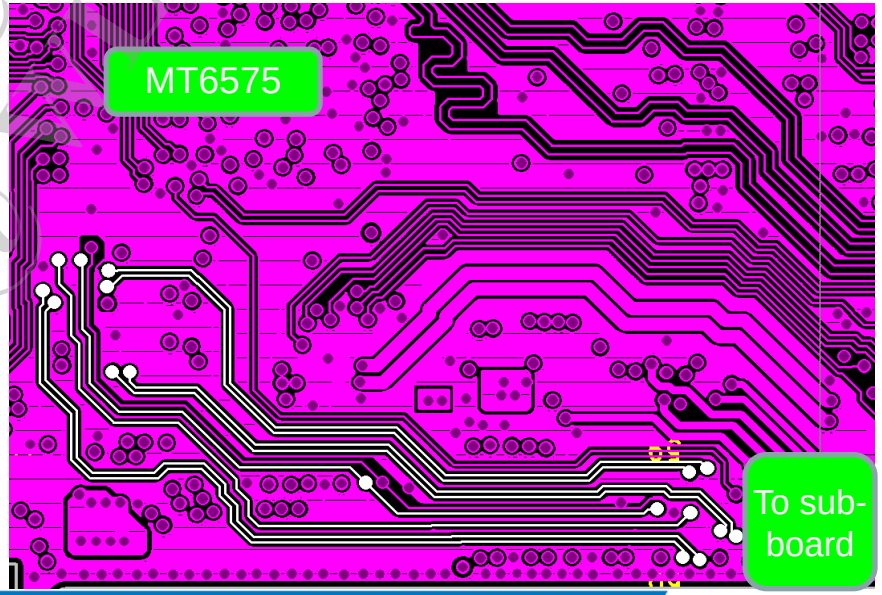
MT6575 Audio (1/2)



- The audio signals should be shielded by GND(adjacent & up/down layers), especially for some audio balls close to RF signal balls.
- Route MICN/MICP as differential pair and shielded by GND.
- HPRP, HPLP, FMINR, FMINL are audio signals, shielded by GND respectively (adjacent & up/down layers).





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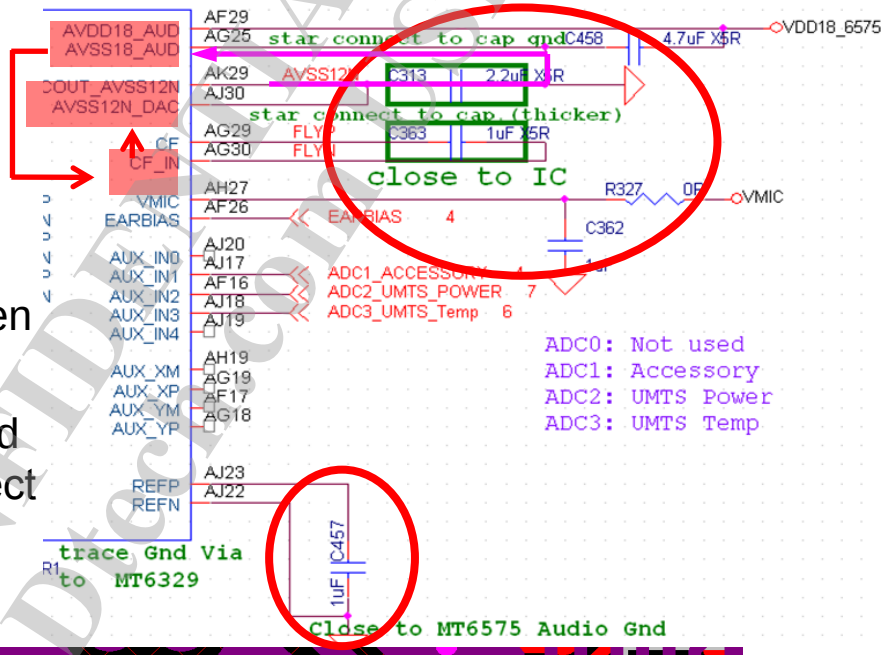
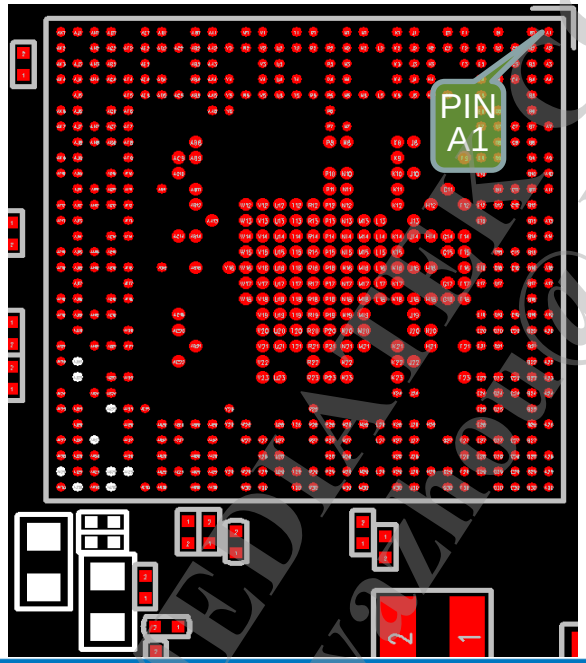
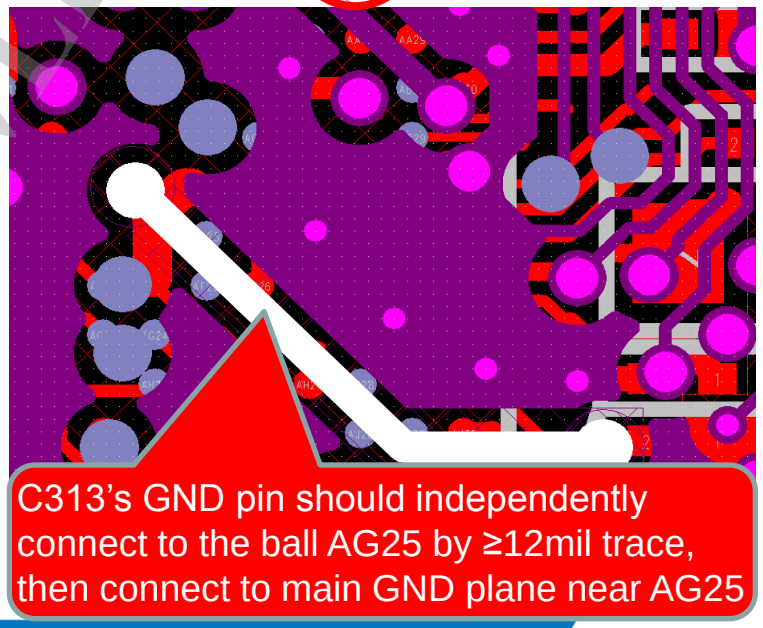
MT6575 Audio (2/2)

- Place the cap. C363, C313, C457, C458, C362 close to MT6575.
- C313's GND pin should independently connect to the ball AG25 by ≥12mil trace, then connect to main GND plane near AG25.
- Ball AJ22 should be independently connected to C457's GND pin by 4mil trace, then connect to main GND plane with C457's GND pin.







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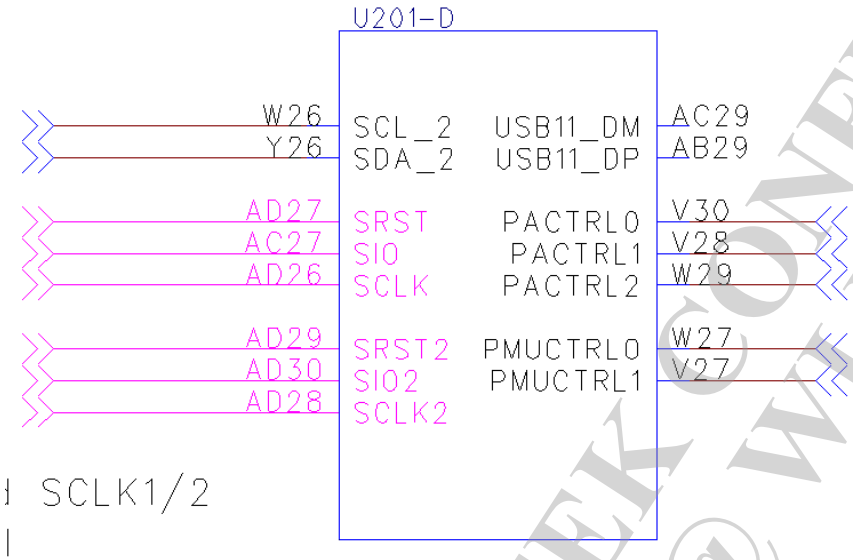
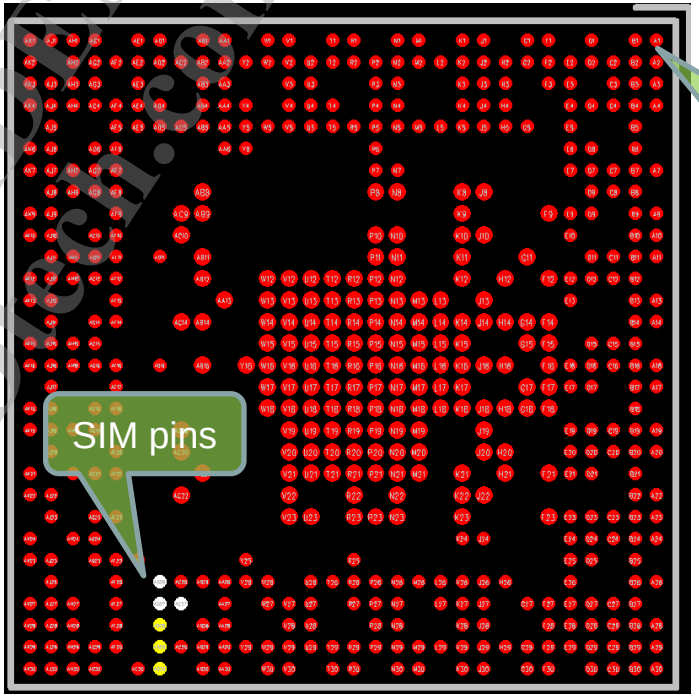
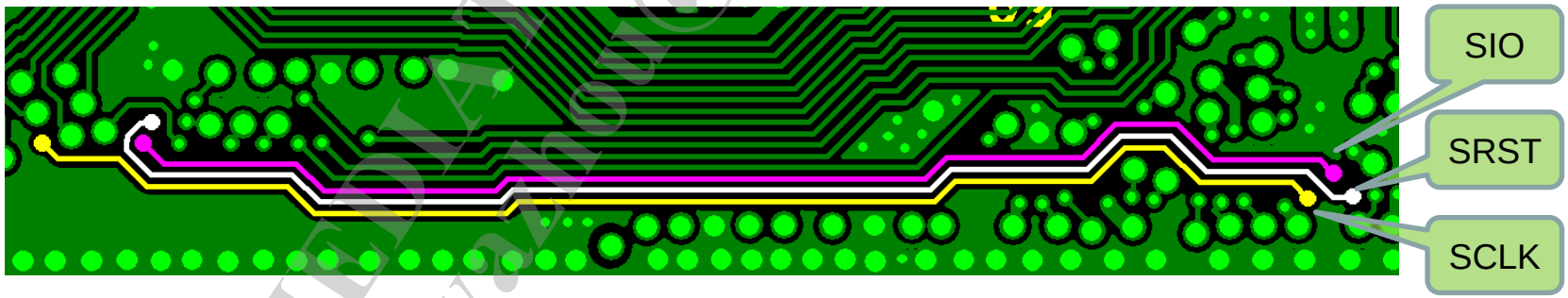
MT6575 SIM CARD

- SCLK signal should be shielded by GND.
- If GND shielding is not available, don't route SCLK signal parallel with SIO signal, and they can be separated by SRST signal.







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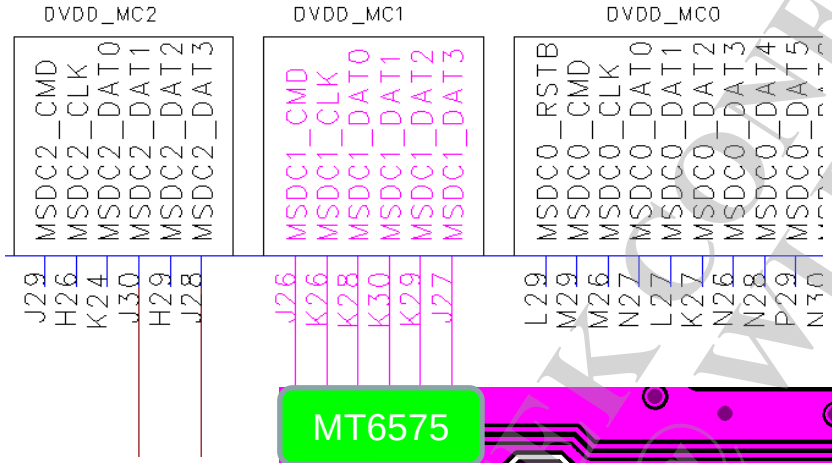
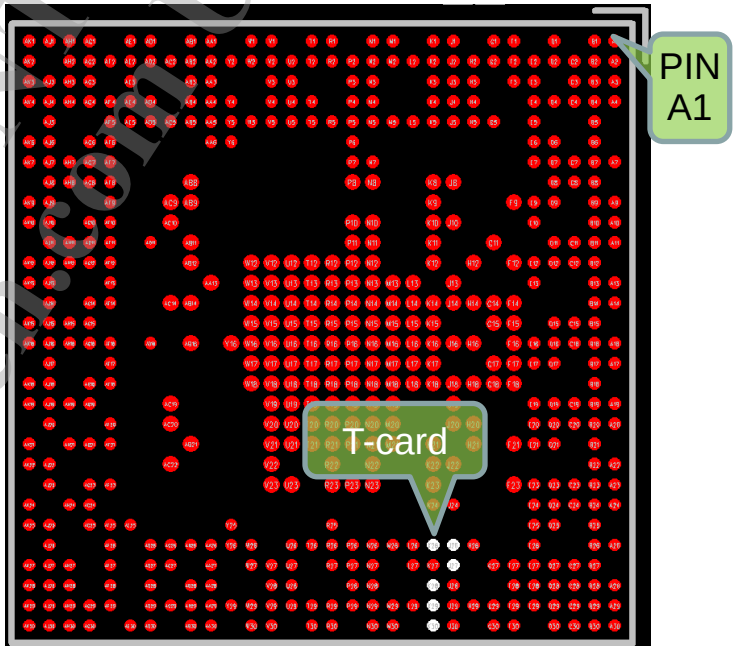
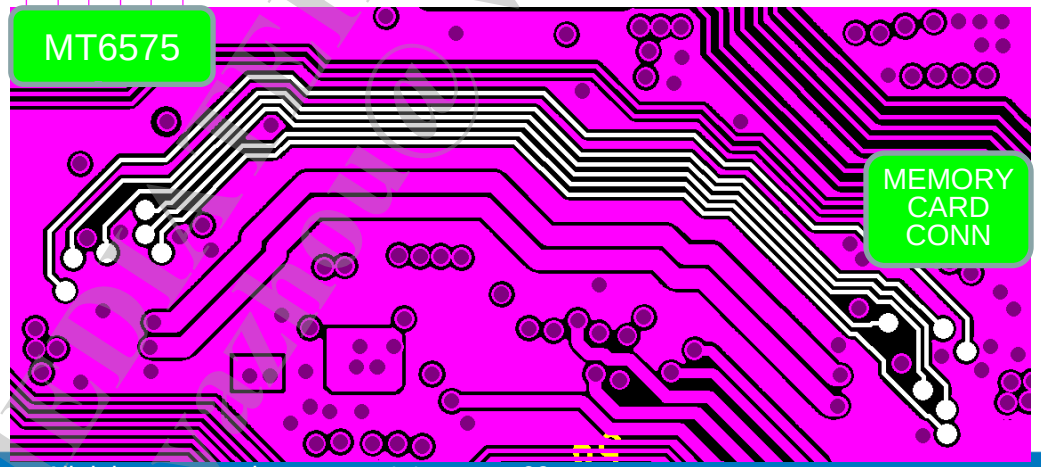
MT6575 T-CARD

- MC_CLK must be shielded by GND(adjacent & up/down layers). MC_DATA/MC_CMD signals need to be shielded by GND.
- Length tolerance of signals for memory card should be within 300mil.
- Place bypass cap. close to the T card connector.







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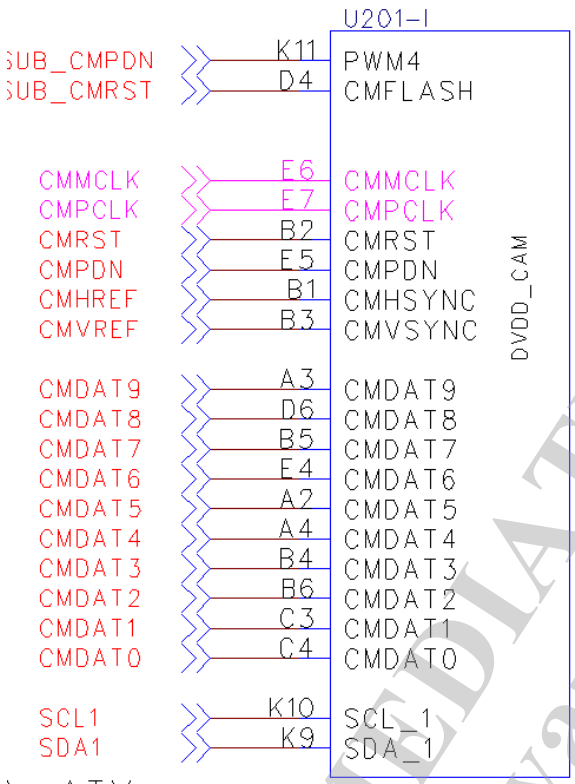
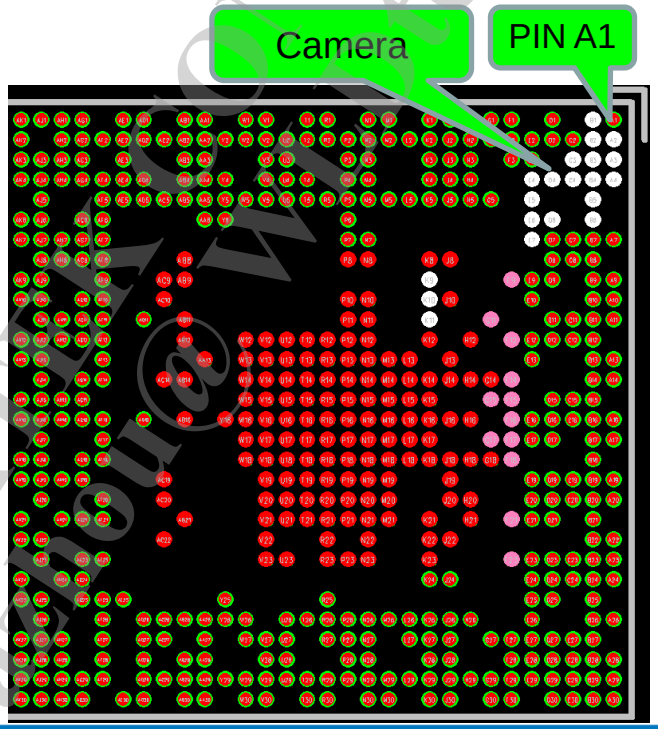
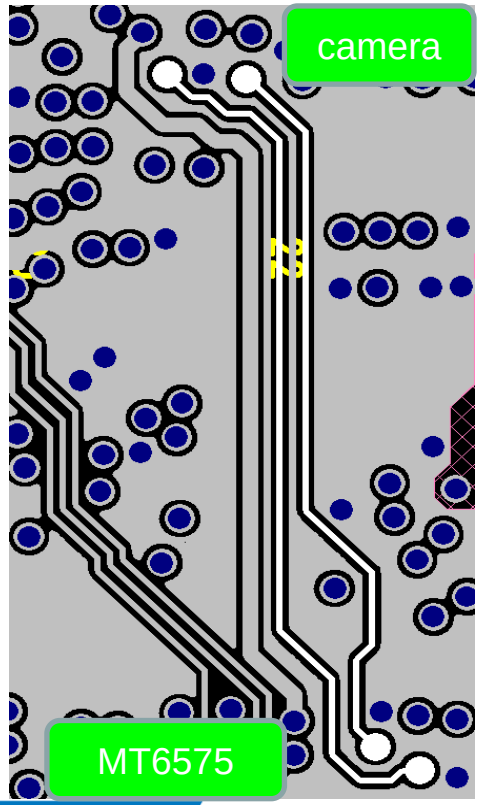
MT6575 CAMERA

- CMMCLK/CMPCLK is differential pair and need to be shielded by GND (adjacent & up/down layers).
- Make the trace width of VCAMA ≥ 12mil and with GND shielding.
- It is recommended to route CMDATA signals in inner layer for noise prevention.







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MT6620
PCB LAYOUT GUIDELINE

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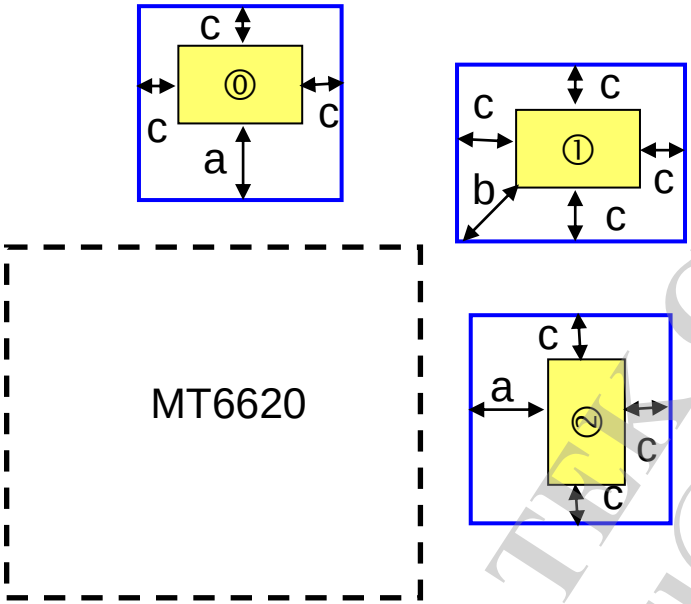
MT6620 BT/FM/WIFI/GPS (1/3)



1.⓪①②are the possible location for TCXO placement.
2.GND clearance “a “: 3 mm
3.GND clearance “b” : 2 mm
4.GND clearance “c” : 1.5 mm

1. TCXO clock must be shielded by GND(adjacent & up/down layers).
2. TCXO need be placed within 6620 shielding case.
3. Others signals across under blue area of TCXO is forbidden.
4. Except opposite layer, remove GND plane under blue area of TCXO.
5. R/L/C components of TCXO are allowed to be placed within blue area of TCXO.
6. All signals in the blue area is allowed to use 4mil trace, including power and GND.

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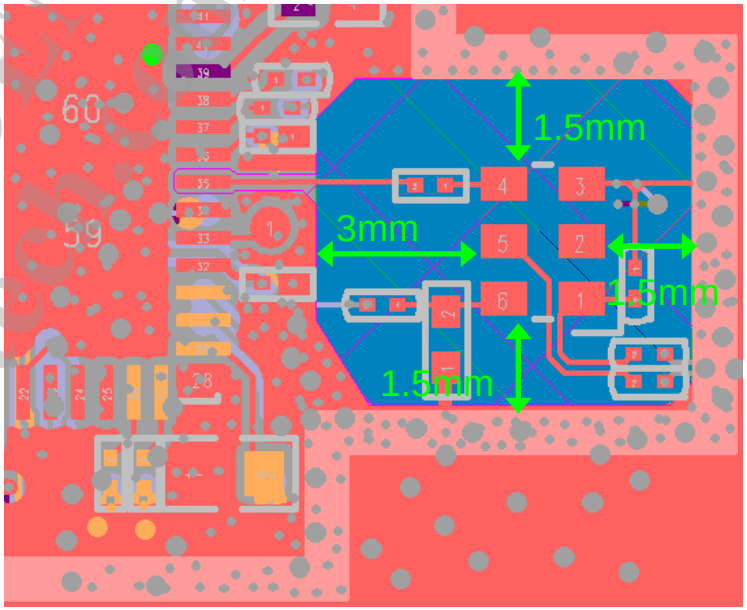
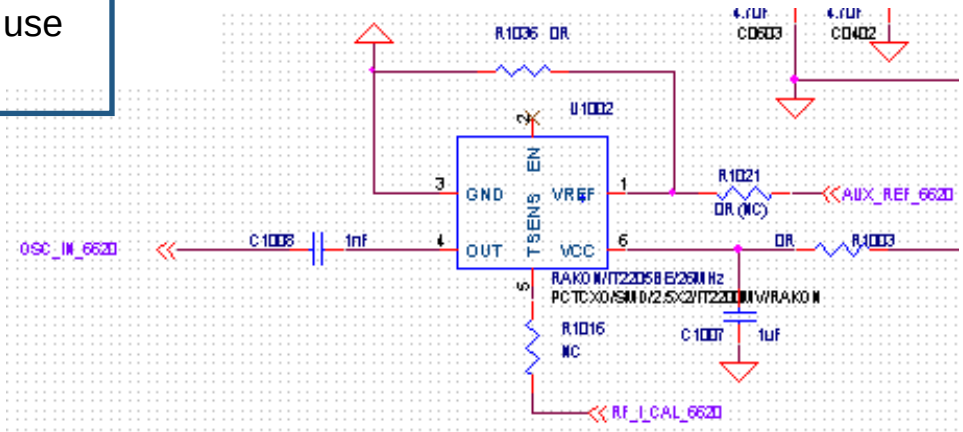
MT6620 BT/FM/WIFI/GPS (2/3)

- PCTCXO

1. Right figure is compatible design for TCXO & PCTCXO.
2. Connect the GND pins of TCXO & PCTCXO to shielding case by 4mil trace.
3. Remove GND plane under blue area of TCXO except opposite layer.
4. Unrelated signals across under blue area of TCXO is forbidden.
5. Route TSENS and VREF as a differential pair, and should be shielded by GND.
6. All signals in the blue area are allowed to use 4mil trace, including power and GND





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MT6620 BT/FM/WIFI/GPS (3/3)

- 50 Ω impedance control for RF signals of BT、WIFI、GPS、FM_TX_OUT .
- Place 2.2uH decouple inductor close to MT6620.
- Route FM_RX_N and FM_RX_P (long ANT for FM) as differential pairs, and must be shielded by GND.
- Route VBAT signal from battery connector to MT6620 independently.
- GND_SMPS(pin13) should be independently connected to C1001 GND pin, and then connect to the main GND.

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MT6329
PCB LAYOUT GUIDELINE

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OUTLINE

- WHAT IS MT6329
- MT6329 VBAT INPUT
- MT6329 BUCK OUTPUT
- MT6329 LDO OUTPUT
- MT6329 SPEAKER
- MT6329 AUDIO
- MT6329 OTHERS

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WHAT IS MT6329

- The MT6329 is a high performance and integrated power management IC(PMIC), which is suitable for high-end 3G smart。phone。
- Integrated functions
  - 5 buck converters, 17 LDOs
  - Boost converter for backlight/flashlight
  - Vibrator，keypad driver, analog switch
  - Pulse charger controller
  - 2 audio AMP(Class-AB/D)
- Applications:
  - Smart phone (MT6575/MT6515)

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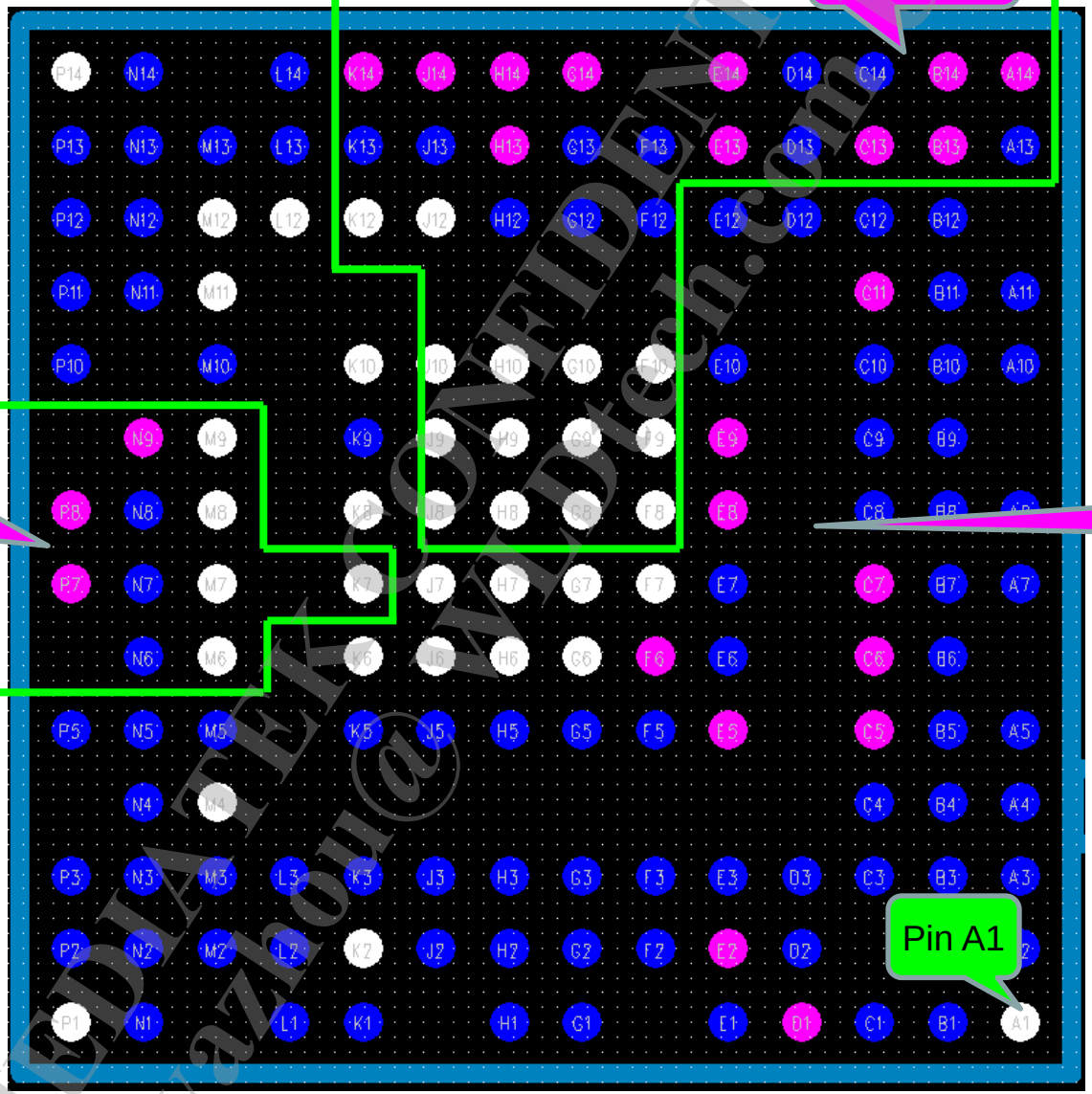
MT6329 VBAT INPUT(1/7)

3 modules of MT6329 VBAT input circuit

1. BUCK

2. SPEAKER

3. LDO



Pink balls: VBAT input balls

White balls: GND balls

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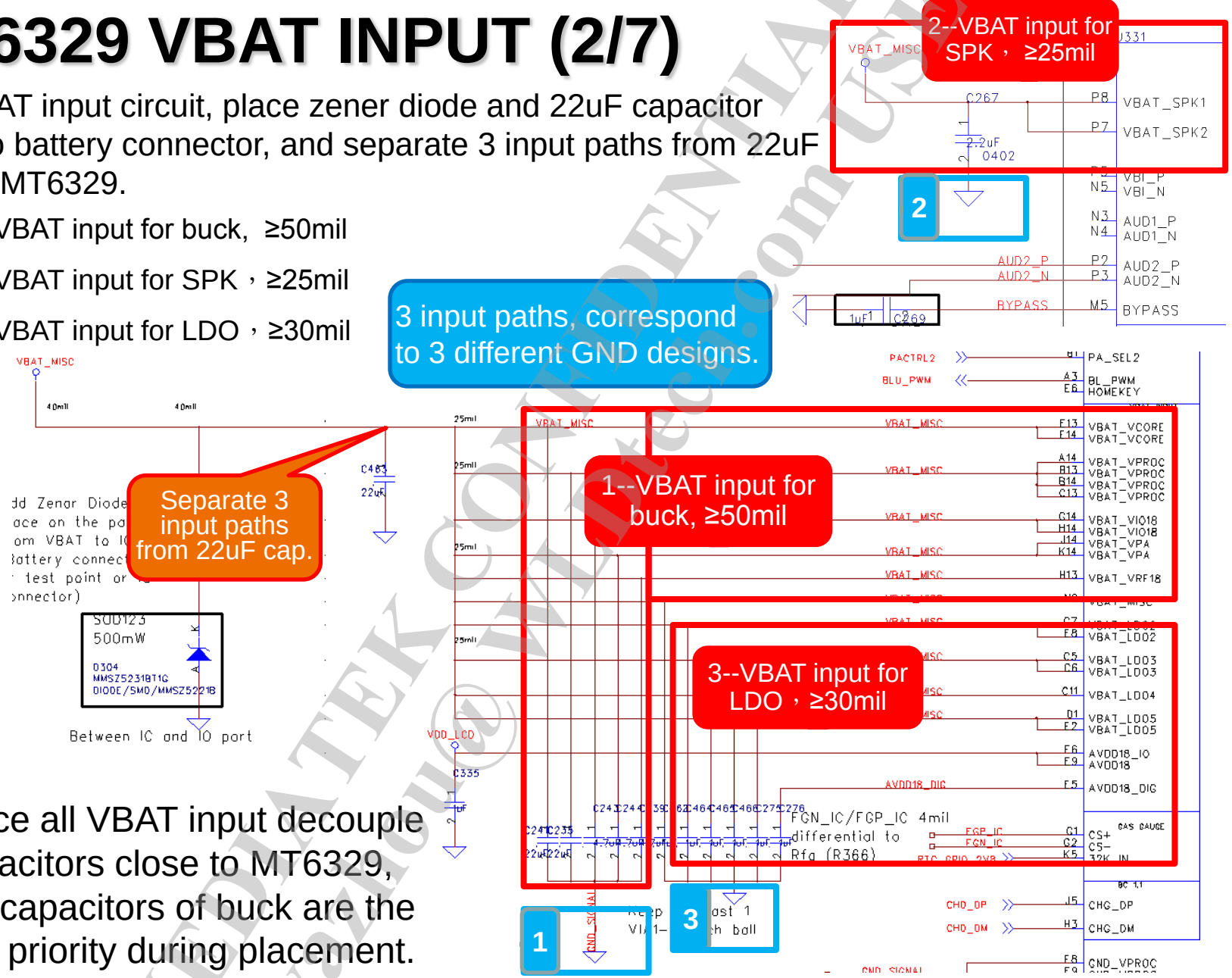
MT6329 VBAT INPUT (2/7)

- For VBAT input circuit, place zener diode and 22uF capacitor close to battery connector, and separate 3 input paths from 22uF cap. to MT6329.
  - 1、 VBAT input for buck, ≥50mil
  - 2、 VBAT input for SPK，≥25mil
  - 3、 VBAT input for LDO，≥30mil



- Place all VBAT input decouple capacitors close to MT6329, the capacitors of buck are the first priority during placement.

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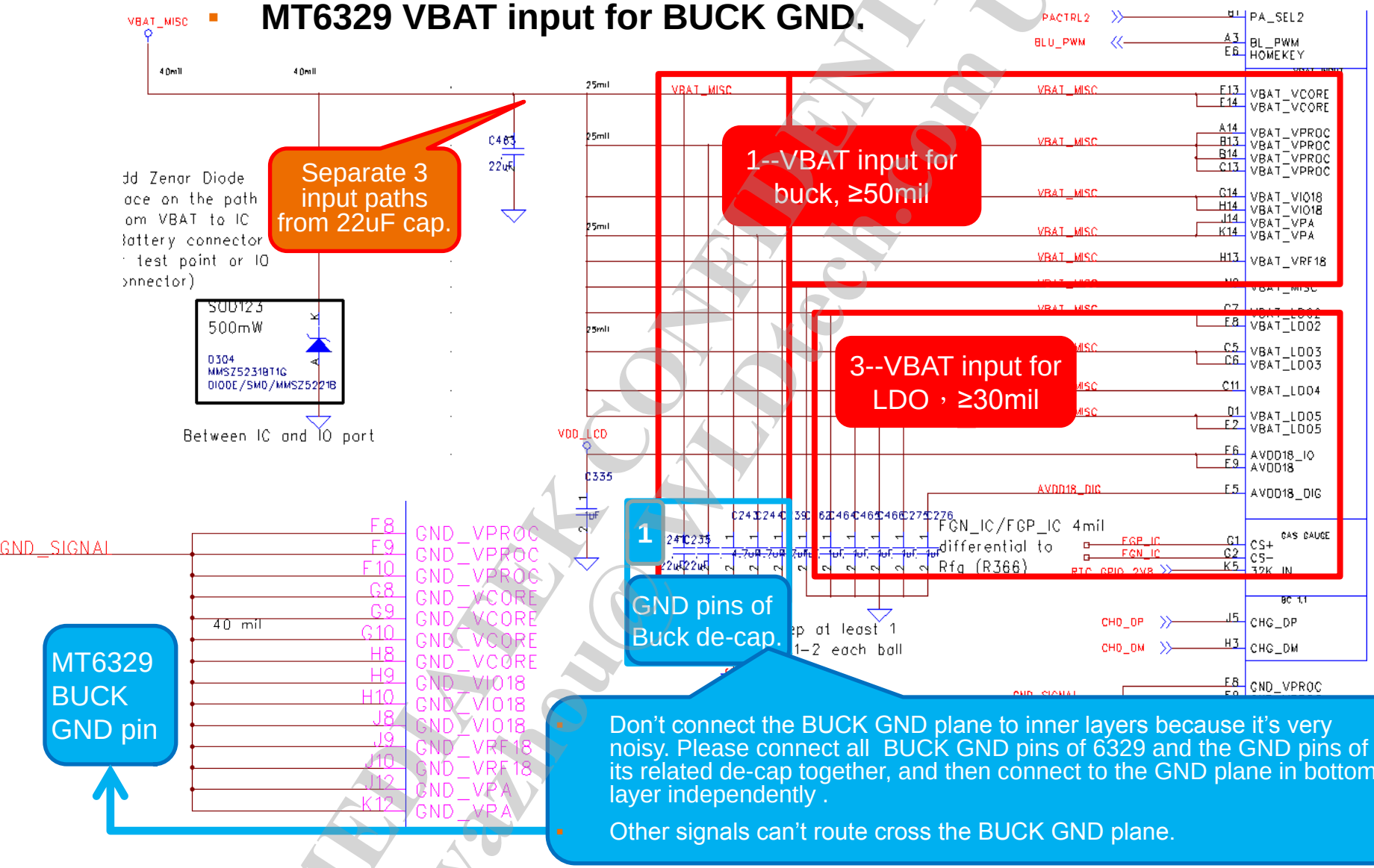
MT6329 VBAT INPUT(3/7)

- **MT6329 VBAT input for BUCK GND.**



- Don't connect the BUCK GND plane to inner layers because it's very noisy. Please connect all BUCK GND pins of 6329 and the GND pins of its related de-cap together, and then connect to the GND plane in bottom layer independently .
- Other signals can't route cross the BUCK GND plane.

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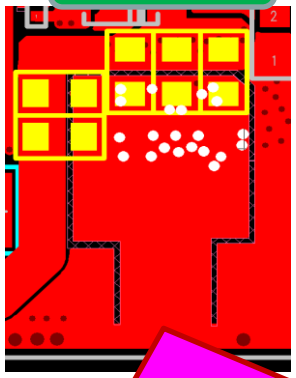
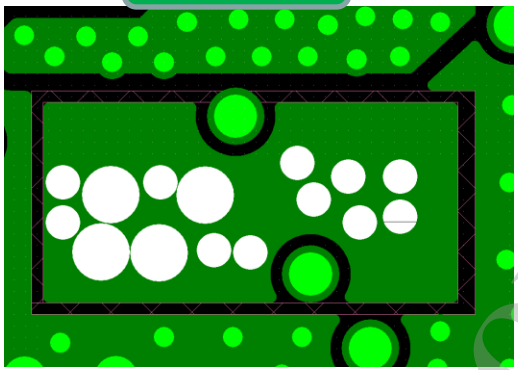
MT6329 VBAT INPUT(4/7)

- **MT6329 VBAT input for BUCK GND**

Layer1



Layer2



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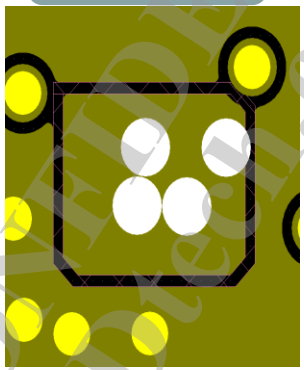
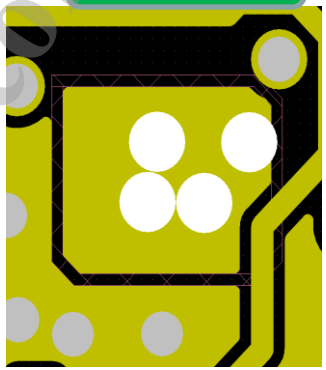
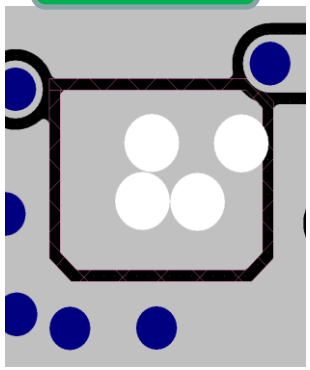


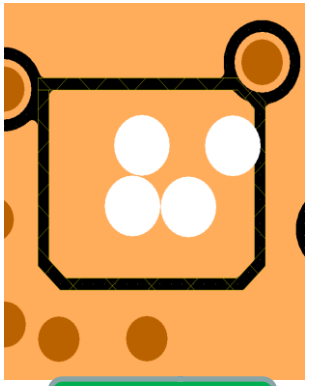
Layer4



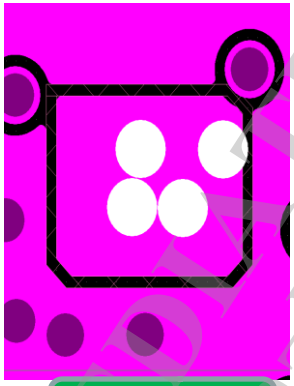
Layer5



Connect all BUCK GND pins of 6329 & its related de-cap GND pins first, and then connect to the bottom layer independently.



Layer6



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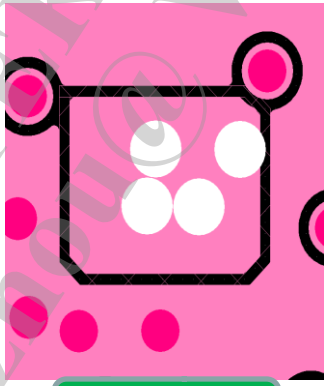
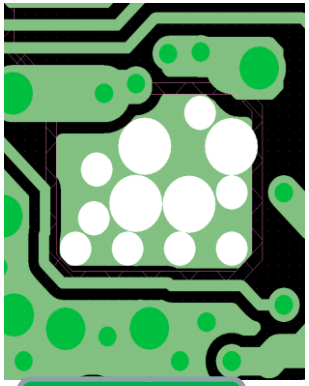


Layer8



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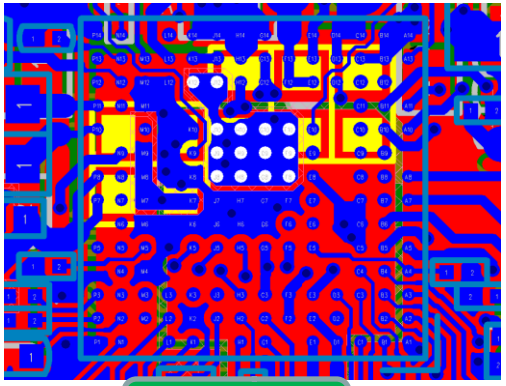

Layer10

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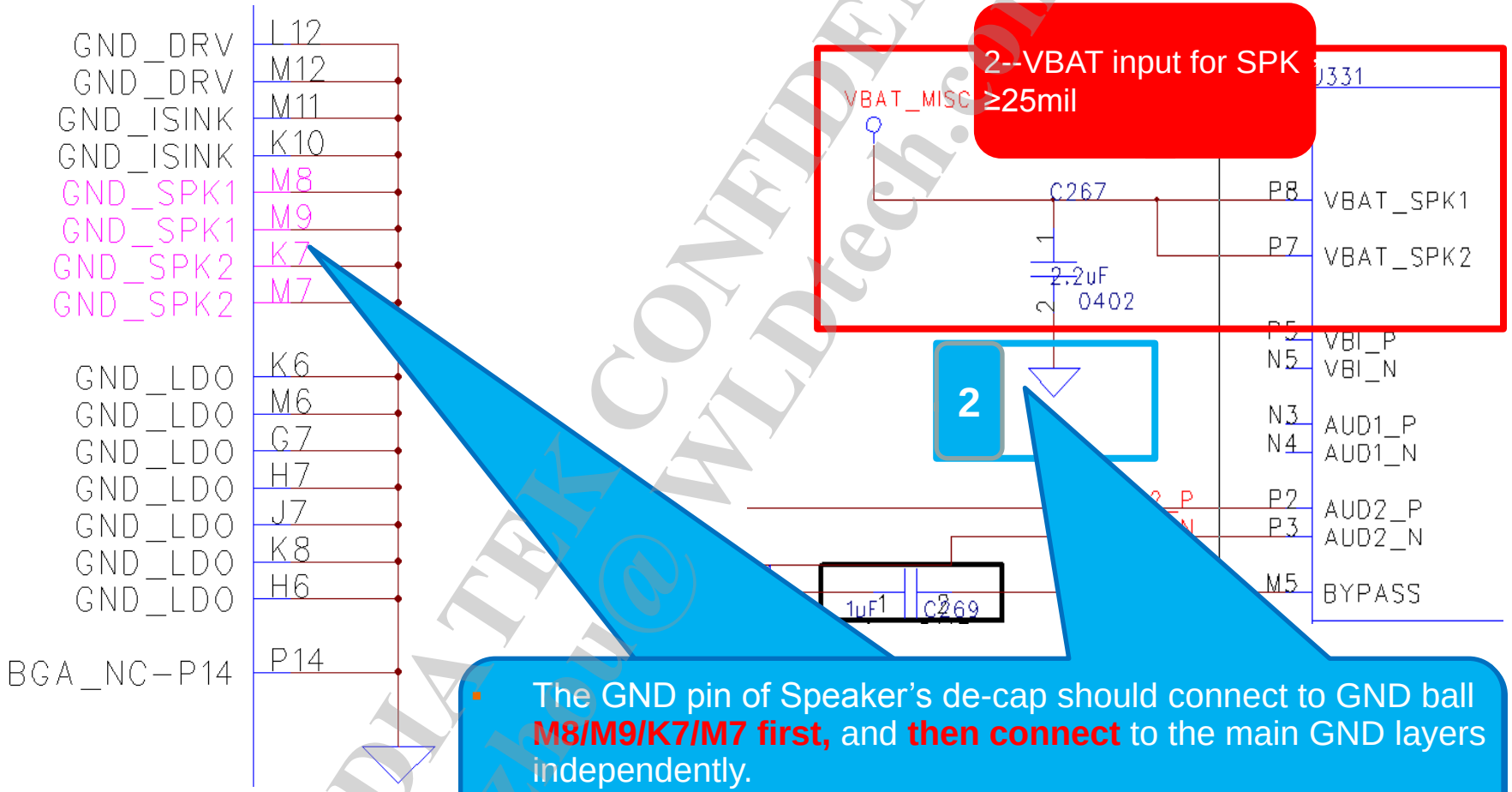
MT6329 VBAT INPUT(5/7)

- **MT6329 VBAT INPUT FOR SPEAKER GND**



- The GND pin of Speaker's de-cap should connect to GND ball **M8/M9/K7/M7 first,** and **then connect** to the main GND layers independently.
- The connection trace width should be ≥50mil.

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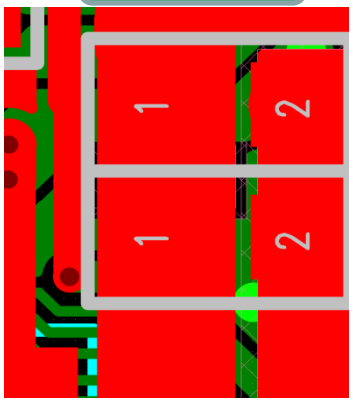
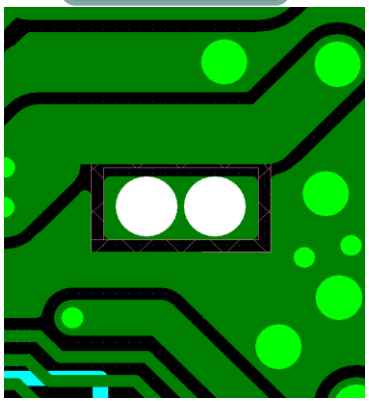
MT6329 VBAT INPUT(6/7)

- **MT6329 VBAT INPUT FOR SPEAKER GND**

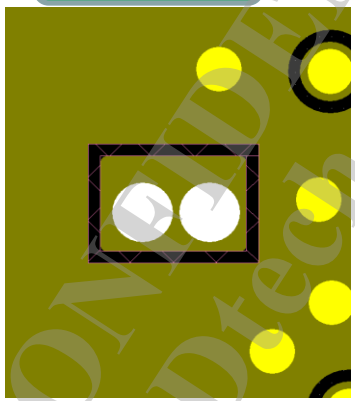
Layer1



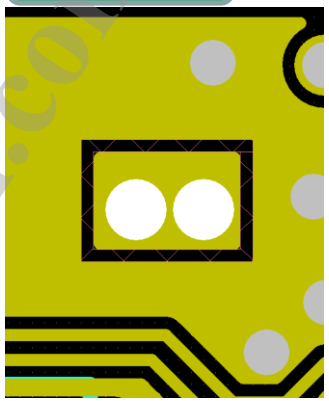
Layer2



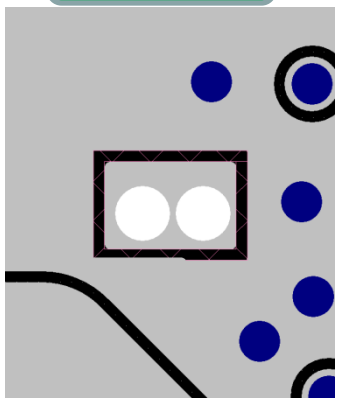
Layer3



Layer4

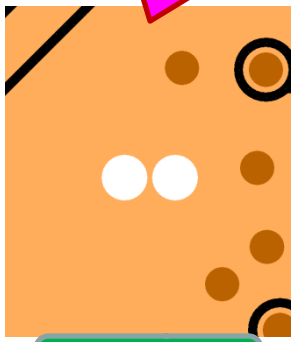


Layer5

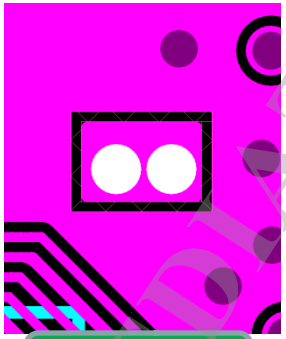


SPEAKER GND connect to main GND plan in Layer 6 only.

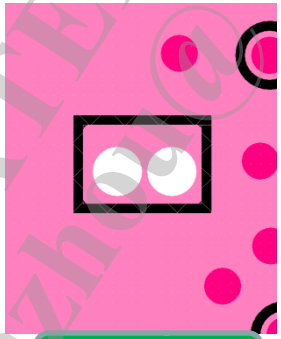
The GND pin of Speaker's de-cap should connect to GND ball **M8/M9/K7/M7 first**, and **then connect** to the main GND layers independently.



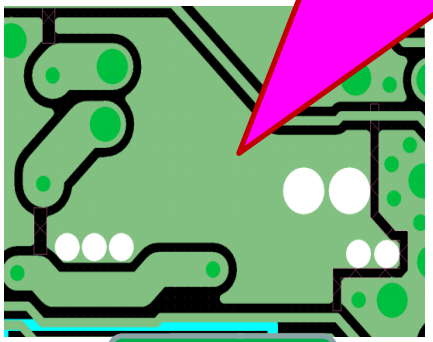
Layer6



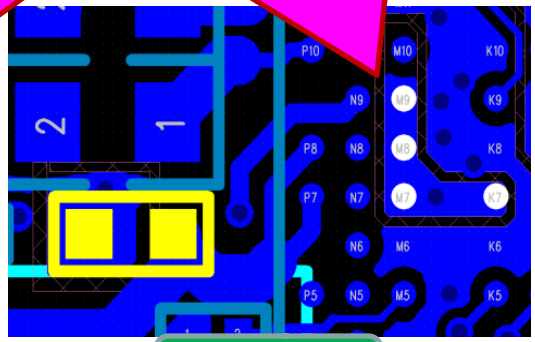
Layer7



Layer8



Layer9



Layer10

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MT6329 VBAT INPUT(7/7)

- Layout recommendation for other VBAT input modules

Ball name	Net name	Trace width
AVDD18	VIO18_PMU	As wide as possible (>20mil) / (10mil under chip area)
VBAT_LDO2	VBAT_LDO2	As wide as possible (>20mil) / (10mil under chip area)
VBAT_LDO2	VBAT_LDO2	
VBAT_LDO3	VBAT_LDO3	As wide as possible (>20mil) / (10mil under chip area)
VBAT_LDO3	VBAT_LDO3	
VBAT_LDO4	VIO18_PMU	As wide as possible (>20mil) / (10mil under chip area)
VBAT_LDO5	VBAT_LDO5	As wide as possible (>20mil) / (10mil under chip area)
VBAT_LDO5	VBAT_LDO5	
AVDD18_IO	VIO18_PMU	As wide as possible (>20mil) / (10mil under chip area)
AVDD18_DIG	AVDD18_DIG	4mil
VBAT_MISC	VBAT_MISC	As wide as possible (>20mil) / (10mil under chip area)

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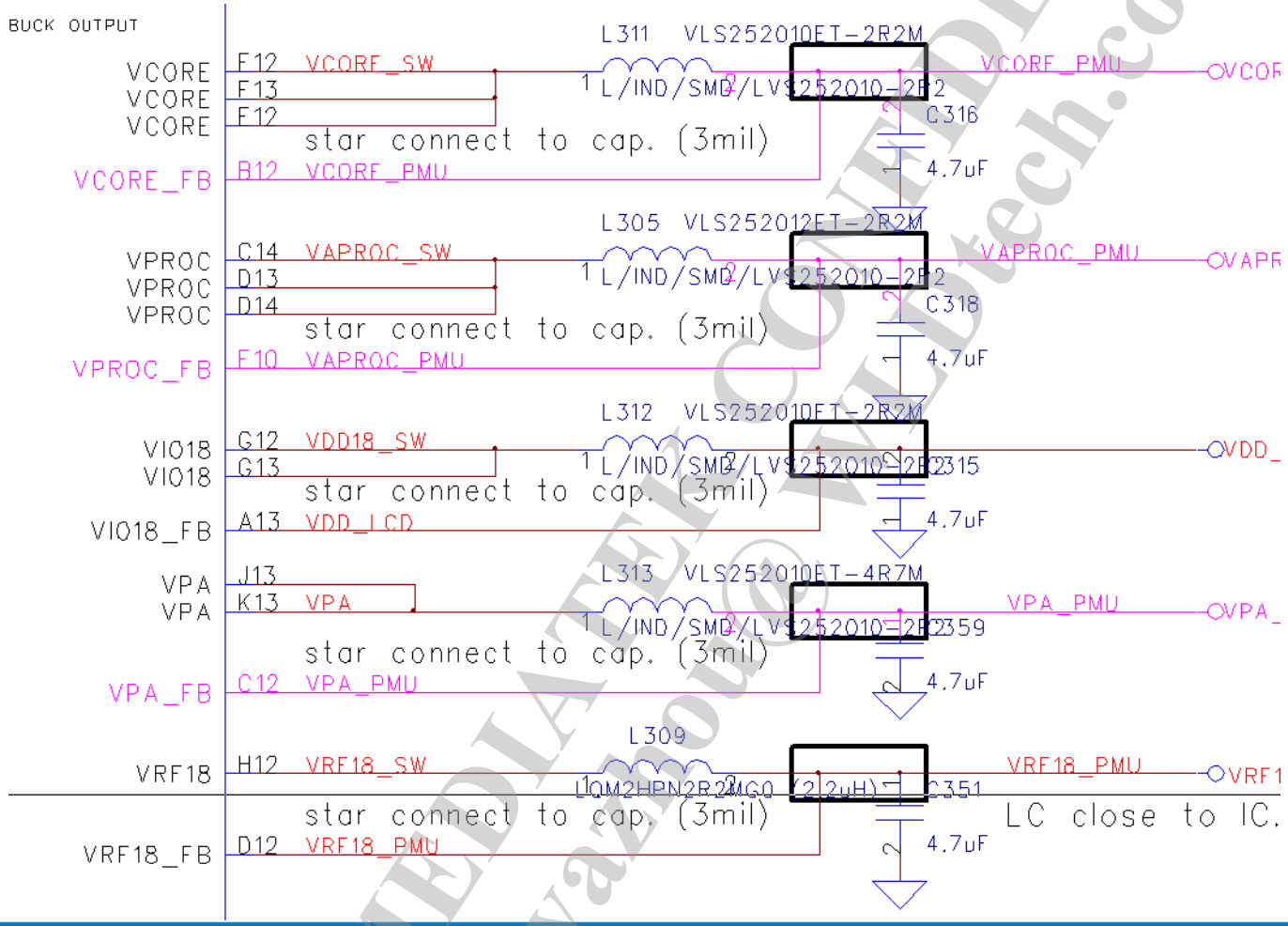
MT6329 BUCK OUTPUT

- **Allocate the L/C components of BUCK close to MT6329**

Priority: VAPROC > VCORE > VPA



Output net name	TraceWidth (mils)
VCORE_PMU	≥50
VAPROC_PMU	≥50
VPA_PMU	≥40
VDD1V8_PMU	≥20
VRF18_PMU	≥12

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MT6329 LDO OUTPUT

- VCAMA should be shielded by GND for noise prevention during the operation of camera.

Ball name	Net name	Trace width
VM12_1	VM12	As wide as possible (>15mil) / (10mil under chip area)
VM12_2	VM12_2	As wide as possible (>15mil) / (10mil under chip area)
VM_INT	VM_INT	As wide as possible (>15mil) / (10mil under chip area)
VRF28	VRF_PMU	As wide as possible (>15mil) / (10mil under chip area)
VTCXO	VTCXO_PMU	As wide as possible (>6mil) / (4mil under chip area)
VA1	VA1	As wide as possible (>15mil) / (10mil under chip area)
VA2	VA2	As wide as possible (>15mil) / (10mil under chip area)
VA2_S	VA2	4mil
VIO28	VIO28	As wide as possible (>20mil) / (10mil under chip area)
VSIM	VSIM	As wide as possible (>6mil) / (4mil under chip area)
VSIM2	VSIM2	As wide as possible (>6mil) / (4mil under chip area)
VMC	VMC	As wide as possible (>15mil) / (10mil under chip area)
VMCH	VMCH	As wide as possible (>20mil) / (10mil under chip area)
VGP	VGP	As wide as possible (>6mil) / (4mil under chip area)
VGP2	VGP2	As wide as possible (>10mil) / (6mil under chip area)
VUSB	VUSB	As wide as possible (>10mil) / (6mil under chip area)
VIBR	VIBR	As wide as possible (>10mil) / (6mil under chip area)
VRTC	VRTC	As wide as possible (>6mil) / (4mil under chip area)
VCAMA	VCAMA	As wide as possible (>15mil) / (10mil under chip area)
VCAMA_S	VCAMA	4mile
VCAM_AF	VCAM_AF	As wide as possible (>10mil) / (6mil under chip area)
VCAMD	VCAMD	As wide as possible (>10mil) / (6mil under chip area)
VCAM_IO	VCAM_IO	As wide as possible (>10mil) / (6mil under chip area)

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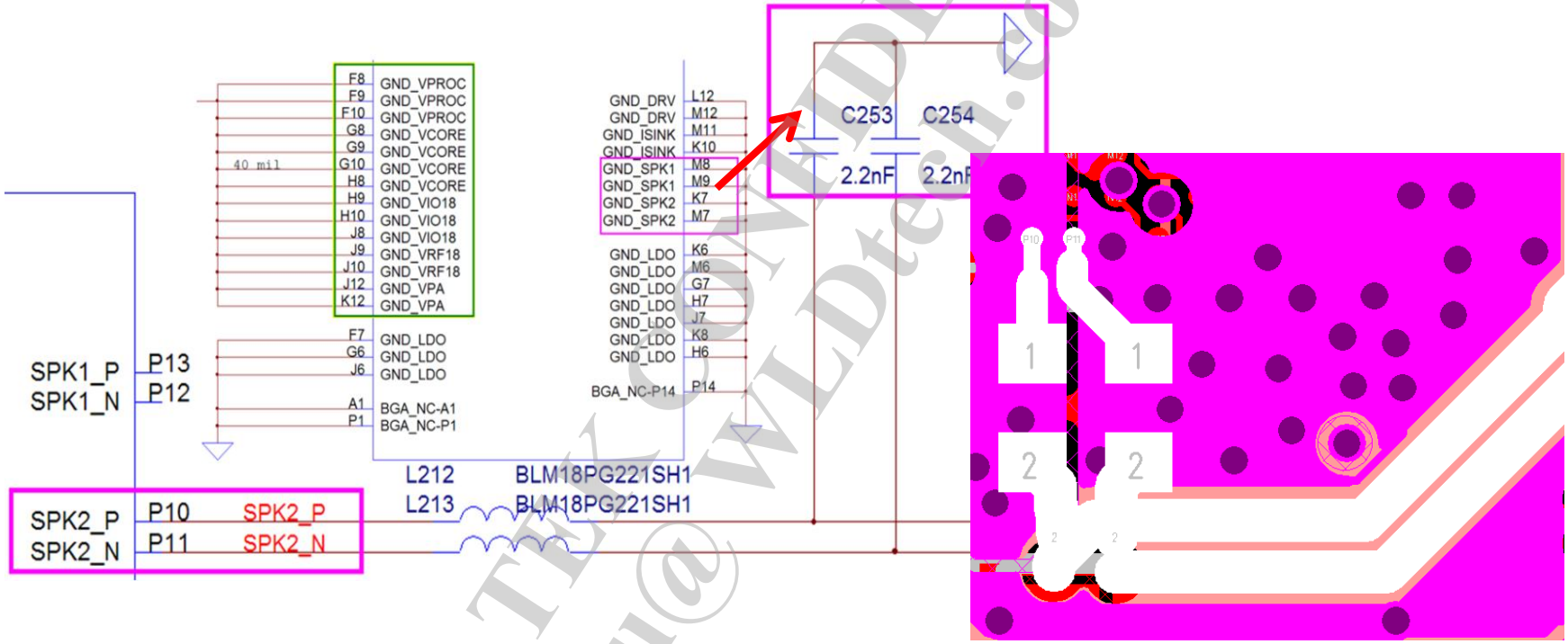
MT6329 SPEAKER

- The differential signals of Speaker should be shielded by GND on adjacent & up/down layers. Trace width≥ 20mi, add more GND vias along the GND shielding if possible, and its L/C should be placed close to MT6329.



- The GND pin of speaker's de-cap should be connected to the GND ball **M8/M9/K7/M7 first,** and then connect to the main GND layers independently.
- Connection trace width should ≥50mil. DO NOT connect these GND pins with BUCK GND due to BUCK GND is noisy.

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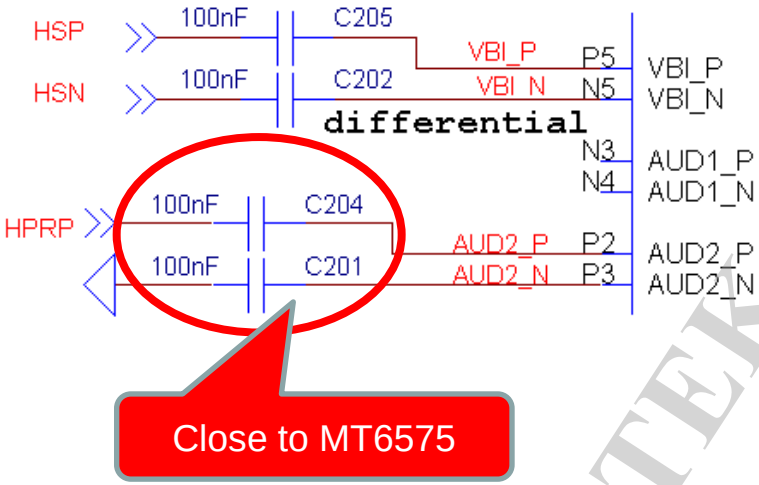
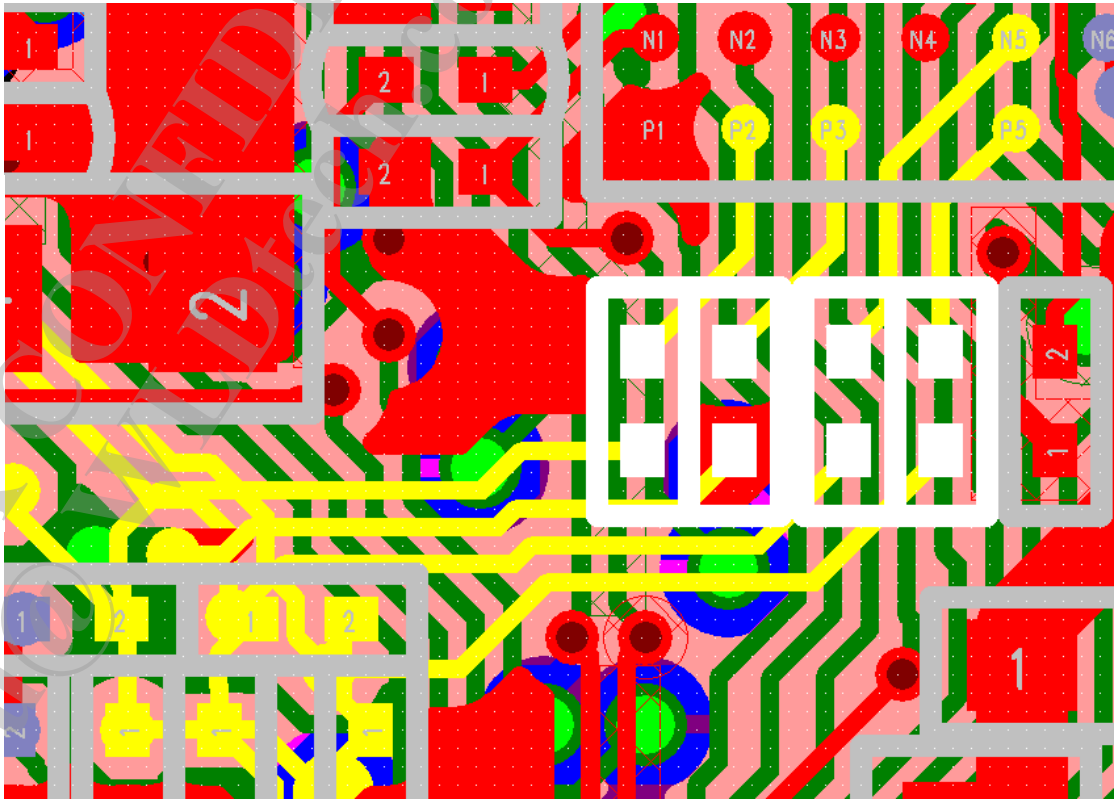
MT6329 AUDIO

- AUD1_P/N, AUD2_P/N, VBI_N/P are differential pairs, need be shielded by GND(adjacent & up/down layers).





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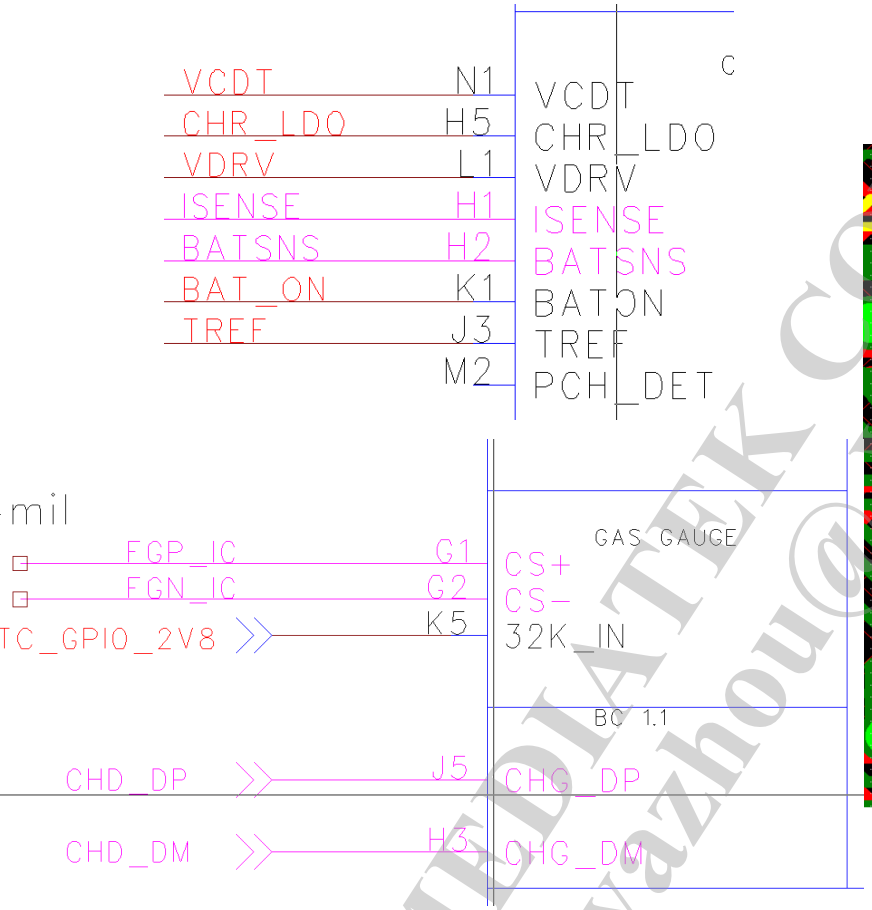
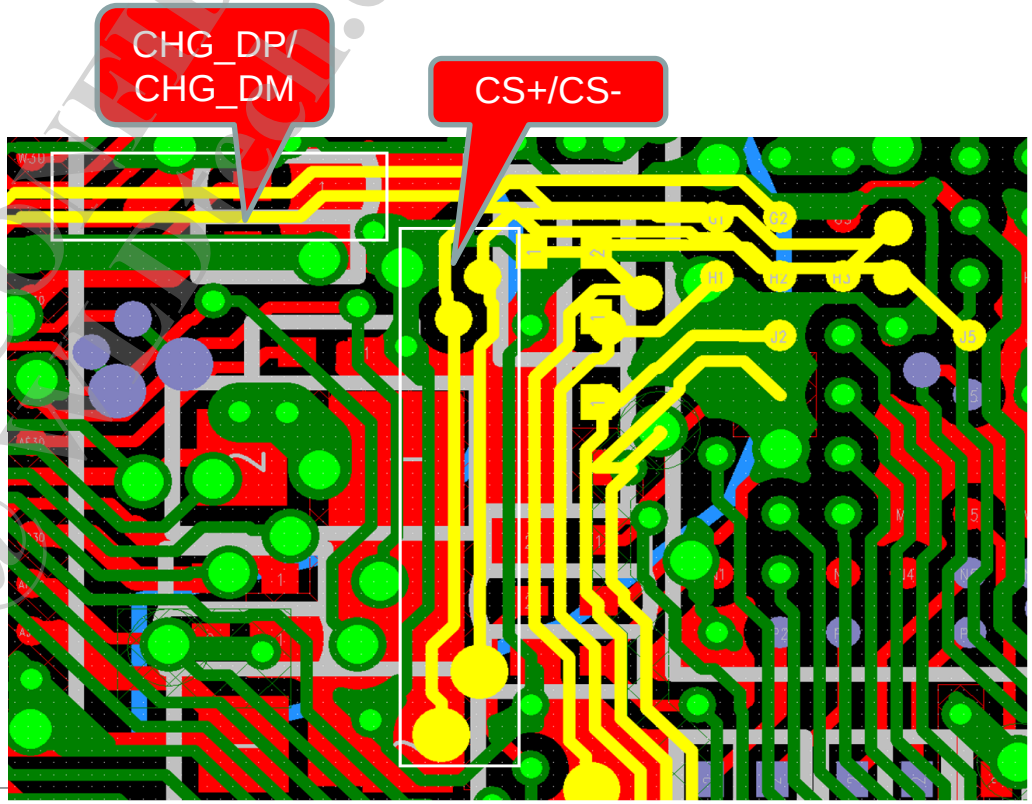
MT6329 OTHERS (1/3)

- ISENSE/BATSNS, CS+/CS-, and CHG_DP/CHG_DM should be routed as differential pairs with width/spacing of 4/4 mil respectively, and shielded by GND(adjacent & up/down layers).





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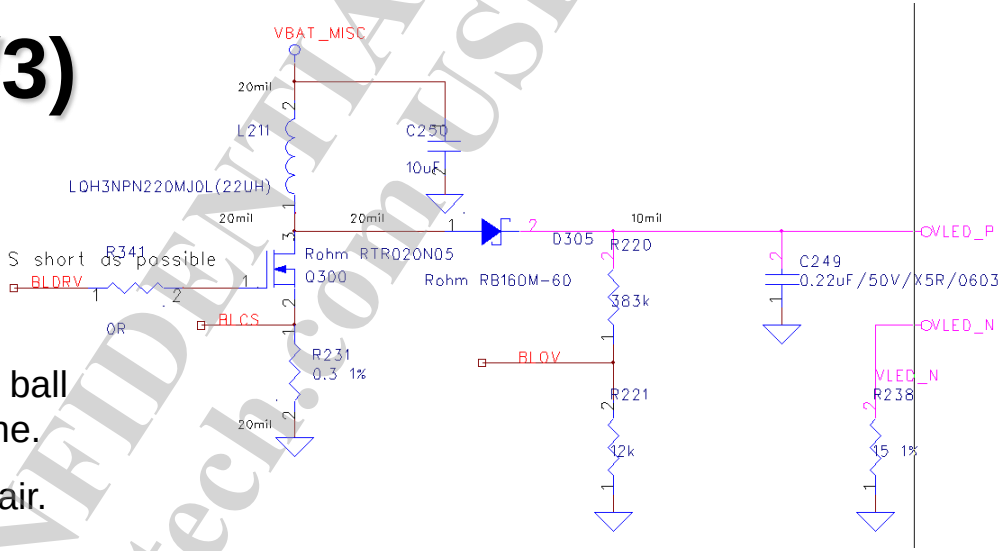
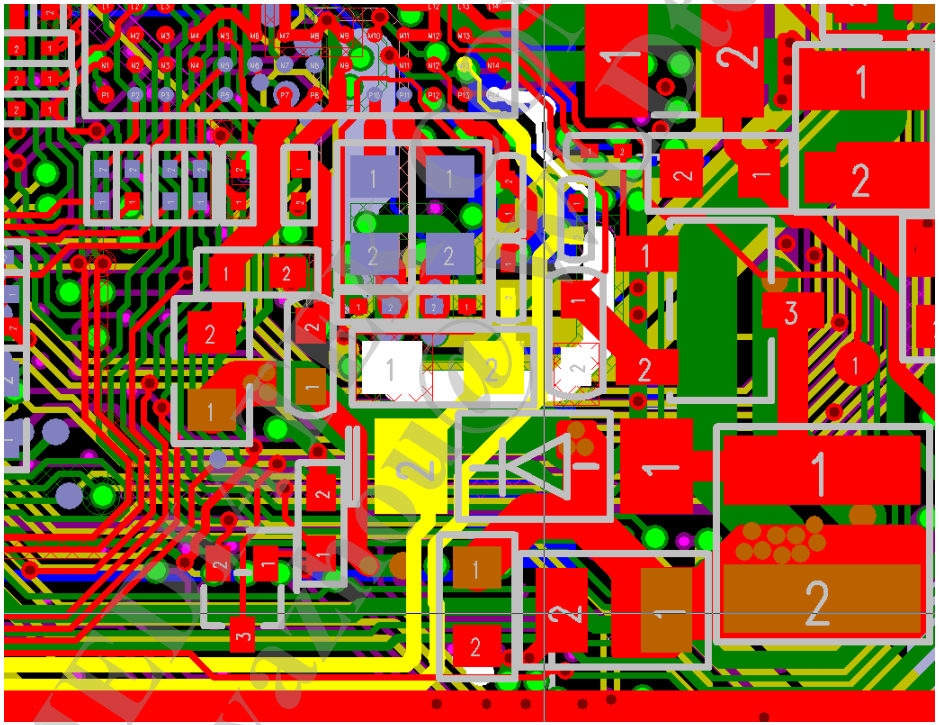
MT6329 OTHERS (2/3)

- Components show on the right figure should place close to MT6329.
- Route BLDRV as short as possible.
- GND pins of C249 & R238 should connect to ball P14 first, and then connect to main GND plane.
- Route VLED_P & VLED_N as a differential pair.





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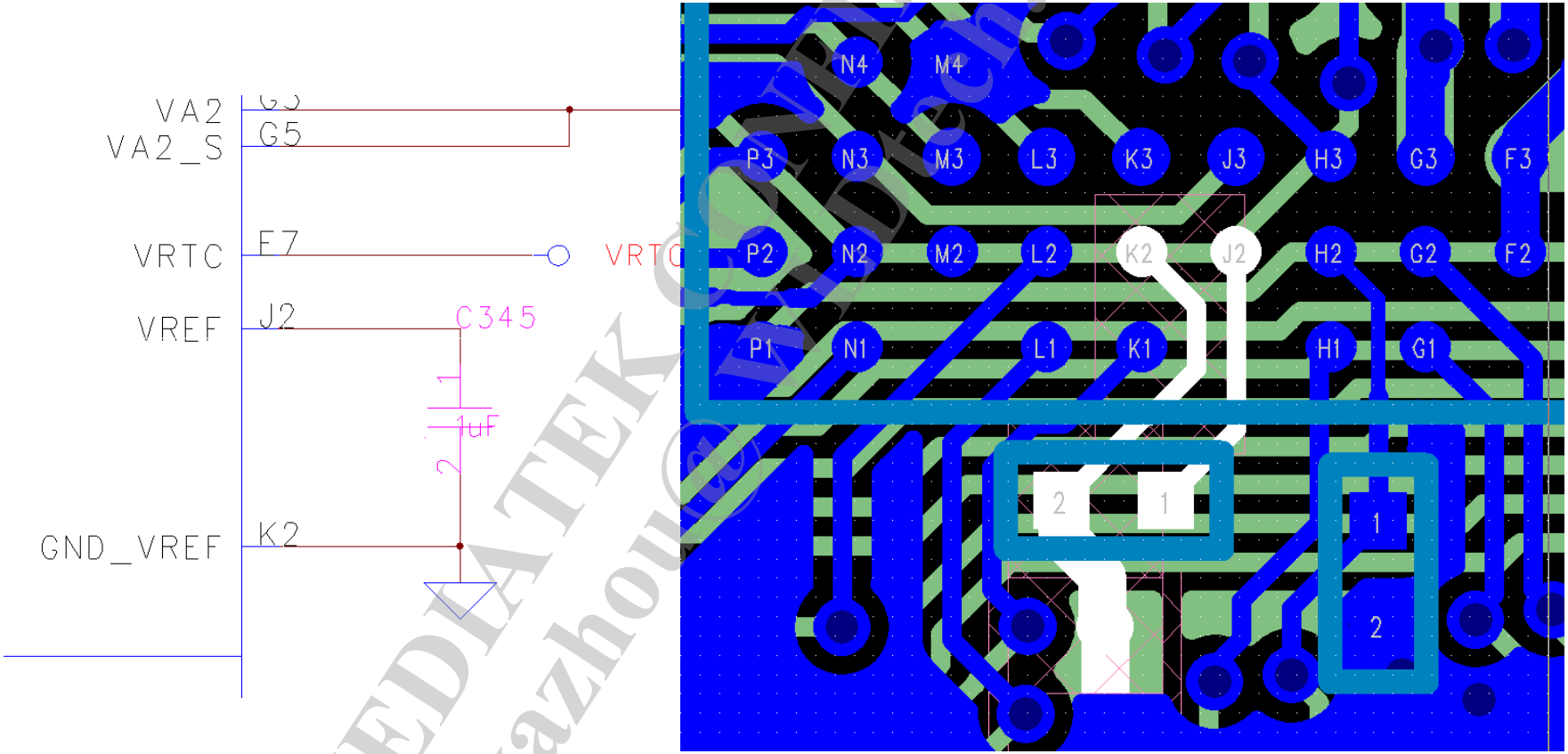
MT6329 OTHERS (3/3)

- Route J2/K2 signals as differential pair.
- Ball K2 should independently connect to C345's GND pin by 4mil trace, and then connect to main GND plane from C345's GND pin.



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