Group 3: LDPC codes in Memory

Tom Wang Natalie Balashov

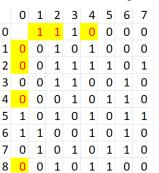
April 10th, 2024

Overview

- 1. Intro to LDPC Codes
- 2. Implementation of LDPC Codes in HDL
- 3. Implementation of Hamming Codes in HDL
- 4. Comparison of LDPC and Hamming Codes

Hamming implementation

- ➤ Typical Hamming codes in implementation uses 64-bit to 72-bit encoding schemes.
- This typical implementation is called **SECDED** (Single Error Correction, Double Error Detection) Hamming code.
- ► The concept of Hamming code is detecting errors in half of the codewords. And then with different combinations of deleting patterns, we can locate a single bit.



Example of correcting error

There are a total of 72 bits, which can be expressed in binary from $6'b000_0000$ to $6'b100_0111$.

Mark the unique position vector as vec[6:0] and let it be bijective to parity bits p[6:0].

We order the bits as shown below:

Figure: Number parity bits and data bits in a Hamming code.

FPGA Implementation

Logic can be easily achieved with a series of *xor gates* and *and gates*.

RTL viewer can be found on GitHub for Hamming72out and Hamming64in.

According to Quartus timing analysis, the highest frequency it can run is **387.3 MHz** under *slow 1100 mV 85C mode*.