Group 3: LDPC codes in Memory

Tom Wang
Natalie Balashov

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Overview

1. Intro to LDPC Codes
2. Implementation of LDPC Codes in HDL
3. Implementation of Hamming Codes in HDL
4. Comparison of LDPC and Hamming Codes

Hamming implementation

- Typical Hamming codes in implementation uses 64-bit to 72-bit encoding schemes.
- This typical implementation is called **SECDED** (Single Error Correction, Double Error Detection) Hamming code.
- The concept of Hamming code is detecting errors in half of the codewords. And then with different combinations of deleting patterns, we can locate a single bit.

	0	1	2	3	4	5	6	7
0		1	1	1	0	0	0	0
1	0	0	1	0	1	0	0	0
2	0	0	1	1	1	1	0	1
3	0	0	1	1	0	0	1	0
4	0	0	0	1	0	1	1	0
5	1	0	1	0	1	0	1	1
6	1	1	0	0	1	0	1	0
7	0	1	0	1	0	1	1	0
8	0	0	1	0	1	1	0	0

Figure: Parity bits and data bits in a Hamming code.

Example of correcting error

There are a total of 72 bits, which can be expressed in binary from $6'b000\_0000$ to $6'b100\_0111$.

Mark the unique position vector as `vec[6:0]` and let it be bijective to parity bits `p[6:0]`.

We order the bits as shown below:

	0	1	2	3	4	5	6	7
0	0	1	2	3	4	5	6	7
1	8	9	10	11	12	13	14	15
2	16	17	18	19	20	21	22	23
3	24	25	26	27	28	29	30	31
4	32	33	34	35	36	37	38	39
5	40	41	42	43	44	45	46	47
6	48	49	50	51	52	53	54	55
7	56	57	58	59	60	61	62	63
8	64	65	66	67	68	69	70	71

Figure: Number parity bits and data bits in a Hamming code.

FPGA Implementation

Logic can be easily achieved with a series of *xor gates* and *and gates*.
RTL viewer can be found on GitHub for Hamming72out and Hamming64in.
According to Quartus timing analysis, the highest frequency it can run is **387.3 MHz** under *slow 1100 mV 85C mode*.