

XINGYU (TOM) WANG

Bachelor of Applied Science in Computer Engineering

@fortily@student.ubc.ca @tomxingyuwang@gmail.com (+1)604-388-5164
luckunately.github.io www.linkedin.com/in/tom-wang-554904220/
https://github.com/luckunately



EXPERIENCE

FPGA Soft IP Engineering Intern

Altera

May 2025 – August 2026

Toronto, ON

- Develop Feature, verify functionality and reduce resource usage of the Test Engine IP, which sends memory traffic to the on-chip memory (HBM, DDRRAM) through NoC interface on FPGA.
- Collaborate with cross-functional teams to ensure seamless integration of the IP into larger FPGA designs, enhancing overall system performance and reliability.

Student Research Assistant

UBC

April 2024 – April 2025

Vancouver, BC

- Investigated supervised learning methods (LSTM, Transformer, etc.) for page prefetching using collected traces; achieved better results than heuristic algorithms (LEAP) on various workloads, with ongoing challenges in deployment and inference time.
- Supervision under: Shaurya Patel, Prof. Alexandra Fedorova in UBC Systopia Lab.

PROJECTS

Evaluating Cache Scheduling Strategies for vLLM Inference

January 2025 – April 2025

Vancouver, BC

- Experiment OS cache prefetching strategies to for vLLM inference.
- Explore adaptive watermark tuning techniques to optimize memory usage and scheduling.
- Report available at [my GitHub](#).

Capstone: Reinforcement Learning with SVT-AV1 Codec

January 2025 – August 2025

Vancouver, BC

- Used reinforcement learning to improve AV1 Codec constant bitrate mode by assigning Quantization Parameter (QP) offsets to superblocks within a frame, given a frame-level QP.
- Built an RL environment by exposing the C program API, enabling per-video optimization; generalization across different videos remains challenging.

Microsystem Design with Microprocessor

Jan 2024 – April 2024

Vancouver, BC

- Build memory, data bus, various I/O around a M68K CPU on FPGA. Interact with CPU using embedded C programming
- Implemented components including DRAM controller, Cache Controller, SPI, Canbus, I2C, ADC/DAC, and Simple RTOS with multi-threading and priority interrupts.
- Integrate the above components with VGA and Voice modules, and map addresses accordingly both in RTL design and C programming to produce a Tetris game with the M68K CPU

AWARDS



NSERC Awards

Natural Sciences and Engineering Research Council of Canada Undergraduate Student Research Award (USRA) for May 2024 - August 2024



Dean's Honors List

Academic Excellence Award 4 years in a row

SKILLS

SystemVerilog

C

Python

tcl

Perl

Pytorch

QEMU

EDUCATION

BASC. in Computer Engineering

University of British Columbia

Sept 2021 – Aug 2026

CGPA: 87%

Upper-level (3rd year+)

courses: 89%

Affiliations: Systopia Lab

Course Highlights:

- Compute Systems:** Computer Architecture, Digital & Microsystem Design, Computing Systems, VLSI, Accelerator Design
- Software:** Software Development, Data Structures & Algorithms, Operating Systems
- Other:** Machine Learning, Error Control Coding, Abstract Math, Video Codec