FPGA-BASED SYSTEM DESIGN LAB – MINI PROJECT - 2025

ABSTRACT REPORT

Project Title

Names of the group members with registration numbers

1. INTRODUCTION:
   a. Background information on the project.
   b. Objectives and scope of the project.
   c. Overview of the Verilog design and why it was chosen.
   d. Problem definition or motivation behind the project.

2. SYSTEM DESIGN AND ARCHITECTURE:
   a. High-level design overview (block diagram of the system).
   b. Description of the overall system architecture.
   c. Key modules and their interconnections.
   d. Explanation of design choices made for the architecture.

3. RESULTS:
   a. Expected simulation results (e.g., waveforms, output data).

4. CONCLUSION:
   Summarize the goals that are expected to be achieved by this project