Computer Architecture: Assignment 6 (Cache)

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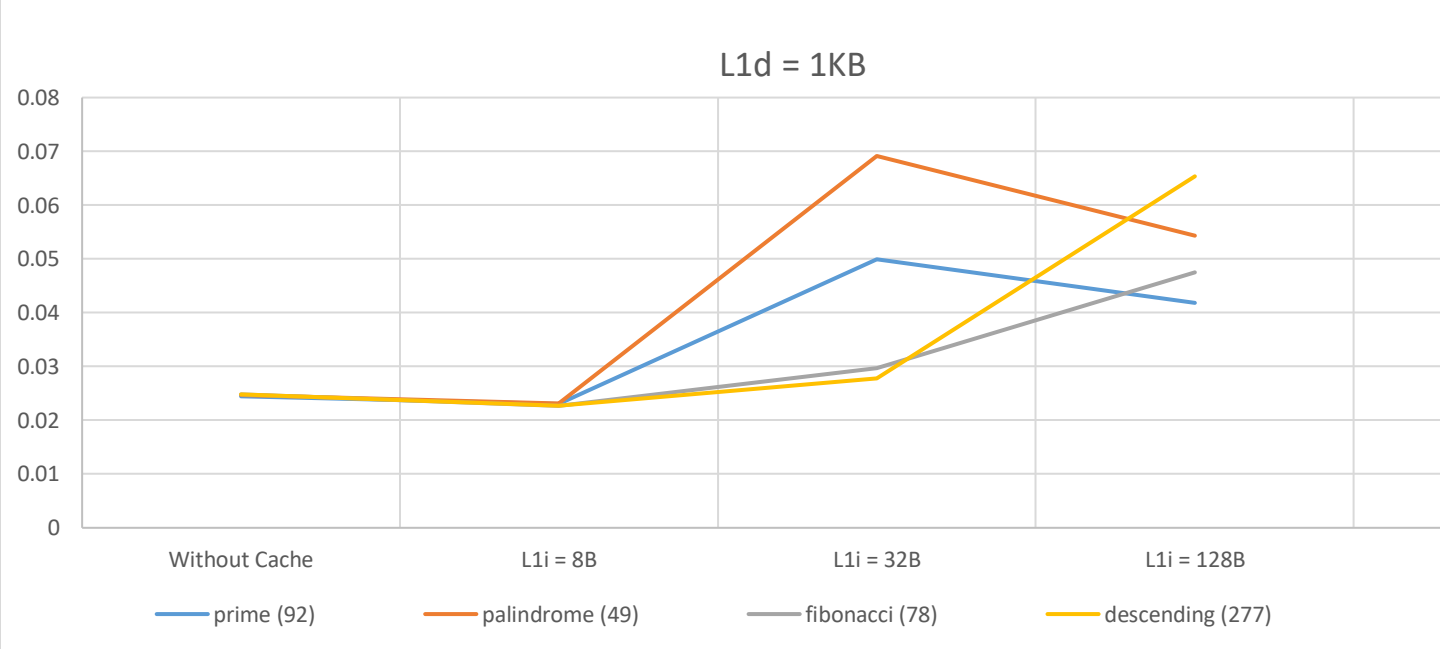
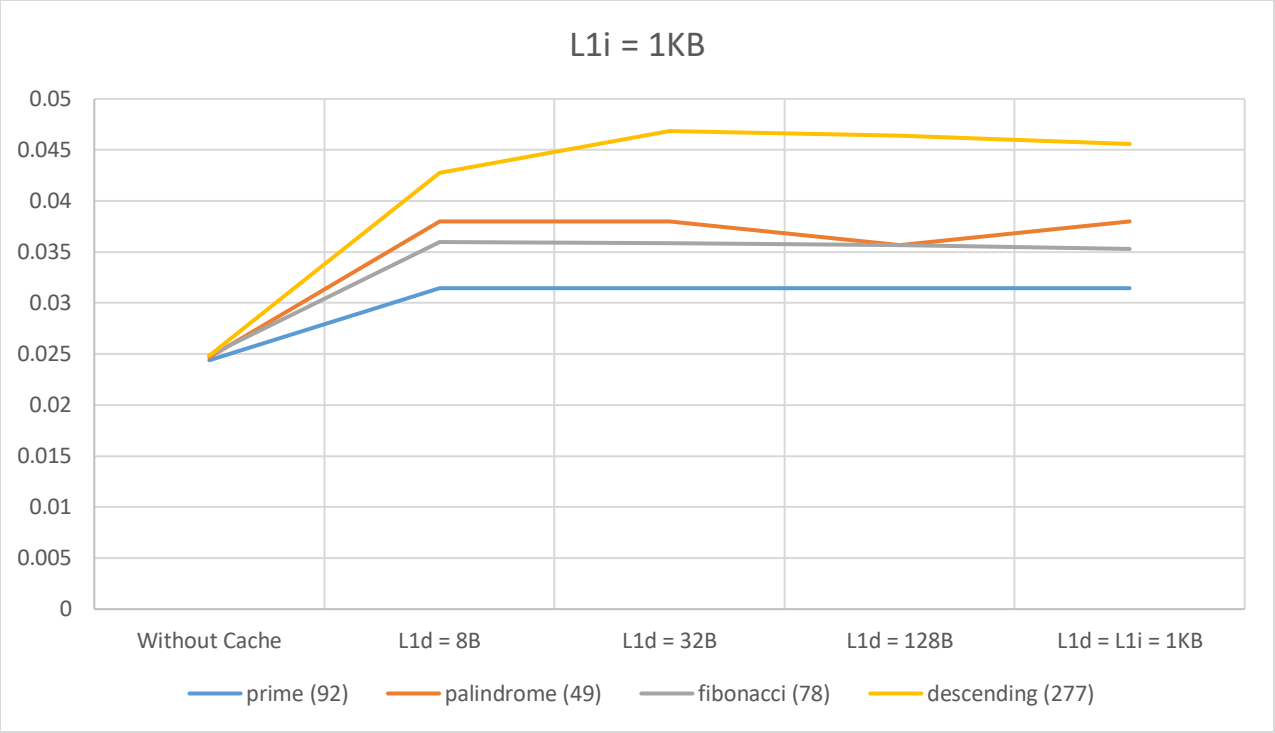
IPC for various program for different values of Cache

Program	IPC	L1d = 1KB			L1d = L1i = 1KB	L1i = 1KB		
	Without Cache	L1i = 8B	L1i = 32B	L1i = 128B		L1d = 128B	L1d = 32B	L1d = 8B
evenodd (6)	0.02419	0.022059	0.021277	0.019868	0.01734104	0.017341	0.017341	0.017341
prime (92)	0.02439	0.023035	0.049927	0.04182	0.031452358	0.031452	0.031452	0.031452
palindrome (49)	0.02468	0.023121	0.069136	0.054369	0.03799186	0.035687	0.037992	0.037992
fibonacci (78)	0.02486	0.022672	0.029709	0.047499	0.035311796	0.035687	0.035878	0.035974
descending (277)	0.02485	0.022703	0.027778	0.065354	0.045585115	0.04642	0.046849	0.042765



This is the plot of IPC for various values of L1i cache where L1d Cache size is fixed to 1KB

As L1i cache size increases, latency also increases, and so does the hit rate. There will be an optimum size of L1i cache where IPC is maximum



This is the plot of IPC for various values of L1d cache where L1i cache size is fixed to 1KB

Here also the latency increases with increment in cache size and hit rate also increases. There will be an optimum size of L1d cache where IPC is maximum