DATASHEET

芯鼎科技
iCatch Technology, Inc.

SPCA1627A

Digital Still Camera Controller

Preliminary

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Version 0.2

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Digital Still Camera Controller

1. GENERAL DESCRIPTION

1.1. Introduction

The SPCA1627A is a low cost digital still camera/camcorder SoC, which features with a full set of key modules required in a digital still camera. The SoC has embedded with iCatch's high quality image processing engine, high- speed JPEG CODEC and a wide range of peripheral interfaces, making a low cost DSC easy to be realized. In low cost camcorder application, SPCA1627A is capable of 720P HD video recording.

1.2. Terms

Abbreviation	Definition
AE	Automatic Exposure
AWB	Automatic White Balance
CODEC	Encoder and Decoder
Color DSP	Color image Digital Signal Processor
DMA	Direct Memory Access
I2C	Inter IC Control
ISP	In System Programming
LCM	Liquid Crystal display Module
MMC	Multi Media Card
PLL	Phase Lock Loop
SD	Secure Digital card
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

2. FEATURES

2.1. CPU

- 8032 with 8KB Data Memory and 2KB Program Memory
- Supports the ISP (In-System-Programming) function via USB
- Program code shadowing function to SDRAM

2.2. Peripheral

- One UART port
- Four PWM ports
- Three timers
- 2-channel general-purpose ADC
- GPIOs
- Embedded low-power Real-Time Clock (RTC) with alarm function

2.3. Memory Interface

- Supports SDRAM with the density of 16Mb to 128Mb
- Programmable DRAM operating frequencies up to 133MHz
- Supports down-grade SDRAM

2.4. Storage Media Interface

- Supports serial flash memory
- Supports MMC and SD memory cards
- Support eMMC/eSD
- Embedded card power supply

2.5. Sensor

- Supports all popular CMOS image sensors
- Image resolution up to 12M pixels
- Supports Digital TV Input, CCIR601 (8-bit data bus) and CCIR656
- Sensor clock up to 96MHz
- I2C serial control port for sensor parameter setting
- Accurate flash light control at pixel level
- Mechanical shutter control
- Support 1.8V sensor interface

2.6. Display

- Supports Digital LCD Display Interface
- Supports ITU-R BT 601 digital video output interface
- Built-in TV encoder to support direct output analog NTSC, PAL and PAL-M composite video signals
- Programmable luminance (contrast, brightness) and chrominance (hue, saturation) control for display
- Support both font-based OSD and graphics-based OSD
- Color correction matrix and edge enhancement
- Supports LCM interface
- Support 1.8V display interface

2.7. Color DSP

- Support RGB Bayer patterns output and YUV422 output sensor.
- Support both master mode and slave mode CMOS sensors.
- Programmable frame rate.
- On-chip color processing engine
- AWB window statistics
  - 2-D edge enhancement with Programmable Gain Curve
  - Luminance histogram
  - Hue/Saturation adjustment
- Brightness/Contrast adjustment
  - Programmable edge enhancement
- Bad pixel concealment can be done by hard-wired engine or by the user-defined firmware.
- Fully programmable Gamma table
- 4 channels 2-D Lens Shading Compensation
- Low-light Green Noise Suppression
- Color Noise Suppression
- Spatial and Tempo Noise Reduction
- Wide Dynamic Range Imaging
- Hardware Face detect and track technology
- Support special image effects such as negative, Solaris, emboss, binaries, sepia, black/white

2.8. Still Image and Video Compression

- Motion JPEG 1280x720 (HD) resolution CODEC up to 30 fps
- Digital image stabilization engine

2.9. USB

- USB 2.0 High Speed function with built-in USB2.0 PHY
- Supports USB Mass Storage Class / Audio Class / Video Class / Still Image Class
- Supports PICTBRIDGE / DPS(Direct Print Standard)

2.10. Audio

- Built-in mono audio ADC for microphone input
- Built-in 250mW amplifier for directly speaker output

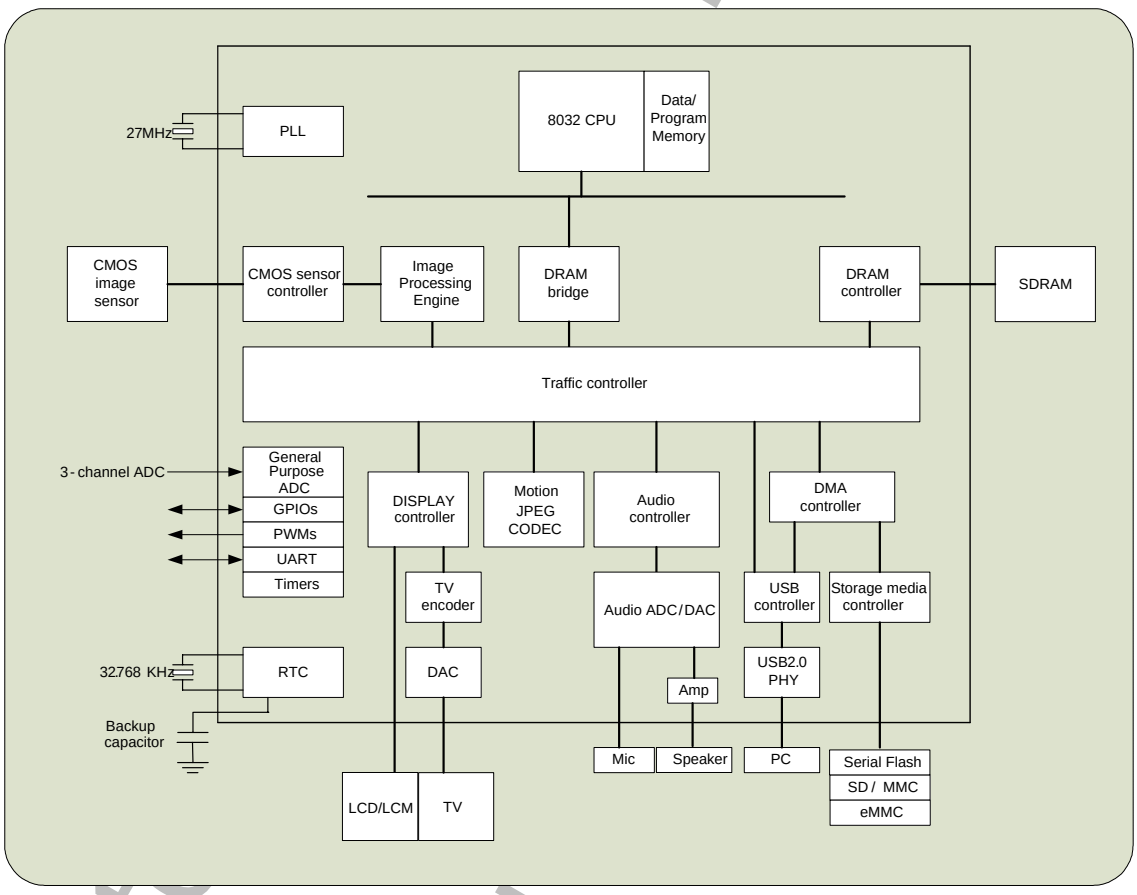
2.11. Package and Power

- 3.3V IO power supply
- 1.8V core power supply
- 128-pin LQFP package

3. BLOCK DIAGRAM

3.1. Block Diagram

The following diagram depicts the internal structure of SPCA1627A and a typical connection to the external devices.



3.2. FUNCTIONAL DESCRIPTIONS

3.2.1. CMOS Sensor Controller

The sensor interface connects to CMOS sensors. It can also connect to a video decoder to capture video. A serial interface is used to program CMOS sensors.

3.2.2. RTC

The RTC module enables the SPCA1627A to maintain the calendar function with minimum power consumption.

3.2.3. PLL

The SPCA1627A has on-chip PLLs to generate all the internal operation clocks, which enables a single crystal (27MHz) system application design.

3.2.4. 8032 CPU

The built-in 8032 CPU coordinates camera operation.

3.2.5. Display Controller

This module has integrated a variety of digital interfaces, which include TFT LCD interface, LCM interface, It also integrates a TV encoder, supporting both NTSC, PAL and PAL-M composite video outputs. Both font-based and graphics-based OSD function are also implemented in this module.

3.2.6. Image Processing Engine

The Image processing engine of the SPCA1627A is a very flexible pipeline. It will perform color interpolation, gamma correction, image scaling for digital zoom, and image enhancement filtering. It also has real-time AF/AE/AWB statistic engines to provide data for computing the optimal control parameters. All the functions are controlled by a set of programmable registers, allowing users to fine-tune the image quality.

3.2.7. JPEG CODEC

This image compression engine can generate JPEG compressed files in JFIF and EXIF format with firmware support. The engine can also decode JPEG compressed images for playback.

3.2.8. DRAM Controller

The DRAM controller provides an access path to the SDRAM for other internal modules of the SPCA1627A. Many special functions are also implemented in this module. For example, image scaling, copy and paste of image parts, image rotation, … etc.

3.2.9. DMA Controller

The DMA controller allows high-speed data transfer between SPCA1627A internal modules.

3.2.10. Storage Media Controller

Storage Media Controller is a high efficiency bridge between different storage media protocols and the internal buses. Both DMA data transfer and PIO data transfer are supported.

3.2.11. USB2.0 High Speed Controller

The USB controller, in which high-performance USB2.0 PHY is integrated, supports USB2.0 full speed and high speed data transfer. SPCA1627A supports all types of USB pipes, including control, bulk, ISO and interrupt pipes. Totally, eight USB endpoints are implemented in SPCA1627A controller. The following table summarizes the function of each endpoint.

Endpoint	Function
0	Control endpoint as default pipe
1	Video ISO IN endpoint
2	Bulk IN endpoint for MSDC
3	Bulk OUT endpoint for MSDC
4	Interrupt IN endpoint for SIDC
5	Interrupt IN endpoint for audio status
6	ISO IN endpoint for audio data
7	Interrupt IN endpoint for debugging

4. PIN DESCRIPTIONS

4.1. Pin Descriptions

4.1.1. SDRAM Interface (37)

No.	Name	Dir.	Description			Memo
1	xsdramclk	O	SDRAM clock			
2	xras_n	O	SDRAM raw address strobe signal			
3	xcas_n	O	SDRAM column address strobe signal			
4	xmwe_n	O	SDRAM write enable signal			
5	xldqm	O	SDRAM data mask signal, low byte			
6	xudqm	O	SDRAM data mask signal, high byte			
7	xcke	O	SDRAM clock enable signal			
8	xmd[0]	B	SDRAM data bus, bit 0			
9	xmd[1]	B	SDRAM data bus, bit 1			
10	xmd[2]	B	SDRAM data bus, bit 2			
11	xmd[3]	B	SDRAM data bus, bit 3			
12	xmd[4]	B	SDRAM data bus, bit 4			
13	xmd[5]	B	SDRAM data bus, bit 5			
14	xmd[6]	B	SDRAM data bus, bit 6			
15	xmd[7]	B	SDRAM data bus, bit 7			
16	xmd[8]	B	SDRAM data bus, bit 8			
17	xmd[9]	B	SDRAM data bus, bit 9			
18	xmd[10]	B	SDRAM data bus, bit 10			
19	xmd[11]	B	SDRAM data bus, bit 11			
20	xmd[12]	B	SDRAM data bus, bit 12			
21	xmd[13]	B	SDRAM data bus, bit 13			
22	xmd[14]	B	SDRAM data bus, bit 14			
23	xmd[15]	B	SDRAM data bus, bit 15			
24	xma[0]	B	SDRAM address bus, bit 0			
25	xma[1]	B	SDRAM address bus, bit 1			
26	xma[2]	B	SDRAM address bus, bit 2			
27	xma[3]	B	SDRAM address bus, bit 3			
28	xma[4]	B	SDRAM address bus, bit 4			
29	xma[5]	B	SDRAM address bus, bit 5			
30	xma[6]	O	SDRAM address bus, bit 6			
31	xma[7]	O	SDRAM address bus, bit 7			
32	xma[8]	O	SDRAM address bus, bit 8			
33	xma[9]	O	SDRAM address bus, bit 9			
34	xma[10]	O	SDRAM address bus, bit 10			
35	xma[11]	O	SDRAM address bus, bit 11			
				64M bit	128M bit	
36	xma[12]	O	BA	BA0	BA0	
37	xma[13]	O	NC	BA1	BA1	

4.1.2. Storage media interface (10)

No.	Name	Dir.	Description			Memo
			Boot source		Storage Card	
			Serial-Flash	eSD/eMMC	SD/MMC	
1	xfmgpio[0]	B	CE	eMMC_D0		
2	xfmgpio[1]	B	SI (IO0)	eMMC_D1		
3	xfmgpio[2]	B	SCK	eMMC_CLK		
4	xfmgpio[3]	B	SO (IO1)	eMMC_D2		
5	xfmgpio[4]	B			CLK (O)	
6	xfmgpio[5]	B			DAT0 (B)	
7	xfmgpio[6]	B			DAT1 (B)	
8	xfmgpio[7]	B			DAT2 (B)	
9	xfmgpio[8]	B	WP (IO2)	eMMC_D3	DAT3 (B)	
10	xfmgpio[9]	B	HOLD (IO3)	eMMC_CMD	CMD (B)	

4.1.3. AUDIO/SAR (9)

No.	Name	Dir.	Description	Memo
1	MICBIAS	O	Buffered voltage output suitable for electro-microphone-capsule biasing.	
2	VREFF	O	Reference voltage for ADC	
3	MICINP	I	Microphone positive input.	
4	MICINN	I	Microphone negative input.	
5	SPOUTP	O	Positive differential analog output signal for external speaker	
6	SPOUTN	O	Negative differential analog output signal for external speaker	
7	LINEOUT	O	One channel lineout for TV audio input	
8	SAR0	I	SAR ADC channel 1	
9	SAR2	I	SAR ADC channel 3	

4.1.4. Video DAC interface (1)

No.	Name	Dir.	Description	Memo
1	COUT	O	Composite video signal output	

4.1.5. Digital TV interface (12)

No.	Name	Dir.	Description				Memo
			CCIR601	LCD	LCM	PROBE	
1	xdigtv[0]	B	DDX0	DDX0	D0	Probe1_0	
2	xdigtv[1]	B	DDX1	DDX1	D1	Probe1_1	
3	xdigtv[2]	B	DDX2	DDX2	D2	Probe1_2	
4	xdigtv[3]	B	DDX3	DDX3	D3	Probe1_3	
5	xdigtv[4]	B	DDX4	DDX4	D4	Probe1_4	
6	xdigtv[5]	B	DDX5	DDX5	D5	Probe1_5	
7	xdigtv[6]	B	DDX6	DDX6	D6	Probe1_6	
8	xdigtv[7]	B	DDX7	DDX7	D7	Probe1_7	

No.	Name	Dir.	Description				Memo
9	xdigtv[8]	B		DEM	D8(VSYNC)		
10	xdigtv[9]	B	VSYNC	VSD	CS		
11	xdigtv[10]	B	HSYNC	HSD	A0		
12	xdigtv[11]	B	DCLK	DCLK	WR	LCM_RESET	

4.1.6. Sensor Interface (14)

No.	Name	Dir.	Description		Memo
1	xrgb[2]	I	Sensor data input bit 0	TV decoder data input bit0	
2	xrgb[3]	I	Sensor data input bit 1	TV decoder data input bit1	
3	xrgb[4]	I	Sensor data input bit 2	TV decoder data input bit2	
4	xrgb[5]	I	Sensor data input bit 3	TV decoder data input bit3	
5	xrgb[6]	I	Sensor data input bit 4	TV decoder data input bit4	
6	xrgb[7]	I	Sensor data input bit 5	TV decoder data input bit5	
7	xrgb[8]	I	Sensor data input bit 6	TV decoder data input bit6	
8	xrgb[9]	I	Sensor data input bit 7	TV decoder data input bit7	
9	tggpio[0]	B	Vertical synchronization signal		
10	tggpio[1]	B	Horizontal synchronization signal		
11	tggpio[2]	B	Sensor master clock		
12	tggpio[3]	B	Sensor pixel clock		
13	tggpio[4]	O	SSISCL		
14	tggpio[5]	B	SSISDA		

4.1.7. USB interface (3)

No.	Name	Dir.	Description	Memo
1	DP	B	USB data plus.	
2	DM	B	USB data minus.	
3	REXT	O	External register pin	

4.1.8. System (5)

No.	Name	Dir.	Description	Memo
1	LVDI	I	Low power detect input	
2	xtal27i	I	27MHz crystal pad input	
3	xtal27o	O	27MHz crystal pad output	
4	xtalrtco	O	32768Hz crystal pad output	
5	xtalrtci	I	32768Hz crystal pad input	

4.1.9. GPIO Pins (11)

No.	Name	Dir.	Description		Memo
			Description	Function	
1	gpio[0]	B	General purpose IO bit 0	SD_WPb	

No.	Name	Dir.	Description				Memo
2	gpio[1]	B	General purpose IO bit 1				
3	gpio[2]	B	General purpose IO bit 2				
4	gpio[3]	B	General purpose IO bit 3	UART_RX			
5	gpio[4]	B	General purpose IO bit 4	LED_SELF	PWM0	UART_TX	
6	gpio[5]	B	General purpose IO bit 5	LED_BUSY	PWM1		
7	gpio[6]	B	General purpose IO bit 6	LCM_BLEN	PWM2		
8	gpio[7]	B	General purpose IO bit 7	POWER_HOLD			
9	gpio[8]	B	General purpose IO bit 8				
10	gpio[9]	B	General purpose IO bit 9				
11	gpio[10]	B	General purpose IO bit 10				

4.1.10. Power (26

No.	Name	Dir.	Description		Memo
1	PMOS_VDD	P	3.3V power supply for Power MOS	OVDD	
2	CARD_POWER	P	3.3V output for card power		
3	AVDD_PLL	P	Crystal power	AVDD_PLL	
4	AVSS_PLL	P	Crystal ground	AVSS_PLL	
5	AVDD_USB	P	USB power		
6	AVSS_USB	P	USB ground		
7	AVSS_VDAC	P	VDAC ground		
8	AVDD_RTC	P	RTC power		
9	AVSS	P	RTC ground	AVSS_SPK	
10	AVDD_SPK	P	Audio speaker power		
11	SENVDD	P	Sensor interface power		
12	LCDVDD	P	LCD interface power		
13	OVDD	P	IO power		
14	OVDD	P	IO power		
15	OVDD	P	IO power		
16	DVDD	P	Core power		
17	DVDD	P	Core power		
18	DVDD	P	Core power		
19	DVDD	P	Core power		
20	DVDD	P	Core power		
21	OVSS	P	IO ground		
22	VSS	P	Ground		
23	VSS	P	Ground		
24	VSS	P	Ground		
25	VSS	P	Ground		
26	VSS	P	Ground		

4.2. IO-TRAP Pins

The IO-TRAP circuit is used to set the hardware configurations of the SPCA1627A. Parts of MA pins are used for the IO-TRAP function. The IO-TRAP configuration is as below:

Pin Name	IO-trap	Description
MA[0]	IOTRAP[0]	Reserved. Please do not add external pull-up resistor.
MA[1]	IOTRAP[1]	Fast reset selection. 1'b0: Normal mode. The internal reset control circuit keeps resetting SPCA1627A core until on chip PLL reaches the stable state. 1'b1: Fast reset mode. The reset control circuit resets SPCA1627A core for 32 crystal clocks. This mode is used in chip test only.
MA[2]	IOTRAP[2]	Reserved. Please do not add external pull-up resistor.
MA[3]	IOTRAP[3]	Reserved. Please do not add external pull-up resistor.
MA[4]	IOTRAP[4]	USB mode selection. 1'b0: High speed. 1'b1: Full speed.
MA[5]	IOTRAP[5]	Loader mode selection. 1'b0: Normal boot. 1'b1: ISP for firmware update
MA[6]	IOTRAP[6]	Boot mode selection. 1'b0: Boot from SPI. 1'b1: Boot from eMMC.
MA[7]	IOTRAP[7]	Reserved. Please do not add external pull-up resistor.
MA[8]	IOTRAP[8]	Reserved. Please do not add external pull-up resistor.

5. ELECTRICAL SPECIFICATION

5.1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V_T	-0.4 to 4.0	V
Supply Voltage relative to VSS	VDD	-0.4 to 4.0	V
Operating temperature	T_{OPT}	-10 to +70	°C
Storage temperature	T_{STG}	-55 to 125	°C
HBM	V_{HBM}	> 2000	V
MM	V_{MM}	> 200	V
LatchUp	I_t	> 100	mA

5.2. DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	I/O operating voltage	3.0	3.3	3.6	V
	Core operating voltage	1.62	1.8	1.98	V
I_{DD}	I_{core} (Suspend)	-	18	-	µA
I_{DD}	I_{IO} (Preview)	-	46.7	-	mA
	I_{core} (Preview)	-	60.7	-	
I_{DD}	I_{IO} (Snap)	-	51.3	-	mA
	I_{core} (Snap)	-	75.1	-	
I_{DD}	I_{IO} (Still Playback)	-	43.2	-	mA
	I_{core} (Still Playback)	-	54.7	-	
I_{DD}	I_{IO} (Video Clip)	-	44.4	-	mA
	I_{core} (Video Clip)	-	65.6	-	
I_{DD}	I_{IO} (Video Playback)	-	52.9	-	mA
	I_{core} (Video Playback)	-	52.9	-	

Symbol	Parameter	Min	Typ.	Max	Unit
V_{IL}	Input low voltage	-0.3	-	0.3 VDD	V
V_{IH}	Input high voltage	0.7 VDD	-	VDD+10%	V
I_{OL}	Output low current	-	2/4/6/8/12/16	-	mA
I_{OH}	Output high current	-	-2/-4/-6/-8/-12/-16	-	mA
V_{T+}	Schmitt trigger positive-going threshold	-	1.5	-	V
V_{T-}	Schmitt trigger negative-going threshold	-	1.2	-	V
V_{HYS}	Hysteresis voltage	-	0.3	-	V
I_{IL}	Input leakage current	-	-	1	µA

5.3. RTC Parameters

Symbol	Parameter	Min	Typ.	Max	Unit
IRTC	Current Consumption, VRTC＝3.3V	-	2	-	µA

RTC accuracy: +/- 2.5 seconds/day

5.4. USB Interface Characteristics

5.4.1. USB DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
Input Levels (full speed)					
V_{IH}	Input level high (driven)	2.0	-	-	V
V_{IHZ}	Input level high (floating)	2.7	-	3.6	V
V_{IL}	Input level low	-	-	0.8	V
V_{DI}	Differential input sensitivity	0.2	-	-	V
Input Levels (high speed)					
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	100	-	150	mV
Output Levels (full speed)					
V_{OL}	Output level low	0.0	-	0.3	V
V_{OH}	Output level high	2.8	-	3.6	V
V_{CRS}	Output signal crossover voltage	1.3	-	2.0	V
Output Levels (high speed)					
VHSOI	High-speed idle level	-10.0	-	10.0	mV
VHSOH	High-speed data signaling high	360	-	440	mV
VHSOL	High-speed data signaling low	-10.0	-	10.0	mV
VCHIRPJ	Chirp J level (differential voltage)	700	-	1100	mV
VCHIRPK	Chirp K level (differential voltage)	-900	-	-500	mV

5.4.2. USB AC Characteristics

Full Speed

Symbol	Parameter	Min.	Typ.	Max.	Unit
Driver Characteristics					
T_{FR}	Rise time	4	-	20	ns
T_{FF}	Fall time	4	-	20	ns
T_{RFM}	Differential Rise and Fall time matching (T_{FR}/T_{FF})	90	-	111.11	%
Clock Timing					
T_{FDRATE}	Average bit rate	-	12.00	-	Mb/s
Full Speed Data Timing					
T_{FDEOP}	EOP width	-	166.67	-	ns
Paired JK jitter	Source jitter for paired JK jitter	-	-	1.00	ns
Paired KJ jitter	Source jitter for paired KJ jitter	-	-	1.00	ns

High Speed

Symbol	Parameter	Min.	Typ.	Max.	Unit
Driver Characteristics					
T_{HSR}	Rise time	500	-	-	ps
T_{HSF}	Fall time	500	-	-	ps
Clock Timing					
T_{HSDRAT}	High-speed data rate	479.760	-	480.240	b/s
T_{HSFRAM}	Microframe interval	124.9375	-	125.0625	ps

5.5. Analog Video Interface Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Power supply		3.0	3.0	3.6	V
Resolution		-	9	-	bit
INL		-	±3	-	LSB
DNL		-	±0.5	-	LSB
Clock frequency		-	27	-	MHz
Output voltage	R_{set}=390ohm	1.27	1.3	1.43	V

5.6. Analog Audio Interface Characteristics

(T_A =25°C, AVDD =3.3V±10%, DVDD=1.8V±10%)

Parameter	Condition	Min.	Typ.	Max.	Unit
Input voltage (MICINP-MICINN)	Boost gain = 20dB PGA gain = 0dB	-	-	**AVDD**/13.75	Vpp
Microphone input resistance	Boost gain = 20dB	-	10K	-	Ω
Microphone input capacitance		-	10P	-	F
Frequency response		20	-	19,200	Hz
Boost amplifier: Gain Range		0	-	20	dB
Step Size		-	20	-	dB
Step Variation		-	2	-	dB
PGA: Gain Range		-12	-	33	dB
Step Size		-	1.5	-	dB
Step Variation		-	0.15	-	dB
Signal to noise ratio (SNR)	F_{IN} = 1kHz, PGA gain = 0dB	-	85	-	dB
Total harmonic distortion + noise (THD+N)	F_{IN} = 1kHz, PGA gain = 0dB	-	-	0.01	%

(T_A=25°C, AVDD=3.3V±10%, DVDD=1.8V±10%, $Clock_{ADMCLK}$=12.288MHz)

Parameter	Condition	Min.	Typ.	Max.	Unit
Bias voltage		-	0.75* **AVDD**	-	V
Bias current source		-	-	3.5	mA
Output noise voltage	1kHz~20kHz	-	25	-	nV/(Hz^0.5)

5.7. General-Purpose ADC Characteristics

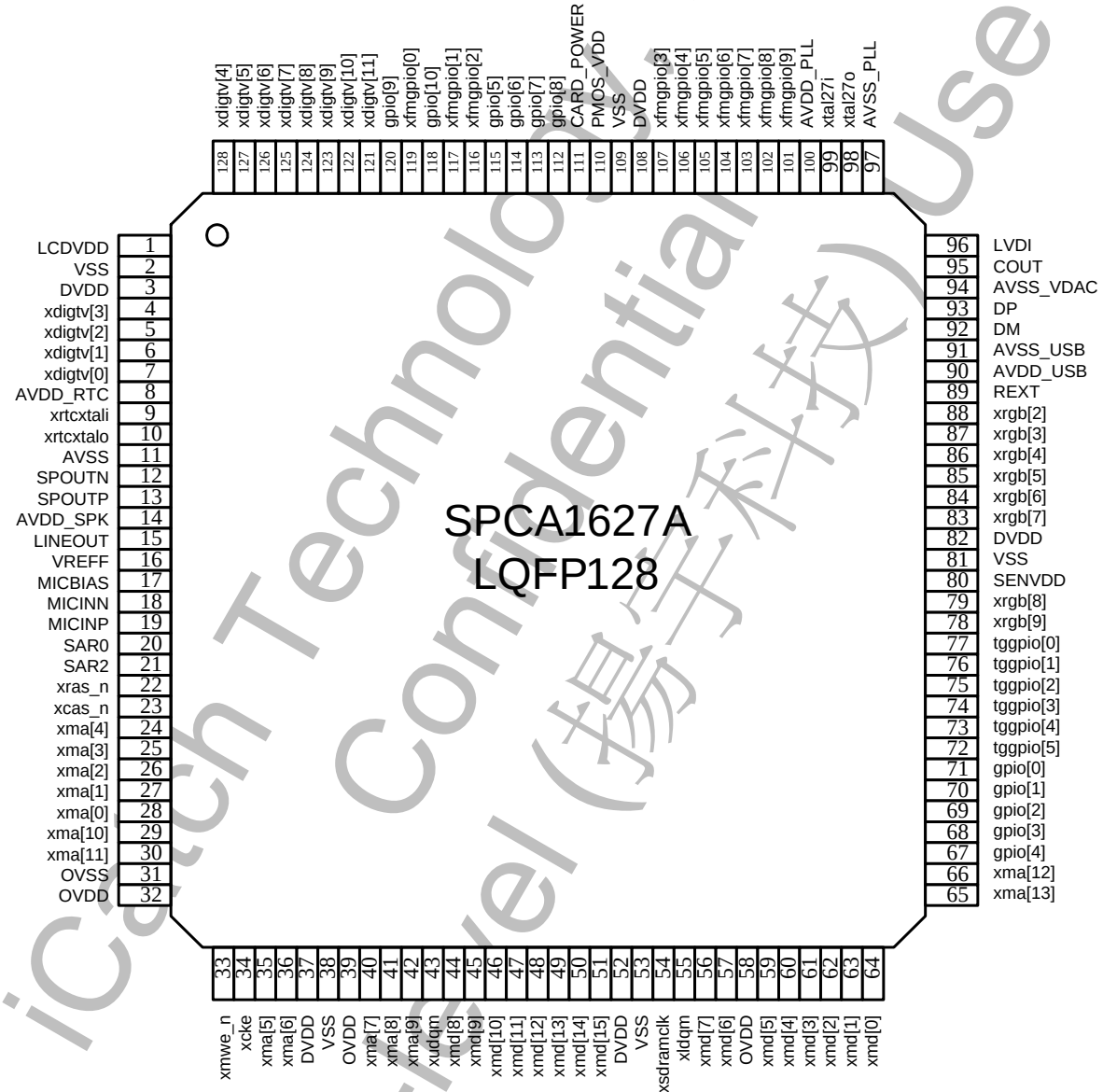
(T_A =25°C, AVDD =3.3V±10%, DVDD=1.8V±10%)

Parameter	Condition	Min.	Typ.	Max.	Unit
Input voltage range		0	-	**AVDD**	V
Input resistance	(SARIN0~SARIN2)	-	-	infinite	Ω
Resolution		-	-	10	bit
No missing codes		-	-	10	bit
Differential Nonlinearity		-	±1	±2	LSB
Integral Nonlinearity		-	±2	±4	LSB

6. PACKAGE INFORMATION

6.1. Pin Assignment

6.1.1. LQFP 128-pin Package



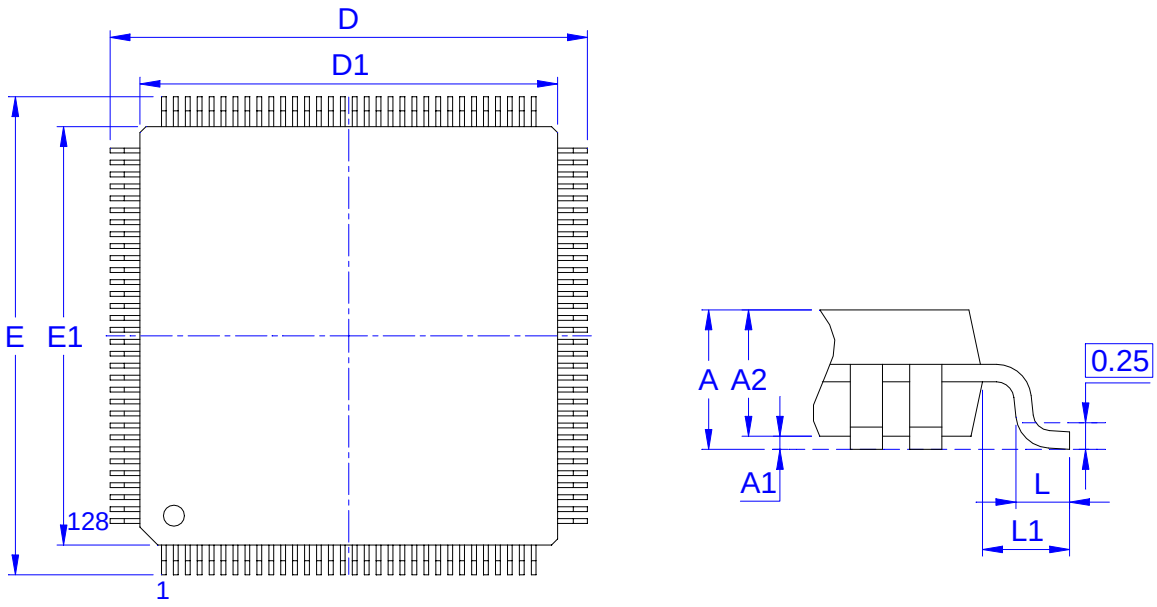
6.2. Pin Name

6.2.1. LQFP 128-pin Package

Pin NO.	Pin Name	Pin NO.	Pin Name	Pin NO.	Pin Name	Pin NO.	Pin Name
1	LCDVDD	33	xmwe_n	65	xma[13]	97	AVSS_PLL
2	VSS	34	xcke	66	xma[12]	98	xtal27o
3	DVDD	35	xma[5]	67	gpio[4]	99	xtal27i
4	xdigtv[3]	36	xma[6]	68	gpio[3]	100	AVDD_PLL
5	xdigtv[2]	37	DVDD	69	gpio[2]	101	xfmgpio[9]
6	xdigtv[1]	38	VSS	70	gpio[1]	102	xfmgpio[8]
7	xdigtv[0]	39	OVDD	71	gpio[0]	103	xfmgpio[7]
8	AVDD_RTC	40	xma[7]	72	tggpio[5]	104	xfmgpio[6]
9	xrtcxtali	41	xma[8]	73	tggpio[4]	105	xfmgpio[5]
10	xrtcxtalo	42	xma[9]	74	tggpio[3]	106	xfmgpio[4]
11	AVSS	43	xudqm	75	tggpio[2]	107	xfmgpio[3]
12	SPOUTN	44	xmd[8]	76	tggpio[1]	108	DVDD
13	SPOUTP	45	xmd[9]	77	tggpio[0]	109	VSS
14	AVDD_SPK	46	xmd[10]	78	xrgb[9]	110	PMOS_VDD
15	LINEOUT	47	xmd[11]	79	xrgb[8]	111	CARD_POWER
16	VREFF	48	xmd[12]	80	SENVDD	112	gpio[8]
17	MICBIAS	49	xmd[13]	81	VSS	113	gpio[7]
18	MICINN	50	xmd[14]	82	DVDD	114	gpio[6]
19	MICINP	51	xmd[15]	83	xrgb[7]	115	gpio[5]
20	SAR0	52	DVDD	84	xrgb[6]	116	xfmgpio[2]
21	SAR2	53	VSS	85	xrgb[5]	117	xfmgpio[1]
22	xras_n	54	xsdramclk	86	xrgb[4]	118	gpio[10]
23	xcas_n	55	xldqm	87	xrgb[3]	119	xfmgpio[0]
24	xma[4]	56	xmd[7]	88	xrgb[2]	120	gpio[9]
25	xma[3]	57	xmd[6]	89	REXT	121	xdigtv[11]
26	xma[2]	58	OVDD	90	AVDD_USB	122	xdigtv[10]
27	xma[1]	59	xmd[5]	91	AVSS_USB	123	xdigtv[9]
28	xma[0]	60	xmd[4]	92	DM	124	xdigtv[8]
29	xma[10]	61	xmd[3]	93	DP	125	xdigtv[7]
30	xma[11]	62	xmd[2]	94	AVSS_VDAC	126	xdigtv[6]
31	OVSS	63	xmd[1]	95	COUT	127	xdigtv[5]
32	OVDD	64	xmd[0]	96	LVDI	128	xdigtv[4]

6.3. Package Size

LQFP 128L, 14x14x1.4mm (Lead Pitch: 0.4mm/Foot-Print: 2.0mm) Outline Drawing



Notes:

1. The top package size may be smaller than the bottom package size by as much as 0.15mm.
2. Dimensions D1 and E1 do not include mold protrusions, the allowable protrusion is 0.25mm per side.
3. Dimension b does not include the “Dambar” protrusion.
4. Exact shape of each package corner is optional.

DIMENSIONS (Unit: mm)

Symbol	A	A1	A2	b	c	D	D1	E	E1	e	L	L1	y
Max.	1.60	0.15	1.45	0.23	0.20	16BSC	14BSC	16BSC	14BSC	0.40BSC	0.75	1.00REF	0.08
Normal	-	-	1.40	-	-						0.60		
Min.	-	0.05	1.35	0.13	0.09						0.45		

6.4. Ordering Information

Product Number	Package Type	Memo
SPCA1627A-HL091	LQFP128 Pin, Green Package	

Note1: Code number is assigned for customer.

6.5. Storage Condition and Period for Package

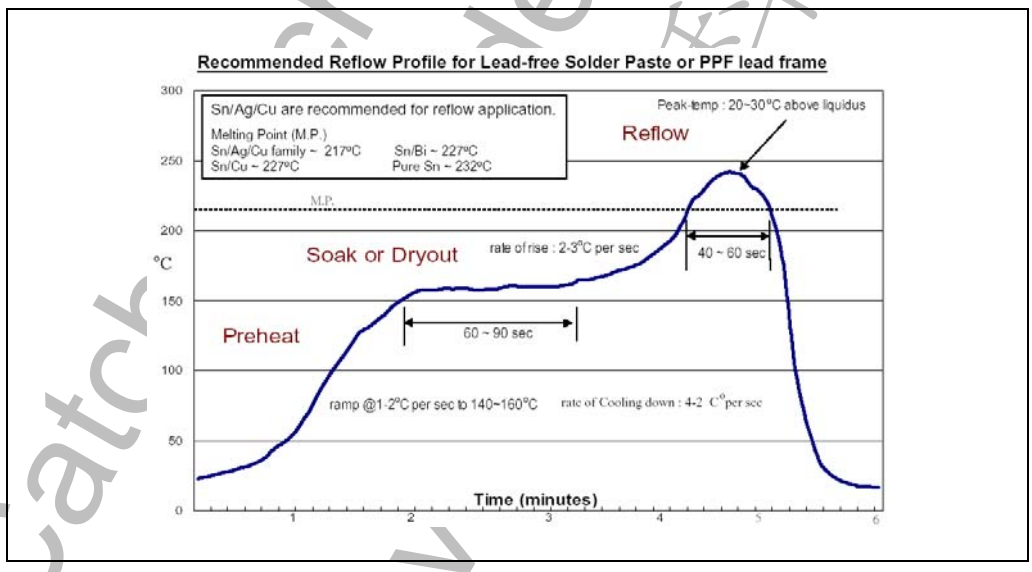
For Green Packages:

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
LQFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≤30℃/ 60% R.H.	Yes

Note: Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JESD22-A112, or the "CAUTION Note" on dry pack bag.

6.6. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT processing reference. Most of iCatch leadframe-based products choose Matte Tin and Sn/Bi for plating recipe. For PPF (Pre-Plated Frame) products with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.



6.7. References

IPC:
http://www.ipc.org

*NEMI (National Electronics Manufacturing Initiative)
http://www.nemi.org

*HDPUG (High Density Package Users Group)
http://www.hdpug.org

*JEDEC (Joint Electronic Device Engineering Council)
http://www.jedec.org

*JEITA (Japan Electronic Industry Association)
http://www.jeita.org

7. DISCLAIMER

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8. REVISION HISTORY

Date	Revision #	Description	Page
Nov. 18, 2010	0.2	1. Modify 2.2 Peripheral, 3-channel general-purpose ADC to 2-channel general-purpose ADC.	4
		2. Modify 4.1.3 Pin description, add VREFF and remove SAR1.	9
		3. Modify 6.1.1 Pin assignment, add VREFF and remove SAR1.	17
		4. Modify 6.2.1 Pin name, add VREFF and remove SAR1.	18
Dec. 25, 2009	0.1	Original	22