dividend_in

dividend_out

quotient_in

R_out

remainder

divisor

iter 1

quotient_out

iter 2

.....

dividend

remainder

divisor

quotient

iter 32

R_out -> remainder[31:0]

Quotient_out -> quotient[31:0]

iter block

lt (1bit)

lt

R_orig[31:0] — shl 1

divisor[31:0]

quotient
mux
setup

quo_le

quo_gt

1

0

quotient_out

lt

R_cmp

Dividend[31:0] — shr 31

or

R_cmp

lt (<)

R_cmp

1

0

R_out

R_sub

dividend_out

1

&

R_cmp

dividend

shl 1

divisor[31:0]

sub

R_sub

divisor

shl 1

dividend_out

quotient mux setup

quotient — shl 1

quo_le

quo_gt

0x1

or