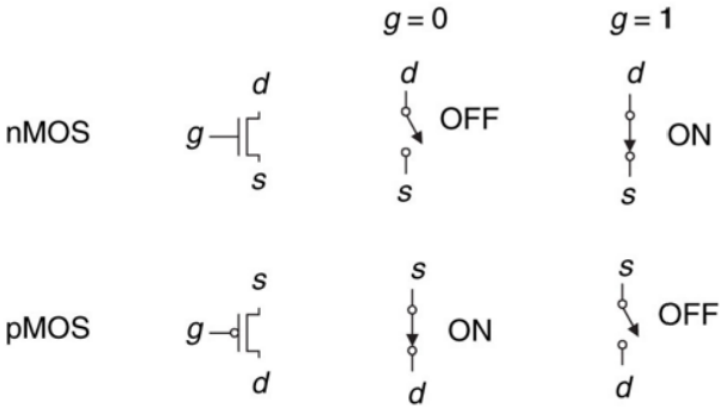
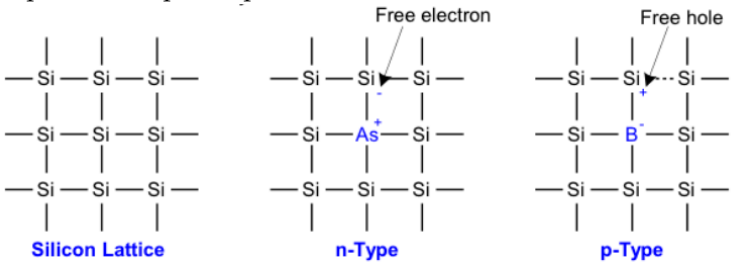
Logic Gates and Transistors

1 Transistors

A transistor is just an electronically controlled switch: 2 ports (d and s) are connected depending on the voltage of 3rd (g)



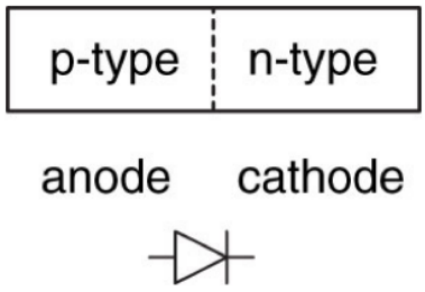
The most common transistor is the MOSFET (Metal Oxide Semiconductor Field Effect Transistor)
Silicon (a semiconductor) is a poor conductor of electricity: all the available electrons(4) are used to form bonds with neighbouring atoms
Impurities (dopants) provide extra electrons or electron holes which increase conductivity



In n type silicon it has a negative charge overall as there is a free electron in the lattice
In p type silicon an additional electron is ripped from the silicon atom, causing the lattice to have an overall positive charge. This lack of an electron can float around in the substrate, and acts like a positive charge.
The n type is a more efficient carrier.

1.1 Diodes

At a junction between p-type and n-type silicon, current can only flow from p type to n-type. This is a diode.



- Attach a negative charge near the p type, the holes will be attracted. This will cause a depleted region in the middle. A positive charge near the n type would pull the charge away from the middle. In this area in the middle current cannot flow.
- Note that with enough voltage charge will be carried whatever way intended

1.2 Capacitors

A **capacitor** is two pieces of conductive material separated by an insulator

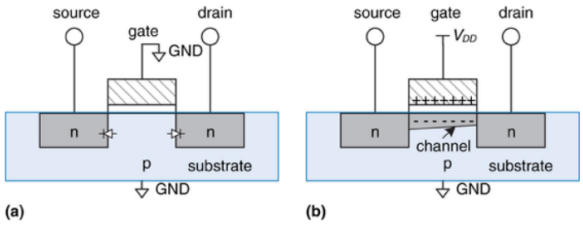
If a positive voltage is applied to one side, it accumulates charge Q and the other side accumulates the opposite charge -Q.

It takes time and energy to charge and discharge a capacitor

- The charges attract each other, and so is maintained when taken away
- Applying a sufficiently high voltage at one end the electrons will be pulled in the intended way

1.3 More detail about transistors

1.3.1 nMOS transistor

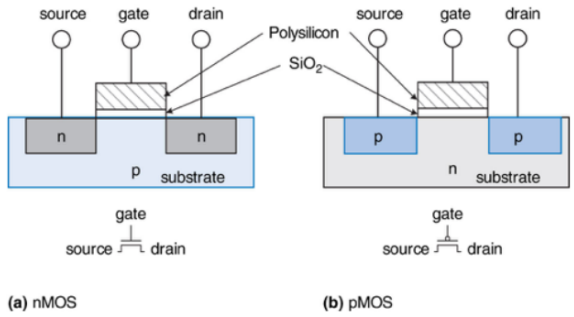


When the gate g is at V_{DD}, the capacitor effect draws negative charge (electrons) to the surface, and create a temporary channel of n type silicon, which allows current to flow from source to drain

- In its natural state there is no conduction
- By raising the gate voltage to a sufficiently high voltage a capacitance effect will be created between the gate and the p type substrate (rip electrons off atoms and pull through the substrate to create a layer of floating electrons between the source and drain.

1.3.2 pMOS transistor

A pMOS transistor is the opposite: on at g low and off at g high



- This is the same design as the nMOS transistor, but with the doped silicon the other way round
- The nMOS transistor is more efficient and so can be made slightly smaller

2 Binary Addition

This is achieved using gates implementing boolean algebra

Boolean algebra: An algebra of 2 values, 0 and 1

Basic Operations

- 0 and 0=0
- 0 and 1=0
- 1 and 0=0
- 1 and 1=1

2.1 Truth Tables

2.1.1 AND

AND gate:  Algebraic expression: $Y = A \cdot B$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Linear truth table

AND	B = 0	B = 1
A = 0	0	0
A = 1	0	1

Rectangular/Coordinate table

2.1.2 OR

OR gate:  Algebraic expression: $Y = A + B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Linear truth table

OR	B = 0	B = 1
A = 0	0	1
A = 1	1	1

Rectangular/Coordinate table

2.1.3 NOT

NOT gate:  Algebraic expression: $Y = \overline{A}$

A	Y
0	1
1	0

Linear truth table

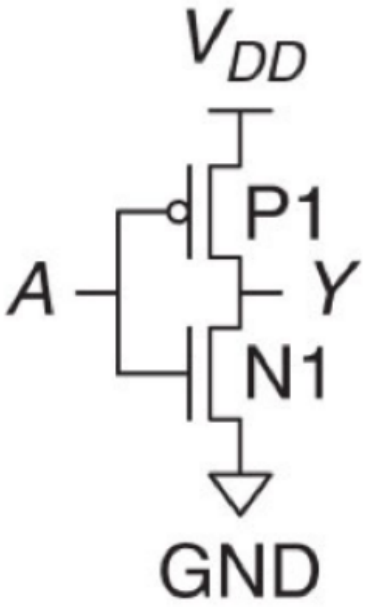
3 From transistors to gates

3.1 NOT

A **NOT** gate: 

If **A** is **high** then the p-MOS P1 is off and the n-MOS N1 is on, so **Y** is connected to GND, i.e. **low**.

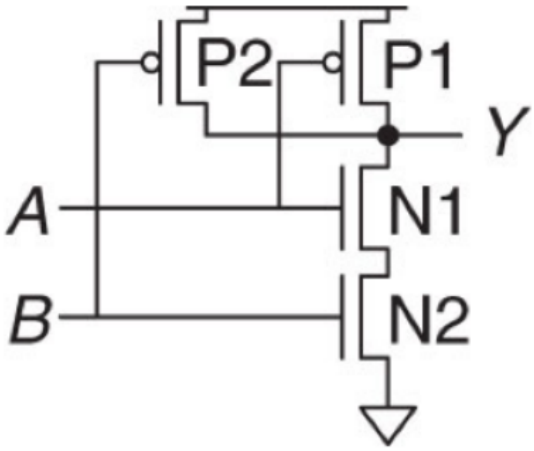
If **A** is **low** then the p-MOS P1 is on and the n-MOS N1 is off, so **Y** is connected to V_{DD}, i.e. **high**.



A	P1	N1	Y
0	on	off	1
1	off	on	0

3.2 NAND

A **NAND** gate: 



A	B	P1	P2	N1	N2	Y
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

4 Beneath the digital abstraction

The chip does not really deal with 0s and 1s. The voltages are real numbers typically between 0V and 5V.

We can take 0V to indicate output 0 and 5V to indicate output 1, but we need to tolerate **noise**. It is obvious if the value is close to one of the extremes, but what if it was 2.5V?

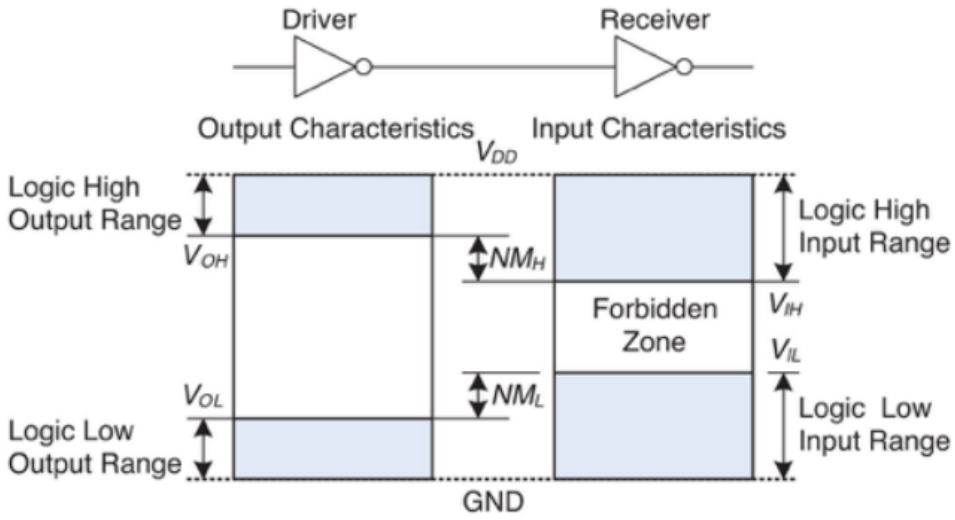
5 Supply Voltage

The low voltage in the system is 0V

Historically the high voltage (V_{DD}) was 5V, but more modern transistors use lower voltages to save power and avoid overloading transistors

The mapping of the continuous voltage measured at any point in the circuit to the discrete 0 and 1 of the digital abstraction is governed by defining **logic levels**

5.1 Logic Levels



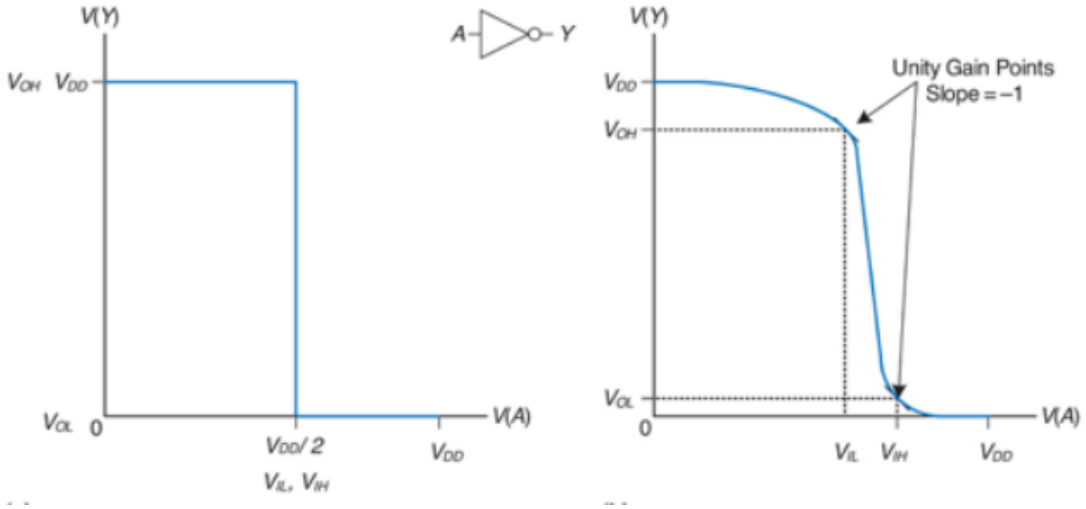
Permitted range for high output: V_{OH} to V_{DD}
Permitted range for low output: GND to V_{OL}
Acceptable range for high input: V_{IH} to V_{DD}
Acceptable range for low input: GND to V_{IL}

Noise margins:

$NM_H = V_{OH} - V_{IH}$
$NM_L = V_{IL} - V_{OL}$

- It is best for logic levels in a system to all be the same so that the components can best interoperate with each other.

5.2 Transfer characteristics



- An ideal inverter would output V_{DD} for outputs up to $V_{DD}/2$ and output 0 for inputs above $V_{DD}/2$
- Real circuits are not ideal
- A reasonable choice of logic levels is at the points where the slope is -1

5.3 The static Discipline

The design restriction that you will **only allow circuit elements that all satisfy the same logic levels**.

This means that (given noise limits) you can successfully apply the **digital abstraction** and **combine elements** without further concern about logic levels or analogue values.

It does reduce your freedom to include arbitrary elements, but makes design much simpler.

Logic Family	V_{DD}	V_{IL}	V_{IH}	V_{OL}	V_{OH}
TTL	5 (4.75 - 5.25)	0.8	2.0	0.4	2.4
CMOS	5 (4.5 - 6)	1.35	3.15	0.33	3.84
LVTTL	3.3 (3 - 3.6)	0.8	2.0	0.4	2.4
LVCMOS	3.3 (3 - 3.6)	0.9	1.8	0.36	2.7

6 Moore's Law

Transistor density doubles in 2 years or computer processing power doubles every 18 months