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| Three Phases of IC Design<br>CT | Three key components in CPU Microarchitecture<br>CT |
| Fetch decode fetch execute cycle<br>CT | Two main components of an IC<br>CT |
| von Neumann bottleneck<br>CT | Registers<br>CT |
| 4 Programming Paradigms<br>CT | 4 Drivers of Programming Languages<br>CT |
| Syntax<br>CT | Semantics<br>CT |
| ISA<br>CT | Process Control Block<br>CT |
| Types of MIPS Instructions<br>CT | Data Security (in the context of OS)<br>CT |
| Virtualisation (in the context of OS)<br>CT | Mutual exclusion<br>CT |
| Critical Selection<br>CT | Life cycle of processes within the operating system<br>CT |
| State transitions in a CPU<br>CT | Context switching<br>CT |

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| Datapath<br>Control<br>Cache | Functional Specification<br>Register Transfer Level<br>Map to physical layout |
| Transistors interconnected by microscopic wires | Instruction Fetch<br>Instruction Decode<br>Operand Fetch<br>Execute Instruction |
| On chip memory locations providing fast access to data | A limitation of the rate of data transfer between the CPU and memory |
| Productivity<br>Reliability<br>Security<br>Execution | Imperative<br>Declarative<br>Data-Oriented<br>Scripting |
| The rules which govern what a program 'means' | Rules that govern what make a program 'legitimately written' |
| A data structure that the kernel uses in order to manage a process | Interface between hardware and software |
| Ensuring that the memory allocated to each program is kept separate and secure from other programs | I Type - Involve data transfer<br>R Type - Work on registers<br>J Type - Involve jumps |
| Ensuring that two threads are not in the critical selection at the same time | Providing abstractions that present clean interfaces to make the computer easier to use |
| new<br>ready<br>running<br>blocked<br>exit | Exclusive access to some shared resource such as memory location |
| Where the operating system pauses one process and resumes another | admit<br>dispatch<br>timeout/yield<br>event-wait<br>event<br>release |

| Notions relating to problem solving CT | Planar graph CT |
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| A graph that can be drawn in a plane without any graph edges crossing | Computation<br>Resource<br>Correctness |
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