CMPE-160 Digital System Design 1

Laboratory Exercise 7

Sequential Circuit Elements

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

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Lecture Section:	1
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Abstract

To better understand sequential circuits, an active-low D latch and a rising-edge master-slave D flip-flop were designed. Each design was verified through simulation and constructed in hardware. An oscilloscope was used to study the D flip-flop. All results were as expected and the exercise was a success.

Design Methodology

A master-slave D flip-flop is built using two D latches. A D-latch is able to store data and load new data. The functionality of a D-latch can be described with three terms. The D-latch can `HOLD`, `SET`, or `RESET`. `SET` and `RESET` loads a value of 1 or 0 into the latch, while `HOLD` holds the previous value.

Table 1 shows the behavior of a D-latch.

Table 1: *D Latch Function Table*

En	D	Q	Qn
0	0	0	1
0	1	1	0
1	X	Q_0	$\overline{Q_0}$

Table 1 shows how En and D output different values. When En, or enable, is low, Q is equivalent to D. When En is high, regardless of the value of D, $Q*$ is equivalent to the previous value of Q, or the value of D before En was switched high.
A D-latch with active-low enable was designed.

Figure 1 shows the circuit schematic of a D-latch.

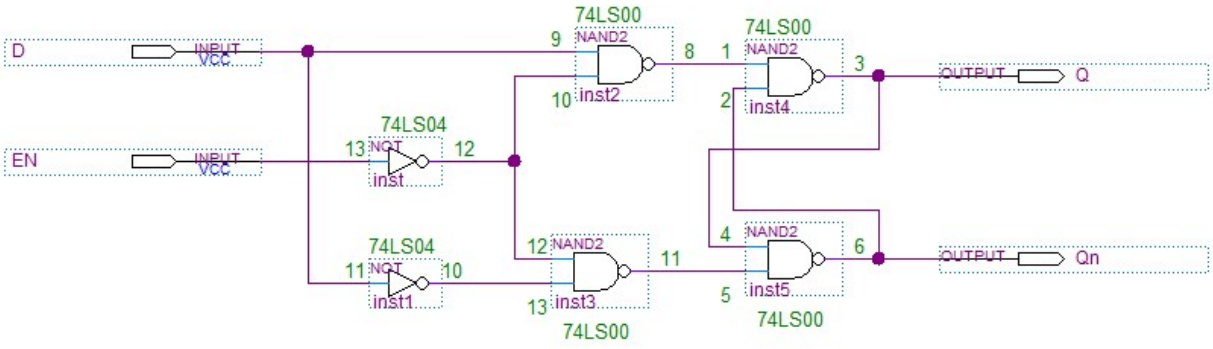

Figure 1: *D-latch Circuit Diagram*

Figure 1 shows why this D-latch is an active-low enable D-latch. Only when EN is low, would the value of D transfer to the output. If EN was high, the NAND gates would output logic 0 regardless of what the D value is. The part numbers of the ICs are included above each gate and the pin number of the ICs are included. The unique behavior of a D-latch to hold and load values is created through how the outputs also become the inputs of the opposite output's NAND gate.

A D flip-flop uses two D latches. The output Q of the first latch feeds into the input D of the second latch. A D flip-flop behaves similarly to a D-latch and is able to load new values and hold previous values. The main difference is the clock. Instead of EN, a D flip-flop is triggered by certain edges of the clock.

Table 2 shows how a clock (CLK) is used with D to create load and hold behaviour.

Table 2: *Rising Edge-Triggered D flip-flop*

CLK	D	Q	Qn
↑	0	0	1
↑	1	1	0
otherwise	X	Q_0	$\overline{Q_0}$

Table 2 shows a D flip-flop that is rising edge triggered. This means that the value of D can only change at the rising edge of the clock wave. Table 2 is very similar to Table 1. Both tables show how values can be loaded or held. The main difference is with the En and CLK. The D value could change asynchronously, whenever En was low, whereas with CLK in this circuit the D value can only change synchronously, whenever a rising edge occurs.

After examining it behavior, a D flip-flop was designed.

Figure 2 shows a rising edge triggered D flip-flop.

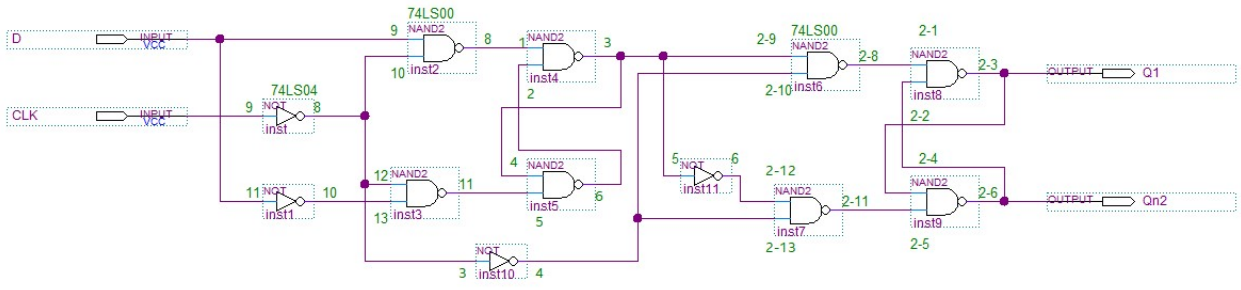

Figure 2: *D Flip-Flop Circuit Diagram*

Figure 2 shows how two D-latches are used to create a D flip-flop. Instead of an En, it is replaced with a clock (CLK). The part numbers of the ICs is labeled on the circuit. The number of part number labels correspond to the necessary amount of ICs needed to create the circuit. Pin numbers are on each pin. Numbers preceded with "2 - " represent the pins of a second IC of the same type. The output of the first D-latch is the input of the second D-latch. CLK is also inverted between the first and second D-latch.

Results and Analysis

To verify the circuits designed in Figure 1 and Figure 2, the designs were simulated in ModelSim.

Figure 3 contains the waveform generated from the D Latch.

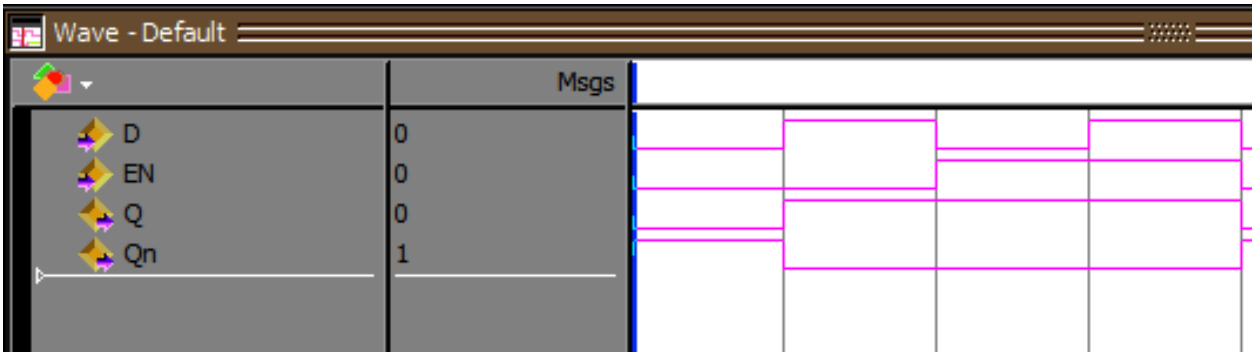

Figure 3: *D Latch Simulation*

Figure 3 showed the expected results, so the design was accurate. The simulated results match with the results expected in Table 1. Whenever EN is low, the Q value is the same as D. When EN switches to high, the Q just retains the value of Q before EN switched. Qn shows the inverse of Q.

Figure 4 contains the waveform generated from the D flip-flop.

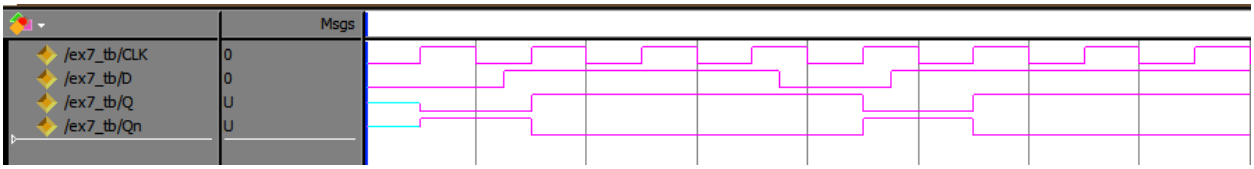

Figure 4: *D Flip-Flop Simulation*

Figure 4 shows the expected results, so the design was accurate. The simulated results match with the results expected in Table 2. At the beginning of Q and Qn, the line is a different color compared to the rest of the waves. This is due to the fact that a rising clock edge has not occurred yet. Before the first rising clock edge, Q and Qn is undefined. Q only changes on the rising-edge of CLK.

After verification, the D flip-flop was constructed in hardware. An oscilloscope was used to create the clock input and to measure CLK and Q.

Figure 5 shows a screen capture of the oscilloscope readings.

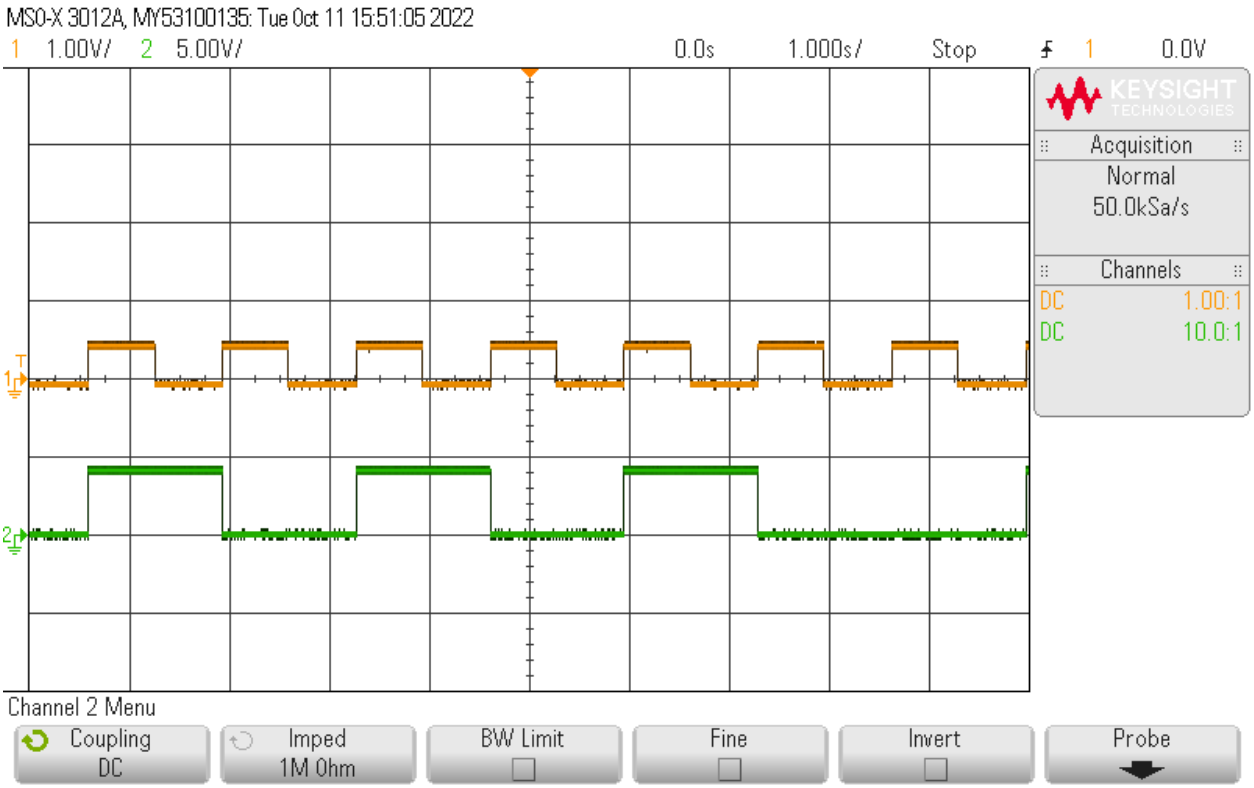

Figure 5: *D Flip-Flop Oscilloscope Capture*

Figure 5 shows two waveforms. The waveform at the top in orange represents the clock (CLK). Similar to a metronome, the CLK maintains a steady and consistent switch. The CLK in this circuit has a 1Hz frequency, 50% duty cycle, 5V peak-to-peak amplitude, and a 2.5 V offset.The waveform of Q only changes on the rising-edge of the clock as expected. This showed that the circuit constructed in hardware worked successfully.

Conclusion

A D-latch and D flip-flop were designed by applying knowledge of their functions. The circuit schematics of each was verified in ModelSim. The generated simulated waveforms were as expected, and confirmed the accuracy of the designs. The D-latch and D flip-flop were constructed in hardware. Using an oscilloscope, the D flip-flop's input Q and CLK were tested and was as expected. Results from simulations and hardware measurements were as expected, so the exercise was a success.

Several new lessons were learned during this exercise. The oscilloscope can output a square function that can be used as a clock. The inverter on the CLK between the two D-latches dictates the clock edge trigger to be rising-edge. An added inverter would change the D latch to be falling edge.

Due to propagation delay, a shift register may be used to delay signals to synchronize with other delayed signals. This way all the data reaches the next input at the same time and no errors occur. A shift register is composed of multiple D flip-flops. Shift registers are important in a lot of circuits to help them work without error. Understanding how D-latches and D flip-flops work will help with more applications in the future (such as shift registers).

Questions

1. Design a falling edge triggered D flip-flop using D latches with active-low enable.

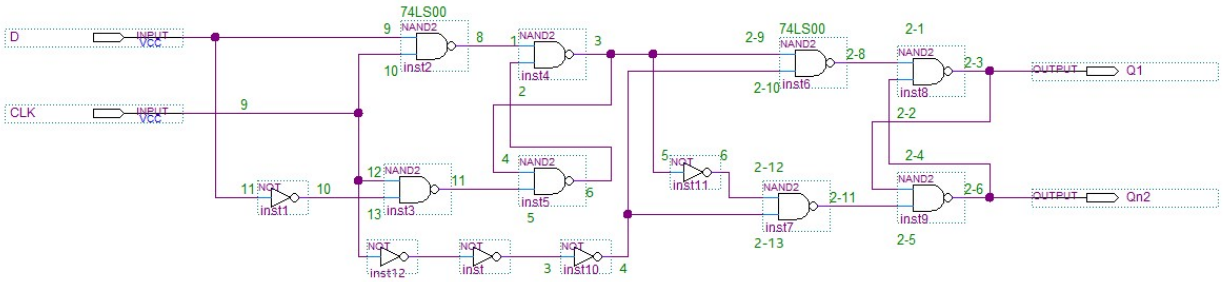

Figure 6: *Falling Edge Triggered D Flip-Flop*

2. The 74LS175 IC has four D flip-flops. What are the timing values for a 74LS175 D flip-flop?

   The maximum time for the asynchronous MR (master reset) is 30 ns. The maximum time for the output to change after the triggering clock edge is 25 ns. The minimum data setup time is 20 ns. The minimum data hold time is 5 ns.

Extra Credit

1. Oscilloscope Capture

Although the change in data seems instantaneous, there is a delay that occurs. Figure 7 shows the delay of the D flip-flop constructed in hardware.

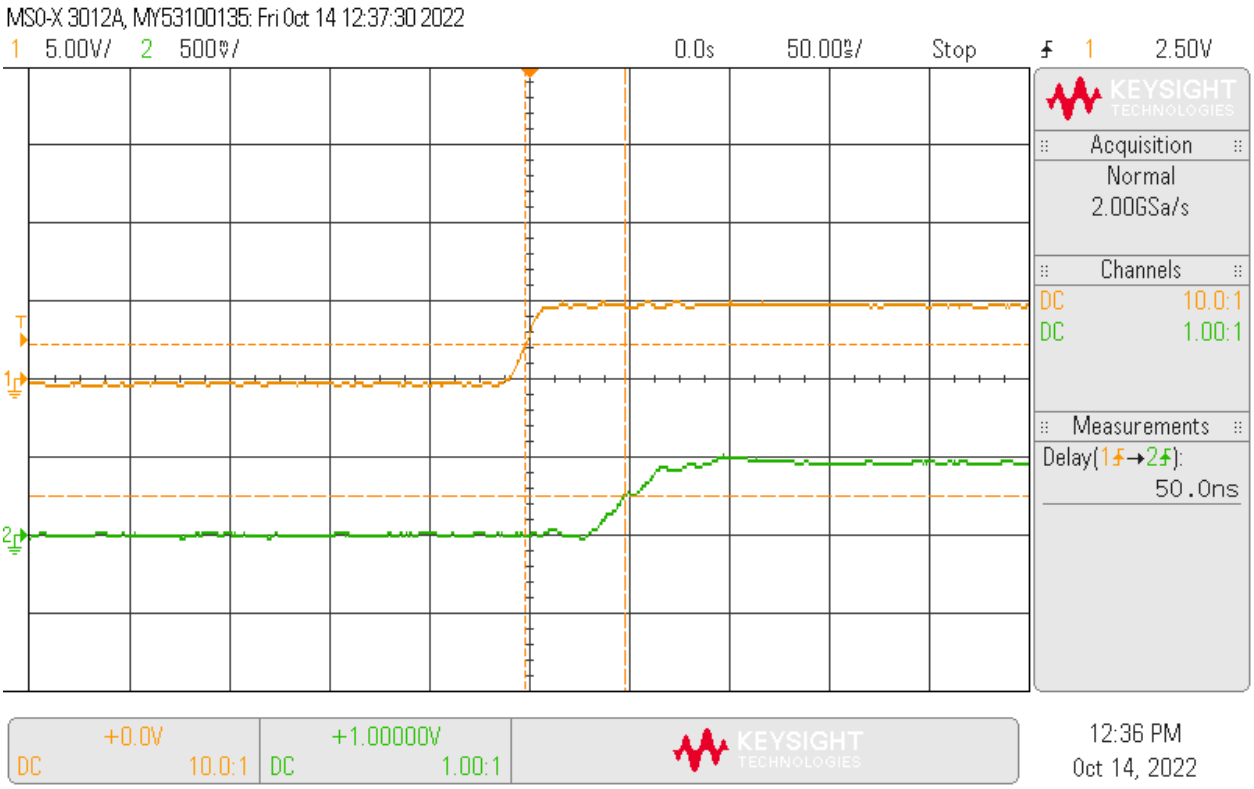

Figure 7: *D Flip-Flop Delay Oscilloscope Capture*

Figure 7 shows the waveform of the hardware. With an x-axis scale of 50 ns/div, the delay between the clock edge and the output can be seen.

2. What was the maximum clock to Q delay measured? Compare this to the answer for Question 2b. What frequency can the flip-flop operate at, assuming no other delays are present?
   Using Measurements, the delay was determined to be 50 ns. Frequency is equal to $1/T$ where T is the period. The period is equivalent to the delay in this case. This means that the delay determines the maximum frequency of a flip-flip. Assuming no other delays are present, the maximum frequency the flip-flop can operate at is 20 MHz.

Exercise 7: Sequential Circuit Elements

Student's Name:_____ Section:_____

Prelab		Point Value	Points Earned	Comments
Part 1	Schematic	4	4	KP 10/14
	Simulations	4	4	CV 10/14
	Parts placement diagram	4	4	Ignored
Part 2	Schematic	4	4	
	Simulations	4	4	KP 10/14

Demo		Point Value	Points Earned	Date
Demo	Latches	20	20	CV 10/7
	Flip-flop	20	20	MCK 10/14

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 7: Sequential Circuit Elements

Report		Point Value	Points Earned	Comments
Abstract		4		
Design Methodology	D latch function table	3		
	D latch circuit diagram	3		
	D flip-flop function table	3		
	D flip-flop circuit diagram	3		
Results and Analysis	D latch simulation	3		
	D flip-flop simulation	3		
	D flip-flop oscilloscope capture	2		
Conclusion		4		
Questions	Q1	4		
	Q2	4		
Extra Credit	Oscilloscope capture	5		
	Question	5		
Writing Composition		4		
Total for prelab, demo, and report		100		