CMPE-160 Digital System Design 1

Laboratory Exercise 3

Electrical and Logical Characteristics of Gates

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

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Lucy Zhang Performed 6 September 2022 Submitted 13 September 2022

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Abstract

The purpose of this exercise was to examine the electrical and delay characteristics of logic gates. Datasheets for IC's were examined for data on electrical characteristics such as the low level input and output voltage, and the high level input and output voltage. The input and output voltage of a two-input NAND gate circuit (74LS00), OR gate circuit (74LS32), and XOR gate circuit (74LS86) were measured. An oscilloscope was used to measure the effect of propagation delay in a TTL inverter. Based on knowledge of truth tables, the LED's lit up as expected. Measured values matched with expected values, so the exercise was a success.

Design Methodology

To demonstrate the electrical characteristics of logic gates, two switches and a LED were used. The switches controlled the voltage level going into the logic gate. Due to the same placement of parts and pins in the IC's used, the same circuit schematic was used for each IC. An Agilent E3631A power supply with a voltage limit of 5 volts and amperage limit of 0.1 amps was used to power the circuit.

Figure 1 shows the circuit that was created.

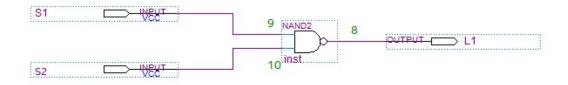


Figure 1: Voltage Measurement Circuit Schematic

In Figure 1, two switches were wired to pin 10 and 9 of a two-input NAND gate (74LS00), OR gate (74LS32), and XOR gate (74LS86) respectively. A red LED was wired to pin 8 of the respective gates. An Agilent 34401A multimeter was used to measure voltage input at pins 10 and 9 and voltage output at pin 8.

To examine the delay characteristics of logic gates, a ring oscillator composed of five inverters was used. The five inverters were arranged in a series with the last in the series connecting to the first.

Figure 2 shows the circuit that was created to form a ring oscillator.

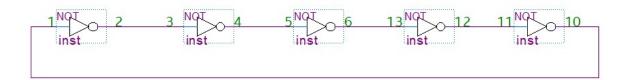


Figure 2: Ring Oscillator Circuit Schematic

Figure 2 shows the circuit schematic for the ring oscillator. Both probes CH1 and CH2 of (THE OSCILLOSCOPE) were grounded. To measure the propagation delay, the CH1 probe was attached to pin 2 of the 74LS04 IC as a reference point and the CH2 probe was placed after each inverter (pin 4, pin 6, pin 12, and pin 10) in the circuit shown in Figure 2. Using the oscilloscope, the time delay between the pins can be determined by measuring the time difference between the initial signal and the resulting inverted signal.

Results and Analysis

The first logic gate that was examined was the quad two-input NAND IC (74LS00N). Using the multimeter, the two inputs and one output voltages were recorded.

Table 1 shows the results of the voltage measurements from the NAND gate.

Switch 1 Position	Switch 2 Position	$V_{in,1}(V)$	$V_{in,2}(V)$	Vout (V)	LED (on/off)
Closed	Closed	0	0	4.16	on
Closed	Open	0	4.99	4.16	on
Open	Closed	4.99	0	4.16	on
Open	Open	0	off		
	N	IAND			
	74	4LS00			

Table 1: Measurements of a Two Input NAND Gate Circuit

In Table 1, when the corresponding input voltage is about 5 volts, the switch is open. When the switch is closed, the corresponding input voltage is 0. Every time the LED is on, the output voltage is 4.16 volts. According to the data sheet, the minimum high level input voltage is 2 volts, and the maximum low level input voltage is 0.7 volts. The voltage measurements in Table 1 follow the characteristics of the IC in its data sheet. Low level input stayed below the 0.7 volts and the high level input stayed above 2 volts. Following the logic of a NAND operator, there are three combinations of switch positions where the result returns true. When the truth table results return true, or logic 1, the LED is on.

The second logic gate that was examined was the quad two-input OR IC (74LS32). Using the multimeter, the two inputs and one output voltages were recorded.

Table 2 shows the results of the voltage measurements from the OR gate.

Switch 1 Position	Switch 2 Position	$V_{in,1}(V)$	$V_{in,2}(V)$	V _{out} (V)	LED (on/off)
Closed	Closed	0	0	0	off
Closed	Open	0	4.99	4.05	on
Open	Closed	4.99	0	4.05	on
Open	Open	4.99	4.05	on	
		OR			
	74	4LS32			

Table 2: Measurements of a Two Input OR Gate Circuit

In Table 2, when the switch is on, the corresponding input voltage is about 5 volts. When the switch is closed, the corresponding input voltage is 0. Every time the LED is on, the output voltage is 4.05 volts. Following the logic of an OR operator, there are three combinations of switch positions where the result returns true. When the truth table results return true, or logic 1, the LED is on. There are three combinations of switch position where the LED turns on.

The last logic gate that was examined was the quad two-input XOR IC (74LS32). Using the multimeter, the two inputs and one output voltages were recorded.

Table 3 shows the results of the voltage measurements from the OR gate.

Switch 1 Position	Switch 2 Position	$V_{in,1}(V)$	$V_{in,2}(V)$	Vout (V)	LED (on/off)
Closed	Closed	0	0	0.14	off
Closed	Open	0	4.99	4.09	on
Open	Closed	4.99	0	4.09	on
Open	Open	4.99	4.99	0.15	off
		XOR			
	74	4LS86			

Table 3: Measurements of a Two Input XOR Gate Circuit

In Table 3, when the switch is on, the corresponding input voltage is about 5 volts. When the switch is closed, the corresponding input voltage is 0. Every time the LED is on, the output voltage is 4.05 volts. Following the logic of an OR operator, there are two combinations of switch positions where the result returns true. When the truth table results return true, or logic 1, the LED is on. There are two combinations of switch position where the LED turns on.

In the ring oscillator created according to Figure 2, the time between one edge of the CH1 signal and the next inverted edge of CH2 on the oscilloscope was measured. The total period was also recorded.

Figure 3 shows the capture of the oscilloscope for finding the total period.

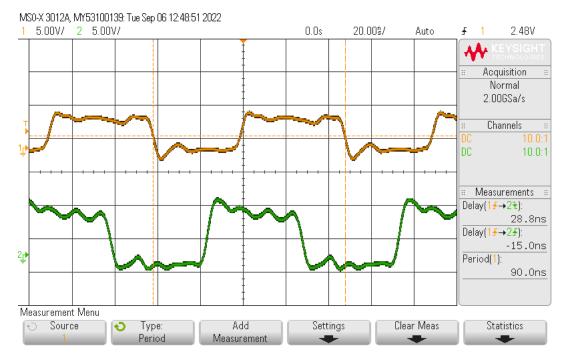


Figure 3: Oscilloscope Screen Capture

In Figure 3, the oscilloscope shows the measurement of the wave form's period, or time it takes to make one full cycle. The delay function was used to measure the time relative to pin 2 between gates. Due to the gates being inverters, the signals inverted after each gate. This is why each measurement for delay must alternate between rising to falling and rising to rising.

Using the data sheet of IC 74LS04, the number of gates between pin was recorded.

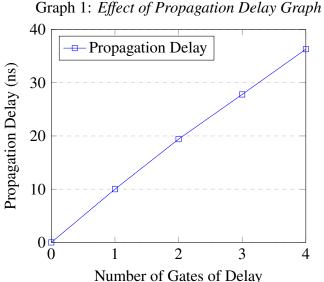
The data of propagation delay found in Figure 3 was recorded in Table 3.

74S04 (pin to pin)	Number of Gates of Delay	Propagation Delay (ns)
2 to 4 (rising to falling)	1	10
2 to 6 (rising to rising)	2	19.4
2 to 12 (rising to falling)	3	27.8
2 to 10 (rising to rising)	4	36.3
	Period:	93.5

Table 4: Effect of Propagation Delay

Table 4 shows the propagation delay time as the number of gates is increased. Each gate has shows the measurement between pin 2 and pin 4. This measurement is the propagation delay between pins 2 and 4. According to the data sheet of IC 74LS04, between pins 2 and 4, there is one NOT gate. This means that the propagation delay of one NOT gate in the circuit described by Figure 2 is about 10 nanoseconds.

To better visualize the correlation between the number of gates and the propagation delay, the data from Table 4 was used to create Graph 1.



Graph 1 shows the effect of propagation delay. There is a linear trend where the number of gates has a direct linear correlation with the delay time.

Conclusion

This lab exercise tested and examined the electrical and delay characteristics of a variety of two-input gate circuits. The electrical characteristics of a gate circuit works exactly as described by a truth table. When the switch in the circuit is off, it can be represented as a logic 0. A closed switch causes a low logic level where the voltage is low. The opposite is true with when the switch is open. An open switch can be represented as a logic 1 and causes a high logic level where voltage is about the amount of VCC. As seen with Table, Table 2, and Table 3, this held true with the input voltage. When the switch was closed, the input voltage was near 0, whereas when the switch was open, the input voltage was about 5 volts, the VCC value. Based on the chip's logic, the voltage output had a distinct difference. As seen in Table 1, Table 2, and Table 3, whenever the result was logic 1, the output voltage was above 4 volts. This gave enough voltage to the LED to subsequently turn it on. Whenever the result was logic 0, the voltage was significantly lower. This can be seen in Table 1 where the largest output voltage was 4.16 volts and the smallest output voltage was 0. The LED did not turn on when there was not enough voltage going through it. The LED performed as expected, so the exercise was a success.

Based on the data gathered, there is a correlation between the number of gates and the propagation delay. Propagation delay is the time it between the input signal going into the circuit and a signal being outputted. As the number of gates increase, the amount of delay time also increases. Engineers need to be aware of the number of gates between input and output signals since the propagation delay time increases proportionally. If propagation delay is not correctly measured and accounted for in circuit schematics, the resulting output signal can be wrong and effect the efficiency of the circuit.

Questions

- 1. What are these voltage values for the 74LS27
 - (a) Minimum input voltage for logic 1 2 V
 - (b) Maximum input voltage for logic 0 0 8 V
 - (c) Minimum output voltage for logic 1 2.7 V

2. Define propagation delay, and discuss how it impacts the output a gate. Why is it a consideration in digital designs?

A gate does not instantaneously produce an output signal. A gate experiences a time delay from input signal(s) to output signal. Propagation delay is the time it takes for a gate to produce an output signal from the input signal(s). As seen with Graph 1, as the amount of gates the between the measured pins increased, the time delay increased accordingly. Propagation delay is important to consider in digital designs because the output signal could be inaccurate up until the maximum propagation delay time has elapsed.

3. Design an XOR gate using 74LS08 (2-input AND), a 74LS04 (6-inverter) and a 74LS32(2-input OR).

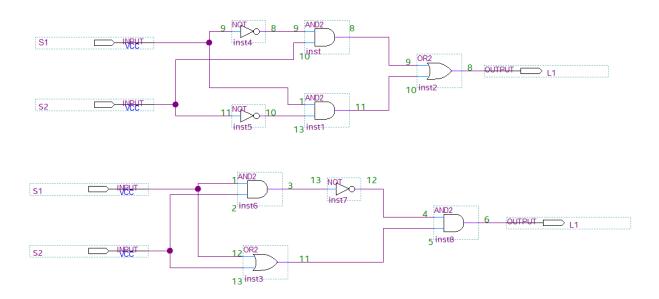


Figure 4: XOR Gate Circuit Schematics

Exercise 3: Electrical and Logical Characteristics of Gates

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I	Prelab	Point Value	Points Earned	Comments
Prelab	Part 1	10	10	201 0/0
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	Demo	Point Value	Points Earned	Date
Demo	Voltage measurements	20 %	a a/b	
	Ring oscillator	20	20	10

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 3: Electrical and Logical Characteristics of Gates

Report		Point Value	Points Earned	Comments
Abstract		3		
Design Methodology	Voltage measurement circuit schematic	4		
	Ring oscillator circuit schematic	4		
	Voltage tables	4		
Results and Analysis	oscilloscope capture(s)	2		
	Delay table	3		
	Delay graph	4		
Conclusion		3		
	Q1	3		
Questions	Q2	3		
	Q3	4		
Writing Composition		3		
Total for prelab, demo, and report		100		