CMPE-160 Digital System Design 1

Laboratory Exercise 5

Combinational Logic Circuit Design Using Karnaugh Map Simplification

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

Lucy Zhang

Lucy Zhang
Performed 20 September 2022
Submitted 27 September 2022

Lab Section:	1
Instructor:	Purab Sutradhar
TA:	Morgan Kreifels
	Karisha Pradham
	Colin Vo
Lecture Section:	1
Lecture Instructor:	Richard Cliver

Abstract

A Boolean expression was put into a K-map to determine the minimum sum of products (SOP) and product of sums (POS) expressions. Using combinational logic design principles, a circuit was designed from the reduced expressions (SOP and POS) and simulated in ModelSim. The circuit with the lowest equivalent gate count (EGC) was constructed in hardware and tested. The waveform generated from the simulation and the constructed circuit performed as expected, so the lab experiment was a success.

Design Methodology

The circuit was designed based on the Boolean expression in (1).

$$F = \sum m(0, 2, 3, 4, 6, 7, 13, 14, 15) \tag{1}$$

Using a Karnaugh map, (1) was simplified into the minimum SOP and POS expression for F.

Table 1 shows the K-map used for the SOP expression for F.

Table 1: *K-map for SOP Expression for F*

AB \ CD	00	01	11	10
00	1	0	1	1
01	1	0	1	1
11	0	1	1	1
10	0	0	0	0

Table 1 shows how (1) was simplified into the minimum sum of products (SOP) expression. The location of the 1's and 0's were determined by (1). The blue, red, yellow, and green boxes were used to simplify (1) to $A'D'$, $A'C$, BC, and ABD respectively.

By taking the sum of these products, (2) was determined.

$$F_{SOP} = A'D' + A'C + BC + ABD \tag{2}$$

Equation (2) shows the reduced SOP expression for F. This expression finds the sum of the products determined from the K-map in Table 1. This expression has an EGC of 8 (not including inverters).

Table 2 shows the same K-map as Table 1, but used differently to find the product of sums (POS) of F.

Table 2: *K-map for POS Expression for F*

AB \ CD	00	01	11	10
00	1	0	1	1
01	1	0	1	1
11	0	1	1	1
10	0	0	0	0

Table 2 demonstrates how the POS was determined. For POS, the 0's are enclosed instead of the 1's. The red, green, and yellow boxes simplify to $A + B + D'$, $A' + C + D$, and $A' + B$ respectively.

By taking the product of these sums, (3) was determined.

$$F_{POS} = (A + C + D')(A' + C + D)(A' + B) \tag{3}$$

Equation (3) shows the reduced POS expression for F. This expression finds the products of the sums determined from the K-map in Table 2. This expression has an EGC of 7 (not including inverters). A circuit diagram was created based on (2) and (3).

Figure 1 shows the digital schematic for the circuit.

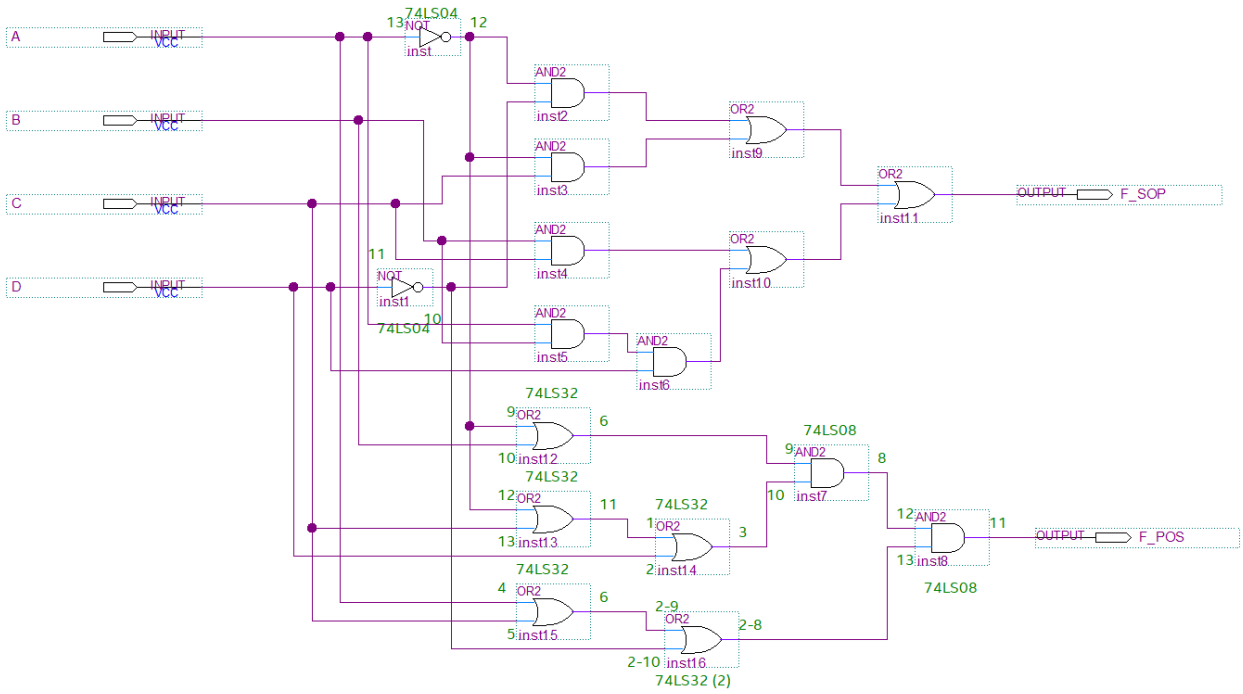

Figure 1: *Circuit Diagram of F Using SOP and POS Expressions*

Figure 1 shows the four inputs A, B, C, and D and the two outputs F_SOP and F_POS. The F_SOP represents the SOP expression in (2) and the F_POS represents the POS expression in (3). The Boolean expression in (1) is represented in two different ways through this circuit. Examining the schematic, F_POS had the lowest cost, so the circuit for F_POS was constructed in hardware. Figure 1 labels the pin numbers for the IC's used as well as the IC's used (74LS04, 74LS32, and 74LS08). One gate has pin numbers that are labeled with "2-" and the IC is labeled with "74SL32 (2)". This represents the second OR IC. The circuit needs five OR gates and one IC has only 4 gates.

Results and Analysis

Taking the implemented circuit schematic, the circuit was simulated in ModelSim.

Figure 2 shows the generated waveform from the simulation.

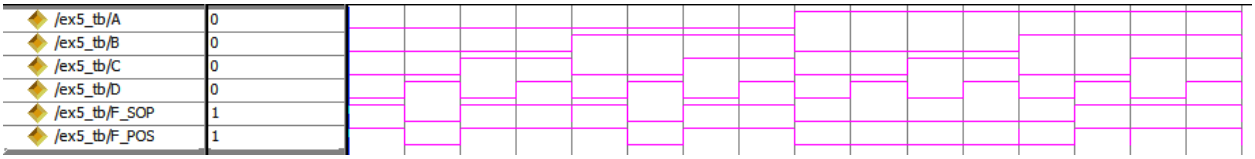

Figure 2: *Simulated Waveform of Circuit*

Figure 2 represents the digital logic of the inputs and outputs of the circuit. The circuit worked successfully with the expected waveform and outputs. Both F_SOP and F_POS generate mostly the same waveform. This is expected as both expressions are equal and are derived from the same original Boolean expression in (1). The only difference in the waveform is in two locations. In the F_POS waveform there are two visible glitches where the output is different from what the output should be. The glitch shows a "1" when the there should have been a "0" and vice versa later in the waveform. This is a "hazard" caused by propagation delay from the gates.

Conclusion

Using K-maps, the minimum POS and SOP expression was created from a Boolean expression. A circuit was designed based on the reduced expressions. The circuit was verified through the simulation generated waveform. The diagram of the circuit with the lower cost was constructed in hardware and tested. The exercise was successful. The waveform was able to show how the POS had hazards, while the SOP does not. However, the POS had a lower EGC and was more efficient than the SOP. Although both expressions produce the same output, there are differences in the method. The POS is lower cost, but is not always accurate. The SOP is less efficient but doesn't have hazards. Depending on the application, either the POS or the SOP could be used. It's important for engineers to understand the differences between each method so they can chose the best method for their application.

Questions

1. Design a 2-level NAND-NAND implementation for the SOP expression.

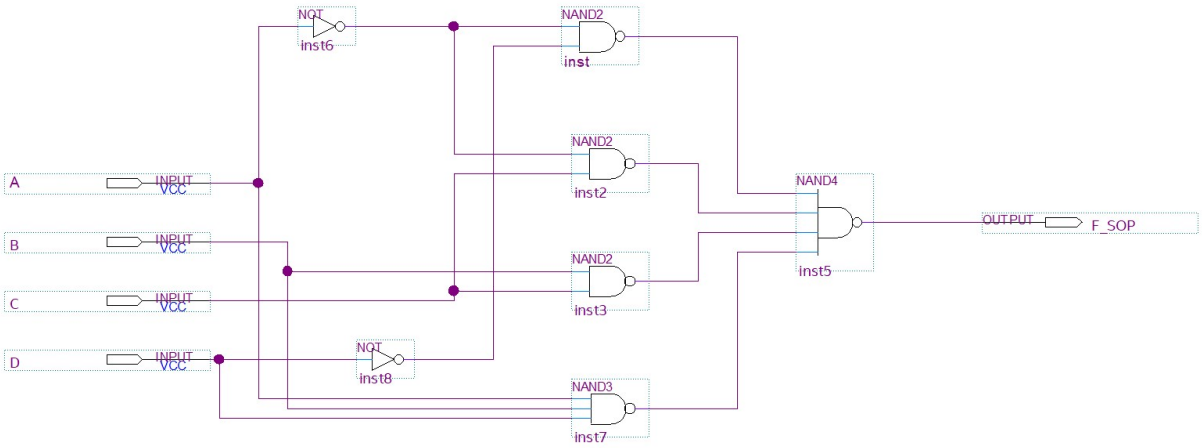

Figure 3: *NAND Implementation of SOP Expression*

2. Design a 2-level NOR-NOR implementation for the POS expression.

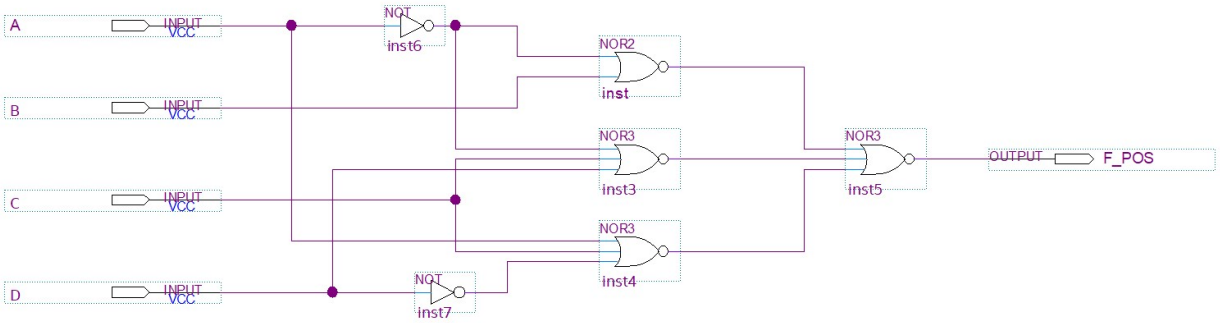

Figure 4: *NOR Implementation of POS Expression*

Exercise 5: Combinational Logic Circuit Design Using Karnaugh Map Simplification

Student's Name: Lucy Zhang Section: 01

Prelab		Point Value	Points Earned	Comments
Part 1	K-maps	4	4	CV 9/20
	Correct Boolean expressions	4	4	
Part 2	Schematic diagram	4	4	
	Simulations	4	4	
	EGC	4	4	CV 9/20

Demo		Point Value	Points Earned	Date
Demo	Test Bench	20	20	mid Feb
	Circuit Construction	20	20	Mon 9/20

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 5: Combinational Logic Circuit Design Using Karnaugh Map Simplification

Report		Point Value	Points Earned	Comments
Abstract		4		
Design Methodology	Karnaugh maps	5		
	Reduced SOP expression	5		
	Reduced POS expression	5		
	Schematic diagram	4		
Results and Analysis	SOP waveforms	2		
	POS waveforms	2		
Conclusion		5		
Question		5		
Writing Composition		3		
Total for prelab. demo, and report		100		