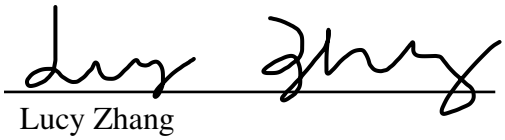
CMPE-160 Digital System Design 1

Laboratory Exercise 11

Modeling of Combinational Circuits Using Concurrent and Sequential Statements

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.



Lucy Zhang
Performed 8 November 2022
Submitted 15 November 2022

Lab Section: 1
Instructor: Purab Sutradhar
TA: Morgan Kreifels
Karisha Pradham
Colin Vo

Lecture Section: 1
Lecture Instructor: Richard Cliver

Abstract

Given the inputs and outputs of a 74LS153 circuit and the data sheet of a 74LS153 IC, VHDL is written to create the circuit. The VHDL was written using structural, data flow, and behavioral models and simulated in ModelSim to verify their correctness. The simulation showed expected waveforms, so the exercise was a success.

Design Methodology

A 74LS153 circuit describes a dual 4-line to 1-line data multiplexer circuit.

Figure 1 shows the circuit schematic of a 74LS153 circuit.

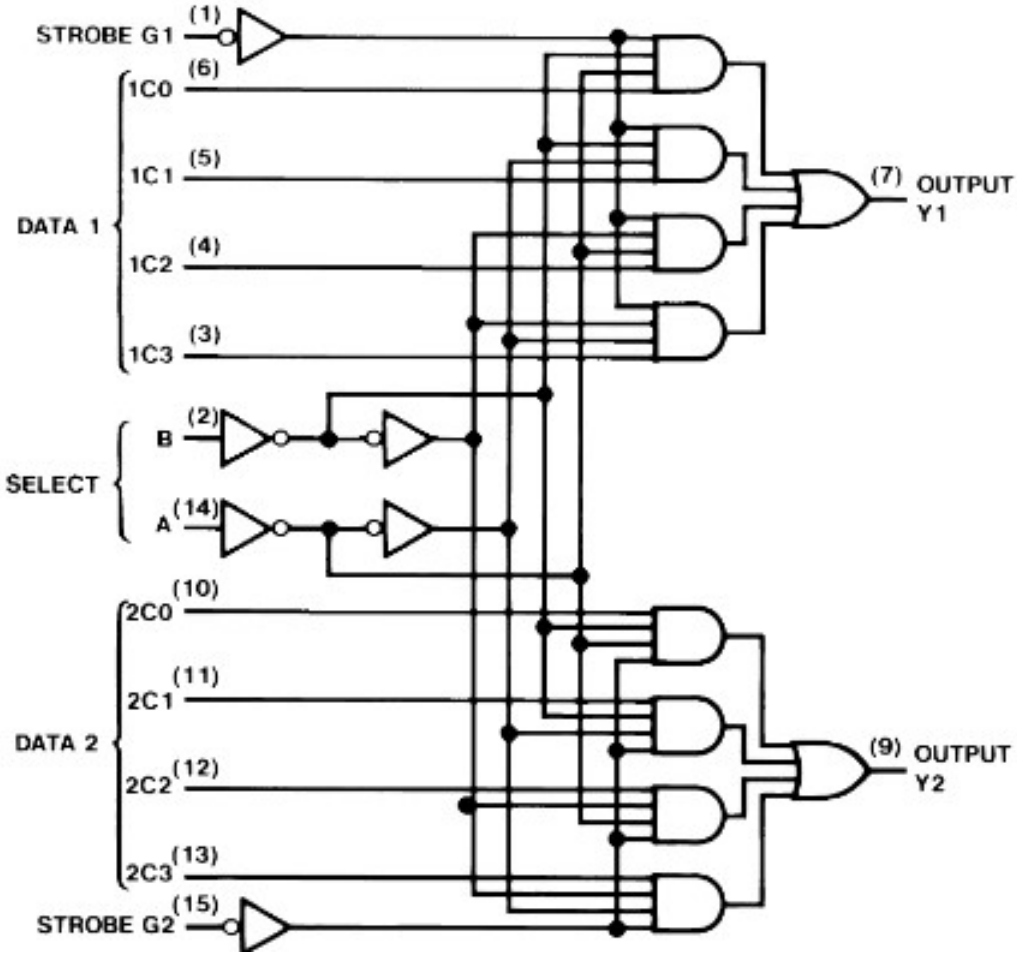


Figure 1: *Circuit Schematic for 74LS153*

Figure 1 shows two 4:1 multiplexers with active low enable. The inputs $G1$ and $G2$ represent the enable for their respective multiplexer. The multiplexers share two select inputs: A and B. $Data1$ which was later called $C1$ represents the first 4-bit data input. $Data2$ which was later called $C2$ represents the second 4-bit input data. The outputs are represented as $Y1$ and $Y2$. Based on the enable, selects, and the data input, two bits of data is outputted from the circuit.

The propagation delay from each gate was taken into account when creating the circuit in VHDL. The data flow model does not contain propagation delay. The structural model included propagation delay for each gate. The inverter had a propagation delay of 4 ns. The AND and OR gates had a propagation delay of 7 ns. The behavioral model included the worst case delay of 22 ns.

Results and Analysis

The circuit was created in VHDL using structural, data flow, and behavioral models. Each model was verified using simulation. A testbench was created in ModelSim to test each model. It should be noted only one multiplexer of the dual 4:1 multiplexer circuit was used in the testbench.

The first test used the test set described in Table 1.

Table 1: *Test Set 1*

G	B	A	C3	C2	C1	C0
0	0	0	1	1	1	0
0	0	0	0	0	0	1
0	0	1	1	1	0	1
0	0	1	0	0	1	0
0	1	0	1	0	1	1
0	1	0	0	1	0	0
0	1	1	0	1	1	1
0	1	1	1	0	0	0

Table 1 describes the simulated input values every 100 ns.. The selects signals are A and B. The inputs $C3$, $C2$, $C1$, and $C0$ represent the four bit input data. The G represents the enable. G was set to logic 0 so the outputs would not be reset automatically to 0. The test set was used with the testbench to simulate the three circuit models.

The resulting simulated waveforms are shown in Figure 2.

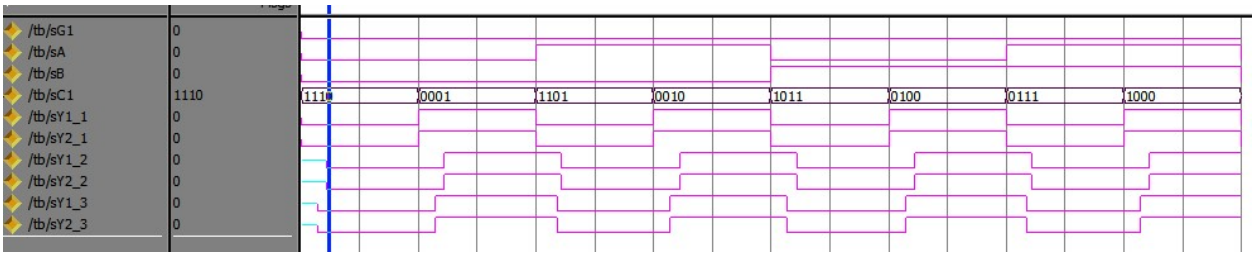


Figure 2: *Simulated Test 1*

Figure 2 shows expected results. Signals $sY1\_1$ and $sY2\_1$ show the data flow model that includes no propagation delay. This can be seen with how the wave forms only change values on the same edge as when G,A, and/or B is changed. Signals $sY1\_2$ and $sY2\_2$ show the output value of the behavioral model that has a propagation delay of 22 ns. This can be seen with how the output change is delayed by 22 ns after the input is changed. Signals $sY3\_2$ and $sY3\_2$ show the output value of the structural model that has propagation delay for each gate. The delay can be seen with how the output change is delayed after the input is changed. The change is not simultaneous like the data flow model. Due to the delay in the structural and behavioral model, their respective output signals are initially undefined.

The second test used the test set described in Table 2.

Table 2: *Test Set 2*

G	B	A	C3	C2	C1	C0
0	0	0	1	0	1	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	1	0	1	0
0	0	0	0	1	0	1
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	0	1	0	1

Table 2 is used in the testbench and describes the simulated input values every 100 ns.

The resulting simulated waveforms of test set 2 are shown in Figure 3.

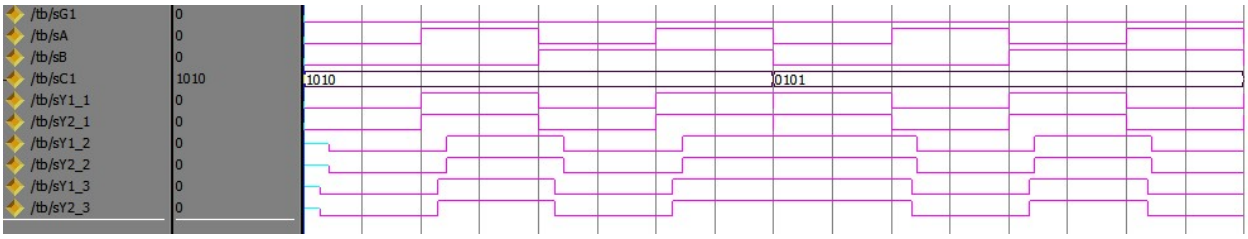


Figure 3: *Simulated Test 2*

Figure 3 shows expected results. Signals $sY1\_1$ and $sY2\_1$ show the data flow model that includes no propagation delay. This can be seen with how the wave forms only change values on the same edge as when G,A, and/or B is changed. Signals $sY1\_2$ and $sY2\_2$ show the output value of the behavioral model that has a propagation delay of 22 ns. This can be seen with how the output change is delayed by 22 ns after the input is changed. Signals $sY3\_2$ and $sY3\_2$ show the output value of the structural model that has propagation delay for each gate. The delay can be seen with how the output change is delayed after the input is changed. The change is not simultaneous like the data flow model. Due to the delay in the structural and behavioral model, their respective output signals are initially undefined.

The third test used the test set described in Table 3.

Table 3: *Test Set 3*

G	B	A	C3	C2	C1	C0
1	0	0	1	0	1	0
1	0	1	1	0	1	0
1	1	0	1	0	1	0
1	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	0	1	0	1

Table 3 is used in the testbench and describes the simulated input values every 100 ns. Table 3 has the same values as Table 2 except G is high.

The resulting simulated waveforms of test set 3 are shown in Figure 4.

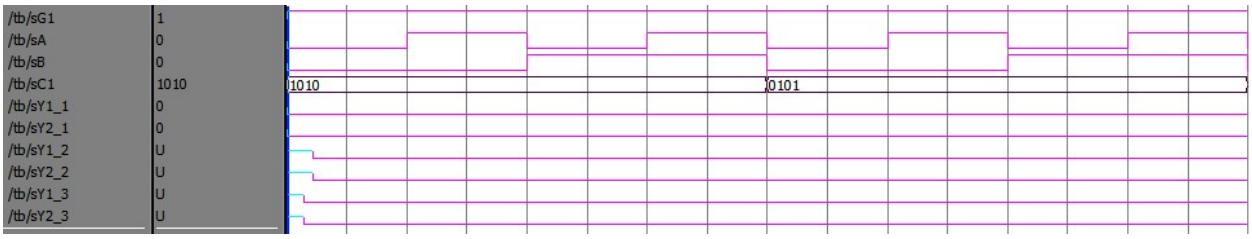


Figure 4: *Simulated Test 3*

Figure 4 shows expected results. Regardless of the model type, because the enable is high (*G* is 1), all outputs will reset to logic 0. This is seen in the Figure 4. Due to the delay in the structural and behavioral model, their respective output signals are initially undefined.

Conclusion

Using a datasheet, a dual 4:1 multiplexer circuit was created using three different models in VHDL. A testbench was created to test one of the 4:1 multiplexers in ModelSim. The data flow, structural, and behavioral models were verified through simulation. The data flow model had no propagation delay, the behavioral model had worst case propagation delay, and the structural model has propagation delay for each gate. Three test sets were simulated and the results were as expected, so the exercise was a success. Each model outputs the same expected results, but with different propagation delay. Understanding multiple ways to create a circuit in VHDL and the timing characteristics of each model is important for engineers to know.

Questions

1. Explain the meaning of delta delays and concurrent statements in the context of VHDL. Show how changes on inputs (signals) trigger the execution of other statements–make delta cycles visible. Draw the corresponding circuit in Quartus II.
   Delta delays are the infinitesimal assignment delay at which signals are changed. Concurrent statements describe signal assignments that happen simultaneously.

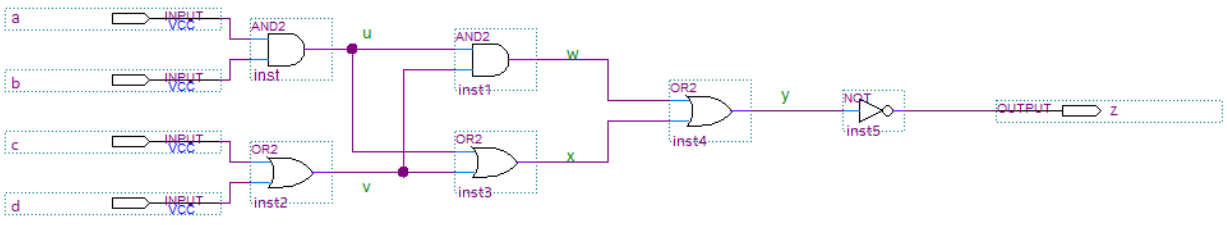


Figure 5: *Circuit Schematic*

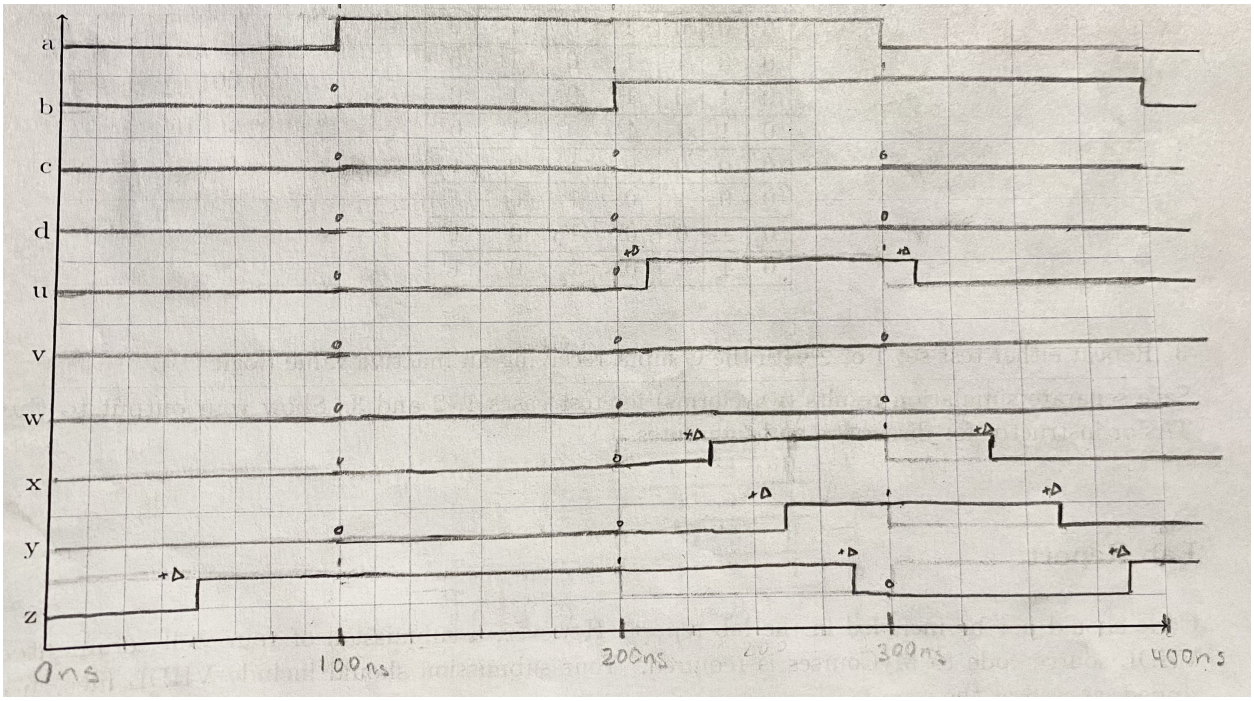


Figure 6: *Timing Diagram*

Exercise 11: Modeling of Combinational Circuits Using Concurrent and Sequential Statements

Student's Name:_____ Section:_____

Prelab		Point Value	Points Earned	Comments
Prelab	Entity declaration	5	5	a 11/8
	Data flow architecture	5	5	
	Behavioral architecture	5	5	
	Structural architecture	5	5	

Demo		Point Value	Points Earned	Date
Demo	Test case 1	15	15	mcm 11/8
	Test case 2	15	14	mcm 11/8
	Test case 3	10	10	mcm 11/8

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 11: Modeling of Combinational Circuits Using Concurrent and Sequential Statements

Report		Point Value	Points Earned	Comments
Abstract		3		
Design Methodology	Discussion of circuit functionality	5		
Results and Analysis	Test methodology	3		
	Simluation results	10		
Conclusion		3		
Questions		6		
Writing Composition		3		
Source code	Comments	3		
	Style	4		
Total for prelab, demo, and report		100		