CMPE-160 Digital System Design 1

Laboratory Exercise 4

Combinational Logic Circuit Design using Boolean Algebra Simplification

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

Lucy Zhang

Lucy Zhang
Performed 13 September 2022
Submitted 20 September 2022

Lab Section:	1
Instructor:	Purab Sutradhar
TA:	Morgan Kreifels Karisha Pradham Colin Vo
Lecture Section:	1
Lecture Instructor:	Richard Cliver

Abstract

A Boolean expression was simplified using Boolean algebraic simplification and implemented in a circuit using combinational logic. The logic circuit is given a two-bit binary number and a selection control signal and performs operations that output a 4-bit number. LED's were used in the circuit implementation to determine the output of the expression and compared with the Boolean expression's truth table. The purpose of this exercise was to identify the effectiveness of simplified Boolean expressions and gain experience with creating combinational logic circuits. The circuit functioned successfully as planned and displayed the correct output.

Design Methodology

The logic circuit has three inputs: the selection control signal (C) and the two-bit binary number represented by N ($N1$, $N0$). The selection control signal at logic state "0" performs the operation $F = N^2$ where the output (F) is N squared. When C is at logic state "1", the output is $F = 5N$, or five times the input number. The output produces a four-bit number represented by F = (W, X, Y, Z). Using a truth table, the output logic state can be determined.

Table 1 is the truth table of C, $N1$, and $N0$.

Table 1: *Truth Table for Mathematical Operations* N^2 *and* $5N$

C	*N1*	*N0*	*W*	*X*	*Y*	*Z*
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	1	0	0
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	1	0	1	0	1
1	1	0	1	0	1	0
1	1	1	1	1	1	1

Table 1 shows the expected output for mathematical operators N^2 and $5N$. Based on the binary number formed by the input of $N1$ and $N2$ and the operator as determined by C, the four-bit output is produced. The W,X,Y, and Z represent the number output in binary. The upper half of the table shows N^2 for the numbers zero through 3. The lower half of the table shows $5N$ for the numbers zero through 3.

Minterms refer to when a truth table outputs a "1". For the truth table in Table 1, the minterms can be found on different rows depending on which output is being examined. For each output column a sum of products Boolean expression can be formed using the minterms.

The sum of products Boolean expressions for the outputs W,X,Y, and Z were:

$$W(C,N1,N0) = C'N1N0 + CN1N0' + CN1N0 \tag{1}$$

$$X(C,N1,N0) = C'N1N0' + CN1'N0 + CN1N0 \tag{2}$$

$$Y(C,N1,N0) = CN1N0' + CN1N0 \tag{3}$$

$$Z(C,N1,N0) = C'N1'N0 + C'N1N0 + CN1'N0 + CN1N0 \tag{4}$$

Equations (1), (2), (3), and (4) describe the output of Table 1 and the function being performed (N^2 and $5N$).

To build the most efficient circuit with the least number of two-input gates used, the Boolean expressions were simplified.

The steps to simplify the Boolean expression for W were as follows:

$$W = (C'N1N0) + (CN1N0') + (CN1N0) \tag{5}$$

$$\textbf{Distributive Law}\quad N1N0(C' + C) + CN1N0 \tag{6}$$

$$\textbf{Complement Law}\quad N1N0(1) + CN1N0 \tag{7}$$

$$\textbf{Identity Law}\quad N1(N0 + CN0') \tag{8}$$

$$\textbf{Absorption Law}\quad N1(N0 + C) \tag{9}$$

$$\textbf{Distributive Law}\quad W = N1N0 + N1C \tag{10}$$

Shown in (5), (6), (7), (8), (9), and (10), different Boolean algebra laws were applied to simplify the original expression. For example, (6) was evaluated by using the distributive law and (7) was derived using the complement law. Equation (10) shows the final simplified Boolean expression for W.

The steps to simplify the Boolean expression for X were as follows:

$$X = C'N1N0' + CN1'N0 + CN1N0 \tag{11}$$

$$\textbf{Distributive Law}\quad CNO(N1' + N1) + C'N1N0' \tag{12}$$

$$\textbf{Complement Law}\quad CN0(1) + C'N1N0' \tag{13}$$

$$\textbf{Identity Law}\quad X = CN0 + C'N1N0' \tag{14}$$

Equations (11), (12), (13), and (14) show the Boolean algebra laws applied to simplify the original expression for X. For example, (13) was derived from (12) using the complement law. The final simplified Boolean expression for X is shown in (14).

The steps to simplify the Boolean expression for Y were as follows:

$$Y = CN1N0' + CN1N0 \tag{15}$$

$$\textbf{Distributive Law} \quad CN1(N0' + N0) \tag{16}$$

$$\textbf{Complement Law} \quad CN1(1) \tag{17}$$

$$\textbf{Identity Law} \quad Y = CN1 \tag{18}$$

Equations (15), (16), (17), and (18) show the Boolean algebra laws applied to simplify the original expression for Y. For example, (17) was derived from (16) using the complement law and (18) was derived from (17) using the identity law. The final simplified Boolean expression for Y is shown in (18).

The steps to simplify the Boolean expression for Z were as follows:

$$Z = C'N1'N0 + C'N1N0 + CN1'N0 + CN1N0 \tag{19}$$

$$\textbf{Distributive Law} \quad N1'N0(C' + C) + N1N0(C' + C) \tag{20}$$

$$\textbf{Complement Law} \quad N1'N0(1) + N1N0(1) \tag{21}$$

$$\textbf{Identity Law} \quad N0(N1' + N1) \tag{22}$$

$$\textbf{Distributive Law} \quad N0(C' + C) \tag{23}$$

$$\textbf{Complement Law} \quad N0(1) \tag{24}$$

$$\textbf{Identity Law} \quad Z = N0 \tag{25}$$

Equations (19), (20), (21), (22), (23), (24), and (25) show the Boolean algebra laws applied to simplify the original expression for Z. More steps were needed to simplify Z. The final simplified Boolean expression for Z is shown in (25). The output Z ended up being the same as the input $N0$.

Using the simplified Boolean expressions in (10), (14), (18), and (25), the circuit in Figure 1 was created.

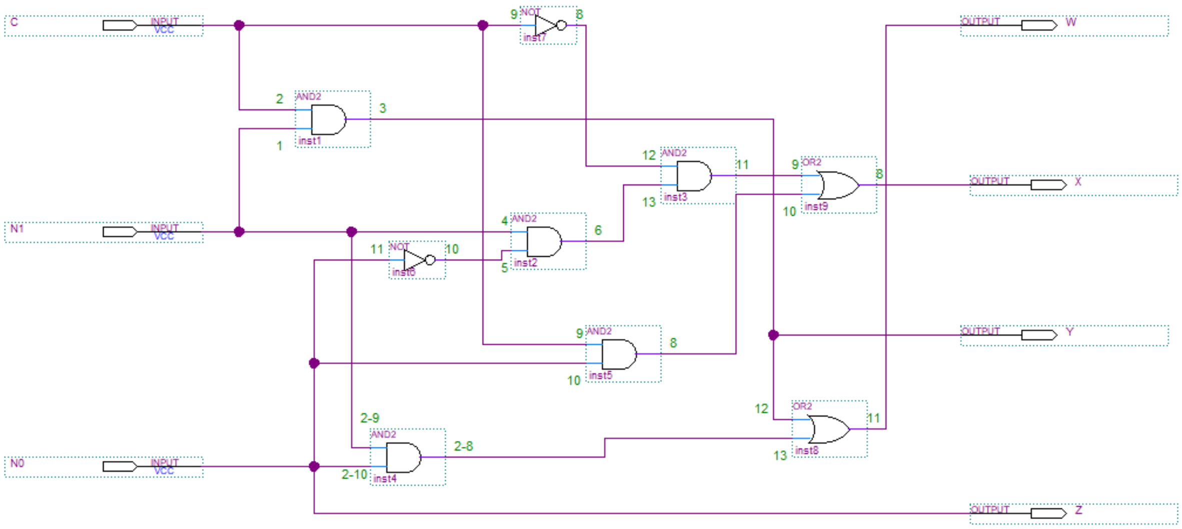
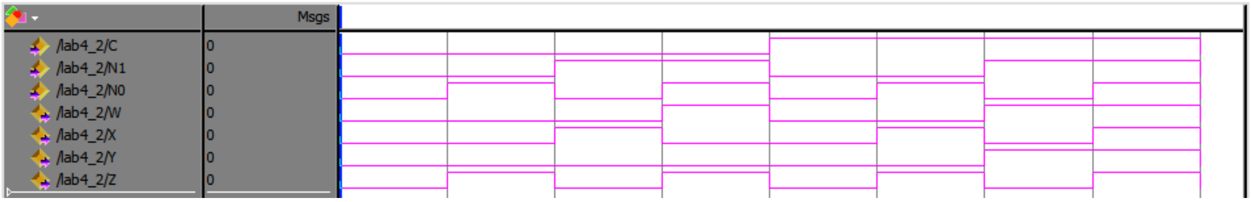


Figure 1: *Circuit Schematic for Mathematical Operations N^2 and $5N$*

Figure 1 shows the circuit schematic for the mathematical operation described in Table 1. There is three inputs (C, $N1$, $N0$) and four outputs (W, X, Y, Z). Each output represents the simplified Boolean expressions derived in (10), (14), (18), and (25). The schematic uses two 2-input AND chips (#74LS08), one 2-input OR chip (#74LS32), and one inverter (#74LS04). The second AND chip is denoted by ”2-” followed by the appropriate pin numbers.

Results and Analysis

To check the accuracy of the circuit created in Figure 1, the waveform in Figure 2 was generated using ModelSim.



```
                Msgs
/lab4_2/C       0
/lab4_2/N1      0
/lab4_2/N0      0
/lab4_2/W       0
/lab4_2/X       0
/lab4_2/Y       0
/lab4_2/Z       0
```

Figure 2: *Waveform for Circuit Schematic*

Figure 2 shows the expected outputs given all the combinations for a three variable input. The waveform proved the circuit in Figure 1 was correct. The waveform generated matched the truth table in Table 1. Every 50 nanoseconds, at least one input inverts its value, creating a simulation of the truth table with 1's and 0's.

A circuit was constructed using the circuit schematic in Figure 1. The inputs (C, $N1$, $N0$) were connected to switches and the outputs (W, X, Y, Z) were connected to red LED's. A closed switch represented a logic 0 and an open switch represented a logic 1. Similarly, the LED's turned on with a logic 1 and turned off with a logic 0. The truth table in Figure 1 can be used to find the expected performance of the LED's.

The test results of the circuit are shown in Table 2:

Table 2: Results of Circuit Created

Switch 1 (C)	Switch 2 ($N1$)	Switch 3 ($N0$)	LED 1 (W)	LED 2 (X)	LED 3 (Y)	LED 4 (Z)
Closed	Closed	Closed	off	off	off	off
Closed	Closed	Open	off	off	off	on
Closed	Open	Closed	off	on	off	off
Closed	Open	Open	on	off	off	on
Open	Closed	Closed	off	off	off	off
Open	Closed	Open	off	on	off	on
Open	Open	Closed	on	off	on	off
Open	Open	Open	on	on	on	on

Table 2 shows the recorded results of the circuit created. When switches corresponding to the value of the inputs (C, $N1$, $N0$) were changed, the LED's representing the outputs (W, X, Y, Z) responded as expected. Compared to the truth table in Table 1, the results are exactly as expected. The circuit worked as expected.

Conclusion

Using a truth table, Boolean algebra expressions were created. Then using Boolean algebra laws, those expressions were simplified. Based on the simplified expressions, a circuit was created and implemented. The circuit was verified first using a simulated waveform that was generated, then verified with the test results. The exercise was a success. The circuit worked as expected. The truth table's expected outputs were the same as the outputs seen with the LED's in the implemented circuit. This shows how the simplified Boolean expressions have the same output as the original Boolean expressions derived from Table 1. The simplified Boolean expressions got the same results as the original expressions while using fewer gates and chips. This experiment shows how a simplified Boolean expression can be more gate and chip efficient.

Questions

1. Equivalent gate count (EGC) -the total number of 2-input gates required to implement the expression.
   (a) For direct implementation of the expressions:
   The EGC was 35 gates (24 two-input AND gates, 8 two-input OR gates, and 3 inverters).
   (b) For simplified expressions
   The EGC was 10 gates (6 two-input AND gates, 2 two-input OR gates, and 2 inverter gates).
2. Chip count from basic gates (i.e., ANDs, ORs, and inverters) -the total number of ICs (chips) required to implement the expression
   (a) For direct implementation of the expressions:
   The chip count was 9 chips (6 two-input AND chips, 2 two-input OR chips, and 1 inverter).
   (b) For simplified expressions
   The chip count was 4 chips (2 two-input AND chips, 1 two-input OR chip, and 1 inverter chip).

Exercise 4: Combinational Logic Circuit Design Using Boolean Algebra Simplification

Student's Name:______________________ Section:______________________

Prelab		Point Value	Points Earned	Comments
Part 1	Table completed	3	3	4/13
	Expressions correct	2	2	
Part 2	Correct simplified equations	1	1	
	Steps shown	2	2	
	Boolean properties shown	2	2	
Part 3	Correct schematic	3	3	
	Pin and chip numbers	1	1	
	Correct simulation	4	4	
	Parts placement diagram	2	2	

Demo		Point Value	Points Earned	Date
Demo	Two fully functional output pins	20	20	4/13
	Additional two fully functional output pins	20	20	

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 4: Combinational Logic Circuit Design Using Boolean Algebra Simplification

Report		Point Value	Points Earned	Comments
Abstract		5		
Design Methodology	Truth table	4		
	Boolean expressions	4		
	Correct simplified equations	1		
	Steps shown	2		
	Boolean properties shown	2		
	Schematic	4		
Results and Analysis	Discussion	5		
Conclusion		3		
Questions	EGC	3		
	Chip count	3		
Writing Composition		4		
Total for prelab. demo. and report		100		