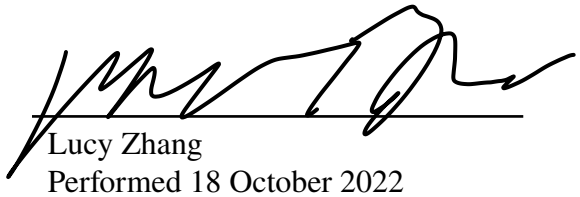
CMPE-160 Digital System Design 1

Laboratory Exercise 8

Analysis and Simulation of Sequential Circuits

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.



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Abstract

The circuit schematic of a 4-bit shift register was created using an AND-OR network for multiplexer logic. The circuit was recreated implementing tri-state buffers for multiplexer logic. Both circuits were simulated and analyzed. The timing of the circuit using an AND-OR network was examined. Results were as expected and the exercise was successful.

Design Methodology

A state/output table was made to describe the functionality of the 4-bit shift register. It was unnecessary to list all possible combinations of 1s and 0s like in a truth table. The functionality of the 4-bit shift register can be described with 4 rows. It should be noted that the 4-bit shift register uses rising edge D flip flops.

Table 1 shows the possible outputs of the 4-bit shift register.

Table 1: *State/Output Table for a 4-bit Shift Register*

CLK	RST	SL	A	B	C	D	Q_A^*	Q_B^*	Q_C^*	Q_D^*	
X	0	X	X	X	X	X	0	0	0	0	reset
↑	1	0	X	X	X	X	SIN	Q_A	Q_B	Q_C	shift-right
↑	1	1	X	X	X	X	A	B	C	D	load
not rising	1	X	X	X	X	X	Q_A	Q_B	Q_C	Q_D	hold

Table 1 shows how the 4-bit shift register only has four different functions: reset, shift-right, load, and hold. The reset function sets all outputs to logic 0. The shift-right function, as the name describes, shifts all previous values to the right ($Q_B{}^*$ becomes Q_A, $Q_C{}^*$ becomes Q_B, etc.) and the leftmost output column in the table, or the most significant bit (MSB), becomes SIN. The load function loads in the values of A, B, C, and D. The hold function retains the previous states values. Denoted to the right of each row is the kind of function of the row. The X symbol means that the value does not matter for the function; regardless of the value the output or function would be the same. The up arrow in the CLK column represent the rising edge of the clock waveform, and "not rising" means any time when the clock is not at the rising edge.

After understanding the functionality of a 4-bit shift register, a circuit schematic was created.

Figure 1 shows the circuit schematic created.

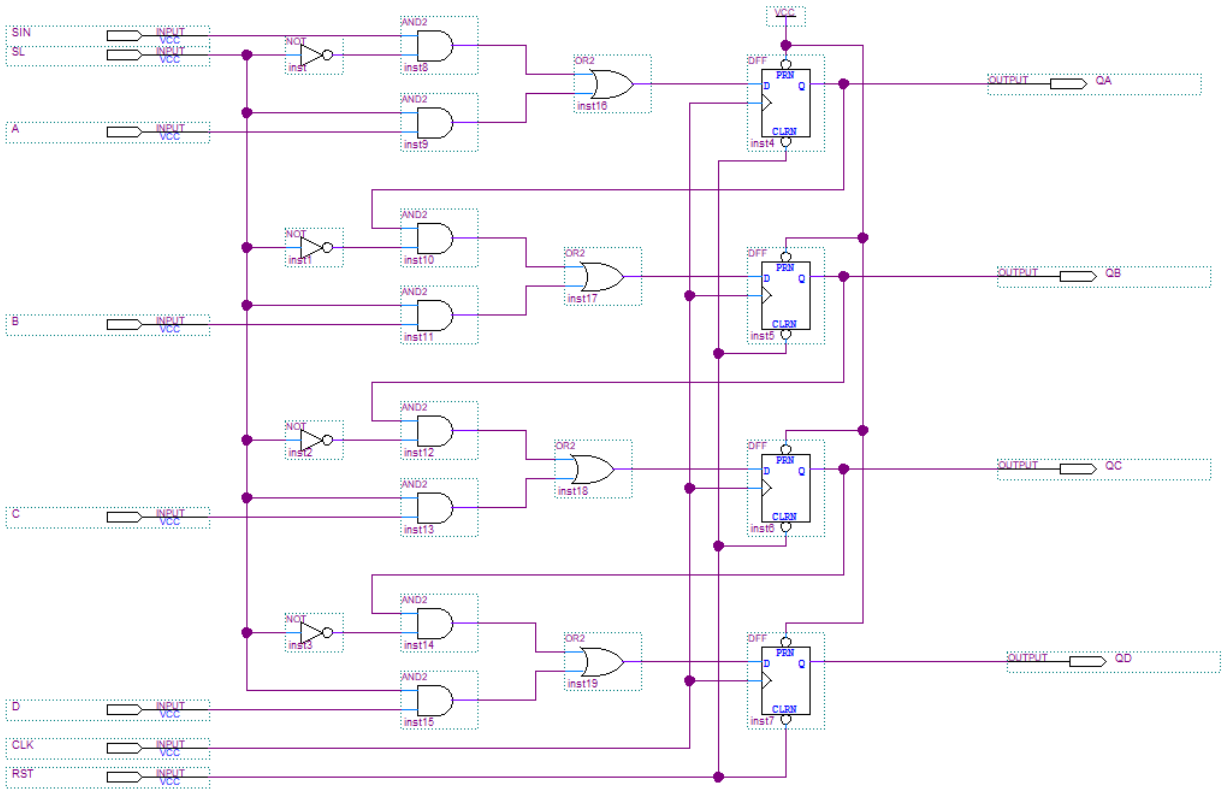

Figure 1: *Four-bit Shift Register with AOI Multiplexers*

Figure 1 shows the circuit schematic of a 4-bit shift register using AOI logic multiplexers. There are several inputs that determine which function the circuit performs. Regardless of all other inputs, if the input RST is 0, all outputs would be 0. The RST is asynchronous (with the clock) and is active low. The input CLK is where the clock waveform is connected to the circuit. Because the circuit uses rising edge triggered D flip flops, the rising edge of the clock determines when either the shift-right or load function happens. The SL input is the control line that switches the function between loading and shifting right. The serial input is SIN which is necessary for the shift right function as seen in Table 1. The SIN becomes the MSB with each shift right operation. The inputs A, B, C, and D are the 4 bit parallel inputs. In this circuit, the 4-bits initially represent "B" in hex. The outputs in the circuit are QA, QB, QC, and QD which correspond to Q_A^*, Q_B^*, Q_C^*, and Q_D^* respectively in Table 1. The outputs are the 4-bit parallel output, where QA is the MSB and QD is the LSB from the LSB flip flop. The AND and OR gates in this circuit perform the same actions as a 2:1 multiplexer.

A 2:1 multiplexer can also be implemented using a tri-state buffer.

Figure 2 shows the circuit schematic of a four-bit shift register using tri-state buffers.

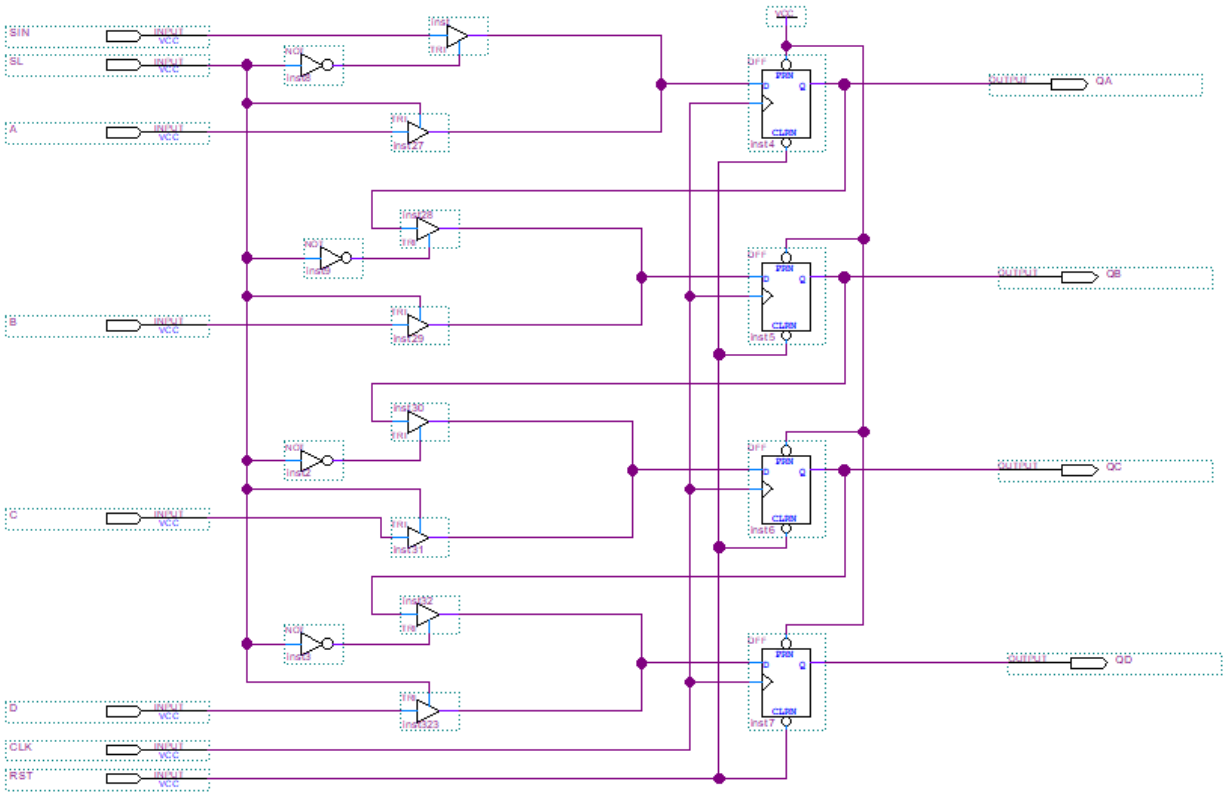

Figure 2: *Four-bit Shift Register with Multiplexers*

Figure 2 shows how the AND-OR logic can be replaced with tri-state buffers. The inputs and outputs remain the same as Figure 1. The functionality of this circuit is the same as the one described in Table 1 and seen in Figure 1.

Results and Analysis

After circuit schematics were made, the circuits were verified in ModelSim. The circuit shown in Figure 1 was simulated.

Figure 3 shows the waveform generated by the circuit with AND-OR gates.

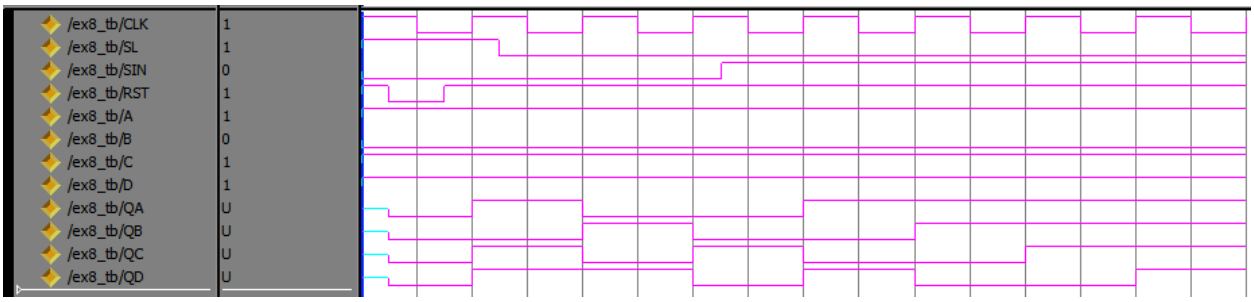

Figure 3: *Simulation Results for Figure 1*

Figure 3 shows the expected waveforms for the circuit described in Figure 1. The outputs are initially blue before the initial rising clock edge. This is due to the fact that the load function is triggered by a rising clock edge. Once *RST* is set to 0 do the outputs have a value of 0. The *RST* can be seen effecting the output asynchronously from the clock (CLK). The outputs also appear to be shifting right (or down in Figure 3) with the MSB being replaced by the value of SIN.

The same simulation was run with the circuit described in Figure 2.

Figure 4 shows the the waveform generated by the circuit with tri-state buffers.

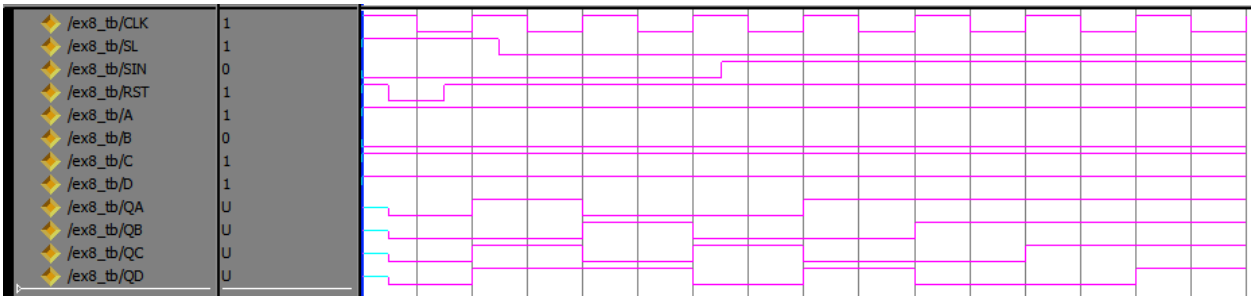

Figure 4: *Simulation Results for Figure 2*

Figure 4 shows the same results as Figure 3 as expected. The two circuits have the same functionality with different logic elements, so the results were expected to be the same.

The results of the simulations were also recorded in a table.

Table 2 shows the operation of the four-bit shift register.

Table 2: *Four-bit Shift Register Operation*

Time	Register Contents		
	Binary ($QA\ QB\ QC\ QD$)	Hex	Decimal
After Reset	0 0 0 0	0	0
Clock Cycle 1	1 0 1 1	B	11
Clock Cycle 2	0 1 0 1	5	5
Clock Cycle 3	0 0 1 0	2	2
Clock Cycle 4	1 0 0 1	9	9
Clock Cycle 5	1 1 0 0	C	12

Table 2 shows how the outputs of the 4-bit shift register changes with each clock cycle. When compared with the waveform in Figure 3, the shift-right operation can be seen clearly. The bits shift right with the MSB being replaced with the SIN value. The results of Table 2 were as expected.

The timing of sequential circuits is important for their operation. T_{min} is the minimum clock period that the circuit can operate correctly at. The maximum operating speed of a circuit can then be determined from the T_{min} of a circuit.

The T_{min} of a circuit can be determined with Equation (1).

$$T_{min} = t_{co} + t_{pd} + t_s$$

Equation (1) describes how the minimum clock period that the circuit with AND-OR logic could operate at correctly. t_{co} is the clock to output time, t_s is the setup time, and t_{pd} is the propagation delay through the logic. For the circuit with AND-OR logic, the t_{co} was 6.078ns, the t_s was 2.689ns, and the t_{pd} was 0ns. The T_{min} was calculated using (1) and was 8.767ns. T_{min} was converted from seconds to 114.064MHz. This means the maximum frequency the shift register can operate at is about 114MHz.

Conclusion

Using knowledge of the operations of a shift register and rising edge D flip flops, a function table for a four-bit shift register was made. A circuit of a four-bit shift register was created with AND-OR logic as multiplexers and another was created with tri-state buffers as multiplexers. Both circuits were verified through simulation. The simulation were as expected and the exercise was successful. A better understanding of timing in the design and operation of sequential circuits was gained. T_{min} is important for finding operating speed and the minimum clock period a circuit can operate at correctly. Thus, it is important to understand how to calculate T_{min} and where the value comes from.

Questions

1. What kind of arithmetic operation occurs when a value is shifted right one bit and a zero is introduced into the most significant bit position?
   The arithmetic operation that occurs is division.

2. What kind of arithmetic operation occurs when a value is shifted left one bit and a zero is introduced into the least significant bit position?
   The arithmetic operation that occurs is multiplication.

3. Assume the flip-flops are sensitive to the rising edge of the clock. Explain why it is not a good idea to change the input signals at exactly the same time as the rising edge of the clock.
   Due to the delay of the change of input signals, the input signal may not be correct exactly at the rising edge of the clock. Changing the input signals at exactly the same time as the rising edge of the clock may cause hazards, where the expected output is different from expected.

Exercise 8: Analysis and Simulation of Sequential Circuits

Student's Name:_____ Section:_____

Prelab		Point Value	Points Earned	Comments
Prelab	Part 1	5	5	MCH 10/18
	Part 2	5	5	
	Part 3	10	10	

Demo		Point Value	Points Earned	Date
Demo	Part 1 Simulation	15	15	KP 10/18
	Part 2 Simulation	15	15	CV 10/18
	Timing Analysis	10	10	MCH 10/14

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 8: Analysis and Simulation of Sequential Circuits

Report		Point Value	Points Earned	Comments
Abstract		3		
Design Methodology	Function table	5		
	Circuit diagram	5		
	Circuit diagram with multiplexors	4		
Results and Analysis	Simulation results	6		
	Timing analysis	3		
Conclusion		4		
Questions	Q1	2		
	Q2	2		
	Q3	2		
Writing Composition		4		
Total for prelab, demo, and report		100		