

# A Unified Capacitor Stress Emulation Method for High-Power Converter Applications

Bo Yao<sup>ID</sup>, *Graduate Student Member, IEEE*, Haoran Wang, *Member, IEEE*, Qian Wang<sup>ID</sup>, *Member, IEEE*, and Huai Wang<sup>ID</sup>, *Senior Member, IEEE*

**Abstract**—In this article, authors propose a unified capacitors stress emulation method, which has two unique test capabilities: concurrent electrical stress emulation to ac capacitors and dc capacitors, and different electrical stress levels (including different ripple current, ripple voltage, and dc voltage) can be individually controlled for the testing samples. It preserves the advantages of a recently reported method with a minimum required power supply and is robust to testing sample degradation. This method is suitable for application-oriented stress emulation testing with different types of dc/ac capacitors and multiple electrical stresses in high-power converter systems. The circuit architecture and testing ability of this method are presented. Moreover, analytical models are derived to size the key components to realize various testing requirements. Proof-of-concept experimental results are presented to verify the feasibility of the proposed test method.

**Index Terms**—AC capacitors, dc capacitors, electrical stresses, high-power converter, key components, stress emulation.

## I. INTRODUCTION

CAPACITOR is typically a high-failure component in power electronic converter systems, and its reliability has become a major focus of attention in recent years [1]. The failure or deterioration of capacitors can lead to a decline in filtering capabilities, which can ultimately lead to the overstressing of components and even the catastrophic failure of the converter system [2]. The realistic stress emulation testing is a significant part of the performance characterization and reliability analysis of capacitors. Through these tests, reliable capacitor parameteric models can be developed and design margins can be optimized to ensure the long-term reliability and safety of the system [3].

There are two emerging demands for capacitor testing in high-power converter applications. On the one hand, it is desirable to

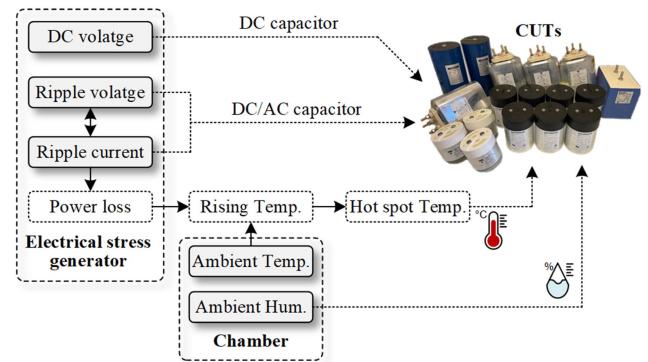


Fig. 1. Stress targets for capacitor stress emulation testing.

perform application-oriented testing with realistic conditions. For the lifetime model and the accelerated aging model, it is necessary to determine its pending empirical coefficients by comparing multiple realistic stresses [4]. In the safe operating area testing, different stress ranges are required to analyze the boundary conditions [5], [6]. On the other hand, it would bring new values if ac and dc capacitors can be concurrently tested with the capability of individual stress control. This can significantly reduce overall test time compared with single stress testing by allowing for concurrent multistress control [7], [8]. The testing parameters of the capacitor stress emulation generally include ripple voltage, ripple current, dc voltage (for dc capacitors), and the environmental conditions (e.g., temperature, humidity, etc.), as shown in Fig. 1 [9]. Different ambient temperatures and humidity can be simulated by the climatic chambers [10]. Therefore, performing multiple electrical stresses under realistic conditions is critical for ac and dc capacitor testing in high-power converter applications.

Recent studies have made significant efforts toward the capacitor stress emulation, as given in Table I. In [11], [12], and [13], a voltage source converter and a current source converter are connected in parallel to apply the dc voltage and ripple current for capacitors under testing (CUTs). However, the scope of testing electrical stresses in those methods is limited by the size of the power supplies. The commercial ripple current testers emulate up to 30–100 V ripple voltage and 10–30 A ripple current for CUTs, but the output ripple power range is restricted to 1 k VA [14], [15]. In [16] and [17], the authors use a circuit structure in which a converter is connected in series with CUTs, and the ripple current can be configured according to

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Bo Yao and Huai Wang are with the Department of Energy, Aalborg University, 9220 Aalborg, Denmark (e-mail: ybo@energy.aau.dk; hwa@energy.aau.dk).

Haoran Wang is with the Three Gorges Intelligent Industrial Control Technology Corporation, Ltd., Wuhan 430070, China (e-mail: wang\_haoran@ctg.com.cn).

Qian Wang is with the School of Automation, Wuhan University of Technology, Wuhan 430070, China (e-mail: qiw@whut.edu.cn).

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TABLE I  
COMPARISONS OF THE EXISTING TEST METHODS

Testing ability in existing capacitor stress emulation methods					Applicable field	Electrical stress emulation range	Reference
DC voltage	Ripple current and ripple voltage (pk to pk)						
10 V	Single stress	1 A	4 V	Single stress	Low power Al capacitors	<1kW power	[11]
-	Single stress	10 A	1 V	Single stress			[12]
-	Single stress	<0.1 A	600 V	Single stress			[13]
500 V	Single stress	30 A	30 V	Single stress	Low power ceramic capacitors	1–10kW	[14]
5000 V	Single stress	30 A	30 V	Single stress	Al capacitors / Ceramic capacitors		[15]
3000 V	Single stress	600 A	30 V	Single stress	Medium power Film capacitors	10–100kW	[16]
	Single stress	18 A	1000 V	Single stress	Medium power Film capacitors		[17]
400 V	Single stress	80 A	150 V	Single stress	Low power Film capacitors		[18]
>3000 V	Single stress	>1000 A	>1000 V	Single stress	Al capacitors and medium power film capacitors	High power film capacitors	[19]
>3000 V	Different stress levels (Individually controlled)	>1000 A	>1000 V	Different stress levels (Individually controlled)	High power film capacitors		MW power
					High power film capacitors	MW power	Lack

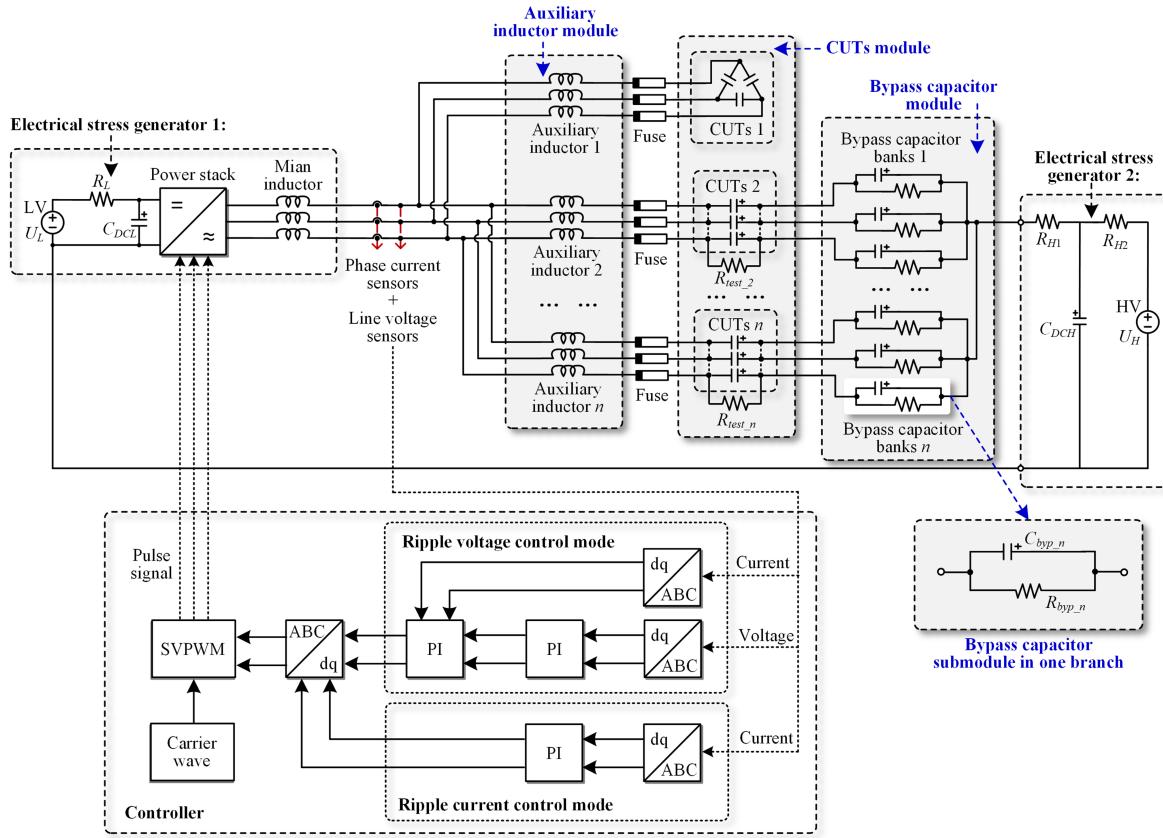


Fig. 2. Circuit architecture of the unified capacitors stress emulation method.

the converter specifications. Nevertheless, the converter needs to directly withstand the dc voltage component of the CUTs in those methods, which may not be feasible for high-power capacitor testing with thousands of volts of dc voltage. The power converters are used in the voltage sources with the fixed 120 °C three-phase symmetrical voltage in [18] and [19]. The ripple voltage and ripple current can be controlled according to the control system, and the dc voltage of the CUTs can be expanded based on the additional dc bias supply. However, only single electrolytic stresses can be emulated at the same time in those testing methods. Existing methods for emulating realistic high-power capacitor electrical stress have limitations, either being unable to provide the megawatt-level testing requirements

in high-power applications [11], [12], [13], [14], [15], [16], [17], [18] or being able to provide such requirements but with the need for multiple test benches or longer testing time [19].

Yao et al. [20] proposed a unified capacitor stress emulation method for concurrently testing dc and ac capacitors. This article version has the following additional contributions.

- 1) Auxiliary inductors and bypass capacitors are proposed for the testing circuit, enabling individual control of the voltage and current stresses of multiple capacitor samples, which cannot be achieved by the method in [20].
- 2) Analytical models and a design flow are provided, which can be used for designing the testing system to fulfill certain specifications.

TABLE II  
TEN TESTING SCENARIOS THAT CAN BE ACHIEVED BY THE PROPOSED CIRCUIT ARCHITECTURE SHOWN IN FIG. 2

Testing scenarios	CUTs	Ripple voltage and ripple current	DC voltage	Electrical stress generator 1	Electrical stress generator 2	Auxiliary inductor module	Bypass capacitor module	Can be done by existing methods or new possibilities
1	AC capacitors	Single	-	✓	-	-	-	Existing methods [11] – [19]
2	DC capacitors	Single	Single	✓	✓	-	-	
3	AC capacitors	Individual	-	✓	-	✓	-	
4	DC capacitors	Individual	Single	✓	✓	✓	-	
5	DC capacitors	Single	Individual	✓	✓	-	✓	
6	DC capacitors	Individual	Individual	✓	✓	✓	✓	
7	DC + AC capacitors	Single	Single	✓	✓	-	-	[20] (Conference version)
8	DC + AC capacitors	Individual	Single	✓	✓	✓	-	Enabled by the extended ideas proposed in this journal paper
9	DC + AC capacitors	Single	Individual	✓	✓	-	✓	
10	DC + AC capacitors	Individual	Individual	✓	✓	✓	✓	

3) Extended experimental testing and application scenarios are presented.

The rest of this article is organized as follows. Section II presents the concept, circuit architecture, and test abilities of the proposed method. Section III gives the design models and typical testing scenarios. Section IV discusses the experimental verification. Finally, Section V concludes this article.

## II. PROPOSED STRESS EMULATION METHOD

### A. Circuit Architecture of the Proposed Method

The circuit architecture of the proposed method is shown in Fig. 2. It is an extension of the circuit presented in [20] by adding an auxiliary inductor module and a bypass capacitor module. Besides the capability to test both dc capacitors and ac capacitors concurrently, the ac voltage, ripple current, and dc bias voltage of the CUTs in different branches can be individually controlled.

1) *Electrical Stress Generator and Controller:* The electrical stress generator 1 is used to apply ripple voltage and ripple current for CUTs. It generates sinusoidal current to the CUTs through the low-voltage (LV) power supply  $U_L$  and the power stack. The electrical stress generator 2 provides the dc bias voltage if necessary, denoted as the high-voltage (HV) power supply  $U_H$ , the filter capacitor  $C_{DCH}$ , and the stack resistors  $R_H$  are included.

In the controller, a three-phase space vector pulsewidth modulation (SVPWM) scheme is used to modulate the three-phase current with the sinusoidal waveform. This controller can operate in either voltage mode or current mode to control the ripple voltage and ripple current, respectively.

2) *Auxiliary Inductor Module:* This module enables the individual ripple voltage and ripple current control of the CUTs in different testing branches. The auxiliary inductors provide reactive power that is opposite in phase to the ripple current and voltage for the CUTs, thereby boosting the output ripple voltage and ripple current of the main inductor. By selecting the different inductance of the auxiliary inductors, the individual ripple voltages and ripple currents for the CUTs are provided in different branches. The ripple voltage and ripple current can be maintained in the presence of capacitor degradation in any branch by the closed-loop control.

3) *CUTs Module:* The CUTs can be Y- or  $\Delta$ -connection for ac capacitors, and Y-connection for dc capacitors, with either

a single or multiple parallel connections. The required ripple voltage and ripple current of the CUTs are provided by the electrical stress generator 1 and the auxiliary inductor module. For dc capacitor testing, the dc component voltage of the CUTs is provided by the electrical stress generator 2 and bypass capacitor module. The parallel resistors of CUTs  $R_{test}$  can serve dual purposes. On the one hand, they can be used to discharge the CUTs at the end of the testing process, and on the other hand, they can divide the dc voltage component based on bypass capacitor modules.

4) *Bypass Capacitor Module:* This module is for providing individual dc-bias control of the dc capacitors in different testing branches. The capacitors and resistors in the circuit are responsible for dividing the output dc voltage of the HV power supply. By selecting specific capacitance  $C_{byp}$  for bypass capacitors, it is possible to provide controllable dc voltage components to the CUTs of different branches in the start up stage. The configured parallel resistors  $R_{byp}$  can serve dual purposes. On the one hand, they can maintain a steady-state dc voltage component, and on the other hand, they can be used to discharge the CUTs at the end of the testing process. Thus, the dc voltage component can maintain a given value at a steady state, despite any changes to the capacitance of the CUTs due to aging [21]. The selection of bypass capacitors and parallel resistors enables the provision of individual dc voltage components to CUTs and ensures that the dc voltage remains constant throughout the testing process.

### B. Testing Scenarios and the Corresponding Circuit Configurations

Table II tabulates ten achievable testing scenarios by configuring the circuit architecture shown in Fig. 2. Out of them, Scenarios 3–10 are unique by the proposed method, with Scenario 7 being presented in [20]. Scenarios 3 and 4 support the function of “individual ripple voltage and ripple current;” Scenario 5 supports the function of “individual dc voltage;” and Scenario 7 supports the function of “concurrent ac and dc capacitor testing.” Moreover, Scenario 6 supports both functions of “individual ripple voltage and ripple current” and “individual dc voltage.” Scenario 8 supports both functions of “individual ripple voltage and ripple current” and “concurrent ac and dc capacitor testing.” Scenario 9 supports both functions of “individual dc

voltage" and "concurrent ac and dc capacitor testing." Scenario 10 supports all three functions.

When the single electrical stress is applied in the ac capacitors and dc capacitors testing, the root mean square (rms) value of ripple voltage  $U_{\text{ripple}}$  and ripple current  $I_{\text{ripple}}$ , and the dc voltage component  $U_{\text{dc}}$  for the dc capacitors of CUTs can be shown as (Scenarios 1, 2, and 7 in Table II)

$$\begin{cases} U_{\text{ripple}} = U_{\text{line}} & (\Delta\text{-connection ac capacitors}) \\ U_{\text{ripple}} = \frac{1}{\sqrt{3}}U_{\text{line}} & (\text{Y-connection ac/dc capacitors}) \\ I_{\text{ripple}} = I_{\text{ac}} = U_{\text{ripple}} \times 2\pi f_R C_{\text{test}} \\ U_{\text{dc}} = U_{\text{HV}} - \frac{1}{2}U_{\text{LV}} & (\text{dc capacitors}) \end{cases} \quad (1)$$

where  $U_{\text{line}}$ ,  $I_{\text{ac}}$ ,  $C_{\text{test}}$ , and  $f_R$  represent the line rms voltage between the inductors and CUTs, the ac-side rms current, the capacitance of the CUTs, and the ripple frequency, respectively. In the dc capacitors testing,  $U_{\text{HV}}$  and  $U_{\text{LV}}$  represent the output voltage of the HV power supply and the LV power supply, respectively.

The auxiliary inductors can boost the output ripple voltage and ripple current based on the main inductor. On the ac side, the reactive power of the CUTs  $Q_C$  and the auxiliary inductors  $Q_L$  can be given as

$$\begin{cases} Q_C = \frac{I_{\text{ripple}}^2}{2\pi f_R \times C_{\text{test}}} \\ Q_L = I_{\text{ripple}}^2 \times 2\pi f_R \times L_{\text{aux}} \end{cases} \quad (2)$$

where  $L_{\text{aux}}$  is the inductance of the auxiliary inductor in different branches.

When individual ripple current and ripple voltage in different branches are applied to CUTs, the rms value of ripple current  $I_{\text{ripple}_i}$  and the rms value of ripple voltage  $U_{\text{ripple}_i}$  of the CUTs at the  $i$ th branch are given by (Scenarios 3, 4, 6, 8, and 10 in Table II)

$$\begin{cases} I_{\text{ripple}_i} = \frac{|Q_c - Q_L|}{U_{\text{ripple}_0}} = \frac{U_{\text{ripple}_0}}{\left| \frac{1}{2\pi f_R C_{\text{test}_i}} - 2\pi f_R L_{\text{aux}_i} \right|} \\ U_{\text{ripple}_i} = \frac{I_{\text{ripple}_i}}{2\pi f_R C_{\text{test}_i}} = \frac{U_{\text{ripple}_0}}{\left| 1 - 4\pi^2 f_R^2 L_{\text{aux}_i} C_{\text{test}_i} \right|} \end{cases} \quad (3)$$

where  $U_{\text{ripple}_0}$  represents the output ripple voltage of the main inductor and  $C_{\text{test}_i}$  represents the capacitance of the CUTs in the  $i$ th branch.

In addition, considering that the individual dc voltage in different branches are applied to dc capacitors, the dc voltage components  $U_{\text{dc}_i}$  of CUTs at the  $i$ th branch are given (Scenarios 5, 6, 9, and 10 in Table II).

At the start up of the testing (charge the CUTs and the bypass capacitors)

$$U_{\text{dc}_i} = \frac{C_{\text{byp}_i}}{C_{\text{test}_i} + C_{\text{byp}_i}} \left( U_{\text{HV}} - \frac{1}{2}U_{\text{LV}} \right). \quad (4)$$

At the steady state

$$U_{\text{dc}_i} = \frac{R_{\text{test}_i}}{R_{\text{test}_i} + R_{\text{byp}_i}} \left( U_{\text{HV}} - \frac{1}{2}U_{\text{LV}} \right) \quad (5)$$

where  $R_{\text{test}_i}$ ,  $R_{\text{byp}_i}$ , and  $C_{\text{byp}_i}$  represent the parallel resistance of CUTs, the parallel resistance of the bypass capacitor, and the capacitance of the bypass capacitor in the  $i$ th branch, respectively. The resistance of parallel resistors set to 100 kΩ–1 MΩ. In this state, the parallel resistance is much smaller than the insulation resistance of the film capacitors (typical value: 10<sup>3</sup>–10<sup>6</sup> MΩ) [22], thus coping with the effects of insulation resistance temperature and aging changes.

### III. DESIGN MODELS FOR COMPONENT PARAMETERS

The properly designed components can effectively minimize excessive margins in parameters. The identification of suitable design components for the testing method, based on application-specific testing requirements, is of concern to users. This section quantitatively analyzes the design parameters of the key components in the testing method. The analytical equations derived are universal and can be applied to the electrical stress requirements of different specifications and quantities of the CUTs testing. The presented numerical results in figures are based on a specific design case with the specifications described.

#### A. Power Stack Selection

The selection of the power stacks is determined primarily by the output current. When the required output current of the power stack is larger, the cost and volume of the power stack increase accordingly [23]. When the single ripple current and ripple voltage are applied to CUTs, the rms value of the required output current for the power stack  $I_{\text{PS-out}}$  can be expressed as

$$I_{\text{PS-out}} = mU_{\text{rate}} \times (2\pi f_R \times C_{\text{test}}) \quad (6)$$

where  $m$  and  $U_{\text{rate}}$  represent the ripple voltage acceleration factor and the rate ripple voltage for CUTs, respectively.

When the individual ripple current and ripple voltage are applied in different branches, the  $I_{\text{PS-out}}$  can be given as

$$I_{\text{PS-out}} = \sum_{i=1}^n m_i U_{\text{rate}} \times (2\pi f_R \times C_{\text{test}_i}) \quad (7)$$

where  $m_i$  represent the ripple voltage acceleration factor for CUTs in the  $i$ th branch.

As shown in Fig. 3(a) and (c), the required output current of the power stack with different testing requirements is obtained. The results indicate that when the voltage acceleration factor is 1.4 and the number of CUTs is 9, the current required by the power stack is 375 A at the ripple frequency of 50 Hz. When the ripple frequency is 60 Hz, the required output current of the power stack rises to 450 A in this case.

#### B. Main Inductor and Auxiliary Inductors Design

The selection of the three-phase inductors is determined primarily by the inductance and rated current. When the inductance and the rated current of inductors are larger, the cost and volume of the inductors increase accordingly [24]. The primary function of the inductors is to boost the ripple voltage and ripple current. The main inductor can boost the output voltage of the power stack, and the auxiliary inductors can further boost the output

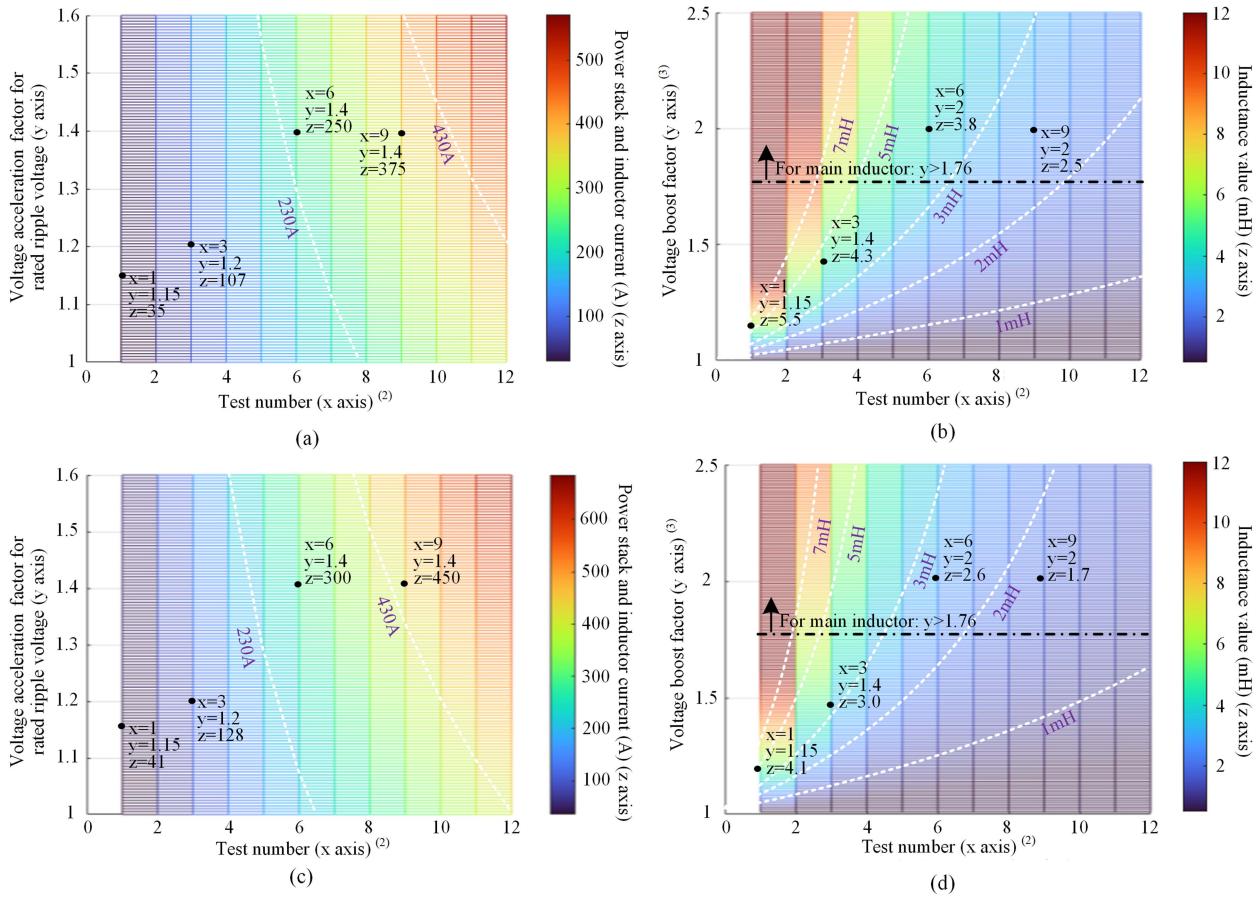


Fig. 3. Selection of power stacks and parameters design of inductors. (a) Required current of power stack, main inductor, and auxiliary inductors ( $f_R = 50$  Hz). (b) Required inductance of main inductors and auxiliary inductors ( $f_R = 50$  Hz). (c) Required current of power stack, main inductor, and auxiliary inductors ( $f_R = 60$  Hz). (d) Required inductance of main inductors and auxiliary inductors ( $f_R = 60$  Hz). (1. CUTs parameters:  $\Delta$  – connection AC capacitors; capacitance of single CUT  $C_{\text{test}_i}$  :  $75 \mu\text{F}$ ; rate ripple voltage  $U_{\text{rate}} = 730$  V.) (2. For the power stack and main inductor, the test number means the total number of CUTs in each of the three-phase branches; for the auxiliary inductors, the test number means the number of CUTs in this three-phase branch.) (3. For the main inductor, the voltage boost rate refers to the ratio of the main inductor output voltage to the power stack output voltage, 530 V; for auxiliary inductors, the voltage boost rate refers to the ratio of the auxiliary inductors output voltage to the main inductor output voltage.) (4. In (a) and (c), the ranges of 230 and 430 A represent the rated output current of two power stacks [23].)

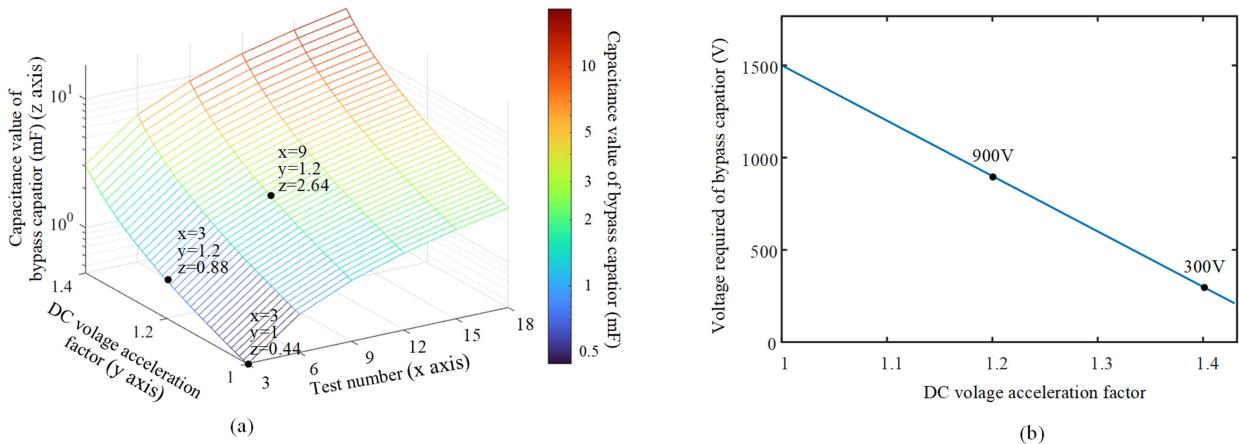


Fig. 4. Design parameters of bypass capacitor. (CUTs parameters: Y-connection DC capacitors; the capacitance of single CUT  $C_{\text{test}_i}$  :  $220 \mu\text{F}$ ; rate DC voltage  $U_{\text{rate}}$  :  $3000$  V, HV voltage  $U_{\text{HV}}$  :  $5000$  V, LV voltage  $U_{\text{LV}}$  :  $1000$  V; test number is the total number of CUTs in each of the three-phase branches.) (a) Required capacitance of bypass capacitor. (b) Required voltage of bypass capacitor.

voltage of the main inductor. When the single ripple current and ripple voltage are applied, the required inductance  $L_{\text{main}}$  and required current  $I_{L-\text{main}}$  of the main inductor can be given as

$$\begin{cases} I_{L-\text{main}} = mU_{\text{rate}} \times (2\pi f_R \times C_{\text{test}}) \\ L_{\text{main}} = \left(1 - \frac{U_m}{U_{\text{ripple}}}\right) \times \frac{1}{4\pi^2 f_R^2 C_{\text{test}}} \end{cases} \quad (8)$$

where  $U_m$  is the output rms voltage in the power stack.

When the individual ripple currents and ripple voltages are applied in different branches, the required inductance  $L_{\text{main}}$  and required current  $I_{L-\text{main}}$  of the main inductor can be given as

$$\begin{cases} I_{L-\text{main}} = \sum_{i=1}^n m_i U_{\text{rate}} \times (2\pi f_R \times C_{\text{test\_}i}) \\ L_{\text{main}} = \left(1 - \frac{U_m}{U_{\text{ripple\_}0}}\right) \times \frac{1}{4\pi^2 f_R^2 C_{\text{test}}} \end{cases} \quad (9)$$

Its required inductance  $L_{\text{Aux}_i}$  and required current  $I_{L-\text{Aux\_}i}$  of the auxiliary inductors in the  $i$ th branch can be given as

$$\begin{cases} I_{L-\text{Aux\_}i} = m_i U_{\text{rate}} \times (2\pi f_R \times C_{\text{test\_}i}) \\ L_{\text{Aux}_i} = \left(1 - \frac{U_{\text{ripple\_}0}}{U_{\text{ripple\_}i}}\right) \times \frac{1}{4\pi^2 f_R^2 C_{\text{test}}} \end{cases} \quad (10)$$

The second function of the ac side inductor in this circuit architecture is filtering, which can convert the output square wave voltage of the power stack into the required sinusoidal ripple voltage. In the circuit architecture of this test method, the inductors and CUTs form an  $LC$  filter loop. The relationship between the cutoff frequency  $f_{\text{cut}}$  and the ripple frequency  $f_R$  can be used to characterize its filtering range. Its filter capability can be expressed by the relationship between the cutoff frequency  $f_{\text{cut}}$  and the ripple frequency  $f_R$  [25]. The ripple frequency should satisfy the following:

$$f_R > \frac{1}{2} f_{\text{cut}} = \frac{1}{2} \times \frac{1}{2\pi \times \sqrt{L_{\text{main}} C_{\text{test}}}}. \quad (11)$$

Therefore, the inductance of the main inductor should satisfy the following:

$$L_{\text{main}} > \frac{1}{16\pi^2 f_R^2 C_{\text{test}}}. \quad (12)$$

The performance of the main inductor and the auxiliary inductors with respect to the current requirements is shown in Fig. 3(a) and (c). The results indicate that the output current of the main inductor is consistent with the output current of the power stack. For example, when the voltage acceleration factor for a single CUT is 1.15, the current required by the auxiliary inductor in this branch is 35 A. When the voltage acceleration factor with three CUTs is 1.2, the current required by the branch auxiliary inductor is 107 A in this branch.

The required inductance of the main inductor and the auxiliary inductors with different numbers of CUTs are shown in Fig. 3(b) and (d). The results demonstrate that, when the boost voltage rate is 2 and the CUTs number is 9, the required inductance of the main inductor is 2.5 and 1.7 mH, respectively, for generating 50 and 60 Hz ripple frequency. In addition, when the boost voltage rate is 1.4 and the CUTs number is 3, the required inductance of the auxiliary inductor in this branch is 4.3 and 3.0 mH, corresponding to the ripple frequency at 50 and 60 Hz, respectively.

Moreover, according to (11) and (12), the inductance of the main inductor is constrained by the cutoff frequency. In this case, the inductance of the main inductor should not be lower than the range of 1.76 times the voltage boosting rate.

### C. Bypass Capacitor and Its Parallel Resistor Design

The selection of the bypass capacitor is primarily determined by the capacitance and rated voltage. The cost and volume of the capacitor are positively related to the capacitance and rated voltage [26].

Similarly, the selection of the parallel resistor depends on its resistance and power.

Different bypass capacitors and parallel resistors can provide individual dc voltage for the CUTs in different branches. The required bypass capacitance  $C_{\text{byp\_}i}$  and parallel resistance  $R_{\text{byp\_}i}$  in the  $i$ th branch can be expressed as

$$\begin{cases} C_{\text{byp\_}i} = \frac{C_{\text{test\_}i} \times m_{\text{dc\_}i} U_{\text{rate\_dc}}}{\left(U_{\text{HV}} - \frac{1}{2} U_{\text{LV}}\right) - m_{\text{dc\_}i} U_{\text{rate\_dc}}} \\ R_{\text{byp\_}i} = \frac{R_{\text{test\_}i} \times \left(\left(U_{\text{HV}} - \frac{1}{2} U_{\text{LV}}\right) - m_{\text{dc\_}i} U_{\text{rate\_dc}}\right)}{m_{\text{dc\_}i} U_{\text{rate\_dc}}} \end{cases} \quad (13)$$

where  $m_{\text{dc\_}i}$  represents the dc voltage acceleration factors in the  $i$ th branch and  $U_{\text{rate\_dc}}$  represents the rated dc voltage for dc capacitors.

The bypass capacitors and parallel resistors need to withstand partial dc voltage division provided by the HV power supply, which should satisfy the following:

$$U_{\text{byp}} = U_{\text{HV}} - \frac{1}{2} U_{\text{LV}} - m_{\text{dc\_}i} U_{\text{rate\_dc}}. \quad (14)$$

The selection of the bypass capacitors with different CUTs numbers and different dc voltage acceleration factors is shown in Fig. 4. The results indicate that as the number of CUTs and the dc voltage acceleration factors increases, the required capacitance of the bypass capacitors in this branch increases and the rated voltage of the bypass capacitors decreases accordingly. For example, when the voltage acceleration factors are 1.0 and 1.2, the capacitance of the bypass capacitors in this branch are 0.44 and 0.88 mF, respectively. In this case, the rated voltage of the bypass capacitors in this branch is 1500 and 900 V, respectively.

### D. Power Supply Sizing

The selection of the power supply is determined primarily by the output power. The cost and volume of the power supply increase accordingly with the required output power of the power supply [27]. In the proposed testing method, the power losses of the power stack, inductors, and CUTs are provided by the LV power supply, and the output voltage of the LV power supply is limited by the output voltage of the power stack  $U_m$ . The power requirement  $P_{\text{LV}}$  and the output voltage  $U_{\text{LV}}$  of the LV power

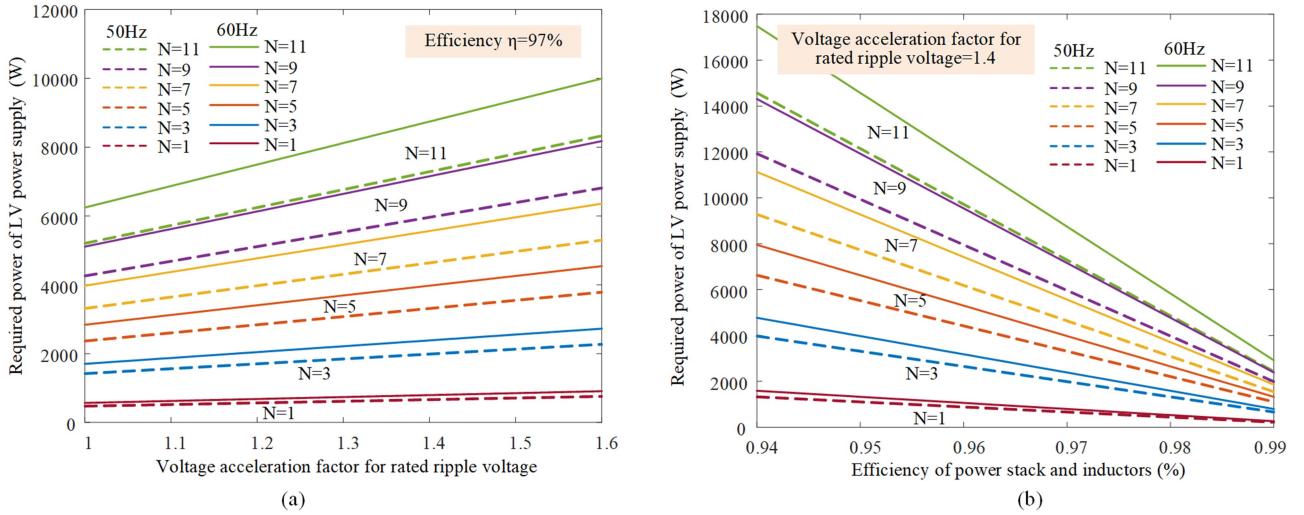


Fig. 5. Selection of LV power supply size. (a) Required power of LV power supply with different voltage acceleration factor. (b) Required power of LV power supply with different efficiency. (CUTs parameters:  $\Delta$  – connection AC capacitors; the capacitance of single CUT  $C_{\text{test}_i}$  : 75  $\mu\text{F}$ ; rate ripple voltage  $U_{\text{rate}}$  : 730 V;  $N$  is the total number of CUTs in each of the three-phase branches.)

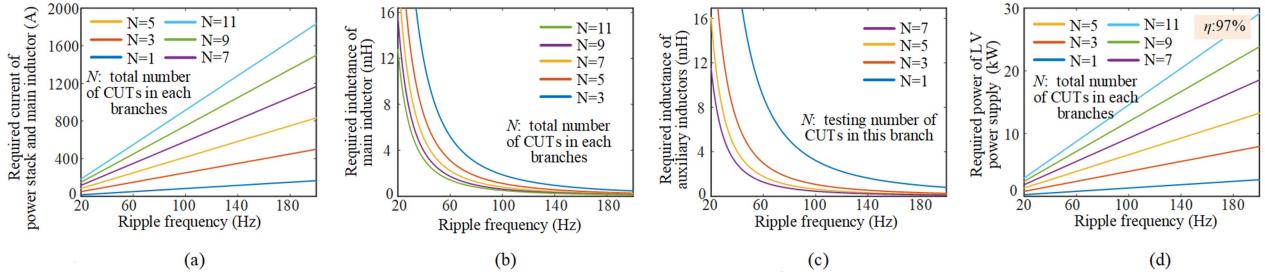


Fig. 6. Design parameters of the power stack, the inductors, and the LV power supply with different ripple frequencies. (a) Required current of power stack and main inductor. (b) Required inductance of main inductor. (c) Required inductance of auxiliary inductor in this branch. (d) Required power of LV power supply. (1. CUTs parameters:  $\Delta$  – connection AC capacitors; the capacitance of single CUT  $C_{\text{test}_i}$  : 75  $\mu\text{F}$ ; rate ripple voltage  $U_{\text{rate}}$  : 730 V.) (2. The Voltage acceleration factor is 1.4 for the power stack and the LV power design; the voltage boost factor for the main inductor is 2.0 and for auxiliary inductors is 1.4.)

supply can be given as

$$\begin{cases} P_{\text{LV}} \approx I_{\text{ripple}}^2 R_{\text{total}} + (1 - \eta) I_{\text{ripple}} U_m \\ U_{\text{LV}} \geq M_r \times \frac{U_m}{0.707} \quad (M_r \leq 1) \end{cases} \quad (15)$$

where the  $\eta$  is the efficiency of the power stack and inductors at the specific operating condition of interest, and the  $R_{\text{total}}$  represents the equivalent series resistance of the CUTs.  $M_r$  represents the utilization rate of dc-link voltage in the SVPWM modulation [28].

The selection of LV power supply based on a specific design case is shown in Fig. 5. As the ripple voltage acceleration factor and the number of CUTs increase, and the efficiency decreases, it can be observed that the output power required by the LV power supply increases. Meanwhile, the output voltage of the LV power supply should not be less than 750 V according to the limitation of the SVPWM modulation ratio and power stack output voltage in this case.

In dc capacitors testing, the dc voltage is determined by the output voltage of the HV power supply. The output current of the HV power supply can be limited by configuring the resistance

of the stack resistor. The required voltage  $U_{\text{HV}}$  and the required current  $I_{\text{HV}}$  of the HV power supply can be given by

$$\begin{cases} U_{\text{HV}} = U_{\text{dc}} + \frac{1}{2} \frac{U_{\text{LV}}}{R_{\text{HV}}} \\ I_{\text{HV}} < \frac{U_{\text{LV}}}{R_{H1} + R_{H2}} \end{cases} \quad (16)$$

where the  $R_{H1}$  and  $R_{H2}$  are two stack resistors in the dc capacitor testing circuit.

#### E. Components Design for Different Ripple Frequencies

According to the preceding models, the design parameters of components, such as power stack, inductors, and power supply, are affected by the ripple frequency of CUTs. Fig. 6 shows the design parameters of the power stack, inductors, and LV power supply with different ripple frequencies. As the ripple frequency increases, so does the required current of the power stack and inductors, and the required power of the LV power supply. Inversely, as the ripple frequency increases, the required inductance of the inductors decreases.

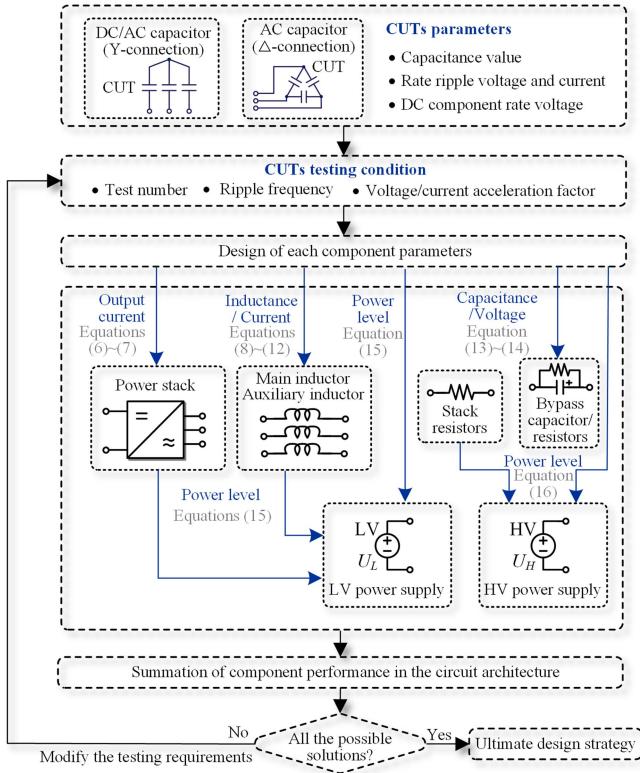


Fig. 7. Design process of the unified stress emulation method.

#### F. Design Process and Application-Oriented Cases

Based on the design models of component parameters, the design process of the proposed method is shown in Fig. 7. According to the specific testing requirements, the output current of the power stack, the inductance and current of the inductors, and the bypass capacitance and parallel resistance can be restricted. Considering the power level of the power stack and inductors, and the ripple current for CUTs, the required size of the LV power supply can be given. Based on the selection of stack resistors and the dc voltage component for CUTs, the required size of the HV power supply can be obtained. If the design parameters obtained from these components can be implemented, the design process results in the desired output; otherwise, the testing conditions need to be adjusted.

The examples of typical testing specifications for different power electronics applications are given in Table V (see the Appendix), including wind power converters [8], railway traction converters [29], and electric vehicle traction inverters [30].

## IV. EXPERIMENTAL VERIFICATION AND IMPLEMENTATION

### A. Experimental Platform and Parameters

The capacitor testing system is shown in Fig. 8. As given in Table III, the capacitance of the CUTs is 75 (ac capacitors) and 220  $\mu\text{F}$  (dc capacitors). The rated ripple voltage of the ac capacitor and the dc capacitor is 730 and 422 V, respectively. The rated voltage of the dc capacitors is 3000 V, and the testing ripple frequencies are 50 and 60 Hz.



Fig. 8. Photograph of the capacitor testing system.

TABLE III  
EXPERIMENTAL PLATFORM PARAMETERS

Experiment platform parameters	
Main inductor	2.5 mH
Auxiliary inductor	5.6 mH
Bypass capacitor and its parallel resistance	1.29 mF 200 k $\Omega$
Stack resistors	10*2 k $\Omega$
LV output voltage	750 V
HV output voltage	3375 V (3000 V dc voltage for dc capacitors + 1/2 LV voltage)
Switch frequency	5000 Hz
CUTs parameters	
Test capacitor	AC capacitor ( $\Delta$ -connection) DC capacitor (Y-connection)
Capacitance of single CUT	75 $\mu\text{F}$
Ripple testing voltage (rms)	730 V/840 V/1022 V
DC testing voltage (rms)	-
Ripple frequency	50/60 Hz

TABLE IV  
ERROR ANALYSIS OF THE TESTING SYSTEM

Testing	Parameter (rms)	Calculation	Testing	Accuracy
Exp. 1 (Fig. 9)	Ripple voltage for ac capacitor	730 V	724 V	99.2%
	Ripple current for ac capacitor	29.7 A	29.3 A	98.7%
	Ripple voltage for dc capacitor	422 V	420 V	99.5%
	Ripple current for dc capacitor	29.0 A	29.1 A	99.6%
	DC voltage for dc capacitor	3000 V	3022 V	99.3%
Exp. 2 (Fig. 10)	LV required current	5.8 A	6.0 A	96.7%
	Ripple voltage with auxiliary inductor	840 V	848 V	99.1%
Exp. 3 (Fig. 11)	Ripple current with auxiliary inductor	34.2 A	34.5 A	99.2%
	DC voltage with bypass capacitor	2000 V	1980 V	99.0%
Exp. 4 (Fig. 12)	Ripple voltage ( $f_R = 50$ Hz)	1022 V	1013 V	99.2%
	Ripple voltage ( $f_R = 60$ Hz)	1022 V	1011 V	98.9%
	Ripple voltage ( $f_R = 100$ Hz)	1022 V	1027 V	99.5%
	Ripple voltage ( $f_R = 120$ Hz)	1022 V	1035 V	98.7%
	Ripple voltage ( $f_R = 300$ Hz)	1022 V	1016 V	99.4%
	Ripple voltage ( $f_R = 360$ Hz)	1022 V	1013 V	99.1%

The specific platform parameters design process is as follows. First, for the power stack and main inductor design, the 1.0–1.4 acceleration factors of ripple voltage and ripple current are applied to CUTs (9 pcs for ac capacitors and 6 pcs for dc capacitors). According to (6)–(9), the rated current of power stack and main inductor should be greater than 375 (50 Hz) and 450 A (60 Hz). Meanwhile, according to (8)–(9) and (11)–(12),

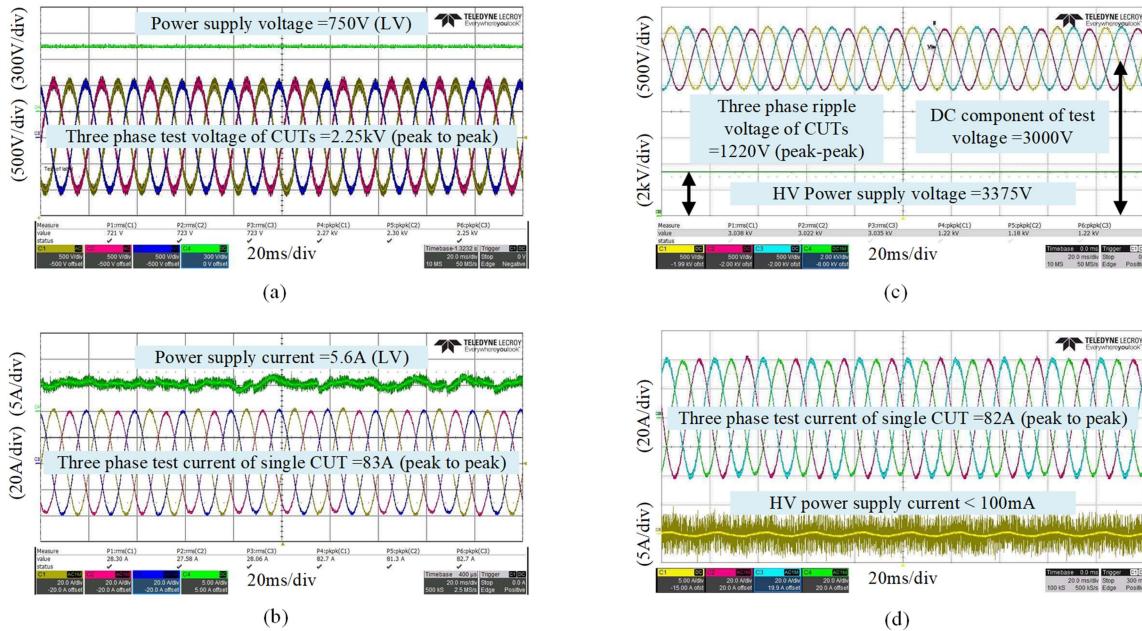


Fig. 9. Experimental results for DC capacitors and AC capacitors concurrently testing. (a) Voltage waveform in AC capacitors testing. (b) Current waveform in AC capacitors testing. (c) Voltage waveform in DC capacitors testing. (d) Current waveform in DC capacitors testing. (Scenario 7 in Table II, 7 pcs AC capacitors and 6 pcs DC capacitors in parallel, ripple frequency: 50 Hz).

the inductance of the main inductor should be greater than 2.5 (50 Hz), 1.7 (60 Hz), and 1.76 mH (cutoff frequency limitation).

For the auxiliary inductor design, one CUT (ac capacitor) is boosted 1.16 times the ripple voltage and current. According to (10), the inductance of the auxiliary inductor in this branch is calculated to be 5.5 mH, and the rated current should be greater than 35 A.

For the bypass capacitor and parallel resistor design, the individual dc voltage for one CUT (dc capacitor) is set to 2000 V. Therefore, according to (13) and (14), the bypass capacitance in this branch is calculated to be 1.29 mF and, and the rated dc voltage should be greater than 1000 V. The parallel resistance for bypass capacitor is set to 200 k $\Omega$ , whereas parallel resistance for CUTs in this branch is set to 400 k $\Omega$ .

For the power supply size, according to (15), the rated voltage and current of the LV power supply should be greater than 750 V, 6.8 A (50 Hz) and 10.3 A (60 Hz), respectively. According to (16), the voltage of the high-voltage power supply should be greater than 3375 V, and the rated current should be less than 100 mA (when the stack resistance value is 20 k $\Omega$ ).

Therefore, the main component parameters are given in Table III. The auxiliary inductors and bypass capacitors are utilized to configure individual electrical stresses in different branches. The following testing results illustrate the functions of “concurrent ac and dc capacitor testing,” “individual ac ripple voltage and current,” “individual dc voltage,” and “different ripple frequency” in the proposed testing method, respectively.

### B. Concurrent Testing of DC and AC Capacitors

The experimental waveforms for concurrently testing dc and ac capacitors are shown in Fig. 9. It shows the three-phase ripple

voltage and the three-phase ripple current of the dc capacitors and the ac capacitors, and the dc voltage component of the dc capacitors. In this test case, the CUTs are seven  $\Delta$ -connection ac capacitors and six Y-connection dc capacitors in parallel, and the same ripple current is applied to the ac capacitors and the dc capacitors. The results show that the ripple voltage and ripple current of the CUTs are stable when ac and dc capacitors are concurrently tested.

### C. Individual Ripple Voltage and Ripple Current Stresses Testing

The experimental waveforms for individual voltage ripple and current ripple stress testing in different branches are shown in Fig. 10. In this test, the CUTs are nine  $\Delta$ -connection ac capacitors in parallel, and one of the CUTs is connected in series with a 5.5 mH three-phase auxiliary inductor in this branch. The results show that the ripple voltage of a single CUT in the branch without the auxiliary inductor is 2.25 kV (peak to peak), and the ripple current is 83 A (peak to peak). The ripple voltage of a single CUT in the branch with the auxiliary inductor is 2.63 kV (peak to peak), and the ripple current is 97 A (peak to peak). It indicates that this auxiliary inductor boosts the ripple voltage and ripple current by 16% from the output of the main inductor.

### D. Individual DC Voltage Component Stresses Testing

The experimental waveforms for concurrently testing individual dc voltage stresses in different branches are shown in Fig. 11. In this case, the CUTs are six Y-connection dc capacitors in parallel, and one of the branches of three CUTs is connected in series with a 1.29 mF bypass capacitor and a 200 k $\Omega$  parallel resistor. The results indicate that the dc voltage component of

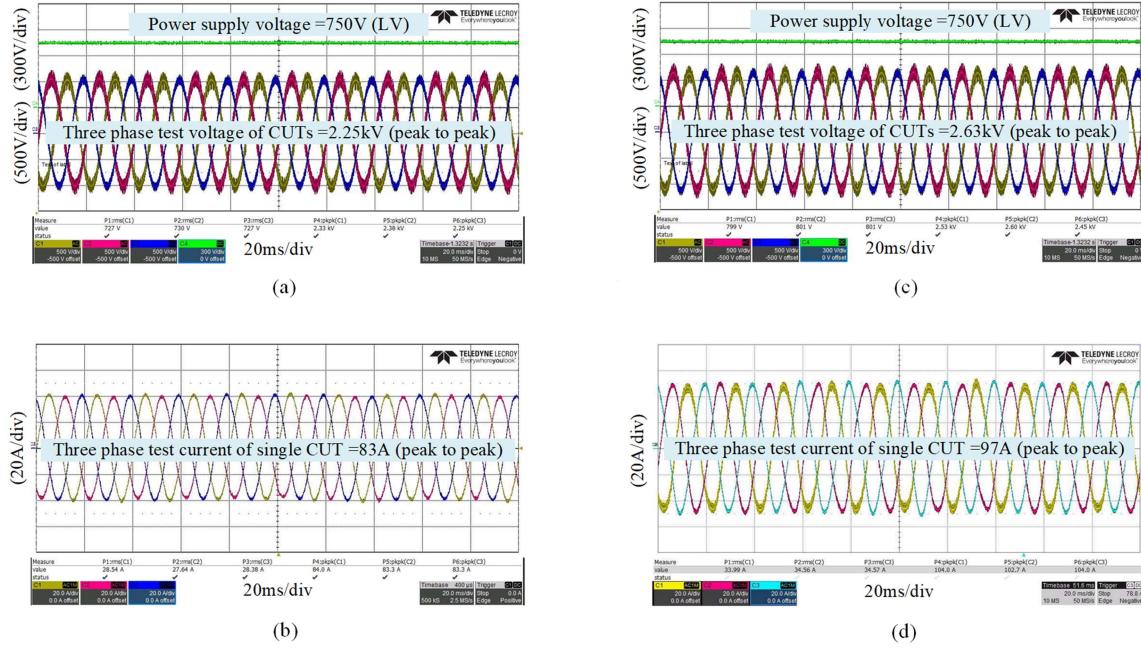


Fig. 10. Experimental results for individual ripple voltage and current testing. (a) Voltage waveform in AC capacitors testing (without the auxiliary inductor in this branch). (b) Current waveform in AC capacitors testing (without the auxiliary inductor in this branch). (c) Voltage waveform in AC capacitors testing (with the auxiliary inductor in this branch). (d) Current waveform in AC capacitors testing (with the auxiliary inductor in this branch). (Scenario 3 in Table II, 8 pcs AC capacitors without auxiliary inductors and 1 pcs DC capacitor with auxiliary inductors in parallel, ripple frequency: 50 Hz).

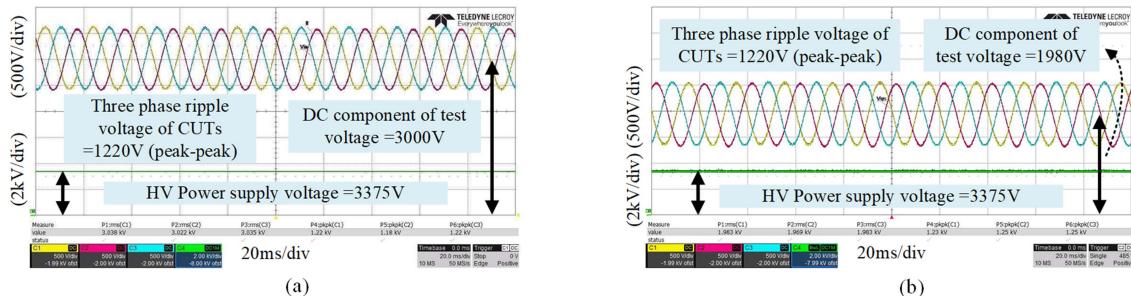


Fig. 11. Experimental results for individual DC voltage component testing. (a) Voltage waveform in DC capacitors testing (without the bypass capacitor in this branch). (b) Voltage waveform in AC capacitors testing (with the bypass capacitor in this branch). (Scenario 5 in Table II, 6 pcs DC capacitors without bypass capacitors and 6 pcs DC capacitors with bypass capacitors in parallel, ripple frequency: 50 Hz).

three CUTs without the bypass capacitor branch is 3.0 kV. The dc component voltage of three CUTs with the bypass capacitor branch is 1.98 kV, which shows that this bypass capacitor divides 34% of the dc voltage component.

#### E. Different Ripple Frequencies Testing

The experimental waveforms for different ripple frequencies are shown in Fig. 12. The voltage acceleration factor of 1.4 for rated ripple voltage (730 V) is applied to the CUTs with 50–360 Hz ripple frequency. When the multiple ripple frequencies are applied, the ripple voltage of the CUTs is stable and under control. If the switching frequency is applied to CUTs, it can be achieved by reducing the inductance of the main inductor according to the calculation of (10) and (11).

#### F. AC and DC Capacitor Gradient Testing

The experimental waveforms for ac and dc capacitor gradient testing are shown in Fig. 13. In the ac capacitor testing, three testing modes are configured to simulate the gradient rise of the ripple current. In mode 1, the given ripple current is 270 A (rate current: 30 A and nine CUTs in parallel). In mode 2, the given ripple current is 324 A (acceleration factor: 1.2). In mode 3, the given ripple current is 378 A (acceleration factor: 1.4). It is possible to emulate the gradient ripple current of the ac capacitor. Due to the closed-loop control system, the actual ripple current gradually increases with the given current until it reaches the given one.

In the dc capacitor testing, three testing modes are configured to simulate the gradient rise of the dc voltage. In mode 1, the

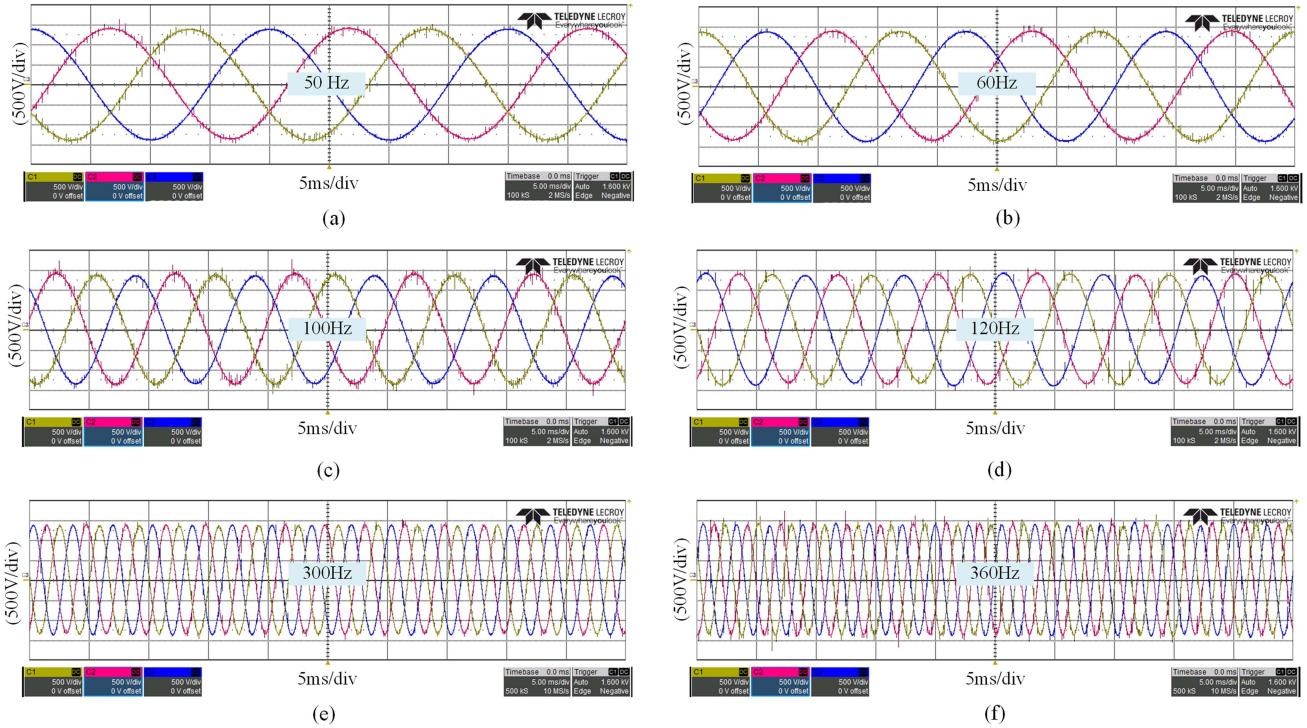


Fig. 12. Experimental results for different ripple frequency testing. (a) Voltage waveform with 50 Hz ripple frequency. (b) Voltage waveform with 60 Hz ripple frequency. (c) Voltage waveform with 100 Hz ripple frequency. (d) Voltage waveform with 120 Hz ripple frequency. (e) Voltage waveform with 300 Hz ripple frequency. (f) Voltage waveform with 360 Hz ripple frequency. (Ripple frequencies: 50, 60, 100, 120, 300, and 360 Hz).

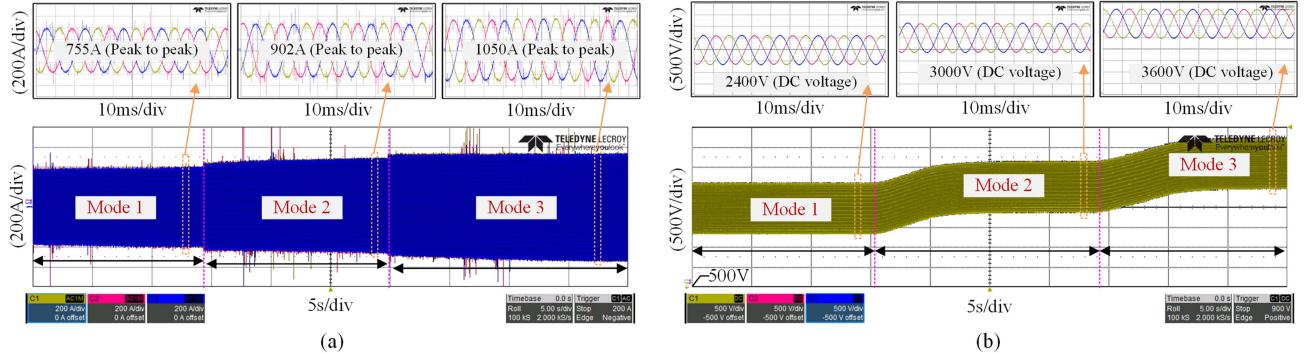


Fig. 13. Experimental results for AC and DC capacitor gradient testing. (a) Current waveform in AC capacitor gradient testing (Mode 1: 270 A ripple current; Mode 2: 324 A ripple current; Mode 3: 378 A ripple current). (b) Voltage waveform in DC capacitor gradient testing (Mode 1: 2400 V DC voltage; Mode 2: 3000 V DC voltage; Mode 3: 3600 V DC voltage; ripple frequency: 50 Hz).

given dc voltage is 2400 V (acceleration factor: 0.8). In mode 2, the given dc voltage is 3000 V (rated voltage: 3000 V). In mode 3, the given dc voltage is 3600 V (acceleration factor: 1.2). Meanwhile, in three modes, the ripple voltage is maintained at 1200 V. The stress emulation of the gradient dc voltage of the dc capacitor can be realized. The stack resistors  $R_{H1}$  and  $R_{H2}$ , and CUTs form the charging loop. When the given dc voltage increases, the test voltage increases accordingly based on the  $RC$  charging. When the CUTs are fully charged, they maintain the given dc voltage.

#### G. Three-Phase Capacitance Mismatch Testing

The experimental waveforms for dc capacitor testing with three-phase mismatch are shown in Fig. 14. In this case, the CUTs of one phase are disconnected to simulate the aging and failure of the CUTs in the dc capacitor testing. The capacitance of one-phase CUTs is reduced from 480 to 440  $\mu$ F. The capacitance of other two-phase CUTs keeps 480  $\mu$ F. When the capacitance of the CUTs mismatches, the ripple voltage and ripple current of the CUTs and the output current of the power supplies remain stable. Three-phase ripple voltage of CUTs keeps 500 V.

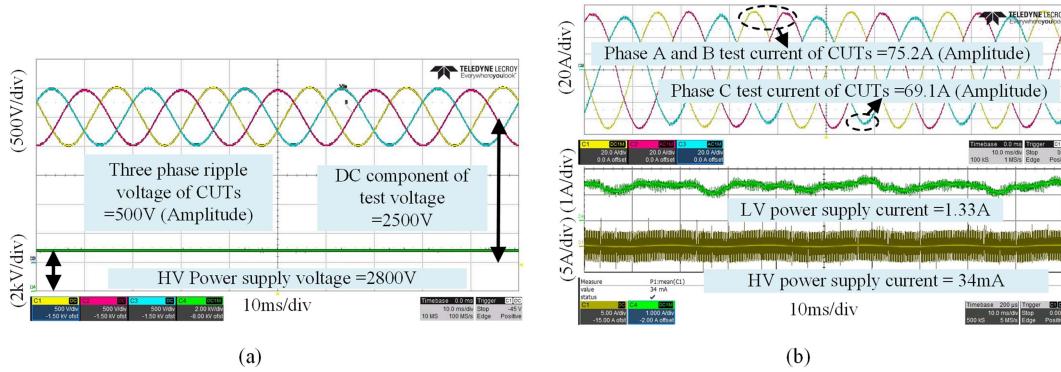


Fig. 14. Experimental results for DC capacitor testing with the three-phase mismatch of CUTs (one-phase capacitance is reduced from 480 to 440  $\mu\text{F}$ ). (a) Voltage waveform in DC capacitor testing (three-phase mismatch of CUTs). (b) Current waveform in DC capacitor testing (three-phase mismatch of CUTs).

TABLE V  
EXAMPLES OF TYPICAL ENGINEERING TESTING SCENARIOS FOR DIFFERENT POWER ELECTRONICS APPLICATIONS

Testing requirement (RMS value)						Required design parameters (RMS value)						
CUTs	Application	CUTs parameter ( $C_{\text{test}}/f_R/I_{\text{ripple}}$ or $U_{\text{ripple}}/U_{\text{rate},DC}$ )	Test Number	Acceleration factor for rated ripple voltage/current	Acceleration factor for rated DC voltage	Power stack output current	AC inductor inductance	AC inductor current	Bypass capacitor capacitance	Bypass capacitor voltage	Required power (LV)	Required voltage (HV)
AC	Wind power	75 $\mu\text{F}/50 \text{ Hz}/730 \text{ V}/\text{-}$	9	$m=1.4$	-	375 A	2.5 mF	375 A	-	-	6830 W	-
	Wind power	75 $\mu\text{F}/60 \text{ Hz}/730 \text{ V}/\text{-}$	9	$m=1.4$	-	450 A	1.7 mF	450 A	-	-	10350 W	-
	Wind power	75 $\mu\text{F}/50 \text{ Hz}/730 \text{ V}/\text{-}$	9	$m_1=1.0 (N_1=3)$ $m_2=1.2 (N_2=3)$ $m_3=1.4 (N_3=3)$	-	321 A	Main=1.35 mF Aux 1=2.5 mF Aux 2=4.3 mF	Main=321 A Sub1=107 A Sub2=125 A	-	-	5860 W	-
	Railway	416 $\mu\text{F}/50 \text{ Hz}/600 \text{ V}/\text{-}$	8	$m=1.4 (840\text{V})$	-	1523 A	0.37 mF	1523 A	-	-	27720 W	-
	Railway	416 $\mu\text{F}/50 \text{ Hz}/600 \text{ V}/\text{-}$	8	$m_1=1.0 (N_1=2)$ $m_2=1.2 (N_2=2)$ $m_3=1.4 (N_3=2)$ $m_4=1.6 (N_4=2)$	-	1410 A	Main=0.12 mF Aux 1=0.68 mF Aux 2=1.16 mF Aux 3=1.53 mF	Main=1410 A Sub1=325 A Sub2=380 A Sub3=434 A	-	-	25680 W	-
DC	Wind power	645 $\mu\text{F}/50 \text{ Hz}/40 \text{ A}/1250 \text{ V}$	24	$m=1.4$	$m_{dc}=1.0$	448 A	0.49 mF	448 A	-	-	8100 W	1625 V
	Wind power	645 $\mu\text{F}/50 \text{ Hz}/40 \text{ A}/1250 \text{ V}$	24	$m_1=1.2 (N_1=12)$ $m_2=1.4 (N_2=12)$	$m_{dc1}=1.0 (N_1=18)$ $m_{dc1}=1.4 (N_2=6)$	416 A	Main=0.49 mF Aux 1=0.57 mF	Main=416 A Sub1=192 A	9.675 mF	500 V	7500 W	2125 V
	Railway	750 $\mu\text{F}/50 \text{ Hz}/200 \text{ A}/3000 \text{ V}$	12	$m_1=1.2 (N_1=6)$ $m_2=1.4 (N_2=6)$	$m_{dc1}=1.0 (N_1=9)$ $m_{dc1}=1.4 (N_2=3)$	976 A	Main=1.62 mF Aux 1=1.93 mF	Main=976 A Sub1=560 A	5.625 mF	1200 V	17550 W	4575 V
	Electric vehicle	440 $\mu\text{F}/50 \text{ Hz}/90 \text{ A}/600 \text{ V}$	24	$m=1.4$	$m_{dc1}=1.0 (N_1=18)$ $m_{dc1}=1.4 (N_2=6)$	1008 A	0.72 mF	1008 A	6.6 mF	240 V	18150 W	1215 V
AC+DC	Wind power	75 $\mu\text{F}/50 \text{ Hz}/730 \text{ V}/\text{-}$ 645 $\mu\text{F}/50 \text{ Hz}/40 \text{ A}/1250 \text{ V}$	9 (AC) 24 (DC)	$m=1.4$	$m_{dc}=1.0$	823 A	Main=0.35 mF Aux 1=3.64 mF	Main=823 A Sub1=375 A	-	-	14850 W	1625 V
	Railway	416 $\mu\text{F}/50 \text{ Hz}/600 \text{ V}/\text{-}$ 750 $\mu\text{F}/50 \text{ Hz}/200 \text{ A}/3000 \text{ V}$	4 (AC) 6 (DC)	$m=1.4$	$m_{dc1}=1.0 (N_1=3)$ $m_{dc1}=1.4 (N_2=3)$	1321 A	Main=0.57 mF Aux 1=1.97 mF	Main=1321 A Sub1=560 A	5.625 mF	1200 V	23760 W	4575 V

1. Using Semikron's SKS SL150 power stack (Rated output current=1600 A), Elektro-automatik's EA-PSI 10000 LV power supply (Rated output power=30 kW) and Technix's SR20-40 HV power supply (Rated output voltage= 10 kV) can be applied to all the above cases, as shown in Fig. 8.

2. In the cases: efficiency  $\eta$ , 96.6%; power stack rated output voltage, 530 V; LV output voltage, 750 V.

3. The configuration of inductors and capacitors can be selected according to needs.

Two-phase ripple current of CUTs is 75.2 A and other one-phase ripple current of CUTs is 69.1 A. Therefore, the test bench can generate stable ripple current and ripple voltage for the CUTs, and maintain the same required power supply, even if the CUTs degrade and have open circuit during the testing.

#### H. Error Analysis of Design and Testing

Comparing the design calculation with the test results in Table IV, the calculated accuracy of ripple current, ripple voltage, and dc voltage of the CUTs between the design value and

the test results is more than 98.5%. The calculated accuracy of source output current between the design value and the test results exceeds 96%. Considering that there are sampling errors of voltage and current sensors, potential noise interference, and power loss by other components, the results indicate that the theoretical analysis of the proposed method is reasonable.

#### V. CONCLUSION

In this article, we propose a unified capacitor stress emulation method for high-power converter applications. The proposed

method has the unique capability to emulate different electrical stress levels, such as ripple voltage, ripple current, and dc voltage, in individual branches, allowing for concurrent testing of both ac and dc capacitors. The testing capabilities and scenarios are given in Table II, which is suitable for application-oriented testing with different stress conditions. The architecture of the circuit and the analytical models for component sizing are described in detail. Examples of typical engineering testing scenarios for different power electronics applications are given in Table V, such as wind power converters, electric vehicle inverters, and railway traction systems. Experimental results with 3.0 kV dc voltage, 3.0 kV ripple voltage, and 1.2 kA ripple current verify the feasibility of the proposed testing method for high-power converter applications. The accuracy of simulated electrical stresses is more than 98.5%, indicating that the derived analytical models of the proposed method are reasonable.

## APPENDIX EXAMPLES OF TYPICAL TESTING SCENARIOS

Examples of typical engineering testing scenarios for different power electronics applications are given in Table V.

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**Bo Yao** (Graduate Student Member, IEEE) received the B.Eng. and M.Eng. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2017 and 2020, respectively. He is currently working toward the Ph.D. degree in power electronic with Aalborg University, Aalborg, Denmark.

He is a Member of the Reliability of Power Electronic Converters (ReliaPEC) research group and X-Power test facility of Aalborg University. His research interests include reliability evaluation and condition monitoring of power electronic components in power converter systems.

Mr. Yao was the recipient of the Best Paper Award of International Conference on Electrical Machines and Systems in 2019 and the SEMIKRON Young Engineer Award in 2023.



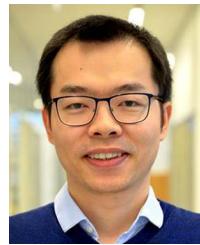
**Haoran Wang** (Member, IEEE) received the B.S. and M.S. degrees in control science and engineering from the Wuhan University of Technology, Wuhan, China, in 2012 and 2015, respectively, and the Ph.D. degree in energy technology from the Center of Reliable Power Electronics, Aalborg University, Aalborg, Denmark, in 2018.

From 2013 to 2014, he was a Research Assistant with the Department of Electrical Engineering, Tsinghua University, Beijing, China. He was a Visiting Scientist with ETH Zurich, Zurich, Switzerland, from 2017 to 2018, and with Kiel University, Kiel, Germany, in 2019. From 2019 to 2021, he was an Assistant Professor with Aalborg University, and Visiting Scientist in Vestas and Danfoss, Denmark. He is currently the Vice General Manager with Three Gorges Intelligent Industrial Control Technology Corporation, Ltd., Wuhan, China. His research interests include reliability of electrical and electronic components and systems, multiobjective life-cycle performance optimization of power electronic systems, and reliable clean energy control systems.



**Qian Wang** (Member, IEEE) was born in Hubei Province, China, in 1990. She received the bachelor's degree in electrical engineering from the Wuhan University of Technology, Wuhan, China, in 2012, the master's degree in high-voltage engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2015, and the Ph.D. degree in high-voltage engineering from Energy Department, Aalborg University, Aalborg, Denmark, in 2018.

From 2019 to 2021, she was an Assistant Professor with Energy Department, Aalborg University. She is currently an Assistant Professor with the School of Automation, Wuhan University of Technology. Her research interests include insulation design, thermal management, and internal short circuit detection of lithium-ion batteries.



**Huai Wang** (Senior Member, IEEE) received the B.E. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2007, and the Ph.D. degree in power electronics from the City University of Hong Kong, Hong Kong, in 2012.

He is currently a Professor with AAU Energy, Aalborg University, Aalborg, Denmark, where he leads the Group of Reliability of Power Electronic Converters and the mission on digital transformation and AI. He was a Visiting Scientist with ETH Zurich, Zurich, Switzerland, from August to September 2014, and with the Massachusetts Institute of Technology, Cambridge, MA, USA, from September to November 2013. He was with ABB Corporate Research Center, Baden, Switzerland, in 2009. His research interests include the fundamental challenges in modeling and validation of power electronic component failure mechanisms and application issues in system-level predictability, condition monitoring, circuit architecture, and robustness design.

Dr. Wang was the recipient of the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society in 2016 and First Prize Paper Award from IEEE Transactions on Power Electronics, in 2021. He is an Associate Editor for the *Journal of Emerging and Selected Topics in Power Electronics* and IEEE TRANSACTIONS ON POWER ELECTRONICS.