Condition Monitoring for Capacitors in Modular Multilevel Converter based on High-frequency Transient Analysis

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***Abstract*—Condition monitoring (CM) methods applied for power electronics can provide effective information for predictive maintenance and prevent unexpected system downtime. This paper proposes a non-invasive and in-situ CM method for capacitors in modular multilevel converters. Unlike the conventional methods that monitor low-frequency signals, the proposed method focuses on high-frequency transient analysis. By analyzing the transient voltage at the capacitor's charging moment with wavelet decomposition, the proposed method can estimate the capacitor's equivalent series resistance in situ. Moreover, the proposed method based on high-frequency transients is decoupled from system operating states, while the conventional low-frequency signals are often affected by operations (e.g., loads, environments, etc.). Finally, the effectiveness of the proposed method has been validated in a 14-kW case study by simulation.**

Keywords—condition monitoring, modular multilevel converter (MMC), capacitor, equivalent series resistance (ESR)

I. INTRODUCTION

Modular multilevel converters (MMCs) are widely applied in high voltage direct current transmissions for its superior performance in output voltage harmonics, modularity [1], etc. However, the large ripple current in the MMC brings great challenge to capacitor's reliability [2]. Failure of a capacitor might result in the malfunctions of the whole system. Solutions such as redundancy [3] and excessive design margins [4] may improve the reliability of the MMC. Nonetheless, the aforementioned methods are still limited to prevent unexpected system downtime due to device degradation.

Condition monitoring (CM), which reflects the real-time health status of capacitors, can provide effective information for predictive maintenance and prevent unexpected system downtime. Thus, many CM methods have been proposed for capacitors in MMC systems recently, which can be summarized into three aspects as follows.

The first aspect often utilizes external hardware or injecting specific signals to obtain the in-situ capacitance [4-9]. By measuring the terminal voltage and charging current of capacitors, the estimated capacitance can reflect the components' health status [4-5]. However, the additional sensors will bring extensive costs in particular of considering the large number of capacitors in the MMC. Injecting signals at a specific frequency is an another solutions to obtain the health status of capacitors [6-9]. However, the response of degradation at the specific injection frequency is often not obvious and suffers from significant noises. Moreover, the additional power losses caused by the injected signal cannot be ignored in the long run. Therefore, the aforementioned methods perform well in obtaining health status in situ, but are invasive to the system somehow. Considering the large amount capacitors in the MMC, the invasive CM is challenging to be applied in practice.

Second, some non-invasive methods have been proposed for the MMC based on special operating conditions. For instance, ref. [10] utilizes the redundancy of the MMC to bypass and re-insert submodule (SM) periodically. The charging and discharging transients of capacitors are used to estimate the health status. Similarly, ref. [11] utilizes the charging and discharging transients in the start-up period to estimate the capacitance. Although both of these methods are non-invasive, the special operating conditions (e.g., redundant SM bypassing, start-up, etc.) have extremely low frequency in the operation of the MMC. As a result, those methods fail to obtain the in-situ health status of the MMC.

Finally, some studies focus on developing a non-invasive, in-situ condition monitoring strategy for the capacitors of the MMC. For example, ref. [12] samples the capacitor voltage and estimates the capacitance based on model reference adaptive control. Ref. [13] evaluates the capacitance using four instantaneous value of capacitor voltage with specific phase information. All the aforementioned investigations use the low-frequency capacitance to characterize the health status of the capacitors in ideal conditions. However, the low frequency information is easily affected by the system operation conditions (e.g., loads, environments, etc.). In a practical operating MMC system, the power fluctuation influences the capacitor voltage and current, which might affect the accuracy of the estimated capacitance. Therefore, the non-invasive and in-situ CM methods of MMC's capacitors still need further investigations.

This paper proposes a non-invasive and in-situ CM method for capacitors in MMC systems. Unlike the conventional methods that monitor low-frequency signals, the proposed method focuses on high-frequency transient analysis. By analyzing the transient voltage at the capacitor's charging moment with wavelet decomposition, the proposed method can estimate the capacitor's equivalent series resistance (*ESR*) in situ. The novelty of this paper holds on three parts: 1) the proposed method based on high-frequency transients is decoupled from system operating states, while the conventional low-frequency signals are often affected by operations (e.g., loads, environments, etc.); 2) the monitor of the *ESR* has higher sensitivity to represent the end-of-life (EOL) of capacitors (i.e., 20% capacitance reduce or 200%

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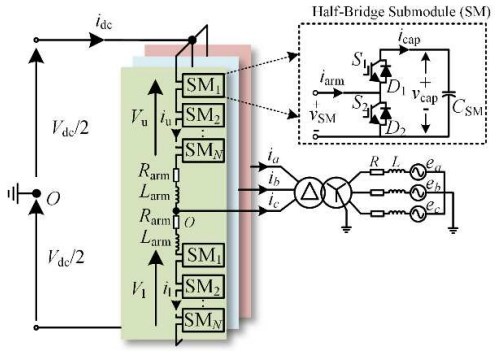


Fig. 1. Circuit configuration of a typical three-phase MMC.

ESR increase at capacitors EOL [14]); and 3) the proposed wavelet decomposition can analyze the aperiodic charging and discharging moment of capacitors in MMCs.

The outline of this paper is summarized as follows. Section II briefly introduces the circuit configuration of the MMC system. The influence of *ESR* on the terminal voltage of the capacitor is also investigated. Section III studies the transient response of the capacitor at the charging moment. The wavelet analysis is introduced to extract the transient voltage. Section IV proposes the condition monitoring method based on the wavelet analysis. A 14-kW MMC simulation case study is established to prove the effectiveness of the proposed method. Conclusions are drawn at last.

II. Capacitor's Status in MMC and *ESR*'s Influence

Capacitors are considered as an ideal one during the charging process in existing studies [15]. However, the voltage on the *ESR* in a degraded capacitor cannot be ignored. In this section, the status of capacitors in MMC is analyzed. Based on an MMC simulation, the influence of the *ESR* on the capacitor voltage is discussed. The increased *ESR* in a degraded capacitor brings a voltage step to the capacitor voltage, which can be used to indicate its health status.

A. Capacitor's Status in MMC

The topology of a typical three-phase MMC system is shown in Fig. 1. The MMC consists of six arms and each arm consists of N SMs, an arm resistor R_{arm}, and an arm inductor L_{arm}. For each SM, a half-bridge topology is usually adopted, which consisting of two IGBTs and two diodes (S_1, D_1, S_2 and D_2) and a capacitor bank (C_{SM}). V_{dc} represents the dc side voltage and v_{SM} represents the output voltage of the SM. i_{arm} is the arm current and i_{cap} is the charging current of the capacitor. v_{cap} is the voltage of the capacitor. V_u is the upper arm voltage and V_l is the lower arm voltage.

Fig. 2 shows status of the capacitor in SM's different operation modes. The capacitor is charged in SM's inserted mode or blocked mode with a positive arm current. The blocked mode is often used for pre-charging capacitors in start-up period, which is not considered in following analysis.

B. Influence of ESR on Capacitor's Terminal Voltage

A capacitor consists of an ideal capacitor C, an equivalent series resistor *ESR* and an equivalent series inductor *ESL*, which is shown in Fig. 3. *ESL* is typically on the order of nH, which is small enough to be ignored in the following analysis. The terminal voltage of the capacitor consists of the voltage of the ideal capacitor C and the *ESR*, which is expressed in (1). The voltage on the *ESR* is small enough to be neglected in a healthy capacitor. However, in an aged capacitor, the voltage on the *ESR* increases, which makes a difference on the capacitor's output voltage.

$$v(t) = v_C(t) + v_{ESR}(t) \tag{1}$$

Fig.4 (a) and (b) show the terminal voltage of the capacitor with and without the *ESR*. The zoomed boxes show the transient response at the charging moment, respectively. Compared to the smoothly charging process of the capacitor without *ESR*, a voltage step occurs at the charging moment of the capacitor with *ESR*. Thus, the increased *ESR* in an aged capacitor brings a voltage step at the charging moment, which can indicate its health status.

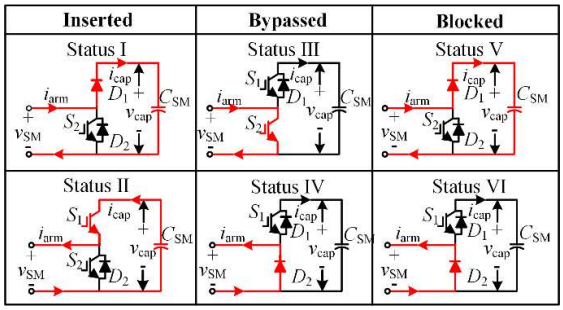


Fig. 2. Operation modes of capacitors in MMC

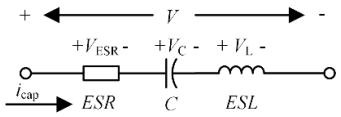
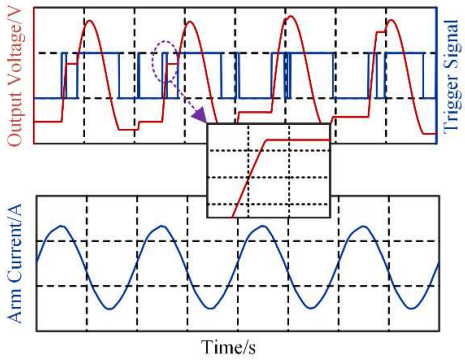
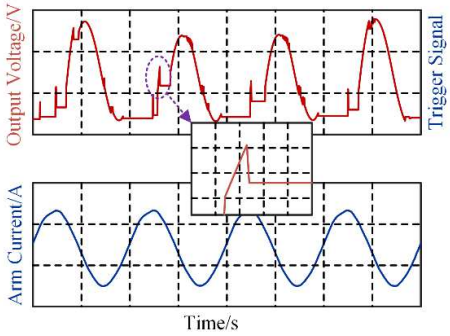


Fig. 3. Equivalent circuit model of capacitors



(a)



(b)

Fig. 4. Influence of the *ESR* on the capacitor's output voltage. (a) without *ESR*. (b) with *ESR*

III. Transient Analysis of Capacitor's Terminal Voltage and *ESR* Estimation With Wavelet Analysis

According to section II, the voltage step at the capacitor charging moment is correlated with the *ESR*. Analyzing the transient voltage step is necessary to estimate the *ESR*. However, the aperiodic charging moment makes it difficult to analyze it with traditional signal processing methods. In this section, the relationship between the *ESR* and the voltage step is established by the high-frequency transient analysis at the charging moment. The wavelet analysis is then introduced to extract the transient information at the charging moment.

A. Transient Analysis of Capacitor's Charging process

The charging process is simplified in Fig. 5. The dashed green curve represents the terminal voltage of the healthy capacitor, while the solid red curve represents the terminal voltage of the degraded one. The arm current is assumed to be positive. The capacitor is charged at t_0 when the SM is inserted, the terminal voltage maintains at t_1 when the SM is bypassed. The transient voltage of the capacitor at t_0 and t_1 are analyzed in the following part.

Considering the long degradation period of the capacitor, the analysis is carried out with the following two assumptions:

1) The capacitor is charged with the same initial voltage.
2) The arm current at the charging moment is same.

When the SM is inserted at t_0, the capacitor is charged via D_1. The charging circuit is then simplified as Fig. 6. Assume that the capacitor is charged at t_0, then the charging current at t_0 can be expressed as

$$i_{cap}(t) = i_{arm}(t) \cdot \theta(t - t_0), \tag{2}$$

where $i_{arm}(t)$ represents the arm current, $\theta(t-t_0)$ represents the step signal at the charging moment, which equals 0 at t_{0-} and equals 1 at t_{0+}.

As the output of a capacitor cannot change suddenly, the capacitor's voltage and the charging current at t_0 are expressed as

$$\begin{cases} v_C(t_{0-}) = v_C(t_{0+}) \\ i_{cap}(t_{0+}) = i_{arm}(t_0) \end{cases} \tag{3}$$

After the SM is inserted, the output voltage of the capacitor includes $v_C(t)$ and $v_{ESR}(t)$, which is expressed as

$$v(t_{0+}) = v_C(t_{0+}) + v_{ESR}(t_{0+}) = v_C(t_{0+}) + i_{cap}(t_{0+}) \cdot ESR \tag{4}$$

The output voltage of the capacitor at t_{0+} is derived by substituting (3) to (4), which is expressed as

$$v(t_{0+}) = v_C(t_{0-}) + i_{arm}(t_0) \cdot ESR, \tag{5}$$

when the SM is bypassed, the simplified circuit of the capacitor's bypassing progress is shown in Fig. 7. Assume that the capacitor is bypassed at t_1, similar to the analysis at t_0, the capacitor's voltage and the charging current at t_1 are expressed as

$$\begin{cases} i_{cap}(t_{1+}) = 0 \\ v_C(t_{1+}) = v_C(t_{1-}) \end{cases} \tag{6}$$

After the capacitor is bypassed, the terminal voltage of the capacitor is expressed as

$$v(t_{1+}) = v_C(t_{1+}) + v_{ESR}(t_{1+}) = v_C(t_{1+}) + i_{cap}(t_{1+}) \cdot ESR \tag{7}$$

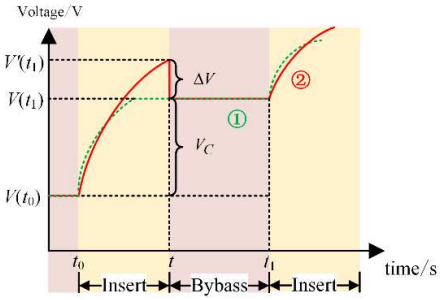


Fig. 5. Simplified charging progress of the capacitor

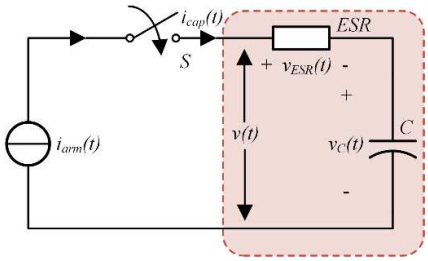


Fig. 6. Simplified circuit of the capacitor's charging transient

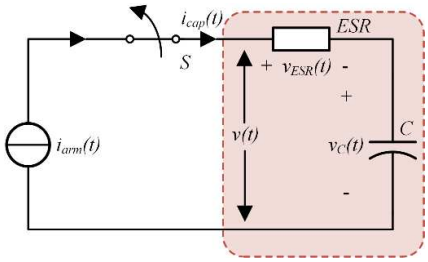


Fig. 7. Simplified circuit of the capacitor's bypassing transient

Thus, the capacitor's voltage at t_{0+} is derived by substituting (6) to (7), which is expressed as

$$v(t_{1+}) = v_C(t_{1-}) \tag{8}$$

The inserted time for an SM is usually short enough to be ignored. Therefore, the output voltage of the capacitor at t_{0+} equals the voltage at t_{1-}, which is expressed as

$$v(t_{0+}) = v(t_{1-}) = v(t_{1+}) \tag{9}$$

Therefore, for a healthy capacitor (*ESR*=0), the terminal voltage at the bypassed time t_1 can be expressed as

$$v(t_{1-}) = v_C(t_{0-}) \tag{10}$$

For a capacitor with increased *ESR*, the voltage is

$$v'(t_{1-}) = v_C(t_{0-}) + i_{arm}(t_0) \cdot ESR \tag{11}$$

Thus, the voltage step at the charging moment of the capacitor is

$$\Delta V = v'(t_{1-}) - v(t_{1-}) = i_{arm}(t_0) \cdot ESR \tag{12}$$

Accordingly, the *ESR* can be estimated with the charging current if the voltage step at the capacitor's charging moment is acquired. However, the inserting moment of the SM is aperiodic, which results in difficulty analyzing the transient response in the time domain or extracting frequency domain information with the traditional Fourier analysis. To extract

the high-frequency voltage step, an effective signal processing method is needed.

B. ESR Estimation based on Wavelet Analysis

The wavelet analysis is one of the multi-scale analysis methods, especially in feature extraction of transient information. It decomposes the original signal into different time scales. As a result, the high-frequency information of the origin signal in different frequency interval are acquired, which is represented as detailed coefficient cD_n, where n is the decomposition layer. An approximated coefficient cA_n is also obtained to show the trend of the original signal. Fig. 9 shows the multi-scale analysis of a three-layer decomposition. The relationship of the original signal s and the decomposition results is shown as

$$s = cA_3 + cD_1 + cD_2 + cD_3. \tag{13}$$

With the advantage of precisely multi-scale analysis, wavelet analysis performs well in analyzing a transient signal at a specific time. As the signals studied in this paper are discretely, the discrete wavelet transform is used to analyze the terminal voltage of an aged capacitor at the charging moment. For simplicity, *haar* wave function is used in this paper. The discrete wavelet transform of $v(t)$ is defined as (14) when the decomposition layer is 1.

$$\begin{cases} cA_1[\alpha,\tau] = \dfrac{1}{\sqrt{2}}\sum_n v(n)\phi_{\alpha,\tau}(n) \\ cD_1[\alpha,\tau] = \dfrac{1}{\sqrt{2}}\sum_n v(n)\psi_{\alpha,\tau}(n) \end{cases} \tag{14}$$

where the $v(n)$ is the output voltage of the aged capacitor, and $\phi_{\alpha,\tau}(n)$ and $\psi_{\alpha,\tau}(n)$ is the *haar* wavelet function, which is expressed in (15). α represents the scaling factor and τ represents the translation factor.

$$\begin{aligned} &\phi[n] = [1,1]; \\ &\psi[n] = [1,-1]. \end{aligned} \tag{15}$$

The acquired discrete voltage $v(L)$ is expressed as

$$v(L) = (v_1, v_2, ..., v_L) \tag{16}$$

where L is a positive even integer that refers to the length of v. The *haar* transform decomposes the discrete signal into two coefficients of half its length.

The approximated $cA_1(L/2)$ and the detailed coefficient $cD_1(L/2)$ are calculated as

$$\begin{cases} cA_1(m) = \dfrac{v(2m-1)+v(2m)}{\sqrt{2}} \\ cD_1(m) = \dfrac{v(2m-1)-v(2m)}{\sqrt{2}} \end{cases}, (m = 0,1,...,L/2), \tag{17}$$

$cD_1(L/2)$ is related to the difference between two sample points. Hence, the detailed coefficient $cD_1(t_0)$ at the inserting moment t_0 is exactly decided by the voltage step ΔV, which is expressed as

$$cD_1(t_0) = \frac{\Delta V(t_0)}{\sqrt{2}} \tag{18}$$

Combined with (12), the *ESR* is then be estimated as

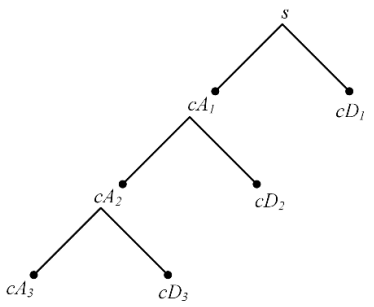


Fig. 9. The multi-scale analysis of a three-layer decomposition

$$ESR = \frac{\sqrt{2}\cdot cD_1(t_0)}{i_{arm}(t_0)} \tag{19}$$

Accordingly, when the voltage step at the charging moment is decomposed by wavelet analysis, the *ESR* can be evaluated by the wavelet coefficient and the arm current. Compared to the traditional capacitance-based methods, the proposed method estimates the *ESR* with the high frequency transient information, which holds a higher sensibility.

IV. Proposed Condition Monitoring Method and Simulation Validation

A. Proposed Condition Monitoring Method

The voltage step at SM's inserting moment, related to the arm current, is utilized to estimate the *ESR*. According to (12), a larger voltage step is generated by larger arm current, which is easier to be sampled. The condition monitoring interval is thus set when the arm current reaches its maximum value.

The flowchart of the proposed condition monitoring process is given in Fig. 10. When the condition monitoring begins, the capacitor voltage and the arm current are sampled by existing sensors in MMC. The capacitor voltage is then decomposed by wavelet analysis. The minimum value of the wavelet coefficient and the maximum value of the arm current is calculated. *ESR* is finally calculated by (19), when the current *ESR* reaches the failure point, the capacitor is regarded as failed.

B. Simulation Validation

To validate the feasibility of the proposed method, simulations are designed in a 14-kW simulation case study. The detailed parameters are listed in Table I. Due to the demand of high capacitance density, aluminum electrolytic capacitors are usually adopted in some low-voltage MMC [16]. Take TDK's B41793A9108Q001 as an example, the *ESR* of it in health status is 0.044Ω. Therefore, the capacitor is connected with 0.06Ω, 0.08Ω and 0.1Ω resistors to simulate the degradation. Fig. 11 shows the output voltage, arm current and the calculated coefficient. The voltage step at the inserting moment varies with different *ESR*. The calculated coefficient reaches its maximum value during the sampling interval, which is shown in the dashed box in Fig. 11. To show the efficiency of the proposed method, one of the wavelet simulation results at the inserting moment is zoomed-in Fig.12. Simulation results show that the calculated detailed coefficient increases with the increase of *ESR*, which verifies the above analysis. The *ESR* estimation results and the error are shown in Table. II. The maximum error of the

estimation error is 6.8% which is relatively low to the 200% increment at the failure point.

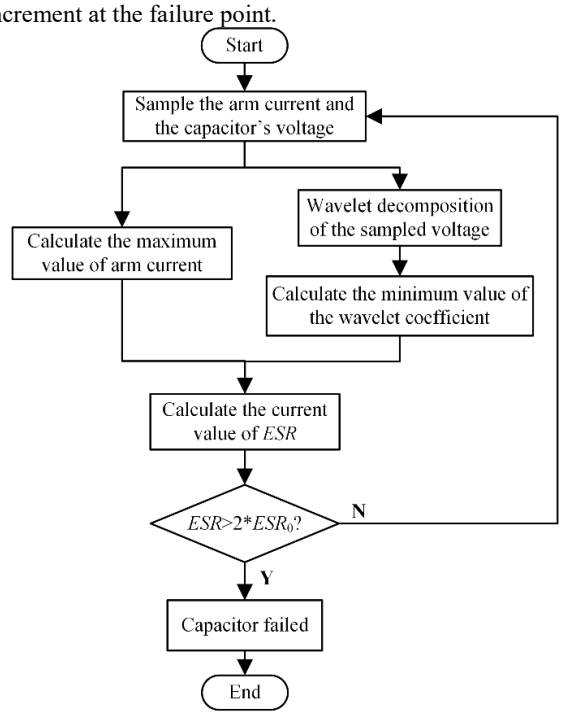


Fig. 10. Flowchart of the proposed condition monitoring method

TABLE I. PARAMETERS OF A 12-MW SIMULATION

Parameters	Values and Units
Nominal apparent power S_N	5 kVA
Nominal active power P_N	4.5 kW
Phase Voltage *Vo*	300V
Number of SMs per arm *N*	5
Arm inductance L_{arm}	1 mH
SM capacitance C_{SM}	1 mF

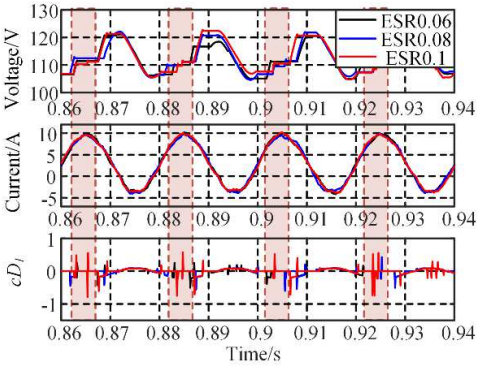


Fig.11. Simulation result of wavelet analysis for capacitors with different *ESR*

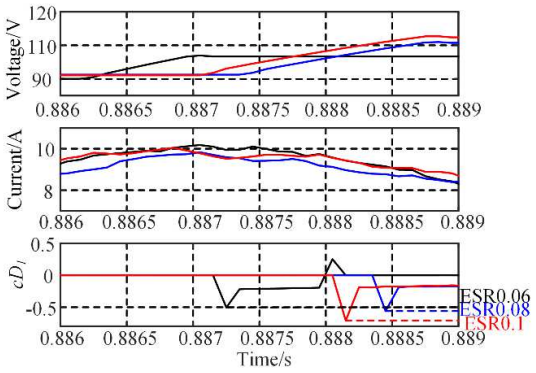


Fig. 12. Zoomed view of the wavelet simulation result at inserting moment

TABLE II. ESTIMATION RESULT AND ERROR OF ESR

ESR/Ω	Estimated value/Ω	Error
0.06	0.0624	4%
0.08	0.0846	5.7%
0.1	0.1068	6.8%

V. CONCLUSION

A non-invasive and in-situ condition monitoring method has been proposed in this paper to estimate the *ESR* of capacitors in the MMC. The influence of *ESR* on the capacitor's terminal voltage at the charging moment is studied. By high frequency transient analysis of the capacitor voltage, the *ESR* is estimated based on wavelet analysis. Compared to the traditional capacitance-based monitoring methods, the proposed strategy holds higher sensibility for using *ESR* as an indicator. Moreover, the *ESR* is estimated by analyzing high frequency transient information in this paper, which makes it independent of the system level and power fluctuation. The outcomes provide a guideline for using capacitor's high frequency information to indicate its health status. However, the results of wavelet decomposition are vulnerable to the noises and sampling frequency in the system. Future investigations need to be done to overcome the challenges.

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