

# Letter

## A Robust Testing Method for DC and AC Capacitors With Minimum Required Power Supply

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**Abstract**—This letter proposes a testing method to emulate realistic stress conditions of dc and ac capacitors, with minimum required power supply and robust operation at the presence of capacitor degradation. It is especially suitable for parameter characterization and accelerated degradation testing of high-voltage and high-ripple current power electronic capacitors. The circuit architecture of the proposed testing method and the constraints of the testing samples under given designs are discussed. Proof-of-concept experiments on both dc and ac capacitors verify the feasibility.

**Index Terms**—AC capacitor, dc capacitor, degradation testing, power electronics.

### I. INTRODUCTION

HERE are two emerging demands for capacitor testing in power electronics applications. The first is parameter characterizations under realistic operating points beyond what are provided in supplier datasheets [1]. The testing results could help build better capacitor parametric models to optimize design margins in power converters. The second is application-oriented accelerated degradation testing under realistic voltage and current stresses [2].

Existing methods emulating realistic high-power capacitor electrical stress have at least one of the two issues.

1) The power supply and power processing circuit requirements make them not viable solutions for capacitors in tens of kilowatt to multi-megawatt power electronics applications. For example, the Type I [3], [4], [5] and Type II [6], [7] solutions are shown in Table I. The stacked methods need to attain dc offset for testing with ac ripple voltage and current. The current sources in the circuits need to process the full voltage and current, implying a considerable power loss as well. In Type II, the commercial ripple current testers emulate up to 500 V dc voltage, 30 V ripple voltage, and 30 A ripple current for dc capacitor [7].

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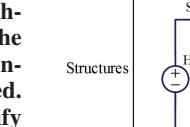
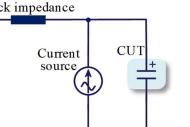
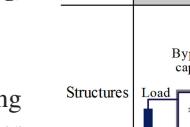
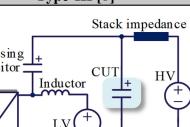
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TABLE I  
COMPARISONS OF THE TYPICAL TEST METHODS

	Type I [3] [4] [5]	Type II [6] [7]
Structures		
Source	Required power supply: + + + +	Required power supply: + + +
	Type III [8]	Type IV [9]
Structures		
Source	Required power supply: + +	Required power supply: + +
Issue	Unbalance current flow into high voltage source when the capacitance mismatch of CUTs	

2) It is lack of robustness to capacitance mismatch between testing samples due to degradation or tolerance. Type III [8] and Type IV [9] solutions shown in Table I reduce the power supply requirement and power loss of the testing system. Nevertheless, low-frequency ripple current component would flow into the HV source at the presence of capacitance mismatch among capacitors under testing (CUT). The mismatch could be caused by initial capacitance tolerance, different degradation rate, and open-circuit fault. It would raise the capacity requirement of the HV source in practical implementation.

This letter focuses on proposing a method for application-oriented capacitor characterizations (i.e., measuring capacitor parameters) and degradation testing by emulating more realistic voltage and current stresses and overcome the previous two issues. The contributions of the presented study areas are as follows.

- Compared with the existing methods, the method can provide the testing conditions of high-power electrical stress with the minimum requirements on power supply.
- The method can control the testing conditions in a robust way at the presence of capacitance mismatch during the testing.

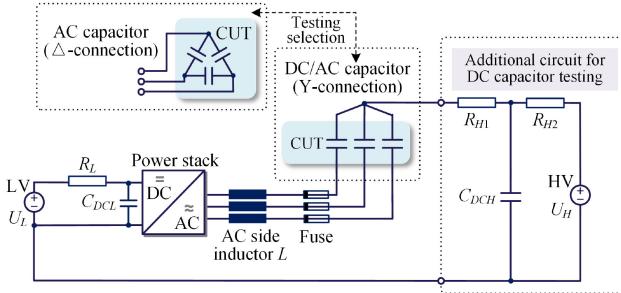


Fig. 1. Circuit architecture of the proposed capacitor testing method (for ac capacitor testing, HV source  $U_H$ , filter capacitor  $C_{DCH}$ , resistors  $R_{H1}$ , and  $R_{H2}$  can be excluded).

- 3) The testing capability in terms of dc voltage, ripple current, and ripple voltage ranges of the CUTs are analytically derived.

## II. PROPOSED CAPACITOR TEST METHOD

### A. Circuit Architecture and Control Structure

The circuit architecture of the proposed testing method is shown in Fig. 1. The low-voltage (LV) power supply  $U_L$  and the power stack are used to generate ac ripple voltage or current. The high-voltage (HV) power supply  $U_H$  is used to generate the dc bias voltage, which is only needed for dc capacitor testing. The ac-side inductors  $L$  are used for both filtering the harmonics and boosting the ac-side output voltage. The CUTs can be configured into Y- or  $\Delta$ -connection for ac capacitors, and Y-connection for dc capacitors, with single or multiple such connections in parallel. Therefore, the maximum CUTs ripple voltage is limited by  $U_L$ ,  $L$ , and the modulation of the power stack inverter. The maximum CUTs dc voltage is limited by  $U_H$ . The maximum CUTs ripple current is limited by the current rating of the power stack and the power rating of the LV power supply. The LV power supply compensates the power losses of the testing system, mainly from the power stack, ac inductors, and CUTs. In addition, the filter capacitors  $C_{DCL}$  and  $C_{DCH}$  are configured on both sides of the LV and HV power supplies. The startup resistor  $R_L$  is added to prevent overcurrent of the LV power supply during startup. The current-limiting resistors  $R_{H1}$  and  $R_{H2}$  are added to limit the current of the HV power supply.

The control of the proposed testing method is shown in Fig. 2. Through the closed-loop controller, the control strategy is used to modulate the robust three-phase current with low-frequency sinusoidal waveforms with  $120^\circ$  phase shift. No matter the degradation status of the CUTs during the life-cycle test, the low-frequency current is recycling internally and balanced all the time based on the feedback proportional-integral (PI) control loop, which can not be achieved by the existing solutions in [8] and [9]. In the control, by maintaining the given ripple voltage  $u_{\text{Ref},d}$  or ripple current  $i_{\text{Ref},d}$ , and ripple frequency  $f_R$  so that the voltage or current stresses in ac side can keep balanced without flowing into the HV source side, even if the capacitance mismatches. Since the phase currents of the power stack can be controlled independently, the ripple current is also adaptively

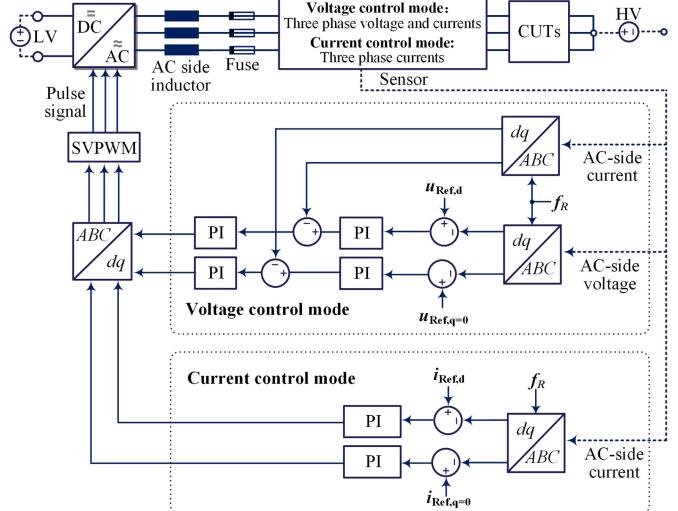


Fig. 2. Control structure of the proposed capacitor testing method.

changed at the presence of equivalent series resistance (ESR) changes to maintain the voltage stresses. The fuses shown in Fig. 1 are for short-circuit protection. Depending on the testing requirement, constant ripple voltage and constant ripple current can be achieved by the voltage-mode control and current-mode control, respectively.

### B. Testing Capability and Constraints

This part quantitatively analyzes the testing capability of the proposed testing method, including the ripple voltage and ripple current testing capability of the CUTs, and the constraints of the power stack and the LV source on the testing capability.

1) *Ripple Voltage and Ripple Current Capability*: The testing capability of the proposed test method can be represented by the ripple voltage and ripple current of CUTs.

In the ac side, the reactive power of the CUT  $Q_C$  and the ac inductor  $Q_L$  can be given by the rms value of ripple current  $I_{\text{ripple}}$  and the ripple frequency  $f_R$

$$Q_C = \frac{I_{\text{ripple}}^2}{2\pi f_R \times C_{\text{test}}} \quad (1)$$

$$Q_L = I_{\text{ripple}}^2 \times 2\pi f_R \times L \quad (2)$$

where  $C_{\text{test}}$  is the capacitance of the CUTs and  $L$  is the inductance of the ac inductor.

The rms value of ripple current  $I_{\text{ripple}}$  and the rms value of ripple voltage  $U_{\text{ripple}}$  of the CUTs are given by

$$I_{\text{ripple}} = \frac{|Q_c - Q_L|}{U_m} = \frac{U_m}{|\frac{1}{2\pi f_R \times C_{\text{test}}} - 2\pi f_R \times L|} \quad (3)$$

$$U_{\text{ripple}} = \frac{I_{\text{ripple}}}{2\pi f_R \times C_{\text{test}}} = \frac{U_m}{|1 - 4\pi^2 f_R^2 \times LC_{\text{test}}|} \quad (4)$$

where  $U_m$  represent the rms value of the output voltage in the power stack.

The range of  $I_{\text{ripple}}$  and  $U_{\text{ripple}}$  of CUTs is proportional to the value of  $U_m$ . Meanwhile, when the values of  $C_{\text{test}}$  and  $L$  are

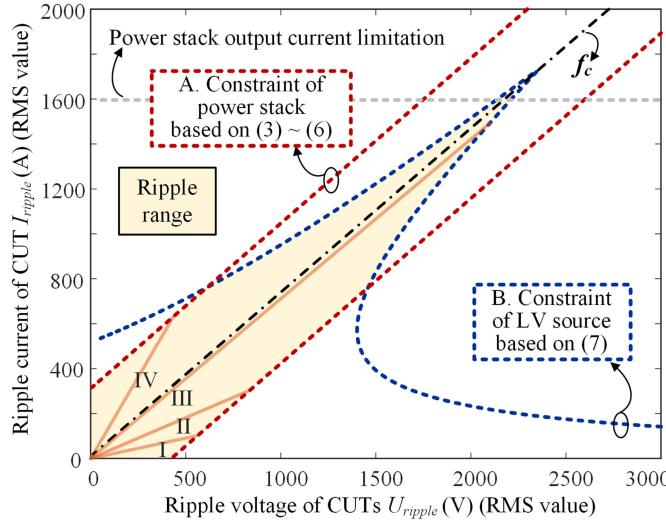


Fig. 3. Ripple voltage and ripple current testing capability. (LV source output voltage and current: 600 V, 20 A; power stack output voltage (rms), current (rms), and efficiency: 530 V, 1600 A, 97%; ripple frequency: 50 Hz; inductance: 2.5mH; CUTs value in Case I–Case IV: 1, 2, 4, and 8mF).

closer to the cutoff frequency  $f_c$ , the range of  $U_{\text{ripple}}$ , and  $I_{\text{ripple}}$  are larger

$$f_c = \frac{1}{2\pi\sqrt{LC_{\text{test}}}}. \quad (5)$$

2) *Constraint of Power Stack*: The ripple voltage and ripple current of the CUTs are limited by the rated rms value of output voltage in the power stack  $U_{o-\text{rate}}$ . In (2), the  $U_m$  should be less than the  $U_{o-\text{rate}}$

$$U_m = m \times U_L \leq U_{o-\text{rate}} \quad (m \leq 0.707) \quad (6)$$

where  $m$  and  $U_L$  represent the utilization rate of dc-link voltage in space vector pulse width modulation (SVPWM) modulation [10] and the LV output voltage, respectively.

3) *Constraint of LV Source*: The testing capability of the ripple current is also affected by the output power of the LV power supply  $P_{\text{out}}$ , which is limited by the output voltage  $U_L$  and the rated current  $I_{\text{rate}}$  of the LV source. It can be expressed as

$$P_{\text{out}} \approx I_{\text{ripple}}^2 R_{\text{total}} + (1 - \eta) I_{\text{ripple}} U_m \leq U_L \times I_{\text{rate}} \quad (7)$$

where the  $\eta$  is the efficiency of the power stack and inductors at the specific operating condition of interest, and the  $R_{\text{total}}$  represents the ESR of the CUTs.

### III. TESTING CAPABILITY ANALYSIS AND BENCHMARK

This section presents the testing capability analysis and benchmark of the proposed testing methods, with specifications for high-power capacitor [11].

#### A. Testing Capability Analysis

According to the constraints in Section III, the testing capability of a studied case specification is shown in Fig. 3. The ripple voltage and ripple current testing range of different CUTs can be obtained in (3) and (4). Equations (6) and (7), respectively,

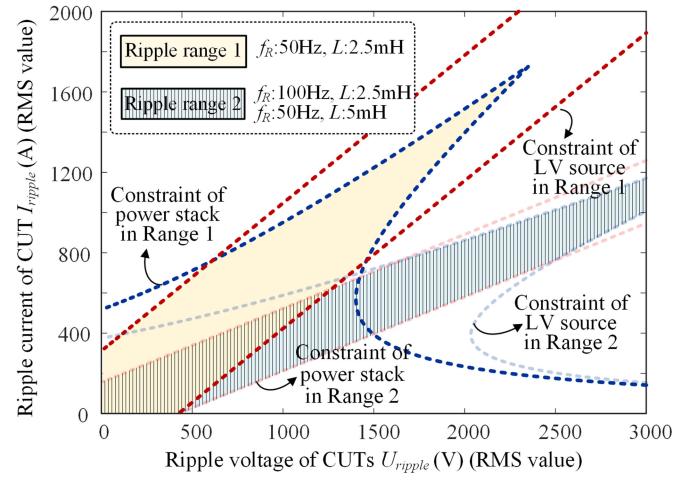


Fig. 4. Impact of different ripple frequency and inductance on ripple voltage and ripple current testing capability. (Specific conditions are same as that in Fig. 3.)

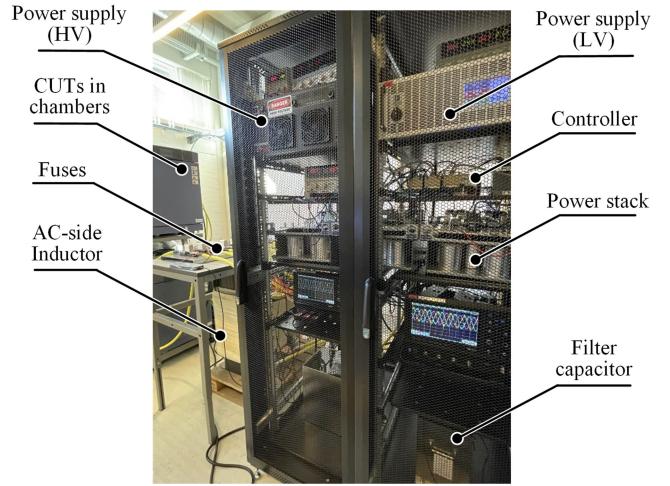


Fig. 5. Implemented AC and DC capacitor testing setup based on the proposed method.

express the constraints of the power stack and LV source. The proposed method can boost the output voltage of the power stack from 530 to 2200 V in maximum through the series circuit of the CUTs and inductors. Meanwhile, higher the efficiency, larger the rated output voltage of the power stack and larger the current of the LV source are beneficial to extend the testing ranges.

The influence of different parameters on the ripple voltage and ripple current testing range is further analyzed and shown in Fig. 4. The power stack constraint in (6) and the LV source constraint in (7) on the test capability is affect by the ripple frequency and inductance value. Different ripple testing capabilities can be obtained by selecting different test frequencies and different inductances in this method.

#### B. Benchmark With Existing Test Methods

1) *Required Power Supply*: Compared with the existing test methods, the proposed method has the minimum required power supply. In the case of emulating the same ripple current and

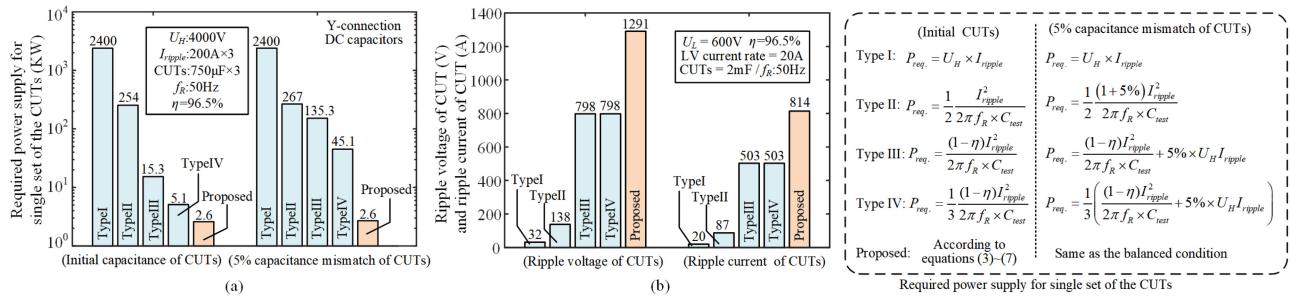


Fig. 6. Benchmark of existing test methods in [3]–[9] and the proposed test method. ( $P_{req}$  represents the required power supply for single set of the CUTs;  $\eta$  represents the efficiency of converters, transformers, and inductors;  $U_H$  and  $U_L$ , respectively, represent the output voltage of HV power supply and LV power supply;  $C_{test}$ ,  $f_R$ , and  $I_{ripple}$  represent the capacitance, ripple frequency, and ripple current of CUTs, respectively). (a) Benchmark of required power supply. (b) Benchmark of ripple voltage and ripple current.

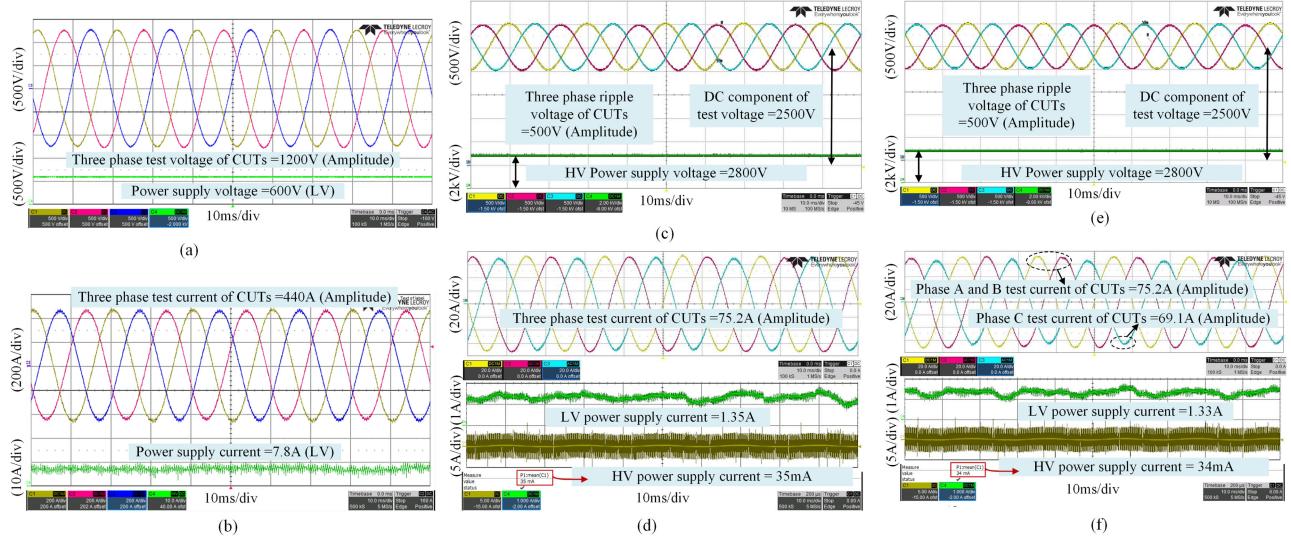


Fig. 7. Experimental testing waveforms. (a) Voltage waveform in ac capacitor testing. (b) Current waveform in ac capacitor testing. (c) Voltage waveform in dc capacitor testing. (d) Current waveform in dc capacitor testing. (e) Voltage waveform in dc capacitor testing with three-phase mismatch. (f) Current waveform in dc capacitor testing with three-phase mismatch.

ripple voltage, the required power supply for single set of the CUTs in the proposed test method only accounts for 1% in Type I and Type II, 15% in the Type III, and 50% in the Type IV, as shown in Fig. 6(a). Compared with Type I and Type II, the power supply of the proposed method only need to deal with the power loss of component in the system. Therefore, the required power supply is much smaller than those of the Type I and Type II methods. Comparing Type III and Type IV, in the proposed test method, due to the reactive power provided by the ac inductor, the output voltage of the converter is lower than the tested ripple voltage. Therefore, the required power supply is still less than the Type III and Type IV methods. Meanwhile, when the degradation rate of the dc capacitor is mismatched, the test system in Type III and Type IV cannot handle the three-phase unbalanced component so that the unbalanced current flows into the HV source. In the proposed method, the ripple current is recycling in the ac side internally all the time through the closed-loop controller, which need the minimum required power supply.

2) *Ripple Voltage and Current Testing Range:* Compared with the existing test methods, the proposed method has a

TABLE II  
EXPERIMENTAL PLATFORM PARAMETERS

CUTs setup	AC capacitor ( $\Delta$ -conection)	DC capacitor (Y-conection)	
AC-side inductor $L$		2.5mH	
Ripple frequency $f_R$		50Hz	
Efficiency $\eta$		96.5%	
LV source voltage $U_L$		600V	
HV source voltage $U_H$	0V	2800V	
Capacitance of CUTs	(75 $\mu$ F*3)*9	220 $\mu$ F*2+40 $\mu$ F	
Ripple amplitude voltage	1200V	500V	
	Calculation	Testing	Error
Ripple amplitude current	441A	440A	0.2%
LV source output current	7.6A	7.8A	2.6%
	Calculation	Testing	Error
	75.4A	75.2A	0.3%
	1.31A	1.35A	2.9%

wider range of the ripple voltage and current. In the case of choosing the same specification CUTs and power sources, the ripple voltage and current capability of the proposed method are 10 times higher than those of Type I and Type II, and 60% higher than those of Type III and Type IV, as shown in Fig. 6(b). Type III, Type IV, and the proposed method have improved the test capability of ripple voltage and current because the reactive power circulate between the power stack and the ac-side circuit in their structures. In the proposed method, the inductor and the

CUTs form the series circuit, which can obtain a higher ripple voltage than the output voltage of the power stack, thus, having a greater test capability of ripple current and ripple voltage than Type III and Type IV.

#### IV. EXPERIMENTAL VERIFICATION

The experimental platform is shown in Fig. 5, and its main parameters are shown in Table II. Fig. 7(a) and (b) shows the waveform of ac capacitor testing. The ripple voltage and current of the CUTs are stable under three-phase balanced condition. At this time, the total reactive power of the CUTs reaches 528 kVA, whereas the LV power supply only needs to provide 4.68 kW of power. As shown in Fig. 7(c) and (d), when the three-phase capacitors are balanced, the ripple voltage and current of the dc test capacitor are also stable. In Fig. 7(e) and (f), the branch capacitor of one phase is disconnected to simulate the aging and failure of the CUTs in the dc capacitor testing. The capacitance value of one phase CUTs is reduced from 480 to 440  $\mu$ F. When the capacitance of the CUTs mismatches, the ripple voltage and ripple current of the CUTs and the output current of the power supplies are still stable. Meanwhile, the HV source only needs to provide the milliamperes current and is not affected by the capacitance mismatch. Therefore, the test bench can generate stable ripple current and ripple voltage for the CUTs, and maintain the same required power supply, even if the CUTs degrades and has open-circuit during the testing. Furthermore, comparing the theoretical calculation with the test results in Table II, the error of ripple current and LV source output current between the calculated value and the test results is less than 3%, indicating that the theoretical analysis of the proposed method is reasonable.

#### V. CONCLUSION

This letter proposes a robust and scalable testing method for dc and ac capacitors with minimum required power supply, which can emulate the realistic voltage and current stresses in the HV and high-current application.

Compared with the solutions in [8] and [9], it extends the ripple voltage and ripple current ranges by 60% and reduce the

power loss of the testing system by 50%, based on a case study of Fig. 6. Proof-of-concept experiments have verify the concept of the proposed method for the dc capacitors and ac capacitors. The LV source only needs to supply the power losses of the overall testing system, and the current of the HV supply is in the range of milliamperes. A testing under capacitance mismatch among the three-phase capacitor DUTs proves the robustness of the testing method. This test method can provide a suitable choice for the parameter evaluation, degradation, and lifetime testing of high-power capacitors.

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