

Optimal Modulation Strategy for Ripple Current Reduction of DC-Link Capacitor in Multidrive Systems

Bo Yao^{ID}, Student Member, IEEE, Zhongting Tang^{ID}, Member, IEEE, Dinesh Kumar^{ID}, Senior Member, IEEE, Haoran Wang^{ID}, Member, IEEE, and Huai Wang^{ID}, Senior Member, IEEE

Abstract—This article proposes a modulation method that significantly reduces the ripple current of the dc-link capacitor in multidrive systems. It is based on the derived analytical model for the capacitor ripple current with an arbitrary number of drives connected in parallel at the dc-link side. The effects of different parameters (including load, power factor, modulation ratio, and switching frequency) on the modulation method in multiple drives are analyzed. Both the low-frequency and high-frequency current components are minimized by the optimal phase shifts of the modulation signal and the carrier signal. The cases with three drives for the optimal phase shifts corresponding to different parameter configurations are given. Benchmark studies of multidrives systems with 2–20 drives reveal that the total capacitor root mean square current is reduced to 34.3%–15.9%. Proof-of-concept experimental results verify the theoretical analysis and the effectiveness of the proposed method.

Index Terms—Analytical model, dc-link capacitor, modulation method, multidrive systems, ripple current.

I. INTRODUCTION

RECENTLY, multidrive system concepts have been used in industrial and residential applications [1], [2]. There are three typical configurations of multidrive systems: dc-side parallel with single AC load [3], [4], grid-side parallel with multiple AC loads [5], [6], and dc-link parallel with multiple AC loads [7], [8], [9], as given in Table I. In Configuration 1, multiple drives are connected in parallel to provide a high-power system, which can be used in on-board ships, electric vehicles (EVs), and hybrid EVs [3], [4]. However, this structure is just suitable for a single load system, and cannot connect multiple loads. In Configuration 2 and Configuration 3, multiple loads are provided by the AC grid or the dc grid, which can be used in pulp and paper,

Manuscript received 5 October 2022; revised 25 January 2023 and 10 April 2023; accepted 3 June 2023. Date of publication 9 June 2023; date of current version 28 July 2023. Recommended for publication by Associate Editor Y. Mohamed. (Corresponding author: Zhongting Tang.)

Bo Yao, Zhongting Tang, and Huai Wang are with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark (e-mail: ybo@energy.aau.dk; zta@energy.aau.dk; hwa@energy.aau.dk).

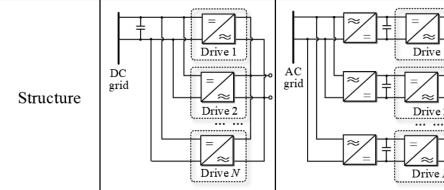
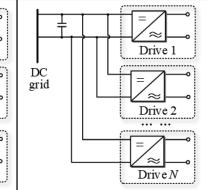
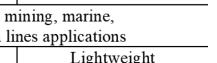
Dinesh Kumar is with the Development Center, Danfoss Drives A/S, 6300 Grasten, Denmark (e-mail: dineshr30@ieee.org).

Haoran Wang is with the Three Gorges Intelligent Industrial Control Technology Company, Ltd., Wuhan 430070, China (e-mail: wang_haoran@ctg.com.cn).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TPEL.2023.3284711>.

Digital Object Identifier 10.1109/TPEL.2023.3284711

TABLE I
THREE CONFIGURATIONS OF THE MULTIDRIVE SYSTEMS

	Configuration 1	Configuration 2	Configuration 3
Definition	DC-side parallel with one ac load	Grid-side parallel with multiple ac loads	DC-link parallel with individual ac loads
Structure			
Application	On-board ships and EV	Paper, metal, mining, marine, and production lines applications	
Advantage	High-power inverters for ac load	Configurable individual ac loads	Lightweight of the system
Limitations	Single ac load application	Multiple rectifiers for the dc link of each inverter	High ripple currents in dc link

metal and mining, marine, and production lines applications [5], [6], [7]. Compared with Configuration 2, Configuration 3 with a common dc-link system has been advocated as a possibility for future integration of drives to reduce the number of conversion stages, improve the reliability, and optimize the cost and volume, which is of interest in this article [7]. Furthermore, Configuration 3 can be more flexible and scalable as the system capacity can be increased by adding more drives without removing existing drives and additional rectifier modules [8], [9].

Despite these benefits, one of the concerns in Configuration 3 is the ripple current generated by harmonic interaction between these parallel connected drives and from pulselwidth modulation (PWM) switching [10]. The ripple current in this multidrive system linearly increases with the number of drives connected with the dc-link. On the one hand, a common practical solution in the market to suppress the dc-link harmonics is to use a large dc-link capacitor, yet the overall system compromises in terms of volume, weight, and cost [11], [12]. On the other hand, the considerable ripple current increases the hot spot temperature and reduces the lifetime of the dc-link capacitor [13], [14]. Therefore, it is important to reduce the dc-link capacitor current in multidrive systems with dc-side parallel and multiple ac loads (i.e., Configuration 3 in Table I).

Existing methods for reducing the dc-link capacitor current in multidrive systems have the following issues. In Configuration 1, a method is proposed to reduce the ripple current of the dc-link

capacitors by extracting the switching signals of drives [15], which needs the shared single ac load for multiple drives, only limited to such a configuration. The modulation methods using phase shifts of the carrier signal are given in [16] and [17], and its derived models consider the effect of different modulation ratios and power factors, respectively, which can be extended to Configuration 3 to reduce the high-order harmonics of the capacitor current. Nevertheless, this method cannot deal with the effects of low-order harmonics caused by multiple loads. In Configuration 2, the method in [18] considers the phase shifts of the modulation signal to reduce the low-order harmonics of the capacitor current. Yang et al. [19] further considered the influence of different loads. However, the derived models in [18] and [19] have mandatory conditions to configure the multiple rectifiers for the dc-link of each drive, thus the derived models are applicable for Configuration 2 only. In Configuration 3, a method is presented to suppress dc-link current harmonics by phase shifts of the carrier and the modulation signal [20]. However, this method only derives the analytical equation for dc-link capacitor ripple current with identical parameters of two drives. In addition, it cannot be used to analyze the optimal phase shifts in systems with different parameters (e.g., different loads, switching frequency, etc.) of more than two drives.

This article proposes a modulation scheme to minimize the dc-link capacitor current ripple for the multidrive systems in Configuration 3. The contribution lies in the following three aspects.

- 1) The dc-link capacitor ripple current is analytically derived and applicable for systems with a different number of drives connected in parallel.
- 2) This method can be applied to different parameters (including load, power factor, modulation ratio, and switching frequency) in multiple drives.
- 3) The modulation scheme features optimal phase shifts of both the low-frequency modulation signal and the switching-frequency carrier signal among the drives.

The rest of this article is organized as follows. Section II presents the proposed optimal modulation modeling. Section III gives the case study. Section IV discusses the experimental verification. Finally, Section V concludes this article.

II. PROPOSED OPTIMAL MODULATION MODELING

The multidrive system with a common dc bus and dc-link capacitors is shown in Fig. 1. It consists of N parallel drives, connected to a common dc bus and dc-link capacitors, powered by the dc grid. In applications, such as paper, metal, mining, marine, and production lines, the parallel drives can be considered synchronized and have the same initial phase [7], [8], [9]. This section analyzes the ripple current of dc-link capacitors and the optimal modulation scheme considering the operating condition of identical parameters and different parameters (including different loads, power factors, modulation ratios, and switching frequencies) in multiple drives.

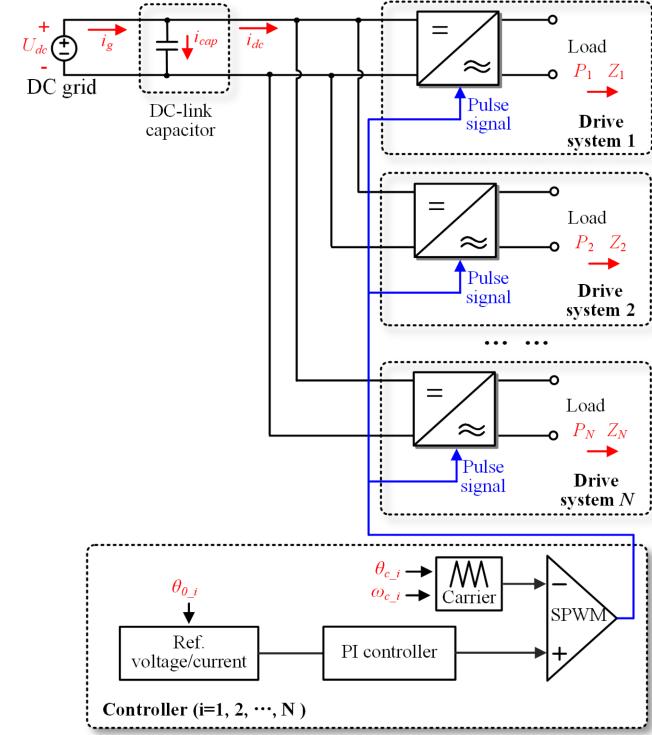


Fig. 1. Multidrive system with DC-side parallel and multiple AC loads.

A. Ripple Current for the Single Drive

The double Fourier analysis method can be used to develop spectral models for regular-sampled PWM [21]. The switching model S_{pwm} under SPWM modulation based on the triangular carrier can be expressed as follows [22]:

$$S_{\text{pwm}} = M \sin(\omega_0 t + \theta_0) + \frac{4}{\pi} \sum_{m=2,4,\dots}^{\infty} \sum_{n=\pm 1, \pm 3, \dots}^{\infty} \left[\frac{(-1)^{\frac{m}{2}}}{m} J_n\left(\frac{\pi m M}{2}\right) \times \sin(n(\omega_0 t + \theta_0) + m(\omega_c t + \theta_c)) \right] \quad (1)$$

where ω_o , ω_c , θ_o , and θ_c represent the angular velocity of the modulation signal and the carrier signal, the phase angle of the modulation signal, and the carrier signal, respectively. M represents the modulation ratio of the drive and $J_n\left(\frac{m\pi M}{2}\right)$ is the Bessel function.

The dc-link input current i_{dc} for the drive can be given as follows:

$$i_{\text{dc}} = S_{\text{pwm}} \times \frac{U_p}{ZP} \sin(\omega_0 t + \theta_0) \quad (2)$$

where U_p , Z , and P represent the amplitude of the ac voltage, the load, and the power factor of the drive, respectively.

According to (1) and (2), the dc-link input current i_{dc} can be expressed as follows:

$$\left\{ \begin{array}{l} i_{dc} = i_{dc_1} + i_{dc_2} \\ i_{dc_1} = M \sin(\omega_0 t + \theta_0) \times \frac{U_p}{ZP} \sin(\omega_0 t + \theta_0) \\ i_{dc_2} = \frac{4}{\pi} \times \frac{U_p}{ZP} \sin(\omega_0 t + \theta_0) \times \\ \sum_{m=2,4,\dots}^{\infty} \sum_{n=\pm 1,3,\dots}^{\infty} \\ \left[(-1)^{\frac{m}{2}} J_n \left(\frac{\pi m M}{2} \right) \right. \\ \left. \times \sin(n(\omega_0 t + \theta_0) + m(\omega_c t + \theta_c)) \right] \end{array} \right. \quad (3)$$

where i_{dc_1} and i_{dc_2} represent the two calculated components of the dc-link input current i_{dc} .

The first calculated component i_{dc_1} can be simplified to

$$i_{dc_1} = \frac{U_p M}{2 Z P} - \frac{U_p M}{2 Z P} \cos(2(\omega_0 t + \theta_0)). \quad (4)$$

When $n = \pm 1, \pm 3, \dots$, the function of $\cos(n(\omega_0 t + \theta_0))$ times is point symmetry, and its sum is 0. Meanwhile, from the properties of the Bessel function, it applies

$$\begin{aligned} J_{-n} \left(\frac{\pi m M}{2} \right) &= (-1)^n J_n \left(\frac{\pi m M}{2} \right) \\ &= J_n \left(\frac{\pi m M}{2} \right) \quad (n = \pm 1, \pm 3, \dots). \end{aligned} \quad (5)$$

Therefore, i_{dc_2} can be further simplified as follows:

$$\begin{aligned} i_{dc_2} &= \frac{8 U_p}{\pi Z P} \\ &\times \sum_{m=2,4,\dots}^{\infty} \sum_{n=1,3,\dots}^{\infty} \\ &\left[\begin{aligned} &(-1)^{\frac{m}{2}} J_n \left(\frac{\pi m M}{2} \right) \times \sin(\omega_0 t + \theta_0) \\ &\times \sin(n(\omega_0 t + \theta_0)) \cos(m(\omega_c t + \theta_c)) \end{aligned} \right]. \end{aligned} \quad (6)$$

According to (4) and (6), it reveals that the dc-link current of one drive consists of the dc component, low-frequency harmonics, and high-frequency harmonics. The dc component i_{dc_DC} , the low-frequency harmonic component (double-fundamental frequency) i_{dcl} , and the high-frequency harmonic component (m th-order harmonic of the carrier frequency) i_{dch} can be expressed as follows:

$$\left\{ \begin{array}{l} i_{dc} = i_{dc_DC} + i_{dcl} + i_{dch} \\ i_{dc_DC} = \frac{U_p M}{2 Z P} \\ i_{dcl} = -\frac{U_p M}{2 Z P} \cos(2(\omega_0 t + \theta_0)) \\ i_{dch} = \sum_{m=2,4,\dots}^{\infty} \\ \left[(-1)^{\frac{m}{2}} \frac{8 U_p M}{\pi Z P} \times \right. \\ \left. \sin(\omega_0 t + \theta_0) \cos(m(\omega_c t + \theta_c)) \times \right. \\ \left. \sum_{n=1,3,\dots}^{\infty} [J_n \left(\frac{\pi m M}{2} \right) \sin(n(\omega_0 t + \theta_0))] \right]. \end{array} \right. \quad (7)$$

B. Ripple Current for the Multiple Drives

In Fig. 1, the low-frequency harmonic component i_{dcl} for multiple drives can be given as follows:

$$i_{dcl} = -\frac{U_p}{2} \sum_{i=1}^N \left[\frac{M_i}{Z_i P_i} \cos(2(\omega_0 t + \theta_{0_i})) \right] \quad (8)$$

where θ_{0_i} , M_i , Z_i , and P_i represent the shifted phase angles of the modulation signal, the amplitude of the ac voltage, the modulation ratio, the impedance, and the power factor in the i th drive, respectively, and N is the number of drives.

The high-frequency harmonic current of the m th-order carrier frequency $i_{dch(m)}$ can be expressed as follows:

$$\left\{ \begin{array}{l} i_{dch(m)} = \sum_{i=1}^N H_{i(m)} \frac{8 U_p M_i}{\pi Z_i P_i} \cos(m(\omega_{c_i} t + \theta_{c_i})) \\ H_{i(m)} = \frac{(-1)^{\frac{m}{2}}}{m} \sin(\omega_0 t + \theta_{0_i}) \times \\ \sum_{n=1,3,\dots}^{\infty} [J_n \left(\frac{\pi m M}{2} \right) \sin(n(\omega_0 t + \theta_{0_i}))] \end{array} \right. \quad (9)$$

where ω_{c_i} and θ_{c_i} are the angular velocity of the modulation signal and the phase-shift angles of the carrier signal of the i th drive, respectively. $H_{i(m)}$ is the coefficient in the high-frequency current harmonics.

Therefore, the dc-link capacitor current i_{cap} can be expressed as follows:

$$i_{cap} = i_{dcl} + i_{dch(m)}. \quad (10)$$

C. Optimal Phase-Shift Scheme for Multiple Drives With Identical Parameters

When the load, the power factor, and the modulation ratio of multiple drives are identical

$$E = \frac{M_1}{Z_1 P_1} = \frac{M_2}{Z_2 P_2} = \dots = \frac{M_N}{Z_N P_N}. \quad (11)$$

In this case, the magnitude of the low-frequency harmonic current I_{dcl_mag} can be simplified as follows:

$$\begin{aligned} I_{dcl_mag} &= \frac{U_p E}{2} \\ &\sqrt{\left[\sum_{i=1}^N \sin(2\theta_{0_i}) \right]^2 + \left[\sum_{i=1}^N \cos(2\theta_{0_i}) \right]^2}. \end{aligned} \quad (12)$$

When switching frequencies are identical in the multiple drives, the magnitude of the m th-order harmonic of the carrier frequency $I_{dch(m)_mag}$ can be simplified as follows:

$$\begin{aligned} I_{dch(m)_mag} &= \frac{8 U_p E}{\pi} \\ &\sqrt{\left[\sum_{i=1}^N H_{i(m)} \sin(m\theta_{c_i}) \right]^2 + \left[\sum_{i=1}^N H_{i(m)} \cos(m\theta_{c_i}) \right]^2}. \end{aligned} \quad (13)$$

The rms current $i_{cap(rms)}$ and power loss P_{cap} of the dc-link capacitor can be expressed as follows:

$$\left\{ \begin{array}{l} i_{cap(rms)} = \sqrt{I_{dcl_mag}^2 + \sum_{m=2,4,\dots}^{\infty} I_{dch(m)_mag}^2} \\ P_{cap} = I_{dcl_mag}^2 R_{(f_{dcl})} \\ + \sum_{m=2,4,\dots}^{\infty} I_{dch(m)_mag}^2 R_{(f_{dch(m)})} \end{array} \right. \quad (14)$$

where $R_{(f_{dcl})}$ and $R_{(f_{dch(m)})}$ are the equivalent series resistance (ESR) of the dc-link capacitor at low and high frequencies, respectively.

According to (12), when the $2\theta_{0_i}$ in multidrive systems is equally divided into 360° , that is, the phase shifts of the modulation signal in the i th drive are $\frac{180}{N} \times (i-1)$, thus low-frequency

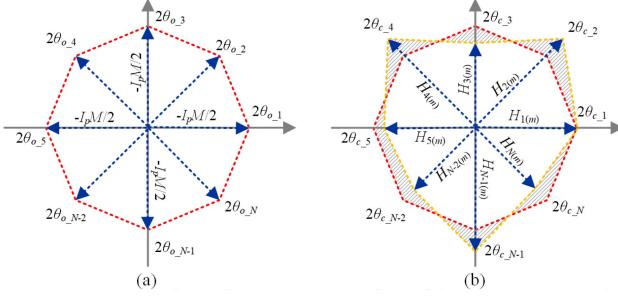


Fig. 2. Optimal phase shifts of the modulation signal and the carrier signal with identical parameters in different drives. (a) Optimal phase shifts for modulation signal. (b) Optimal phase shifts for carrier signal.

current harmonics can be completely canceled, as shown in Fig. 2(a). According to (13), the \$2\theta_{c,i}\$ can also be equally divided into \$360^\circ\$. The phase shifts of the carrier signal in the \$i\$th drive are \$\frac{180}{N} \times (i - 1)\$. It can significantly reduce the high-frequency current harmonic components. It should be noted that the abovementioned phase shifts method cannot eliminate all the high-frequency harmonics since \$H_{i(m)}\$ magnitudes are unequal in different drives. The shaded area in Fig. 2(b) represents the remaining high-frequency current components.

The selection of the phase shifts of the carrier signal or the modulation signal depends on the number of running drives. When the number of drives is \$N\$, the \$\theta_{o,i}\$ and \$\theta_{c,i}\$ of the \$i\$th drive are

$$i \in \{1, 2, \dots, N\} \quad \theta_{o,i} = \theta_{c,i} = \left\{ \frac{180}{N} \times (i - 1) \right\}. \quad (15)$$

Therefore, the implementation of the proposed optimal modulation scheme for multiple drives with identical parameters is described in Case 1 of Fig. 3(a).

D. Optimal Phase-Shift Scheme for Multiple Drives With Different Parameters

1) Different Loads, Power Factors, and Modulation Ratios:

When the load, the power factor, and the modulation ratio are different in multiple drives, the magnitude of the low-frequency harmonic current \$I_{dcl_mag}\$ can be simplified as follows:

$$I_{dcl_mag} = \frac{U_p}{2} \sqrt{\left[\sum_{i=1}^N \frac{M_i}{Z_i P_i} \sin(2\theta_{o,i}) \right]^2 + \left[\sum_{i=1}^N \frac{M_i}{Z_i P_i} \cos(2\theta_{o,i}) \right]^2}. \quad (16)$$

The magnitude of the \$m\$th-order harmonic of the carrier frequency \$I_{dch(m)_mag}\$ can be simplified as follows (17) shown at the bottom of the next page:

In this case, the rms current \$i_{cap(rms)}\$ and power loss \$P_{cap}\$ of the dc-link capacitor can be expressed by (14).

The implementation of the proposed optimal modulation scheme for multiple drives with different loads, power factors, and modulation ratios is described in Case 2 of Fig. 3(a). In the scheme, the optimal phase shifts of the modulated signal and the carrier signal are obtained, respectively, through the

particle swarm optimization (PSO) algorithm. PSO is a global optimization algorithm, which can be used to find the optimal solution for the undetermined parameters and is suitable for analyzing the optimal phase shifts in this method [23], [24]. When different drives are set with different parameters, the PSO algorithm can be used to obtain the optimal phase shifts, as shown in Fig. 3(b). To implement PSO, the first step is to set the range of the phase shifts in different drives, whose values can be assumed as \$[0, 2\pi]\$. The next step is to set particle swarm settings in the algorithm, whose values can be assumed empirically and updated in follow-up calculations [25]. According to the analytical model derived in this article, the low-order or high-order current harmonics corresponding to different groups of phase shifts within the set range are calculated, and the rms current and power loss corresponding to different phase shifts are further obtained. When the calculation result of rms current and power loss of dc-link capacitors is the minimum, the corresponding optimal phase shifts in different drives are output, which is the optimal solution.

2) Different Switching Frequencies: When the switching frequencies are different in multiple drives, the magnitude of the low-frequency harmonic current \$I_{dcl_mag}\$ can be expressed by (12).

The Hash(\$s\$) indicates the number of elements in the combination of \$m\$ orders the different switching frequencies for multiple drives

$$\text{Hash}(s) = \begin{bmatrix} 2\omega_{c,1} & 4\omega_{c,1} & \cdots & m\omega_{c,1} \\ 2\omega_{c,2} & 4\omega_{c,2} & \cdots & m\omega_{c,2} \\ \cdots & \cdots & \cdots & \cdots \\ 2\omega_{c,N} & 4\omega_{c,N} & \cdots & m\omega_{c,N} \end{bmatrix}. \quad (18)$$

The magnitude of the \$s\$th-order harmonic of the carrier frequency \$I_{dch(s)_mag}\$ can be simplified as follows (19) shown at the bottom of the next page:

where \$p\theta_{c,q}\$ and \$x_{pq}\$ denote the same element in Hash(\$s\$) and the number of that group, respectively.

In this case, the rms current \$i_{cap(rms)}\$ and power loss \$P_{cap}\$ of the dc-link capacitor can be expressed as follows:

$$\begin{cases} i_{cap(rms)} = \sqrt{I_{dcl_mag}^2 + \sum_{i=1}^s I_{dch(i)_mag}^2} \\ P_{cap} = I_{dcl_mag}^2 R_{(f_{dcl})} + \sum_{i=1}^s I_{dch(i)_mag}^2 R_{(f_{dch(i)})}. \end{cases} \quad (20)$$

The implementation of the proposed optimal modulation scheme for multiple drives with different switching frequencies is described in Case 3 of Fig. 3(a). In addition, the optimal phase shifts of the carrier signal are obtained by the PSO algorithm in Fig. 3(b).

III. CASE STUDY

According to the derived analytical model and the modulation strategy proposed in Fig. 3, the optimal phase shifts of the drives under different parameters can be obtained, as given in Table II. Taking three drives as an example, Table II(a) gives the calculation results of the optimum phase shifts for each drive at different power factors. Similarly, the table can also represent the results for different conductance (reciprocal of load) and modulation

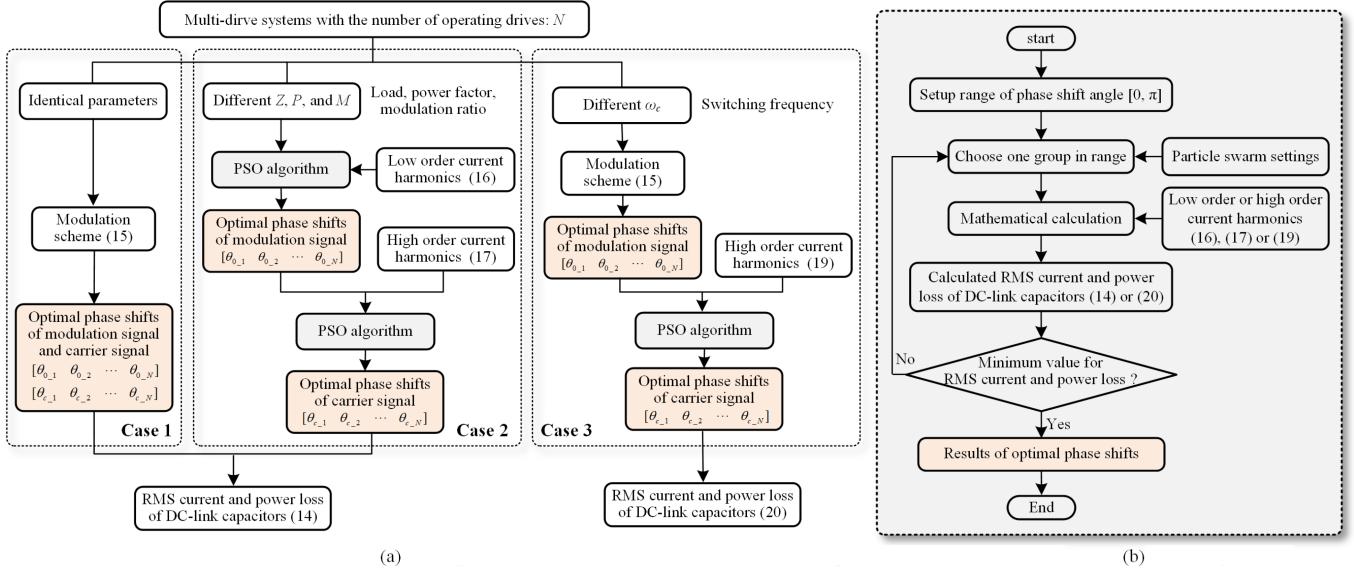


Fig. 3. (a) Proposed optimal modulation scheme for three cases for multiple drives—Case 1, Case 2, and Case 3 represent the scheme for multidrive systems with identical parameters, different load/power factor/modulation ratio, and different switching frequency among multiple drives, respectively. (b) Calculation process of the PSO algorithm.

TABLE II
LOOKUP TABLE FOR OPTIMAL PHASE SHIFTS IN DIFFERENT CONDITIONS OF MULTIPLE DRIVES (TAKE THREE DRIVES AS AN EXAMPLE)

Table I.(a)
Individual conductance/modulation ratio/power factor in the drives

		Rate of conductance/modulation ratio/power factor in the second drive				
		100%	80%	60%	40%	20%
Rate of conductance/modulation ratio/power factor in the 3 rd drive	100%	M: (60°, 120°) C: (60°, 120°)	M: (66°, 123°) C: (67°, 123°)	M: (72°, 126°) C: (73°, 126°)	M: (78°, 129°) C: (81°, 131°)	M: (84°, 132°) C: (87°, 134°)
	80%	M: (66°, 123°) C: (67°, 123°)	M: (64°, 116°) C: (64°, 116°)	M: (72°, 117°) C: (61°, 109°)	M: (79°, 115°) C: (58°, 99°)	M: (90°, 90°) C: (50°, 93°)
	60%	M: (72°, 126°) C: (73°, 126°)	M: (72°, 117°) C: (61°, 109°)	M: (73°, 107°) C: (70°, 110°)	M: (90°, 90°) C: (73°, 99°)	M: (90°, 90°) C: (86°, 110°)
	40%	M: (78°, 129°) C: (81°, 131°)	M: (79°, 115°) C: (58°, 99°)	M: (90°, 90°) C: (73°, 99°)	M: (90°, 90°) C: (80°, 100°)	M: (90°, 90°) C: (79°, 95°)
	20%	M: (84°, 132°) C: (87°, 134°)	M: (90°, 90°) C: (50°, 93°)	M: (90°, 90°) C: (86°, 110°)	M: (90°, 90°) C: (79°, 95°)	M: (90°, 90°) C: (90°, 90°)

- Keep the conductance/modulation ratio/power factor in the First drive at 100%; (Conductance is the inverse of the loading.)
- Keep the phase shift of the carrier signal and modulation signal in the First drive both at 0°;
- M indicates phase shift of the modulation signals of the second and third drives;
- C indicates phase shift of the carrier signals of the second and third drives.

Table I.(b)
Individual switching frequency in the drives

		Multiples of switching frequency in the second drive				
		1.0	1.5	2.0	3.0	5.0
Multiples of switching frequency in the 3 rd drive	1.0	M: (60°, 120°) C: (60°, 120°)	M: (60°, 120°) C: (84°, 108°)	M: (60°, 120°) C: (90°, 90°)	M: (60°, 120°) C: (76°, 114°)	M: (60°, 120°) C: (101°, 162°)
	1.5	M: (60°, 120°) C: (84°, 108°)	M: (60°, 120°) C: (90°, 90°)	M: (60°, 120°) C: (92°, 163°)	M: (60°, 120°) C: (90°, 180°)	M: (60°, 120°) C: (90°, 180°)
	2.0	M: (60°, 120°) C: (90°, 90°)	M: (60°, 120°) C: (92°, 163°)	M: (60°, 120°) C: (90°, 180°)	M: (60°, 120°) C: (84°, 105°)	M: (60°, 120°) C: (18°, 85°)
	3.0	M: (60°, 120°) C: (76°, 114°)	M: (60°, 120°) C: (90°, 180°)	M: (60°, 120°) C: (84°, 105°)	M: (60°, 120°) C: (45°, 126°)	M: (60°, 120°) C: (90°, 180°)
	5.0	M: (60°, 120°) C: (101°, 162°)	M: (60°, 120°) C: (90°, 180°)	M: (60°, 120°) C: (18°, 85°)	M: (60°, 120°) C: (90°, 180°)	M: (60°, 120°) C: (37°, 132°)

- Keep the multiple of switching frequency in the First drive at 1.0;
- Keep the phase shift of the carrier signal and modulation signal in the First drive both at 0°;
- M indicates phase shift of the modulation signals of the second and third drives;
- C indicates phase shift of the carrier signals of the second and third drives.

factors for multiple drives. With the identical power factors in the multiple drives, it can be seen that both the optimal phase shifts of the carrier signal and modulation signal are 0° , 60° , and 120° in the multiple drives, which agrees well with (15). With the different power factors in the multiple drives, the optimal phase shifts of the carrier signal and the modulation signal are dynamic, which is obtained by the PSO algorithm. Meanwhile, if N drives have the same switching frequency, and one of those has a significantly lower load, the optimal phase shifts of the modulation signal would converge toward that of $N - 1$ drives.

$$I_{\text{dch}(m)-\text{mag}} = \frac{8U_p}{\pi} \times \sqrt{\left[\sum_{i=1}^N \frac{M_i H_{i(m)}}{Z_i P_i} \sin(m\theta_{c-i}) \right]^2 + \left[\sum_{i=1}^N \frac{M_i H_{i(m)}}{Z_i P_i} \cos(m\theta_{c-i}) \right]^2}. \quad (17)$$

$$I_{\text{dch}(s)-\text{mag}} = \frac{8U_p}{\pi} \times \sqrt{\left[\sum_{i=1}^{x_{pq}} \frac{M_i H_{i(s)}}{Z_i P_i} \sin(p\theta_{c-q}) \right]^2 + \left[\sum_{i=1}^{x_{pq}} \frac{M_i H_{i(s)}}{Z_i P_i} \cos(p\theta_{c-q}) \right]^2}. \quad (19)$$

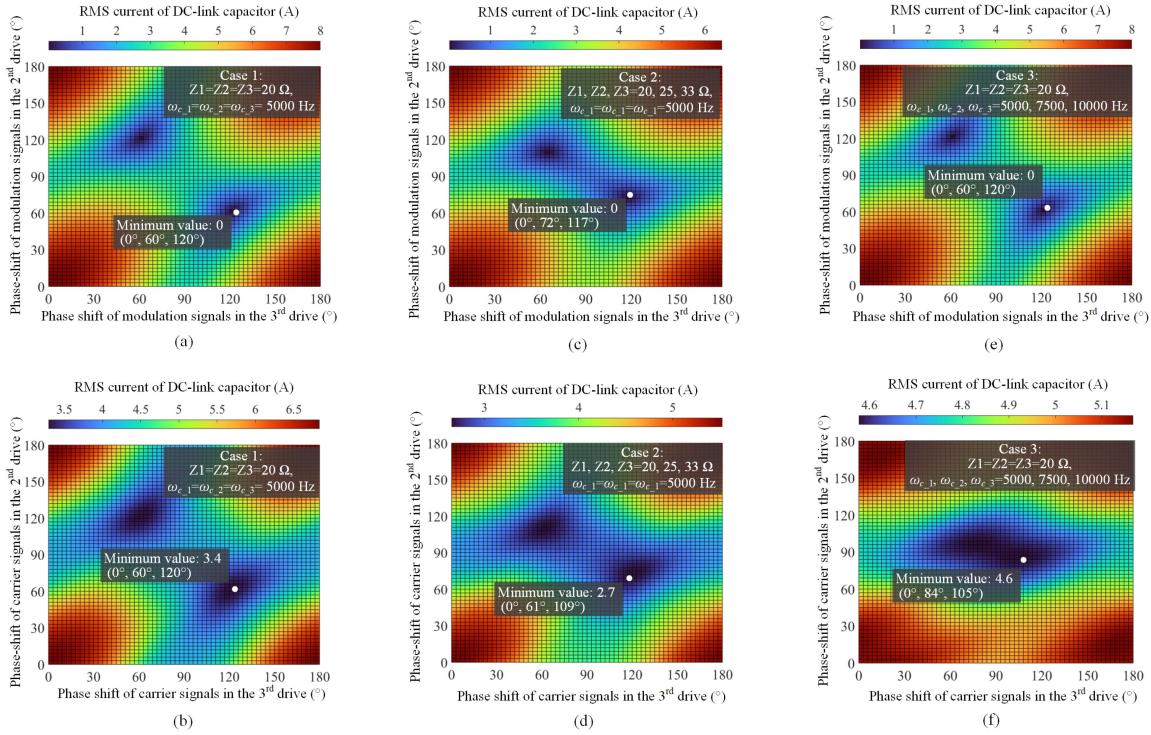


Fig. 4. RMS current of DC-link capacitor by the analytical equations in the three drives system. (a), (b) Case 1: identical parameters in multiple drives. (c), (d) Case 2: different loads in multiple drives. (e), (f) Case 3: different switching frequency in multiple drives. The phase shift of the carrier signal in the first drive is 0° in each case. The numerical results are specific to the system with the specifications given in Table III discussed later in Section IV. (a) RMS value of low-frequency harmonic current (Case 1). (b) RMS value of high-frequency harmonic current (Case 1). (c) RMS value of low-frequency harmonic current (Case 2). (d) RMS value of high-frequency harmonic current (Case 2). (e) RMS value of low-frequency harmonic current (Case 3). (f) RMS value of high-frequency harmonic current (Case 3).

Table II(b) gives the calculation results of the optimum phase shifts for each drive at the different switching frequencies. The optimal phase shifts of the modulation signal are all 0° , 60° , and 120° , which are consistent with (15). Furthermore, with the different switching frequency in the multiple drives, the optimal phase shifts of the carrier signal are dynamic, which is obtained by the PSO algorithm. The method adopted is to obtain the lookup table according to the offline precomputation of the optimized modulation scheme proposed in Fig. 3. The table is then embedded into the control program.

Fig. 4 shows the rms current of the dc-link capacitors of low-frequency harmonic and high-frequency harmonic with different carrier and modulation phase shifts when three drives are connected in parallel. In Fig. 4, three cases are considered, respectively, with identical parameters, different loads, and different switching frequency in the multiple drives. When the identical parameters in the three drives are set in Fig. 4(a) and (b), it can be seen that both the optimal phase shifts of the carrier signal and the modulation signal are 0° , 60° , and 120° in the multiple drives, which agrees well with Table I. When the different loads with 100%, 80%, and 60% values in the three drives are set in Fig. 4(c) and (d), it can be seen that the optimal phase shifts of the carrier signal and the modulation signal are $[0^\circ, 72^\circ, 117^\circ]$ and $[0^\circ, 61^\circ, 109^\circ]$, respectively, which consistent with the results in Table I. When the different switching frequency with 1.0, 1.5, and 2.0 times in the three drives are set in Fig. 4(e) and (f), it can be seen that the optimal phase shifts of the carrier signal and

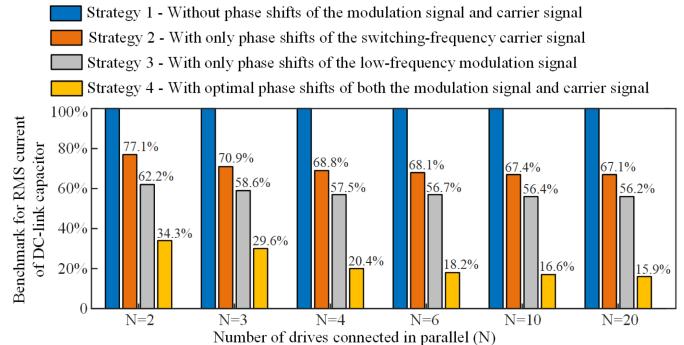


Fig. 5. Benchmark for the rms value of DC-link capacitor ripple current with identical parameters in the multiple drives.

the modulation signal are $[0^\circ, 60^\circ, 120^\circ]$ and $[0^\circ, 84^\circ, 105^\circ]$, respectively, which is also consistent with the results in Table I.

The benchmark of the dc-link capacitor rms current with identical parameters and different N is further analyzed in Fig. 5. The rms current ratios of dc-link capacitors, including four phase-shift strategies of the carrier signal and the modulation signal, are compared. It can be seen that the rms current of the dc-link capacitor with the proposed modulation method is only 34.3%–15.9% of that without a phase-shift scheme if N varies from 2 to 20, respectively. Based on the frequency-dependent ESR values and dc-link capacitor ripple current spectrum, the power loss of the specific dc-link capacitors can be obtained.

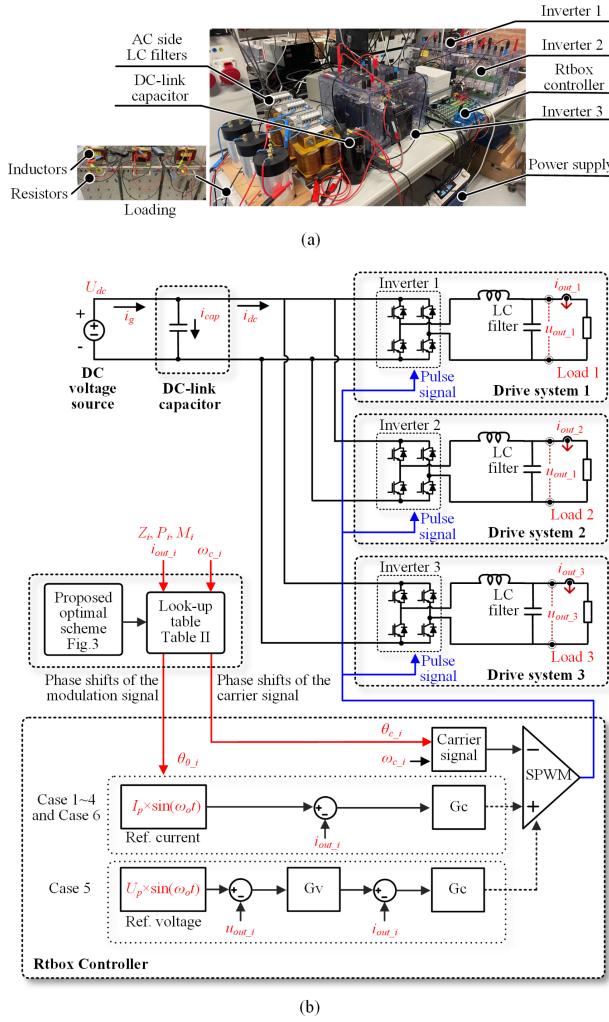


Fig. 6. (a) Experimental prototype of the multiple drives. (b) Schematic diagram of the multiple drives.

IV. EXPERIMENTAL VERIFICATION

A. Experimental Setup

The experimental platform and the control schematic are shown in Fig. 6, where three drives are connected in parallel. Each inverter consists of four insulated gate bipolar transistors (IGBTs) (with antiparallel diodes). In addition, each inverter is configured with an *LC*-type filter and a load. The RT-box controller is used, which integrates the field programmable gate array (FPGA) chip to control multiple drives simultaneously, thus the clock frequency of each drive is synchronized. It should be noted that when each drive has a separate control platform, the clock synchronization settings for the DSPs or FPGAs of different drives can be achieved by the clock synchronization methods [26], [27].

The control schematic is presented in Fig. 6(b), where the double-loop control method and single-loop control method are both adopted. First, the reference voltage $U_p \times \sin(\omega_o t)$ or reference current $I_p \times \sin(\omega_o t)$ are given, and the frequency ω_0 can be changed along with different motor speed. In the

TABLE III
SYSTEM PARAMETERS

Circuit parameters	
DC-source output voltage	150 V
AC-side output voltage	110 V
Capacitance and ESR of DC-link capacitor	2.75 mF (100 Hz) 122 mΩ (100 Hz)
<i>LC</i> filters in ac side	2 mH / 40 μF
PWM dead time	2×10^{-7} s
Inductance of <i>LC</i> nonlinear load	5.6 mH
Output frequency of inverters	Cases 1–4, Case 6: 50 Hz Cases 5: 30–90 Hz
AC side loads of three inverters	Cases 1, 3, and 5: $20 \Omega / 20 \Omega / 20 \Omega$ Cases 2 and 4: $20 \Omega / 25 \Omega / 33 \Omega$ Cases 6: $[20 \ 20 \ 20] \rightarrow [20 \ 20 \ 25] \rightarrow [20 \ 25 \ 33] \rightarrow [20 \ 33 \ 50] \Omega$
Switching frequency of three inverters	Case 1, 2, 5 and 6: 5 kHz / 5 kHz / 5 kHz Case 3 and 4: 5 kHz / 7.5 kHz / 10 kHz

double-loop control method, compared with the reference voltage and the measurement voltage u_{out-i} , the voltage error goes through a proportional integral (PI) voltage controller (G_v) to generate the reference current. In the single-loop control method, the current error, generated by comparing the reference current and the feedback current i_{out-i} , passes through a PI current controller G_c to generate modulation ratios of full-bridge drives. Finally, the triangular carrier (switching frequency is ω_{c-i}) and the modulation ratios can generate the PWM signals through modulation methods, where the pulse signal PWMs 1–3 are set for drive system 1–3, respectively. A dead time of 200 ns is set in the SPWM.

Meanwhile, how to integrate the proposed optimal scheme into the controller is given in Fig. 6(b). According to the modulation scheme shown in Fig. 3 for the three cases, the obtained Table II is embedded in the controller. The proposed optimal scheme aims to generate θ_{0-i} and θ_{c-i} , which can be obtained by setting different parameters of the drives (e.g., load, power factor, modulation ratio, switching frequency, etc.).

The specifications are given in Table III, including six experimental cases. In Case 1, three drives have the same parameters, i.e., loads are 20Ω and switching frequencies are 5 kHz. Case 2 has different loads in those three drives, i.e., the loads of drive 1–3 are $20, 25$, and 33Ω , respectively, and the switching frequencies are 5 kHz. Case 3 sets different switching frequencies, where loads are 20Ω , and switching frequencies are 5, 7.5, and 10 kHz in drives 1–3, respectively. Case 4 sets both different loads and different switching frequencies in drives 1–3, respectively. In Case 5, the experiment of dynamic output current frequency is given, where the single-loop current control method is used. Step changes in load and number of drives are shown in Case 6. Four different modulation schemes are compared, where Strategy 1 is the modulation method without the phase-shift scheme, Strategy 2 represents the modulation scheme with only phase shifts of the switching-frequency carrier signal, Strategy 3 is the modulation method with phase shifts of only the low-frequency modulation signal, and Strategy 4 is the proposed modulation strategy with optimal phase shifts of both the low-frequency modulation signal and the switching-frequency carrier signal.

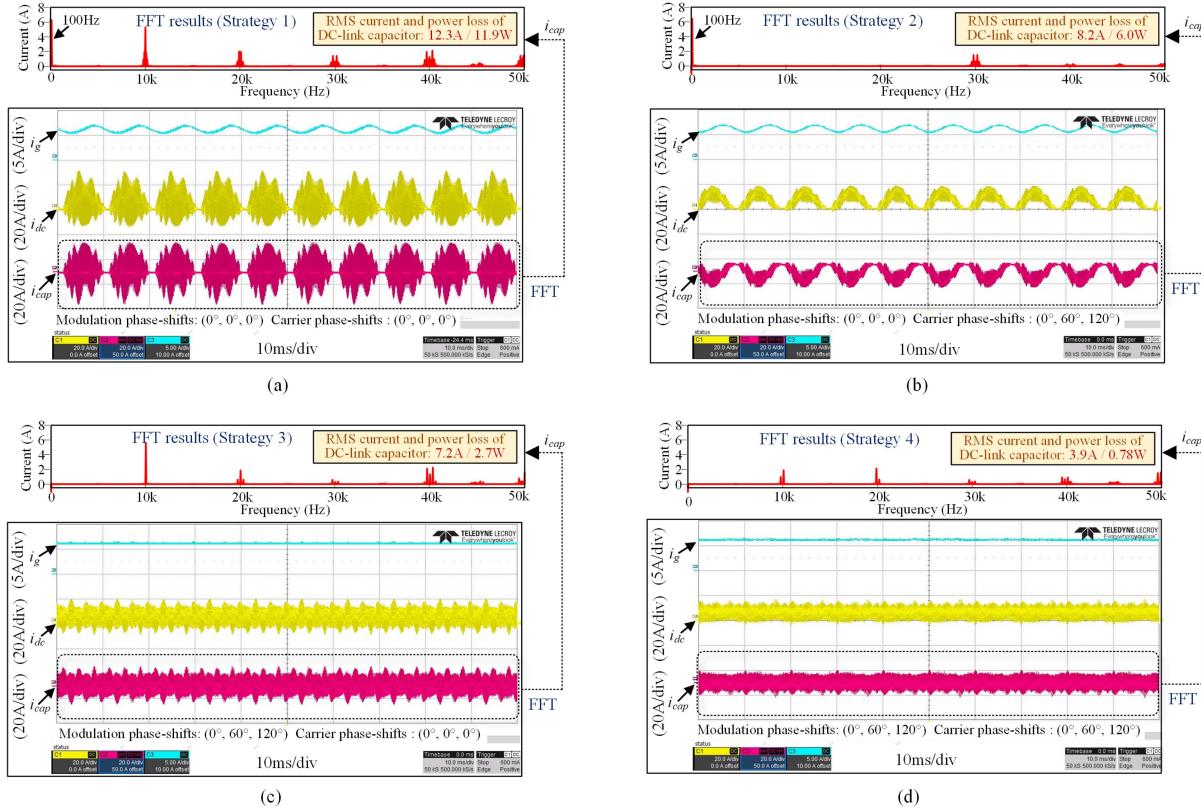


Fig. 7. Steady-state experimental current waveforms and DC-link capacitor ripple current spectrum with identical parameters in multiple drives. (a) Strategy 1. (b) Strategy 2. (c) Strategy 3. (d) Strategy 4. (Three drives are in parallel with an identical load of $20\ \Omega$ and identical switching frequency of $5\ kHz$: i_g —DC-side supply current, i_{dc} —DC bus current, and i_{cap} —capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

B. Case 1: Multiple Drives With Identical Load and Switching Frequency

Fig. 7 shows the waveforms of the dc-side supply current i_g , the dc bus current i_{dc} , and the capacitor ripple current i_{cap} with identical parameters in multiple drives for all four strategies. i_{dc} and i_{cap} vary according to different phase-shift schemes. The phase shifts are obtained from Case 1 in Fig. 3. The fast Fourier transform (FFT) analysis verifies the results that when the phase shifts of the modulation signal are 0° , 60° , and 120° (with Strategy 3 and Strategy 4), the low-frequency harmonics can be eliminated. When the phase shifts of the carrier signal are 0° , 60° , and 120° (with Strategy 2 and Strategy 4), the high-frequency harmonic current can be reduced. With Strategy 2 and Strategy 4, there are still high-order harmonics, which correspond to the shaded areas in Fig. 2. It shows that the rms current of the dc-link capacitor with Strategy 2, Strategy 3, and Strategy 4 are 66.7%, 58.5%, and 31.3%, respectively, of that with Strategy 1. The error of the experimental results with the benchmark in Fig. 5 is within 6%, indicating that the proposed analytical model is accurate. Meanwhile, the power loss of the dc-link capacitor with Strategy 4 is only 6.5% of that with Strategy 1.

To characterize the effect of nonlinear loads on the motor, the R - L nonlinear load (the inductor in series with the resistor) is set in the experimental prototype to emulate the ac motor nonlinearity, as shown in Fig. 8. Due to the nonlinear loads,

its dc-link current harmonics increase, the ripple current of the dc-link capacitor increases from 12.3 A (experimental results for linear load in Fig. 7 of this article) to 13.1 A in Strategy 1. In Fig. 8(a) and (b), comparing the results of the modulation strategy without phase shift and the modulation strategy with the proposed optimized phase shift, it can be found that considering the R - L nonlinear loads in operation, the modulation with the proposed optimized phase shift can also effectively reduce the ripple current of dc-link capacitor. In this case, the rms current and power loss of the dc-link capacitor with the proposed optimized phase shift are 32% and 6.7% of that without phase shift, respectively. The results imply that the ripple current of the dc-link capacitor can be also optimized in multiple drives with R - L load.

C. Case 2: Multiple Drives With Identical Switching Frequency and Different Loads

Fig. 9 shows the waveforms of the dc-side supply current i_g , the dc bus current i_{dc} , and the capacitor ripple current i_{cap} with different loads in multiple drives for all four strategies. The i_{dc} and i_{cap} vary according to different phase-shift strategies. With Strategy 2, the phase shifts of the carrier signal are 0° , 60° , and 120° . With Strategy 3, the phase shifts of the modulation signal are 0° , 60° , and 120° . With Strategy 4, the optimal phase shifts (0° , 72° , 117° in the modulation signal and 0° , 61° , and 109° in

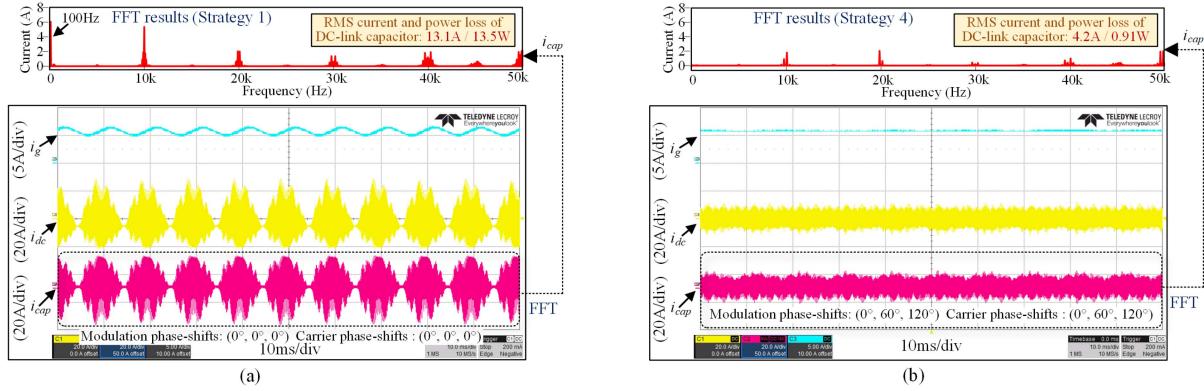


Fig. 8. Steady-state experimental current waveforms and DC-link capacitor ripple current spectrum with $R-L$ nonlinear load in multiple drives. (a) Strategy 1. (b) Strategy 4. (Three drives are in parallel with an identical load of $20\ \Omega$ resistor and 5.6 mH inductor, and identical switching frequency of 5 kHz ; i_g —DC-side supply current, i_{dc} —DC bus current, and i_{cap} —capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

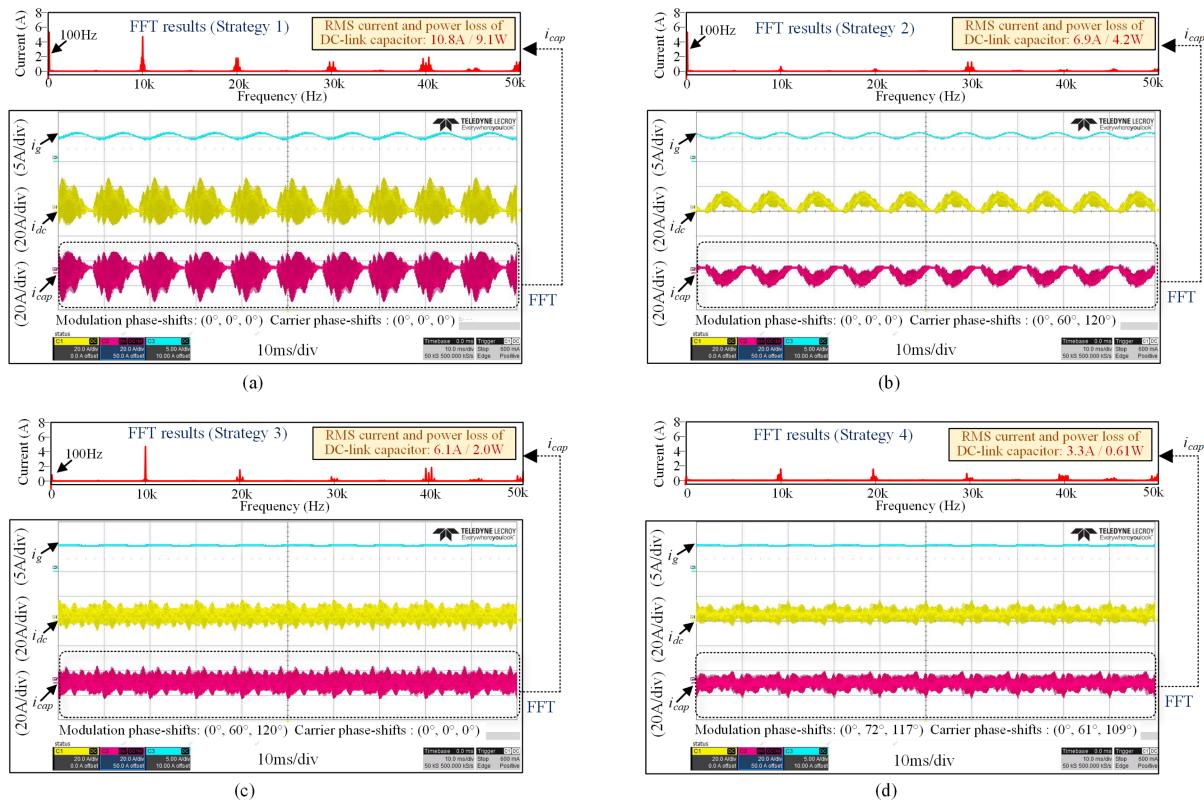


Fig. 9. Steady-state experimental current waveforms and DC-link capacitor ripple current spectrum with different loads in multiple drives. (a) Strategy 1. (b) Strategy 2. (c) Strategy 3. (d) Strategy 4. (Three drives are in parallel with different loads of 20 , 25 , and $33\ \Omega$, and an identical switching frequency of 5 kHz ; i_g —DC-side supply current, i_{dc} —DC bus current, and i_{cap} —capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

the carrier signal) are obtained from the proposed modulation scheme in Fig. 3 and results in Table II. The FFT analysis verifies the results that when the phase shifts of the modulation signal are 0° , 72° , and 117° with different loads of 20 , 25 , and $33\ \Omega$ in three drives (in Strategy 4), the low-frequency harmonics can be eliminated. When the phase shifts of the carrier signal are 0° , 61° , and 109° (in Strategy 4), the high-frequency harmonic current

can be reduced. Through the calculation, the rms current of the dc-link capacitor with Strategy 2, Strategy 3, and Strategy 4 are 63.9% , 56.5% , and 30.6% of that with Strategy 1. Meanwhile, the power loss of the dc-link capacitor with Strategy 4 is only 6.7% of that with Strategy 1. It indicates that the proposed optimal modulation method is reasonable in multiple drives with different loads.

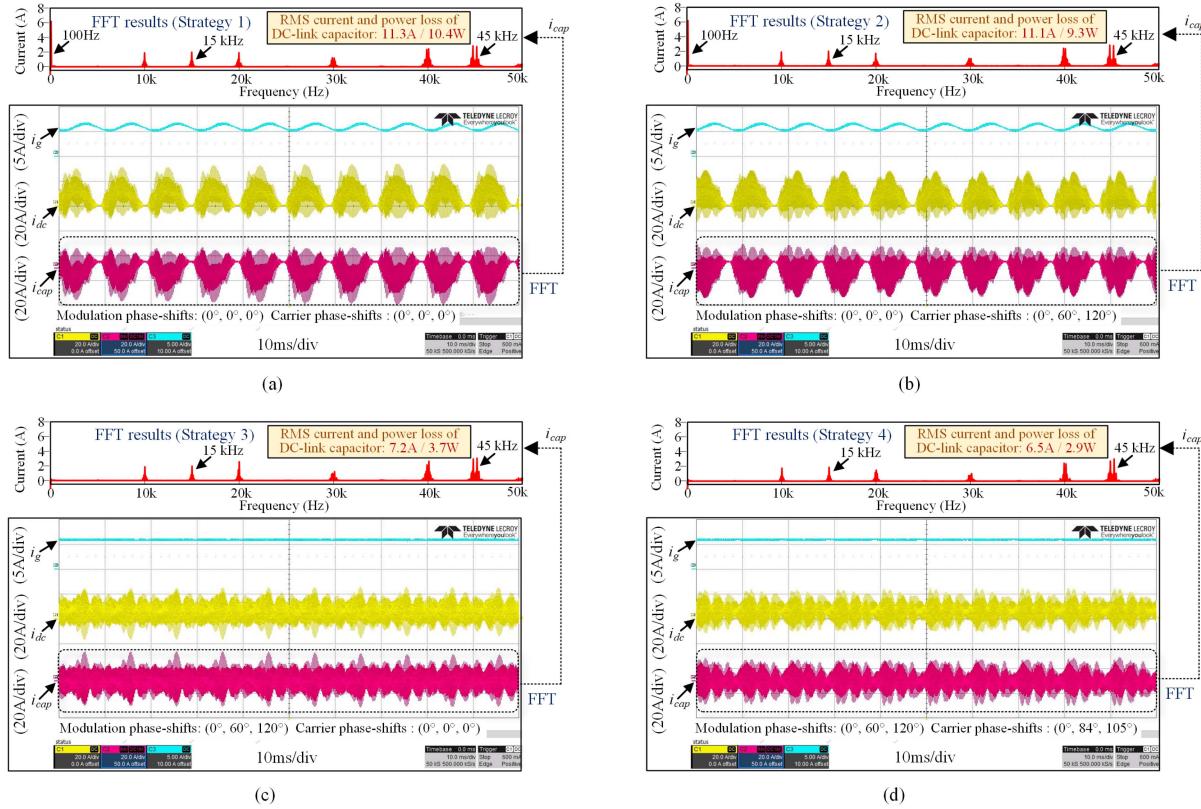


Fig. 10. Steady-state experimental current waveforms and DC-link capacitor ripple current spectrum with different switching frequencies in multiple drives. (a) Strategy 1. (b) Strategy 2. (c) Strategy 3. (d) Strategy 4. (Three drives are in parallel with an identical load of 20Ω , and different switching frequencies of 5, 7.5, and 10 kHz; i_g —DC-side supply current, i_{dc} —DC bus current, and i_{cap} —capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

D. Case 3: Multiple Drives With Identical Load and Different Switching Frequency

Fig. 10 shows the waveforms of the dc-side supply current i_g , the dc bus current i_{dc} , and the capacitor ripple current i_{cap} with different switching frequencies in multiple drives for all four strategies. i_{dc} and i_{cap} vary according to different phase-shift strategies. With Strategy 2, the phase shifts of the carrier signal are 0° , 60° , and 120° . With Strategy 3, the phase shifts of the modulation signal are 0° , 60° , and 120° . With Strategy 4, the optimal phase shifts (0° , 60° , and 120° in the modulation signal and 0° , 84° , and 105° in the carrier signal) are obtained from the proposed modulation scheme in Fig. 3 and the results in Table II. The FFT analysis verifies the results that when the phase shifts of the modulation signal are 0° , 60° , and 120° with different switching frequencies in three drives (with Strategy 3 and Strategy 4), the low-frequency harmonics can be eliminated, which is consistent with Case 1. When the phase shifts of the carrier signal are 0° , 84° , and 105° (with Strategy 4), the high-frequency harmonic current can be reduced. Through the calculation, the rms current of the dc-link capacitor with Strategy 2, Strategy 3, and Strategy 4 are 98.2%, 63.7%, and 57.5% of that with Strategy 1. Meanwhile, the power loss of the dc-link capacitor with Strategy 4 is 27.9% of that with Strategy 1. It indicates that the proposed optimal modulation method is still effective in multiple drives with different switching frequencies.

E. Case 4: Multiple Drives With Different Loads and Switching Frequency

Fig. 11 shows the current waveforms and dc-link capacitor ripple current spectrum with both different loads and switching frequencies in multiple drives. In this case, three drives are in parallel with different loads of 20 , 25 , and 33Ω , and different switching frequencies of 5, 7.5, and 10 kHz. In Fig. 11(a), the phase shifts of the modulation signal and carrier signal are all 0° . In Fig. 11(b), according to the modulation strategy of Case 2 in Fig. 3, since the different switching frequencies do not affect the low-frequency harmonics, the optimal modulation phase shift can be obtained as $(0^\circ, 72^\circ, 117^\circ)$ based on the different loads in three drives. Meanwhile, in addition, according to the modulation strategy of Case 3 in Fig. 3, considering the different switching frequency, the optimal carrier phase shift can be obtained as $(0^\circ, 74^\circ, 107^\circ)$. Through the calculation, the rms current and power loss of the dc-link capacitor with the optimal phase shift are 57.7% and 29.6% of that without phase shift, respectively. It indicates that the proposed optimal modulation method is reasonable in multiple drives with both different loads and different switching frequency.

F. Case 5: Dynamic Output Frequency of Drives

The R - L load is used to emulate the nonlinearity of the ac motor in this case. In this arrangement, the motor speed dynamic

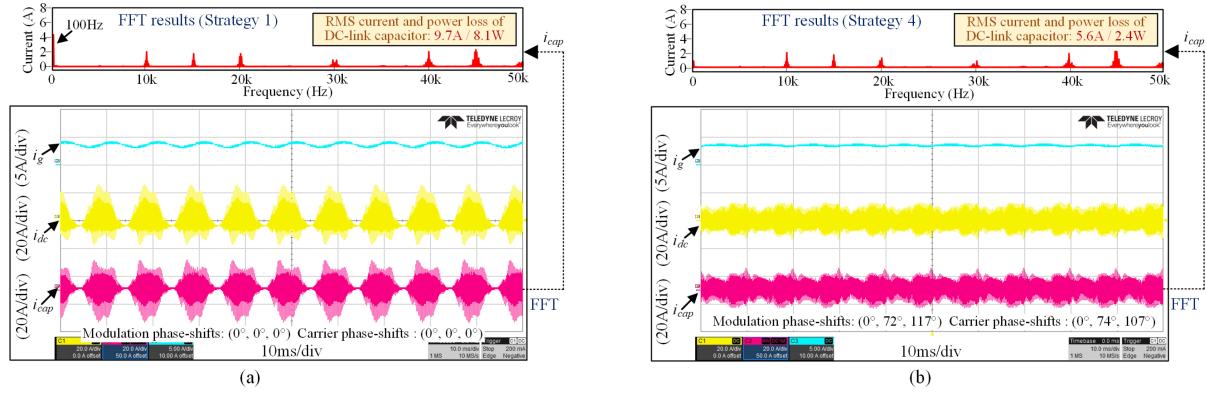


Fig. 11. Steady-state experimental current waveforms and DC-link capacitor ripple current spectrum with both different loads and switching frequencies in multiple drives. (a) Strategy 1. (b) Strategy 4. (Three drives are in parallel with an identical load of 20, 25, and 33 Ω, and different switching frequencies of 5, 7.5, and 10 kHz; i_g —DC-side supply current, i_{dc} —DC bus current, and i_{cap} —capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

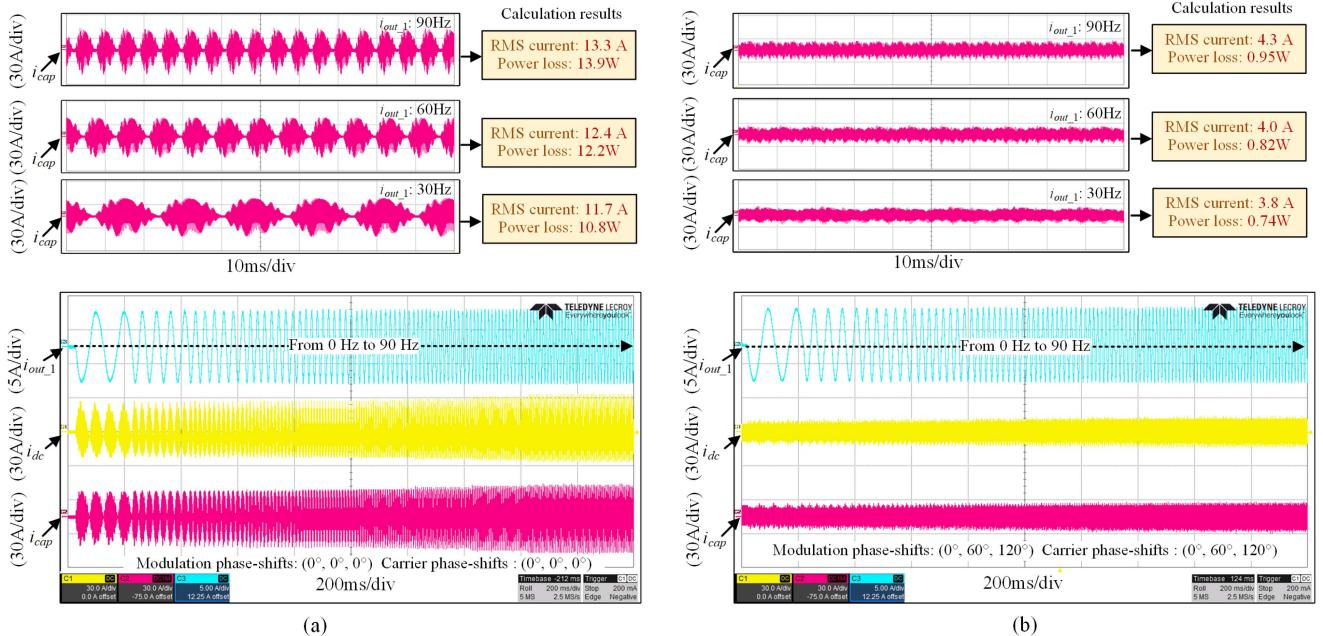


Fig. 12. Experimental current waveforms and DC-link capacitor ripple current spectrum with dynamic output current frequency. (a) Strategy 1. (b) Strategy 4. (Output current frequency change from 0 to 90 Hz in operation; i_g —DC-side supply current, i_{dc} —DC bus current, and i_{cap} —capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

represents with output frequency of the drives. The experimental waveforms with dynamic output frequency are given to simulate the change in motor speed. Fig. 12 shows the results with the output frequency change from 0 to 90 Hz in operation. The results show that the modulation strategy proposed in this article can still reduce the ripple current of the dc-link capacitor when the output frequency of the drives varies dynamically. According to Fig. 12(a) and (b), comparing the modulation strategy without phase shift and the modulation strategy with the proposed optimized phase shift, it can be found that at different output frequencies, the modulation with the proposed optimized phase shift can effectively reduce the ripple current of the dc-link capacitor. For example, when the output frequency is 30 Hz, the rms current and power loss of the dc-link capacitor with

the proposed optimized phase shift are 32.4% and 6.8% of that without phase shift, respectively. When the output frequency is 90 Hz, the rms current and power loss of the dc-link capacitor with the proposed optimized phase shift are 32.5% and 7.0% of that without phase shift, respectively. The results imply that the optimized performance can be also maintained with dynamic output frequency in operation.

G. Case 6: Dynamic Change of the Load and Number of Drives

Fig. 13 shows the results of the source output current, the drive input current, and the dc-link capacitor ripple current with the load step and continuous changing of drives in operation.

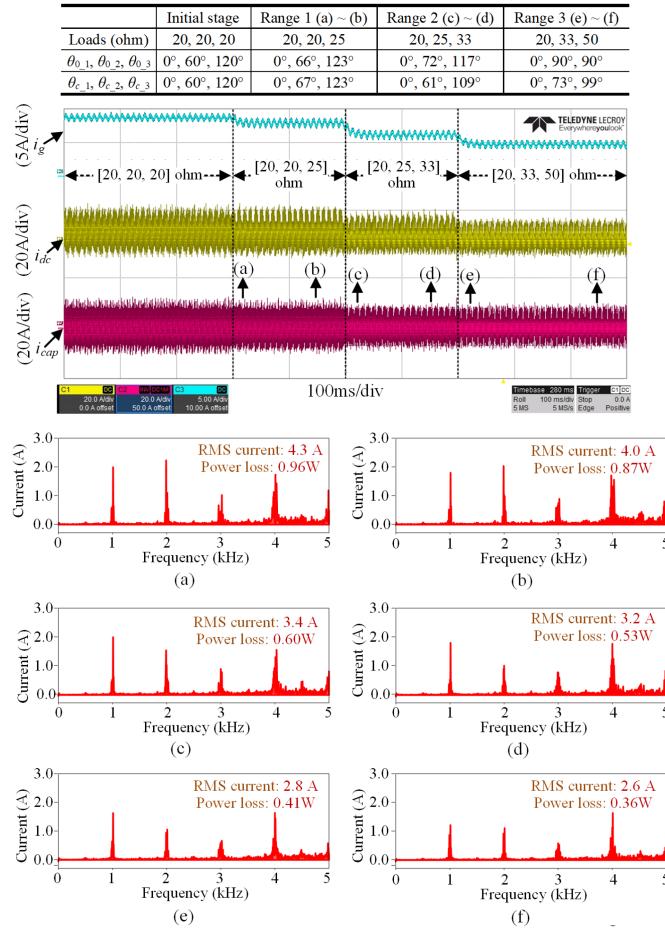


Fig. 13. Experimental capacitor ripple current waveforms and FFT analysis results with load steps and continuous changes. (a) Dynamic range 1. (b) Stable range 1. (c) Dynamic range 2. (d) Stable range 2. (e) Dynamic range 3. (f) Stable range 3. (i_g —DC-side supply current, i_{dc} —DC bus current, and i_{cap} —capacitor ripple current; Strategy 4—modulation with the proposed optimal phase shifts.)

Four sets of load changes are given in three drives. The optimized modulation and carrier phase shifts are given in the table of Fig. 13 based on the load changes. The (a) represents the dynamic stage of Range 1, (b) represents the stable stage of Range 1, (c) represents the dynamic stage of Range 2, (d) represents the stable stage of Range 2, (e) represents the dynamic stage of Range 3, and (f) represents the stable stage of Range 3. Comparing the stable and dynamic stages of each range shows that continuous modifications to the modulation and carrier phase shift produce spectral effects. During dynamic changes, high-frequency components of the harmonics are higher than in the steady state. However, the dynamic stage only lasts for 1 to 2 fundamental periods before operating in the low-harmonic stable state.

In addition, the dynamic variation of the drive output current based on various operating conditions and phase-shift changes is presented in Fig. 14. The four sets of load variations and optimized modulation and carrier phase shifts are consistent with Fig. 13. Similarly, the ac output current of the drives (using output current of drive 1 as an example) collected is subjected to FFT analysis, and the frequency spectrum analysis results and

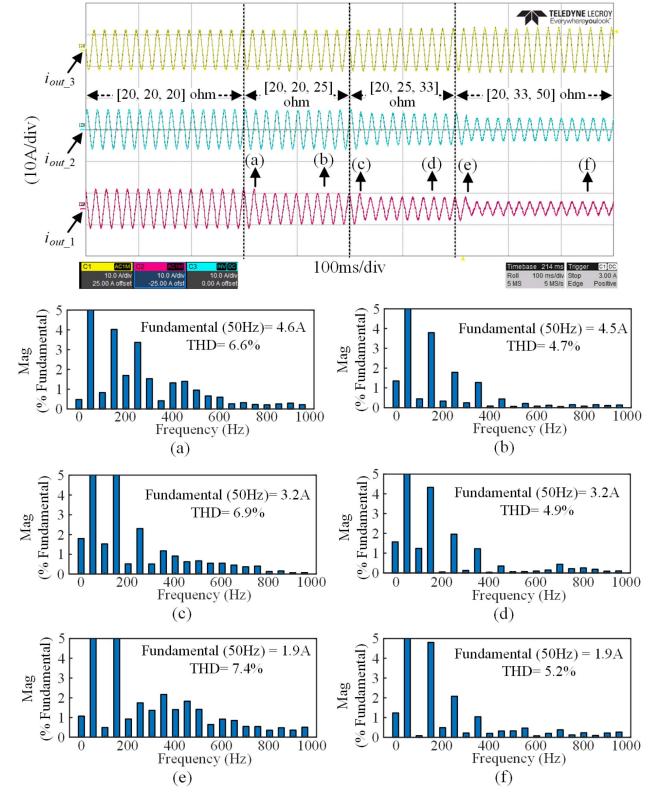


Fig. 14. Experimental output current waveforms and FFT analysis results with load steps and continuous changes. (a) Dynamic range 1. (b) Stable range 1. (c) Dynamic range 2. (d) Stable range 2. (e) Dynamic range 3. (f) Stable range 3. (i_{out_1} , i_{out_2} , and i_{out_3} , respectively, represent the output current of those three drives.)

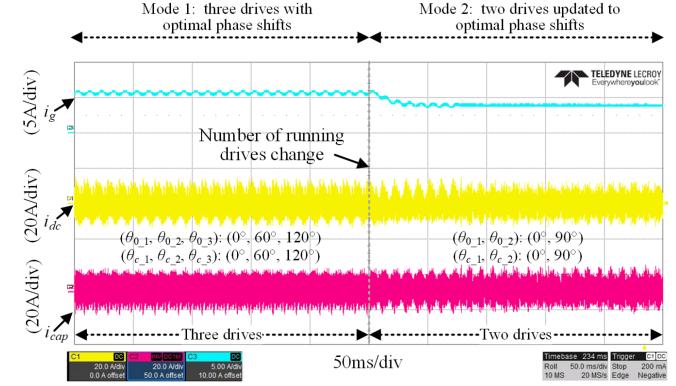


Fig. 15. Experimental current waveforms with switching from three drives to two drives. (i_g —DC-side supply current, i_{dc} —DC bus current; i_{cap} —capacitor ripple current; In Strategy 4 - modulation with proposed optimal phase shifts.).

THD values are given. The (a)–(f) represent the dynamic and stable state of range 1, the dynamic and stable state of range 2, and the dynamic and stable state of range 3, respectively. Comparing the stable and dynamic stages of each range, it can be observed that the continuous modification of the modulation wave and carrier wave forms can also have spectral effects on the output current. During dynamic changes, the THD value is higher than the steady-state stage.

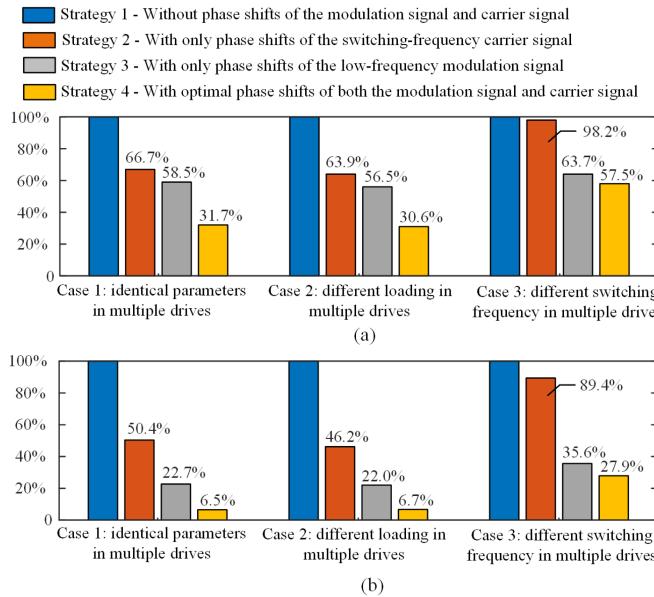


Fig. 16. Comparison of the experimental results of the DC-link capacitor rms current and power loss with different cases and different modulation strategies in the three drives. (a) Comparison of the rms current of DC-link capacitor (b) Comparison of the power loss of DC-link capacitor.

Fig. 15 shows the results under a dynamic change in the number of drives in operation. Before the change, Mode 1 is three drives with optimal phase shifts. Mode 2 is when the third drive is turned OFF, and the phase shifts of the first and the second drives are updated to the optimal ones. In Mode 2, the dc-side supply current i_g reduces from 6.6 to 4.4 A since the load of each drive in operation remains the same. In Mode 2, the controller only needs 2 to 3 fundamental cycles (within 100 ms) to update to the optimal phase shift. The results imply that the performance can be maintained by updating the optimal phase shifts according to the number of drives in operation.

H. Comparison of Experimental Results With Different Cases and Different Modulation Strategies

Fig. 16 compares the capacitor ripple current and power loss under the four different modulation strategies and three cases for three drives system. When identical parameters or different loads are applied in multidrive systems, the proposed modulation scheme can greatly reduce the rms current and power loss of the dc-link capacitor. The results are consistent with the benchmark in Fig. 5. When different switching frequencies are applied in multidrive systems, using the proposed modulation scheme also reduces the rms current and power loss of the dc-link capacitors. Relatively, low-frequency ripple current components have a higher impact on the capacitor loss compared with high-frequency ones due to frequency-dependent ESR values. In Strategy 4, the low-frequency ripple currents are reduced almost to zero. Therefore, from the capacitor power loss perspective, the percentage of reduction is even more significant compared with that of ripple current rms value. In addition, different switching frequencies generate higher current harmonic distributions on the dc side than the identical switching frequency, such as the

harmonic currents at 15 and 45 kHz shown in Fig. 11. Therefore, the larger rms currents and power losses of dc-link capacitors are introduced with different switching frequencies in multiple drives system.

V. CONCLUSION

This article proposes an optimal modulation method for minimizing the ripple current of dc-link capacitors in multidrive systems. Based on the derived analytical model and the calculated scheme, the method can concurrently reduce the low- and high-frequency harmonics of dc-link capacitors and is applicable for systems with different loads, power factors, modulation ratios, and switching frequency in multidrive systems. In the case studies shown in Fig. 5, the rms current of the dc-link capacitors is reduced to 34.3%–15.9% for systems with 2–20 drives, respectively, compared with that without the phase-shift scheme. The rms current and power loss of the dc-link capacitor are reduced to 31.7% and 6.5% with the identical parameters, 30.6% and 6.7% with the different loads, and 57.5% and 27.9% with the different switching frequencies, respectively, for an experimental system with three multidrive based on the proposed method. The performance is also verified under a dynamic change of the load, switching frequency, output frequency, and number of multidrive in operation by updating the phase shifts.

REFERENCES

- [1] D. Kumar, F. Zare, and A. Ghosh, "DC microgrid technology: System architectures, AC grid interfaces, grounding schemes, power quality, communication networks, applications, and standardizations aspects," *IEEE Access*, vol. 5, pp. 12230–12256, 2017.
- [2] A. K. Kaviani, B. Hadley, and B. Mirafzal, "A time-coordination approach for regenerative energy saving in multiaxis motor-drive systems," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 931–941, Feb. 2012.
- [3] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "Impact of interleaving on ac passive components of paralleled three-phase voltage-source converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, May/Jun. 2010.
- [4] "IGBT Slimline Stacks," Semikron, 2022. [Online]. Available: <https://www.semikron.com/products/product-lines/air-cooled-ibt-stacks/semikube-slimline-ibt-stacks.html>
- [5] H. M. Delpino and D. Kumar, "Line harmonics on systems using reduced DC-link capacitors," in *Proc. IEEE 39th Annu. Conf. Ind. Electron.*, 2013, pp. 961–966.
- [6] H. Wang et al., "Lifetime prediction of DC-link capacitors in multiple drives system based on simplified analytical modeling," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 844–860, Jan. 2021.
- [7] D. Kumar, P. W. Wheeler, J. C. Clare, and T.-W. Kim, "Weight/volume effective multi-drive system based on two-stage matrix converter," in *Proc. IEEE 34th Annu. Conf. Ind. Electron.*, 2008, pp. 2782–2787.
- [8] "The benefits of DC-sharing-focus on drives," Danfoss, 2015. [Online]. Available: <https://www.focustrondrives.com/the-benefits-of-dc-sharing/>
- [9] "Vacon NXP common DC bus utilize and redistribute energy efficiently," VACON, 2016. [Online]. Available: https://files.danfoss.com/download/DrivesDKDDPB911A122_NXP_Common_DC_Bus_LR.pdf,
- [10] Z. Ni, Q. Qian, S. Xie, J. Xu, and B. Zeng, "Harmonic suppression and stability enhancement for grid-connected inverters based on UPQC," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 4922–4926.
- [11] H. Wang, C. Li, G. Zhu, Y. Liu, and H. Wang, "Model-based design and optimization of hybrid dc-link capacitor banks," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8910–8925, Sep. 2020.
- [12] B. Yao et al., "Electrothermal stress analysis and lifetime evaluation of DC-link capacitor banks in the railway traction drive system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4269–4284, Aug. 2021.
- [13] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.

- [14] B. Yao, X. Ge, H. Wang, H. Wang, D. Zhou, and B. Gou, "Multitimescale reliability evaluation of DC-link capacitor banks in metro traction drive system," *IEEE Trans. Transport. Electric.*, vol. 6, no. 1, pp. 213–227, Mar. 2020.
- [15] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, Mar. 2008.
- [16] X. Lyu, Y. Li, and D. Cao, "DC-link RMS current reduction by increasing paralleled three-phase inverter module number for segmented traction drive," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 171–181, Mar. 2017.
- [17] J. S. Siva Prasad and G. Narayanan, "Minimization of grid current distortion in parallel-connected converters through carrier interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan. 2014.
- [18] Y. Yang, P. Davari, F. Zare, and F. Blaabjerg, "A DC-link modulation scheme with phase-shifted current control for harmonic cancellations in multidrive applications," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1837–1840, Mar. 2016.
- [19] Y. Yang, P. Davari, Z. Firuz, and F. Blaabjerg, "Enhanced phase-shifted current control for harmonic cancellation in three-phase multiple adjustable speed drive systems," *IEEE Trans. Power Del.*, vol. 32, no. 2, pp. 996–1004, Apr. 2017.
- [20] S. Baburajan et al., "Design of common DC-link capacitor in multiple-drive system based on reduced DC-link current harmonics modulation," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9703–9717, Aug. 2022.
- [21] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley, 2003.
- [22] F. Vasca and L. Iannelli, *Dynamics and Control of Switched Electronic Systems*. London, U.K.: Springer, 2012.
- [23] J. Kennedy and R. Eberhart, "Particle swarm optimization," in *Proc. Int. Conf. Neural Netw.*, 1995, vol. 4, pp. 1942–1948.
- [24] M. Steczek, P. Chudzik, M. Lewandowski, and A. Szlega, "PSO-based optimization of DC-link current harmonics in traction VSI for an electric vehicle," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8197–8208, Oct. 2020.
- [25] Y. Peng, S. Zhao, and H. Wang, "A digital twin based estimation method for health indicators of DC–DC converters," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2105–2118, Feb. 2021.
- [26] T. Xu, F. Gao, X. Wang, and F. Blaabjerg, "A carrier synchronization method for global synchronous pulselwidth modulation application using phase-locked loop," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10720–10732, Nov. 2019.
- [27] J.-S. Kim, D.-H. Kim, J.-H. Lee, and J.-S. Lee, "Smooth pulse number transition strategy considering time delay in synchronized SVPWM," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 2252–2261, Feb. 2023.



Bo Yao (Student Member, IEEE) received the B.Eng. and M.Eng. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2017 and 2020, respectively. He is currently working toward the Ph.D. degree in power electronic with Aalborg University, Aalborg, Denmark.

He is currently a Research Assistant with the Energy Department, Aalborg University, in cooperation with Vestas Wind Systems A/S. His research focuses on reliability evaluation and condition monitoring of power electronic components in power converter systems.

Mr. Yao was the recipient of the Best Paper Award of International Conference on Electrical Machines and Systems in 2019 and the SEMIKRON Young Engineer Award from the European Center for Power Electronics and SEMIKRON Foundation in 2023.



Zhongting Tang (Member, IEEE) was born in Sichuan, China, in 1990. She received the B.S. degree in automation control in 2012, and the Ph.D. degree in control science and engineering from Central South University, Changsha, China, in 2020.

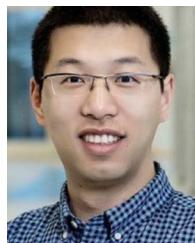
During 2018–2020, she was a Guest Ph.D. Student with AAU Energy, Aalborg University, Aalborg, Denmark, where she is currently a Postdoc with Aalborg University. Her research interests include the topology and modulation technology of the grid-integrated photovoltaics converter and its application and reliability, and closed-loop impedance modeling for generic converters considering the EMI performance.



Dinesh Kumar (Senior Member, IEEE) received the M.Tech. degree in power system engineering from the Indian Institute of Technology Roorkee, Roorkee, India, in 2004, and the Ph.D. degree in power electronics from the University of Nottingham, Nottingham, U.K., in 2010.

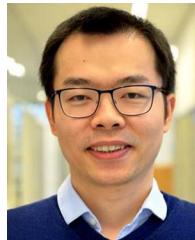
From 2004 to 2005, he was a Lecturer with Electrical Engineering Department, National Institute of Technology, Kurukshetra, India. In 2006, he joined the Chemnitz University of Technology, Chemnitz, Germany, as a Research Fellow in power electronics. Since 2011, he has been with Danfoss Drives A/S, Grasten, Denmark, where he is involved in many research and industrial projects. He is an Adjunct Associate Professor with the School of Electrical Engineering and Robotics, Faculty of Engineering, Queensland University of Technology, Brisbane, QLD, Australia. His current research interests include motor drive, harmonic analysis and mitigation techniques, power quality, and electromagnetic interference in power electronics.

Dr. Kumar is a Member of the IEC standardization Working Group in TC77 A, TC22/SC22 G, and SyC LVDC committee. He is the Editor-in-Chief of *International Journal of Power Electronics* and the Associate Editor for IEEE TRANSACTION ON INDUSTRY APPLICATIONS, IEEE ACCESS, and Member of the Editorial Board of IEEE TRANSPORTATION ELECTRIFICATION eNewsletter. He was the recipient of two IEEE best paper awards.



Haoran Wang (Member, IEEE) received the B.S. and M.S. degrees in control science and engineering from the Wuhan University of Technology, Wuhan, China, in 2012 and 2015, respectively, and the Ph.D. degree in energy technology from the Center of Reliable Power Electronics, Aalborg University, Aalborg, Denmark, in 2018.

From 2013 to 2014, he was a Research Assistant with the Department of Electrical Engineering, Tsinghua University, Beijing, China. From 2017 to 2018, he was a Visiting Scientist with the ETH Zurich, Zurich, Switzerland, and in 2019, he was with Kiel University, Kiel, Germany, and Danfoss Drives A/S, Grasten, Denmark. From 2019 to 2021, he was an Assistant Professor with Aalborg University. He is currently the Vice General Manager with Three Gorges Intelligent Industrial Control Technology Company Ltd., Wuhan, China. His research interests include reliability of electrical and electronic components and systems, multiobjective life-cycle performance optimization of power electronic systems, and reliable clean energy control systems.



Huai Wang (Senior Member, IEEE) received the B.E. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2007, and the Ph.D. degree in power electronics from the City University of Hong Kong, Hong Kong, in 2012.

He is currently a Professor with AAU Energy, Aalborg University, Aalborg, Denmark, where he leads the Group of Reliability of Power Electronic Converters and the mission on Digital Transformation and AI. From August to September 2014, he was a Visiting Scientist with ETH Zurich, Zurich, Switzerland, and from September to November 2013, he was with the Massachusetts Institute of Technology, Cambridge, MA, USA. In 2009, he was with ABB Corporate Research Center, Zurich, Switzerland. His research interests include the fundamental challenges in modeling and validation of power electronic component failure mechanisms and application issues in system-level predictability, condition monitoring, circuit architecture, and robustness design.

Dr. Wang was the recipient of the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society in 2016, and the 1st Prize Paper Award from IEEE TRANSACTIONS ON POWER ELECTRONICS, in 2021. He is an Associate Editor for the *Journal of Emerging and Selected Topics in Power Electronics* and IEEE TRANSACTIONS ON POWER ELECTRONICS.