

A Stress Emulation Method for Concurrent Testing of AC and DC Capacitors

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Abstract—This paper proposes a capacitor testing method that can concurrently emulate the electrical stresses of both AC and DC capacitors for high-power converter applications. It preserves the advantages of a recently reported method with a minimum required power supplies and is robust to testing sample degradation, which, however, limits to test either AC or DC capacitors. The circuit architecture and application examples are presented. Experimental results verify the feasibility and effectiveness of the proposed testing method.

Keywords—Electrical stresses, DC capacitors, AC capacitors, converter applications.

I. INTRODUCTION

Capacitor is one of the highest failure rate components in power electronic systems [1]. The degradation and failure of capacitors could lead to worse filtering capability and over-stresses as well as severe catastrophe to the power converters [2]. The realistic stress testing of capacitors is significant part in the performance characterization and lifetime prediction of capacitors [3] [4].

With the development of power electronics, both DC capacitors and AC capacitors are widely used in power converter systems [5]. The parametric characteristics and reliability testing of both AC capacitor banks and DC capacitor banks cannot be ignored for high power converter applications such as railway and wind power [6] [7]. Therefore, how to cost-effectively simulate electrical stresses for AC and DC capacitors has become an emerging demand for capacitor testing in high power converter applications.

In the last two decades, extensive efforts have been made to generating capacitor testing stress conditions. In [8] and [9], a voltage source and a current source converter are connected in parallel to apply the DC voltage and ripple current, while the converter has to process the full-scale voltage and current of the voltage source. The test stresses level and test frequency of this test method are limited by the power supply capability and cannot be extended, which are only suitable for low-power aluminum electrolytic capacitors and ceramic capacitors testing. The commercial ripple current tester Chroma 11800 and 1120 can simulate different ripple voltage and current according to different extension components [10] [11]. But limited by the size of the hardware, its output ripple current and ripple voltage are only kilowatts. The [12] and [13] use a circuit structure in which a power converter is connected in series with CUTs, and

the ripple current can be configured according to the converter parameters. However, the converter needs to directly withstand the DC voltage component of the CUTs in this method, which cannot be tolerated in the high power capacitor testing with kilovolt DC voltage. Due to the power converters are used in the voltage sources with fixed 120 °C three phase symmetrical voltage, it can improve the test range for electrical stresses, where the ripple voltage, ripple current, and DC voltage of the CUTs can be expand according to test requirements [14] [15]. However, only independent stresses condition of DC capacitors or AC capacitors can be emulated in this testing method.

In general, existing capacitor testing methods still limits to test either AC or DC capacitors for high power applications. This paper propose a stress emulation method for capacitors. This method can concurrently test DC capacitors and AC capacitors, which preserves the advantages of a recently reported method with a minimum required power supplies and is robust to testing sample degradation. In additon, this paper provides a few examples of typical testing scenarios for different power electronics applications, such as wind power converters and railway traction systems.

The structure of this paper is as follows: Section II presents the concept of the test method; Section III gives the test parameters and cases analysis; Experimental verification is given in Section IV, followed by the conclusions.

II. CONCEPT OF PROPOSED STRESS EMULATION METHOD

The circuit architecture of the proposed unified stress emulation method is shown in Fig. 1. It is achieved by decoupling the DC voltage bias generation and AC ripple voltage generator, by the HV supply and LV supply plus the PWM inverter, respectively.

The AC ripple voltage generator mostly consists of the LV power supply that generates ripple voltage and ripple current, the power stack, the AC-side inductor L , the CUTs, the stack resistors R_L and the filter capacitors C_{DCL} . The structure can apply sinusoidal current to the CUTs through the LV power supply and the power stack. The power is circulated in the system, so that the LV supplies the power losses only of the testing system and the DUTs only, implying a minimum current rating.

The HV power supply that generates DC voltage component, the filter capacitors C_{DCH} , and the stack

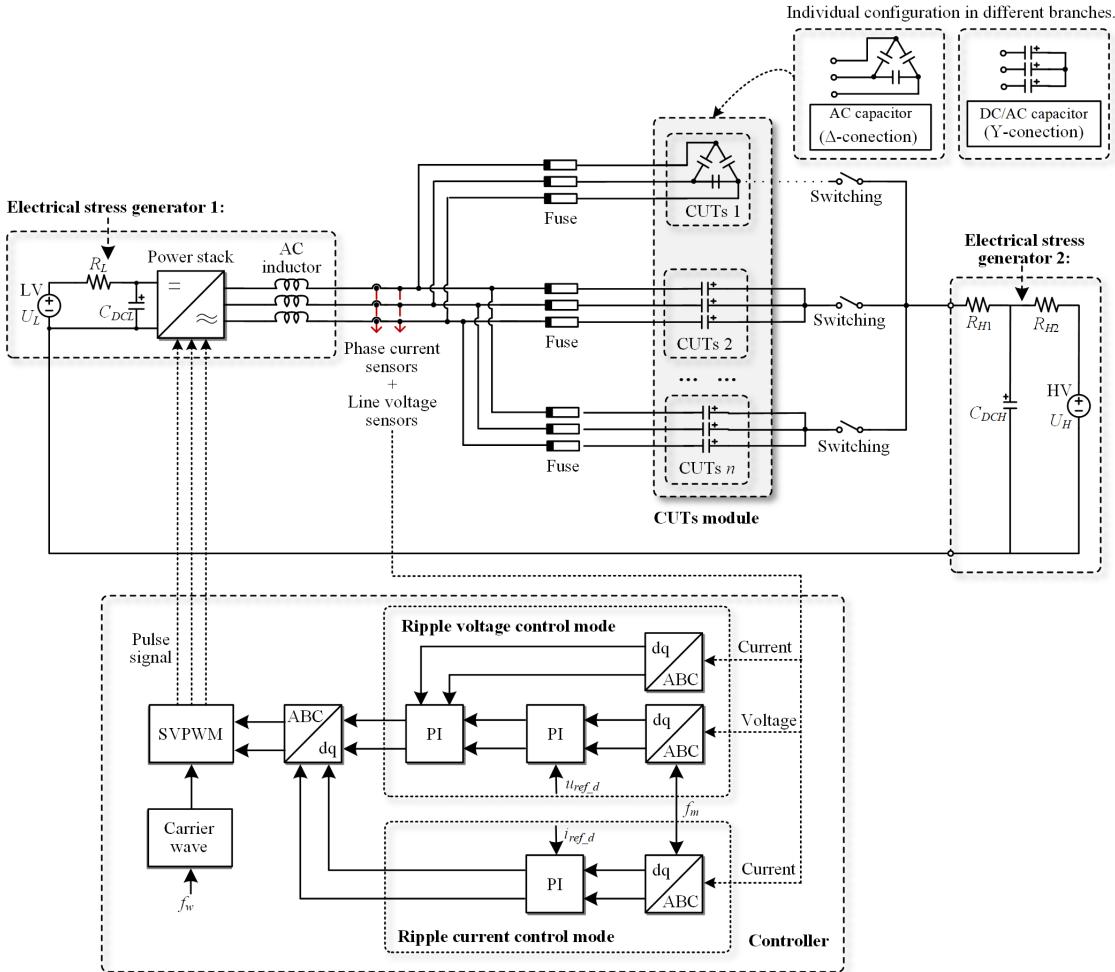


Fig. 1. Circuit architecture of the unified reliability test method.

resistors R_H are added for the DC capacitor test setup. By setting the stack resistors R_H , the current flowing into the circuit of the HV power supply is limited in the DC capacitor test setup. The HV is used to generate DC bias voltage for DC capacitor testing, which supplies typically mA current only.

The CUTs module realizes the function of concurrent AC and DC capacitor testing for different branches. The CUTs can be configured into Y- or Δ -connection for AC capacitors, and Y-connection for DC capacitors, with single or multiple such connections in parallel. The tested ripple voltage and ripple current of the CUTs are provided by the electrical stress generator 1. In DC capacitors testing, the DC component voltage of the CUTs are provided by the electrical stress generator 2. Meanwhile, the fuses are used for short-circuit protection and the switchings are used for turning on or turning off the DC capacitors testing circuit in different branches.

The three-phase SVPWM vector control model is used in the test method, which can be divided into voltage mode to control ripple voltage and current mode to control ripple current. The control system is to modulate the three-phase current with low-frequency sinusoidal waveforms. Through the Park's transformation of

($ABC \Rightarrow dq$), the ripple voltage $u_{Ref,d}$ or ripple current $i_{Ref,d}$, and the modulation frequency f_m are set in the controller. Then performing the Park's inverse transformation ($dq \Rightarrow ABC$), thereby getting the switch signal.

Base on this structure, the proposed method can test the following CUTs:

- Separate AC capacitors testing (Δ / Y-connection);
- Separate DC capacitors testing;
- AC capacitors and DC capacitors concurrently testing.

All of the above testing setup can adopt voltage control mode or current control mode.

III. TEST PARAMETERS AND CASES ANALYSIS

In AC capacitor test setup, the RMS (root mean square) value of ripple voltage U_{ripple} and ripple current I_{ripple} of CUTs can be shown as:

$$\begin{cases} U_{ripple} = U_{line} \\ I_{ripple} = I_{AC} = U_{ripple} \times 2\pi f_R C_{test} \end{cases} \quad (1)$$

where U_{line} , I_{AC} , and C_{test} represent the line voltage between the inductor and CUTs, the AC-side current, and

TABLE I. EXAMPLES OF TYPICAL TESTING SCENARIOS FOR DIFFERENT POWER ELECTRONICS APPLICATIONS

CUTs	Application	Requirement			Design (Minimum required value) (RMS value) ($\eta=96.6\%$)					
		Capacitor parameter (Capacitance/frequency/ Ripple/DC voltage)	Test Number	Scaling factor for rated ripple voltage (RMS)	Power stack output voltage	Power stack and inductor current	Inductance value	Required power (LV)	Power source voltage (HV)	Power source current (HV)
AC	Wind power	75μF/50Hz/730V	9	m=1.4 (1022V)	530V	375A	2.40mF	6830W	-	-
	Railway	416μF/50Hz/600V	4	m=1.4 (840V)	530V	761A	0.75mF	22080W	-	-
DC	Wind power	645μF/50Hz/1250V	24	m=1.4 (280V)	530V	448A	0.15mF	8100W	1250V	<100mA
	Railway	750μF/50Hz/3000V	6	m=1.4 (1189V)	530V	560A	2.5mF	10050W	3375V	<100mA
AC+DC	Railway	416μF/50Hz/600V	4 (AC)	m=1.4 (840V)	530V	1161A	0.72mF	20850W	3375V	<100mA
		750μF/50Hz/3000V	6 (DC)	m=1.0 (840V)						

TABLE II. EXPERIMENTAL PLATFORM PARAMETERS.

CUTs setup	AC capacitor (Δ-conection)	DC capacitor (Y-conection)
AC-side inductor L	2.5mH	
Ripple frequency f_R	50Hz / 60Hz	
Switch frequency f_s	5000Hz	
LV source voltage U_L	750V	
HV source voltage U_H	0V	3375V
Capacitance of CUTs	75μF*3*(9 / 7)	220μF*2
Given ripple voltage (RMS)	730V*1.0/1.2/1.4	730V/√3
Testing Ripple voltage (RMS)	1013V	424V
Testing Ripple current (RMS)	363.2A	58.1A

1. HV source voltage:3375V (3000V DC voltage for DC capacitors + ½ LV voltage)



Fig. 2. Photo of experimental test rig.

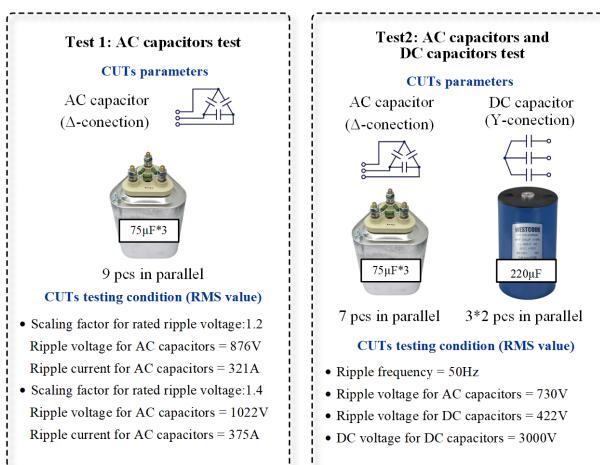


Fig. 3. Setup of AC capacitors and DC capacitors.

the capacitance of the CUTs, respectively. The f_R of the CUTs is ripple frequency of CUTs.

In DC capacitor test setup, the U_{ripple} , I_{ripple} , and the DC component voltage U_{DC} of CUTs can be shown as:

$$\begin{cases} U_{DC} = U_{HV} - \frac{1}{2}U_{LV} \\ U_{ripple} = \frac{1}{\sqrt{3}}U_{line} \\ I_{ripple} = I_{AC} = U_{ripple} \times 2\pi f_R C_{test} \end{cases} \quad (2)$$

where U_{HV} and U_{LV} respectively represent the output voltage of HV power supply and LV power supply.

The RMS value of ripple current I_{ripple} of the DC capacitors and AC capacitors are given by:

$$I_{ripple} = \frac{U_m}{\sqrt{3} | \frac{1}{2\pi f_R \times C_{test}} - 2\pi f_R \times L |} \quad (3)$$

where L is the inductance of the AC-side inductor, and U_m is the RMS value of the output voltage in the power stack.

The AC-side inductor can boost the output voltage of the power stack, and its minimum value can be given as:

$$L = \left(1 - \frac{U_m}{U_{ripple}} \right) \times \frac{1}{4\pi^2 f_R^2 C_{test}} \quad (4)$$

The power requirement of the LV power supply P_{LV} can be given as:

$$P_{LV} \approx I_{ripple}^2 R_{total} + (1 - \eta) I_{ripple} U_m \quad (5)$$

where the η and the R_{total} represent the total operation efficiency of the converter and inductors, and the ESR of the total CUTs, respectively.

Based on the above analysis, according to the test requirements of capacitors in different high power applications, the design parameters of the power stack, the AC-side inductor, and the power supplies in this testing method can be obtained. A few examples of typical testing scenarios for different power electronics applications are given in Table I [5] [7].

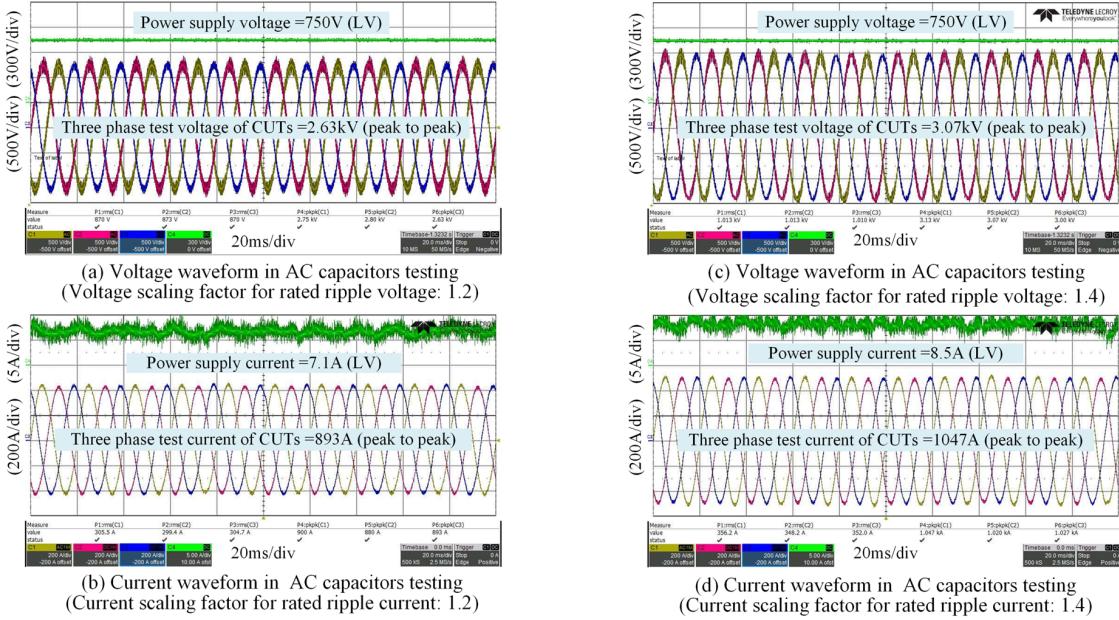


Fig. 4. Experiment results for AC capacitors testing with different ripple voltage scaling factors.

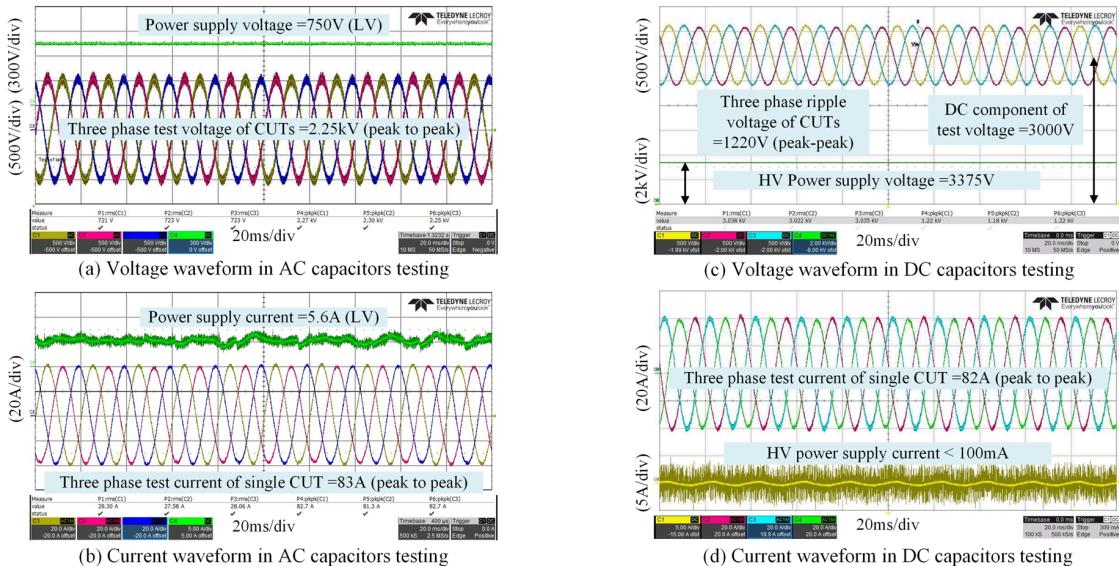


Fig. 5. Experiment results for DC capacitors and AC capacitors concurrently testing.

IV. EXPERIMENTAL VERIFICATION

A. Settings and parameters of the experiment

In order to verify the rationality of the proposed test method, this section analyzes the test performance through a full scale experimental platform. The experimental platform is shown in Fig. 2. The control system is carried out through the RTbox controller, and the power stack uses the Semikron slimLine platform [16]. In addition, the output power of the LV power supply is set to 750V. The output power of the HV power supply is set to 3350V, so that the DC voltage of the DC capacitor is 3000V. The main parameters of the experimental platform and the CUTs are given in Table II and Fig. 3, where CUTs include AC capacitors and DC capacitors.

B. AC capacitor banks testing with with different ripple voltage scaling factor

The test results of AC capacitor are shown in Fig. 4. It shows the ripple voltage and ripple current of the three-phase CUTs as well as the output voltage and current of the LV power supply. In this testing, the CUTs are 9 Δ -connection AC capacitors in parallel. The 1.2 and 1.4 scaling factor for rated ripple voltage are emulated for CUTs, as shown in Fig.4 (a)-(b) and Fig.4 (c)-(d), respectively. It can be seen from the results that by setting different ripple voltages and ripple currents, different stress testing requirements can be met. When keeping the constant LV voltage (750V), the LV current that needs to be provided increase accordingly. In the Fig.5 (c)-(d), the total testing power of the CUTs reaches 3.2 MVA, while

the LV power supply only needs to provide 6.4 kW of power.

C. Concurrent testing of AC and DC capacitors

The test results of the unified DC capacitor and AC capacitor are shown in Fig. 5. It shows the three-phase ripple voltage and ripple current of the DC capacitors and the AC capacitors, and the DC voltage component of the DC capacitors, as well as the output voltage and current of the HV power supply. In this testing, the CUTs are 7 Δ-connection AC capacitors and 6 Y-connection DC capacitors in parallel. The same ripple voltage is applied to the AC capacitors and the DC capacitors, as shown in Fig. 5 (a)-(b) and Fig. 5 (c)-(d), respectively. It can be seen from the results that the ripple voltage and current of the test capacitor are also stable when AC capacitors and DC capacitors are mixed testing. Meanwhile, the HV source only needs to provide the mA current.

V. CONCLUSION

This paper proposes a stress emulation method for high-power capacitors, which is able to concurrently emulate realistic electrical stresses of DC and AC capacitors with high ripple voltage (kV) and high ripple current (kA). This concurrently and parallel testing method can reduce the testing time and testing cost. It is suitable for the application-oriented testing of DC and AC capacitors, including the accelerated aging testing, the fault physics analysis, and the lifetime prediction, especially for capacitors testing in high-power (MW) applications such as railway traction systems and wind power systems. Examples of typical testing scenarios for different power electronics applications illustrate the practicability of this method in the high power converter application cases, such as wind power converters and railway traction systems, which is convenient for laboratory and industrial implementation. The full scale experiments verify the concept of the proposed method for DC capacitors and AC capacitors testing.

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