TEXAS INSTRUMENTS
MCT8316Z
SLVSF18 – MARCH 2021

MCT8316Z Sensored Trapezoidal Integrated FET BLDC Motor Driver

1 Features

- Three-phase BLDC motor driver with Sensored Trapezoidal control
- 4.5-V to 35-V operating voltage (40-V abs max)
- High output current capability: 8-A Peak
- Low MOSFET on-state resistance
  - 100-mΩ $R_{DS(ON)}$ (HS + LS) at T_A = 25°C
- Low power sleep mode
  - 1.5-µA at V_{VM} = 24-V, T_A = 25°C
- Configurable PWM modulation: Synchronous/ Asynchronous
- Supports Analog or Digital Hall inputs
- Supports 200-kHz PWM frequency
- Cycle-by-cycle current limit
- Integrated built-in current sense
  - Doesn't require external current sense resistors
- Hardware or 5-MHz 16-bit SPI interface
- Supports 1.8-V, 3.3-V, and 5-V logic inputs
- Built-in 3.3-V (5%), 30-mA LDO regulator
- Built-in 3.3-V/5-V, 200-mA buck regulator
- Delay compensation reduces duty cycle distortion
- Suite of integrated protection features
  - Supply undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Motor lock protection
  - Thermal warning and shutdown (OTW/OTSD)
  - Fault condition indication pin (nFAULT)
  - Optional fault diagnostics over SPI interface

2 Applications

- Brushless-DC (BLDC) Motor Modules
- Small home appliances
- HVAC motors
- Office automation machines
- Factory automation and robotics
- Automotive LIDAR

3 Description

The MCT8316Z provides a single-chip code-free sensored trapezoidal solution for customers driving 12- to 24-V brushless-DC motors.

The MCT8316Z integrates three 1/2-H bridges with 40-V absolute maximum capability and a very low RDS(ON) of100 mOhms (high-side and low-side combined) to enable high power drive capability. Current is sensed using an integrated current sensing feature which eliminates the need for external sense resistors. Power management features of an adjustable buck regulator and LDO generate the necessary voltage rails for the device and can be used to power external circuits.

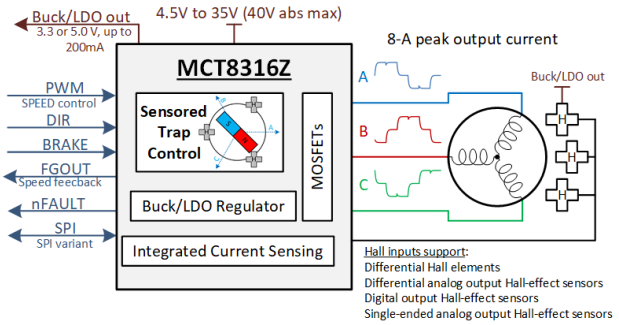
MCT8316Z implements sensored trapezoidal control, and so an external microcontroller is not required to spin the brushless-DC motor. The algorithm is implemented in a fixed-function state machine, so no coding is needed. The device integrates three analog hall comparators for position sensing to achieve sensored trapezoidal BLDC motor control. The control scheme is highly configurable through hardware pins or register settings ranging from motor current limiting behavior to fault response. The speed can be controlled through a PWM input.

There are a large number of protection features integrated into the MCT8316Z, intended to protect the device, motor, and system against fault events.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MCT8316ZR(2)	VQFN (40)	7.00 mm × 5.00 mm
MCT8316ZT	VQFN (40)	7.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Device available for preview only.



Simplified Schematic

ADVANCE INFORMATION

Table of Contents

4 Revision History

DATE	REVISION	NOTES
March 2021	*	Initial release.

5 Device Comparison Table

DEVICE	PACKAGES	INTERFACE	BUCK REGULATOR
MCT8316ZR(1)	40-pin VQFN (7x5 mm)	SPI	Yes
MCT8316ZT		Hardware	

(1) Device available for preview only.

Table 5-1. MCT8316ZR (SPI variant) vs. MCT8316ZT (Hardware variant) configuration comparison

Parameters	MCT8316ZR (SPI variant)	MCT8316ZT (Hardware variant)
PWM control mode settings	PWM_MODE (4 settings)	MODE pin (7 settings)
Slew rate settings	SLEW (4 settings)	SLEW pin (4 settings)
Direction settings	DIR (2 settings)	DIR pin (2 settings)
DRVOFF pin configuration	DRV_OFF (2 settings)	Enabled
Current limit threshold	ILIMIT pin: AVDD/2 to AVDD/2-0.4V	ILIMIT pin: AVDD/2 to AVDD/2-0.4V
Current limit configuration	ILIM_RECIR (2 settings), PWM_100_DUTY_SEL	Recirculation fixed to Brake mode and PWM frequency for 100% duty fixed to 20 kHz
CSA GAIN	CSA_GAIN (4 settings)	Fixed to 0.15 V/A
Lead angle settings	ADVANCE_LVL (8 settings)	ADVANCE pin (7 settings)
Buck enable	BUCK_DIS (2 settings)	Enabled
Buck threshold	BUCK_SEL(4 settings)	VSEL_BK pin (4 settings)
Buck configuration: power sequencing, current limit and slew rate	BUCK_PS_DIS (2 settings), BUCK_CL(2 settings) and BUCK_SR (2 settings)	Power sequencing enabled, current limit: 600 mA and slew rate: 1000 V/us
FGOUT configuration	FGOUT_SEL (4 settings)	Fixed to commutation frequency
Motor lock configuration: mode, detection and retry timing	MTR_LOCK_MODE (4 settings), MTR_LOCK_TDET (4 settings), MTR_LOCK_RETRY (2 settings)	Enabled with latched shutdown mode and detection time of 1000 ms
Active demagnetization	EN_AAR (2 settings) and EN_ASR (2 settings)	MODE pin (7 settings)
OCP configuration: Mode,	OCP_MODE (4 settings) , OCP_LVL (4 settings) ,OCP_DEG (4 settings) and OCP_RETRY (2 settings)	Enabled with latched shutdown mode, level is fixed to 16A with 0.6 us deglitch time
Overvoltage protection configuration	OVP_EN (2 settings) , OVP_SEL (2 settings)	Enabled and level is fixed to 34V (typ)
Driver delay compensation configuration	DLYCMP_EN (2 settings), DLY_TARGET (16 settings)	Disabled
SDO pin configuration	SDO_MODE (2 settings)	NA
SPI fault configuration	SPI_PARITY(2 settings), SPI_SCLK_FLT(2 settings), SPI_ADDR_FLT(2 settings)	NA

ADVANCE INFORMATION

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6 Pin Configuration and Functions

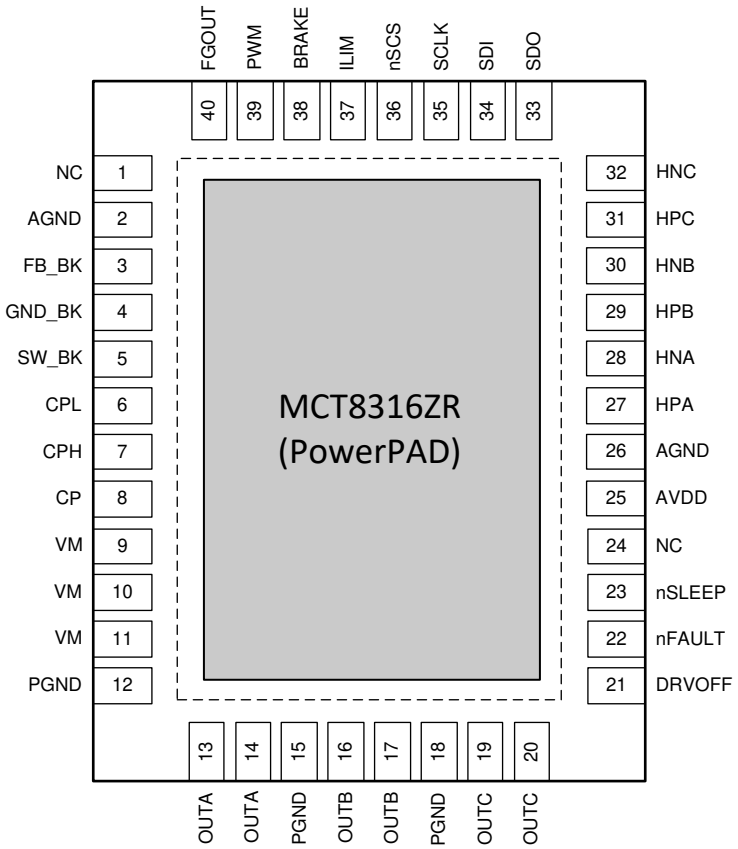


Figure 6-1. MCT8316ZR 40-Pin VQFN With Exposed Thermal Pad Top View

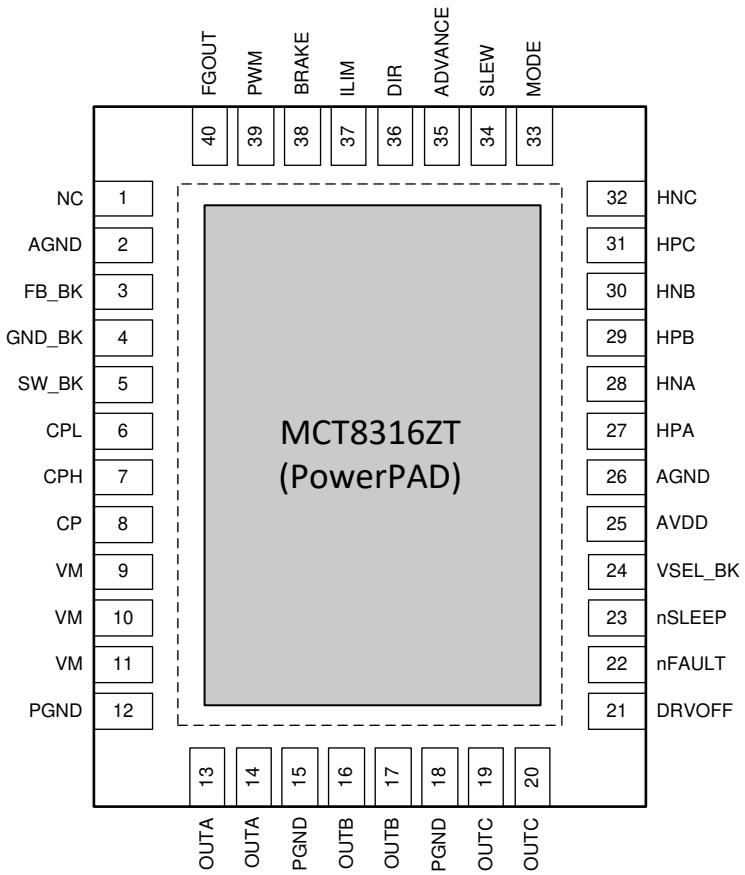


Figure 6-2. MCT8316ZT 40-Pin VQFN With Exposed Thermal Pad Top View

ADVANCE INFORMATION

Pin Functions

PIN	40-pin Package		TYPE[1]	DESCRIPTION
NAME	MCT8316ZR	MCT8316ZT		
ADVANCE	—	35	I	OCP level setting. This pin is a 2-level input pin set by an external resistor (Hardware devices).
AGND	2, 26	2, 26	PWR	Device analog ground. Connect to system ground.
AVDD	25	25	PWR	3.3-V internal regulator output. Connect an X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 30 mA externally.
BRAKE	38	38	I	Causes motor to brake by turning all low side MOSFETs ON. Internal pulldown resistor.
CP	8	8	PWR	Charge pump output. Connect an X5R or X7R, 1-µF, 16-V ceramic capacitor between the VCP and VM pins.
CPH	7	7	PWR	Charge pump switching node. Connect an X5R or X7R,10-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
CPL	6	6	PWR	Charge pump switching node. Connect an X5R or X7R,10-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
DIR	—	36	I	Direction pin for setting the direction of the motor rotation to clockwise or counterclockwise. Internal pulldown resistor (Hardware devices).
DRVOFF	21	21	I	Disables all six MOSFETs.
FB_BK	3	3	PWR	Feedback for buck regulator. Connect output of buck regulator to this pin.
FGOUT	40	40	O	Outputs a frequency proportional to motor commutation speed.
GND_BK	4	4	PWR	Buck regulator ground. Connect to system ground.
HPA	27	27	I	Phase A hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HPB	29	29	I	Phase B hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HPC	31	31	I	Phase C hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HNA	28	28	I	Phase A hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HNB	30	30	I	Phase B hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HNC	32	32	I	Phase C hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
ILIM	37	37	I	Set the threshold for phase current used in cycle by cycle current limit.
MODE	—	33	I	PWM input mode setting. This pin is a 2-level input pin set by an external resistor (Hardware devices).
NC	1, 24	1	—	No Connect.
nFAULT	22	22	O	Fault indication pin. Pulled logic-low with fault condition; open-drain output requires an external pullup.
nSCS	36	—	I	Serial chip select. A logic low on this pin enables serial interface communication (SPI devices).
nSLEEP	23	23	I	Driver nSLEEP. When this pin is logic low, the device goes into a low-power sleep mode. An 8 to 40-µs low pulse can be used to reset fault conditions.
OUTA	13, 14	13, 14	O	Half bridge output A
OUTB	16, 17	16, 17	O	Half bridge output B
OUTC	19, 20	19, 20	O	Half bridge output C
PGND	12, 15, 18	12, 15, 18	PWR	Device power ground. Connect to system ground.
PWM	39	39	I	PWM input for motor control. Set the output voltage and switching frequency of the phase voltage of the motor.
SCLK	35	—	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin (SPI devices).

ADVANCE INFORMATION

PIN	40-pin Package		TYPE(1)	DESCRIPTION
NAME	MCT8316ZR	MCT8316ZT		
SDI	34	—	I	Serial data input. Data is captured on the falling edge of the SCLK pin (SPI devices).
SDO	33	—	O	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor (SPI devices).
SLEW	—	34	I	Slew rate control setting. This pin is a 4-level input pin set by an external resistor (Hardware devices).
SW_BK	5	5	PWR	Buck switch node. Connect this pin to an inductor or resistor.
VM	9, 10, 11	9, 10, 11	PWR	Power supply. Connect to motor supply voltage; bypass to GND with two 0.1-µF capacitors (for each pin) plus one bulk capacitor rated for VM.
VSEL_BK	—	24	I	Buck output voltage setting. This pin is a 4-level input pin set by an external resistor (Hardware devices).
Thermal pad			PWR	Must be connected to ground.

(1) I = input, O = output, PWR = power, NC = no connect

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply pin voltage (VM)	–0.3	40	V
Power supply voltage ramp (VM)		4	V/µs
Voltage difference between ground pins (GND_BK, PGND, AGND)	–0.3	0.3	V
Charge pump voltage (CPH, CP)	–0.3	V_M + 6	V
Charge pump negative switching pin voltage (CPL)	–0.3	V_M + 0.3	V
Switching regulator pin voltage (FB_BK)	–0.3	5.75	V
Switching node pin voltage (SW_BK)	–0.3	V_M + 0.3	V
Analog regulators pin voltage (AVDD)	–0.3	5.75	V
Logic pin input voltage (DRVOFF, INHx, INLx, nSCS, nSLEEP, SCLK, SDI)	–0.3	5.75	V
Logic pin output voltage (nFAULT, SDO)	–0.3	5.75	V
Output pin voltage (OUTA, OUTB, OUTC)	–1	V_M + 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage tempertaure, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	V_{VM}	4.5	24	35	V
f_{PWM}	Output PWM frequency	OUTA, OUTB, OUTC			200	kHz
I_{OUT} (1)	Peak output winding current	OUTA, OUTB, OUTC			8	A
V_{IN}	Logic input voltage	DRVOFF, INHx, INLx, nSCS, nSLEEP, SCLK, SDI	–0.1		5.5	V
V_{OD}	Open drain pullup voltage	nFAULT, SDO	–0.1		5.5	V
V_{SDO}	Push-pull voltage	SDO	2.2		5.5	V
I_{OD}	Open drain output current	nFAULT, SDO			5	mA
V_{VREF}	Voltage reference pin voltage	VREF	2.8		AVDD	V
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating Junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC(1)		MCT8316ZT, MCT8316ZR VQFN (RGF) 40 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMQ}	VM sleep mode current	V_{VM} > 6 V, nSLEEP = 0, T_A = 25 °C		1.5	2.5	µA
		nSLEEP = 0		2.5	5	µA
I_{VMS}	VM standby mode current (Buck regulator disabled)	nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', BUCK_DIS = 1;		4	10	mA
		V_{VM} > 6 V, nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', T_A = 25 °C, BUCK_DIS = 1;		4	5	mA
I_{VMS}	VM standby mode current (Buck regulator enabled)	V_{VM} > 6 V, nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', I_{BK} = 0, T_A = 25 °C, BUCK_DIS = 0;		5	6	mA
		nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', I_{BK} = 0, BUCK_DIS = 0;		6	10	mA
I_{VM}	VM operating mode current (Buck regulator disabled)	V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 25 kHz, T_A = 25 °C, BUCK_DIS = 1		10	13	mA
		V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 200 kHz, T_A = 25 °C, BUCK_DIS = 1		18	21	mA
		nSLEEP =1, f_{PWM} = 25 kHz, BUCK_DIS = 1		12	15	mA
		nSLEEP =1, f_{PWM} = 200 kHz, BUCK_DIS = 1		17	27	mA
I_{VM}	VM operating mode current (Buck regulator enabled)	V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 25 kHz, T_A = 25 °C, BUCK_DIS = 0; BUCK_PS_DIS = 0		10.8	12	mA
		V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 200 kHz, T_A = 25 °C, BUCK_DIS = 0; BUCK_PS_DIS = 0		18.5	22	mA
V_{AVDD}	Analog regulator voltage	0 mA ≤ I_{AVDD} ≤ 30 mA; BUCK_PS_DIS = 0	3.135	3.3	3.465	V
I_{AVDD}	External analog regulator load				30	mA
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM		4.7		V
f_{CP}	Charge pump switching frequency			400		kHz
t_{PWM_LOW}	PWM low time required for motor lock detection			200		ms
t_{WAKE}	Wakeup time	V_{VM} > V_{UVLO}, nSLEEP = 1 to outputs ready and nFAULT released			1	ms

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SLEEP}	Sleep Pulse time	nSLEEP = 0 period to enter sleep mode	120			µs
t_{RST}	Reset Pulse time	nSLEEP = 0 period to reset faults	20		40	µs
BUCK REGULATOR						
V_{BK}	Buck regulator average voltage (L_{BK} = 47 µH, C_{BK} = 22 µF) (SPI Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b) or V_{VM} < 6.0 V (BUCK_SEL = 11b), 0 mA ≤ I_{BK} ≤ 200 mA		V_{BK}– I_{BK}*(R_{LBK}+ 2)		V
V_{BK}	Buck regulator average voltage (L_{BK} = 22 µH, C_{BK} = 22 µF) (SPI Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b) or V_{VM} < 6.0 V (BUCK_SEL = 11b), 0 mA ≤ I_{BK} ≤ 50 mA		V_{BK}– I_{BK}*(R_{LBK}+ 2)		V
V_{BK}	Buck regulator average voltage (R_{BK} = 22 Ω, C_{BK} = 22 µF) (SPI Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b) or V_{VM} < 6.0 V (BUCK_SEL = 11b), 0 mA ≤ I_{BK} ≤ 40 mA		V_{BK}– I_{BK}*(R_{BK}+2)		V
V_{BK}	Buck regulator average voltage (L_{BK} = 47 µH, C_{BK} = 22 µF) (HW Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, VSEL_BK pin tied to AGND	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, VSEL_BK pin to Hi-Z	4.6	5.0	5.4	
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, VSEL_BK pin to 47 kΩ +/- 5% tied to AVDD	3.7	4.0	4.3	
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 200 mA, VSEL_BK pin to AGND	5.2	5.7	6.2	
		V_{VM} < 6.0 V, 0 mA ≤ I_{BK} ≤ 200 mA		V_{BK}– I_{BK}*(R_{LBK}+ 2)		V

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BK}	Buck regulator average voltage (L_{BK} = 22 µH, C_{BK} = 22 µF) (HW Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, VSEL_BK pin tied to AGND	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, VSEL_BK pin to Hi-Z	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, VSEL_BK pin to 47 kΩ +/- 5% tied to AVDD	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 50 mA, VSEL_BK pin to AGND	5.2	5.7	6.2	V
		V_{VM} < 6.0 V, 0 mA ≤ I_{BK} ≤ 50 mA		V_{BK}– I_{BK}*(R_{LBK}+ 2)		V
V_{BK}	Buck regulator average voltage (R_{BK} = 22 Ω, C_{BK} = 22 µF) (HW Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, VSEL_BK pin tied to AGND	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, VSEL_BK pin to Hi-Z	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, VSEL_BK pin to 47 kΩ +/- 5% tied to AVDD	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 40 mA, VSEL_BK pin to AGND	5.2	5.7	6.2	V
		V_{VM} < 6.0 V, 0 mA ≤ I_{BK} ≤ 40 mA		V_{BK}– I_{BK}*(R_{BK}+2)		V
V_{BK_RIP}	Buck regulator ripple voltage	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, Buck regulator with inductor, L_{BK} = 47 uH, C_{BK} = 22 µF	–100		100	mV
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, Buck regulator with inductor, L_{BK} = 22 uH, C_{BK} = 22 µF	–100		100	mV
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, Buck regulator with resistor; R_{BK} = 22 Ω, C_{BK} = 22 µF	–100		100	mV
I_{BK}	External buck regulator load	L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			200	mA
		L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			200 – I_{AVDD}	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			50	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			50 – I_{AVDD}	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			40	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			40 – I_{AVDD}	mA
BUCK_SR	Buck slew rate (SPI Device)	BUCK_SR = 0b		1000		V/us
		BUCK_SR = 1b		200		V/us
	Buck slew rate (HW Device)			1000		V/us
f_{SW_BK}	Buck regulator switching frequency	Regulation Mode	TBD		535	kHz
		Linear Mode	0		535	kHz

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BK_UV}	Buck regulator undervoltage lockout (SPI Device)	V_{BK} rising, BUCK_SEL = 00b	2.7	2.8	2.9	V
		V_{BK} falling, BUCK_SEL = 00b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 01b	4.3	4.4	4.5	V
		V_{BK} falling, BUCK_SEL = 01b	4.1	4.2	4.3	V
		V_{BK} rising, BUCK_SEL = 10b	2.7	2.8	2.9	V
		V_{BK} falling, BUCK_SEL = 10b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 11b	4.3	4.4	4.5	V
		V_{BK} falling, BUCK_SEL = 11b	4.1	4.2	4.3	V
V_{BK_UV}	Buck regulator undervoltage lockout (HW Device)	V_{BK} rising, VSEL_BK pin tied to AGND	2.7	2.8	2.9	V
		V_{BK} falling, VSEL_BK pin tied to AGND	2.5	2.6	2.7	V
		V_{BK} rising, VSEL_BK pin to 47 kΩ +/- 5% tied to AVDD	4.3	4.4	4.5	V
		V_{BK} falling, VSEL_BK pin to 47 kΩ +/- 5% tied to AVDD	4.1	4.2	4.3	V
		V_{BK} rising, VSEL_BK pin to Hi-Z	2.7	2.8	2.9	V
		V_{BK} falling, VSEL_BK pin to Hi-Z	2.5	2.6	2.7	V
		V_{BK} rising, VSEL_BK pin tied to AVDD	4.3	4.4	4.5	V
		V_{BK} falling, VSEL_BK pin tied to AVDD	4.1	4.2	4.3	V
$V_{BK\_UV\_HYS}$	Buck regulator undervoltage lockout hysteresis	Rising to falling threshold		200		mV
I_{BK_CL}	Buck regulator Current limit threshold (SPI Device)	BUCK_CL = 0b		600		mA
		BUCK_CL = 1b		150		mA
I_{BK_CL}	Buck regulator Current limit threshold (HW Device)			600		mA
I_{BK_OCP}	Buck regulator Overcurrent protection trip point		2	3	4	A
t_{BK_RETRY}	Overcurrent protection retry time			1		ms
LOGIC-LEVEL INPUTS (BRAKE, DIR, DRVOFF, nSLEEP, PWM, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage	Other Pins	1.5		5.5	V
		nSLEEP	1.6		5.5	V
V_{HYS}	Input logic hysteresis	Other PIns	180	300	420	mV
		nSLEEP	95	250	420	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–1		1	µA
I_{IH}	Input logic high current	nSLEEP, V_{PIN} (Pin Voltage) = 5 V	15		30	µA
		Other pins, V_{PIN} (Pin Voltage) = 5 V	30		75	µA
R_{PD}	Input pulldown resistance	nSLEEP	150	200	300	kΩ
		Other pins	70	100	130	kΩ
C_{ID}	Input capacitance			30		pF
LOGIC-LEVEL INPUTS (nSCS)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis		180	300	420	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V			75	µA
I_{IH}	Input logic high current	V_{PIN} (Pin Voltage) = 5 V	–1		25	µA
R_{PU}	Input pullup resistance		80	100	130	kΩ
C_{ID}	Input capacitance			30		pF

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FOUR-LEVEL INPUTS (SLEW, VSEL_BK)						
V_{L1}	Input mode 1 voltage	Tied to AGND	0		0.2*AVDD	V
V_{L2}	Input mode 2 voltage	Hi-Z	0.27*AVDD	0.5*AVDD	0.545*AVDD	V
V_{L3}	Input mode 3 voltage	47 kΩ +/- 5% tied to AVDD	0.606*AVDD	0.757*AVDD	0.909*AVDD	V
V_{L4}	Input mode 4 voltage	Tied to AVDD	0.94*AVDD		AVDD	V
R_{PU}	Input pullup resistance	To AVDD	70	100	130	kΩ
R_{PD}	Input pulldown resistance	To AGND	70	100	130	kΩ
SEVEN-LEVEL INPUTS (ADVANCE and MODE)						
V_{L1}	Input mode 1 voltage	Tied to AGND	0		0.09*AVDD	V
V_{L2}	Input mode 2 voltage	22 kΩ ± 5% to AGND	0.12*AVDD	0.15*AVDD	0.2*AVDD	V
V_{L3}	Input mode 3 voltage	100 kΩ ± 5% to AGND	0.27*AVDD	0.33*AVDD	0.4*AVDD	V
V_{L3}	Input mode 3 voltage	Hi-Z	0.45*AVDD	0.5*AVDD	0.55*AVDD	V
V_{L5}	Input mode 5 voltage	100 kΩ ± 5% to AVDD	0.6*AVDD	0.66*AVDD	0.73*AVDD	V
V_{L6}	Input mode 6 voltage	22 kΩ ± 5% to AVDD	0.77*AVDD	0.85*AVDD	0.9*AVDD	V
V_{L4}	Input mode 3 voltage	Tied to AVDD	0.94*AVDD		AVDD	V
R_{PU}	Input pullup resistance	To AVDD		100		kΩ
R_{PD}	Input pulldown resistance	To AGND		100		kΩ
OPEN-DRAIN OUTPUTS (FGOUT, nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OH}	Output logic high current	V_{OD} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
PUSH-PULL OUTPUTS (SDO)						
V_{OL}	Output logic low voltage	I_{OP} = 5 mA	0		0.4	V
V_{OH}	Output logic high voltage	I_{OP} = 5 mA	2.2		5.5	V
I_{OL}	Output logic low leakage current	V_{OP} = 0 V	–1		1	µA
I_{OH}	Output logic high leakage current	V_{OP} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
DRIVER OUTPUTS						
$R_{DS(ON)}$	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		100		mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		105		mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_J = 150 °C		130		mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_J = 150 °C		130		mΩ

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND		25		V/us
		V_{VM} = 24 V, SLEW = 01b or SLEW pin to Hi-Z		50		V/us
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 47 kΩ +/- 5% to AVDD		125		V/us
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to AVDD		200		V/us
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND		25		V/us
		V_{VM} = 24 V, SLEW = 01b or SLEW pin to Hi-Z		50		V/us
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 47 kΩ +/- 5% to AVDD		125		V/us
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to AVDD		200		V/us
I_{LEAK}	Leakage current on OUTx	V_{OUTx} = V_{VM}, nSLEEP = 1			5	mA
	Leakage current on OUTx	V_{OUTx} = 0 V, nSLEEP = 1			1	µA
t_{DEAD}	Output dead time (high to low / low to high)	V_{VM} = 24 V, SR = 25 V/µs, HS driver ON to LS driver OFF		2500	3400	ns
		V_{VM} = 24 V, SR = 50 V/µs, HS driver ON to LS driver OFF		1200	1550	ns
		V_{VM} = 24 V, SR = 125 V/µs, HS driver ON to LS driver OFF		750	1000	ns
		V_{VM} = 24 V, SR = 200 V/µs, HS driver ON to LS driver OFF		500	750	ns
t_{PD}	Propagation delay (high-side / low-side ON/OFF)	V_{VM} = 24 V, INHx = 1 to OUTx transisition, SR = 25 V/µs		3000	3500	ns
		V_{VM} = 24 V, INHx = 1 to OUTx transisition, SR = 50V/µs		1300	1700	ns
		V_{VM} = 24 V, INHx = 1 to OUTx transisition, SR = 125 V/µs		950	1100	ns
		V_{VM} = 24 V, INHx = 1 to OUTx transisition, SR = 200 V/µs		700	900	ns
t_{MIN_PULSE}	Minimum output pulse width	SR = 200 V/µs	600			ns
HALL COMPARATORS						
V_{ICM}	Input Common Mode Voltage (Hall)		0.5		AVDD – 1.2	V
V_{HYS}	Voltage hysteresis (SPI Device)	HALL_HYS = 0	3.5	5	7.5	mV
		HALL_HYS = 1	35	50	75	mV
	Voltage hysteresis (HW Device)		3.5	5	7.5	mV
ΔV_{HYS}	Hall comparator hysteresis difference	Between Hall A, Hall B and Hall C comparator	–5		5	mV
$V_{H(MIN)}$	Minimum Hall Differential Voltage		40			mV
I_I	Input leakage current	HPX = HNX = 0 V	–1		1	µA
t_{HDG}	Hall deglitch time		1.1	1.15	1.2	µs
t_{HEDG}	Hall Enable deglitch time	During Power up		5	TBD	µs
PULSE-BY-PULSE CURRENT LIMIT						
V_{LIM}	Voltage on VLIM pin for cycle by cycle current limit		AVDD/2		AVDD/2–0.4	V
I_{LIMIT}	Current limit corresponding to VLIM pin voltage range		0		8	A

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIMIT}	Current limit corresponding to VLIM pin voltage range		0		5	A
I_{LIM_AC}	Current limit accuracy		–10		10	%
t_{BLANK}	Cycle by cycle current limit blank time			5		µs
ADVANCE ANGLE						
θ_{ADV}	Advance Angle Setting (SPI Device)	ADVANCE_LVL = 000 b		0°		V
		ADVANCE_LVL = 001 b		4°		V
		ADVANCE_LVL = 010 b		7°		V
		ADVANCE_LVL = 011 b		11°		V
		ADVANCE_LVL = 100 b		15°		V
		ADVANCE_LVL = 101 b		20°		V
		ADVANCE_LVL = 110 b		25°		V
		ADVANCE_LVL = 111 b		30°		V
θ_{ADV}	Advance Angle Setting (HW Device)	Advance pin tied to AGND		0°		V
		Advance pin tied to 22 kΩ ± 5% to AGND		4°		V
		Advance pin tied to 100 kΩ ± 5% to AGND		11°		V
		Advance pin tied to Hi-Z		15°		V
		Advance pin tied to 100 kΩ ± 5% to AVDD		20°		V
		Advance pin tied to 22 kΩ ± 5% to AVDD		25°		V
		Advance pin tied to Tied to AVDD		30°		V
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	VM rising	4.3	4.4	4.5	V
		VM falling	4.1	4.2	4.3	V
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling threshold	140	200	350	mV
t_{UVLO}	Supply undervoltage deglitch time		3	5	7	µs
V_{OVP}	Supply overvoltage protection (OVP) (SPI Device)	Supply rising, OVP_EN = 1, OVP_SEL = 0	32.5	34	35	V
		Supply falling, OVP_EN = 1, OVP_SEL = 0	31.8	33	34.3	V
		Supply rising, OVP_EN = 1, OVP_SEL = 1	20	22	23	V
		Supply falling, OVP_EN = 1, OVP_SEL = 1	19	21	22	V
V_{OVP_HYS}	Supply overvoltage protection (OVP) (SPI Device)	Rising to falling threshold, OVP_SEL = 1	0.9	1	1.1	V
		Rising to falling threshold, OVP_SEL = 0	0.7	0.8	0.9	V
t_{OVP}	Supply overvoltage deglitch time			5		µs
V_{CPUV}	Charge pump undervoltage lockout (above VM)	Supply rising		2.5		V
		Supply falling		2.4		V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold		100		mV
V_{AVDD_UV}	Analog regulator undervoltage lockout	Supply rising	2.7	2.85	3	V
		Supply falling	2.5	2.65	2.8	V
$V_{AVDD\_UV\_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold		200		mV

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCP}	Overcurrent protection trip point (SPI Device)	OCP_LVL = 0b	10	16	20	A
		OCP_LVL = 1b	15	24	28	A
	Overcurrent protection trip point (HW Device)	OCP pin tied to AGND	10	16	21.5	A
		OCP pin tied to AVDD	15	24	31	A
t_{OCP}	Overcurrent protection deglitch time (SPI Device)	OCP_DEG = 00b		0.2		µs
		OCP_DEG = 01b		0.6		µs
		OCP_DEG = 10b		1.1		µs
		OCP_DEG = 11b		1.6		µs
	Overcurrent protection deglitch time (HW Device)			0.2		µs
t_{RETRY}	Overcurrent protection retry time (SPI Device)	OCP_RETRY = 0		5		ms
		OCP_RETRY = 1		500		ms
t_{RETRY}	Overcurrent protection retry time (HW Device)			5		ms
t_{MTR_LOCK}	Motor lock detection time (SPI Device)	MOTOR_LOCK_TDET = 00b		300		ms
		MOTOR_LOCK_TDET = 01b		500		ms
		MOTOR_LOCK_TDET = 10b		1000		ms
		MOTOR_LOCK_TDET = 11b		5000		ms
t_{MTR_LOCK}	Motor lock detection time (HW Device)			1000		ms
$t_{MTR\_LOCK\_RETRY}$	Motor lock retry time (SPI Device)	MOTOR_LOCK_RETRY = 0b		500		ms
		MOTOR_LOCK_RETRY = 1b		5000		ms
$t_{MTR\_LOCK\_RETRY}$	Motor lock retry time (HW Device)			500		ms
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	135	145	160	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)	10	15	20	°C
T_{TSD}	Thermal shutdown temperature	Die temperature (T_J)	150	160	175	°C
T_{TSD_HYS}	Thermal shutdown hysteresis	Die temperature (T_J)	10	15	20	°C

7.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{READY}	SPI ready after power up			1	ms
t_{HI_nSCS}	nSCS minimum high time	300			ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{HD_nSCS}	nSCS input hold time	25			ns
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{HD_SDI}	SDI input data hold time	25			ns
t_{DLY_SDO}	SDO output data delay time			25	ns
t_{EN_SDO}	SDO enable delay time			50	ns
t_{DIS_SDO}	SDO disable delay time			50	ns

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The MCT8316Z device is an integrated 100-mΩ (combined high-side and low-side MOSFET's on-state resistance) driver for 3-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three half-bridge MOSFETs, gate drivers, charge pump, linear regulator for the external load and buck regulator. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors.

The architecture uses an internal state machine to protect against short-circuit events, and protect against dv/dt parasitic turnon of the internal power MOSFET.

The MCT8316Z device integrates three-phase sensored trapezoidal commutation using analog or digital hall sensors for position detection.

In addition to the high level of device integration, the MCT8316Z device provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD undervoltage lockout (AVDD_UV), buck regulator ULVO for MCT8316ZR/T and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

The MCT8316ZT and MCT8316ZR device are available in 0.5-mm pin pitch, VQFN surface-mount packages. The VQFN package size is 7 mm × 5 mm.

8.2 Functional Block Diagram

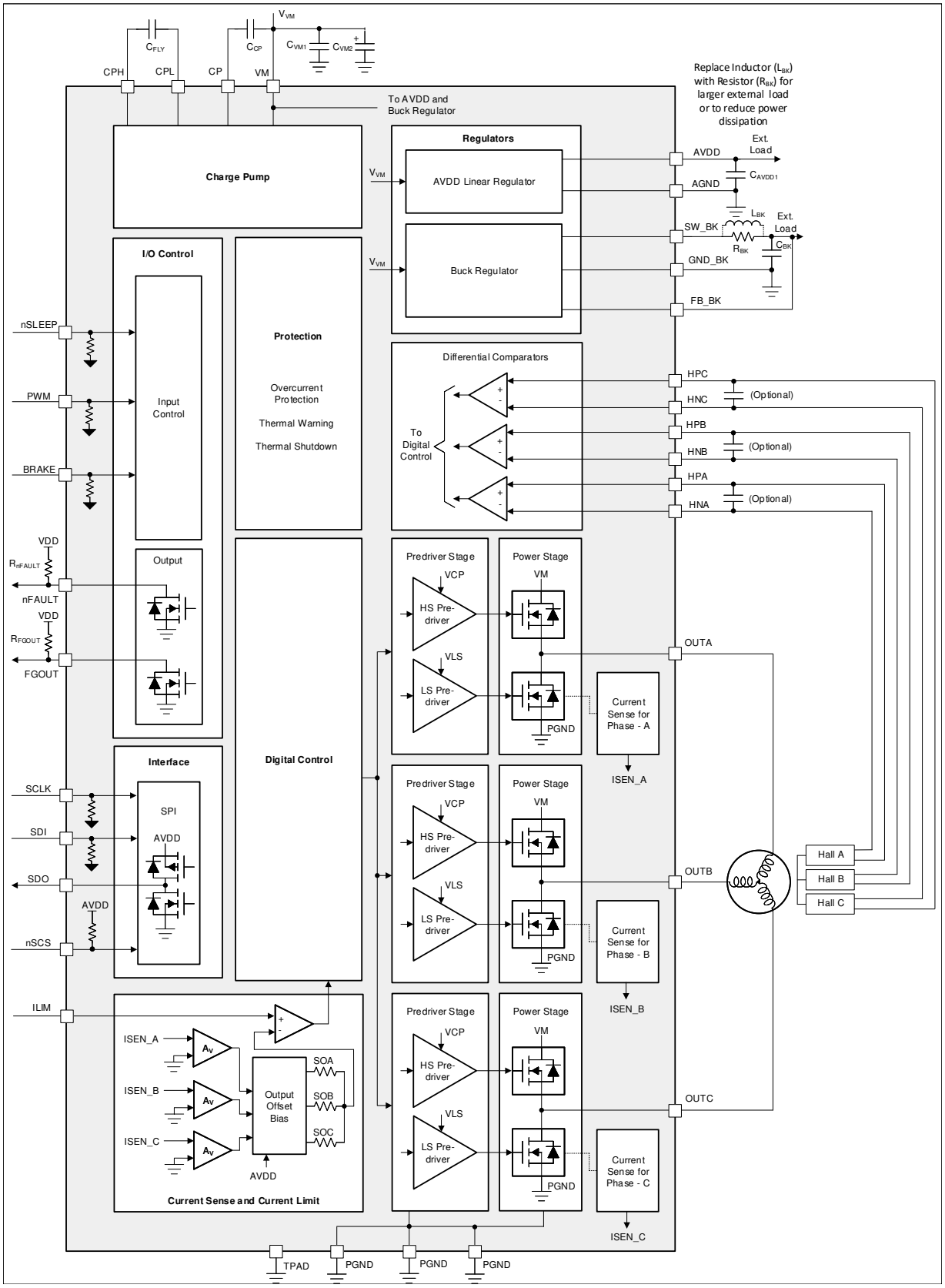


Figure 8-1. MCT8316ZR Block Diagram

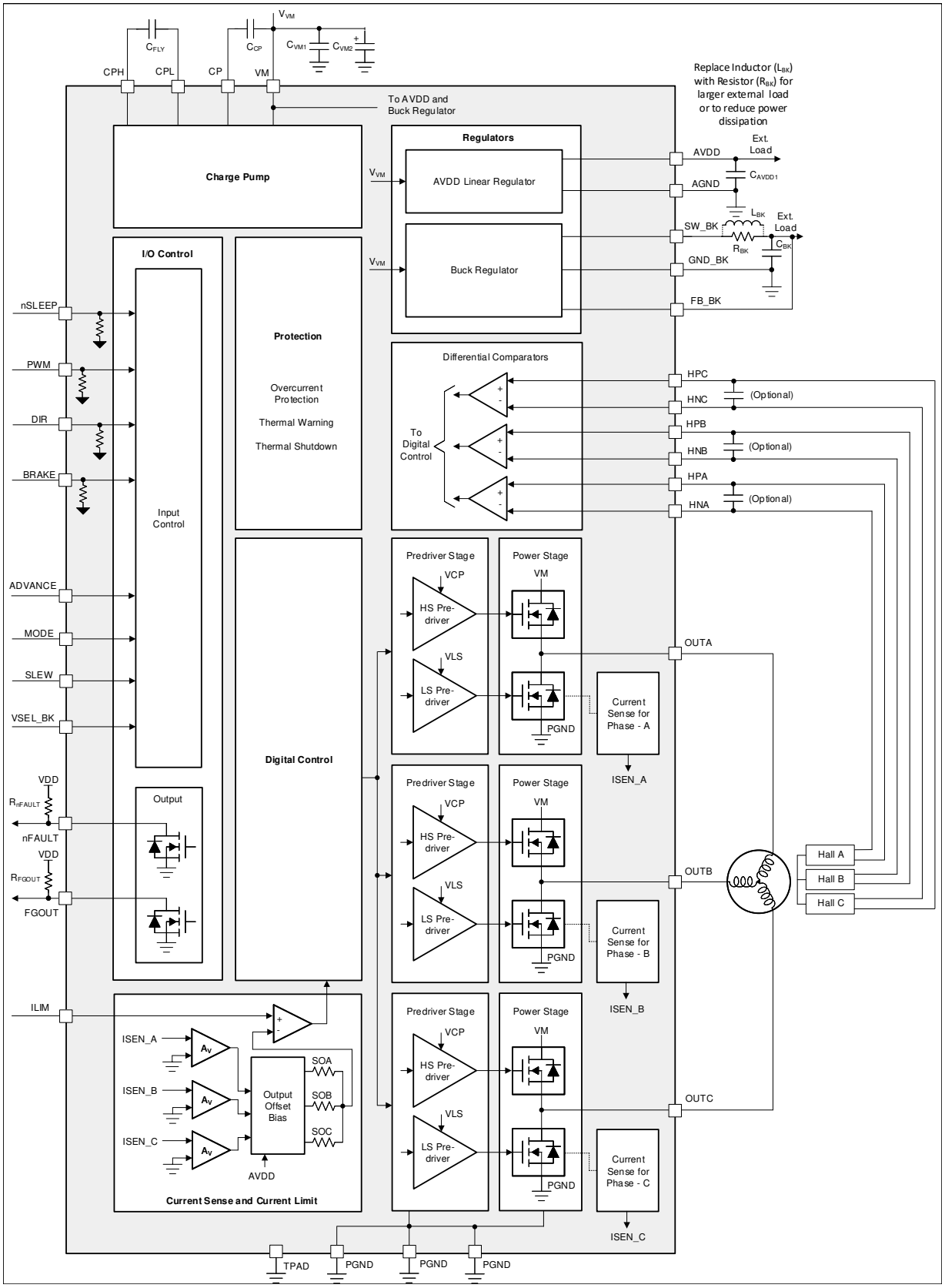


Figure 8-2. MCT8316ZT Block Diagram

ADVANCE INFORMATION

8.3 Feature Description

Table 8-1 lists the recommended values of the external components for the driver.

Note

TI recommends to connect pull up on nFAULT even if it is not used to avoid undesirable entry into internal test mode.

Table 8-1. MCT8316Z External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1-µF, VM-rated capacitor
C_{VM2}	VM	PGND	≥ 10-µF, VM-rated capacitor
C_{CP}	CP	VM	X5R or X7R, 16-V, 1-µF capacitor
C_{FLY}	CPH	CPL	X5R or X7R, 10-nF, VM-rated capacitor
C_{AVDD}	AVDD	AGND	X5R or X7R, 1-µF, 6.3-V capacitor
C_{BK}	SW_BK	GND_BK	X5R or X7R, buck-output rated capacitor
L_{BK}	SW_BK	FB_BK	Output inductor
R_{nFAULT}	VCC	nFAULT	5.1-kΩ, Pullup resistor
R_{MODE}	MODE	AGND or AVDD	MCT8316Z hardware interface
R_{SLEW}	SLEW	AGND or AVDD	MCT8316Z hardware interface
$R_{ADVANCE}$	ADVANCE	AGND or AVDD	MCT8316Z hardware interface
R_{VSEL_BK}	VSEL_BK	AGND or AVDD	MCT8316Z hardware interface
C_{ILIM}	ILIM	AGND	X5R or X7R, 0.1-µF, AVDD-rated capacitor (Optional)

8.3.1 Output Stage

The MCT8316Z device consists of an integrated 100-mΩ (combined high-side and low-side FET's on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FET's across a wide operating-voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs. The device has three VM motor power-supply pins which are to be connected together to the motor-supply voltage.

8.3.2 PWM Control Mode (1x PWM Mode)

The MCT8316Z family of devices provides seven different control modes to support various commutation and control methods. The MCT8316Z device provides a 1x PWM control mode for driving the BLDC motor in trapezoidal current-control mode. The MCT8316Z device uses 6-step block commutation tables that are stored internally. This feature lets a three-phase BLDC motor be controlled using a single PWM sourced from a simple controller. The PWM is applied on the PWM pin and determines the output frequency and duty cycle of the half-bridges.

The MCT8316Z family of devices supports both analog and digital hall inputs by changing mode input setting. Differential hall inputs should be connected to HPx and HNx pins (see Figure 8-3). Digital hall inputs should be connected to the HPx pins while keeping the HNx pins floating (see Figure 8-4).

The half-bridge output states are managed by the HPA, HNA, HPB, HNB, HPC and HNC pins in analog mode and HPA, HPB, HPC in digital mode which are used as state logic inputs. The state inputs are the position feedback of the BLDC motor. The 1x PWM mode usually operates with synchronous rectification (low-side MOSFET recirculation); however, the mode can be configured to use asynchronous rectification (MOSFET body diode freewheeling) as shown below

Table 8-2. PWM_MODE Configuration

MODE Type	MODE Pin (Hardware Variant)	Hall Configuration	Modulation	ASR and AAR Mode
Mode 1	Connected to AGND	Analog Hall Input	Asynchronous	ASR and AAR Disabled

Table 8-2. PWM_MODE Configuration (continued)

MODE Type	MODE Pin (Hardware Variant)	Hall Configuration	Modulation	ASR and AAR Mode
Mode 2	Connected to AGND with R_{MODE1}	Digital Hall Input	Asynchronous	ASR and AAR Disabled
Mode 3	Connected to AGND with R_{MODE2}	Analog Hall Input	Synchronous	ASR and AAR Disabled
Mode 4	Hi-Z	Digital Hall Input	Synchronous	ASR and AAR Disabled
Mode 5	Connected to AVDD with R_{MODE2}	Analog Hall Input	Synchronous	ASR and AAR Enabled
Mode 6	Connected to AVDD with R_{MODE1}	Digital Hall Input	Synchronous	ASR and AAR Enabled
Mode 7	Connected to AVDD	Digital Hall Input	Synchronous	ASR and AAR Enabled

Note

Texas Instruments does not recommend changing the MODE pin or MODE register during operation of the power MOSFETs. Set all INHx and INLx pins to logic low before changing the MODE pin or MODE register. Set PWM to a low level before changing the MODE pin or MODE register.

8.3.2.1 Analog Hall Input Configuration

Figure 8-3 shows the connection of Analog Hall inputs to the driver. Analog hall elements are fed to the hall comparators, which zero crossing is used to generate the commutation logic.

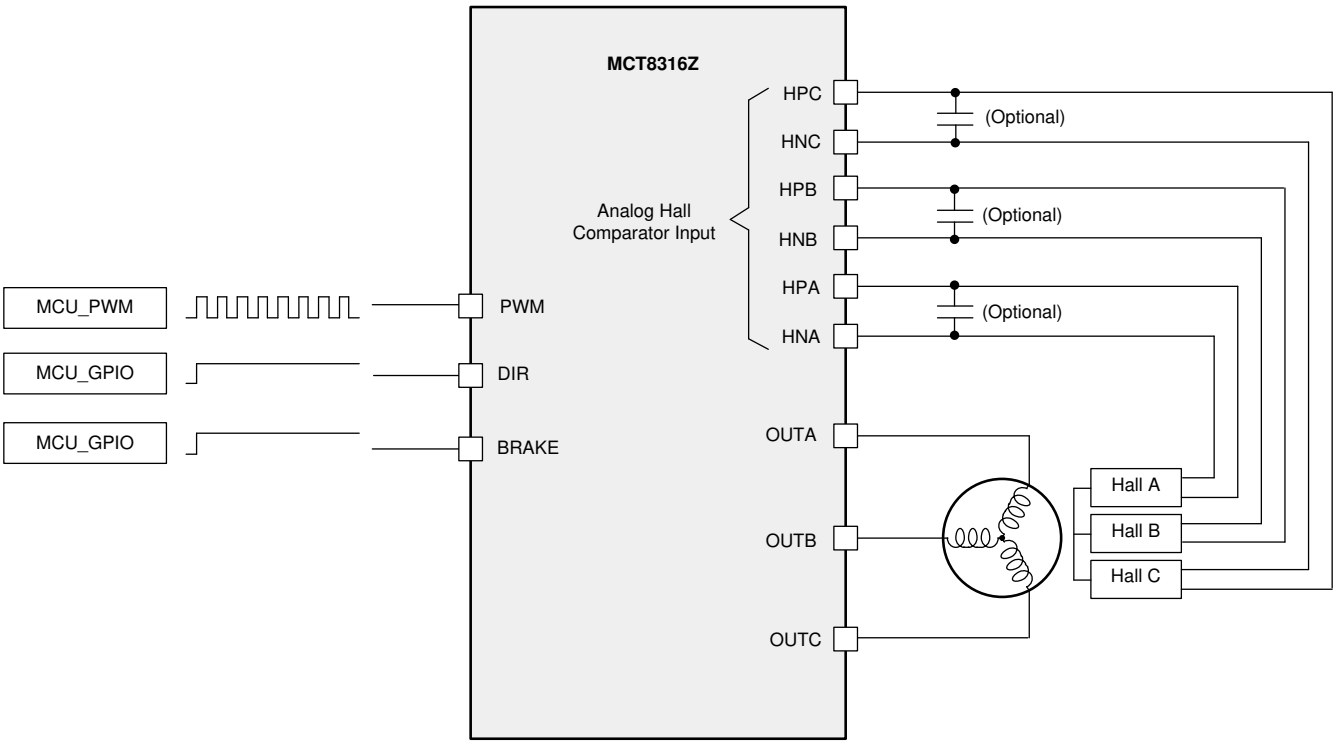


Figure 8-3. 1x PWM Mode with Analog Hall Input

Note

Texas Instruments recommends motor direction (DIR) change when the motor is stationary.

ADVANCE INFORMATION

8.3.2.2 Digital Hall Input Configuration

Figure 8-4 shows the connection of Digital Hall inputs to the driver.

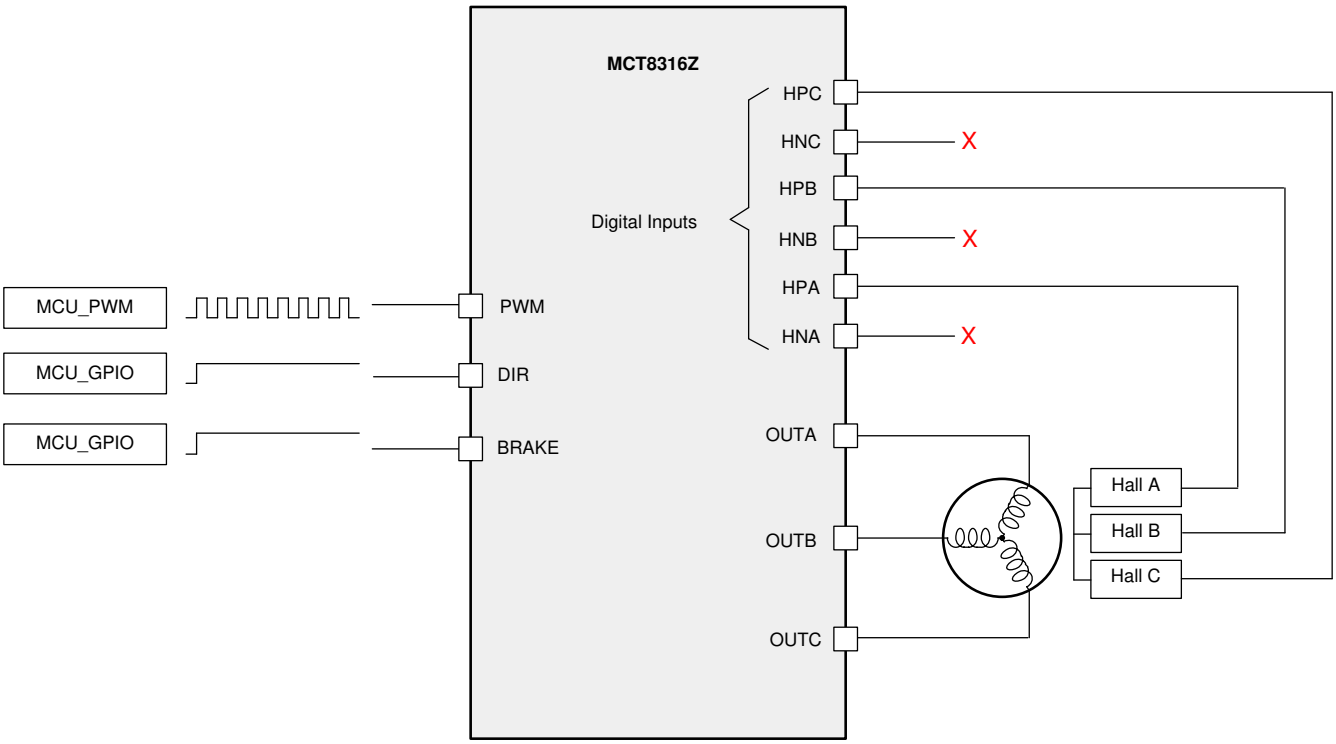


Figure 8-4. 1x PWM Mode with Digital Hall Input

8.3.2.3 Asynchronous Modulation

The DIR pin controls the direction of BLDC motor in either clockwise or counter-clockwise direction. Tie the DIR pin low if this feature is not required.

The BRAKE input halts the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when it is pulled high. This brake is independent of the states of the other input pins. Tie the BRAKE pin low if this feature is not required.

Table 8-3 shows the configuration in 1x PWM mode with asynchronous modulation.

Table 8-3. Asynchronous Modulation

HALL INPUTS							DRIVER OUTPUTS						
STATE	DIR = 0			DIR = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	High Side	Low Side	High Side	Low Side	High Side	Low Side	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	L	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

8.3.2.4 Synchronous Modulation

Table 8-4 shows the configuration in 1x PWM mode with synchronous modulation.

Table 8-4. Synchronous Modulation

HALL INPUTS							DRIVER OUTPUTS						
STATE	DIR = 0			DIR = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	High Side	Low Side	High Side	Low Side	High Side	Low Side	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

8.3.2.5 Motor Operation

Figure 8-5 and Figure 8-6 shows the BLDC motor commutation with direction setting (DIR) as 0 and 1 respectively.

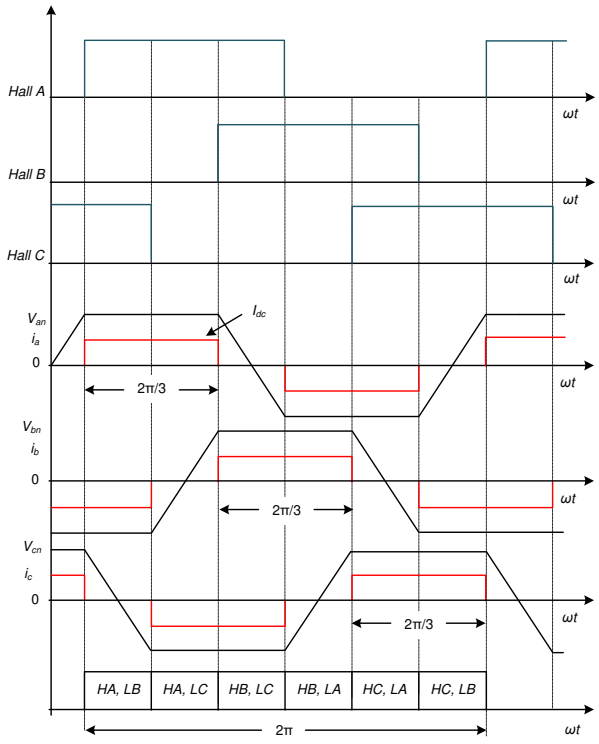


Figure 8-5. BLDC Motor Commutation with DIR = 0

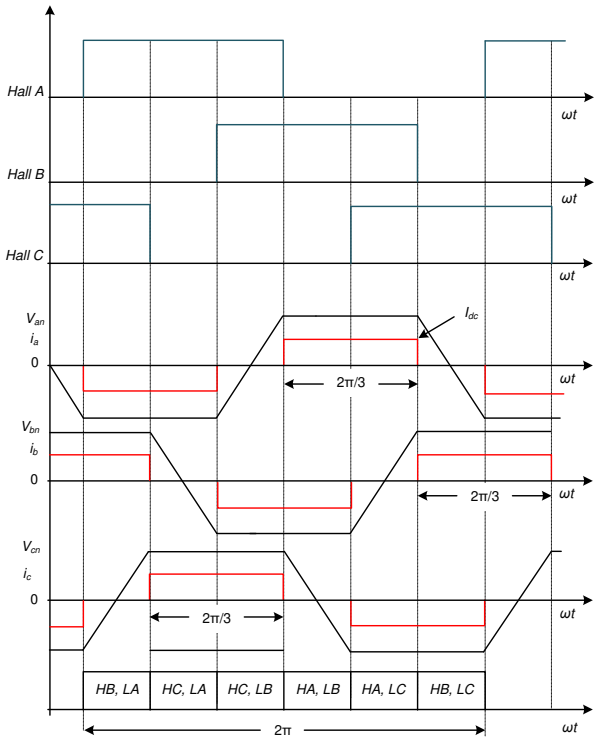


Figure 8-6. BLDC Motor Commutation with DIR = 1

ADVANCE INFORMATION

8.3.3 Device Interface Modes

The MCT8316Z family of devices supports two different interface modes (SPI and hardware) to let the end application design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin-to-pin compatible. This compatibility lets application designers evaluate with one interface version and potentially switch to another with minimal modifications to their design.

8.3.3.1 Serial Peripheral Interface (SPI)

The SPI devices support a serial communication bus that lets an external controller send and receive data with the MCT8316Z. This support lets the external controller configure device settings and read detailed fault information. The interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins which are described as follows:

- The SCLK pin is an input that accepts a clock signal to determine when data is captured and propagated on the SDI and SDO pins.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin uses an open-drain structure and requires an external pullup resistor.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the MCT8316Z.

For more information on the SPI, see the *Section 8.5* section.

8.3.3.2 Hardware Interface

Hardware interface devices convert the four SPI pins into four resistor-configurable inputs which are ADVANCE, MODE, SLEW and VSEL_BK.

This conversion lets the application designer configure the most common device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

- The MODE pin configures the PWM control mode.
- The SLEW pin configures the slew rate of the output voltage.
- The ADVANCE pin configures the lead angle of the output with respect to hall signals.
- The VSEL_BK pin is used to configure the buck regulator voltage.

For more information on the hardware interface, see the *Section 8.3.10* section.

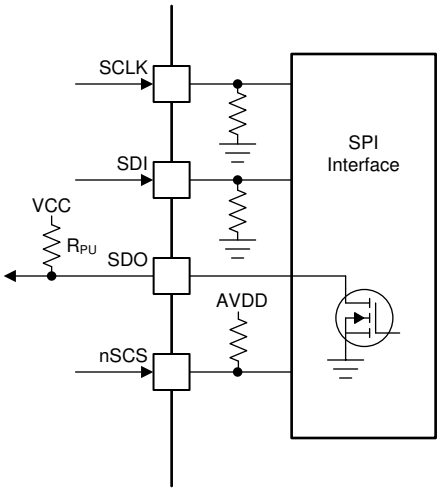


Figure 8-7. MCT8316ZR SPI Interface

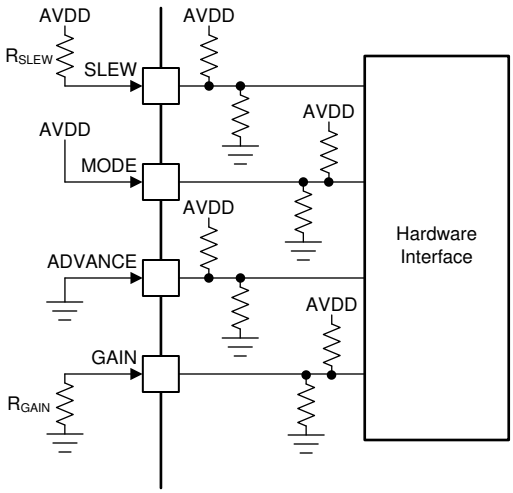


Figure 8-8. MCT8316ZT Hardware Interface

8.3.4 AVDD Linear Voltage Regulator

A 3.3-V, linear regulator is integrated into the MCT8316Z family of devices and is available for use by external circuitry. The AVDD regulator is used for powering up the internal digital circuitry of the MCT8316Z device. Additionally, this regulator can also provide the supply voltage for a low-power MCU or other circuitry supporting low current (up to 30mA). The output of the AVDD regulator should be bypassed near the AVDD pin with an X5R or X7R, 1-µF, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3V.

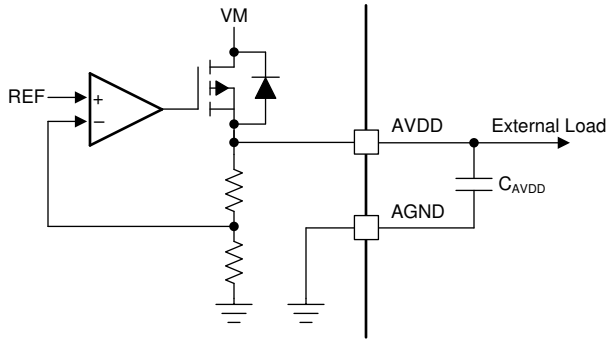


Figure 8-9. AVDD Linear Regulator Block Diagram

Use Equation 1 to calculate the power dissipated in the device by the AVDD linear regulator.

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a V_{VM} of 24 V, drawing 20 mA out of AVDD results in a power dissipation as shown in Equation 2.

$$P = (24\ V - 3.3\ V) \times 20\ mA = 414\ mW \quad (2)$$

ADVANCE INFORMATION

8.3.5 Step-Down Buck Regulator MCT8316ZR and MCT8316ZT)

The MCT8316ZR and MCT8316ZT have an integrated buck regulator in conjunction with analog linear regulator to supply regulated 3.3/5V power for an external controller or system voltage rail. Additionally, the buck output can also be configured to 4/5.7V to support extra headroom for an external LDO generating a 3.3/5V supply. The output voltage of the buck is set by the VSEL_BK pin in the MCT8316ZT device (hardware variant) and BUCK_SEL bits in the MCT8316ZR device (SPI variant).

The buck regulator has a very-low quiescent current during light loads to prolong battery life. The device improves performance during line and load transients by implementing a pulse-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design.

8.3.5.1 Buck Inductor Mode

The buck regulator in MCT8316Z device is primarily designed to support low inductance of 47µH and 22µH inductors. The 47µH inductor allows the buck regulator to operate up to 200 mA load current support, whereas the 22µH inductor limits the load current to 50 mA.

Figure 8-10 shows the connection of buck regulator in inductor mode.

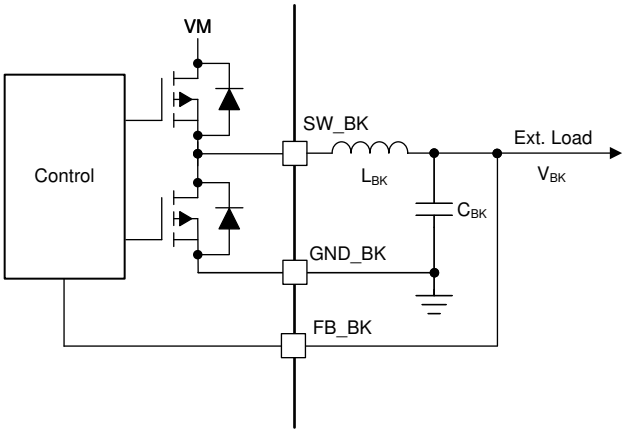


Figure 8-10. Buck (Inductor Mode)

8.3.5.2 Buck Resistor mode

If the external load requirement is less than 40 mA, the inductor can be replaced with a resistor. In resistor mode, power is dissipated from the external resistor and the efficiency is lower than inductor mode.

Figure 8-11 shows the connection of buck regulator in resistor mode.

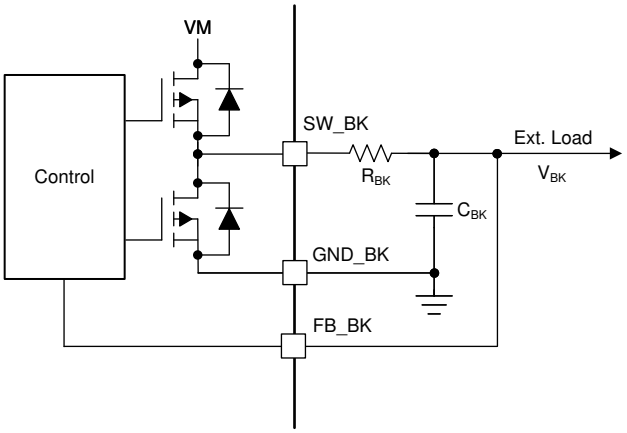


Figure 8-11. Buck (Resistor Mode)

8.3.5.3 Buck Regulator with External LDO

The buck regulator in the MCT8316Z device also supports the voltage requirement to feed to an external LDO to generate the standard 3.3V/5V output rail. The buck output voltage is configured to 4V or 5.7V to provide an extra headroom to support the external LDO for generating a 3.3V or 5V rail as shown in Figure 8-12. This allows a lower-voltage LDO design to save cost and better thermal management due to low drop-out voltage.

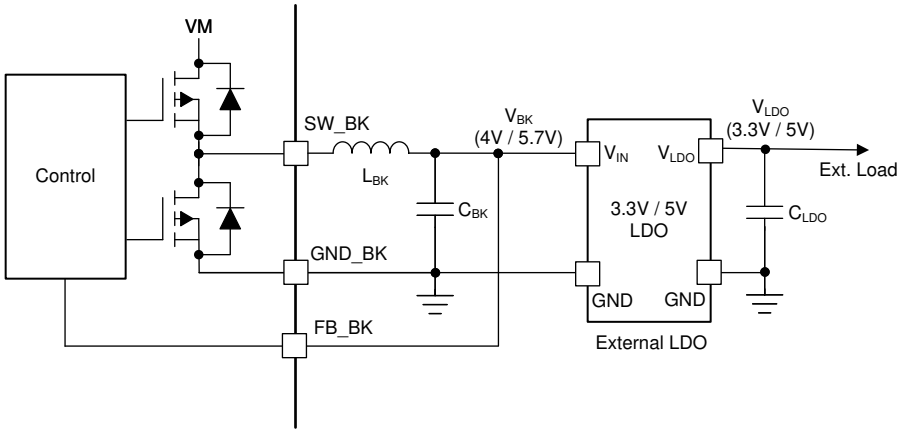


Figure 8-12. Buck Regulator with External LDO

ADVANCE INFORMATION

8.3.5.4 LDO Power Sequencing on Buck Regulator

The LDO of MCT8316ZR and MCT8316ZT devices has an option of accepting the power supply from buck regulator to reduce power dissipation. The power sequencing mode in the MCT8316ZR and MCT8316ZT device allows on-the-fly changeover of the LDO power supply from the DC mains (VM) to buck output (VBK) as shown in Figure 8-13. This sequencing automatically happens in the hardware device when the buck voltage is set to either 5V or 5.7V. For disabling the power sequencing in the SPI device, set the BUCK_PS_DIS bit to 1.

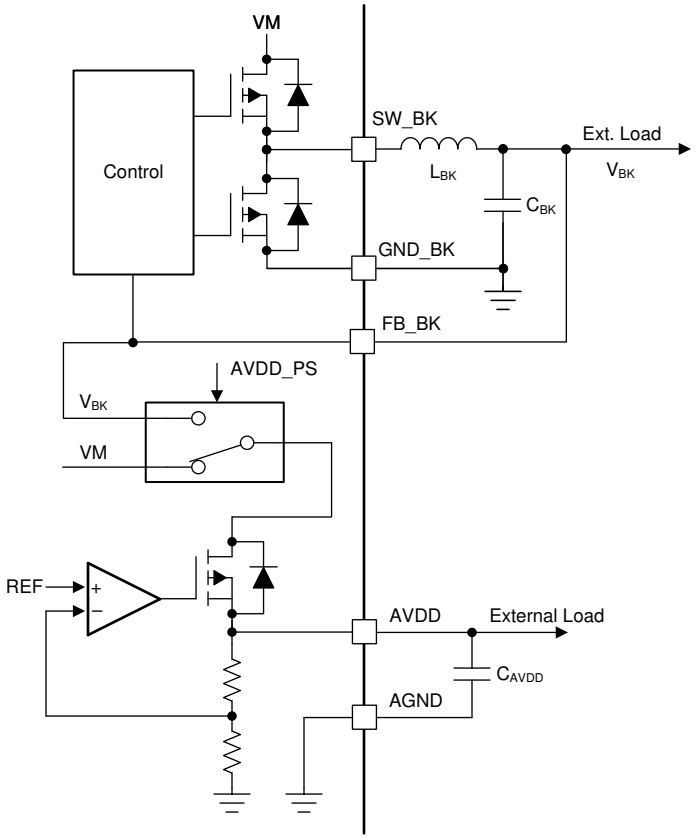


Figure 8-13. LDO Power Sequencing on Buck Regulator

8.3.5.5 Buck Operation and Control

The buck regulator in MCT8316ZR and MCT8316ZT implements a pulse frequency modulation (PFM) architecture with peak current mode control. The output voltage of the buck regulator is compared with the reference voltage (V_{BK_REF}) which is internally generated depending on the buck-output voltage setting (VSEL_BK pin or BUCK_SEL bits) which constitutes an outer voltage control loop. Now, depending on the comparator output going high ($V_{BK} < V_{BK\_REF}$) or low ($V_{BK} > V_{BK\_REF}$), the high-side power FET of the buck turns on and off respectively. An independent current control loop monitors the current in the high-side power FET (I_{BK}) and turns off the high-side FET when the current becomes higher than the buck current limit (I_{BK_CL}). This implements a current limit control for the buck regulator. Figure 8-14 shows the architecture of the buck and various control/protection loops to avoid unwanted scenarios.

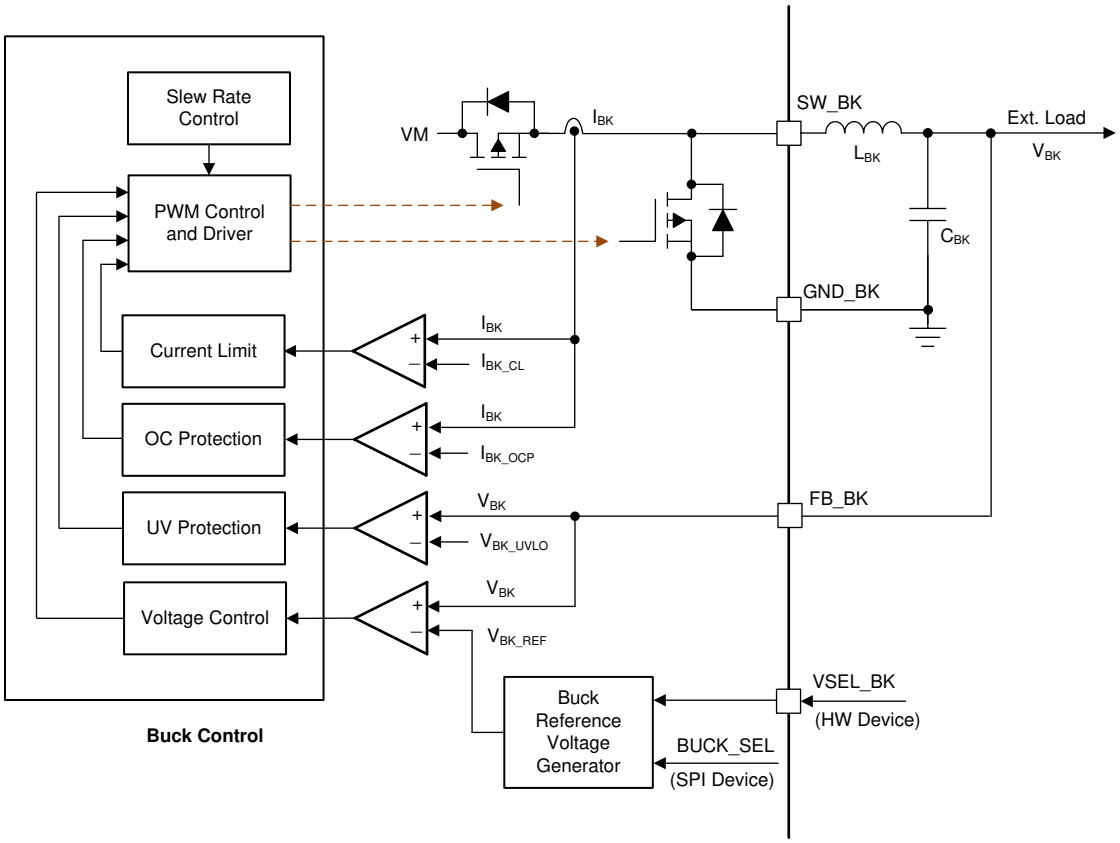


Figure 8-14. Buck Operation and Control Loops

ADVANCE INFORMATION

8.3.5.6 Buck Undervoltage Protection

If at any time the input supply voltage on the FB_BK pin falls lower than the V_{BK_UVLO} threshold, all of the both high-side and low-side MOSFETs of the buck regulator are disabled and the nFAULT pin is driven low. The FAULT, BK_FLT and BUCK_UV bits are also latched high in the registers on SPI devices. Normal operation starts again (buck operation and the nFAULT pin is released) when the VBK undervoltage condition clears. The BUCK_UV bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

8.3.5.7 Buck Overcurrent Protection

The overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current across high-side MOSFET exceeds the I_{BK_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a buck OCP event is recognized and nFAULT pin is driven low. The FAULT, BK_FLT and BK_OCP bits are latched high in the SPI registers. Normal operation starts again automatically (buck operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT, BK_FLT and BK_OCP bits stay latched until the t_{RETRY} period expires.

On hardware interface devices, the I_{BK_OCP} threshold is set to 600-mA, whereas on SPI devices, the I_{BK_OCP} threshold is set through the BUCK_CL bit to either to 600-mA or 150-mA.

8.3.6 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The MCT8316Z integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. See the block diagram, pin descriptions and see section (Section 8.3) for details on these capacitors (value, connection, and so forth).

The charge pump shuts down when nSLEEP is low.

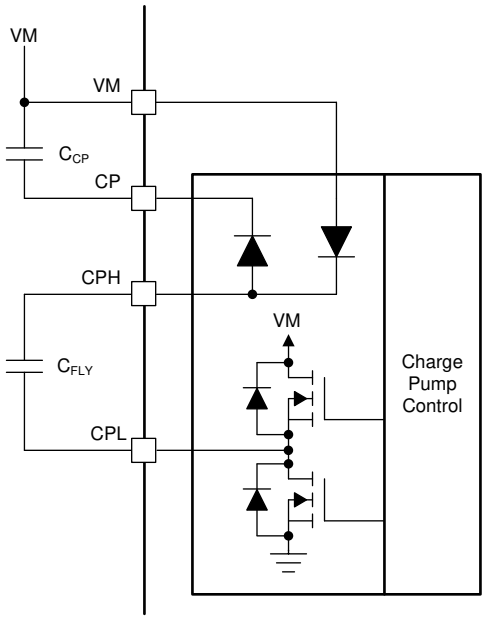


Figure 8-15. MCT8316Z Charge Pump

ADVANCE INFORMATION

8.3.7 Slew Rate Control

An adjustable gate-drive current control to the MOSFETs of half-bridges is implemented to achieve the slew rate control. The MOSFET VDS slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes, and switching voltage transients related to parasitics. These slew rates are predominantly determined by the rate of gate charge to internal MOSFETs as shown in Figure 8-16.

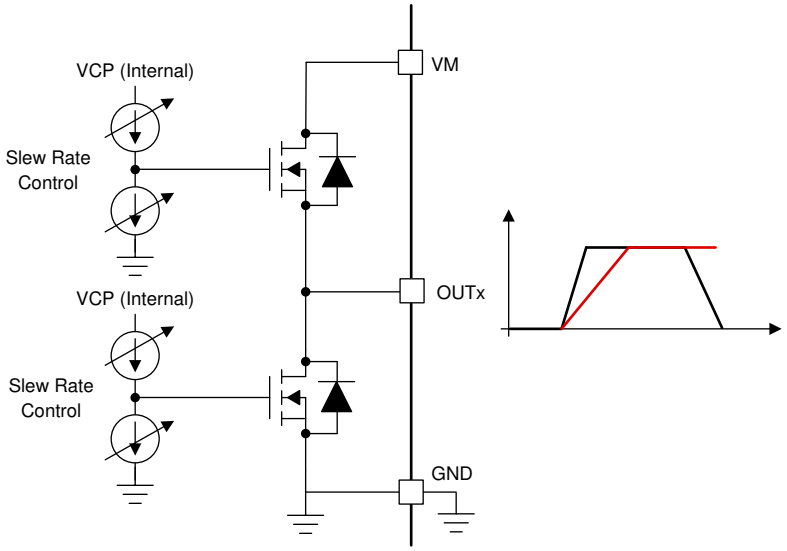


Figure 8-16. Slew Rate Circuit Implementation

The slew rate of each half-bridge can be adjusted by the SLEW pin in hardware device variant or by using the SLEW bits in SPI device variant. Each half-bridge can be selected to either of a slew rate setting of 25-V/µs, 50-V/µs, 125-V/µs or 200-V/µs. The slew rate is calculated by the rise time and fall time of the voltage on OUTx pin as shown in Figure 8-17.

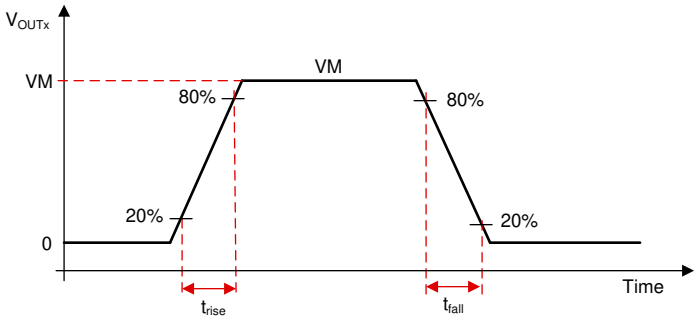


Figure 8-17. Slew Rate Timings

8.3.8 Cross Conduction (Dead Time)

The device is fully protected for any cross conduction of MOSFETs. In half-bridge configuration, the operation of high-side and low-side MOSFETs are ensured to avoid any shoot-through currents by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that VGS of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in Figure 8-18 and Figure 8-19.

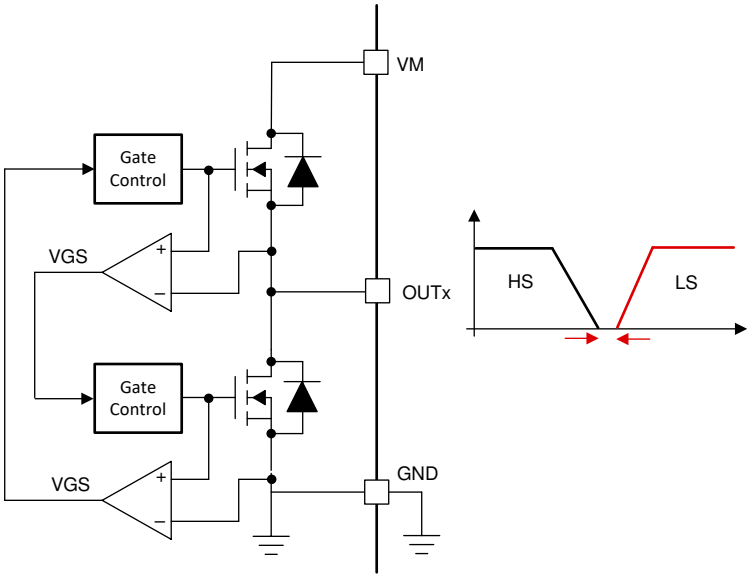


Figure 8-18. Cross Conduction Protection

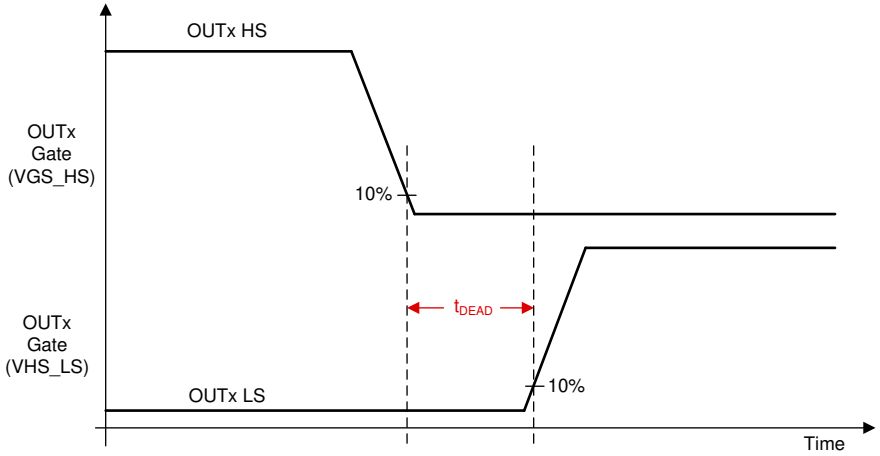


Figure 8-19. Dead Time

ADVANCE INFORMATION

8.3.9 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to change in gate driver voltage. This time has three parts consisting of the digital input deglitcher delay, analog driver, and comparator delay.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes, a small digital delay is added as the input command propagates through the device.

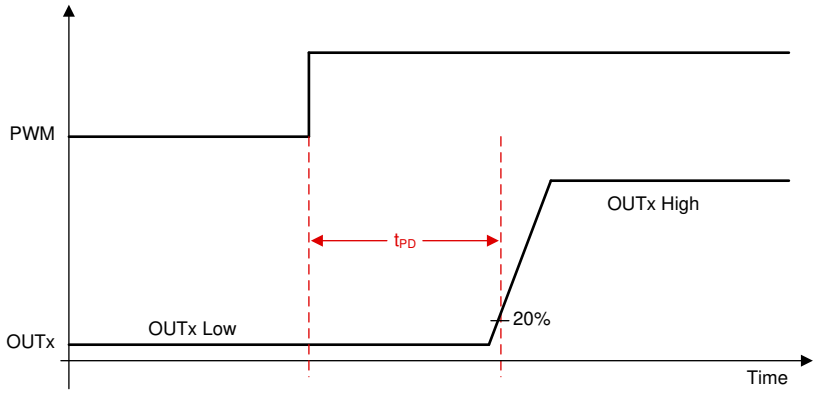


Figure 8-20. Propagation Delay Timing

8.3.9.1 Driver Delay Compensation

MCT8316Z monitors the prorogation delay internally and adds a variable delay on top of it to provide fixed delay as shown in Figure 8-21 and Figure 8-22. Delay compensation feature reduces uncertainty caused in timing of current measurement and also reduces duty cycle distortion caused due to propagation delay.

The fixed delay is summation of propagation delay (t_{PD}) caused to internal driver delay and variable delay (t_{VAR}) added to compensate for uncertainty. The fixed delay can be configured through DLY_TARGET register. Refer Table 8-5 for recommendation on configuration for DLY_TARGET for different slew rate settings.

Delay compensation is only available in SPI variant MCT8316ZR and can be enabled by configuring DLYCMP_EN and DLY_TARGET. It is disabled in hardware variant MCT8316ZT

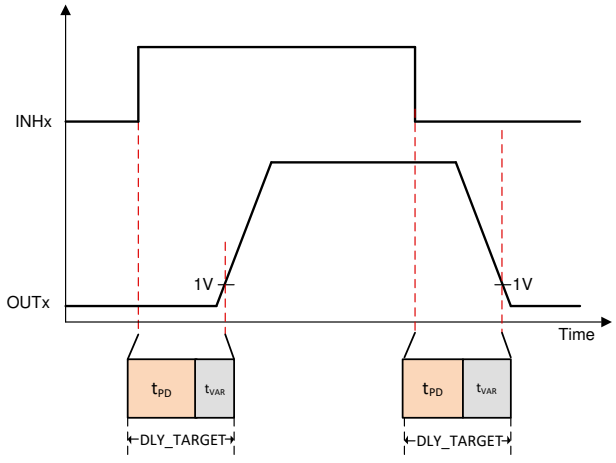


Figure 8-21. Delay Compensation with current flowing out of phase

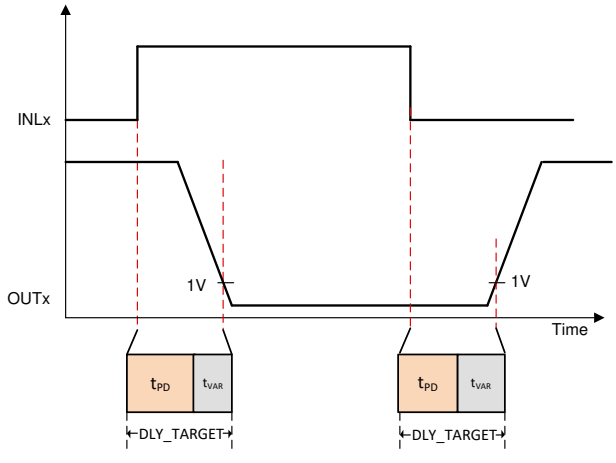


Figure 8-22. Delay Compensation with current flowing into the phase

Table 8-5. Delay Target Recommendation

SLEW RATE	DLY_TARGET
200 V/µs	DLY_TARGET = 0x5 (1.2 µs)
125 V/µs	DLY_TARGET = 0x8 (1.8 µs)
50 V/µs	DLY_TARGET = 0xB (2.4 µs)
25 V/µs	DLY_TARGET = 0xF (3.2 µs)

8.3.10 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

8.3.10.1 Logic Level Input Pin (Internal Pulldown)

Figure 8-23 shows the input structure for the logic level pins, BRAKE, DIR, DRVOFF, nSLEEP, PWM, SCLK and SDI. The input can be with a voltage or external resistor. It is recommended to put these pins low in device sleep mode to reduce leakage current through internal pull-down resistors.

STATE	CONNECTION
V_{IH}	Tied to AVDD
V_{IL}	Tied to GND

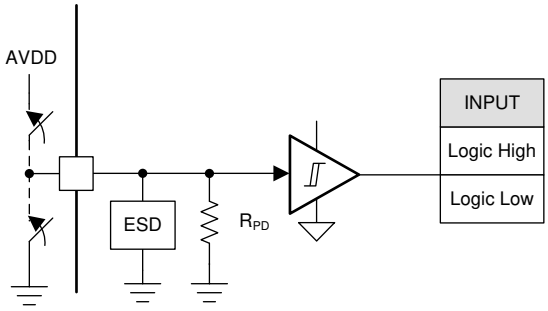


Figure 8-23. Logic-Level Input Pin Structure

8.3.10.2 Logic Level Input Pin (Internal Pullup)

Figure 8-24 shows the input structure for the logic level pin, nSCS. The input can be driven with a voltage or external resistor.

STATE	CONNECTION
V_{IH}	Tied to AVDD
V_{IL}	Tied to GND

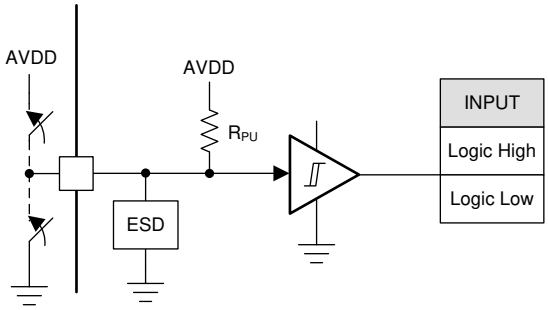


Figure 8-24. Logic nSCC

8.3.10.3 Open Drain Pin

Figure 8-25 shows the structure of the open-drain output pins, nFAULT and FGOUT. The open-drain output requires an external pullup resistor to function properly.

STATE	STATUS
No Fault	Pulled-Up
Fault	Pulled-Down

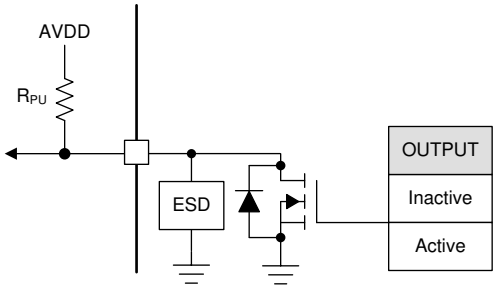


Figure 8-25. Open Drain

8.3.10.4 Push Pull Pin

Figure 8-26 shows the structure of push-pull pin, SDO.

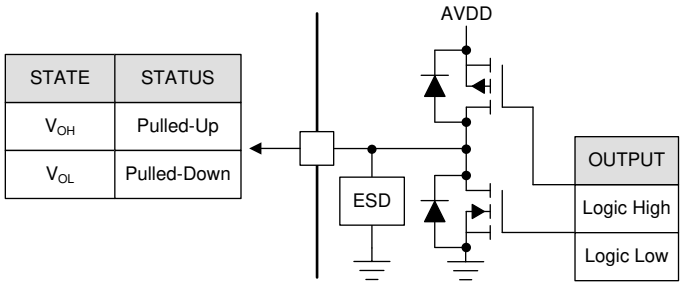


Figure 8-26. Push Pull

8.3.10.5 Four Level Input Pin

Figure 8-27 shows the structure of the four level input pins, SLEW and VSEL_BK on hardware interface devices. The input can be set with an external resistor.

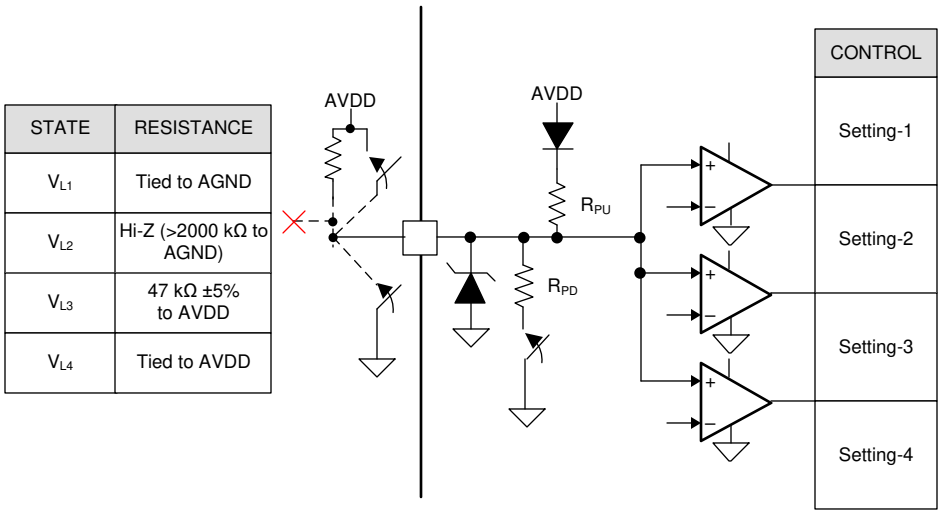


Figure 8-27. Four Level Input Pin Structure

ADVANCE INFORMATION

8.3.10.6 Seven Level Input Pin

Figure 8-28 shows the structure of the seven level input pins, ADVANCE and MODE, on hardware interface devices. The input can be set with an external resistor.

STATE	RESISTANCE
V_{L1}	Tied to AGND
V_{L2}	22 kΩ ± 5% to AGND
V_{L3}	100 kΩ ± 5% to AGND
V_{L4}	Hi-Z (>2000 kΩ to AGND)
V_{L5}	100 kΩ ± 5% to AVDD
V_{L6}	22 kΩ ±5% to AVDD
V_{L7}	Tied to AVDD

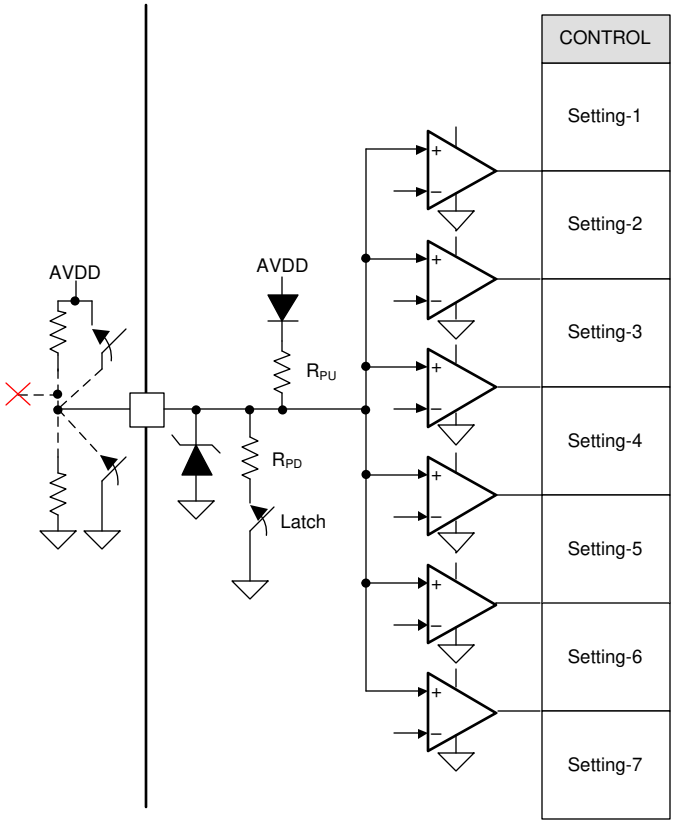


Figure 8-28. Seven Level Input Pin Structure

ADVANCE INFORMATION

8.3.11 Active Demagnetization

MCT8316Z family of devices has smart rectification features (actice demagnetization) which reduces power losses in device by reducing diode conduction losses. When this feature is enabled device automatically turns ON FET whenever it detects diode conduction. This feature can be configured with the MODE pins in hardware variants. In SPI device variants this can be configured through EN_ASR and EN_AAR bits. The smart rectification is classified into two categories of automatic synchronous rectification (ASR) mode and automatic asynchronous rectification (AAR) mode which are described in sections below.

Note

In SPI device variants both bits, EN_ASR and EN_AAR needs to set to 1 to enable active demagnetization.

The MCT8316Z device includes a high-side (AD_HS) and low-side (AD_LS) comparator which detects the negative flow of current in the device on each half-bridge. The AD_HS comparator compares the sense-FET output with the supply voltage (VM) threshold, whereas the AD_LS compatator compares with the ground (0-V) threshold. Depending upon the flow of current from OUTx to VM or PGND to OUTx, the AD_HS or the AD_LS comparator trips. This comparator provides a reference point for the operation of active demagnetization feature.

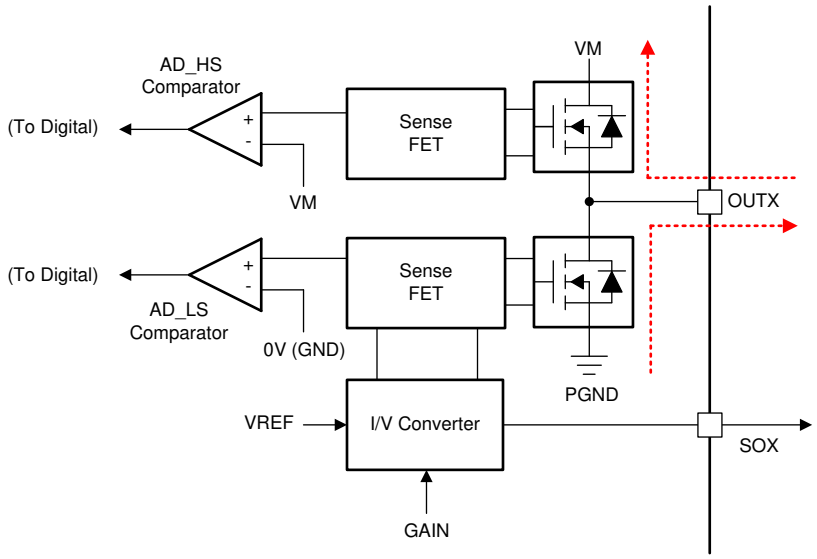


Figure 8-29. Active Demagnetization Operation

Table 8-6 shows the configuration of ASR and AAR mode in the MCT8316Z device.

Table 8-6. PWM_MODE Configuration

MODE Type	MODE Pin (Hardware Variant)	MODE Bits (SPI Variant)	Hall Configuration	Modulation	ASR and AAR Mode
Mode 1	Connected to AGND	EN_ASR = 0, EN_AAR = 0	Analog Hall Input	Asynchronous	ASR and AAR Disabled
Mode 2	Connected to AGND with R_{MODE1}	EN_ASR = 0, EN_AAR = 0	Digital Hall Input	Asynchronous	ASR and AAR Disabled
Mode 3	Connected to AGND with R_{MODE2}	EN_ASR = 0, EN_AAR = 0	Analog Hall Input	Synchronous	ASR and AAR Disabled
Mode 4	Hi-Z	EN_ASR = 0, EN_AAR = 0	Digital Hall Input	Synchronous	ASR and AAR Disabled
Mode 5	Connected to AVDD with R_{MODE2}	EN_ASR = 1, EN_AAR = 1	Analog Hall Input	Synchronous	ASR and AAR Enabled
Mode 6	Connected to AVDD with R_{MODE1}	EN_ASR = 1, EN_AAR = 1	Digital Hall Input	Synchronous	ASR and AAR Enabled

ADVANCE INFORMATION

Table 8-6. PWM_MODE Configuration (continued)

MODE Type	MODE Pin (Hardware Variant)	MODE Bits (SPI Variant)	Hall Configuration	Modulation	ASR and AAR Mode
Mode 7	Connected to AVDD	EN_ASR = 1, EN_AAR = 1	Digital Hall Input	Synchronous	ASR and AAR Enabled

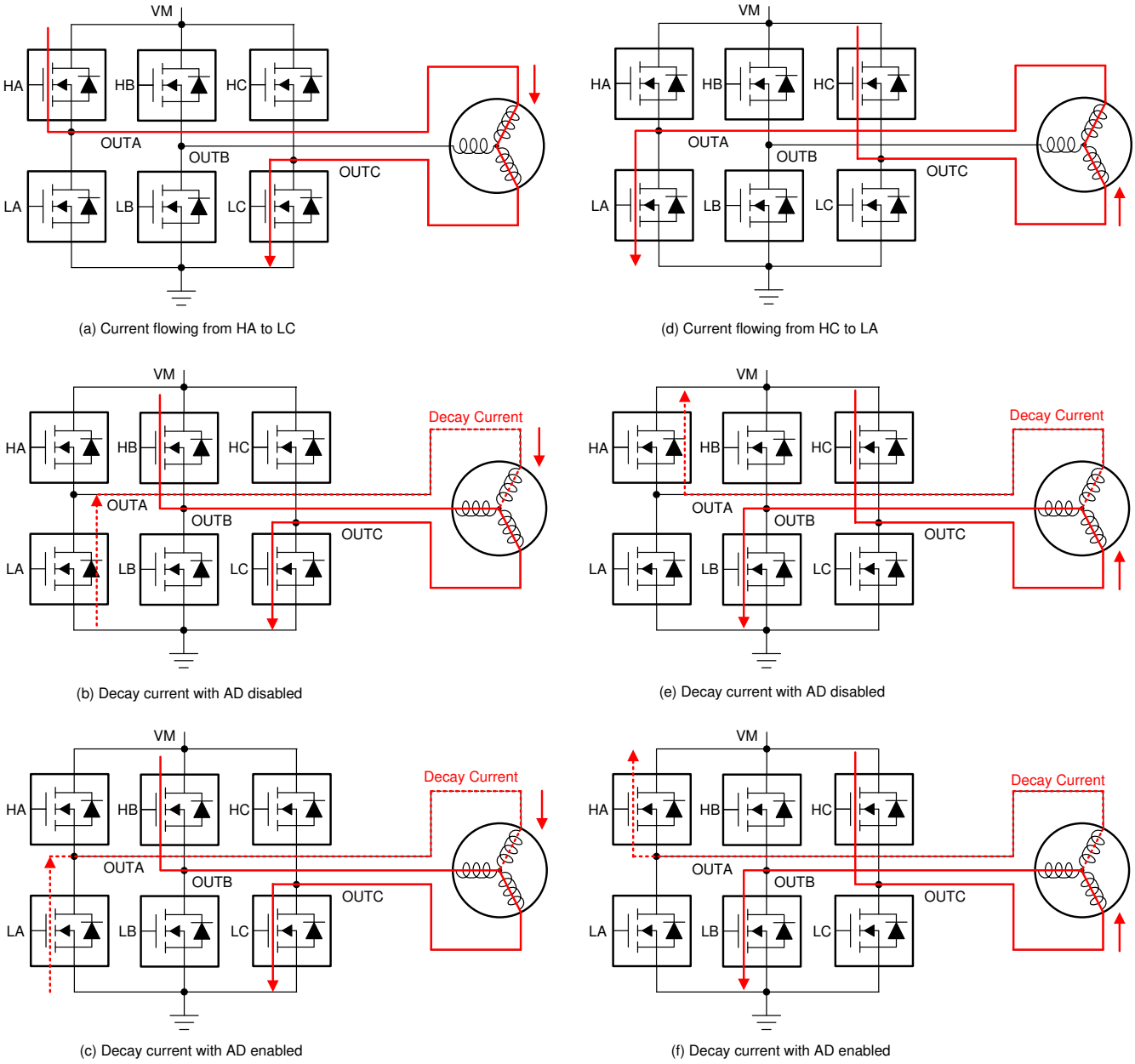
8.3.11.1 Automatic Synchronous Rectification Mode (ASR Mode)

The automatic synchronous rectification (ASR) mode is divided into two categories of ASR during commutation and ASR during PWM mode.

8.3.11.1.1 Automatic Synchronous Rectification in Commutation

Figure 8-30 shows the operation of active demagnetization during the BLDC motor commutation. As shown in Figure 8-30 (a), the current is flowing from HA to LC in one commutation state. During the commutation changeover as shown in Figure 8-30 (b), the HC switch is turned on, whereas the commutation current (due to motor inductance) in OUTA flows through the body diode of LA. This incorporates a higher diode loss depending on the commutation current. This commutation loss is reduced by turning on the LA for the commutation time as shown in Figure 8-30 (c).

Similarly the operation of high-side FET is realized in Figure 8-30 (d), (e) and (f).



(a) Current flowing from HA to LC

(d) Current flowing from HC to LA

(b) Decay current with AD disabled

(e) Decay current with AD disabled

(c) Decay current with AD enabled

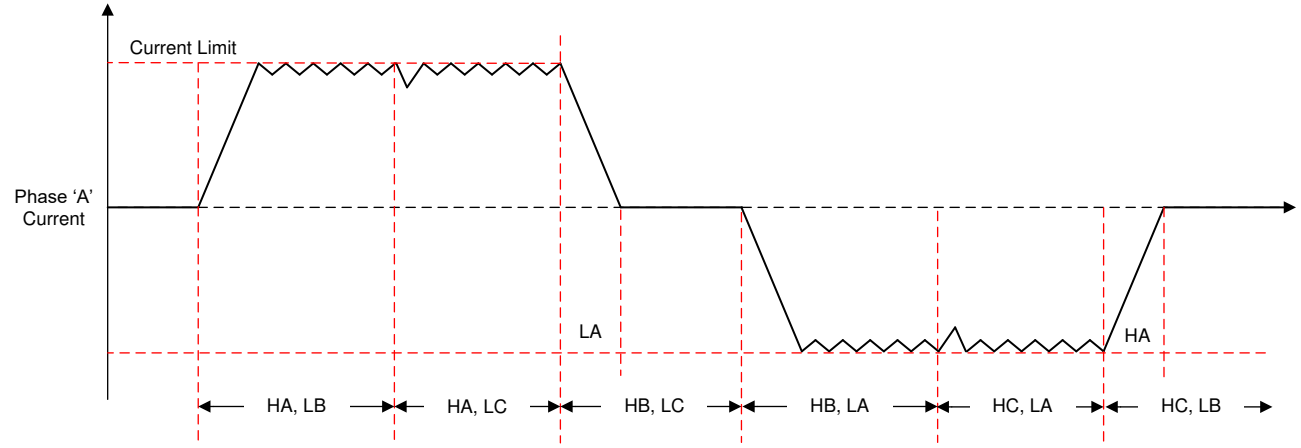
(f) Decay current with AD enabled

Figure 8-30. ASR in BLDC Motor Commutation

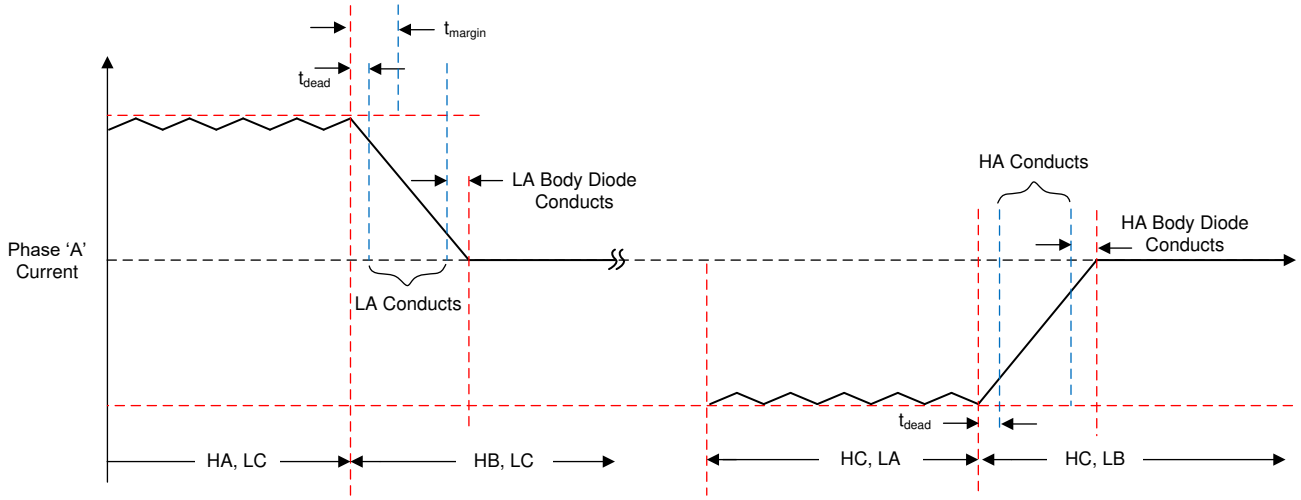
ADVANCE INFORMATION

Figure 8-31 (a) shows the BLDC motor phase current waveforms for automatic synchronous rectification mode in BLDC motor operating with trapezoidal commutation. This figure shows the operation of various switches in a single commutation cycle.

Figure 8-31 (b) shows the zoomed waveform of commutation cycle with details on the ASR mode start with margin time (t_{margin}) and ASR mode early stop due to active demag. comparator threshold and delays.



(a) Commutation current of Phase "A"



(b) Zoomed waveform of Active Demagnetization

Figure 8-31. Current Waveforms for ASR in BLDC Motor Commutation

8.3.11.1.2 Automatic Synchronous Rectification in PWM Mode

Figure 8-32 shows the operation of ASR in PWM mode. As shown in this figure, a PWM is applied only on the high-side FET, whereas the low-side FET is always off. During the PWM off time, current decays from the low-side FET which results in higher power losses. Therefore, this mode supports turning on the low-side FET during the low-side diode conduction.

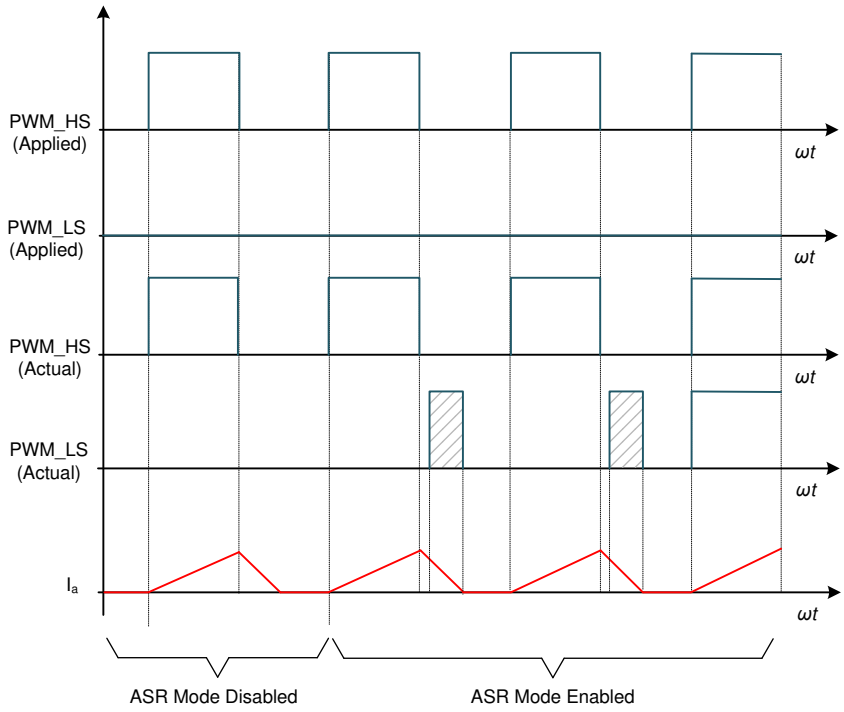


Figure 8-32. ASR in PWM Mode

ADVANCE INFORMATION

8.3.11.2 Automatic Asynchronous Rectification Mode (AAR Mode)

Figure 8-33 shows the operation of AAR in PWM mode. As shown in this figure, a PWM is applied in a synchronous rectification to the high-side and low-side FETs. During the low-side FET conduction, for lower inductance motors, the current can decay to zero and becomes negative since low side FET is in on-state. This creates a negative torque on the BLDC motor operation. When AAR mode is enabled, the current during the decay is monitored and the low-side FET is turned off as soon as the current reaches near to zero. This saves the negative current building in the BLDC motor which results in better noise performance and better thermal management.

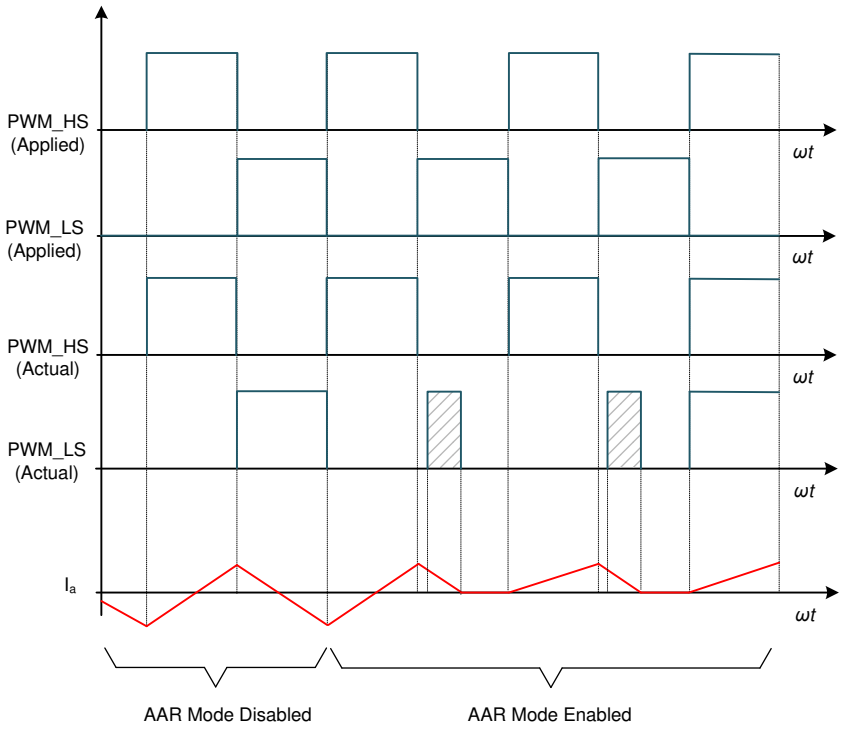


Figure 8-33. AAR in PWM Mode

8.3.12 Cycle-by-Cycle Current Limit

The current-limit circuit activates if the current flowing through the low-side MOSFET exceeds the I_{LIMIT} current. This feature restricts motor current to less than the I_{LIMIT}.

The current-limit circuitry utilizes the current sense amplifier output of the three phases compared with the voltage at ILIM pin. Figure 8-34 shows the implementation of current limit circuitry. As shown in this figure, the output of current sense amplifiers is combined with star connected resistive network. This measured voltage V_{MEAS} is compared with the external reference voltage e V_{ILIM} pin to realize the current limit implementation. The relation between current sensed on OUTX pin and V_{MEAS} threshold is given as:

$$V_{MEAS} = \left({}^{V_{AVDD}}/_{2}\right) - \left((I_{OUTA} + I_{OUTB} + I_{OUTC}) \times GAIN/3\right) \quad (3)$$

where

- AVDD is 3.3-V LDO output
- OUTX is current flowing into the low-side MOSFET
- GAIN is the CSA_GAIN setting

The I_{LIMIT} threshold can be adjusted by configuring ILIM pin between AVDD/2 to (AVDD/2 - 0.4) V. AVDD/2 is minimum value and when it is applied on ILIM pin cycle by cycle current limit is disabled, whereas maximum threshold of 8A can be configured by applying (AVDD/2 - 0.4) V on ILIM pin.

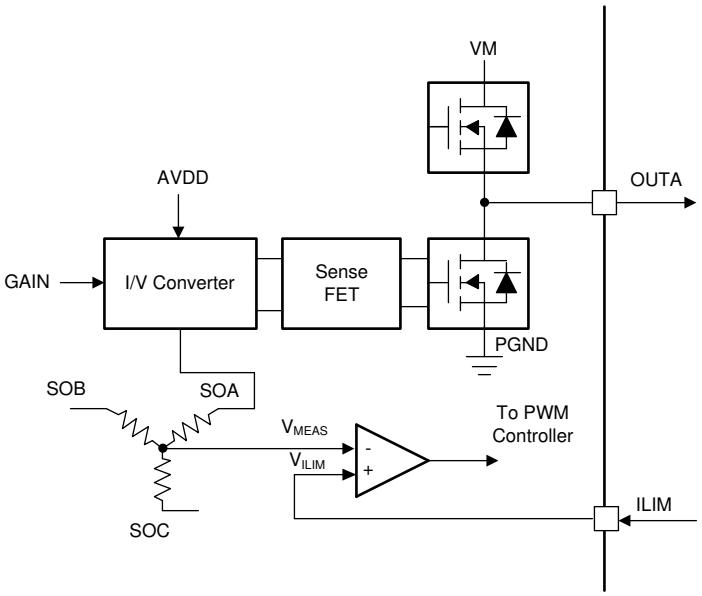


Figure 8-34. Current Limit Implementation

When then the current limit activates, the high-side FET is disabled until the beginning of the next PWM cycle as shown in Figure 8-35. The low-side FETs can operate in brake mode or high-Z mode by configuring the ILIM_RECIR bit in the SPI device variant.

ADVANCE INFORMATION

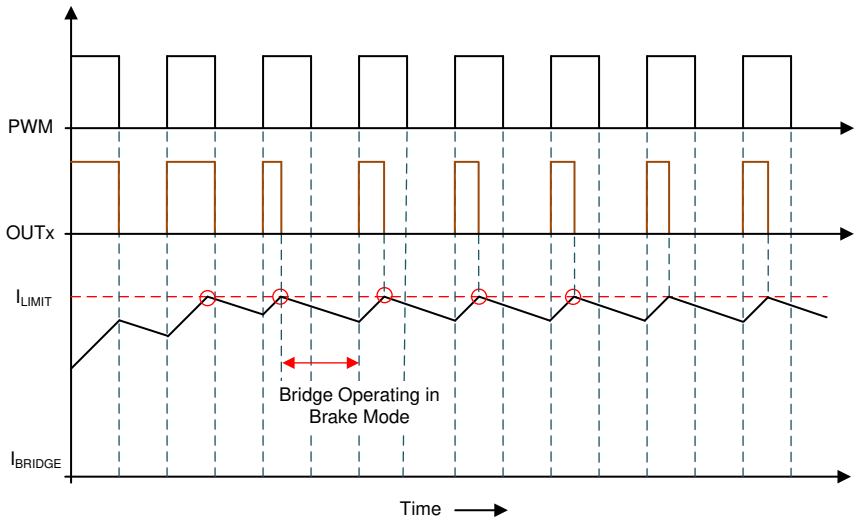


Figure 8-35. Cycle-by-Cycle Current-Limit Operation

In the MCT8316Z device, when the current limit activates in synchronous rectification mode, the current recirculates through the low-side FETs while the high-side FETs are disabled as shown in Figure 8-36

Moreover, when the current limit activates in asynchronous rectification mode, the current recirculates through the body diodes of the low-side FETs while the high-side FETs are disabled as shown in Figure 8-37

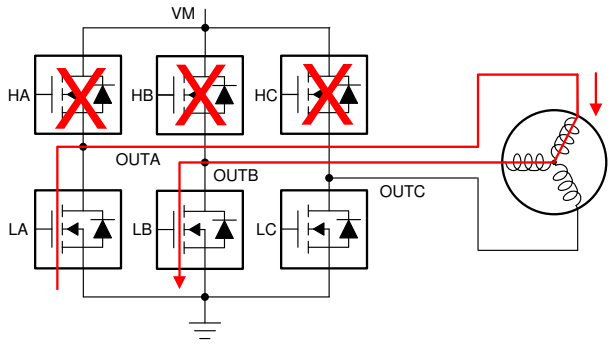


Figure 8-36. Brake State

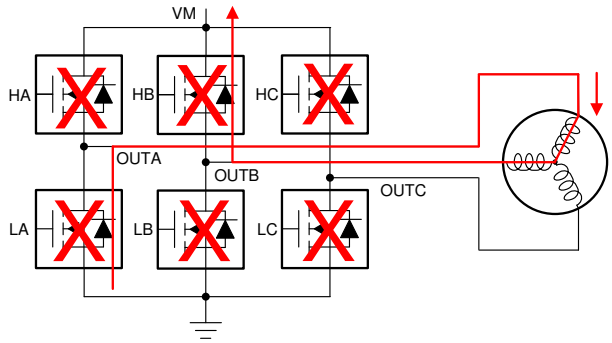


Figure 8-37. Coast State

Note

The current-limit circuit is ignored immediately after the PWM signal goes active for a short blanking time to prevent false trips of the current-limit circuit.

Note

During the brake operation, a high-current can flow through the low-side FETs which can eventually trigger the over current protection circuit. This allows the body-diode of the high-side FET to conduct and pump brake energy to the VM supply rail.

ADVANCE INFORMATION

8.3.12.1 Cycle by Cycle Current Limit with 100% Duty Cycle Input

In case of 100% duty cycle applied on PWM input, there is no edge available to turn high-side FET back on. To overcome this problem, MCT8316Z has built in internal PWM clock which is used to turn high-side FET back on once it is disabled after exceeding I_{LIMIT} threshold. In SPI variant MCT8316ZR, this internal PWM clock can be configured to either 20 kHz or 40 kHz through PWM_100_DUTY_SEL. In H/W variant MCT8316ZT PWM internal clock is set to 20 kHz. Figure 8-38 shows operation with 100 % duty cycle.

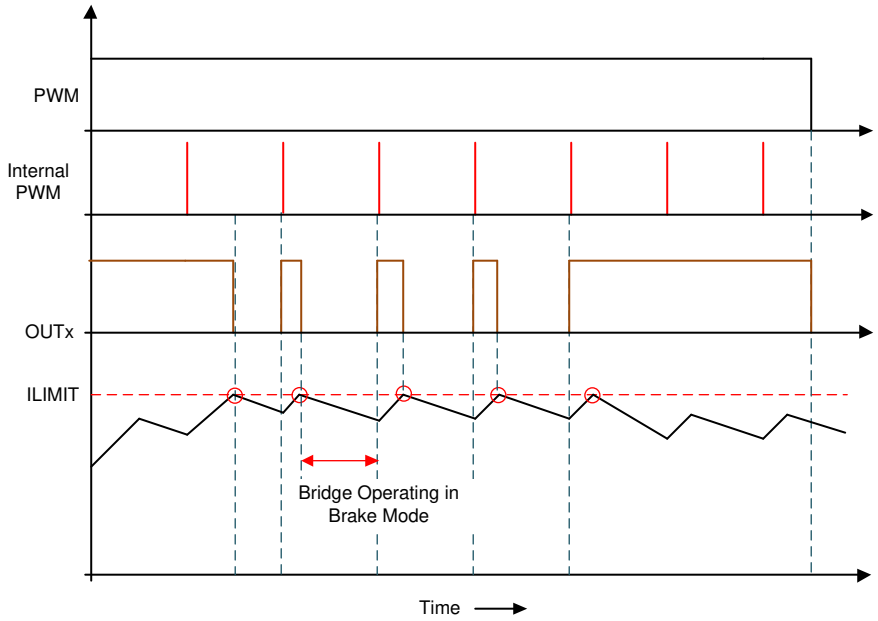


Figure 8-38. Cycle-by-Cycle Current-Limit Operation with 100% PWM Duty Cycle

8.3.13 Hall Comparators (Analog Hall Inputs)

Three comparators are provided to process the raw signals from the Hall-effect sensors to commutate the motor. The Hall comparators sense the zero crossings of the differential inputs and pass the information to digital logic. The Hall comparators have hysteresis, and their detect threshold is centered at 0. The hysteresis is defined as shown in Figure 8-39.

In addition to the hysteresis, the Hall inputs are deglitched with a circuit that ignores any extra Hall transitions for a period of t_{HDEG} after sensing a valid transition. Ignoring these transitions for the t_{HDEG} time prevents PWM noise from being coupled into the Hall inputs, which can result in erroneous commutation.

If excessive noise is still coupled into the Hall comparator inputs, adding capacitors between the positive and negative inputs of the Hall comparators may be required. The ESD protection circuitry on the Hall inputs implements a diode to the AVDD pin. Because of this diode, the voltage on the Hall inputs should not exceed the AVDD voltage.

Because the AVDD pin is disabled in sleep mode (nSLEEP inactive), the Hall inputs should not be driven by external voltages in sleep mode. If the Hall sensors are powered externally, the supply to the Hall sensors should be disabled if the MCT8316Z device is put into sleep mode. In addition, the Hall sensors' power supply should be powered up after enabling the motor otherwise an invalid Hall state may cause a delay in motor operation.

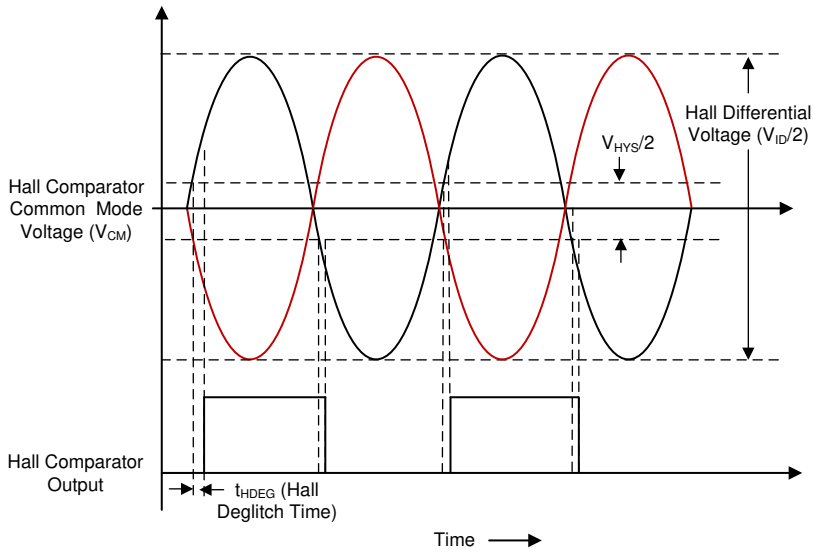


Figure 8-39. Hall Comparators Operation

ADVANCE INFORMATION

8.3.14 Advance Angle

The MCT8316Z includes device an advance angle feature to advance the commutation by a specified electrical angle based on the voltage on the ADVANCE pin (in H/W device variant) or the ADVANCE bits (in SPI device variant). Figure 8-40 shows the operation of advance angle feature.

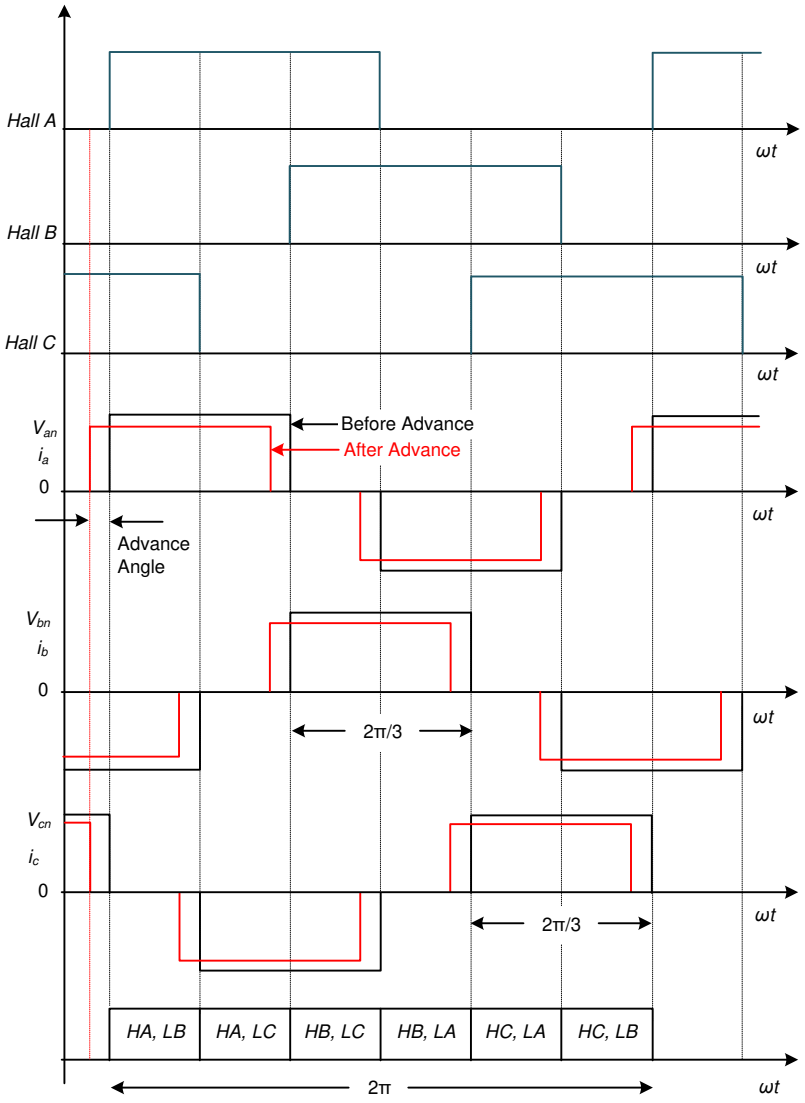


Figure 8-40. Advance Angle

8.3.15 FGOUT Signal

The MCT8316Z device also has an open-drain FGOUT signal that can be used for closed-loop speed control of a BLDC motor. This signal includes the information of all three Hall-elements inputs as shown in Section 8.3.15. In the MCT8316ZR (SPI variant), FGOUT can be configured to be a different division factor of Hall signals as shown in Section 8.3.15. In the MCT8316ZT (Hardware variant), the default mode is FGOUT = 00b.

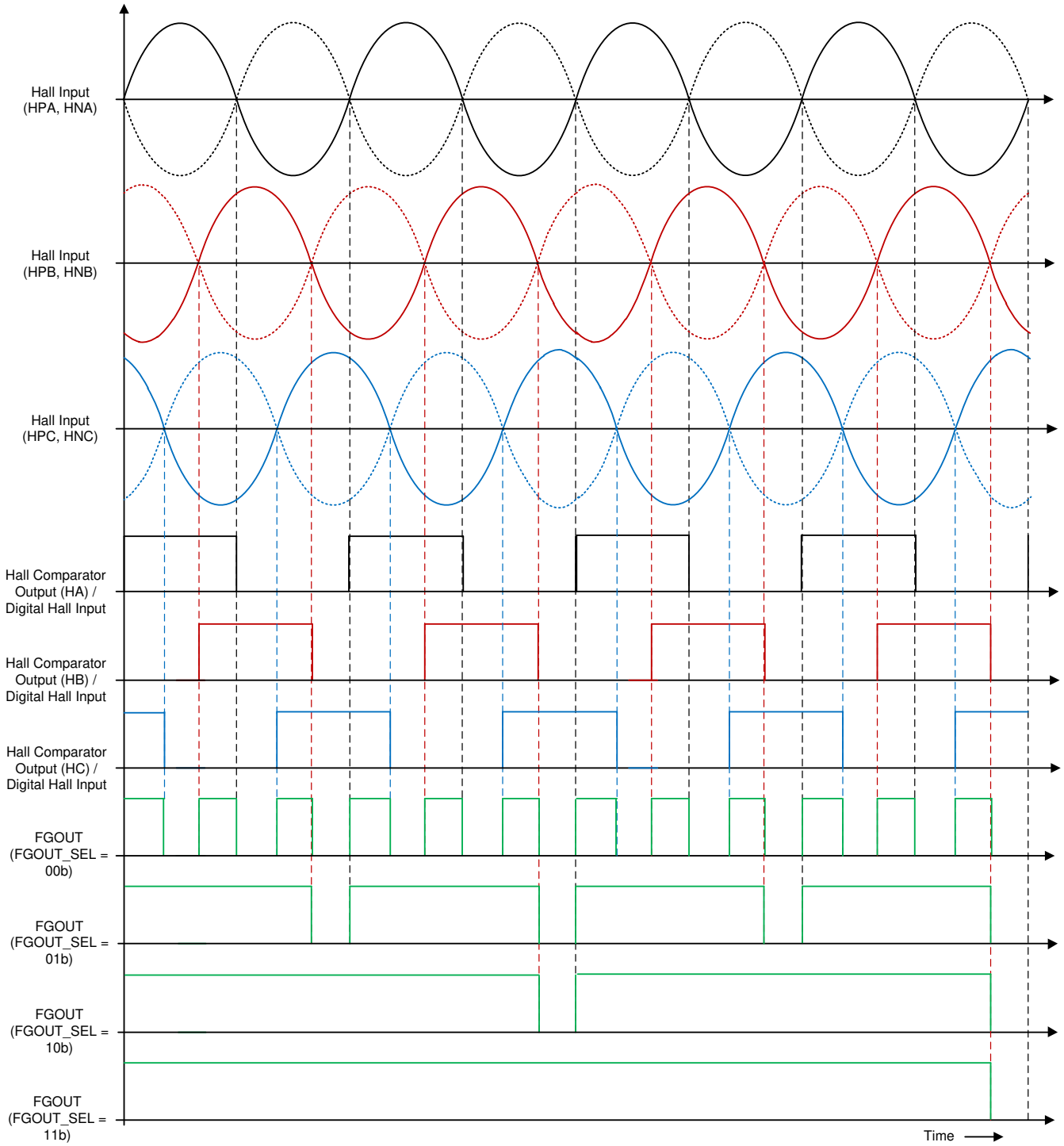


Figure 8-41. FGOUT Signal

ADVANCE INFORMATION

8.3.16 Protections

The MCT8316Z family of devices is protected against VM undervoltage, charge pump undervoltage, and overcurrent events. Table 8-7 summarizes various faults details.

Table 8-7. Fault Action and Response (SPI Devices)

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
VM undervoltage (NPOR)	$V_{VM} < V_{UVLO}$	—	—	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO\_R}$ CLR_FLT, nSLEEP Reset Pulse (NPOR bit)
AVDD undervoltage (NPOR)	$V_{AVDD} < V_{AVDD\_UV}$	—	nFAULT	Hi-Z	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_UV\_R}$ CLR_FLT, nSLEEP Reset Pulse (NPOR bit)
Buck undervoltage (BUCK_UV)	$V_{FB\_BK} < V_{BK\_UV}$	—	nFAULT	Active	Active	Automatic: $V_{FB\_BK} > V_{BUCK\_UV\_R}$ CLR_FLT, nSLEEP Reset Pulse (BUCK_UV bit)
Charge pump undervoltage (VCP_UV)	$V_{CP} < V_{CPUV}$	—	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$ CLR_FLT, nSLEEP Reset Pulse (VCP_UV bit)
OverVoltage Protection (OVP)	$V_{VM} > V_{OVP}$	OVP_EN = 0b	None	Active	Active	No action (OVP Disabled)
		OVP_EN = 1b	FAULT	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$ CLR_FLT, nSLEEP Reset Pulse (OVP bit)
Overcurrent Protection (OCP)	$I_{PHASE} > I_{OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	Automatic: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 11b	None	Active	Active	No action
Buck Overcurrent Protection (BUCK_OCP)	$I_{BK} > I_{BK\_OC}$	—	nFAULT	Active	Active	Retry: t_{RETRY}
SPI Error (SPI_FLT)	SCLK fault and ADDR fault	SPI_FLT_REP = 0b	nFAULT	Active	Active	Automatic: CLR_FLT, nSLEEP Reset Pulse (SPI_FLT bit)
		SPI_FLT_REP = 1b	None	Active	Active	No action
OTP Error (OTP_ERR)	OTP reading is erroneous	—	nFAULT	Hi-Z	Active	Latched: Power Cycle, nSLEEP Reset Pulse
Motor Lock (MTR_LOCK)	No Hall Signals > $t_{MTR\_LOCK\_TDET}$	MTR_LOCK_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Pulse (MTR_LOCK bit)
		MTR_LOCK_MODE = 01b	nFAULT	Hi-Z	Active	Retry: $t_{MTR\_LOCK\_RETRY}$
		MTR_LOCK_MODE = 10b	nFAULT	Active	Active	Automatic: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		MTR_LOCK_MODE = 11b	None	Active	Active	No action
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 0b	None	Active	Active	No action
		OTW_REP = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{HYS}$ CLR_FLT, nSLEEP Pulse (OTW bit)
Thermal shutdown (OTSD)	$T_J > T_{OTSD}$	—	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{OTSD} - T_{HYS}$ CLR_FLT, nSLEEP Pulse (OTS bit)

8.3.16.1 VM Supply Undervoltage Lockout (NPOR)

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all of the integrated FETs, driver charge-pump and digital logic controller are disabled as shown in Figure 8-42. Normal operation resumes (driver operation) when the VM undervoltage condition is removed. The NPOR bit is reset and latched low in the IC status (IC_STAT) register once the device presumes VM. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

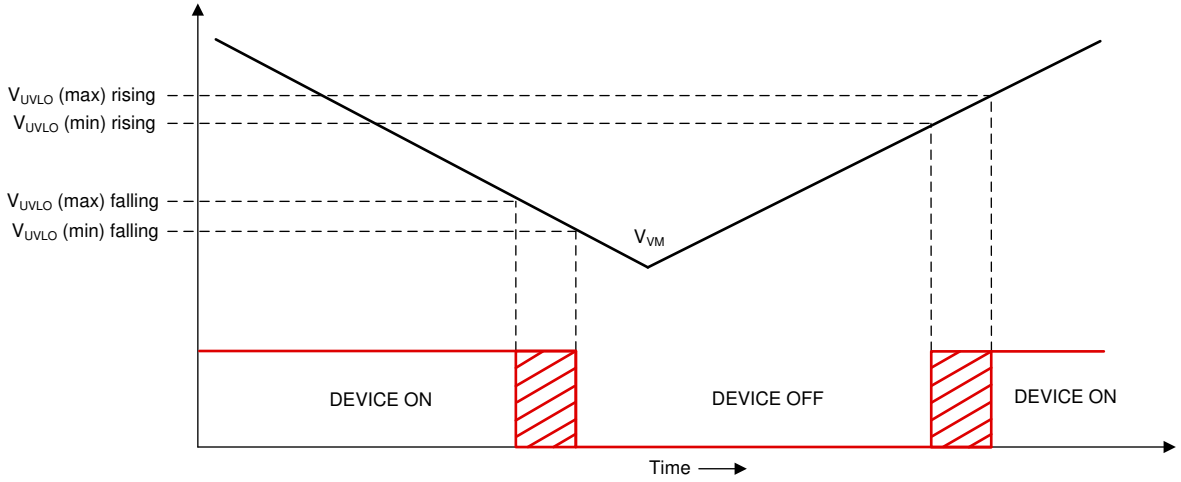


Figure 8-42. VM Supply Undervoltage Lockout

8.3.16.2 AVDD Undervoltage Lockout (AVDD_UV)

If at any time the voltage on AVDD pin falls lower than the V_{AVDD_UV} threshold, all of the integrated FETs, driver charge-pump and digital logic controller are disabled. Normal operation resumes (driver operation) when the AVDD undervoltage condition is removed. The NPOR bit is reset and latched low in the IC status (IC_STAT) register once the device presumes VM. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

8.3.16.3 BUCK Undervoltage Lockout (BUCK_UV)

If at any time the voltage on VFB_BK pin falls lower than the V_{BK_UV} threshold, the integrated FETs of the buck regulator are disabled while the driver FETs, charge pump, and digital logic control continue to operate normally. The nFAULT pin is driven low in the event of a buck undervoltage fault, and the BK_FLT bit in IC_STAT register is set in SPI devices. The FAULT and BUCK_UV bits are also latched high in the registers on SPI devices. Normal operation starts again (buck regulator operation and the nFAULT pin is released) when the BUCK undervoltage condition clears. The BK_FLT and BUCK_UV bits stay set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

8.3.16.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold voltage of the charge pump, all of the integrated FETs are disabled and the nFAULT pin is driven low. The FAULT and VCP_UV bits are also latched high in the registers on SPI devices. Normal operation starts again (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The CPUV bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). The CPUV protection is always enabled in both hardware and SPI device varaints.

8.3.16.5 Overvoltage Protections (OV)

If at any time input supply voltage on the VM pins rises higher lower than the V_{OVP} threshold voltage, all of the integrated FETs are disabled and the nFAULT pin is driven low. The FAULT and OVP bits are also latched high in the registers on SPI devices. Normal operation starts again (driver operation and the nFAULT pin is released) when the OVP condition clears. The OVP bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin

ADVANCE INFORMATION

reset pulse (t_{RST}). Setting the OVP_EN bit high on the SPI devices enables this protection feature. On hardware interface devices, the OVP protection is always enabled and set to a 34-V threshold.

The OVP threshold is also programmable on the SPI device variant. The OVP threshold can be set to 20-V or 32-V based on the OVP_SEL bit.

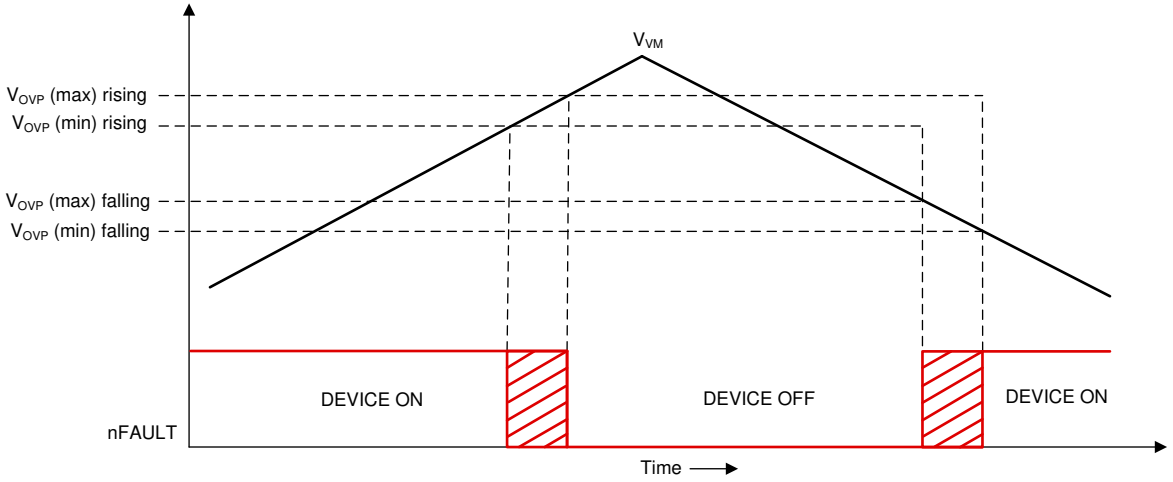


Figure 8-43. Over Voltage Protection

8.3.16.6 Overcurrent Protection (OCP)

A MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the t_{OCP} deglitch time, an OCP event is recognized and action is done according to the OCP_MODE bit. On hardware interface devices, the I_{OCP} threshold is fixed at 16-A threshold, the t_{OCP_DEG} is fixed at 0.6-µs, and the OCP_MODE bit is configured for latched shutdown. On SPI devices, the I_{OCP} threshold is set through the OCP_LVL SPI register, the t_{OCP_DEG} is set through the OCP_DEG SPI register, and the OCP_MODE bit can operate in four different modes: OCP latched shutdown, OCP automatic retry, OCP report only, and OCP disabled.

8.3.16.6.1 OCP Latched Shutdown (OCP_MODE = 00b)

After a OCP event in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

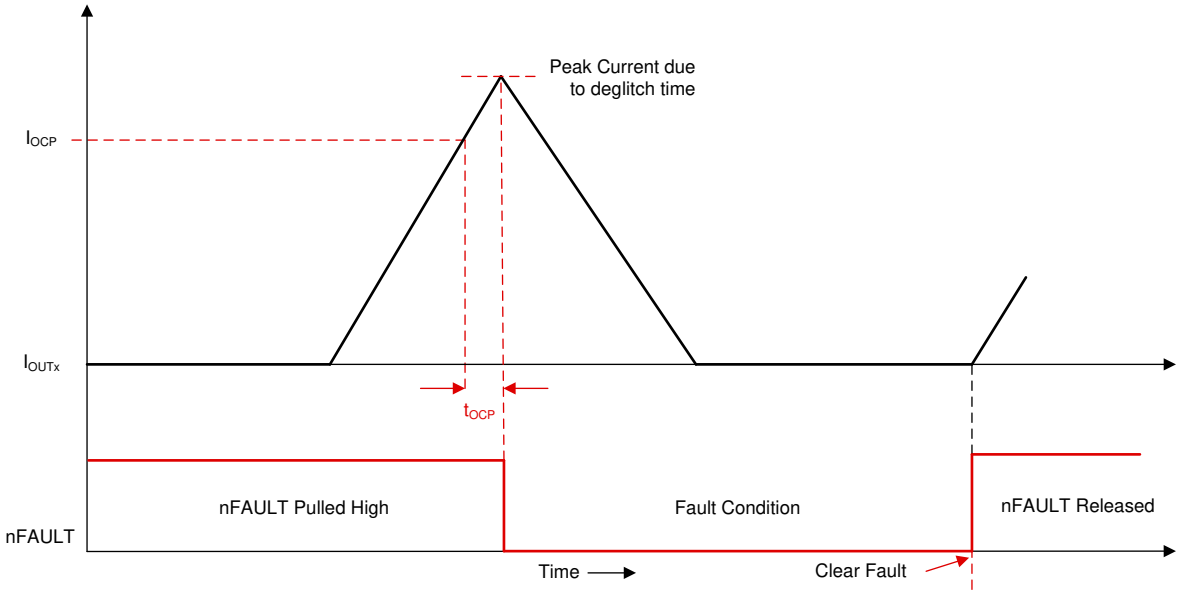


Figure 8-44. Overcurrent Protection - Latched Shutdown Mode

8.3.16.6.2 OCP Automatic Retry (OCP_MODE = 01b)

After a OCP event in this mode, all the FETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. After the t_{RETRY} time elapses, the FAULT, OCP, and corresponding FET's OCP bits stay latched until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

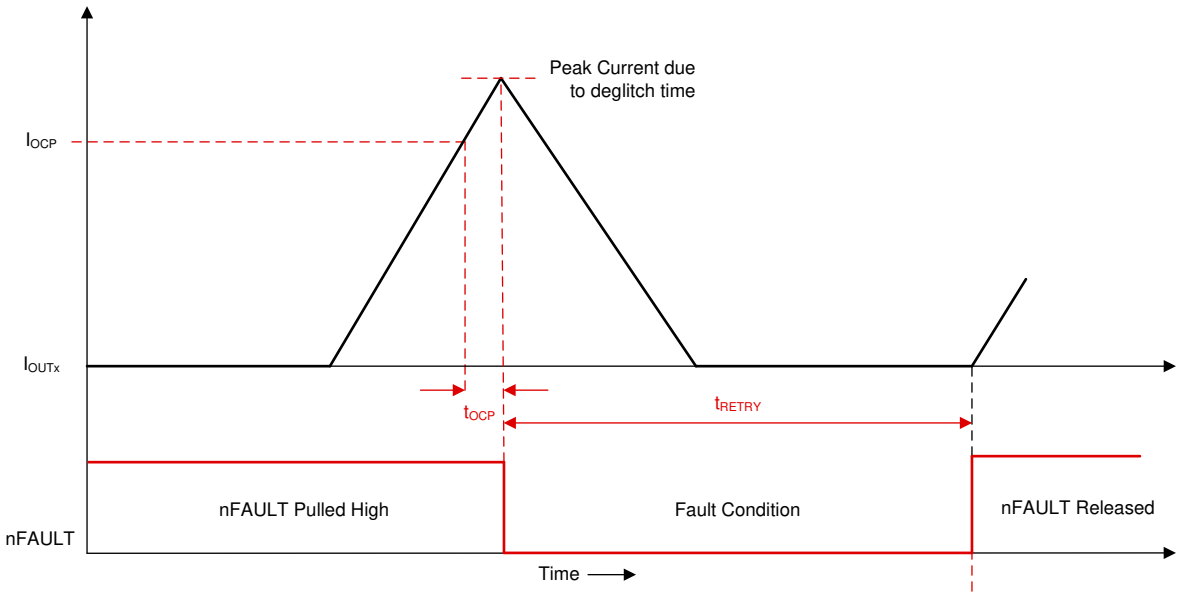


Figure 8-45. Overcurrent Protection - Automatic Retry Mode

8.3.16.6.3 OCP Report Only (OCP_MODE = 10b)

No protective action occurs after a OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, OCP, and corresponding FET's OCP bits high in the SPI registers. The MCT8316Z continues to operate as usual. The external controller manages the overcurrent condition by acting

ADVANCE INFORMATION

appropriately. The reporting clears (nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

8.3.16.6.4 OCP Disabled (OCP_MODE = 11b)

No action occurs after a OCP event in this mode.

8.3.16.7 Buck Overcurrent Protection

A buck overcurrent event is sensed by monitoring the current flowing through buck regulator's FETs. If the current across the buck regulator FET exceeds the I_{BK_OCP} threshold for longer than the t_{BK_OCP} deglitch time, an OCP event is recognized. The buck OCP mode is configured in automatic retry setting. In this setting, after a buck OCP event is detected, all the buck regulator's FETs are disabled and the nFAULT pin is driven low. The FAULT, BK_FLT, and BUCK_OCP bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{BK_RETRY} time elapses. The FAULT, BK_FLT, and BUCK_OCP bits stay latched until the t_{RETRY} period expires.

8.3.16.8 Motor Lock (MTR_LOCK)

During motor is in lock condition the hall signals will be not available, so a Motor Lock event is sensed by monitoring the hall signals. If the hall signals are not present for for longer than the t_{MTR_LOCK}, a MTR_LCK event is recognized and action is done according to the MTR_LOCK_MODE bits. On hardware interface devices, the t_{MTR_LOCK} threshold is set to 1000-ms, and the MTR_LOCK_MODE bit is configured for latched shutdown. On SPI devices, the t_{MTR_LOCK} threshold is set through the MTR_LOCK_TDET register and the MTR_LOCK_MODE bit can operate in four different modes: MTR_LOCK latched shutdown, MTR_LOCK automatic retry, MTR_LOCK report only, and MTR_LOCK disabled.

8.3.16.8.1 MTR_LOCK Latched Shutdown (MTR_LOCK_MODE = 00b)

After a motor lock event in this mode, all FETs are disabled and the nFAULT pin is driven low. The FAULT and MTR_LOCK bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

8.3.16.8.2 MTR_LOCK Automatic Retry (MTR_LOCK_MODE = 01b)

After a motor lock event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and MTR_LOCK bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the $t_{MTR\_LOCK\_RETRY}$ time elapses. The FAULT and MTR_LOCK bits stay latched until the $t_{MTR\_LOCK\_RETRY}$ period expires.

8.3.16.8.3 MTR_LOCK Report Only (MTR_LOCK_MODE= 10b)

No protective action occurs after a MTR_LOCK event in this mode. The motor lock event is reported by driving the nFAULT pin low and latching the FAULT and MTR_LOCK bits high in the SPI registers. The MCT8316Z continues to operate as usual. The external controller manages the motor lock condition by acting appropriately. The reporting clears (nFAULT pin is released) when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

8.3.16.8.4 MTR_LOCK Disabled (MTR_LOCK_MODE = 11b)

No action occurs after a MTR_LOCK event in this mode.

8.3.16.8.5

Note

The motor lock detection scheme requires the PWM off-time (t_{PWM_OFF}) to be lower than the motor lock detection time (t_{MTR_LOCK})

8.3.16.9 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OT bit in the IC status (IC_STAT) register and OTW bit in the status register is set. The reporting of OTW on the nFAULT pin can be enabled by

ADVANCE INFORMATION

setting the over-temperature warning reporting (OTW_REP) bit in the configuration control register. The device performs no additional action and continues to function. In this case, the nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}) and the die temperature is lower than thermal warning trip (T_{OTW}).

Note

Over temperature warning is not reported on nFAULT pin by default.

8.3.16.10 Thermal Shutdown (OTS)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTS}), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and OT bit in the IC status (IC_STAT) register and OTS bit in the status register is set. Normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears. The OTS bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}). This protection feature cannot be disabled.

8.4 Device Functional Modes

8.4.1 Functional Modes

8.4.1.1 Sleep Mode

The nSLEEP pin manages the state of the MCT8316Z family of devices. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all FETs are disabled, sense amplifiers are disabled, buck regulator (if present) is disabled, the charge pump is disabled, the AVDD regulator is disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all MOSFETs are disabled.

Note

During power up and power down of the device through the nSLEEP pin, the nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the t_{SLEEP} or t_{WAKE} time.

8.4.1.2 Operating Mode

When the nSLEEP pin is high and the V_{VM} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, AVDD regulator, buck regulator, and SPI bus are active.

8.4.1.3 Fault Reset (CLR_FLT or nSLEEP Reset Pulse)

In the case of device latched faults, the MCT8316Z family of devices goes to a partial shutdown state to help protect the power MOSFETs and system.

When the fault condition clears, the device can go to the operating state again by either setting the CLR_FLT SPI bit on SPI devices or issuing a reset pulse to the nSLEEP pin on either interface variant. The nSLEEP reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the nSLEEP pin. The low period of the sequence should fall with the t_{RST} time window or else the device will start the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks.

8.4.2 DRVOFF functionality

When DRVOFF pin is high, all six MOSFETs are disabled. If nSLEEP is high when the DRVOFF pin is high, the charge pump, AVDD regulator, buck regulator, and SPI bus are active and any driver-related faults such as OCP will be inactive.

ADVANCE INFORMATION

8.5 SPI Communication

8.5.1 Programming

On MCT8316Z SPI devices, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16-bit word, with a 6-bit address and 8 bits of data. The SPI output consists of 16 bit word, with a 8 bits of status information (STAT register) and 8-bit register data.

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of the SCLK pin and data is propagated on the rising edge of the SCLK pin.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit status data.

The SPI registers are reset to the default settings on power up and when the device is enters sleep mode

8.5.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B15)
- 6 address bits, A (bits B14 through B9)
- Parity bit, P (bit B8)
- 8 data bits, D (bits B7 through B0)

The SDO output data word is 16 bits long and the first 8 bits are status bits. The data word is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

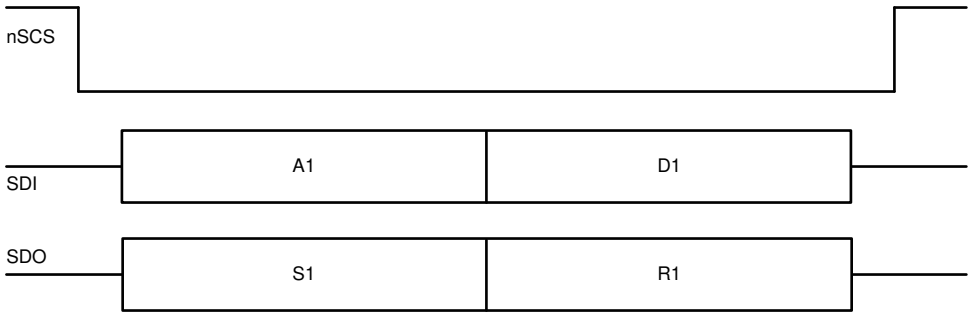


Figure 8-46.

ADVANCE INFORMATION

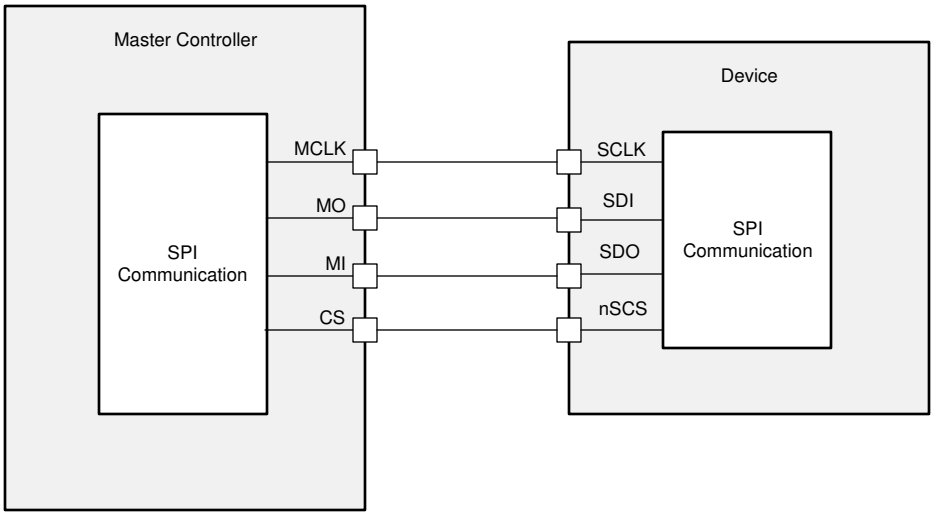


Figure 8-47.

Table 8-8. SDI Input Data Word Format

R/W	ADDRESS							Parity	DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	A5	A4	A3	A2	A1	A0	P	D7	D6	D5	D4	D3	D2	D1	D0

Table 8-9. SDO Output Data Word Format

STATUS								DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
S7	S6	S5	S4	S3	S2	S1	S0	D7	D6	D5	D4	D3	D2	D1	D0

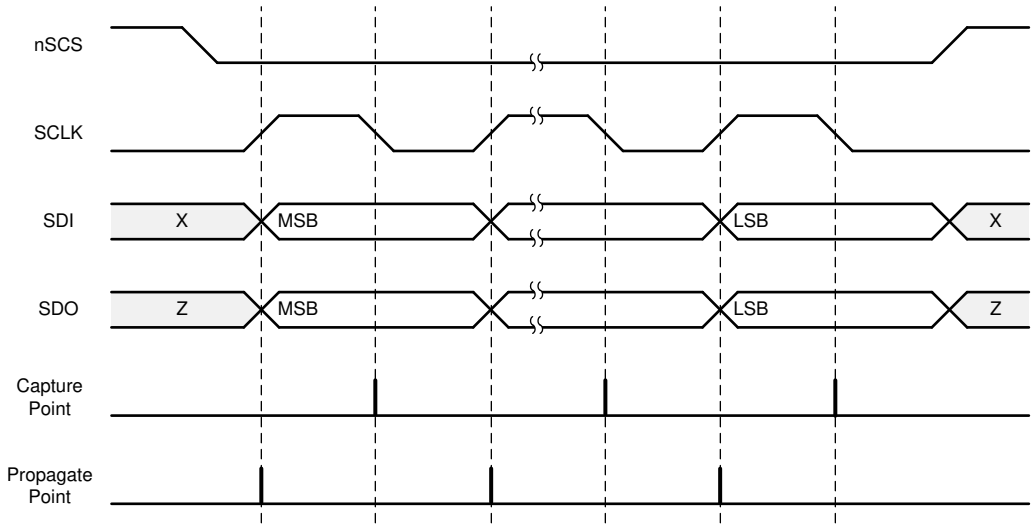


Figure 8-48. SPI Slave Timing Diagram

8.6 Register Map

8.6.1 STATUS Registers

Table 8-10 lists the STATUS registers. All register offset addresses not listed in Table 8-10 should be considered as reserved locations and the register contents should not be modified.

Status Configuration

Table 8-10. STATUS Registers

Address	Acronym	Register Name	Section
0x0	IC_Status_	IC Status Register	Go
0x1	Status__1	Status Register 1	Go
0x2	Status__2	Status Register 2	Go

Complex bit access types are encoded to fit into small table cells. Table 8-11 shows the codes that are used for access types in this section.

Table 8-11. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Reset or Default Value		
- *n*		Value after reset or the default value

8.6.1.1 IC_Status_ Register (Address = 0x0) [Reset = 0x0]

IC_Status_ is shown in Table 8-12.

Return to the Summary Table.

Table 8-12. IC_Status_ Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MTR_LOCK	R	0x0	Motor Lock Staus Bit 0x0 = No motor lock is detected 0x1 = Motor lock is detected
6	BK_FLT	R	0x0	Buck Fault Bit 0x0 = No buck regulator fault condition is detected 0x1 = Buck regulator fault condition is detected
5	SPI_FLT	R	0x0	SPI Fault Bit 0x0 = No SPI fault condition is detected 0x1 = SPI Fault condition is detected
4	OCP	R	0x0	Over Current Protection Status Bit 0x0 = No overcurrent condition is detected 0x1 = Overcurrent condition is detected
3	NPOR	R	0x0	Supply Power On Reset Bit 0x0 = Power on reset condition is detected on VM 0x1 = No power-on-reset condition is detected on VM
2	OVP	R	0x0	Supply Overvoltage Protection Status Bit 0x0 = No overvoltage condition is detected on VM 0x1 = Overvoltage condition is detected on VM
1	OT	R	0x0	Overtemperature Fault Status Bit 0x0 = No overtemperature warning / shutdown is detected 0x1 = Overtemperature warning / shutdown is detected
0	FAULT	R	0x0	Device Fault Bit 0x0 = No fault condition is detected 0x1 = Fault condition is detected

8.6.1.2 Status__1 Register (Address = 0x1) [Reset = 0x0]

Status__1 is shown in Table 8-13.

Return to the Summary Table.

Table 8-13. Status__1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTW	R	0x0	Overtemperature Warning Status Bit 0x0 = No overtemperature warning is detected 0x1 = Overtemperature warning is detected
6	OTS	R	0x0	Overtemperature Shutdown Status Bit 0x0 = No overtemperature shutdown is detected 0x1 = Overtemperature shutdown is detected
5	OCP_HC	R	0x0	Overcurrent Status on High-side switch of OUTC 0x0 = No overcurrent detected on high-side switch of OUTC 0x1 = Overcurrent detected on high-side switch of OUTC
4	OCL_LC	R	0x0	Overcurrent Status on Low-side switch of OUTC 0x0 = No overcurrent detected on low-side switch of OUTC 0x1 = Overcurrent detected on low-side switch of OUTC
3	OCP_HB	R	0x0	Overcurrent Status on High-side switch of OUTB 0x0 = No overcurrent detected on high-side switch of OUTB 0x1 = Overcurrent detected on high-side switch of OUTB
2	OCP_LB	R	0x0	Overcurrent Status on Low-side switch of OUTB 0x0 = No overcurrent detected on low-side switch of OUTB 0x1 = Overcurrent detected on low-side switch of OUTB
1	OCP_HA	R	0x0	Overcurrent Status on High-side switch of OUTA 0x0 = No overcurrent detected on high-side switch of OUTA 0x1 = Overcurrent detected on high-side switch of OUTA
0	OCP_LA	R	0x0	Overcurrent Status on Low-side switch of OUTA 0x0 = No overcurrent detected on low-side switch of OUTA 0x1 = Overcurrent detected on low-side switch of OUTA

8.6.1.3 Status__2 Register (Address = 0x2) [Reset = 0x0]

Status__2 is shown in Table 8-14.

Return to the Summary Table.

Table 8-14. Status__2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OTP_ERR	R	0x0	One Time Programmabilty Error 0x0 = No OTP error is detected 0x1 = OTP Error is detected
5	BUCK_OCP	R	0x0	Buck Regulator Overcurrent Staus Bit 0x0 = No buck regulator overcurrent is detected 0x1 = Buck regulator overcurrent is detected
4	BUCK_UV	R	0x0	Buck Regulator Undervoltage Staus Bit 0x0 = No buck regulator undervoltage is detected 0x1 = Buck regulator undervoltage is detected
3	VCP_UV	R	0x0	Charge Pump Undervoltage Status Bit 0x0 = No charge pump undervoltage is detected 0x1 = Charge pump undervoltage is detected
2	SPI_PARITY	R-0	0x0	SPI Parity Error Bit 0x0 = No SPI parity error is detected 0x1 = SPI parity error is detected
1	SPI_SCLK_FLT	R	0x0	SPI Clock Framing Error Bit 0x0 = No SPI clock framing error is detected 0x1 = SPI clock framing error is detected
0	SPI_ADDR_FLT	R	0x0	SPI Address Error Bit 0x0 = No SPI address fault is detected (due to accessing non-user register) 0x1 = SPI address fault is detected

8.6.2 CONTROL Registers

Table 8-15 lists the CONTROL registers. All register offset addresses not listed in Table 8-15 should be considered as reserved locations and the register contents should not be modified.

Control Configuration

Table 8-15. CONTROL Registers

Address	Acronym	Register Name	Section
0x3	Control__1	Control Register 1	Go
0x4	Control__2A	Control Register 2A	Go
0x5	Control__3	Control Register 3	Go
0x6	Control__4	Control Register 4	Go
0x7	Control__5	Control Register 5	Go
0x8	Control__6	Control Register 6	Go
0x9	Control__7	Control Register 7	Go
0xA	Control__8	Control Register 8	Go
0xB	Control__9	Control Register 9	Go
0xC	Control__10	Control Register 10	Go

Complex bit access types are encoded to fit into small table cells. Table 8-16 shows the codes that are used for access types in this section.

Table 8-16. CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WAPU	W APU	Write Atomic write with password unlock
Reset or Default Value		
- *n*		Value after reset or the default value

ADVANCE INFORMATION

8.6.2.1 Control__1 Register (Address = 0x3) [Reset = 0x11]

Control__1 is shown in Table 8-17.

Return to the Summary Table.

Table 8-17. Control__1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x2	Reserved
2-0	REG_LOCK	R/WAPU	0x1	Register Lock Bits 0x0 = No effect unless locked or unlocked 0x1 = No effect unless locked or unlocked 0x2 = No effect unless locked or unlocked 0x3 = Write 011b to this register to unlock all registers 0x4 = No effect unless locked or unlocked 0x5 = No effect unless locked or unlocked 0x6 = Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x03h bits 2-0. 0x7 = No effect unless locked or unlocked

8.6.2.2 Control__2A Register (Address = 0x4) [Reset = 0x20]

Control__2A is shown in Table 8-18.

Return to the Summary Table.

Table 8-18. Control__2A Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	SDO_MODE	R/W	0x1	SDO Mode Setting 0x0 = SDO IO in Open Drain Mode 0x1 = SDO IO in Push Pull Mode
4-3	SLEW	R/W	0x0	Slew Rate Settings 0x0 = Slew rate is 25 V/µs 0x1 = Slew rate is 50 V/µs 0x2 = Slew rate is 150 V/µs 0x3 = Slew rate is 200 V/µs
2-1	PWM_MODE	R/W	0x0	Device Mode Selection 0x0 = Asynchronous rectification with analog Hall 0x1 = Asynchronous rectification with digital Hall 0x2 = Synchronous rectification with analog Hall 0x3 = Synchronous rectification with digital Hall
0	CLR_FLT	W1C	0x0	Clear Fault 0x0 = No clear fault command is issued 0x1 = To clear the latched fault bits. This bit automatically resets after being written.

8.6.2.3 Control__3 Register (Address = 0x5) [Reset = 0x0]

Control__3 is shown in Table 8-19.

Return to the Summary Table.

Table 8-19. Control__3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	PWM_100_DUTY_SEL	R/W	0x0	Freqency of PWM at 100% Duty Cycle 0x0 = 20KHz 0x1 = 40KHz
3	OVP_SEL	R/W	0x0	Overvoltage Level Setting 0x0 = VM overvoltage level is 34-V 0x1 = VM overvoltage level is 22-V
2	OVP_EN	R/W	0x0	Overvoltage Enable Bit 0x0 = Overvoltage protection is disabled 0x1 = Overvoltage protection is enabled
1	SPI_FLT_REP	R/W	0x0	SPI Fault Reporting Disable Bit 0x0 = SPI fault reporting on nFAULT pin is enabled 0x1 = SPI fault reporting on nFAULT pin is disabled
0	OTW_REP	R/W	0x0	Overtemperature Warning Reporting Bit 0x0 = Over temperature reporting on nFAULT is disabled 0x1 = Over temperature reporting on nFAULT is enabled

8.6.2.4 Control__4 Register (Address = 0x6) [Reset = 0x1]

Control__4 is shown in Table 8-20.

Return to the Summary Table.

Table 8-20. Control__4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DRV_OFF	R/W	0x0	Driver OFF Bit 0x0 = No Action 0x1 = Enter Low Power Standby Mode
6	OCP_CBC	R/W	0x0	OCP PWM Cycle Operation Bit 0x0 = OCP clearing in PWM input cycle change is disabled 0x1 = OCP clearing in PWM input cycle change is enabled
5-4	OCP_DEG	R/W	0x0	OCP Deglitch Time Settings 0x0 = OCP deglitch time is 0.2 µs 0x1 = OCP deglitch time is 0.6 µs 0x2 = OCP deglitch time is 1.1 µs 0x3 = OCP deglitch time is 1.6 µs
3	OCP_RETRY	R/W	0x0	OCP Retry Time Settings 0x0 = OCP retry time is 5 ms 0x1 = OCP retry time is 500 ms
2	OCP_LVL	R/W	0x0	Overcurrent Level Setting 0x0 = OCP level is 16 A 0x1 = OCP level is 24 A
1-0	OCP_MODE	R/W	0x1	OCP Fault Options 0x0 = Overcurrent causes a latched fault 0x1 = Overcurrent causes an automatic retrying fault 0x2 = Overcurrent is report only but no action is taken 0x3 = Overcurrent is not reported and no action is taken

8.6.2.5 Control__5 Register (Address = 0x7) [Reset = 0x0]

Control__5 is shown in Table 8-21.

Return to the Summary Table.

Table 8-21. Control__5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	ILIM_RECIR	R/W	0x0	Current Limit Recirculation Settings 0x0 = Current recirculation through FETs (Brake Mode) 0x1 = Current recirculation through diodes (Coast Mode)
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	EN_AAR	R/W	0x0	Active Asynshronous Rectification Enable Bit 0x0 = AAR mode is disabled 0x1 = AAR mode is enabled
2	EN_ASR	R/W	0x0	Active Synchronous Rectification Enable Bit 0x0 = ASR mode is disabled 0x1 = ASR mode is enabled
1-0	CSA_GAIN	R/W	0x0	Current Sense Amplifier's Gain Settings 0x0 = CSA gain is 0.15 V/A 0x1 = CSA gain is 0.3 V/A 0x2 = CSA gain is 0.6 V/A 0x3 = CSA gain is 1.2 V/A

8.6.2.6 Control__6 Register (Address = 0x8) [Reset = 0x0]

Control__6 is shown in Table 8-22.

Return to the Summary Table.

Table 8-22. Control__6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	BUCK_PS_DIS	R/W	0x0	Buck Power Sequencing Disable Bit 0x0 = Buck power sequencing is enabled 0x1 = Buck power sequencing is disabled
3	BUCK_CL	R/W	0x0	Buck Current Limit Setting 0x0 = Buck regulator current limit is set to 600 mA 0x1 = Buck regulator current limit is set to 150 mA
2-1	BUCK_SEL	R/W	0x0	Buck Voltage Selection 0x0 = Buck voltage is 3.3 V 0x1 = Buck voltage is 5.0 V 0x2 = Buck voltage is 4.0 V 0x3 = Buck voltage is 5.7 V
0	BUCK_DIS	R/W	0x0	Buck Disable Bit 0x0 = Buck regulator is enabled 0x1 = Buck regulator is disabled

8.6.2.7 Control__7 Register (Address = 0x9) [Reset = 0x1]

Control__7 is shown in Table 8-23.

Return to the Summary Table.

Table 8-23. Control__7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	HALL_HYS	R/W	0x0	Hall Comparator Hysteresis Settings 0x0 = 5 mV 0x1 = 50 mV
3	BRAKE_MODE	R/W	0x0	Brake Mode Setting 0x0 = Device operation is braking in brake mode 0x1 = Device operation is coasting in brake mode
2	COAST	R/W	0x0	Coast Bit 0x0 = Device coast mode is disabled 0x1 = Device coast mode is enabled
1	BRAKE	R/W	0x0	Brake Bit 0x0 = Device brake mode is disabled 0x1 = Device brake mode is enabled
0	DIR	R/W	0x1	Direction Bit 0x0 = Motor direction is set to clockwise direction 0x1 = Motor direction is set to anti-clockwise direction

8.6.2.8 Control__8 Register (Address = 0xA) [Reset = 0x41]

Control__8 is shown in Table 8-24.

Return to the Summary Table.

Table 8-24. Control__8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FG_MODE	R/W	0x1	Electrical Frequency Generation Output Mode Bits 0x0 = FGOUT frequency is commutation frequency 0x1 = FGOUT frequency is 1/2 of commutation frequency 0x2 = FGOUT frequency is 1/4 of commutation frequency 0x3 = FGOUT frequency is 1/8 of commutation frequency
5	RESERVED	R	0x0	Reserved
4	MTR_LOCK_RETRY	R/W	0x0	Motor Lock Retry Time Settings 0x0 = 500 ms 0x1 = 5000 ms
3-2	MTR_LOCK_TDET	R/W	0x0	Motor Lock Detection Time Settings 0x0 = 300 ms 0x1 = 500 ms 0x2 = 1000 ms 0x3 = 5000 ms
1-0	MTR_LOCK_MODE	R/W	0x1	Motor Lock Fault Options 0x0 = Motor lock causes a latched fault 0x1 = Motor lock causes an automatic retrying fault 0x2 = Motor lock is report only but no action is taken 0x3 = Motor lock is not reported and no action is taken

8.6.2.9 Control__9 Register (Address = 0xB) [Reset = 0x0]

Control__9 is shown in Table 8-25.

Return to the Summary Table.

Table 8-25. Control__9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved
2-0	ADVANCE_LVL	R/W	0x0	Phase Advance Setting 0x0 = 0° 0x1 = 4° 0x2 = 7° 0x3 = 11° 0x4 = 15° 0x5 = 20° 0x6 = 25° 0x7 = 30°

8.6.2.10 Control__10 Register (Address = 0xC) [Reset = 0x0]

Control__10 is shown in Table 8-26.

Return to the Summary Table.

Table 8-26. Control__10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	DLYCMP_EN	R/W	0x0	Driver Delay Compensation enable 0x0 = Disable 0x1 = Enable
3-0	DLY_TARGET	R/W	0x0	Delay Target for Driver Delay Compensation 0x0 = 0 us 0x1 = 0.4 us 0x2 = 0.6 us 0x3 = 0.8 us 0x4 = 1 us 0x5 = 1.2 us 0x6 = 1.4 us 0x7 = 1.6 us 0x8 = 1.8 us 0x9 = 2 us 0xA = 2.2 us 0xB = 2.4 us 0xC = 2.6 us 0xD = 2.8 us 0xE = 3 us 0xF = 3.2 us

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The MCT8316Z can be used to drive Brushless-DC motors. The following design procedure can be used to configure the MCT8316Z.

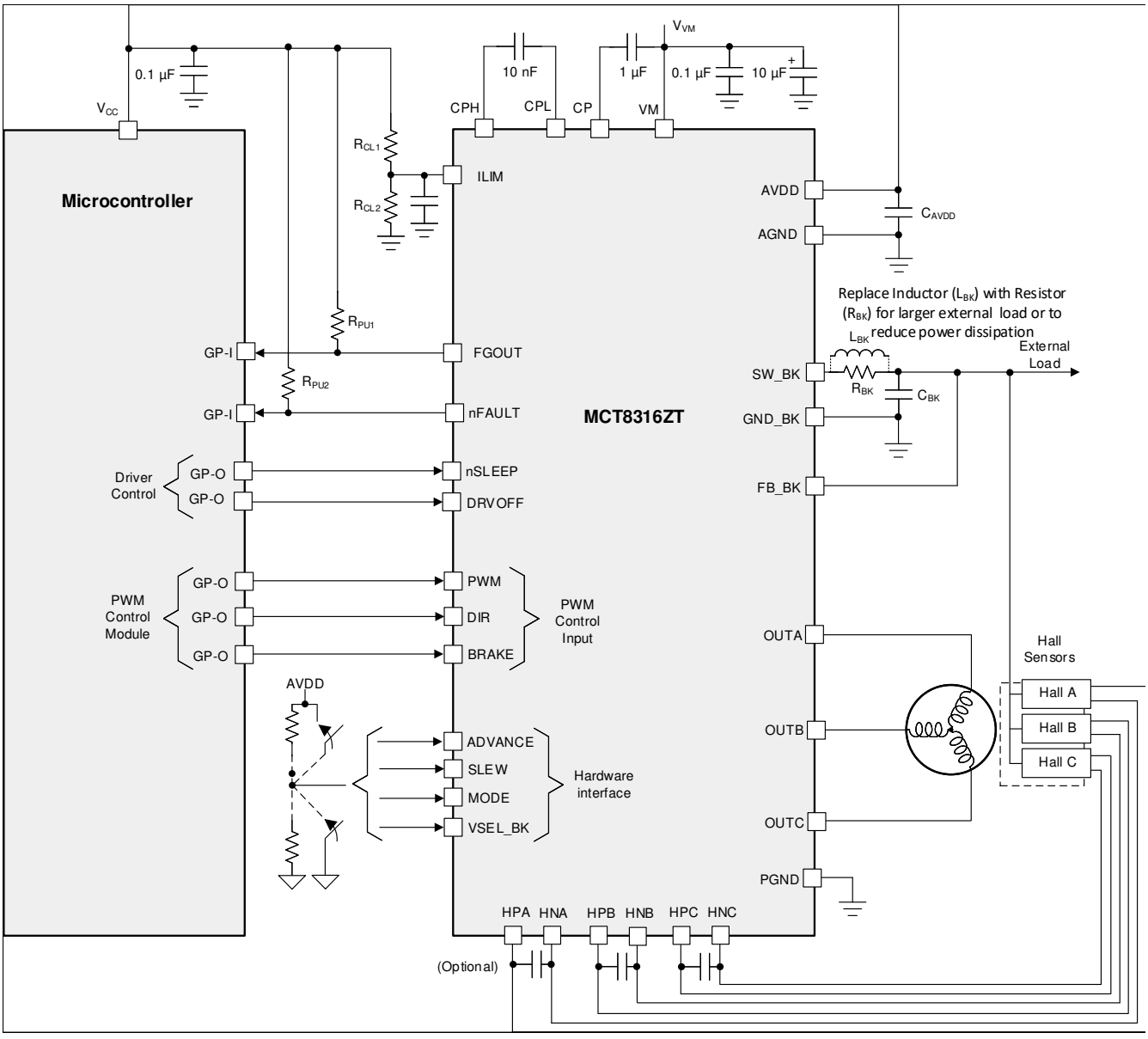


Figure 9-1. Primary Application Schematics

9.2 Hall Sensor Configuration and Connection

The combinations of Hall sensor connections in this section are common connections.

9.2.1 Typical Configuration

The Hall sensor inputs on the DRV10686 device can interface with a variety of Hall sensors. Typically, a Hall element is used, which outputs a differential signal. To use this type of sensor, the AVDD regulator can be used to power the Hall sensor. Figure 9-2 shows the connections.

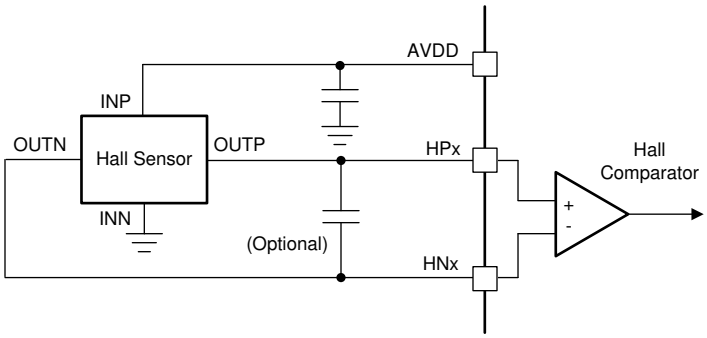


Figure 9-2. Typical Hall Sensor Configuration

Because the amplitude of the Hall-sensor output signal is very low, capacitors are often placed across the Hall inputs to help reject noise coupled from the motor. Capacitors with a value of 1 nF to 100 nF are typically used.

9.2.2 Open Drain Configuration

Some motors use digital Hall sensors with open-drain outputs. These sensors can also be used with the DRV10686 device, with the addition of a few resistors as shown in Figure 9-3.

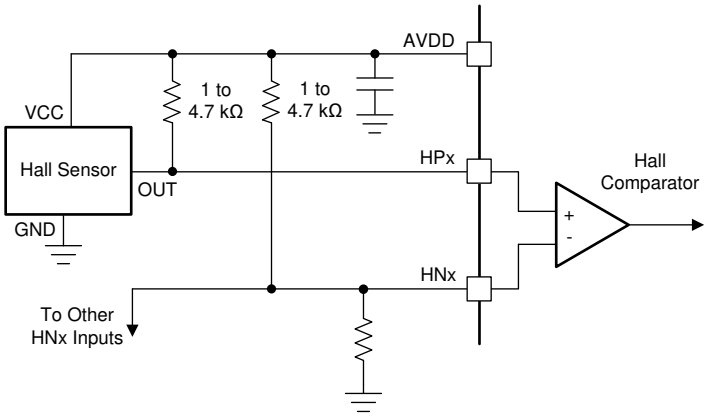


Figure 9-3. Open-Drain Hall Sensor Configuration

The negative (HNx) inputs are biased to AVDD / 2 by a pair of resistors between the AVDD pin and ground. For open-collector Hall sensors, an additional pullup resistor to the VREG pin is required on the positive (HPx) input. Again, the AVDD output can usually be used to supply power to the Hall sensors.

ADVANCE INFORMATION

9.2.3 Series Configuration

Hall elements are also connected in series or parallel depending upon the Hall sensor current/voltage requirement. Figure 9-4 shows the series connection of Hall sensors powered via the DRV10686 internal LDO (AVDD). This configuration is used if the current requirement per Hall sensor is high (>10 mA)

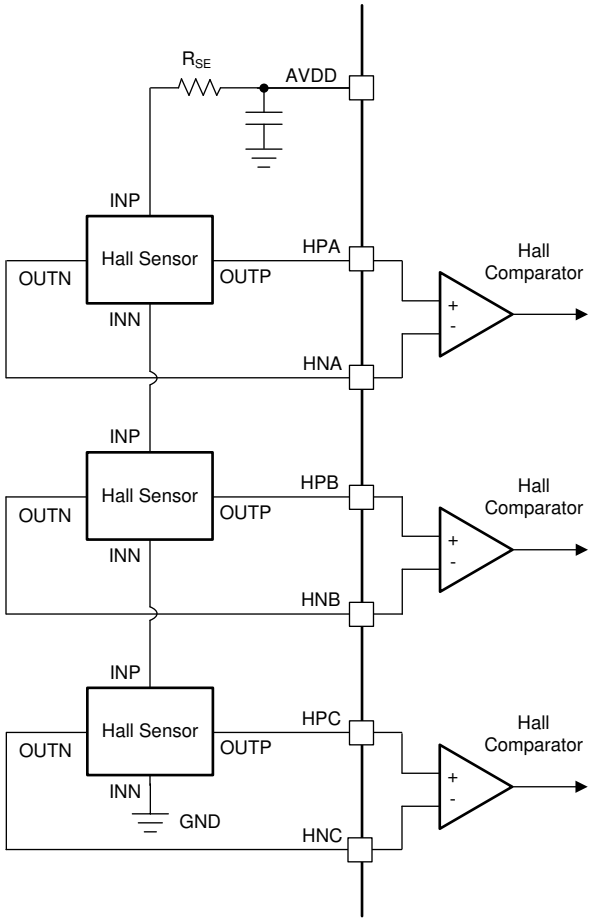


Figure 9-4. Hall Sensor Connected in Series Configuration

9.2.4 Parallel Configuration

Figure 9-5 shows the parallel connection of Hall sensors which is powered by the AVDD. This configuration can be used if the current requirement per Hall sensor is low (<10 mA).

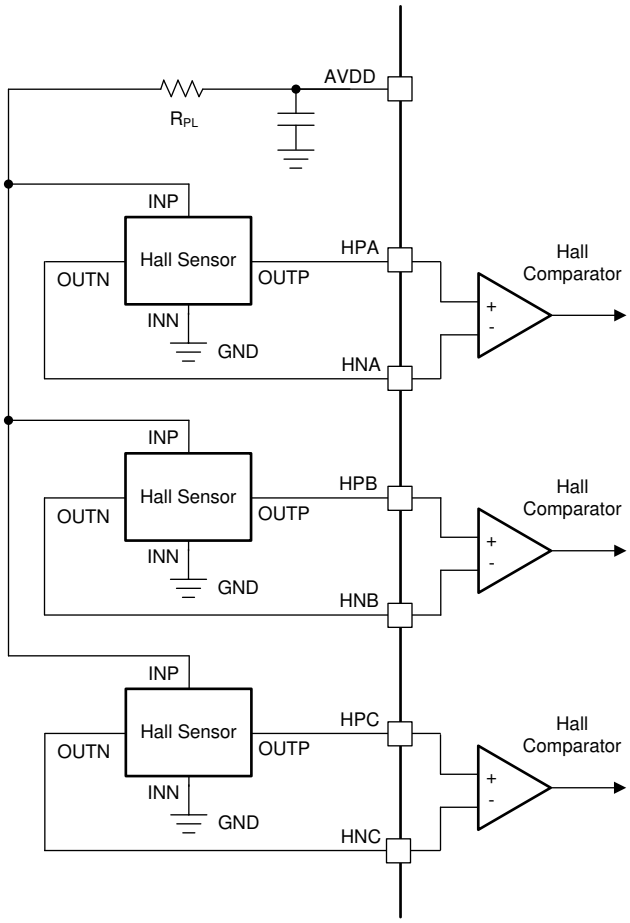


Figure 9-5. Hall Sensors Connected in Parallel Configuration

ADVANCE INFORMATION

9.3 Typical Applications

9.3.1 Three-Phase Brushless-DC Motor Control With Current Limit

In this application, the MCT8316Z is used to drive a brushless-DC motor with current limit.

9.3.1.1 Detailed Design Procedure

Table 9-1 lists the example input parameters for the system design.

Table 9-1. Design Parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{VM}	24 V
Motor peak current	I_{PEAK}	8 A
PWM Frequency	f_{PWM}	50 kHz
Slew Rate Setting	SR	200 V/µs
Buck regulator output voltage	V_{BK}	3.3 V

9.3.1.1.1 Motor Voltage

Brushless-DC motors are typically rated for a certain voltage (for example 12 V and 24 V). Operating a motor at a higher voltage corresponds to a lower drive current to obtain the same motor power. A higher operating voltage also corresponds to a higher obtainable rpm. MCT8316Z device allows for the use of higher operating voltage because of a maximum VM rating of 40 V.

Operating at lower voltages generally allows for more accurate control of phase currents. The MCT8316Z functions down to a supply of 4.5V.

9.3.1.1.2 ILIM Implementation

The ILIM pin on the MCT8316Z device is used to set a cycle-by-cycle current limit proportional to the voltage on the ILIM pin. Applying AVDD/2 on the ILIM pin disables the cycle-by-cycle current limit, and applying (AVDD/2 - 0.4) V on ILIM pin sets the current limit at the maximum threshold of 8A.

To set a peak current limit of 8A, a resistor divider with resistors R_{ILIM1} and R_{ILIM2} is implemented with AVDD as the source VCC voltage to set ILIM equal to 1.25V (AVDD/2 - 0.4).

$$ILIM = AVDD\ (\frac{R_{ILIM2}}{R_{ILIM1} + R_{ILIM2}})$$

To reduce current load on AVDD, R_{ILIM2} is configured to be 10 kΩ.

$$1.25V = 3.3V\ \left(\frac{10k\Omega}{R_{ILIM1} + 10k\Omega}\right)$$

$$R_{ILIM1} = 16.4k\Omega$$

10 Power Supply Recommendations

10.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

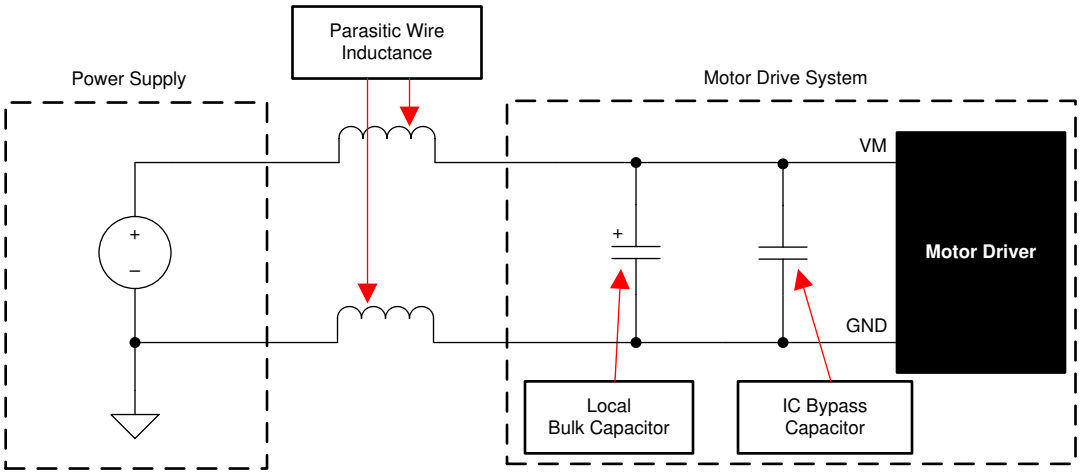


Figure 10-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

11 Layout

11.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors such as the charge pump, AVDD, and VREF capacitors should be ceramic and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Optionally, GND_BK can be split. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

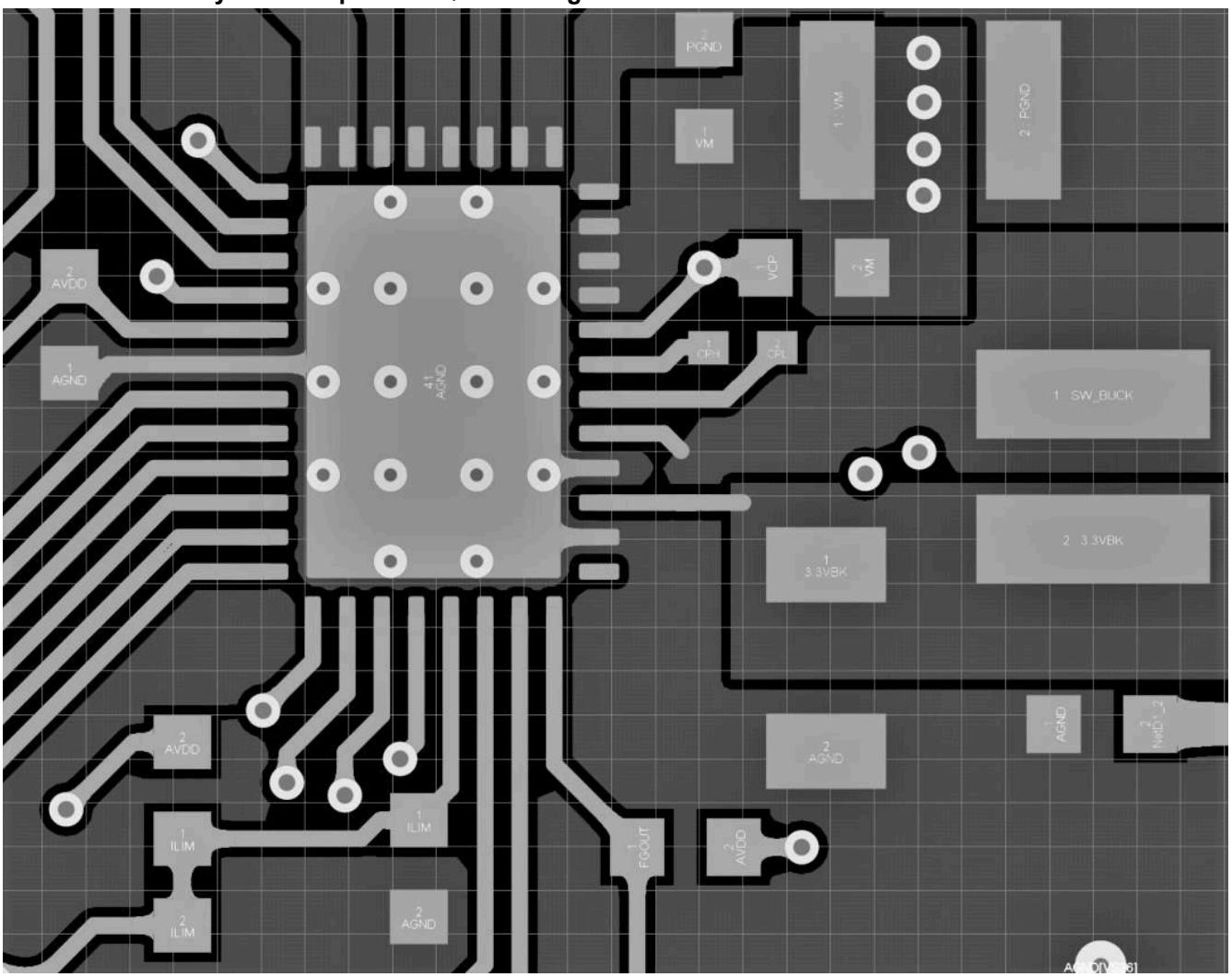
To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve theremal dissipation from the die surface.

Separate the SW_BUCK and FB_BUCK traces with ground separation to reduce buck switching from coupling as noise into the buck outer feedback loop. Widen the FB_BUCK trace as much as possible to allow for faster load switching.

Recommended Layout Example for VQFN Package shows a layout example for the MCT8316Z.

11.2 Layout Example

Recommended Layout Example for VQFN Package



ADVANCE INFORMATION

11.3 Thermal Considerations

The MCT8316Z has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

11.3.1 Power Dissipation

The power dissipated in the output FET resistance, or $R_{DS(on)}$ dominates power dissipation in the MCT8316Z.

At start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration.

The total device dissipation is the power dissipated in each of the three half-H-bridges added together.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

12 Device and Documentation Support

12.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

ADVANCE INFORMATION

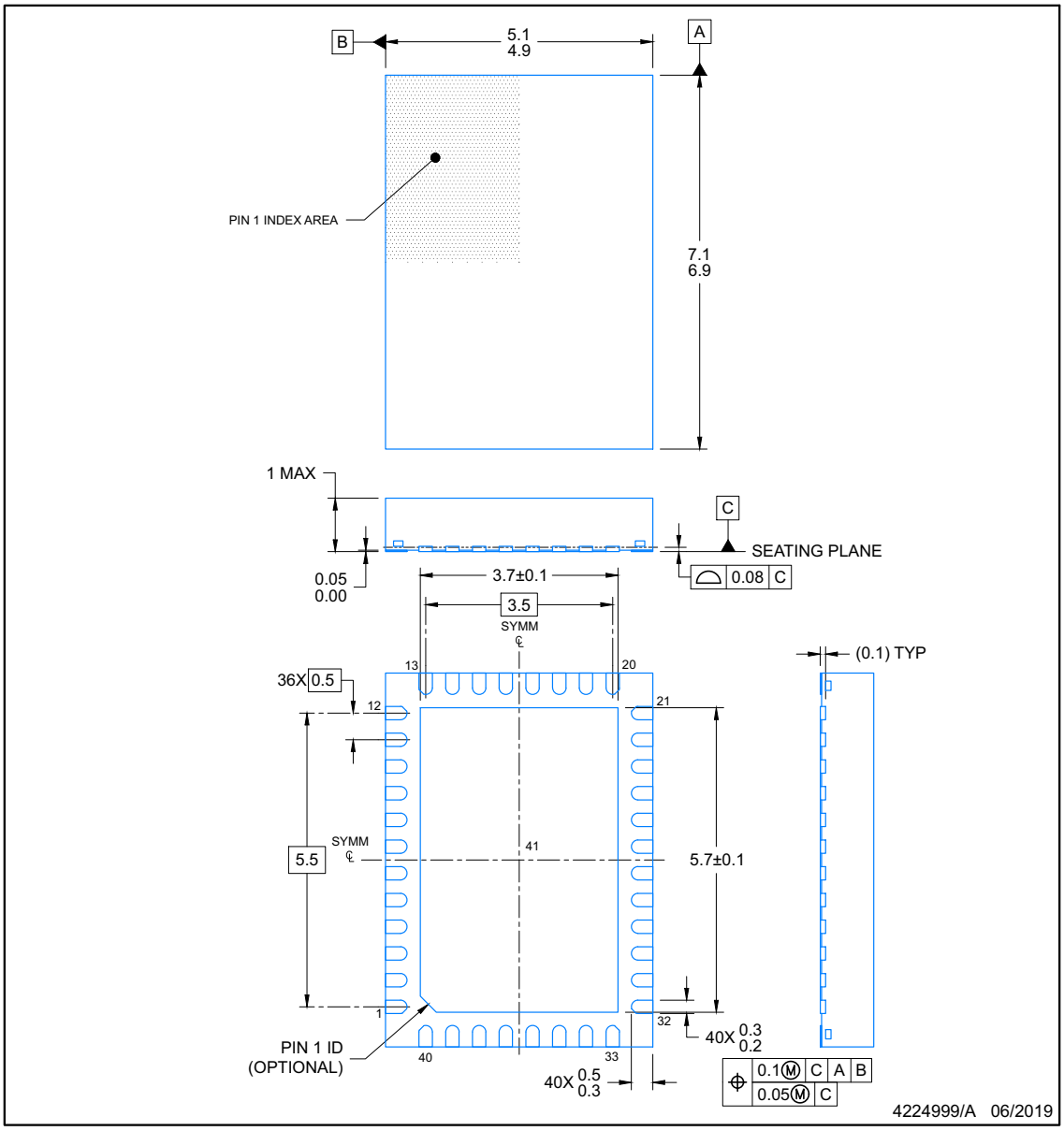
ADVANCE INFORMATION

PACKAGE OUTLINE

RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

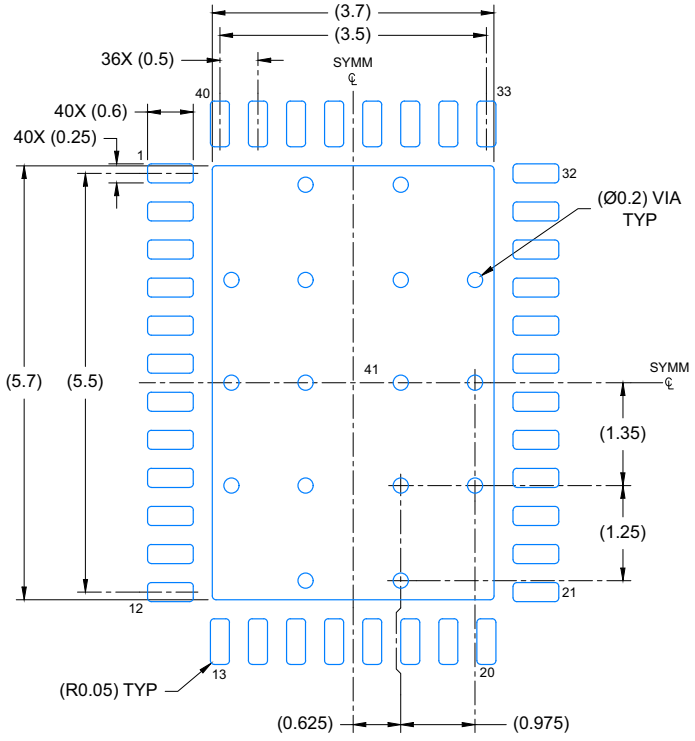
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

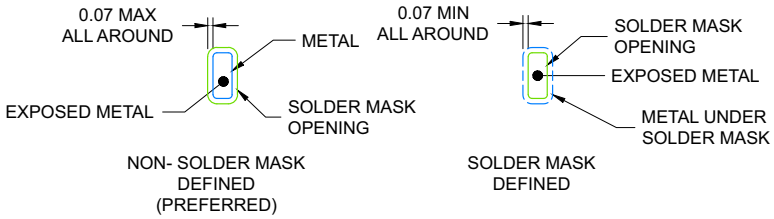
RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

4224999/A 06/2019

NOTES: (continued)

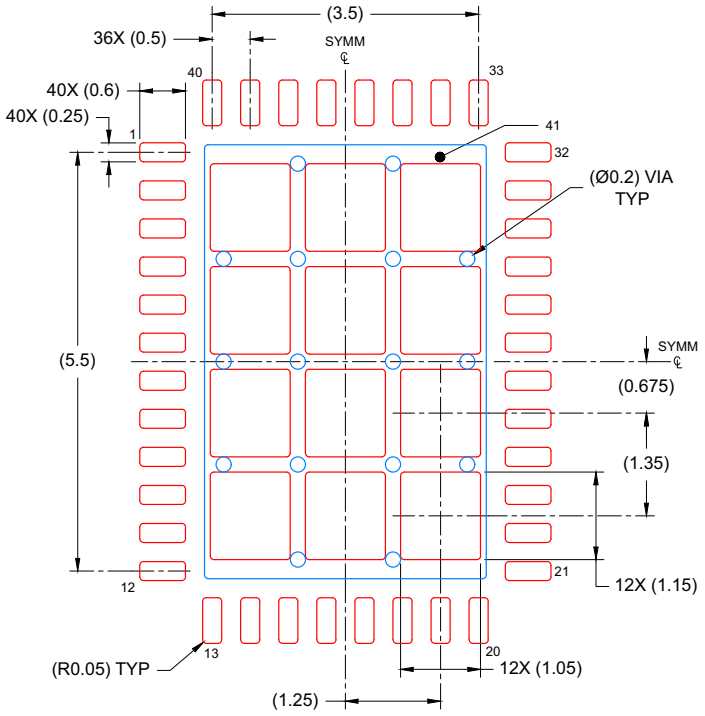
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGF0040E — **VQFN - 1 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

4224999/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PMCT8316Z0TRGFR	ACTIVE	VQFN	RGF	40	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

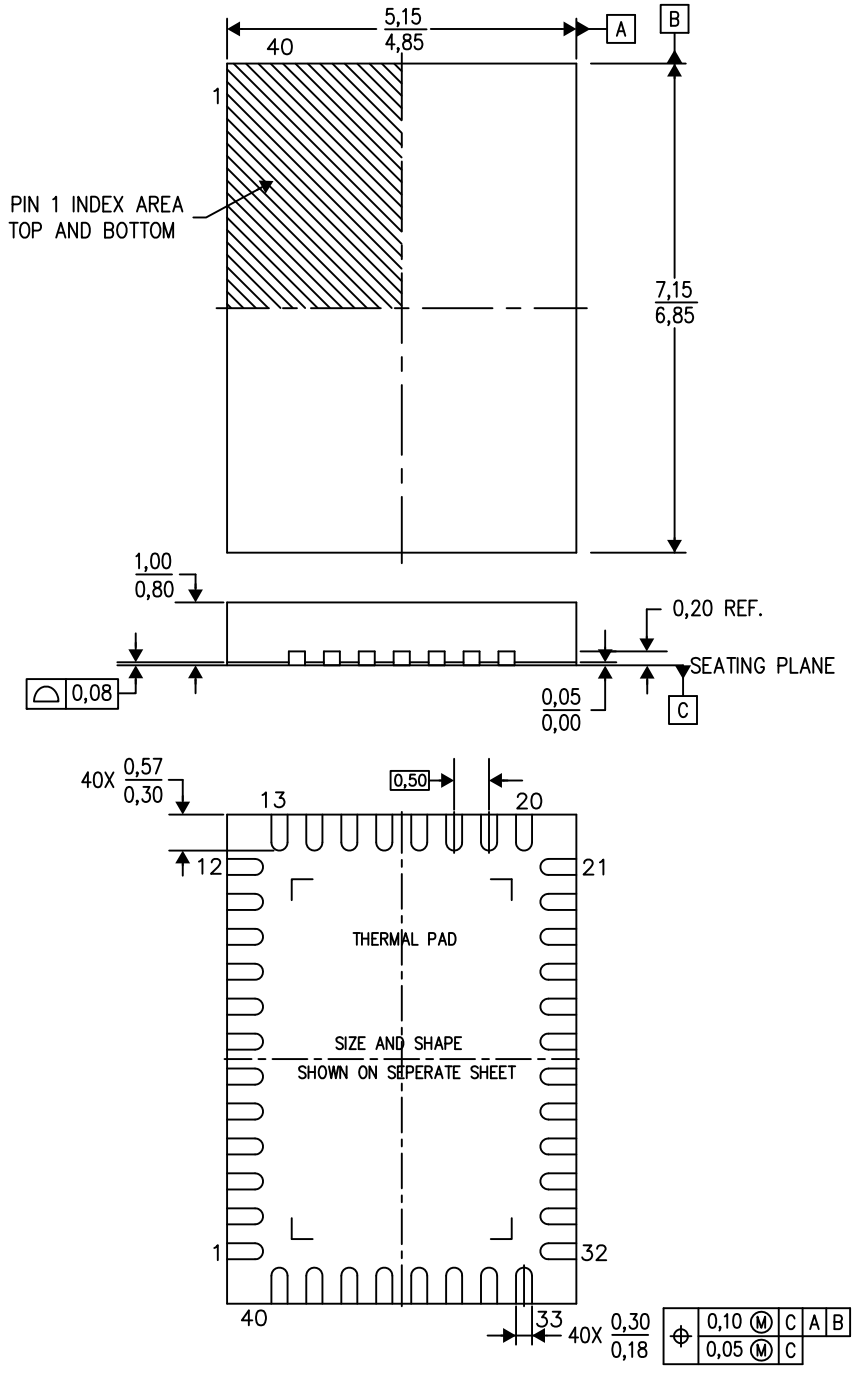
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RGF (R–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding lands and the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265