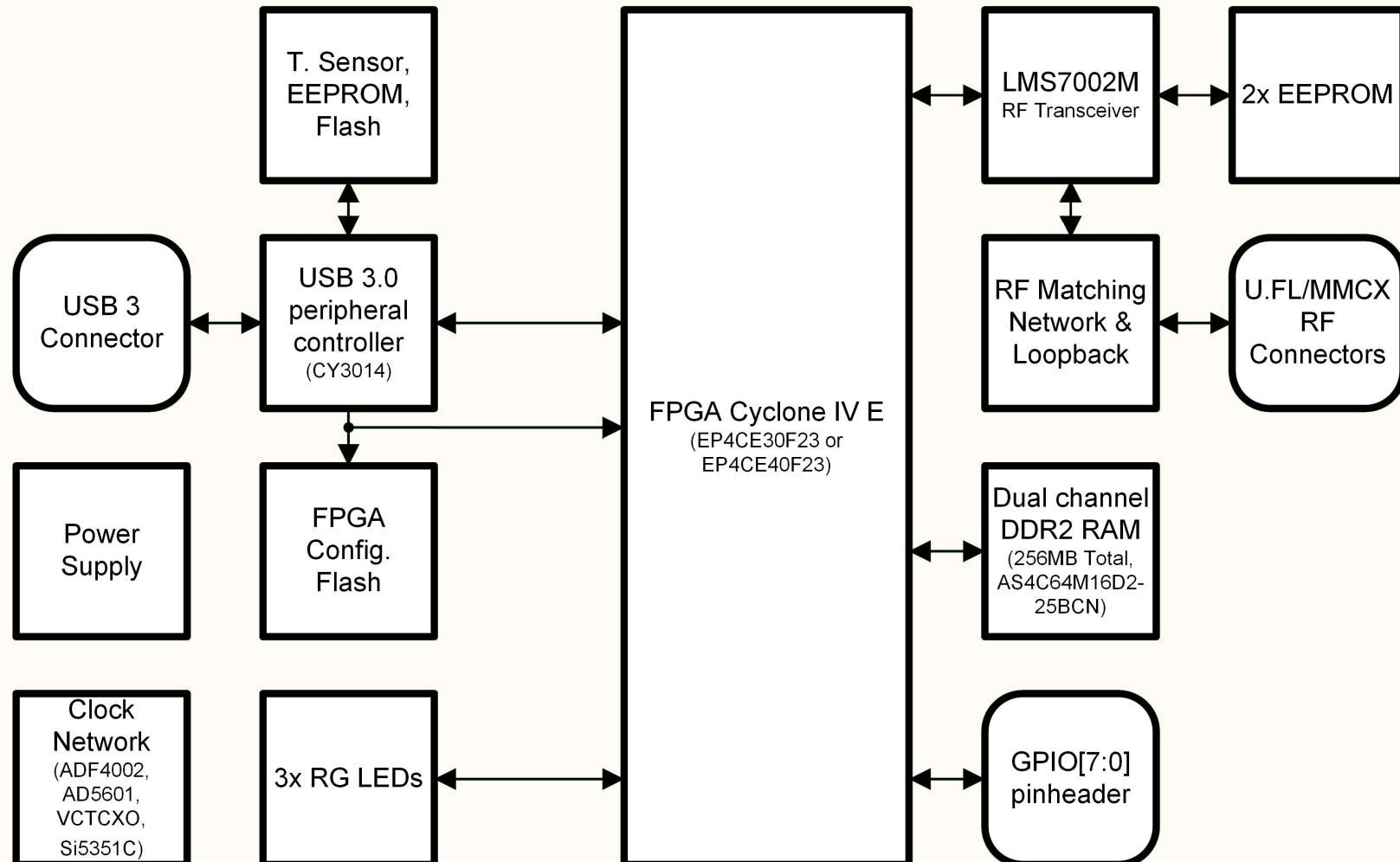


Block diagram



Project name: **LimeSDR-USB_1v4s.PrjPcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.4s**

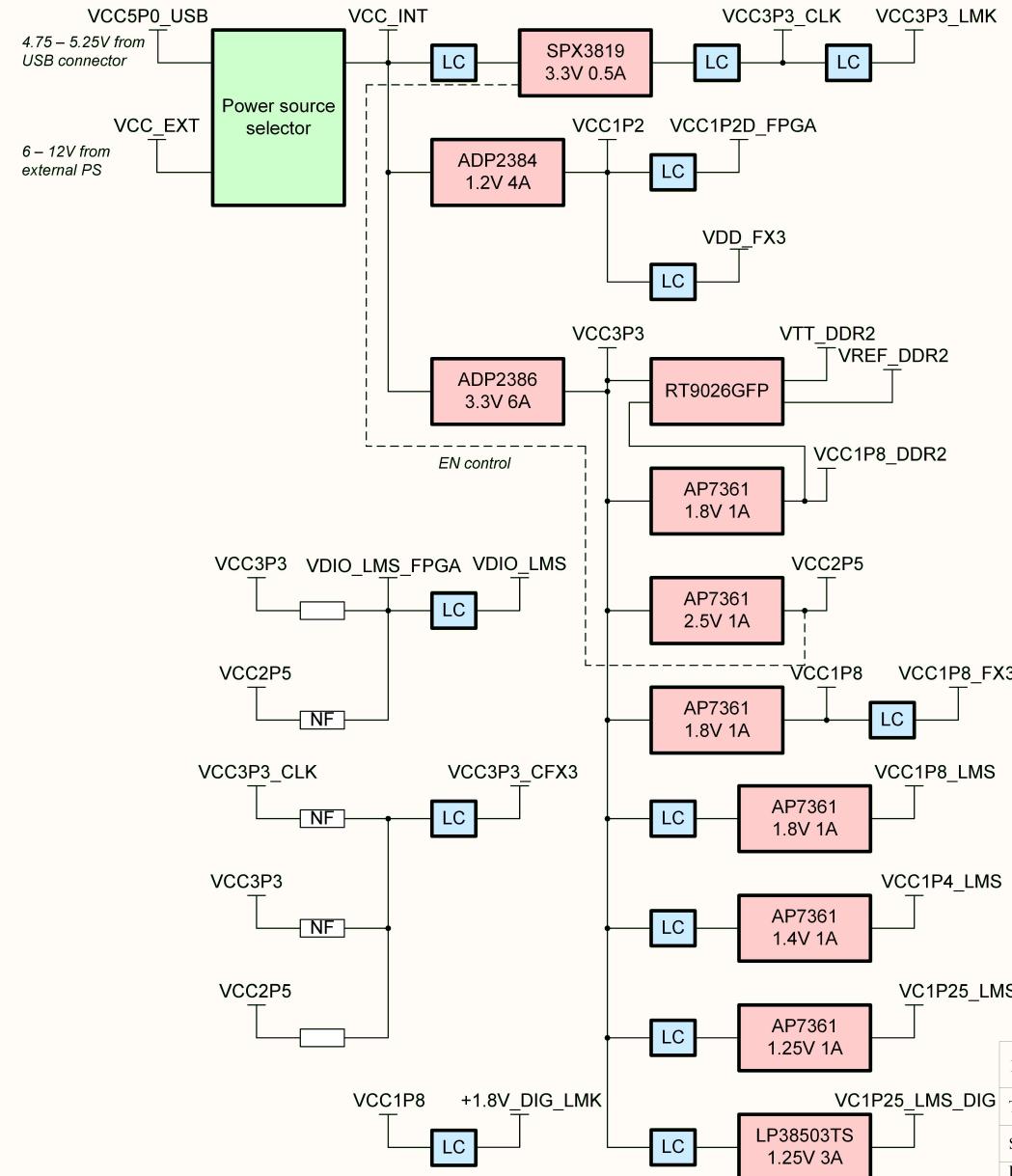
Date: **2016-10-31** Time: **10:06:12** Sheet **1** of **15**

File: **01_BlockDiagram.SchDoc**

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Power diagram



Project name: **LimeSDR-USB_Iv4s.PnjPcb**

Title: **Power diagram**

Size: **A4** Revision: **v1.4s**

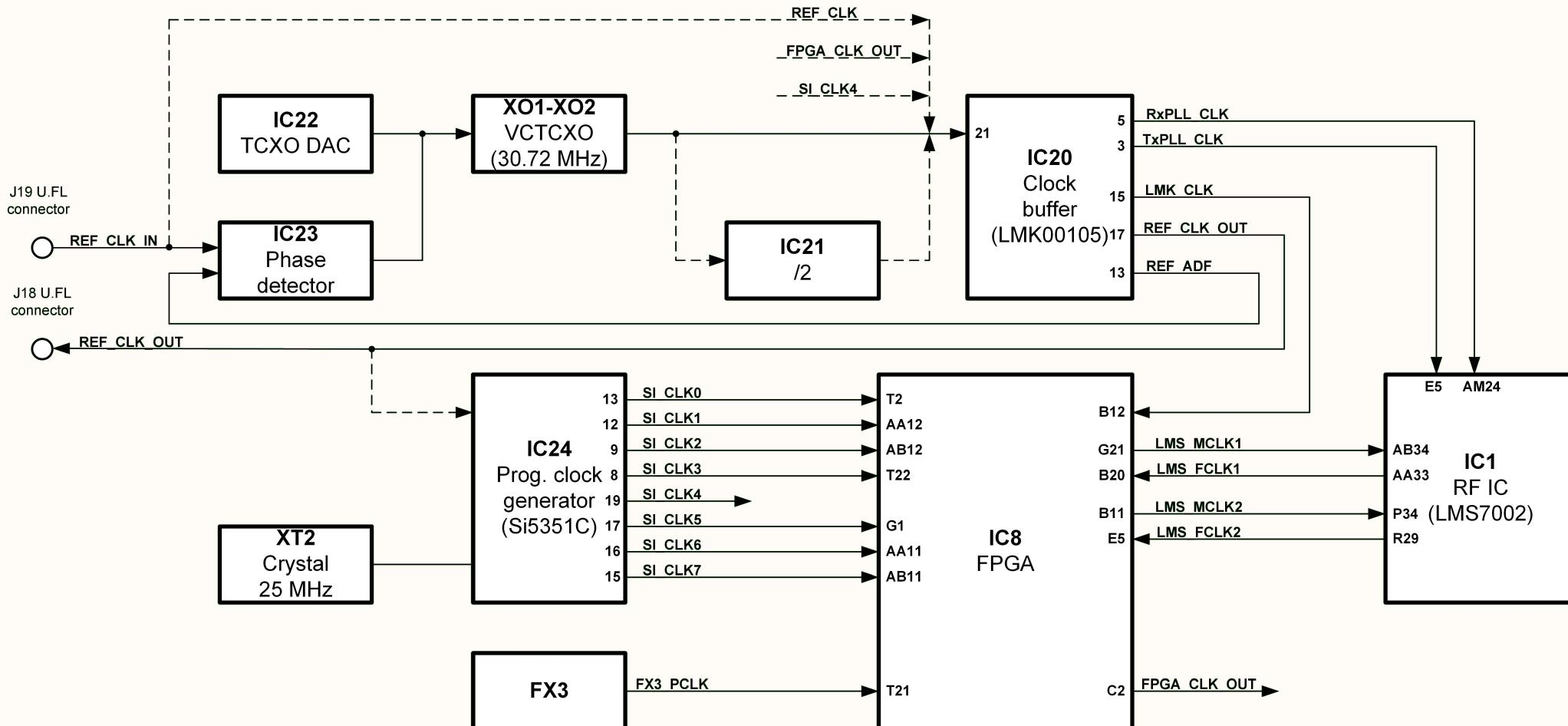
Date: **2016-10-31** Time: **10:06:16** Sheet**2** of **15**

File: **02_PowerDiagram.SchDoc**

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Clock diagram



Project name: *LimeSDR-USB_Iv4s.PnjPcb*

Title: *Clock diagram*

Size: **A4** Revision: **v1.4s**

Date: **2016-10-31** Time: **10:06:25** Sheet**3** of **15**

File: **03_ClockDiagram.SchDoc**

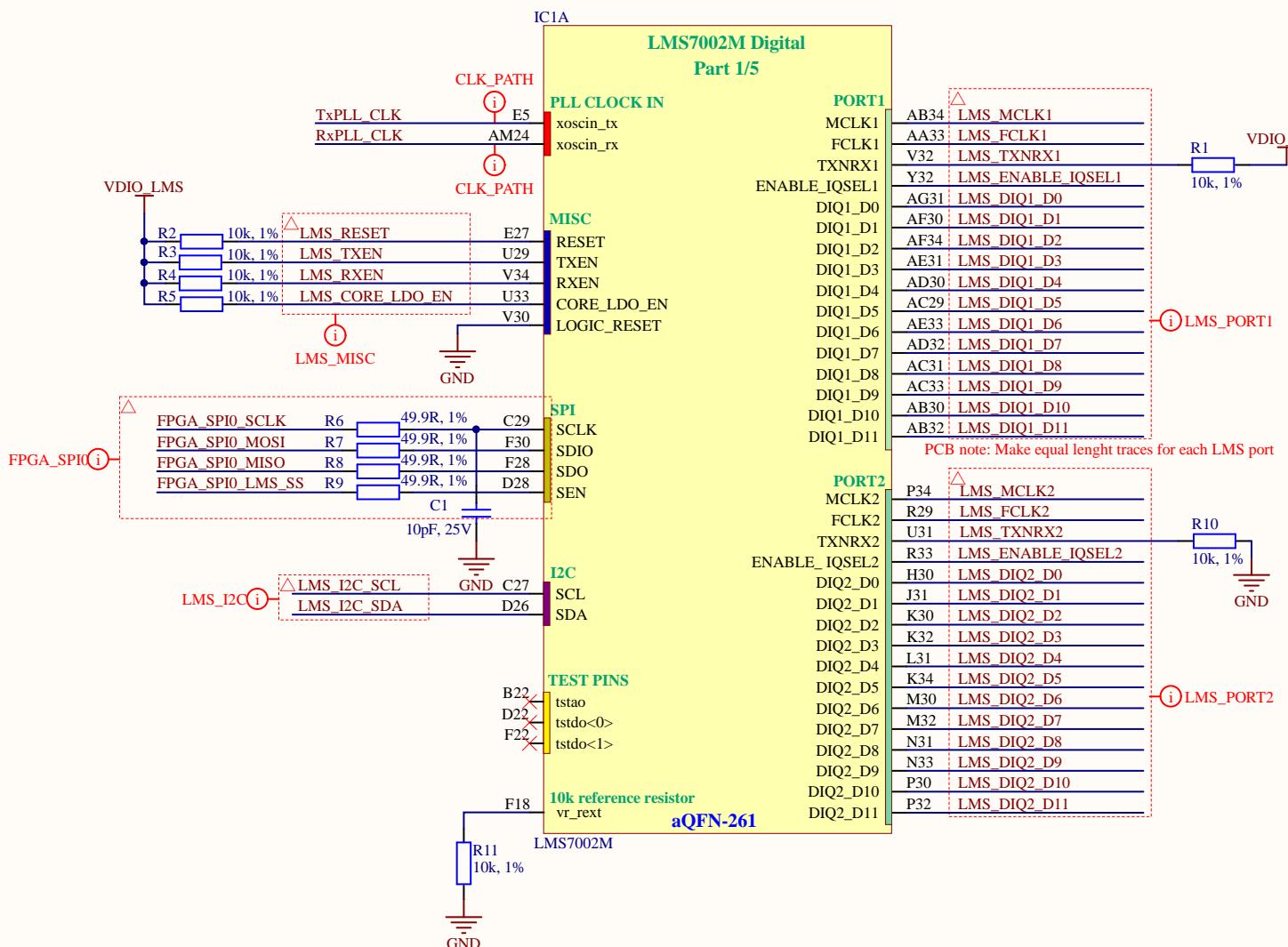
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



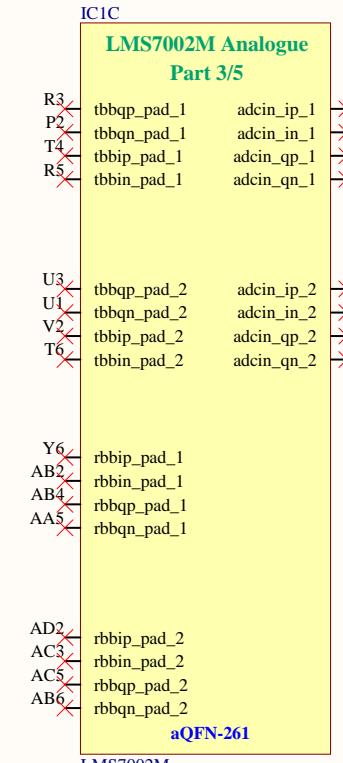
NF elements on sheet: -
Number of NF elements on sheet: 0

LMS7002M misc

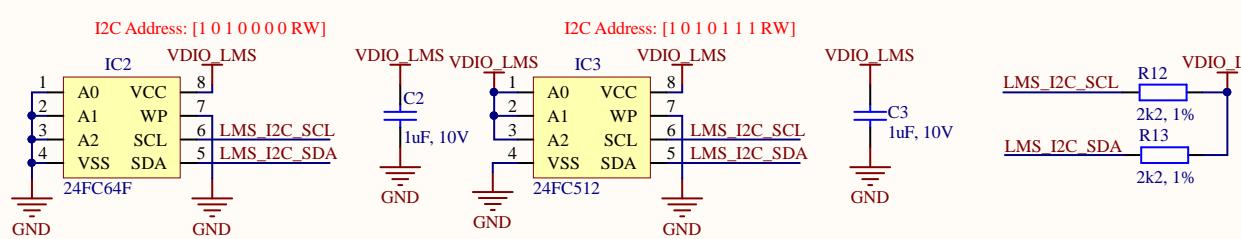
Digital interfaces



Baseband external IO



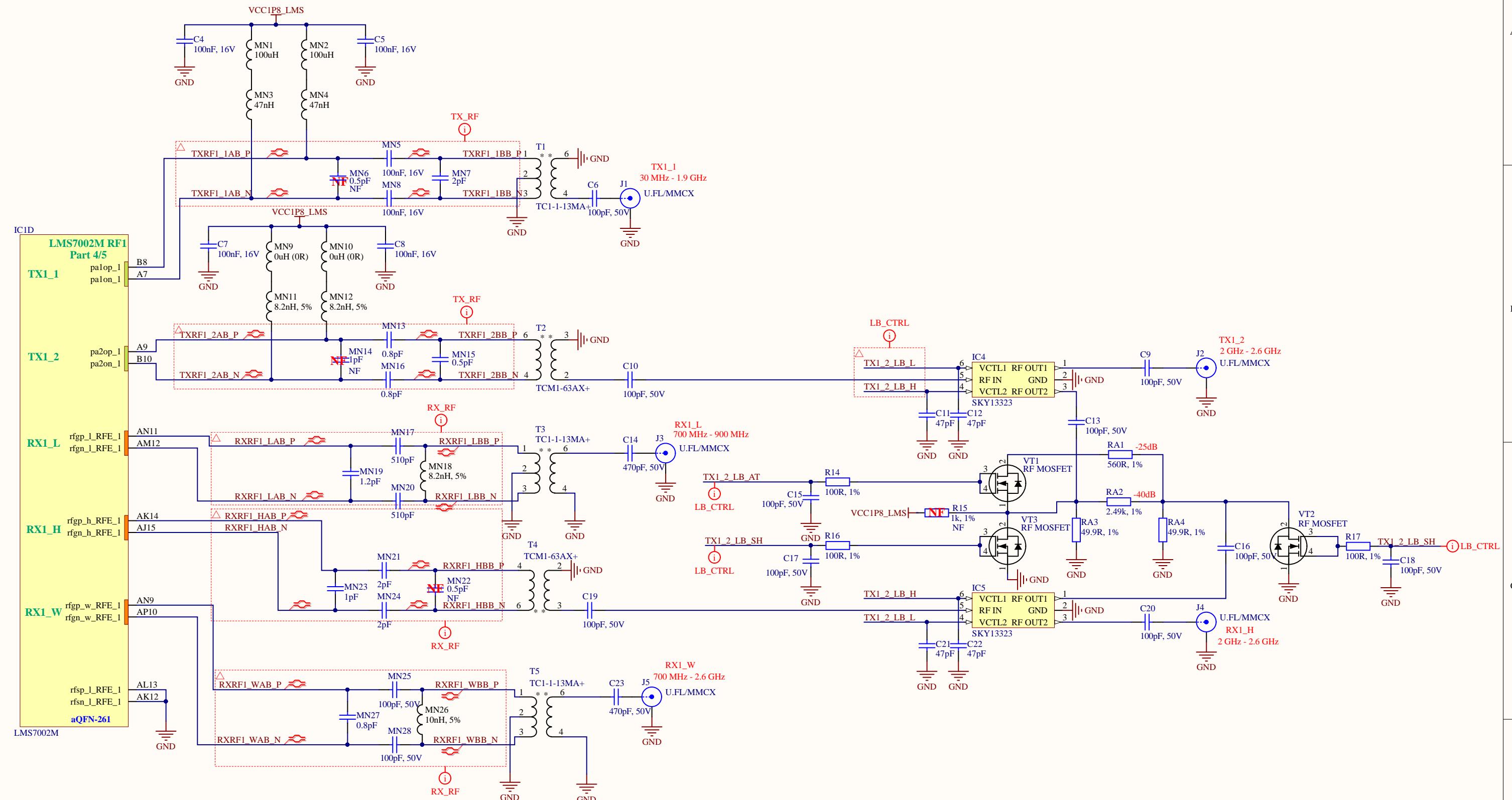
LMS EEPROMS



Project name:	LimeSDR-USB_1v4s.PrjPcb
Title:	LMS7002M misc
Size:	A3
Revision:	v1.4s
Date:	2016-10-31
Time:	10:06:32
Sheet	4 of 15
File:	04_LMS7002M_Misc.SchDoc

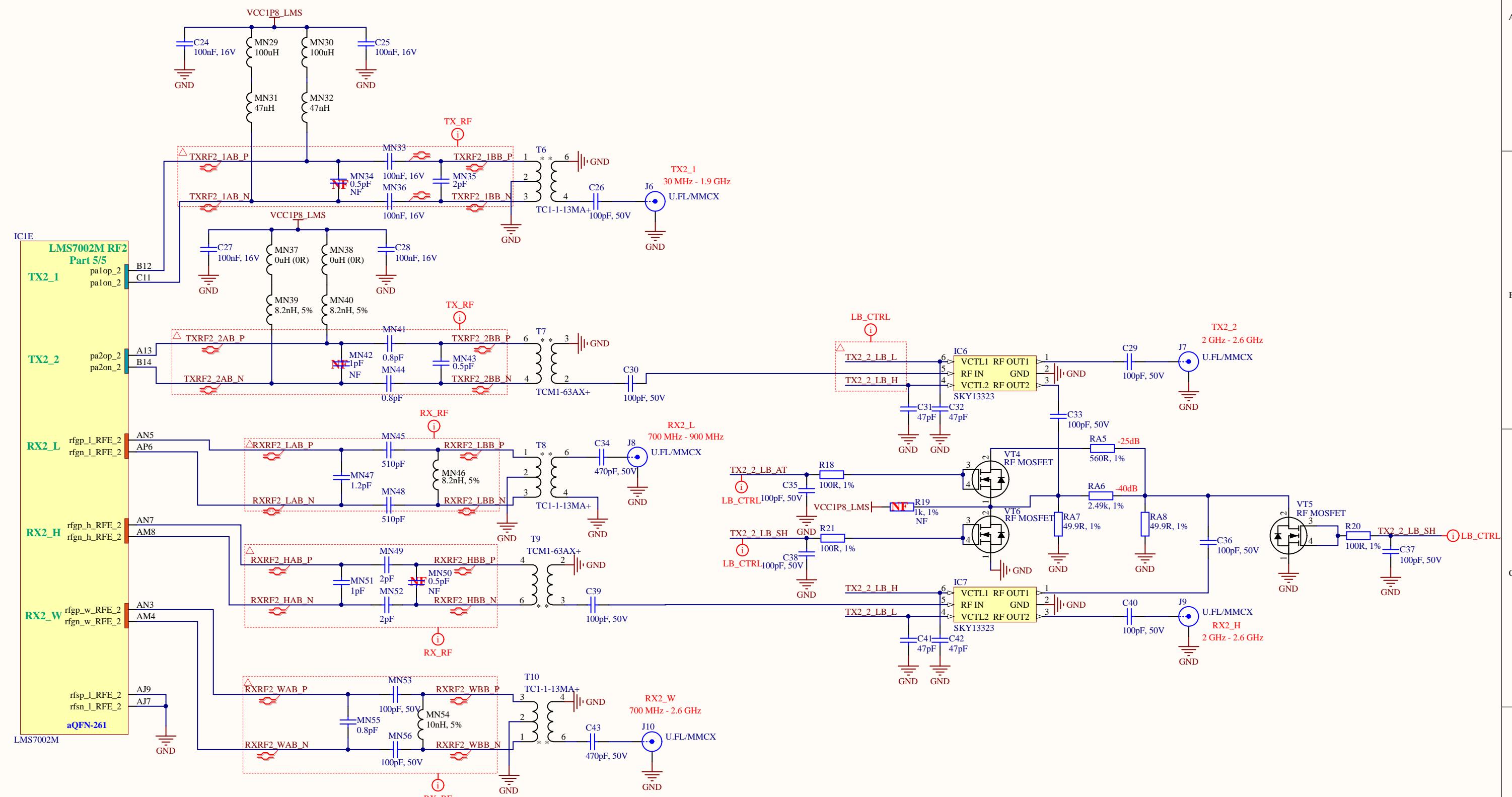
NF elements on sheet: MN6, MN14, MN22, R15
 Number of NF elements on sheet: 4

LMS7002M RF1 circuits



NF elements on sheet: MN34, MN42, MN50, R19
Number of NF elements on sheet: 4

LMS7002M RF2 circuits



Project name: **LimeSDR-USB_1v4s_PriPch**

Title: LMS7002M RF

Sigma A3 Position: v1.45

Date: 2016-10-31 Time: 10:06:37 Sheet 6 of 15

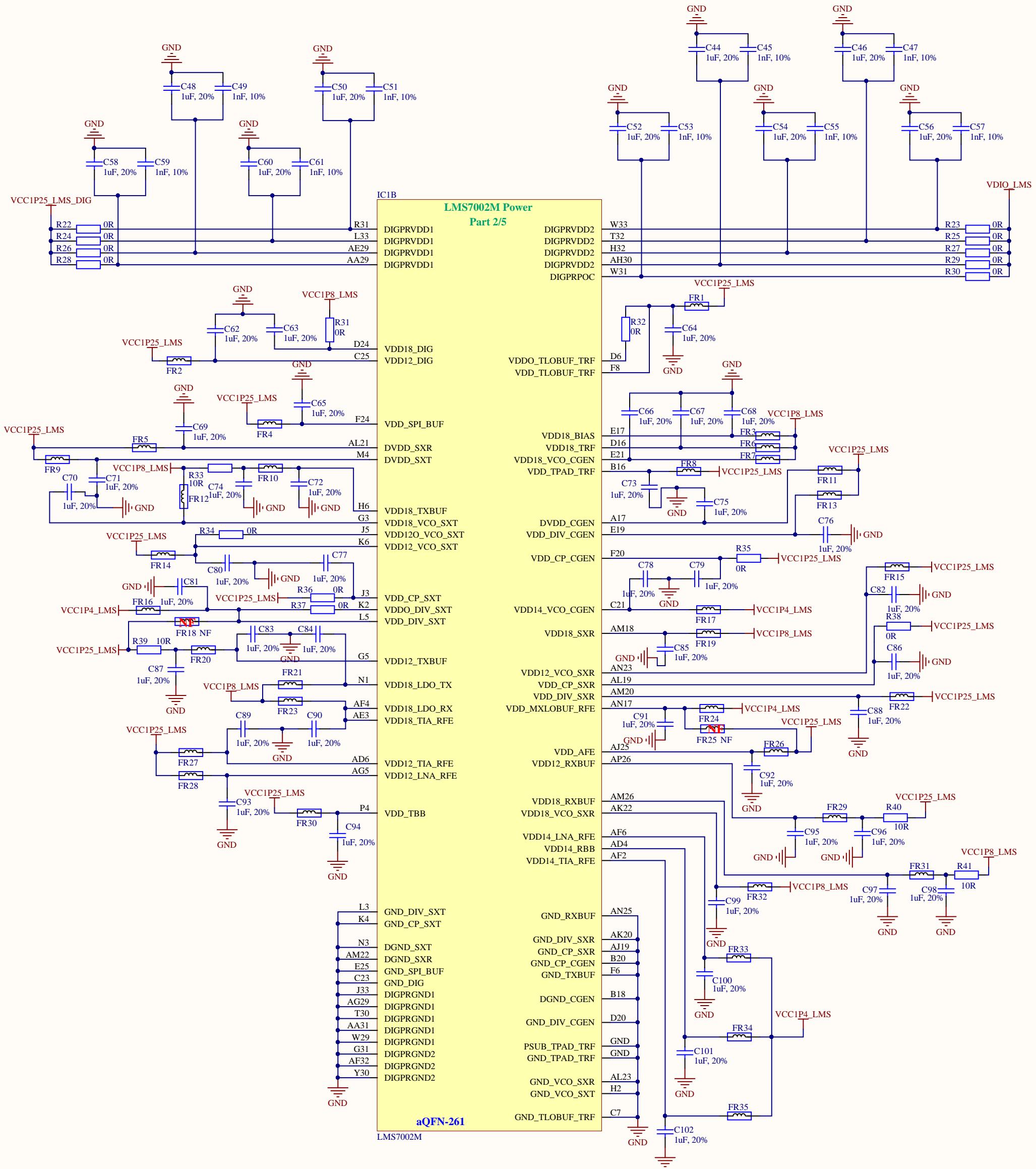
File: 06_LMS7002M_RF2.SchDoc

*Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom*



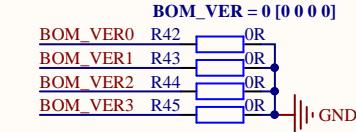
NF elements on sheet: FR18, FR25
Number of NF elements on sheet: 2

LMS7002M power supply circuit



FPGA banks 1, 2, 3, 4

NF elements on sheet: -
Number of NF elements on sheet: 0



A

IC8A
BANK 1
VCC3P3

IO, DIFFIO_L1p	G4	FPGA_GPIO4
IO, DIFFIO_L1n	G3	FPGA_GPIO5
IO, DIFFIO_L2p, (DQ2L)/(DQ1L)/(DQ1L)	S2	BRDG_SPI_SCLK
IO, DIFFIO_L2n, (DQ2L)/(DQ1L)/(DQ1L)	B1	BRDG_SPI_MOSI
IO, VREFB1N0	65	FX3_LED_G
IO, DIFFIO_L4p, (nRESET), (DQ2L)/(DQ1L)/(DQ1L)	E4	FAN_CTRL
IO, DIFFIO_L4n, (DQ2L)/(DQ1L)/(DQ1L)	E3	FPGA_LED1_R
IO, DIFFIO_L7p, (DQS2L/CQ3L,CDPCLK0)/(DQS2L/CQ3L,CDPCLK0)	C2	FPGA_CLK_OUT
IO, DIFFIO_L7n, (DQ2L)/(DQ1L)/(DQ1L)	C1	BRDG_SPI_MISO
IO, DIFFIO_L8p, (DQ2L)/(DQ1L)/(DQ1L)	D2	FPGA_LED1_G
IO, DIFFIO_L8n, (DATA1,ASDO)	D1	FPGA_AS_ASDO
IO, VREFB1N1	J7	FPGA_I2C_SCL
IO, DIFFIO_L9p, (DQ2L)/(DQ1L)/(DQ1L)	H6	FPGA_GPIO1
IO, DIFFIO_L9n, (DQ2L)/(DQ1L)/(DQ1L)	J6	LM75_OS
IO, DIFFIO_L10p, (FLASH_nCE,nCSO)	E2	FPGA_AS_NCSO
IO, DIFFIO_L10n, (.)/(DQ1L)/(DQ1L)	E1	FPGA_LED2_R
IO, DIFFIO_L12p, (DM2L)/(DM1L/BWS#1L)/(DM1L/BWS#1L)	F2	FPGA_GPIO6
IO, DIFFIO_L12n, (DQ0L)/(DQ1L)/(DQ1L)	F1	FPGA_GPIO7
IO, DIFFIO_L14p	H8	FPGA_GPIO0
IO, DIFFIO_L18n	8	FPGA_UART_TX
IO, VREFB1N2	5	FPGA_SPI1_ADF_SS
IO, DIFFIO_L20p	H5	FX3_LED_R
IO, DIFFIO_L20n	8	FPGA_SPI1_MOSI
IO, DIFFIO_L21p	K8	FPGA_SPI1_SCLK
IO, DIFFIO_L21n	J7	FPGA_I2C_SDA
IO, (DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)	K7	BRDG_SPI_FPGA_SS
IO, DIFFIO_L23p, (DQ0L)/(DQ1L)	J4	FPGA_LED2_G
IO, DIFFIO_L23n, (DQ0L)/(DQ1L)	H2	FPGA_GPIO2
IO, VREFB1N3	H1	FPGA_GPIO3
IO, DIFFIO_L24p, (DQ0L)/(DQ1L)/(DQ1L)	J3	FPGA_SPI1_DAC_SS
IO, DIFFIO_L24n, (DQ0L)/(DQ1L)/(DQ1L)	J2	ADP_MUXOUT
IO, DATA0	I1	FPGA_UART_RX

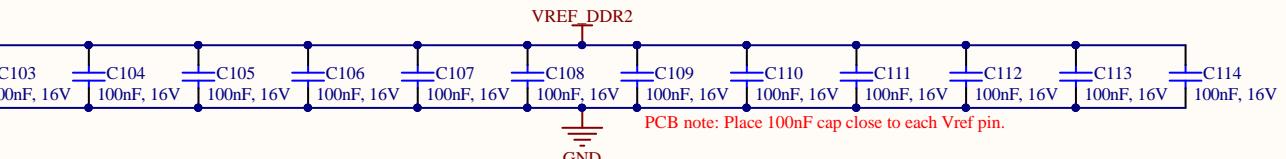
EP4CE40F23C8N

B

IC8C
BANK 3
VCC1P8

IO, DIFFIO_B1p	V6	DDR2_1_A3
IO, DIFFIO_B1n, (DM3B/BWS#3B)/(DM3B/BWS#3B)/(DM5B/BWS#5B)	V5	DDR2_1_DM1
IO, DIFFIO_B3p	U7	DDR2_1_CLK_P
IO, VREFB3N3	U8	DDR2_1_CLK_N
Y4	VREF DDR2	
IO, DIFFIO_B4p, (DQ3B)/(DQ3B)/(DQ5B)	Y3	DDR2_1_A2
IO, DIFFIO_B6p, (DQS1B/CQ1B#,CDPCLK2)/(DQS1B/CQ1B#,CDPCLK2)/(DQS1B/CQ1B#,CDPCLK2)	Y6	DDR2_1_A10
IO, PLL1_CLKOUTp	AA3	DDR2_1_A1
IO, PLL1_CLKOUTn	AB3	DDR2_1_A5
IO, DIFFIO_B7p, (DQ3B)/(DQ3B)/(DQ5B)	W6	DDR2_1_DQ8
IO, DIFFIO_B7n	Y7	DDR2_1_A9
IO, (DQ3B)/(DQ3B)/(DQ5B)	AA4	DDR2_1_DQ15
IO, VREFB3N2	AB4	VREF DDR2
IO, DIFFIO_B8p, (DQ3B)/(DQ3B)/(DQ5B)	AA5	DDR2_1_DQ9
IO, DIFFIO_B8n	AB5	DDR2_1_A7
IO, DIFFIO_B11p	T8	DDR2_1_A12
IO, DIFFIO_B11n	T9	DDR2_2_WEn
IO, DIFFIO_B12p, (DQ3B)/(DQ3B)/(DQ5B)	W7	DDR2_1_DQ10
IO, DIFFIO_B12n, (DQ3B)/(DQ3B)/(DQ5B)	Y7	DDR2_1_DQ13
IO, DIFFIO_B13p, (DQ3B)/(DQ3B)/(DQ5B)	J9	DDR2_1_DQ14
IO, DIFFIO_B13n, (DQ3B)/(DQ3B)/(DQ5B)	V8	DDR2_1_DQ11
IO, (DQ3B)/(DQ3B)/(DQ5B)	W8	DDR2_1_DQ12
IO, DIFFIO_B14p, (DM5B/BWS#5B)/(DM3B/BWS#3B)/(DM5B/BWS#5B)	AA7	DDR2_1_DM0
IO, DIFFIO_B14n, (DQ5B)/(DQ3B)/(DQ5B)	AB7	DDR2_1_DQ2
IO, (DQ5B)/(DQ3B)/(DQ5B)	Y8	DDR2_2_CSn
IO, DIFFIO_B15p	T10	DDR2_2_CASn
IO, DIFFIO_B15n	T11	DDR2_2_RASn
IO, VREFB3N1	V9	VREF DDR2
IO, DIFFIO_B16p, (DQS3B/CQ3B#,DPCLK2)/(DQS3B/CQ3B#,DPCLK2)/(DQS3B/CQ3B#,DPCLK2)	V10	DDR2_1_DQS1
IO, DIFFIO_B17n, (DQ5B)/(DQ3B)/(DQ5B)	U10	DDR2_1_DQ0
IO, DIFFIO_B18p, (DQ5B)/(DQ3B)/(DQ5B)	AA8	DDR2_1_DQ6
IO, DIFFIO_B18n, (DQ5B)/(DQ3B)/(DQ5B)	AB8	DDR2_1_DQ1
IO, DIFFIO_B21p, (DQ5B)/(DQ3B)/(DQ5B)	AA9	DDR2_1_DQ3
IO, DIFFIO_B21n, (DQS5B/CQ5B#,DPCLK3)/(DQS5B/CQ5B#,DPCLK3)/(DQS5B/CQ5B#,DPCLK3)	AB9	DDR2_1_DQS0
IO, VREFB3N0	U11	VREF DDR2
IO, DIFFIO_B25n, (DQ5B)/(DQ3B)/(DQ5B)	V11	DDR2_1_DQ4
IO, DIFFIO_B26p, (DQ5B)/(DQ3B)/(DQ5B)	W10	DDR2_1_DQ5
IO, DIFFIO_B26n, (DQ5B)/(DQ3B)/(DQ5B)	Y10	DDR2_1_DQ7
IO, DIFFIO_B27p, (DM4B)/(DM5B/BWS#5B)/(DM5B/BWS#5B)	AA10	DDR2_2_DM1
IO, DIFFIO_B27n, (.)/(DQ5B)/(DQ5B)	AB10	DDR2_2_CKE

EP4CE40F23C8N

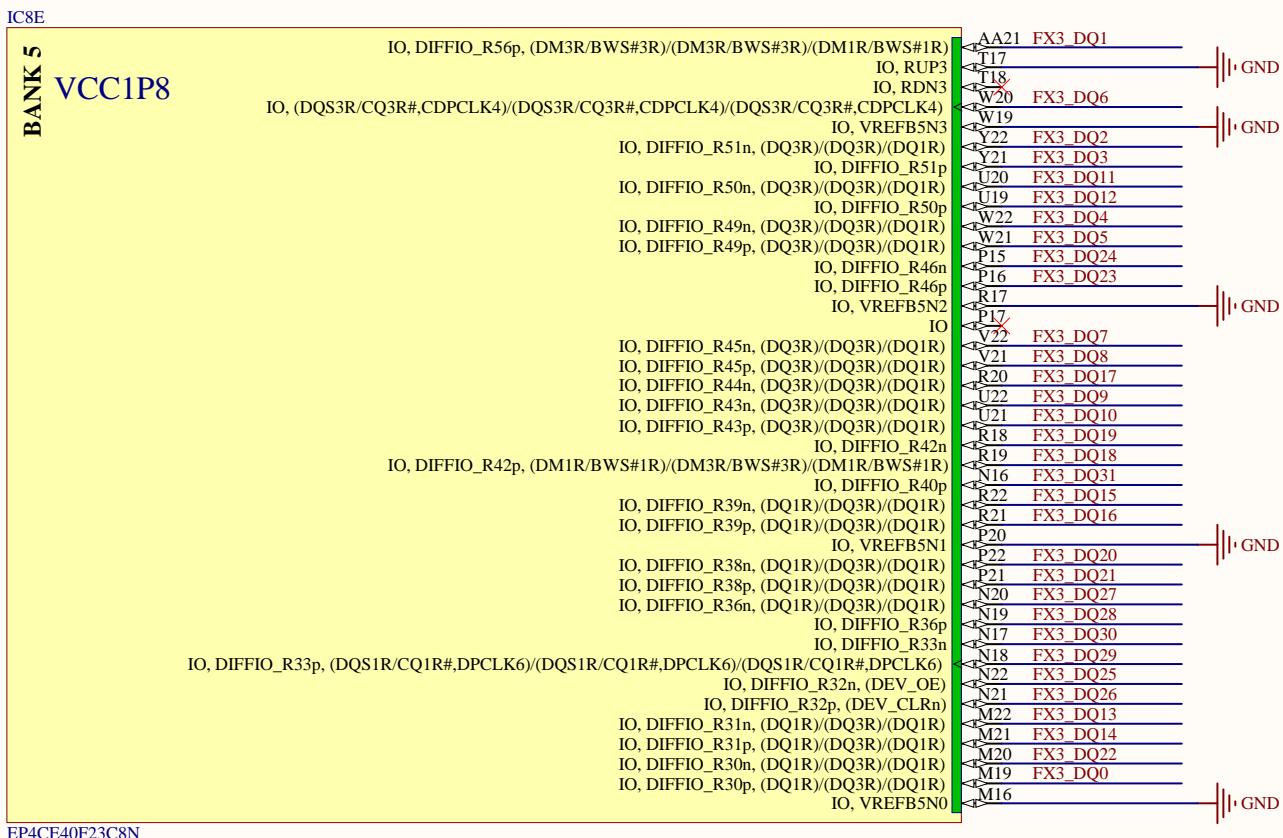


IC8B
BANK 2
VCC1P8

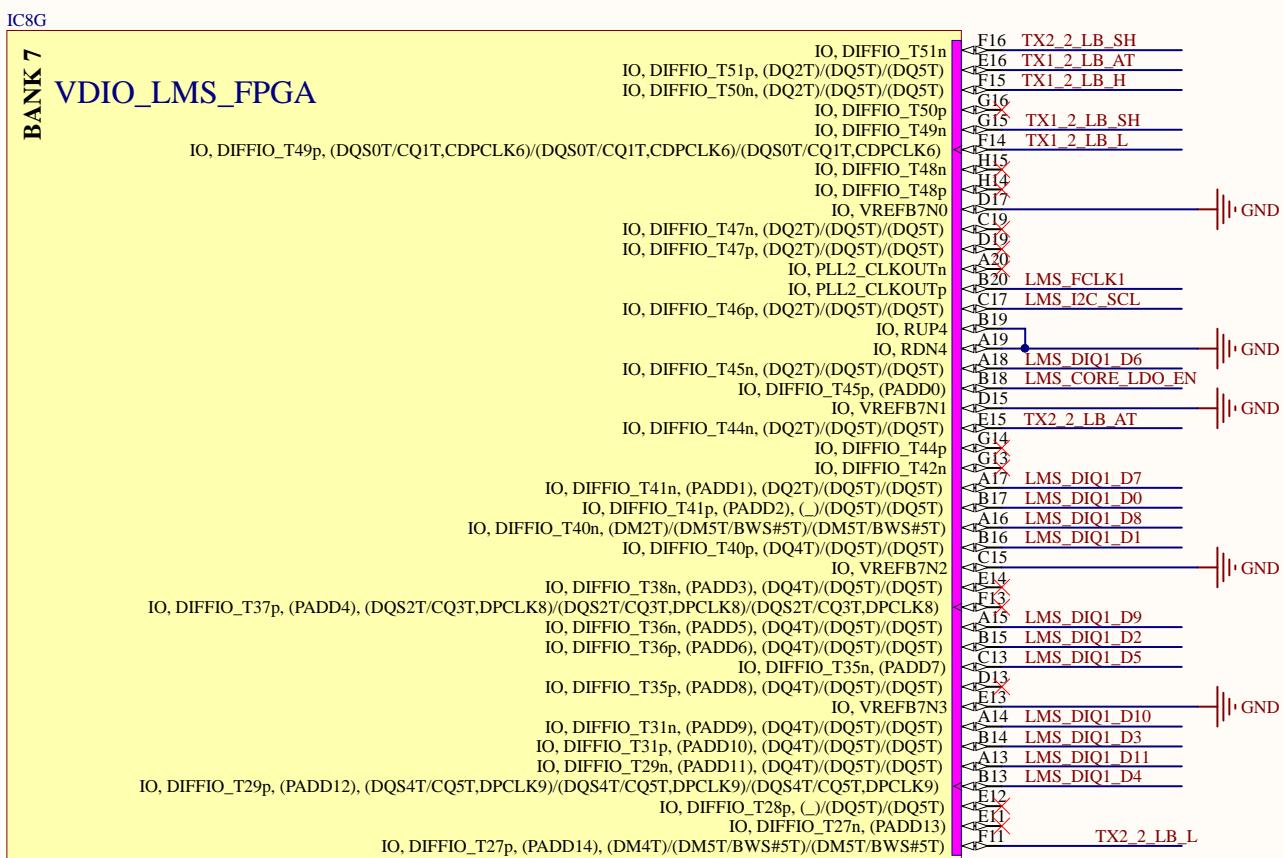
IO, DIFFIO_L26p, (DQ0L)/(DQ1L)/(DQ1L)	L6	FX3_CTL0
IO, DIFFIO_L26n, (DQ0L)/(DQ1L)/(DQ1L)	M6	FX3_CTL6
IO, DIFFIO_L27p, (DQ0L)/(DQ1L)/(DQ1L)	M2	FX3_CTL3
IO, DIFFIO_L27n, (.)/(DQ1L)/(DQ1L)	M1	FX3_CTL2
IO, DIFFIO_L28p, (DM0L)/(DM1L/BWS#1L)/(DM1L/BWS#1L)	M4	FX3_CTL5
IO, DIFFIO_L28n, (DQ1L)/(DQ3L)/(DQ1L)	M3	FX3_CTL4
IO, DIFFIO_L29n, (DQ1L)/(DQ3L)/(DQ1L)	N2	FX3_CTL10
IO, DIFFIO_L30n, (DQ1L)/(DQ3L)/(DQ1L)	N7	FX3_CTL1
IO, VREFB2N0	M5	VREF DDR2
IO, DIFFIO_L32p, (DQ1L)/(DQ3L)/(DQ1L)	P2	FX3_DCTL9
IO, DIFFIO_L32n, (DQ1L)/(DQ3L)/(DQ1L)	P1	BOM_VER0
IO, DIFFIO_L33p, (DQ1L)/(DQ3L)/(DQ1L)	R2	BOM_VER1
IO, DIFFIO_L33n, (DQ1L)/(DQ3L)/(DQ1L)	P1	BRDG_INT
IO, VREFB2N1	N5	FX3_CTL11
IO, DIFFIO_L34p, (DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)	P4	
IO, DIFFIO_L34n, (DQ1L)/(DQ3L)/(DQ1L)	P3	
IO, DIFFIO_L35p, (DM1L/BWS#1L)/(DM3L/BWS#1L)/(DM1L/BWS#1L)	U2	BOM_VER2
IO, DIFFIO_L35n, (DQ3L)/(DQ3L)/(DQ1L)	U1	BOM_VER3
IO, DIFFIO_L38p, (DQ3L)/(DQ5L)/(DQ1L)	V2	DDR2_2_BA2
IO, DIFFIO_L38n, (DQ3L)/(DQ3L)/(DQ1L)	V1	DDR2_1_BA2
IO, VREFB2N2	P5	VREF DDR2
IO, DIFFIO_L41p, (DQ3L)/(DQ1L)	N6	FX3_CTL12
IO, DIFFIO_L41n	M7	FX3_CTL7
IO, DIFFIO_L42p	M8	FX3_CTL8
IO, DIFFIO_L42n	T8	DDR2_2_A7
IO, DIFFIO_L44p, (DQ3L)/(DQ3L)/(DQ1L)	W2	DDR2_1_A11
IO, DIFFIO_L44n, (DQ3L)/(DQ3L)/(DQ1L)	W1	DDR2_1_A0
IO, DIFFIO_L45p, (DQ3L)/(DQ3L)/(DQ1L)	V2	DDR2_1_A6
IO, DIFFIO_L45n, (DQ3L)/(DQ3L)/(DQ1L)	V1	DDR2_1_A8
IO, VREFB2N2	N7	FX3_DCTL10
IO, DIFFIO_B50n, (DQ3L)/(DQ3L)/(DQ1L)	AA1	DDR2_1_A4
IO, RUP1	V4	DDR2_1_BA0
IO, RDN1	V3	DDR2_1_BA1
IO, DIFFIO_L52p	P6	DDR2_1_ODT
IO, (DQS3L/CQ3L#,DPCLK1)/(DQS3L/CQ3L#,DPCLK1)	T5	DDR2_1_RASn
IO, VREFB2N3	U4	DDR2_1_CASn
IO, DIFFIO_L53p	R5	DDR2_1_CSn
IO, DIFFIO_L53n	R6	DDR2_1_CKE
IO, DIFFIO_L53n	R7	DDR2_1_WE
IO, DIFFIO_B32n, (DQS4B/CQ5B,DPCLK4)/(DQS4B/CQ5B,DPCLK4)	V13	DDR2_2_DQ8
IO, DIFFIO_B33p, (DQ4B)/(DQ5B)/(DQ5B)	Y13	DDR2_2_DQS1
IO, DIFFIO_B34p, (DQ4B)/(DQ5B)/(DQ5B)	AA15	DDR2_2_DQ10
IO, DIFFIO_B35p, (DM2B)/(DM5B/BWS#5B)/(DMS5B/BWS#5B)	A12	DDR2_2_DM0
IO, DIFFIO_B35n, (DQ2B)/(DQ5B)/(DQ5B)	AB16	DDR2_2_DQ6
IO, DIFFIO_B36n	T13	DDR2_2_ODT
IO, DIFFIO_B36p	V13	DDR2_2_BA1
IO, DIFFIO_B38n	U13	DDR2_2_BA0
IO, DIFFIO_B39p, (DQ2B)/(DQ5B)/(DQ5B)	Y14	DDR2_2_DQ1
IO, DIFFIO_B39n	U14	DDR2_2_A12
IO, DIFFIO_B40p	U15	DDR2_2_A0
IO, DIFFIO_B41n, (DQ2B)/(DQ5B)/(DQ5B)	V15	DDR2_2_DQ0
IO, DIFFIO_B42p	T14	DDR2_2_A2
IO, DIFFIO_B42n, (DQ2B)/(DQ5B)/(DQ5B)	T15	DDR2_2_DQ4
IO, (DQ5B)/(DQ5B)/(DQ5B)	AB18	DDR2_2_DQ3
IO, DIFFIO_B43p	AA17	DDR2_2_A1
IO, DIFFIO_B43n	AB17	DDR2_2_A10
IO, VREFB4N1	AA18	VREF DDR2
IO, RUP2	AA19	
IO, RDN2	AB19	
IO, DIFFIO		

NF elements on sheet: R49
Number of NF elements on sheet: 1

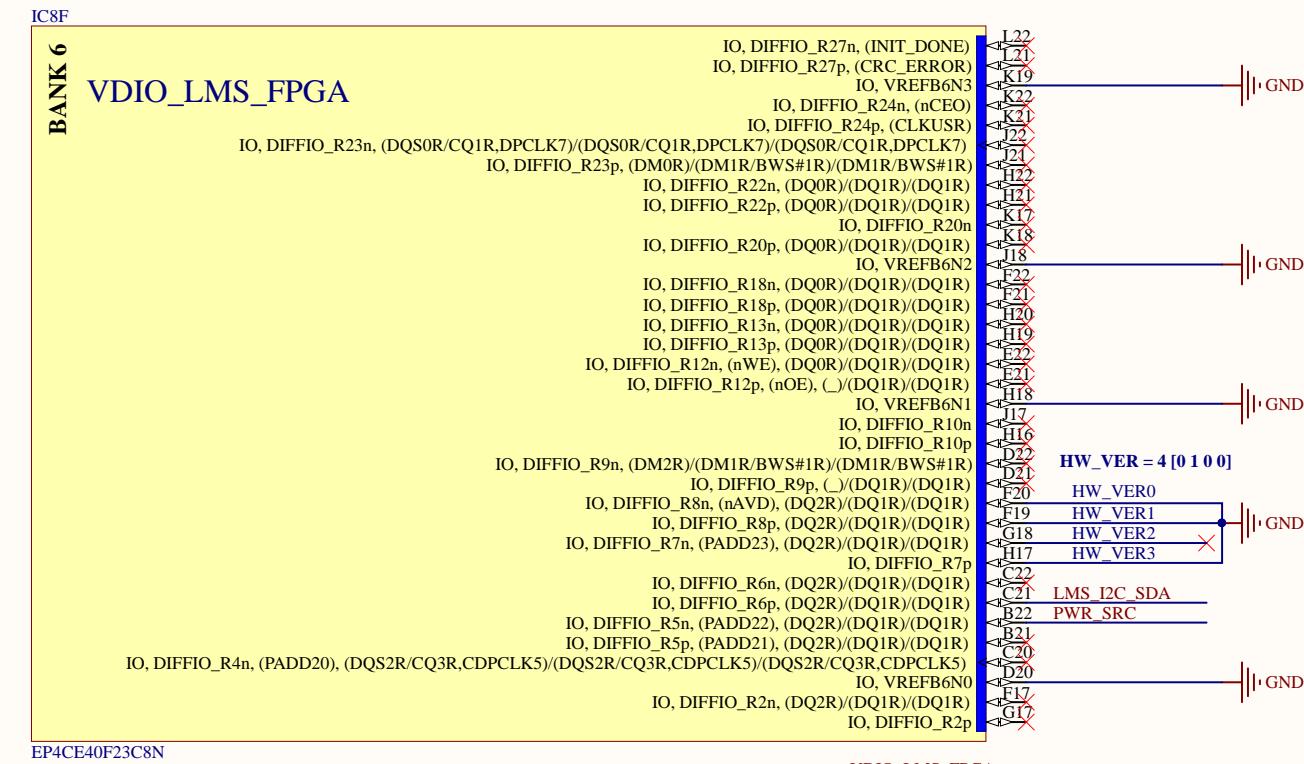
FPGA banks 5, 6, 7, 8



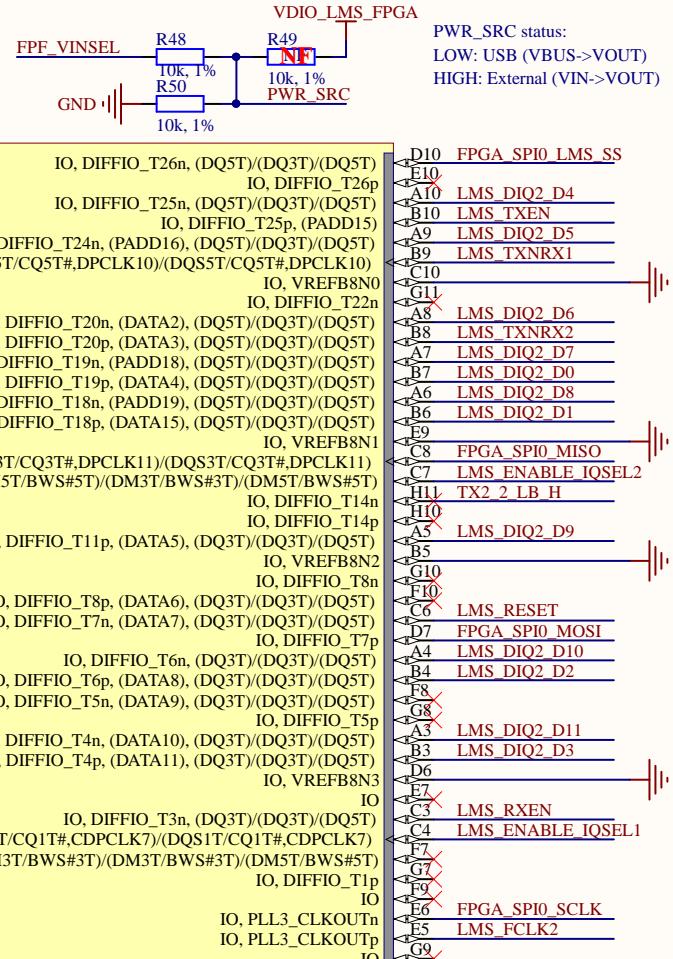
EP4CE40F23C8N



EP4CE40F23C8N



EP4CE40F23C8N



EB4GE49E23G2N

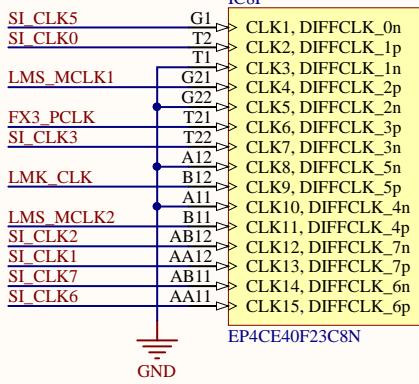
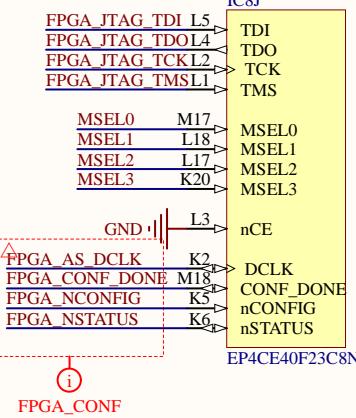
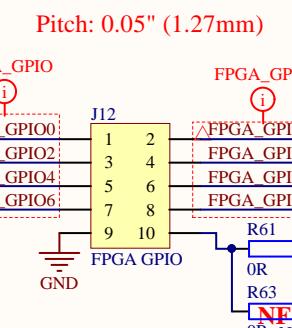
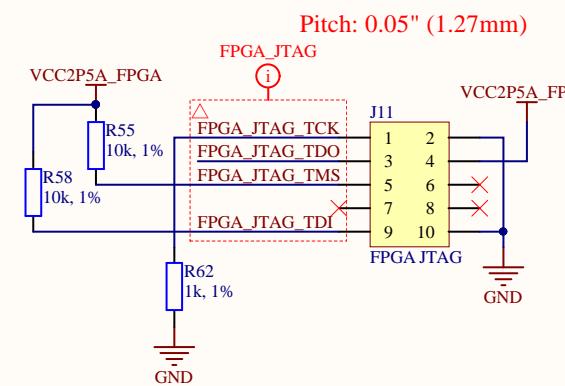
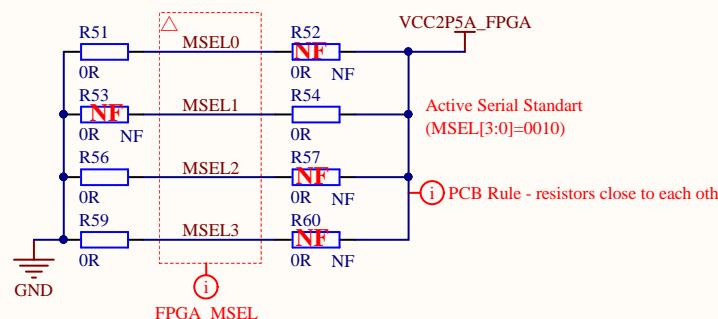
Project name: **LimeSDR-USB_1v4s.PrbPcb**

Title: FPGA banks 5, 6, 7, 8		<i>Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom</i>	
Size: A3	Revision: v1.4s		
Date: 2016-10-31	Time: 10:06:45	Sheet 9 of 15	
File: 09_FPGA_banks_5_6_7_8.SchDoc			

NF elements on sheet: R52, R53, R57, R60, R63, R65, R67, R74, J13, C142
Number of NF elements on sheet: 10

FPGA misc (power, clocks, config)

MSEL config

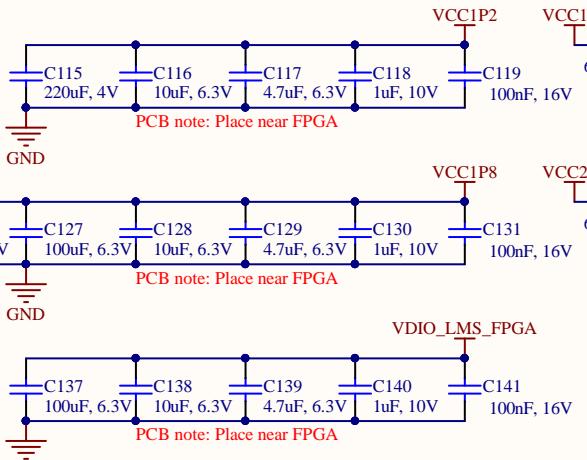
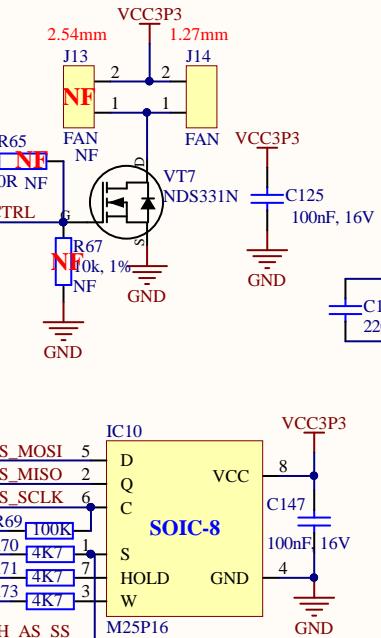
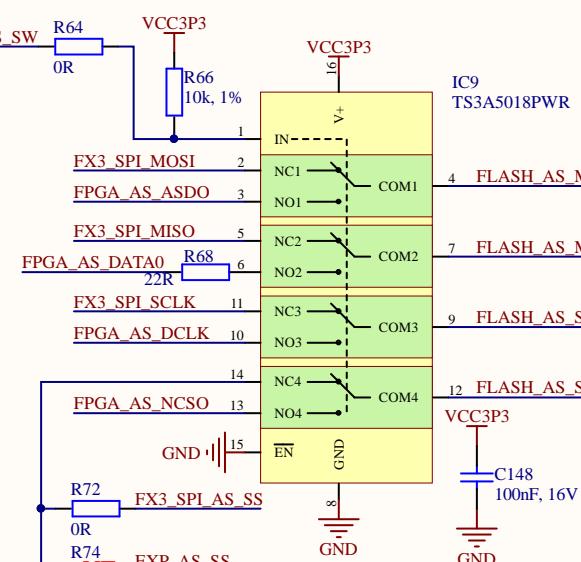


FPGA AS FLASH + Switch

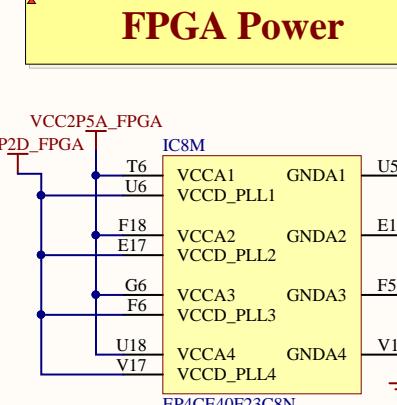
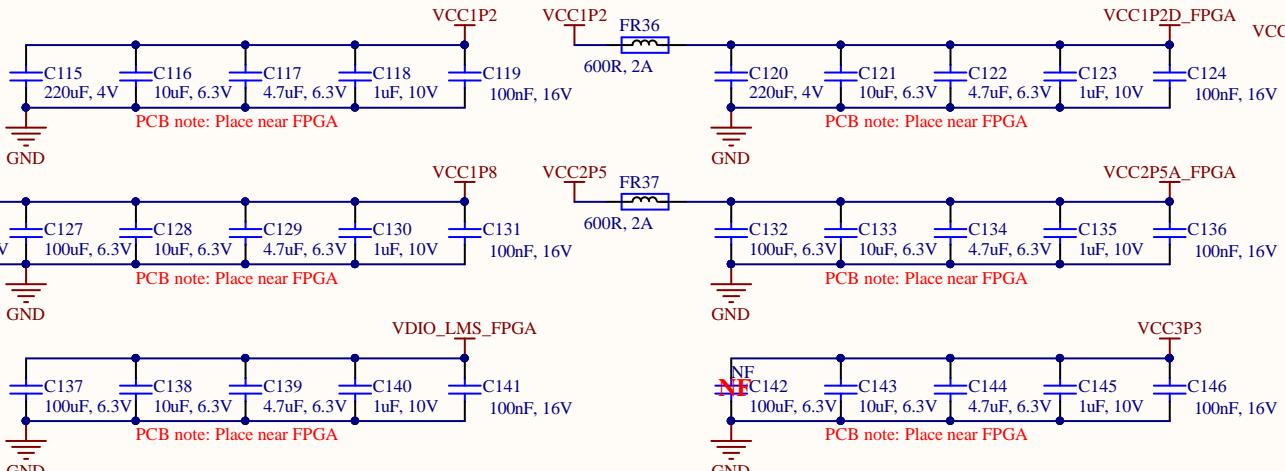
IN:

0: FLASH connected to FX3 (NC to COM)

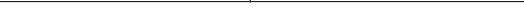
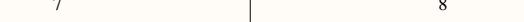
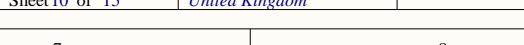
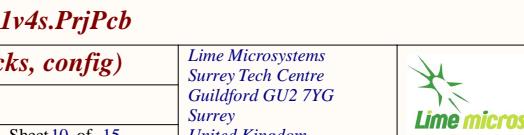
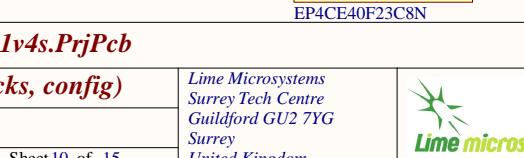
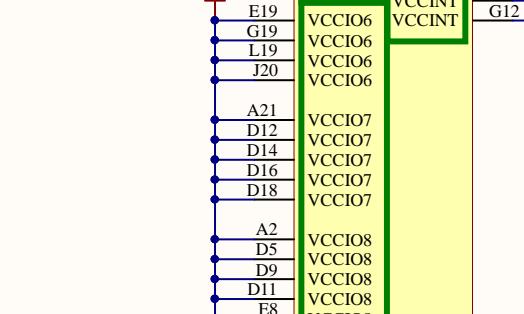
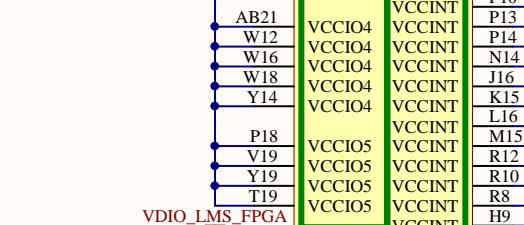
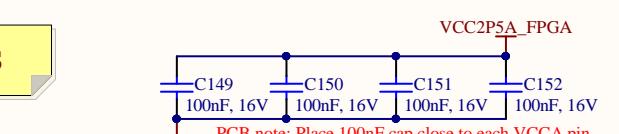
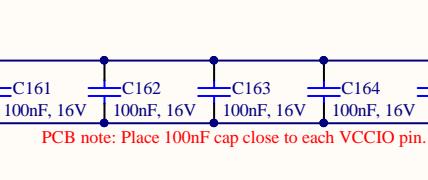
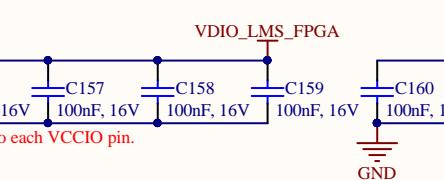
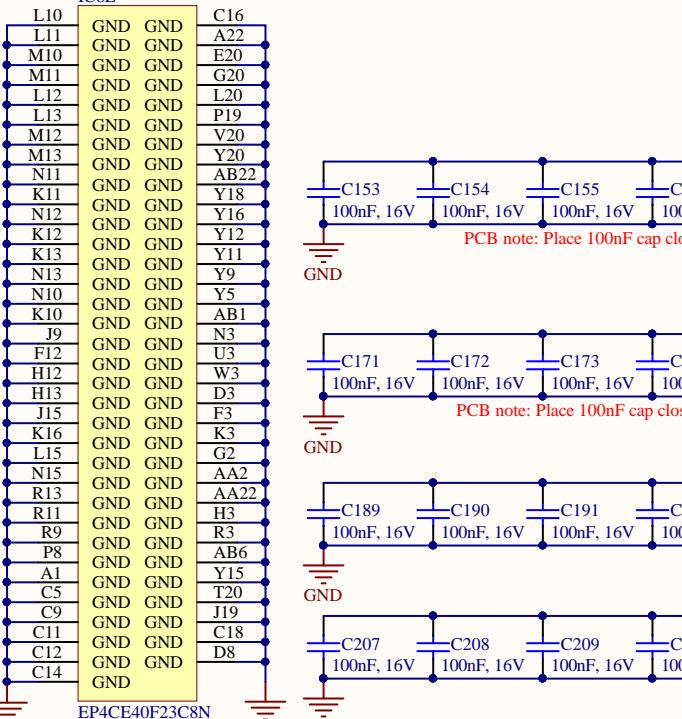
1: FLASH connected to FPGA (NO to COM)



FPGA Bulk caps

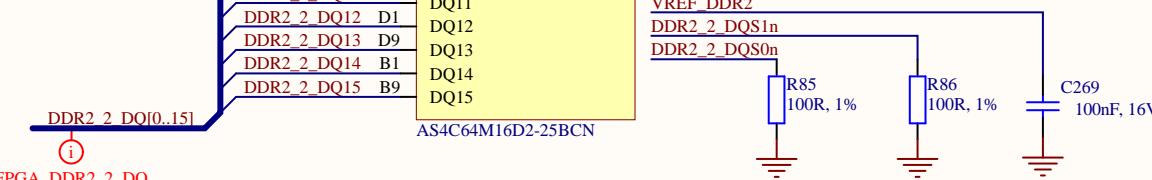
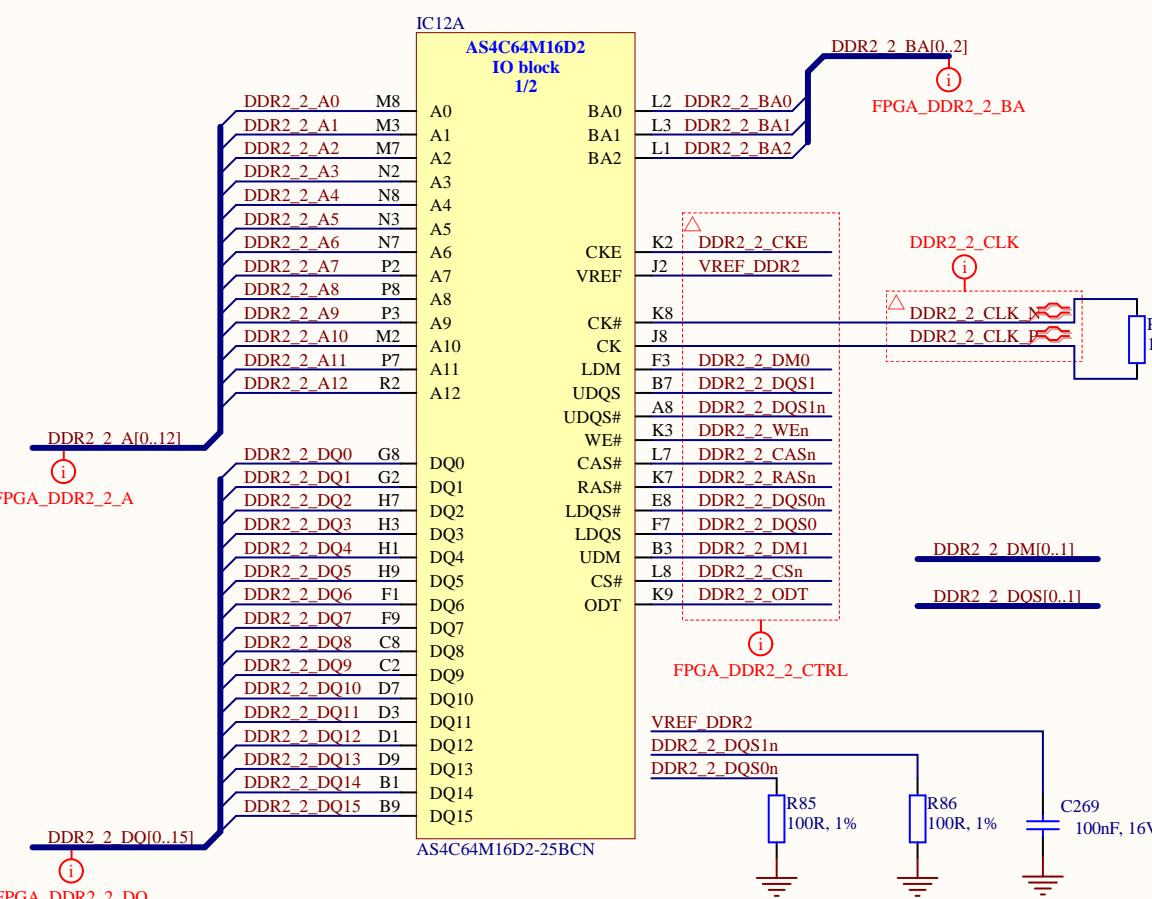
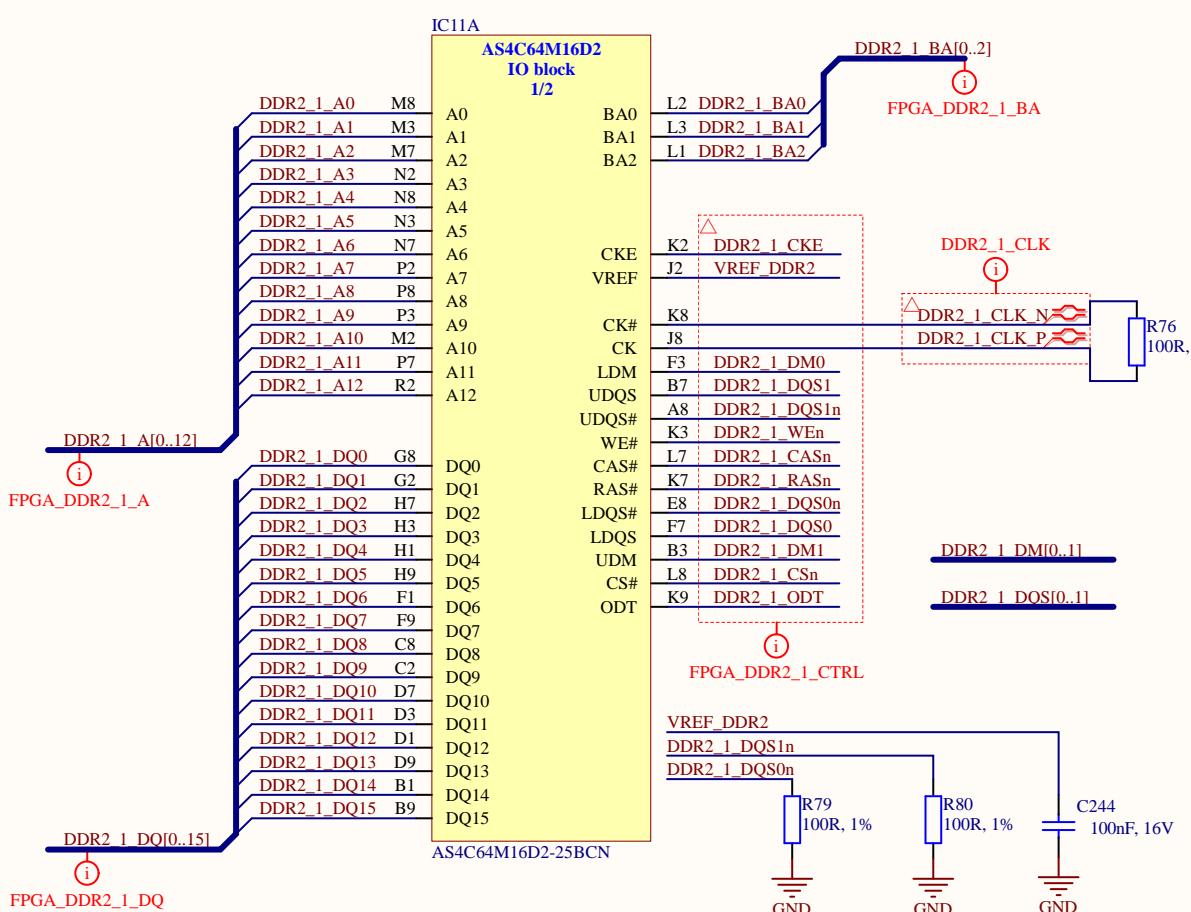


FPGA Decoupling caps



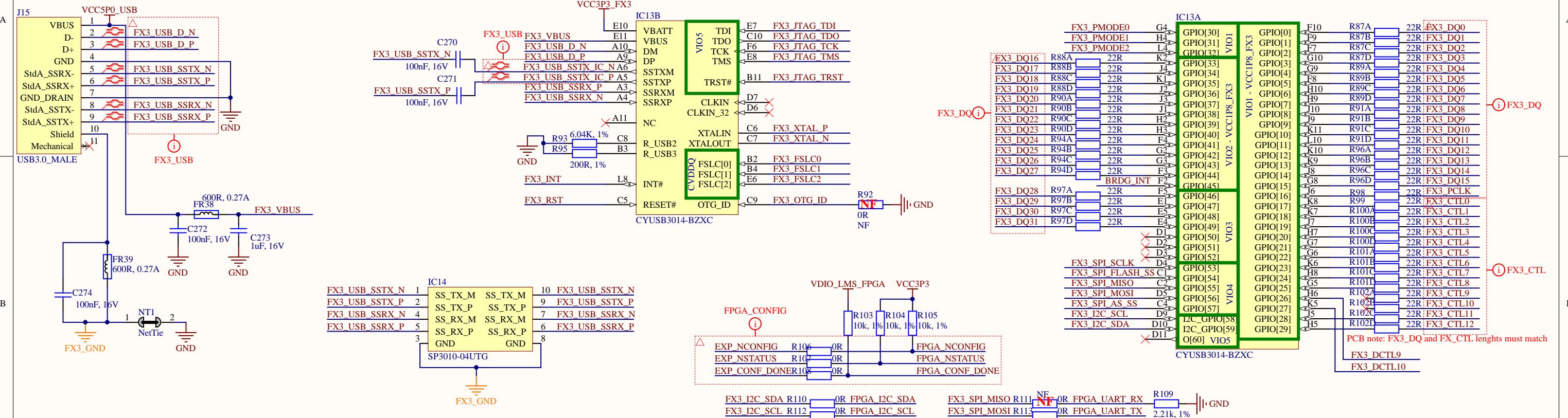
NF elements on sheet: -
Number of NF elements on sheet: 0

DDR2_1 (BOT L)

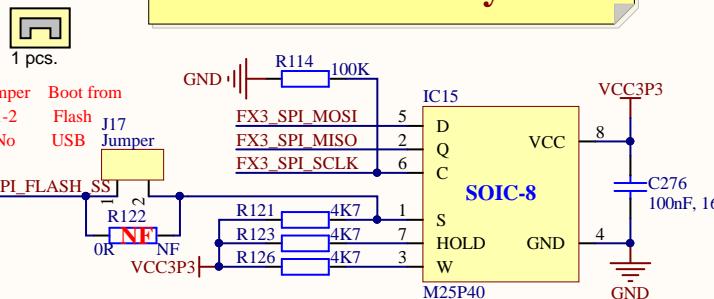


NF elements on sheet: R92, R111, R116, R119, R120, R122, R124, IC19
Number of NF elements on sheet: 8

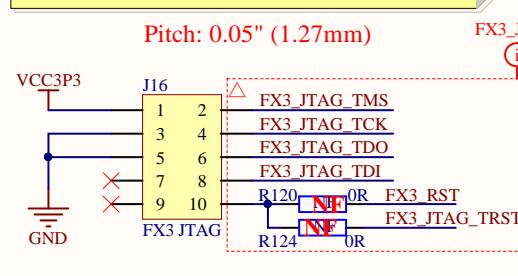
FX3 (USB3) core



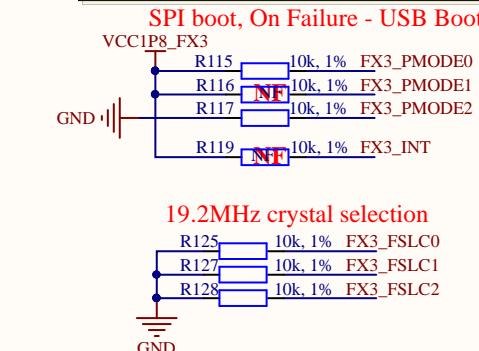
FX3 memory



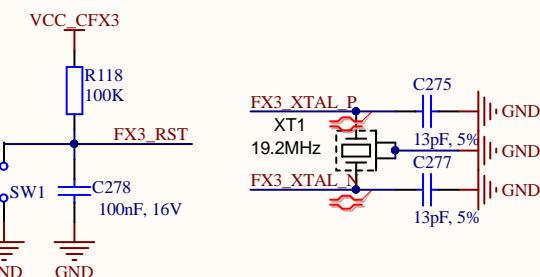
FX3 JTAG (10 pin)



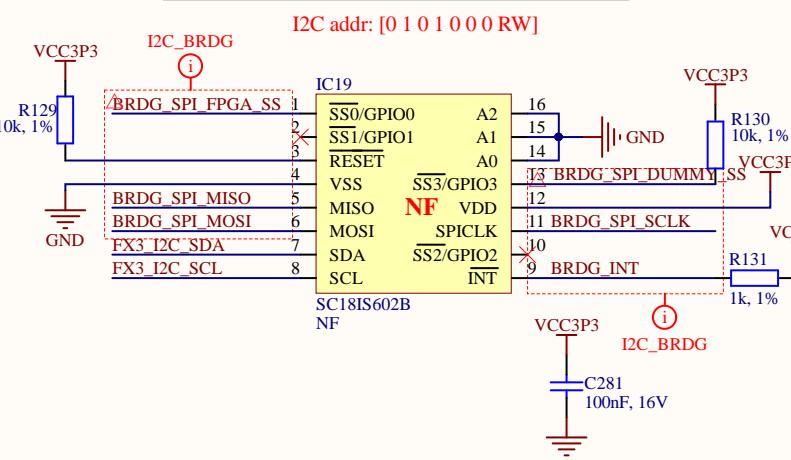
FX3 Config



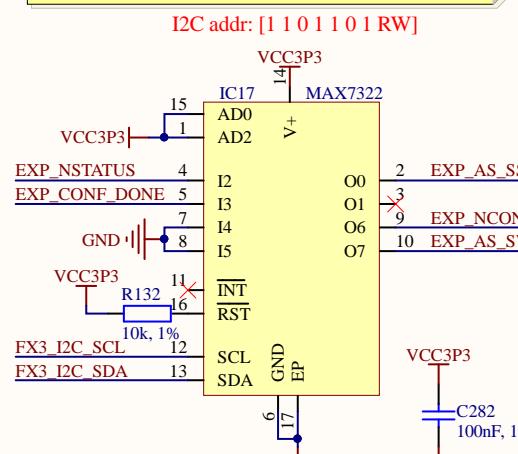
FX3 Misc



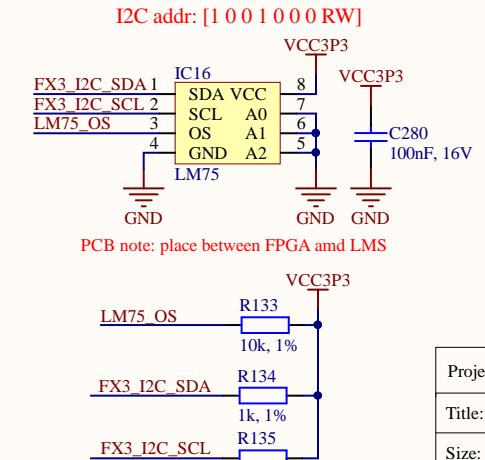
I2C SPI Bridge



I2C Port Expander



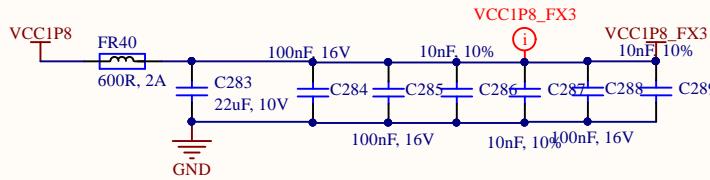
I2C Temperature sensor



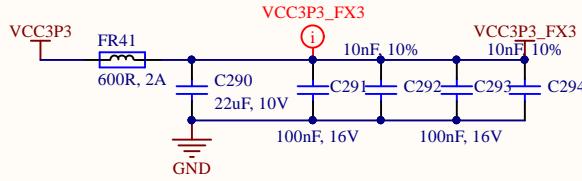
NF elements on sheet: FR42, FR43
Number of NF elements on sheet: 2

USB3 power

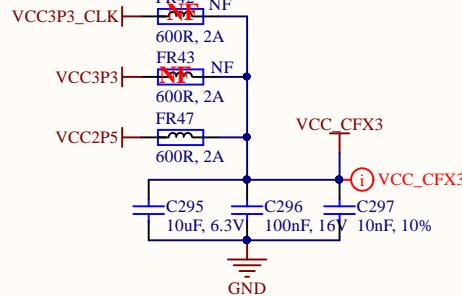
A



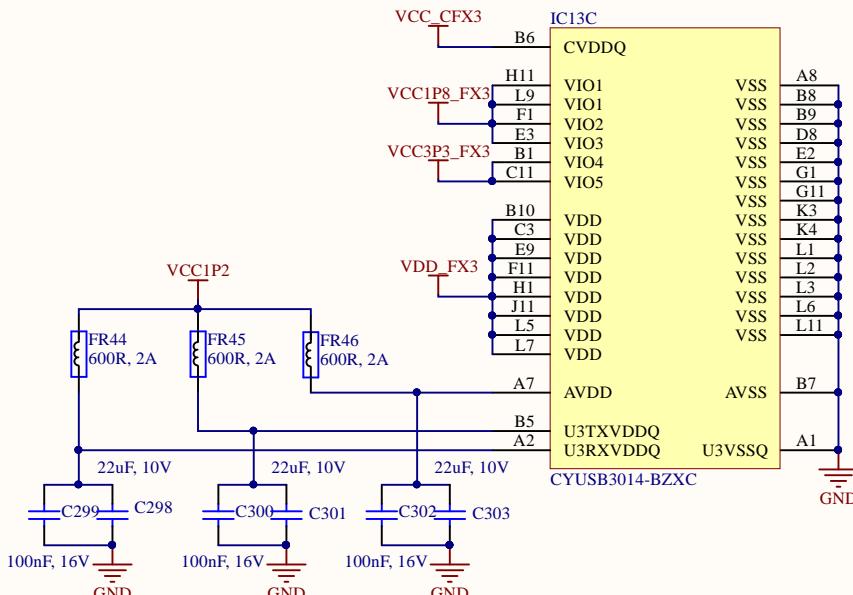
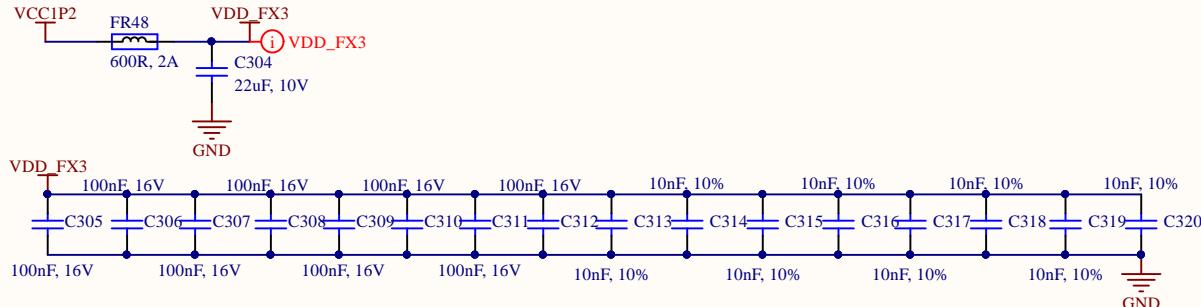
B



C



D



Project name: **LimeSDR-USB_Iv4s.PrfPcb**

Title: **USB3.0 power**

Size: **A4** Revision: **v1.4s**

Date: **2016-10-31** Time: **10:06:57** Sheet **13 of 15**

File: **13_USB3_0_power.SchDoc**

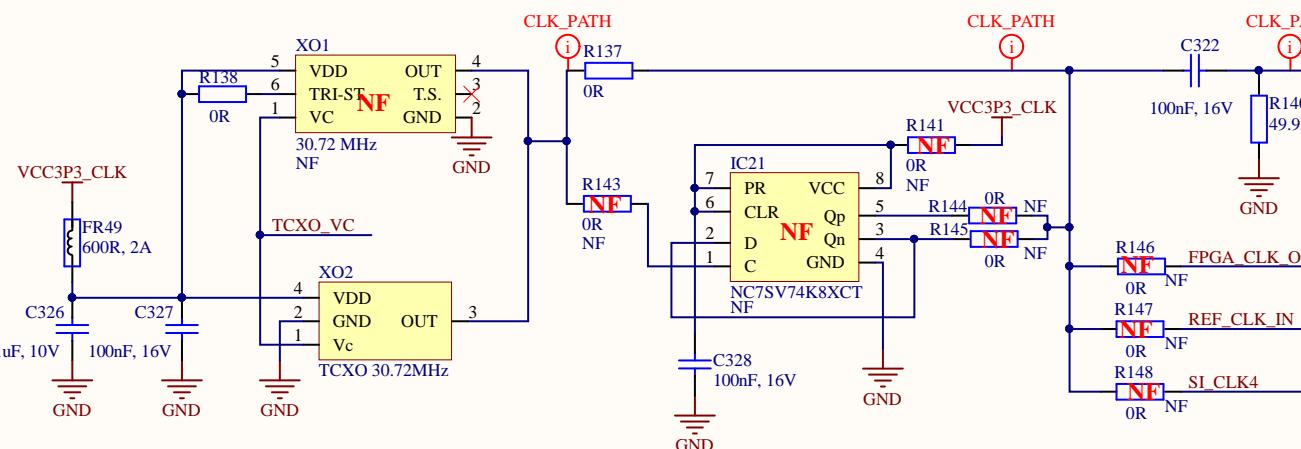
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



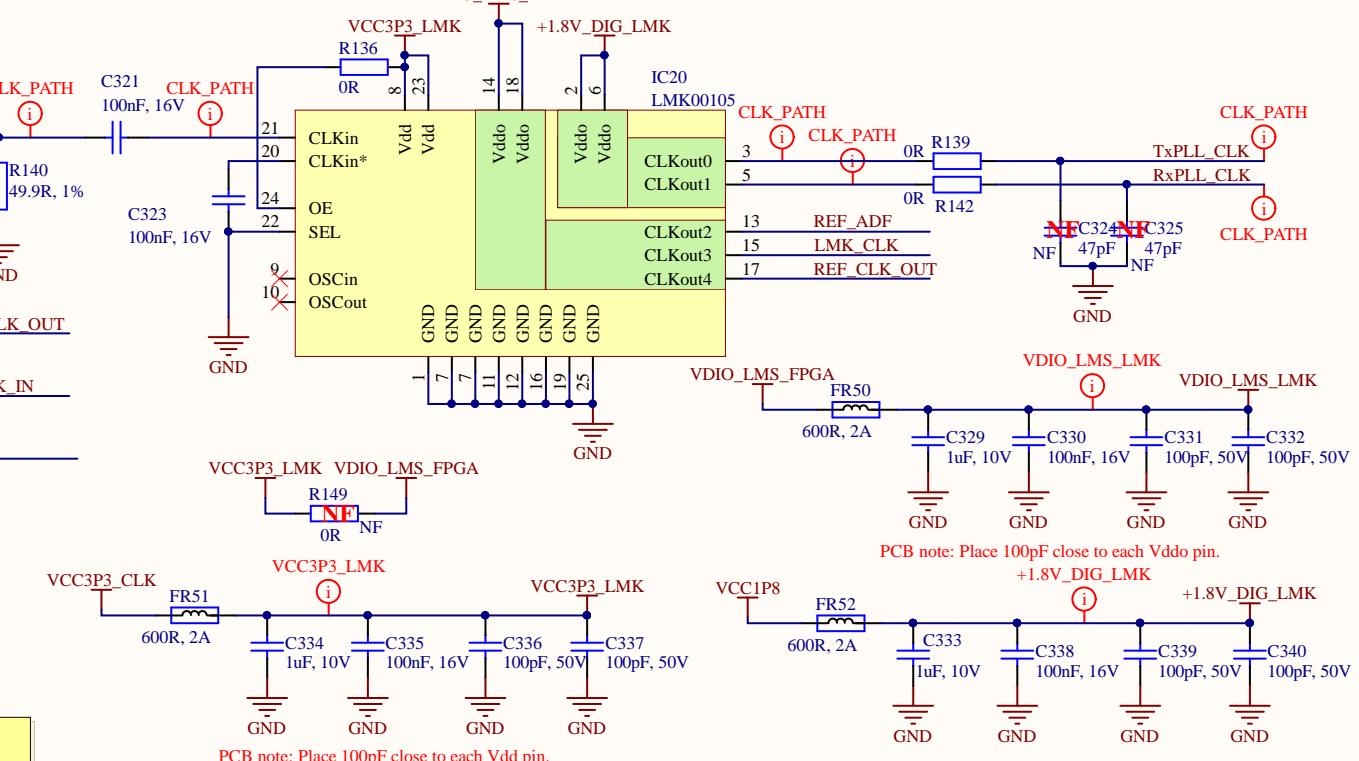
NF elements on sheet: XO1, R141, R143, R144, R145, R146, R147, R148, R149, R151, R155, C324, C325, C341, IC21
Number of NF elements on sheet: 15

Clock circuits

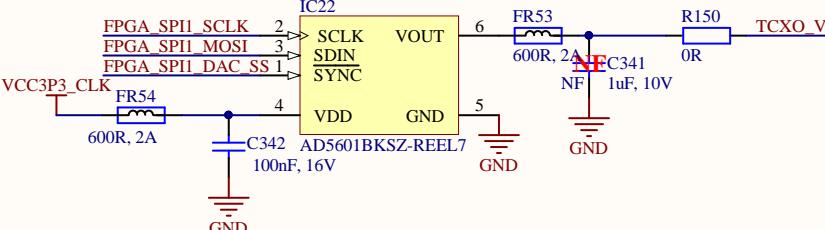
(VC)TCXO



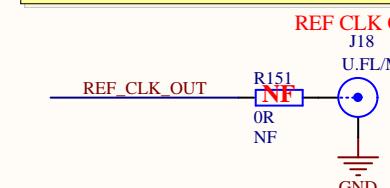
Clock buffer



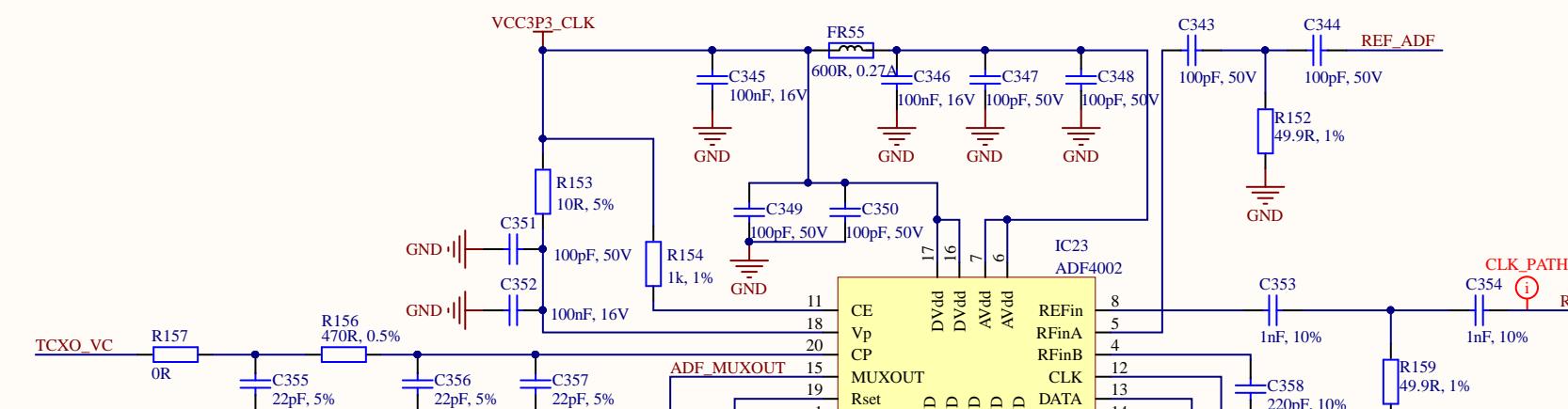
TCXO DAC



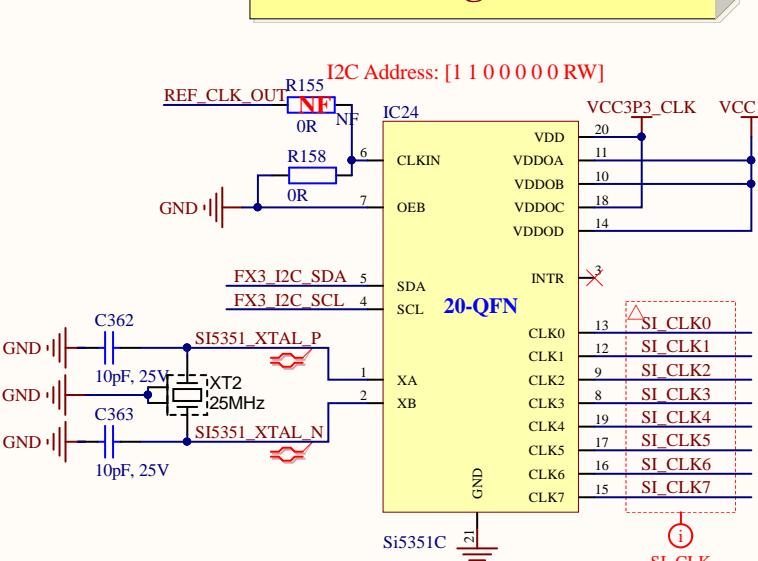
REF CLK OUT



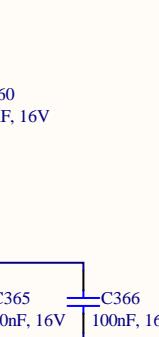
Phase detector



Clock generator



VCC3P3_CLK



Project name: LimeSDR-USB_1v4s.PrfPcb

Title: Clocks

Size: A3

Revision: v1.4s

Date: 2016-10-31 Time: 10:06:59 Sheet 14 of 15

File: 14_Clocks.SchDoc



NF elements on sheet: R166, R167, R172, R177, R181, R196, R212, J21, LED3, LED4, LED5, LED6, LEDS1, LEDS2
Number of NF elements on sheet: 14
Total number of NF elements on all sheets: 60

Board power circuits

