Intel® Dual-Band Wireless-AC 7265; Intel® Dual-Band Wireless-N 7265; Intel® Wireless-N 7265 (Stone Peak 2 M.2 2230 and 1216); Intel® Dual-Band Wireless-AC 3165 (Stone Peak M.2 2230)

External Product Specification (EPS)

September 2018

Revision 4.1

Intel Confidential

Revision History

Revision	Description	Date
0.8	Initial release	October 3, 2013
1.0	Added Section 1 – Android* POR note Added Section 6 – receive sensitivity targets Added Section 7.2.6 – note regarding SAR SKU transmit power setting Updated Section 3.4 – power consumption targets	November 12, 2013
1.1	Added Section 7 Wi-Fi Throughput Targets	December 4, 2013
2.0	Added Section 3.4.3.1 – L1 PM substates Control Register Updated Section 3.4 – power consumption tables Updated Section 3.6 – regarding LED open drain status Updated Section 6 – RX sensitivity tables Updated Section 8 – TX power tables	April 3, 2014
3.0	Updated Section 4.1 – PCIe Interface, signal rise time Updated Section 8.2.1 – Channel configuration Updated Section 8.2.3 – TX power tables	May 1, 2014
3.1	Added Section 9.3.1 Antenna connector insertion tool Updated Section 3.6 LED indicators	May 21, 2014
3.2	Added Stone Peak 1 Added Stone Peak 2 1216 (merged from previously separate 1216 EPS) Added Stone Peak 1216 1.8 V – change to internal 1.8 V supply	December 12, 2014
3.3	Updated Section 3 – airplane mode implementation recommendation Updated Section 5 – updated power consumption targets Updated Section 11 – updated weight details	April 9, 2015
3.4	Updated Regulatory: Added default Tx power table (in addition to FCC and ROW). Removing WW tables, since we have "default" tables Added some fixes to the regulatory per country specifications Added Power up testing limitations Added Schematic Review guidelines Updated Antenna specification (swapped 1216 and 2230) Updated with text fixes, plus cleaning of 2230/1216 reference Added StP1 1216SD Updated 1216SD 3D drawing	July 21, 2015
3.5	Added requirement for the PERST# rise time Updated Section 3 with heading fixes	November 24, 2015
3.6	Updated more requested data on PERST Rise-time requirement Updated the PDG appendix section Added StP-D1 support for Bluetooth 4.1 and 4.2	December 10, 2015
3.7	Section 6 – Updated Bluetooth RX/TX Sensitivity Section 7 – Updated Bluetooth TX Power Section 8 – Updated Bluetooth Throughput	April 29, 2016

Revision	Description	Date
3.8	Added StP-D1 device description to the HW SKUs to Table 1-1	November 24, 2016
3.9	Updated Table 3-3 (Platform power rail slew rate) with min/max values	February 28, 2018
4.0	Added StP SKU with customer (low) Tx power to Table 1-1	May 30, 2018
4.1	Updated Table 3-3 (Platform power rail slew rate) with min value (0.5mSec instead of 1mSec) Updated Bluetooth Tx power numbers for the 1216 form factor in Section 7	September 4, 2018

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1   Introduction

Targeting the Ultrabook™, notebook, and desktop platform intercept for BTS '14, Intel provides a very high-throughput (VHT-5G, IEEE802.11ac compliant) Wi-Fi and Bluetooth® (BT) combination product as well as a discrete Wireless LAN (Wi-Fi) that meets Ultrabook™ and Microsoft* Windows* 8.1 Connected Standby requirements.

Intel® Dual Band Wireless-AC 7265 (code name Stone Peak 2 or StP2) is the VHT-5G Wi-Fi 2x2 and Bluetooth combination single-chip solution. StP2 uses Intel's 2nd generation 802.11ac Wi-Fi solution and supports both 2.4 and 5.2 GHz bands. The 5.2 GHz band operates on an 80 MHz-wide channel reaching PHY rates of up to 867 Mbps. StP2 uses a Bluetooth core that supports Bluetooth® 4.0 standard including Bluetooth® 4.0 Low Energy (BLE). StP2-D1 version supports Bluetooth® 4.1 and 4.2 standard. StP 2 comes in two form factors: M.2 2230 and M.2 1216 (soldered down module). StP2 has two antenna ports: one for Wi-Fi only and the second shared between Wi-Fi and Bluetooth. Wi-Fi supports Rx antenna diversity.

Intel® Dual Band Wireless-AC 3165 (code name Stone Peak 1 or StP1) is the VHT-5G Wi-Fi 1x1 and Bluetooth combination single-chip solution. StP1 uses Intel's 2nd generation 802.11ac Wi-Fi solution and supports both 2.4 and 5.2 GHz bands. The 5.2 GHz band operates on an 80 MHz-wide channel reaching PHY rates of up to 433 Mbps. StP1 uses a Bluetooth core that shall support Bluetooth® 4.0 standard including Bluetooth® 4.0 Low Energy (BLE). StP1 has two antenna ports: one for Wi-Fi only and the second shared between Wi-Fi and Bluetooth. Wi-Fi supports Rx antenna diversity.

Table 1-1 lists the Stone Peak SKUs.

Note:

- AMT applicable for Microsoft Windows* OS only and only for StP2
- 802.11 AC POR TBD for non-Microsoft Windows* OS
- Android* POR is TBD

Table 1-1   Stone Peak SKUs product/technology

Product (*)	FF	Model #	Target platforms	OS support	Instant Go	Intel® vPro Technology
Intel® Dual Band Wireless-AC 7265 (2×2 AC + BT 4.0)	M.2 1216	7265D2WGW	BDW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	Y
Intel® Dual Band Wireless-N 7265 (2×2 AGN + BT4.0)	M.2 1216	7265D2W ANG	BDW, BSW. SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	Y
Intel® Dual Band Wireless-AC 7265 (2×2 AC + BT 4.0)	M.2 1216 1.8 V	7265.D2WG18V	CHT	Windows 8.1* Windows 10*	Y	N
Intel® Dual Band Wireless-N 7265 (2×2 AGN + BT 4.0)	M.2 1216 1.8 V	7265.D2WANG18V	CHT	Windows 8.1* Windows 10*	Y	N
Intel® Dual Band Wireless-AC 7265 (2×2 AC + BT 4.0)	M.2 2230	7265NGW	BDW, HSW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	Y

Product (*)	FF	Model #	Target platforms	OS support	Instant Go	Intel® vPro Technology
Intel® Dual Band Wireless-AC 7265 (2×2 AC + BT 4.0) – Consumer (No vPro)	M.2 2230	7265NGWG.NV	BDW, HSW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	N
Intel® Dual Band Wireless-N 7265 (2×2 AGN + BT 4.0)	M.2 2230	7265NGW AN	BDW, HSW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	Y
Intel® Dual Band Wireless-N 7265 (2×2 AGN) 1	M.2 2230	7265NGW NB	BDW, HSW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	Y
Intel® Wireless-N 7265 (2×2 BGN + BT 4.0)	M.2 2230	7265NGW BN	BDW, HSW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	N
Intel® Dual Band Wireless-AC 3165 (1×1 AC + BT 4.0)	M.2 2230	3165NGWG	BDW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	N
Intel® Dual Band Wireless-AC 3165 (1×1 AC + BT 4.0)	M.2 1216	3165D2WG	BDW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	N
Intel® Dual Band Wireless-AC 7265 (2×2 AC + BT 4.2) – Consumer (No vPro)	M.2 2230	7265.NGWG.NVB (944401)	BDW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	N
Intel® Dual Band Wireless-AC 7265 (2×2 AC + BT 4.2) – Consumer (No vPro) Low Tx Power (SAR)	M.2 2230	7265.NGWG.NVS B (944402)	BDW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	N
Intel® Dual Band Wireless-AC 7265 (2×2 AC + BT 4.2) – Consumer (No vPro)	M.2 1216	7265.D2WG.NVB (944431)	BDW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	N
Intel® Dual Band Wireless-AC 7265 (2×2 AC + BT 4.2) – Consumer (No vPro) Low Tx Power (SAR)	M.2 1216	7265.D2WG.NVS B (944432)	BDW, BSW, SKL	Windows 7* Windows 8* Windows 8.1* Windows 10*	Y	N
Intel® Dual Band Wireless-AC 7265 (2×2 AC + BT 4.2) No vPro, Custom Power Tables	M.2 1216	7265.D2GGL.NVB (962475)	KBL	Chrome	N	N

(*) Support of Bluetooth® 4.1 and 4.2 standard requires SKUs that use the StP-D1 silicon

From a host interface perspective, Wi-Fi COM will use the legacy PCIe* interface. The Bluetooth part of StP1 and StP2 shall support USB interfaces.

All Stone Peak SKUs use the same Si, board and software. The only difference is the module label and EEPROM (to select 2×2 or 1×1, disable .11ac, .11a, and/or BT functionality).

Stone Peak SD 3.3 V supports platforms with 3.3 V IOs. The power supply for this module is 3.3 V only. The StP2 SD 1.8 V module supports platforms with VDD IO of 1.8 V. The 1.8 V to the GPIOs is generated internally in the module, no need for external 1.8 V.

Table 1-2   Intel® Dual Band Wireless-AC product features

Feature	Stone Peak 2	Stone Peak 1
Wi-Fi standard	802.11ac 2×2	802.11ac 1×1
Antennas	2	2
Wi-Fi TX/RX chains	2×2 chains	1×1 chains
Supported Bands	2.4 GHz, 5 GHz	2.4 GHz, 5 GHz
Antenna Allocation	• Wi-Fi Only • Shared Wi-Fi-BT	• Wi-Fi only • Shared Wi-Fi-BT
Wi-Fi TX/RX Throughput	867 Mbps	433 Mbps
Bluetooth Core	Bluetooth® 4.0 (4.1, 4.2 for StP2-D1 SKUs)	Bluetooth® 4.0
Intel® WiDi Support	Intel® WiDi 5	Intel® WiDi 5
Single/Dual chip	Single	Single
Windows* OS AOAC	Microsoft CS and Intel® Smart Connect Technology	Microsoft CS and Intel® Smart Connect Technology not suppored
OS	Microsoft Windows 7*, Microsoft Windows 8*, Windows 8.1*, Linux*, Chrome* OS v29	Microsoft Windows 7*, Microsoft Windows 8*, Windows 8.1*, Windows 10*, Linux*
Wi-Fi Alliance certifications for Windows OS	802.11ac, 802.11n, 802.11w, StPA, StPS, WMM, WFD, Wi-Fi Direct	802.11ac, 802.11n, 802.11w, StPA, StPS, WMM, WFD, Wi-Fi Direct
Wi-Fi Alliance certifications for Chrome OS	802.11n, StPA, WMM,	802.11n, StPA, WMM
Microsoft certifications	Microsoft Windows 8.1 Logo*, Microsoft Windows 7 Logo*, Windows 8.1 Connected Standby Logo*	Microsoft Windows 8.1 Logo*, Microsoft Windows 7 Logo*, Windows 8.1 Connected Standby Logo*
Chrome certification	Pass AVL (StP2 only)	
Bluetooth	Integrated Bluetooth® Intel® Bluetooth® Core Bluetooth® certification BT4.0 LE – Smart Ready – Intel responsible for BT certification for Android and Windows only.	Integrated Bluetooth® Intel® Bluetooth® Core Bluetooth® certification BT4.0 LE – Smart Ready – Intel responsible for BT certification for Android and Windows only.
Software compatibility for Windows based OS	Intel® PRO/Set Wireless Software v17.0 and later.	Intel® PRO/Set Wireless Software v17.5 and later.
Software compatibility for Chrome (StP2 only)	Adapt our Wi-Fi/BT solution to work with Kernel 3.8 and without Compat. For Wi-Fi – we provide our driver + our MAC80211 BT stack supported BlueZ 5.3.	

Feature	Stone Peak 2	Stone Peak 1
Intel® Active Management Technology v9.5 (Windows only)	Support for Intel® AMT 10.0 on Broadwell Y and Broadwell U. StP2 vPro SKUs Only	
Cisco-Compatible Extensions -CCX. (Windows* only)	Support for CCX4 and on Microsoft Windows 7*, CCX Lite** on Microsoft Windows 8* **Pending Cisco* program definition and rollout **NOTE:** CCX supported only when the host OS is Windows.	
Advanced Bluetooth-Wi-Fi co-existence	Intel's coexistence scheme, implementing internal messaging protocol, and supporting a tight/loose coexistence scheme for different antenna isolations. **NOTE:** No support for external Wi-Fi-Bluetooth coexistence signaling.	Intel's coexistence scheme, implementing internal messaging protocol, and supporting a tight/loose coexistence scheme for different antenna isolations. **NOTE:** No support for external Wi-Fi-Bluetooth coexistence signaling.
Platform power/Extending battery life	Intel Power Optimizer (CPPM) For Linux-based OS – no support for RTD3.	Intel Power Optimizer (CPPM) For Linux-based OS – no support for RTD3.

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2 System Architecture

Both the Stone Peak 1 and Stone Peak 2 contain a single chip Wi-Fi + Bluetooth solution, including Wi-Fi MAC and PHY as well as Bluetooth MAC and PHY.

The modules are M.2 format.

Figure 2-1   Stone Peak 2 block diagram
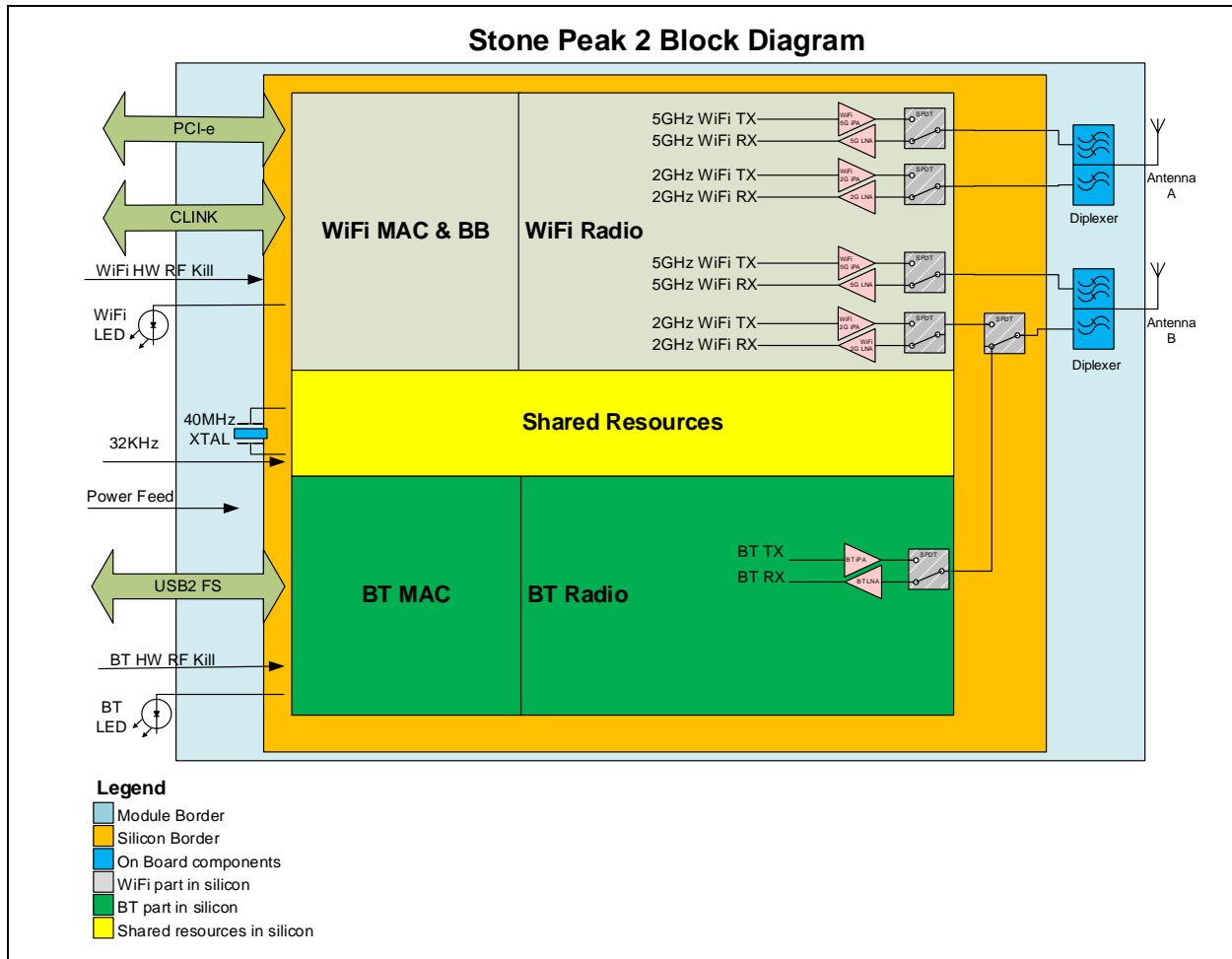
The StP1 block diagram is basically the same as the StP2 block diagram. The main difference is that the StP2 is capable of transmitting and receiving MIMO packets and rates.

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3   Electrical Specifications

This section provides electrical specification information for the product's hardware. The specification covers the module hardware interface signals, power consumption, and DC/AC characteristics.

3.1   PCIe* hardware interface signals

The hardware design is based on the PCI Express* M.2 Specification. Table 3-1 describes the system interface signals. For more details see the *PCI Express M.2 Specification.*

3.2   M.2 form factor

The M.2 form factor (M.2), is the designated codename for the NIC, used for mobile add-in cards. The M.2 is a natural transition from the mini card and half mini card to a smaller form factor in both size and volume. M.2 is a form factor that will enable integration of functions into a single module solution.

M.2 modules and the corresponding system interconnect based on a 67/49-pin edge card connection scheme and a 69-pad soldered down scheme for system interfaces.

See the latest M.2 Specification document under the PCISIG releases:
http://www.pcisig.com/specifications/pciexpress/review_zone/#M.2

3.3   M.2 2230 hardware interface signals

Table 3-1   M.2 2230 module side pinout

Pin/Pad number	Function (print side)	Function (component side)	Pin/Pad number
74	3.3 V	GND	75
72	3.3 V	N/C	73
70	N/C	N/C	71
68	N/C	GND	69
66	N/C	N/C	67
64	N/C	N/C	65
62	N/C	GND	63
60	N/C	N/C	61
58	N/C	N/C	59
56	W_DISABLE1# (I)(0/3.3 V)	GND	57
54	W_DISABLE2# (I)(0/3.3 V)	PEWAKE0# (IO)(0/3.3 V)	55
52	PERST0#(I)(0/3.3 V)	CLKREK0# (IO)(0/3.3 V)	53
50	SUSCLK (32 kHz) (I)(0/3.3 V)	GND	51
48	COEX1 (I/O)(0/1.8 V)	REFCLKN0	49
46	COEX2 (I/O)(0/1.8 V)	REFCLKP0	47
44	COEX3 (I/O)(0/1.8 V)	GND	45
42	CLINK CLK (I/O)	PETn0	43

Pin/Pad number	Function (print side)	Function (component side)	Pin/Pad number
40	CLINK DATA (I/O)	PETp0	41
38	CLINK Reset (I)(0/3.3 V)	GND	39
36	N/C	PERn0	37
34	N/C	PERp0	35
32	N/C	GND	33
	Module Key E	Module Key E	
	Module Key E	Module Key E	
	Module Key E	Module Key E	
	Module Key E	Module Key E	
22	N/C	N/C	23
20	N/C	N/C	21
18	GND	N/C	19
16	LED2# (O)(OD)	N/C	17
	Module Key A	Module Key A	
	Module Key A	Module Key A	
	Module Key A	Module Key A	
	Module Key A	Module Key A	
6	LED1# (O)(OD)	GND	7
4	3.3 V	USB_D-	5
2	3.3 V	USB_D+	3
		GND	1

NOTES: For more details see *Broadwell ULT Platform – Design Guide.*

3.4 M.2 1216 module side hardware interface signals

Table 3-2 M.2 1216 pinout

Pin #	Pin definition according to M.2 1216 spec	Pin assignment for StP2/StP1 M.2 1216 3.3 V	Pin assignment for StP2/StP1 M.2 1216 1.8 V	Pin description
1	UIM_POWER_SRC/GPIO1	NC	NC	
2	UIM_POWER_SNK	NC	NC	
3	UIM_SWP	NC	NC	
4	3.3 V	3.3 V	3.3 V	M.2 Power Pins
5	3.3 V	3.3 V	3.3 V	M.2 Power Pins
6	GND	GND	GND	M.2 Ground (GND)
7	RESERVED (NFC_RESET#)	NC	NC	
8	ALERT#	NC	NC	

Pin #	Pin definition according to M.2 1216 spec	Pin assignment for StP2/StP1 M.2 1216 3.3 V	Pin assignment for StP2/StP1 M.2 1216 1.8 V	Pin description
9	I2C CLK	NC	NC	
10	I2C DATA	NC	NC	
11	COEX1	NC	NC	
12	COEX2	NC	NC	
13	COEX3	NC	NC	
14	SYSCLK/GNSS0	NC	NC	
15	TX_BLANKING/GNSS1	NC	NC	
16	RESERVED	RESERVED	RESERVED	
17	GND	GND	GND	M.2 Ground (GND)
18	RESERVED	NC	NC	
19	RESERVED	NC	NC	
20	GND	NC	NC	
21	RESERVED	NC	NC	
22	RESERVED	NC	NC	
23	GND	NC	NC	
24	RESERVED	NC	NC	
25	RESERVED	NC	NC	
26	GND	GND	GND	M.2 Ground (GND)
27	SUSCLK(32 kHz)	SUSCLK(32 kHz) (3.3 V)	SUSCLK(32 kHz) (1.8 V)	SUSCLK (32 kHz)
28	W_DISABLE1#	W_DISABLE1# (3.3 V)	W_DISABLE1# (1.8 V)	Wi-Fi RF Disable
29	PEWAKE#	PEWAKE# (3.3 V)	PEWAKE# (1.8 V)	PCIe* Interface
30	CLKREQ#	CLKREQ# (3.3 V)	CLKREQ# (1.8 V)	PCIe* Interface
31	PERST#	PERST# (3.3 V)	PERST# (1.8 V)	PCIe* Interface
32	GND	GND	GND	M.2 Ground (GND)
33	REFCLKN0	REFCLKN0	REFCLKN0	PCIe* Interface
34	REFCLKP0	REFCLKP0	REFCLKP0	PCIe* Interface
35	GND	GND	GND	M.2 Ground (GND)
36	PETn0	PETn0	PETn0	PCIe* Interface
37	PETp0	PETp0	PETp0	PCIe* Interface
38	GND	GND	GND	M.2 Ground (GND)
39	PERn0	PERn0	PERn0	PCIe* Interface
40	PERp0	PERp0	PERp0	PCIe* Interface
41	GND	GND	GND	M.2 Ground (GND)
42	Vendor Defined (CLINK CLK)	CLINK CLK	CLINK CLK	CLINK Interface

Pin #	Pin definition according to M.2 1216 spec	Pin assignment for StP2/StP1 M.2 1216 3.3 V	Pin assignment for StP2/StP1 M.2 1216 1.8 V	Pin description
43	Vendor Defined (CLINK DATA)	CLINK DATA	CLINK DATA	CLINK Interface
44	Vendor Defined (CLINK RESET)	CLINK RESET	CLINK RESET (1.8 V)	CLINK Interface
45	SDIO_RESET#	NC	NC	
46	SDIO_WAKE#	NC	NC	
47	SDIO_DATA3	NC	NC	
48	SDIO_DATA2	NC	NC	
49	SDIO_DATA1	NC	NC	
50	SDIO_DATA0	NC	NC	
51	SDIO_CMD	NC	NC	
52	SDIO_CLK	NC	NC	
53	UART_UART_ WAKE#WAKE#	NC	NC	
54	UART_RTS (LPSS)	NC	NC	
55	UART_RXD (LPSS)	NC	NC	
56	UART_TXD (LPSS)	NC	NC	
57	UART_CTS (LPSS)	NC	NC	
58	PCMFR1	NC	NC	
59	PCMOUT	NC	NC	
60	PCMIN	NC	NC	
61	PCMCLK	NC	NC	
62	GND	GND	GND	M.2 Ground (GND)
63	W_DISABLE2#	W_DISABLE2# (3.3 V)	W_DISABLE2# (1.8 V)	Bluetooth RF Disable
64	LED2#	LED2#	LED2#	LED Indicators
65	LED1#	LED1#	LED1#	LED Indicators
66	RESERVED	NC	NC	
67	RESERVED	NC	NC	
68	GND	GND	GND	M.2 Ground (GND)
69	USB_D-	USB_D-	USB_D-	USB Interface
70	USB_D+	USB_D+	USB_D+	USB Interface
71	GND	GND	GND	M.2 Ground (GND)
72	3.3 V	3.3 V	3.3 V	M.2 Power Pins
73	3.3 V	3.3 V	3.3 V	M.2 Power Pins
74	GND	GND	GND	M.2 Ground (GND)
75	GND	GND	GND	M.2 Ground (GND)

Pin #	Pin definition according to M.2 1216 spec	Pin assignment for StP2/StP1 M.2 1216 3.3 V	Pin assignment for StP2/StP1 M.2 1216 1.8 V	Pin description
76	GND	GND	GND	M.2 Ground (GND)

For more details, please refer to *Broadwell ULT Platform – Design Guide.*

3.5 M.2 2230/1216 signals details

3.5.1 M.2 2230/1216 power pins

The module is fed by a 3.3 V aux rail.

For the M.2 2230 module, the power pins are pins 2, 4, 72, 74.

For the M.2 1216 module, the power pins are pins 4, 5, 72, 73. Power-filtering caps should be added to every power pin. The recommended caps are a set of 4.7uF+0.1uF+0.01uF.

Generation of PME, reporting status and enabling PME: The M.2 PCIe module uses a PME to request a change from a power savings state (S3/S4) to a fully operational state (full power) -> Wake-up Event (WoME, WoWLAN).

Note: Connecting active signals to the input pins is not allowed unless a power supply is provided to the power rails pins.

3.5.2 M.2 power and ripple limits

The module is fed by a single 3.3 V-power tail, called by the platform 3.3 V Aux. At least three of the power pins need to be connected to the platform 3.3 V aux rail.

For the 1216SD 1.8 V module, the 1.8 V power to the GPIOs is generated internally in the module itself, no need for an external feed of the 1.8 V.

3.5.2.1 M.2 power sequence

Power supply must be provided to Stone Peak module before any input signals are active. The rise time slew rate of the power (0 V to 3.3 V) must be according to Table 3-3.

Table 3-3   Platform power rail slew rate

Item	Value	
	min	max
Power feed max slew rate (0 V to 3.3 V)	0.5mSec	10mSec

The signal rise characteristics should be based on a level's ramps. An example is in Figure 3-1.

Figure 3-1   M.2 power sequence
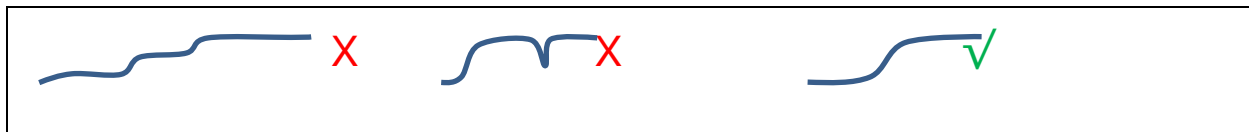
Note that there must not be a glitch on the power supply that is higher than 0.3 V; any glitch that is higher than 0.3 V might be interpreted by the Stone Peak module as a power-on reset, which will cause the card to lose stored data. In stand-by mode this will lead to connection maintenance failure. Platform designers should carefully design the transition from on state to stand-by state and vice versa so the power supply will be stable and without glitches.

3.5.2.2   M.2 power and ripple limits

Table 3-4   Platform power rail requirements

Item	Value
Power feed range	3.3 V +/– 0.165 V
Maximum ripple	200 mVPP, frequency 10–500 KHz
Allowed power rail noise	300 mVpp

3.5.3   Ground (GND)

All ground pins are connected on the M.2 to a common ground plane. The platform designer should connect all M.2 GND pins to the platform system GND.

3.5.4   Wi-Fi RF disable

Note: Chrome OS doesn't support HW RF kill or SW RF kill. Airplane mode for Chrome* OS is achieved by detaching the driver from StPA_Supplicant.

The W_DISABLE1# input signal (Pin #56 on M.2 2230 module, Pin #28 on M.2 1216 module) allows the hardware to disable the Wi-Fi RF circuitry.

The W_DISABLE1# signal is an active low signal. When driven low by the platform, this signal disables Wi-Fi radio operation. The assertion and de-assertion of the W_DISABLE1# signal is asynchronous to any platform clock. All transients resulting from mechanical switches need to be de-bounced by platform circuitry.

In normal operation, the card must stop any RF activity within seconds after the W_DISABLE1# signal is asserted. The disabling operation does not depend on SW state. The card should resume normal operation within seconds of de-assertion of the W_DISABLE1# signal.

The platform designer is required to assure that W_DISABLE1# is in a deterministic state (asserted or de-asserted) whenever power is applied to the card (for example, whenever +3.3 V is present).

If the customer does not intend to use this signal, it is recommended to leave this pin not connected.

Table 3-5   W_DISABLE1# characteristics

Characteristic	Description
Minimum Sink Current to ground	<1 mA (typical: 50 uA)
Internal pull up resistor	>100 kOhm
V_{IL} for Asserting	0.0 V [+/– 0.3 V]
V_{IH} for De-asserting	3.3 V [+/– 0.15 V] or float (not connected)

When W_DISABLE1# signal is asserted, Stone Peak will terminate all RF activities, Wi-Fi LED will be turned off and the Wi-Fi part of the device will go into low power mode.

StP SD also supports Wi-Fi SW RF Kill. The device will react to Wi-Fi SW RF Kill similar to the way it reacts to the HW RF Kill signal.

The Wi-Fi radio will be active only if both HW RF kill pin and SW RF kill mechanism are in *enable* state.

Table 3-6   Hardware RF disable logic

Software setting	Hardware Switch	Radio transmitter function
Enabled	Enabled/Float	Enabled
Enabled	Disabled/Low	Disabled
Disabled	Enabled/Float	Disabled
Disabled	Disabled/Low	Disabled

It is *not* recommended to implement airplane mode by taking down the module power of the whole NIC (WiFi+BT). The recommended approach is using HWRFKILL (W_DISABLE# pin) as described above.

For more information on the W_DISABLE1# pin, see the *PCI Express M.2 Specification* document Section 3.1.11.3.

Note: For the 1216SD 1.8 V module, this GPIO is a 1.8 V GPIO.

3.5.5   Bluetooth RF disable

Note: Chrome OS doesn't support HW RF kill or SW RF kill. Airplane mode for Chrome* OS is achieved by TBD.

The W_DISABLE2# input signal ((Pin #54 on M.2 2230 module, Pin #63 on M.2 1216 module) allows the hardware to disable the BT RF circuitry.

The W_DISABLE2# signal is an active low signal. When driven low by the platform, this signal disables BT radio operation. The assertion and de-assertion of the W_DISABLE2# signal is asynchronous to any platform clock. All transients resulting from mechanical switches need to be de-bounced by platform circuitry.

Asserting W_DISABLE#_2 signal will result in a complete shutdown of the Bluetooth part. From the user perspective, the experience is like removing the Bluetooth device from the laptop.

The platform designer is required to assure that W_DISABLE2# is in a deterministic state (asserted or de-asserted) whenever power is applied to the card (for example, whenever +3.3 V is present).

If the customer does not intend to use this signal, Intel recommends leaving this pin unconnected.

Table 3-7   W_DISABLE2# characteristics

Characteristic	Description
Minimum Sink Current to ground	<1 mA (typical: 50 uA)
Internal pull up resistor	>130 kOhm
VIL for Asserting	0.0 V [+/− 0.3 V]
VIH for De-asserting	3.3 V [+/− 0.15 V] or float (not connected)

StP SD also supports Bluetooth SW RF Kill. The behavior of the BT SW RF Kill is similar to the BT HW RF Kill: all RF activities are terminated, LED is turned off and device goes into low power mode.

The BT radio will be active only if both HW RF kill pin and SW RF kill mechanism are in *enable* state.

For more information on the W_DISABLE2# pin, please refer to *PCI Express M.2 Specification* document Section 3.1.11.3.

Note: For the 1216SD 1.8 V module, this GPIO is a 1.8 V GPIO.

3.5.6 PCIe* interface

This host interface supports PCIe version 2.1 features.

The product supports the PCIe interface as defined in the *PCI Express M.2 Specification* document Sections 3.1.1 and 3.1.2. The section below add information specific to StP SD implementation.

3.5.6.1 PERST# rise time timing

The PERST# signal rise time needs to meet the below limitations. This guarantees robust out-of-reset flow of the – device and better immunity to Noise that can be carried by this signal. In addition, it is required that this signal rise in a monotonic way and avoid a stair-like rise.

Table 3-8 PERST# rise time

PERST# rise time	
PERST# rise time	<20 nSec montonic rise

Note: For Practical Platform design guideline needs: The 20 nSec reqirement is the solution for a robust design, but it leads to usage of an active-level-shifter on some Atom-based platforms (with 1.8 V IOs), which has cost impact. The platform designer may consider using a passive-level-shifter, which would typically create a higher rise time (about 150-300 nSec). This has a potential risk, but if the power supply/rails are clean enough and don't create noise on the PERST signal during this long rise time, the platform designer may decide to take the risk. In such designs it is recommended to keep a placeholder for an active-level-shifter as a mitigation.

3.5.6.2 Squelch detect mechanism – implementation note

The Squelch (SQ) Detect mechanism in StP SD may not consistently identify PCH *wake* signaling (TS1 symbols) as valid above SQ Max threshold of 175 mV, as defined by PCIe spec.

It is important to follow proper platform design and layout guidelines as defined in the PCIe CEM specification to ensure PCH wake signaling (Electrical Idle Detect Threshold – `Vrx-idle-det-diff-p-p` parameter) according to Table 3-9.

Table 3-9 Squelch (SQ) detect mechanism idle detect threshold

Parameter	Min (mV)	Max (mV)
Vrx-idle-det-diff-p-p	65	220

Customer should design/plan appropriately for all adapters that may be used in a given platform.

3.5.6.3 Voltage maximum values – clarification

Maximum PCIe DC voltage should be 3.465 V, as specified in the PCIe specification, and maximum spike should not exceed 5.4 V, as specified in JEDEC spec JESD78.

Note: For the 1216SD 1.8 V module, this GPIO is a 1.8 V GPIO.

3.5.6.4 Common clock configuration – clarification

PCIe on both platform side (PCH) and WLAN NIC side must operate using common clock configuration. Both PCH and WLAN NIC are configured for this by default (bit 6 is set in registers 0x50 and 0xF0). From hardware perspective, the same reference clock (REFCLK) must be used for both PCH and Wi-Fi card.

Figure 3-2   Common clock configuration
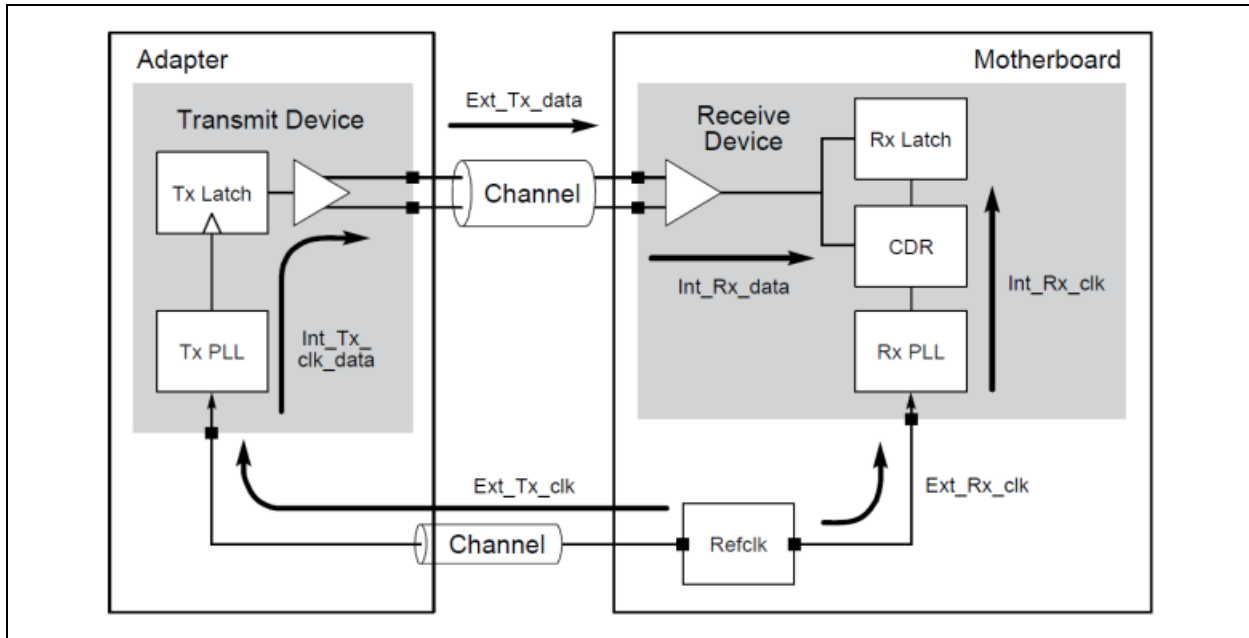
Source: *PCI Express Rev 2.0* spec (PCI_Express_Base_Rev_2.0_20Dec06a, figure 4-50)

3.5.7   USB interface

The product supports the USB interface as defined in the *PCI Express M.2 Specification* document Section 3.1.4. The section below adds information specific to StP SD implementation.

Table 3-10   USB interface signal description

Feature	Description
USB Version	2.0
USB Operational Mode	FS (Full Speed)
Bus Power	Defined as Self Powered (Powered from Module power feed)
Suspend Support	Yes. According to the USB 2.0 spec, the host may set the interface into suspend mode, allowing the device to save power by switching to low power mode. The D+ signal is kept as logical 1 value by an internal pull-up.

3.5.8   CLINK interface

The CLINK signals are specific for Intel® AMT based platforms. For those platforms that do not support AMT, the CLINK interface MUST NOT be used, and the CLINK pins should be kept disconnected on the platform level.

For more details on the CLINK interface, please refer to *CLINK Interface Specifications*.

3.5.9   LED indicators

StP2 SD products supports two LED indications: A Bluetooth LED, and a Wi-Fi LED.

The Bluetooth LED functionality is described in Table 3-11, while the Wi-Fi LED is described in Table 3-12.

Table 3-11   Bluetooth LED functionality

LED state	Device state
LED Off	No Power, HW RF Kill, SW RF Kill, Driver disable
LED On	Otherwise

Table 3-12   Wi-Fi LED functionality

LED state	Device state
LED Off	No Power, HW RF Kill, SW RF Kill, Driver disable
LED On	Otherwise

Note: **For StP-C:** In Stone Peak C-Step, the LED output pins (for both Wi-Fi and Bluetooth) are not open drain pins when using software v17.0.3 and earlier.With later versions software Stone Peak C-Step is open drain. When LEDs are not open drain, It is not allowed to Wire-Or the two LED pins and connect them to a single LED without glue logic. Maple Peak (WiGig) uses Stone Peak D-Step only.

Note: **For StP-D:** Stone Peak D-Step LEDs output are open drain regardless of software version used.

Note: Platforms that do not use LEDs can remove the LEDs and keep the LED GPIOs unconnected. When using StP-C step, in some cases, the device power consumption might increase when the LEDs GPIOs are not connected. Therefore, It is advisable, that instead of removing the LEDs, the customer shall replace them with a 100 kOhm pull-up resistor. This is in order to maintain stable power consumption in states in which the LED is turned off.

3.5.10   SUSCLK (32 KHz)

StP1 and StP22 do not use the external 32 KHz SUSCLK signal. The low-power modes of the StP device use the StP internal low-power XTAL.

3.5.11   Recommendation for installing No BT SKUs

For SKUs without BT, follow the guidelines in Table 3-13.

Table 3-13   Wi-Fi LED functionality

2230 Pin # (1216 Pin #)	Function	Recommendation
16 (64)	LED2#	NC
54 (63)	W_DISABLE2#	Connect to GND
3 (69)	USB_D-	NC
5 (70)	USB_D+	NC

3.6   Power states support

3.6.1   ACPI device state support

The modules are implemented according to the ACPI v3.0 Specification, supporting the peripheral power states D0 and D3 as listed in Table 3-14.

D3 hot means D3 with PERST# high (de-asserted) and power on.

D3 cold means D3 with PERST# low (asserted) and auxiliary power on.

StP modules support both D3 cold and D3 hot, the specific platform the adapter is used in may have limitations or recommendations. Please consult the applicable platform design guide. From a StP module perspective there is no difference in power consumption whether in D3 cold or D3 hot. In the absence of a platform recommendation, recommendation is to implement D3 hot.

Table 3-14   Supported D-states

Device Power States	Description
D0 (Uninitiated and Active)	Supported
D3 (hot and cold)	Supported for PCIe

3.6.2   Support of deep Sx

StP modules support Deep Sx, the specific platform the adapter is used in may have limitations or recommendations. Please consult the applicable platform design guide. From a StP module perspective there is no difference in power consumption whether in Deep Sx or not in Deep Sx. In the absence of a platform recommendation, recommendation is to not implement Deep Sx.

3.6.3   Enabling ethernet controllers with ASPM

ASPM defines the L states of the PCIe connections, L0, L0s, L1 and L2; among all those states, L0s has very low power saving vs. high complexity and risk. As a result the StP w/Bluetooth hardware devices shall not support PCI Express* ASPM L0s power state, and shall support the L1 state that has high value as a power saving state.

StP supports ASPM optionality ECN, allowing support of L1 without L0s. No special BIOS actions are required.

3.6.4   Intel® Power Optimizer

The Intel® Power Optimizer is a power management framework that allows for usage of deep, long latency platform power management states through new bus extensions.

Table 3-15   Stone Peak 2 family Intel® Power Optimizer capability

Family	Technology	Form factor	Interface	LTR	RTD3[1]	L1 states (L1.1, L1.2)
7265.NGWG	2×2 AC + BT	M.2	PCIe/USB	Yes	Yes	Yes
7265.NGWANG	2×2 AGN + BT	M.2	PCIe/USB	Yes	Yes	Yes
7265.NGWNBG	2×2 AGN (No BT)	M.2	PCIe	Yes	Yes	Yes
7265.NGWBNG	2×2 BGN + BT	M.2	PCIe/USB	Yes	Yes	Yes
3165.NGWG	1x1 AC + BT	M.2	PCIe/USB	Yes	Yes	Yes

NOTES: 1. Connected standby systems only.

Note: PCIe L1 states and LTR are supported by the NIC but also require platform support and BIOS enablement. For Linux based OSes, check what is supported by specific OS/Platform combination. For HSW-ULT L1 off is supported, and most likely LTR.

Note: For connected standby systems, the native PCI Express mode must be enabled in BIOS

3.6.5 T_power_on_scale value in L1 PM substates control 2 register

Current implementation in StP supports only the value of 00 in the T_power_on_scale field (bits 1:0). Other settings are not supported.

Details: According to the PCIe standard, the *L1 PM Substates Control 2 Register* (Offset 0Ch) can accept several scale range values. Stone Peak supports only the default value of 00b which indicates range of 2 uSec.

Impact: Most of the customers take the Intel reference design, which is set by default to 00b in this field, so no impact. Other customers need to make sure they set the value to 00b.

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4 Thermal Specifications

4.1.1 Thermal power dissipation

Max thermal power dissipation is based on the assumption that both Wi-Fi and Bluetooth communication are active. Table 4-1 describes the thermal dissipation and the targets per operated mode.

Table 4-1   Stone Peak1/2 thermal power dissipation

Name	Value (mW)	Description
StP2 TDP Limit Functional targets	1750	The worst case TDP shall be based on average power consumption measurement over 5 minutes with max TCP/IP throughput activity.
StP1 TDP Limit Functional targets	1200	The worst case TDP shall be based on average power consumption measurement over 5 minutes with max TCP/IP throughput activity.

Note: Functional modes include all product operation scenarios that can be accessed, using end users distribution software (artificial scenarios that may only be exercised using lab or OEM support software tools are not included).

4.2 Thermal management

4.2.1 Critical shutdown

The device thermal management will cut off RF operation once a maximum temperature (Critical Temperature CT-Kill) threshold has been reached. After cutoff point has been reached, the RF remains at the off position until it cools down to the thermal activation threshold. While in RF cut off state, the host cannot set the RF back to on.

4.2.2 Wi-Fi thermal throttling

When StP SD is heating up and reaching close to CT Kill, StP SD will start throttling its operation in order to prevent the unit from heating further and reaching critical temperature.

During throttling, StP SD performance might be degraded gradually (connectivity will be maintained).

See Table 4-2 for more information on the StP SD thermal management thresholds.

Table 4-2   Thermal management

Name	Value (°C)	Description
Thermal Shield for full Performance targets	80	Testing conditions: System environmental conditions: **High limit:** ~50 °C under controlled environment (oven), with no air flow (inside a box). **Low limit:** 0 °C (starting point) under controlled environment (oven), with no air flow (inside a box).
Thermal Silicon protection	85	Thermal silicon protection will be activated when StP SD reached 85 °C T-shield temperature.

4.2.3 Thermal NIC placement recommendations

The StP module dissipates heat through three main mechanisms:

- The RF shield cover;
- The metallized mounting screw that grounds the PCB to the chassis (for 2230 form factor only);
- The GND pads soldered to the PCB (for 1216 form factor only).

Correct NIC placement will ensure optimal thermal performance. The customer should make sure that the installation of the StP module is according to the following guidelines (For more information, see the *M.2 Specification* document Section 6.5):

- Recommended: Module orientation should be shield up
- M.2 module connection to chassis should be using an appropriate metal screw (2230 only)

4.2.4 CTDP requirements (TBD)

TBD

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5 Module Power Consumption

5.1 Module-level power consumption

5.1.1 Power consumption definitions

Module power consumption: 3.3 V rail power consumption.

Note: Power consumption numbers define the total consumed power from the 3.3 V rail

- Unless stated otherwise, power consumption refers to the highest average-power consumption value over any 1-second period.
- Meter: measured using current probe loop on the power rails of the module
- PCI-e ASPM (L1) and L1 sub states are enabled. (Note that L0s is not used.)

Idle state assumes no scans. Scans will add ~15 mW to power consumption.

- Transmit output power is assumed to be 15 dBm (32 mW).
- Platform is running on battery and power index is set to max power save (battery life.)

Table 5-1   M.2 power consumption (mW) targets

Test	Benchmark	Description	StP2 2230 and 1216 – max power [mW] Wi-Fi + Bluetooth	StP1 – max power [mW] Wi-Fi + Bluetooth
1	Comms HW disabled HW RF kill	All of the wireless devices on this card are disabled by HW RF-Kill.	< 2.5 (3.5 for 1216SD 1.8 V)	2.5
2	Comms SW disabled SW RF kill	All of the wireless devices on this card are disabled by SW RF-Kill. (PCI at L1 Off / L2, USB at L2)	< 2.5 (3.5 for 1216SD 1.8 V)	2.5
3	Connected standby logo tests	Wi-Fi is in connected standby (D0i3), low band, with no scan. Bluetooth core not paired (Windows OOB).	<3.5 (4.5 for 1216SD 1.8V)	3.5
4	Windows idle associated, low band	Wi-Fi is idle associated in low band. BT is running active A2DP profile (linked to stereo headset) but with no traffic.	7 (8 for 1216SD 1.8V)	7
5	Skype* video conferencing	Wi-Fi is running Skype conference (2 people, SISO LB 20 MHz, 1.5 Mbps full duplex.) Bluetooth paired with HFP (audio eSCO S2/S3.)	120	120
6	Video streaming (LB)	Wi-Fi is running unidirectional Rx, 720/1080p at 30 fps (8 mbps) on low band. Bluetooth paired with A2DP at 345 kbps.	400	400
7	WiDi DCM scenario	Laptop is streaming WiDi content (max resolution) – 12 Mbps.	400	NA

Test	Benchmark	Description	StP2 2230 and 1216 – max power [mW] Wi-Fi + Bluetooth	StP1 – max power [mW] Wi-Fi + Bluetooth
		Wi-Fi BSS client on LB, WiDi on HB (40 MHz channel.) Bluetooth is connected to a mouse (HID)		
8	Comms excursion (modeled)	Wi-Fi: 802.11n link at 200 mbps, FTP transmitting 90% and FTP receiving 10%. Bluetooth: A2DP, 375 Kbps (Tx).	<1580	1200

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6   Bluetooth RX/TX Sensitivity

The values in this section are the Bluetooth Rx sensitivity levels specified at the product antenna port for nominal temperature, voltage, and process.

The values refer to non-spur channels and do not include channels falling on reference clock (40MHz) harmonics.

The values are applicable to both 2230 and 1216 form factors.

While measurements are being performed, all co-located cores must be disabled or BT sensitivity will be degraded. Measurements were done in a screen room.

Table 6-1   Bluetooth sensitivity levels

Bluetooth Receiver Sensitivity	Typical (dbm)
BR RX Sensitivity	-90.5
EDR2 RX Sensitivity	-89.5
EDR3 RX Sensitivity	-83.0
BLE RX Sensitivity	-91.0

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7   Bluetooth TX Power

The requirements in this section apply to the Bluetooth output power at the antenna port of the product.

In the table below, Tx power levels are across channels. Values apply to the average of a representative quantity of samples at nominal temperature, voltage, and process.

Product maximum output power (EIRP) is limited by regulatory requirements, BT SIG requirements, and the actual implementation of the product's RF front-end and platform limitations: cable-loss, antenna-gain, trace loss, antenna mismatch.

Table 7-1   Bluetooth TX power

Bluetooth Transmit Power	Typical (dbm, +/-1.5dB)	
	2230	1216
BR TX Power	5.3	4.7
EDR2 TX Power	1.3	-1.1
EDR3 TX Power	1.2	-2.0
BLE TX Power	3.2	2.8

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8 Bluetooth Throughput Targets

This section details the throughput at a given attenuation for the given profile.

The values are applicable to both 2230 and 1216 form factors.

- OPP throughput testing occurs in fully conductive environment.
- BTOE is a Broadcom 2070 card in an Intel NUC.
- Throughput is tested at every 3 dB of attenuation starting at 25 dB and running until the devices can no longer connect at ~90 dB.
- Size of the file transferred is 3 MB and is tested three (3) times at each point.
- Wi-Fi and other cores are disabled. Bluetooth is connectable, not discoverable.

Table 8-1   Bluetooth throughput targets

Test Type	Attenuation	Typical TPT
TX OPP	25db	1425kbs
TX OPP	28db	1425kbs
TX OPP	31db	1425kbs
TX OPP	34db	1425kbs
TX OPP	37db	1425kbs
TX OPP	40db	1425kbs
TX OPP	43db	1425kbs
TX OPP	46db	1425kbs
TX OPP	49db	1425kbs
TX OPP	52db	1425kbs
TX OPP	55db	1425kbs
TX OPP	58db	1425kbs
TX OPP	61db	1425kbs
TX OPP	64db	1425kbs
TX OPP	67db	1375kbs
TX OPP	70db	1375kbs
TX OPP	73db	1375kbs
TX OPP	76db	950kbs
TX OPP	79db	750kbs
TX OPP	82db	500kbs
TX OPP	85db	0kbs
TX OPP	88db	0kbs
TX OPP	91db	0kbs
TX OPP	93db	0kbs
RX OPP	25db	1425kbs
RX OPP	28db	1425kbs
RX OPP	31db	1425kbs

Test Type	Attenuation	Typical TPT
RX OPP	34db	1425kbs
RX OPP	37db	1425kbs
RX OPP	40db	1425kbs
RX OPP	43db	1425kbs
RX OPP	46db	1425kbs
RX OPP	49db	1425kbs
RX OPP	52db	1425kbs
RX OPP	55db	1425kbs
RX OPP	58db	1425kbs
RX OPP	61db	1425kbs
RX OPP	64db	1425kbs
RX OPP	67db	1375kbs
RX OPP	70db	1375kbs
RX OPP	73db	1375kbs
RX OPP	75db	1375kbs
RX OPP	76db	950kbs
RX OPP	79db	750kbs
RX OPP	82db	500kbs
RX OPP	85db	0
RX OPP	87db	0
RX OPP	91db	0
RX OPP	93db	0

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9 Wi-Fi Sensitivity Targets

9.1 Wi-Fi sensitivity table

- Typical material at room temperature.
- Resolution is 0.5 dB (inaccuracy of up to +−0.25 dB).
- Numbers refer to AVG over all channels. LB variance is +−0.25 dB, HB variance is +−1 dB.

Table 9-1   Wi-Fi sensitivity table – StP2 2230/1216 and StP1

Name	Target
RX – Sensitivity | LB | Chain A | 1 | 20 MHz – dBm (Max)	−96.0
RX – Sensitivity | LB | Chain B | 1 | 20 MHz – dBm (Max)	−94.0
RX – Sensitivity | LB | Chain A | 11 | 20 MHz – dBm (Max)	−88.5
RX – Sensitivity | LB | Chain B | 11 | 20 MHz – dBm (Max)	−87.0
RX – Sensitivity | LB | Chain A | 6 | 20 MHz – dBm (Max)	-93.5
RX – Sensitivity | LB | Chain B | 6 | 20 MHz – dBm (Max)	−92.0
RX – Sensitivity | LB | Chain A | 54 | 20 MHz – dBm (Max)	−75.5
RX – Sensitivity | LB | Chain B | 54 | 20 MHz – dBm (Max)	−74.0
RX – Sensitivity | LB | Chain A | HT0 | 40 MHz-wide – dBm (Max)	−90.0
RX – Sensitivity | LB | Chain B | HT0 | 40 MHz-wide – dBm (Max)	−88.5
RX – Sensitivity | LB | Chain A | HT7 | 40 MHz-wide – dBm (Max)	−70.5
RX – Sensitivity | LB | Chain B | HT7 | 40 MHz-wide – dBm (Max)	−69.5
RX – Sensitivity | LB | MIMO | HT15 | 40 MHz-wide – dBm (Max)	−69.5
RX – Sensitivity | HB | Chain A | 6 | 20 MHz – dBm (Max)	−91.5
RX – Sensitivity | HB | Chain B | 6 | 20 MHz – dBm (Max)	−91.0
RX – Sensitivity | HB | Chain A | 54 | 20 MHz – dBm (Max)	−73.5
RX – Sensitivity | HB | Chain B | 54 | 20 MHz – dBm (Max)	−73.5
RX – Sensitivity | HB | Chain A | HT0 | 40 MHz-wide – dBm (Max)	−88.5
RX – Sensitivity | HB | Chain B | HT0 | 40 MHz-wide – dBm (Max)	−88.0
RX – Sensitivity | HB | Chain A | HT7 | 40 MHz-wide – dBm (Max)	−68.5
RX – Sensitivity | HB | Chain B | HT7 | 40 MHz-wide – dBm (Max)	−68.5
RX – Sensitivity | HB | MIMO | HT15 | 40 MHz-wide – dBm (Max)	−67.5
RX – Sensitivity | HB | Chain A | VHT0 | 80 MHz-wide – dBm (Max)	−85.0
RX – Sensitivity | HB | Chain B | VHT0 | 80 MHz-wide – dBm (Max)	−84.5
RX – Sensitivity | HB | MIMO | VHT0 | 80 MHz-wide – dBm (Max)	−84.5
RX – Sensitivity | HB | Chain A | VHT8 | 80 MHz-wide – dBm (Max)	−61.5
RX – Sensitivity | HB | Chain B | VHT8 | 80 MHz-wide – dBm (Max)	−61.5
RX – Sensitivity | HB | MIMO | VHT8 | 80 MHz-wide – dBm (Max)	−61.0
RX – Sensitivity | HB | Chain A | VHT9 | 80 MHz-wide – dBm (Max)	−59.5

Name	Target
RX – Sensitivity | HB | Chain B | VHT9 | 80 MHz-wide – dBm (Max)	−59.0
RX – Sensitivity | HB | MIMO | VHT9 | 80 MHz-wide – dBm (Max)	−59.0

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10 Wi-Fi Throughput Targets

Table 10-1 Conductive without AMPDU

Conductive, best attenuation, BE, UDP								
			RX			**TX**		
Protocol	**Band**	**Channel**	**Target**	**Min**		**Target**	**Min**	**Units**
11n	LB	20 MHz	129	125		130	125	mbps
11n	HB	40 MHz	261	251		266	256	mbps
11ac	HB	80 MHz	631	600		672	647	mbps

Table 10-2 Conductive with AMPDU

Conductive, best attenuation, BE, TCP								
			RX			**TX**		
Protocol	**Band**	**Channel**	**Target**	**Min**		**Target**	**Min**	**Units**
11b	LB	20 MHz	5.5	5.4		5.5	5.4	mbps
11g	LB	20 MHz	22.6	21.8		22.6	21.8	mbps
11a	HB	20 MHz	22.9	22.2		22.9	22.2	mbps
11n	LB	20 MHz	127	122		111	107	mbps
11n	HB	40 MHz	253	243		230	221	mbps
11ac	HB	80 MHz	589	558		529	507	mbps

Table 10-3 OTA performance targets

Scott Church House, consumer environment, NLOS OTA, AMPDU disabled						
Protocol	**Band**	**Channel**	**Station**	**RX**	**TX**	**Units**
11n	LB	20 MHz	SCH1 L0	TBD	TBD	Mbps
			SCH1 L1	TBD	TBD	Mbps
			SCH1 L2	TBD	TBD	Mbps
			SCH1 L3	TBD	TBD	Mbps
11n	HB	40 MHz	SCH1 L0	TBD	TBD	Mbps
			SCH1 L1	TBD	TBD	Mbps
			SCH1 L2	TBD	TBD	Mbps
			SCH1 L3	TBD	TBD	Mbps
11ac	HB	80 MHz	SCH1 L0	TBD	TBD	Mbps
			SCH1 L1	TBD	TBD	Mbps
			SCH1 L2	TBD	TBD	Mbps
			SCH1 L3	TBD	TBD	Mbps

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11 Regulatory

11.1 Regulatory channel support and output power

Stone Peak provides regulatory compliance via statically configured SKUs or DRS (Dynamic Regulatory Solution). Static configurations are covered in this document. DRS is covered by the document: *Wi-Fi Dynamic Regulatory Solution (DRS) for Stone Peak* – CDI # 554827.

11.2 Wi-Fi channel configuration

11.2.1 Channel configuration tables

Figure 11-1   Scan details
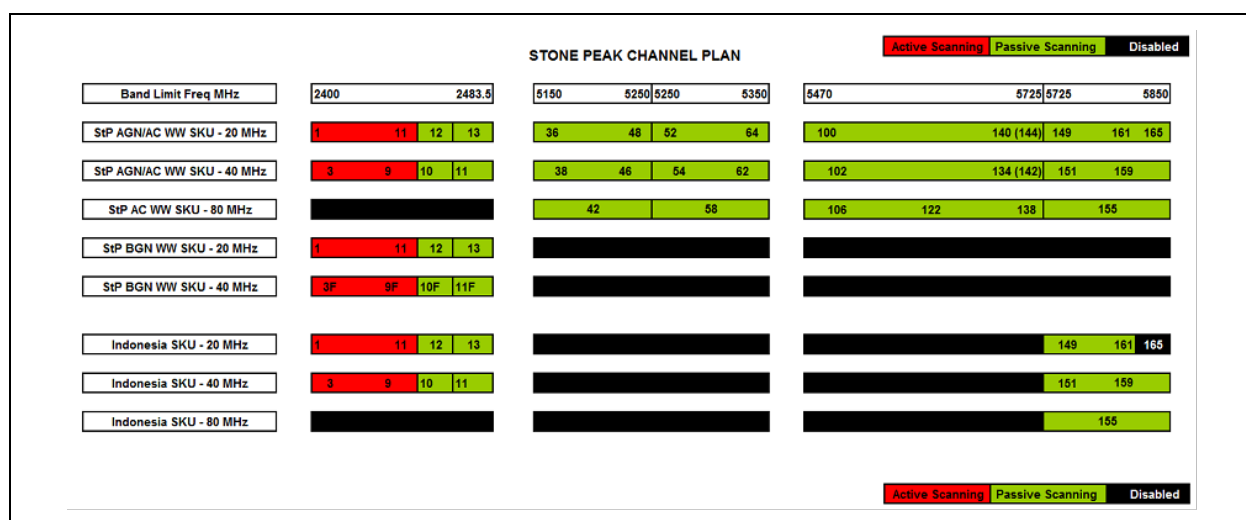
11.2.2 Output power restrictions (main geos)

Figure 11-2   Output power restrictions, main geographies

Country/Geo	2.4GHz	5.15 - 5.25GHz	5.25 - 5.35GHz	5.47 - 5.725GHz	5.725 - 5.85GHz	Output Power Spectral Density
Canada	1W **	50mW **	250mW **	250mW **	1W **	Output Power
Canada	8dBm/3kHz **	4dBm/MHz **	11dBm/MHz **	11dBm/MHz **	8dBm/3kHz **	Spectral Density
EU Countries	100mW EIRP	200mW EIRP	200mW EIRP	1W EIRP	N/A	Output Power
EU Countries	10dBm/MHz EIRP	10dBm/MHz EIRP	10dBm/MHz EIRP	17dBm/MHz EIRP	N/A	Spectral Density
Japan	12.14dBm/MHzEIRP	10dBm/MHz EIRP	10dBm/MHz EIRP	14dBm/MHz EIRP	N/A	Spectral Density
S. Korea *	10dBm/MHz ** No averaging	4dBm/MHz ** No Averaging	10dBm/MHz ** No Averaging	10dBm/MHz ** No Averaging 5.65 - 5.725GHz Not Allowed	10dBm/MHz ** No Averaging Channel 165 -5.825GHz Not Allowed	Spectral Density
United States	1W **	50mW **	250mW **	250mW **	1W **	Output Power
United States	8dBm/3kHz **	4dBm/MHz **	11dBm/MHz **	11dBm/MHz **	8dBm/3kHz **	Spectral Density
** Allowance of up to a 6dBi antenna allowed, if antenna is > 6dBi output power must be reduced by 1dB per dBi of antenna gain						
* Levels valid for 20 MHz channels. To be divided by 2 (reduce 3dB) for 40 MHz channels.						

NOTE: Reference antenna gain: Max. Antenna Gain 3 dBi for 2.4 GHz and 5 dBi for 5 GHz

11.2.3 Channel configuration tables/RF output power

The values listed in the power table (EEPROM table) represent the target power for the calibration process without antennae gain. This value has been verified to ensure margin from the regulatory limit based on post EEPROM factory calibration measurements using a diagnostic tool that operates the WLAN card at a ~99% DC (Duty Cycle) taken on both the main and auxiliary antenna ports.

As part of the factory test process, Intel measures the output power of every card. Any cards that exceed the maximum limits (EEPROM + 1.25 dB) will not pass the factory test. While in operation the card adjusts TX power using a closed loop TX power calibration algorithm.

Intel uses the following assumption for the antennae gain value and country certification work: 3 dbi for 2.4 GHz and 5 dBi for 5 GHz.

Intel also incorporates a lower limit to ensure that compliance of the WLAN card is maintained. The minimum limits are set by factory process. In MIMO mode this value is the sum limit. Generally if sum = 15 then Tx1 limit = 12 dBm and Tx2 limit = 12 dBm (exception for some channels according to the table below.)

StP1 and StP2 2230

Notes:

- StP1 supports all SISO rates – legacy, HT0-HT7 and VHT0-VHT9 SISO. It does not support MIMO rates – HT8-HT15 and VHT0-VHT9 MIMO.
- StP1 and StP2 D-step support the Dynamic Regulatory Solution (DRS) feature. For TX power tables and details see CDI document #554827 Intel Wireless Dynamic Regulatory Solution Application Note.
- The tables below list the Tx power in three cases: default Tx power (before detecting of the user location), and FCC and ROW (become active when user location is obtained).

Table 11-1   Stone Peak 1 and 2 default M.2 2230, CCK mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
1	2.412	Y	Y	Y	N	N	14.5	14.5
2	2.417	Y	Y	Y	N	N	14.5	14.5
3	2.422	Y	Y	Y	N	N	14.5	14.5
4	2.427	Y	Y	Y	N	N	14.5	14.5
5	2.432	Y	Y	Y	N	N	14.5	14.5
6	2.437	Y	Y	Y	N	N	14.5	14.5
7	2.442	Y	Y	Y	N	N	14.5	14.5
8	2.447	Y	Y	Y	N	N	14.5	14.5
9	2.452	Y	Y	Y	N	N	14.5	14.5
10	2.457	Y	Y	Y	N	N	14.5	14.5
11	2.462	Y	Y	Y	N	N	14.5	14.5
12	2.467	N	N	Y	N	N	14.5	14.5
13	2.472	N	N	Y	N	N	14.5	14.5
	NOTES: Prior to production phase the Tx power setting is not set accurately.							

Table 11-2   Stone Peak 1 and 2 default M.2 2230, OFDM mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
1	2.412	Y	Y	Y	N	N	12.5	13	10.5
2	2.417	Y	Y	Y	N	N	14	14	12
3	2.422	Y	Y	Y	N	N	15	15	12
4	2.427	Y	Y	Y	N	N	15	15	12
5	2.432	Y	Y	Y	N	N	15	15	12
6	2.437	Y	Y	Y	N	N	15	15	12
7	2.442	Y	Y	Y	N	N	15	15	12
8	2.447	Y	Y	Y	N	N	15	15	12
9	2.452	Y	Y	Y	N	N	15	15	12
10	2.457	Y	Y	Y	N	N	14	14	12
11	2.462	Y	Y	Y	N	N	11	11	10.5
12	2.467	N	N	Y	N	N	15	15	12
13	2.472	N	N	Y	N	N	15	15	12
36	5.180	N	N	Y	N	Y	12.5	12.5	10
40	5.200	N	N	Y	N	Y	13.5	13.5	10
44	5.220	N	N	Y	N	Y	13.5	13.5	10
48	5.240	N	N	Y	N	Y	13.5	13.5	10
52	5.260	N	N	N	Y	N	14.5	14.5	11,5
56	5.280	N	N	N	Y	N	14.5	14.5	11,5
60	5.300	N	N	N	Y	N	14.5	14.5	11,5
64	5.320	N	N	N	Y	N	12	12	10
100	5.500	N	N	N	Y	N	12	12	9
104	5.520	N	N	N	Y	N	14.5	14.5	12
108	5.540	N	N	N	Y	N	14.5	14.5	12
112	5.560	N	N	N	Y	N	14.5	14.5	12
116	5.580	N	N	N	Y	N	14.5	14.5	12
120	5.600	N	N	N	Y	N	14.5	14.5	12
124	5.620	N	N	N	Y	N	14.5	14.5	12
128	5.640	N	N	N	Y	N	14.5	14.5	12
132	5.660	N	N	N	Y	N	14.5	14.5	12
136	5.680	N	N	N	Y	N	14.5	14.5	12

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
140	5.700	N	N	N	Y	N	11.5	11.5	9.5
144	5.720	N	N	N	Y	N	14.5	14	12
149	5.745	N	N	Y	N	Y	14.5	14	12
153	5.765	N	N	Y	N	Y	14.5	14	12
157	5.785	N	N	Y	N	Y	14.5	14	12
161	5.805	N	N	Y	N	Y	14.5	14	12
165	5.825	N	N	Y	N	Y	14.5	14	12
3n40	2.422	Y	Y	Y	N	N	12	12	8
4n40	2.427	Y	Y	Y	N	N	13	13	10
5n40	2.432	Y	Y	Y	N	N	14	14	10.5
6n40	2.437	Y	Y	Y	N	N	15	15	12
7n40	2.442	Y	Y	Y	N	N	13	12	11
8n40	2.447	Y	Y	Y	N	N	12	11	10
9n40	2.452	Y	Y	Y	N	N	11	10	8
10n40	2.457	N	N	Y	N	N	15	15	12
11n40	2.462	N	N	Y	N	N	15	15	12
38n40	5.190	N	N	Y	N	Y	10.5	12	8.5
46n40	5.230	N	N	Y	N	Y	14.5	14.5	11.5
54n40	5.270	N	N	N	Y	N	14.5	14.5	11.5
62n40	5.310	N	N	N	Y	N	12	12	10
102n40	5.510	N	N	N	Y	N	12	12.5	10
110n40	5.550	N	N	N	Y	N	14.5	14.5	12
118n40	5.590	N	N	N	Y	N	14.5	14.5	12
126n40	5.630	N	N	N	Y	N	14.5	14.5	12
134n40	5.670	N	N	N	Y	N	14.5	14.5	12
142n40	5.710	N	N	N	Y	N	15	15	12.5
151n40	5.755	N	N	Y	N	Y	15	15	12.5
159n40	5.795	N	N	Y	N	Y	15	15	12.5
42ac80	5.210	N	N	Y	N	N	12	12	10
58ac80	5.290	N	N	N	Y	N	12	12	10
106ac80	5.530	N	N	N	Y	N	12	12	10
122ac80	5.610	N	N	N	Y	N	13.5	13.5	12

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
138ac80	5.690	N	N	N	Y	N	15	15	12.5
155ac80	5.775	N	N	Y	N	Y	15	15	12.5

Table 11-3   Stone Peak 1 and 2 default M.2 1216, CCK mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
1	2.412	Y	Y	Y	N	N	14.5	14.5
2	2.417	Y	Y	Y	N	N	14.5	14.5
3	2.422	Y	Y	Y	N	N	14.5	14.5
4	2.427	Y	Y	Y	N	N	14.5	14.5
5	2.432	Y	Y	Y	N	N	14.5	14.5
6	2.437	Y	Y	Y	N	N	14.5	14.5
7	2.442	Y	Y	Y	N	N	14.5	14.5
8	2.447	Y	Y	Y	N	N	14.5	14.5
9	2.452	Y	Y	Y	N	N	14.5	14.5
10	2.457	Y	Y	Y	N	N	14.5	14.5
11	2.462	Y	Y	Y	N	N	14.5	14.5
12	2.467	N	N	Y	N	N	14.5	14.5
13	2.472	N	N	Y	N	N	14.5	14.5
	NOTES: Prior to production phase the Tx power setting is not set accurately.							

Table 11-4   Stone Peak 1 and 2 default M.2 1216, OFDM mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
1	2.412	Y	Y	Y	N	N	12.5	13	10.5
2	2.417	Y	Y	Y	N	N	14	14	12
3	2.422	Y	Y	Y	N	N	15	15	12
4	2.427	Y	Y	Y	N	N	15	15	12
5	2.432	Y	Y	Y	N	N	15	15	12
6	2.437	Y	Y	Y	N	N	15	15	12
7	2.442	Y	Y	Y	N	N	15	15	12
8	2.447	Y	Y	Y	N	N	15	15	12

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
9	2.452	Y	Y	Y	N	N	15	15	12
10	2.457	Y	Y	Y	N	N	14	14	12
11	2.462	Y	Y	Y	N	N	11	11	10.5
12	2.467	N	N	Y	N	N	15	15	12
13	2.472	N	N	Y	N	N	15	15	12
36	5.180	N	N	Y	N	Y	12.5	12.5	10
40	5.200	N	N	Y	N	Y	13.5	13.5	10
44	5.220	N	N	Y	N	Y	13.5	13.5	10
48	5.240	N	N	Y	N	Y	13.5	13.5	10
52	5.260	N	N	N	Y	N	14.5	14.5	11,5
56	5.280	N	N	N	Y	N	14.5	14.5	11,5
60	5.300	N	N	N	Y	N	14.5	14.5	11,5
64	5.320	N	N	N	Y	N	12	12	10
100	5.500	N	N	N	Y	N	12	12	9
104	5.520	N	N	N	Y	N	14.5	14.5	12
108	5.540	N	N	N	Y	N	14.5	14.5	12
112	5.560	N	N	N	Y	N	14.5	14.5	12
116	5.580	N	N	N	Y	N	14.5	14.5	12
120	5.600	N	N	N	Y	N	14.5	14.5	12
124	5.620	N	N	N	Y	N	14.5	14.5	12
128	5.640	N	N	N	Y	N	14.5	14.5	12
132	5.660	N	N	N	Y	N	14.5	14.5	12
136	5.680	N	N	N	Y	N	14.5	14.5	12
140	5.700	N	N	N	Y	N	11.5	11.5	9.5
144	5.720	N	N	N	Y	N	14.5	14	12
149	5.745	N	N	Y	N	Y	14.5	14	12
153	5.765	N	N	Y	N	Y	14.5	14	12
157	5.785	N	N	Y	N	Y	14.5	14	12
161	5.805	N	N	Y	N	Y	14.5	14	12
165	5.825	N	N	Y	N	Y	14.5	14	12
3n40	2.422	Y	Y	Y	N	N	12	12	8
4n40	2.427	Y	Y	Y	N	N	13	13	10.5

Regulatory

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
5n40	2.432	Y	Y	Y	N	N	14	14	11.5
6n40	2.437	Y	Y	Y	N	N	15	15	12
7n40	2.442	Y	Y	Y	N	N	13	12	11
8n40	2.447	Y	Y	Y	N	N	12	11	10
9n40	2.452	Y	Y	Y	N	N	11	10	8
10n40	2.457	N	N	Y	N	N	15	15	12
11n40	2.462	N	N	Y	N	N	15	15	12
38n40	5.190	N	N	Y	N	Y	10.5	12	8.5
46n40	5.230	N	N	Y	N	Y	15	15	12
54n40	5.270	N	N	N	Y	N	15	15	12
62n40	5.310	N	N	N	Y	N	12	12	10
102n40	5.510	N	N	N	Y	N	12	12.5	10
110n40	5.550	N	N	N	Y	N	15	15	12
118n40	5.590	N	N	N	Y	N	15	15	12
126n40	5.630	N	N	N	Y	N	15	15	12
134n40	5.670	N	N	N	Y	N	15	15	12
142n40	5.710	N	N	N	Y	N	15	15	12
151n40	5.755	N	N	Y	N	Y	15	15	12
159n40	5.795	N	N	Y	N	Y	15	15	12
42ac80	5.210	N	N	Y	N	N	12	12	10
58ac80	5.290	N	N	N	Y	N	12	12	10
106ac80	5.530	N	N	N	Y	N	12	12	10
122ac80	5.610	N	N	N	Y	N	15	15	12
138ac80	5.690	N	N	N	Y	N	15	15	12
155ac80	5.775	N	N	Y	N	Y	15	15	12

Table 11-5   Stone Peak 1 and 2 FCC M.2, CCK-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
1	2.412	Y	Y	Y	N	N	15	15
2	2.417	Y	Y	Y	N	N	16	16
3	2.422	Y	Y	Y	N	N	16	16

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
4	2.427	Y	Y	Y	N	N	16	16
5	2.432	Y	Y	Y	N	N	16	16
6	2.437	Y	Y	Y	N	N	16	16
7	2.442	Y	Y	Y	N	N	16	16
8	2.447	Y	Y	Y	N	N	16	16
9	2.452	Y	Y	Y	N	N	16	16
10	2.457	Y	Y	Y	N	N	16	16
11	2.462	Y	Y	Y	N	N	15	15
12	2.467	N	N	Y	N	N	10.5	12
13	2.472	N	N	Y	N	N	9.5	11
NOTES: Prior to production phase the Tx power setting is not set accurately.								

Table 11-6   Stone Peak 1 and 2 FCC M.2, OFDM-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
1	2.412	Y	Y	Y	N	N	12.5	13	10.5
2	2.417	Y	Y	Y	N	N	14	14	12
3	2.422	Y	Y	Y	N	N	16	16	16
4	2.427	Y	Y	Y	N	N	16	16	16
5	2.432	Y	Y	Y	N	N	16	16	16
6	2.437	Y	Y	Y	N	N	16	16	16
7	2.442	Y	Y	Y	N	N	16	16	16
8	2.447	Y	Y	Y	N	N	16	16	16
9	2.452	Y	Y	Y	N	N	16	16	16
10	2.457	Y	Y	Y	N	N	14	14	12
11	2.462	Y	Y	Y	N	N	11	11	10.5
12	2.467	N	N	Y	N	N	8.5	7.5	5.5
13	2.472	N	N	Y	N	N	0	0	0
36	5.180	N	N	Y	N	Y	12.5	12.5	10
40	5.200	N	N	Y	N	Y	13.5	13.5	10
44	5.220	N	N	Y	N	Y	13.5	13.5	10
48	5.240	N	N	Y	N	Y	13.5	13.5	10
52	5.260	N	N	N	Y	N	14.5	15	12

Regulatory

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
56	5.280	N	N	N	Y	N	14.5	15	12
60	5.300	N	N	N	Y	N	14.5	15	12
64	5.320	N	N	N	Y	N	12	12	10
100	5.500	N	N	N	Y	N	12	12	9
104	5.520	N	N	N	Y	N	14.5	15	13
108	5.540	N	N	N	Y	N	14.5	15	13
112	5.560	N	N	N	Y	N	14.5	15	13
116	5.580	N	N	N	Y	N	14.5	15	13
120	5.600	N	N	N	Y	N	14.5	15	13
124	5.620	N	N	N	Y	N	14.5	15	13
128	5.640	N	N	N	Y	N	14.5	15	13
132	5.660	N	N	N	Y	N	14.5	15	13
136	5.680	N	N	N	Y	N	14.5	15	13
140	5.700	N	N	N	Y	N	11.5	11.5	9.5
144	5.720	N	N	N	Y	N	14.5	14	12
149	5.745	N	N	Y	N	Y	14.5	14	12
153	5.765	N	N	Y	N	Y	14.5	14	12
157	5.785	N	N	Y	N	Y	14.5	14	12
161	5.805	N	N	Y	N	Y	14.5	14	12
165	5.825	N	N	Y	N	Y	14.5	14	12
3n40	2.422	Y	Y	Y	N	N	12	12	8
4n40	2.427	Y	Y	Y	N	N	13	13	10
5n40	2.432	Y	Y	Y	N	N	14	14	10.5
6n40	2.437	Y	Y	Y	N	N	15	15	12
7n40	2.442	Y	Y	Y	N	N	15	13	12
8n40	2.447	Y	Y	Y	N	N	14.5	12	10
9n40	2.452	Y	Y	Y	N	N	11	10	8
10n40	2.457	N	N	Y	N	N	9	8	6
11n40	2.462	N	N	Y	N	N	0	0	0
38n40	5.190	N	N	Y	N	Y	10.5	12	8.5
46n40	5.230	N	N	Y	N	Y	15	15	13
54n40	5.270	N	N	N	Y	N	15	15	15
62n40	5.310	N	N	N	Y	N	12	12	10
102n40	5.510	N	N	N	Y	N	12	12.5	10

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
110n40	5.550	N	N	N	Y	N	15	15	15
118n40	5.590	N	N	N	Y	N	15	15	15
126n40	5.630	N	N	N	Y	N	15	15	15
134n40	5.670	N	N	N	Y	N	15	15	15
142n40	5.710	N	N	N	Y	N	15	15	15
151n40	5.755	N	N	Y	N	Y	15	15	15
159n40	5.795	N	N	Y	N	Y	15	15	15
42ac80	5.210	N	N	Y	N	N	12	12	10
58ac80	5.290	N	N	N	Y	N	12	12	10
106ac80	5.530	N	N	N	Y	N	12	12	10
122ac80	5.610	N	N	N	Y	N	15	15	15
138ac80	5.690	N	N	N	Y	N	15	15	15
155ac80	5.775	N	N	Y	N	Y	15	15	15

Table 11-7   Stone Peak 1 and 2 FCC/SAR M.2, CCK-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
1	2.412	Y	Y	Y	N	N	13.5	13.5
2	2.417	Y	Y	Y	N	N	13.5	13.5
3	2.422	Y	Y	Y	N	N	13.5	13.5
4	2.427	Y	Y	Y	N	N	13.5	13.5
5	2.432	Y	Y	Y	N	N	13.5	13.5
6	2.437	Y	Y	Y	N	N	13.5	13.5
7	2.442	Y	Y	Y	N	N	13.5	13.5
8	2.447	Y	Y	Y	N	N	13.5	13.5
9	2.452	Y	Y	Y	N	N	13.5	13.5

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
10	2.457	Y	Y	Y	N	N	13.5	13.5
11	2.462	Y	Y	Y	N	N	13.5	13.5
12	2.467	N	N	Y	N	N	10.5	12
13	2.472	N	N	Y	N	N	9.5	11
	NOTES: Prior to production phase the Tx power setting is not set accurately.							

Table 11-8   Stone Peak 1 and 2 FCC/SAR M.2, OFDM-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spread-ing	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
1	2.412	Y	Y	Y	N	N	12.5	13	10.5
2	2.417	Y	Y	Y	N	N	13.5	13.5	12
3	2.422	Y	Y	Y	N	N	13.5	13.5	13.5
4	2.427	Y	Y	Y	N	N	13.5	13.5	13.5
5	2.432	Y	Y	Y	N	N	13.5	13.5	13.5
6	2.437	Y	Y	Y	N	N	13.5	13.5	13.5
7	2.442	Y	Y	Y	N	N	13.5	13.5	13.5
8	2.447	Y	Y	Y	N	N	13.5	13.5	13.5
9	2.452	Y	Y	Y	N	N	13.5	13.5	13.5
10	2.457	Y	Y	Y	N	N	13.5	13.5	12
11	2.462	Y	Y	Y	N	N	11	11	10.5
12	2.467	N	N	Y	N	N	8.5	7.5	5.5
13	2.472	N	N	Y	N	N	0	0	0
36	5.180	N	N	Y	N	Y	12	12	10
40	5.200	N	N	Y	N	Y	12	12	10
44	5.220	N	N	Y	N	Y	12	12	10
48	5.240	N	N	Y	N	Y	12	12	10
52	5.260	N	N	N	Y	N	12	12	12
56	5.280	N	N	N	Y	N	12	12	12
60	5.300	N	N	N	Y	N	12	12	12
64	5.320	N	N	N	Y	N	12	12	10
100	5.500	N	N	N	Y	N	12	12	9
104	5.520	N	N	N	Y	N	12	12	12
108	5.540	N	N	N	Y	N	12	12	12
112	5.560	N	N	N	Y	N	12	12	12

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spread-ing	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
116	5.580	N	N	N	Y	N	12	12	12
120	5.600	N	N	N	Y	N	12	12	12
124	5.620	N	N	N	Y	N	12	12	12
128	5.640	N	N	N	Y	N	12	12	12
132	5.660	N	N	N	Y	N	12	12	12
136	5.680	N	N	N	Y	N	12	12	12
140	5.700	N	N	N	Y	N	11.5	11.5	9.5
144	5.720	N	N	N	Y	N	12	12	12
149	5.745	N	N	Y	N	Y	12	12	12
153	5.765	N	N	Y	N	Y	12	12	12
157	5.785	N	N	Y	N	Y	12	12	12
161	5.805	N	N	Y	N	Y	12	12	12
165	5.825	N	N	Y	N	Y	12	12	12
3n40	2.422	Y	Y	Y	N	N	12	12	8
4n40	2.427	Y	Y	Y	N	N	13	13	10
5n40	2.432	Y	Y	Y	N	N	13.5	13.5	10.5
6n40	2.437	Y	Y	Y	N	N	13.5	13.5	12
7n40	2.442	Y	Y	Y	N	N	13.5	13	12
8n40	2.447	Y	Y	Y	N	N	13.5	12	10
9n40	2.452	Y	Y	Y	N	N	11	10	8
10n40	2.457	N	N	Y	N	N	9	8	6
11n40	2.462	N	N	Y	N	N	0	0	0
38n40	5.190	N	N	Y	N	Y	10.5	12	8.5
46n40	5.230	N	N	Y	N	Y	12	12	12
54n40	5.270	N	N	N	Y	N	12	12	12
62n40	5.310	N	N	N	Y	N	12	12	10
102n40	5.510	N	N	N	Y	N	12	12	10
110n40	5.550	N	N	N	Y	N	12	12	12
118n40	5.590	N	N	N	Y	N	12	12	12
126n40	5.630	N	N	N	Y	N	12	12	12
134n40	5.670	N	N	N	Y	N	12	12	12
142n40	5.710	N	N	N	Y	N	12	12	12
151n40	5.755	N	N	Y	N	Y	12	12	12
159n40	5.795	N	N	Y	N	Y	12	12	12
42ac80	5.210	N	N	Y	N	N	12	12	10

Regulatory

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spread-ing	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
58ac80	5.290	N	N	N	Y	N	12	12	10
106ac80	5.530	N	N	N	Y	N	12	12	10
122ac80	5.610	N	N	N	Y	N	12	12	12
138ac80	5.690	N	N	N	Y	N	12	12	12
155ac80	5.775	N	N	Y	N	Y	12	12	12

ROW SKU

Table 11-9   Stone Peak 1 and 2 ROW M.2, CCK-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
1	2.412	Y	Y	Y	N	N	14.5	14.5
2	2.417	Y	Y	Y	N	N	14.5	14.5
3	2.422	Y	Y	Y	N	N	14.5	14.5
4	2.427	Y	Y	Y	N	N	14.5	14.5
5	2.432	Y	Y	Y	N	N	14.5	14.5
6	2.437	Y	Y	Y	N	N	14.5	14.5
7	2.442	Y	Y	Y	N	N	14.5	14.5
8	2.447	Y	Y	Y	N	N	14.5	14.5
9	2.452	Y	Y	Y	N	N	14.5	14.5
10	2.457	Y	Y	Y	N	N	14.5	14.5
11	2.462	Y	Y	Y	N	N	14.5	14.5
12	2.467	N	N	Y	N	N	14.5	14.5
13	2.472	N	N	Y	N	N	14.5	14.5

NOTES: Prior to production phase the Tx power setting is not set accurately.

Table 11-10   Stone Peak 1 and 2 ROW M.2, OFDM-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
1	2.412	Y	Y	Y	N	N	15	15	12
2	2.417	Y	Y	Y	N	N	15	15	12
3	2.422	Y	Y	Y	N	N	15	15	12
4	2.427	Y	Y	Y	N	N	15	15	12
5	2.432	Y	Y	Y	N	N	15	15	12

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
6	2.437	Y	Y	Y	N	N	15	15	12
7	2.442	Y	Y	Y	N	N	15	15	12
8	2.447	Y	Y	Y	N	N	15	15	12
9	2.452	Y	Y	Y	N	N	15	15	12
10	2.457	Y	Y	Y	N	N	15	15	12
11	2.462	Y	Y	Y	N	N	15	15	12
12	2.467	N	N	Y	N	N	15	15	12
13	2.472	N	N	Y	N	N	15	15	12
36	5.180	N	N	Y	N	Y	14.5	14.5	11.5
40	5.200	N	N	Y	N	Y	14.5	14.5	11.5
44	5.220	N	N	Y	N	Y	14.5	14.5	11.5
48	5.240	N	N	Y	N	Y	14.5	14.5	11.5
52	5.260	N	N	N	Y	N	14.5	14.5	11.5
56	5.280	N	N	N	Y	N	14.5	14.5	11.5
60	5.300	N	N	N	Y	N	14.5	14.5	11.5
64	5.320	N	N	N	Y	N	14.5	14.5	11.5
100	5.500	N	N	N	Y	N	14.5	14.5	12
104	5.520	N	N	N	Y	N	14.5	14.5	12
108	5.540	N	N	N	Y	N	14.5	14.5	12
112	5.560	N	N	N	Y	N	14.5	14.5	12
116	5.580	N	N	N	Y	N	14.5	14.5	12
120	5.600	N	N	N	Y	N	14.5	14.5	12
124	5.620	N	N	N	Y	N	14.5	14.5	12
128	5.640	N	N	N	Y	N	14.5	14.5	12
132	5.660	N	N	N	Y	N	14.5	14.5	12
136	5.680	N	N	N	Y	N	14.5	14.5	12
140	5.700	N	N	N	Y	N	14.5	14.5	12
144	5.720	N	N	N	Y	N	15	15	12
149	5.745	N	N	Y	N	Y	15	15	12
153	5.765	N	N	Y	N	Y	15	15	12
157	5.785	N	N	Y	N	Y	15	15	12
161	5.805	N	N	Y	N	Y	15	15	12
165	5.825	N	N	Y	N	Y	15	15	12
3n40	2.422	Y	Y	Y	N	N	15	15	12
4n40	2.427	Y	Y	Y	N	N	15	15	12

Regulatory

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
5n40	2.432	Y	Y	Y	N	N	15	15	12
6n40	2.437	Y	Y	Y	N	N	15	15	12
7n40	2.442	Y	Y	Y	N	N	15	15	12
8n40	2.447	Y	Y	Y	N	N	15	15	12
9n40	2.452	Y	Y	Y	N	N	15	15	12
10n40	2.457	N	N	Y	N	N	15	15	12
11n40	2.462	N	N	Y	N	N	15	15	12
38n40	5.190	N	N	Y	N	Y	13.5	13.5	11.5
46n40	5.230	N	N	Y	N	Y	14.5	14.5	11.5
54n40	5.270	N	N	N	Y	N	14.5	14.5	11.5
62n40	5.310	N	N	N	Y	N	14.5	14.5	11.5
102n40	5.510	N	N	N	Y	N	14.5	14.5	12
110n40	5.550	N	N	N	Y	N	14.5	14.5	12
118n40	5.590	N	N	N	Y	N	14.5	14.5	12
126n40	5.630	N	N	N	Y	N	14.5	14.5	12
134n40	5.670	N	N	N	Y	N	14.5	14.5	12
142n40	5.710	N	N	N	Y	N	15.5	15.5	12.5
151n40	5.755	N	N	Y	N	Y	15.5	15.5	12.5
159n40	5.795	N	N	Y	N	Y	15.5	15.5	12.5
42ac80	5.210	N	N	Y	N	N	13	13	10.5
58ac80	5.290	N	N	N	Y	N	13	13	10.5
106ac80	5.530	N	N	N	Y	N	12.5	12.5	11.5
122ac80	5.610	N	N	N	Y	N	13.5	13.5	12
138ac80	5.690	N	N	N	Y	N	15.5	15.5	12.5
155ac80	5.775	N	N	Y	N	Y	15.5	15.5	12.5

Table 11-11   Stone Peak 1 and 2 ROW/SAR M.2, CCK-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
1	2.412	Y	Y	Y	N	N	13.5	13.5
2	2.417	Y	Y	Y	N	N	13.5	13.5
3	2.422	Y	Y	Y	N	N	13.5	13.5
4	2.427	Y	Y	Y	N	N	13.5	13.5
5	2.432	Y	Y	Y	N	N	13.5	13.5

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
6	2.437	Y	Y	Y	N	N	13.5	13.5
7	2.442	Y	Y	Y	N	N	13.5	13.5
8	2.447	Y	Y	Y	N	N	13.5	13.5
9	2.452	Y	Y	Y	N	N	13.5	13.5
10	2.457	Y	Y	Y	N	N	13.5	13.5
11	2.462	Y	Y	Y	N	N	13.5	13.5
12	2.467	N	N	Y	N	N	13.5	13.5
13	2.472	N	N	Y	N	N	13.5	13.5
	NOTES: Prior to production phase the Tx power setting is not set accurately.							

Table 11-12   Stone Peak 1 and 2 ROW/SAR M.2, OFDM-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
1	2.412	Y	Y	Y	N	N	13.5	13.5	12
2	2.417	Y	Y	Y	N	N	13.5	13.5	12
3	2.422	Y	Y	Y	N	N	13.5	13.5	12
4	2.427	Y	Y	Y	N	N	13.5	13.5	12
5	2.432	Y	Y	Y	N	N	13.5	13.5	12
6	2.437	Y	Y	Y	N	N	13.5	13.5	12
7	2.442	Y	Y	Y	N	N	13.5	13.5	12
8	2.447	Y	Y	Y	N	N	13.5	13.5	12
9	2.452	Y	Y	Y	N	N	13.5	13.5	12
10	2.457	Y	Y	Y	N	N	13.5	13.5	12
11	2.462	Y	Y	Y	N	N	13.5	13.5	12
12	2.467	N	N	Y	N	N	13.5	13.5	12
13	2.472	N	N	Y	N	N	13.5	13.5	12
36	5.180	N	N	Y	N	Y	12	12	11.5
40	5.200	N	N	Y	N	Y	12	12	11.5
44	5.220	N	N	Y	N	Y	12	12	11.5
48	5.240	N	N	Y	N	Y	12	12	11.5
52	5.260	N	N	N	Y	N	12	12	11.5
56	5.280	N	N	N	Y	N	12	12	11.5
60	5.300	N	N	N	Y	N	12	12	11.5
64	5.320	N	N	N	Y	N	12	12	11.5

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
100	5.500	N	N	N	Y	N	12	12	12
104	5.520	N	N	N	Y	N	12	12	12
108	5.540	N	N	N	Y	N	12	12	12
112	5.560	N	N	N	Y	N	12	12	12
116	5.580	N	N	N	Y	N	12	12	12
120	5.600	N	N	N	Y	N	12	12	12
124	5.620	N	N	N	Y	N	12	12	12
128	5.640	N	N	N	Y	N	12	12	12
132	5.660	N	N	N	Y	N	12	12	12
136	5.680	N	N	N	Y	N	12	12	12
140	5.700	N	N	N	Y	N	12	12	12
144	5.720	N	N	N	Y	N	12	12	12
149	5.745	N	N	Y	N	Y	12	12	12
153	5.765	N	N	Y	N	Y	12	12	12
157	5.785	N	N	Y	N	Y	12	12	12
161	5.805	N	N	Y	N	Y	12	12	12
165	5.825	N	N	Y	N	Y	12	12	12
3n40	2.422	Y	Y	Y	N	N	13.5	13.5	12
4n40	2.427	Y	Y	Y	N	N	13.5	13.5	12
5n40	2.432	Y	Y	Y	N	N	13.5	13.5	12
6n40	2.437	Y	Y	Y	N	N	13.5	13.5	12
7n40	2.442	Y	Y	Y	N	N	13.5	13.5	12
8n40	2.447	Y	Y	Y	N	N	13.5	13.5	12
9n40	2.452	Y	Y	Y	N	N	13.5	13.5	12
10n40	2.457	N	N	Y	N	N	13.5	13.5	12
11n40	2.462	N	N	Y	N	N	13.5	13.5	12
38n40	5.190	N	N	Y	N	Y	12	12	11.5
46n40	5.230	N	N	Y	N	Y	12	12	11.5
54n40	5.270	N	N	N	Y	N	12	12	11.5
62n40	5.310	N	N	N	Y	N	12	12	11.5
102n40	5.510	N	N	N	Y	N	12	12	12
110n40	5.550	N	N	N	Y	N	12	12	12
118n40	5.590	N	N	N	Y	N	12	12	12
126n40	5.630	N	N	N	Y	N	12	12	12
134n40	5.670	N	N	N	Y	N	12	12	12

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
142n40	5.710	N	N	N	Y	N	12	12	12
151n40	5.755	N	N	Y	N	Y	12	12	12
159n40	5.795	N	N	Y	N	Y	12	12	12
42ac80	5.210	N	N	Y	N	N	12	12	10.5
58ac80	5.290	N	N	N	Y	N	12	12	10.5
106ac80	5.530	N	N	N	Y	N	12	12	11.5
122ac80	5.610	N	N	N	Y	N	12	12	12
138ac80	5.690	N	N	N	Y	N	12	12	12
155ac80	5.775	N	N	Y	N	Y	12	12	12

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Table 11-13   Stone Peak 2 FCC SD, CCK-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
1	2.412	Y	Y	Y	N	N	15	15
2	2.417	Y	Y	Y	N	N	16	16
3	2.422	Y	Y	Y	N	N	16	16
4	2.427	Y	Y	Y	N	N	16	16
5	2.432	Y	Y	Y	N	N	16	16
6	2.437	Y	Y	Y	N	N	16	16
7	2.442	Y	Y	Y	N	N	16	16
8	2.447	Y	Y	Y	N	N	16	16
9	2.452	Y	Y	Y	N	N	16	16
10	2.457	Y	Y	Y	N	N	16	16
11	2.462	Y	Y	Y	N	N	15	15
12	2.467	N	N	Y	N	N	10.5	12
13	2.472	N	N	Y	N	N	9.5	11
	NOTES: Prior to production phase the Tx power setting is not set accurately.							

Table 11-14   Stone Peak 2 FCC SD, OFDM-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
1	2.412	Y	Y	Y	N	N	12.5	13	10.5

Regulatory

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
2	2.417	Y	Y	Y	N	N	14	14	12
3	2.422	Y	Y	Y	N	N	16	16	16
4	2.427	Y	Y	Y	N	N	16	16	16
5	2.432	Y	Y	Y	N	N	16	16	16
6	2.437	Y	Y	Y	N	N	16	16	16
7	2.442	Y	Y	Y	N	N	16	16	16
8	2.447	Y	Y	Y	N	N	16	16	16
9	2.452	Y	Y	Y	N	N	16	16	16
10	2.457	Y	Y	Y	N	N	14	14	12
11	2.462	Y	Y	Y	N	N	11	11	10.5
12	2.467	N	N	Y	N	N	8.5	7.5	5.5
13	2.472	N	N	Y	N	N	0	0	0
36	5.180	N	N	Y	N	Y	12.5	12.5	10
40	5.200	N	N	Y	N	Y	13.5	13.5	10
44	5.220	N	N	Y	N	Y	13.5	13.5	10
48	5.240	N	N	Y	N	Y	13.5	13.5	10
52	5.260	N	N	N	Y	N	14.5	15	12
56	5.280	N	N	N	Y	N	14.5	15	12
60	5.300	N	N	N	Y	N	14.5	15	12
64	5.320	N	N	N	Y	N	12	12	10
100	5.500	N	N	N	Y	N	12	12	9
104	5.520	N	N	N	Y	N	14.5	15	13
108	5.540	N	N	N	Y	N	14.5	15	13
112	5.560	N	N	N	Y	N	14.5	15	13
116	5.580	N	N	N	Y	N	14.5	15	13
120	5.600	N	N	N	Y	N	14.5	15	13
124	5.620	N	N	N	Y	N	14.5	15	13
128	5.640	N	N	N	Y	N	14.5	15	13
132	5.660	N	N	N	Y	N	14.5	15	13
136	5.680	N	N	N	Y	N	14.5	15	13
140	5.700	N	N	N	Y	N	11.5	11.5	9.5
144	5.720	N	N	N	Y	N	14.5	14	12
149	5.745	N	N	Y	N	Y	14.5	14	12
153	5.765	N	N	Y	N	Y	14.5	14	12
157	5.785	N	N	Y	N	Y	14.5	14	12

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
161	5.805	N	N	Y	N	Y	14.5	14	12
165	5.825	N	N	Y	N	Y	14.5	14	12
3n40	2.422	Y	Y	Y	N	N	12	12	8
4n40	2.427	Y	Y	Y	N	N	13	13	10.5
5n40	2.432	Y	Y	Y	N	N	14	14	11.5
6n40	2.437	Y	Y	Y	N	N	15	15	15
7n40	2.442	Y	Y	Y	N	N	13	12	11
8n40	2.447	Y	Y	Y	N	N	12	11	10
9n40	2.452	Y	Y	Y	N	N	11	10	8
10n40	2.457	N	N	Y	N	N	8.5	7.5	5.5
11n40	2.462	N	N	Y	N	N	0	0	0
38n40	5.190	N	N	Y	N	Y	10.5	12	8.5
46n40	5.230	N	N	Y	N	Y	15	15	13
54n40	5.270	N	N	N	Y	N	15	15	15
62n40	5.310	N	N	N	Y	N	12	12	10
102n40	5.510	N	N	N	Y	N	12	12.5	10
110n40	5.550	N	N	N	Y	N	15	15	15
118n40	5.590	N	N	N	Y	N	15	15	15
126n40	5.630	N	N	N	Y	N	15	15	15
134n40	5.670	N	N	N	Y	N	15	15	15
142n40	5.710	N	N	N	Y	N	15	15	15
151n40	5.755	N	N	Y	N	Y	15	15	15
159n40	5.795	N	N	Y	N	Y	15	15	15
42ac80	5.210	N	N	Y	N	N	12	12	10
58ac80	5.290	N	N	N	Y	N	12	12	10

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
106a c80	5.530	N	N	N	Y	N	12	12	10
122a c80	5.610	N	N	N	Y	N	15	15	15
138a c80	5.690	N	N	N	Y	N	15	15	15
155a c80	5.775	N	N	Y	N	Y	15	15	15

Table 11-15   Stone Peak 2 FCC/SAR SD, CCK-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
1	2.412	Y	Y	Y	N	N	13.5	13.5
2	2.417	Y	Y	Y	N	N	13.5	13.5
3	2.422	Y	Y	Y	N	N	13.5	13.5
4	2.427	Y	Y	Y	N	N	13.5	13.5
5	2.432	Y	Y	Y	N	N	13.5	13.5
6	2.437	Y	Y	Y	N	N	13.5	13.5
7	2.442	Y	Y	Y	N	N	13.5	13.5
8	2.447	Y	Y	Y	N	N	13.5	13.5
9	2.452	Y	Y	Y	N	N	13.5	13.5
10	2.457	Y	Y	Y	N	N	13.5	13.5
11	2.462	Y	Y	Y	N	N	13.5	13.5
12	2.467	N	N	Y	N	N	10.5	12
13	2.472	N	N	Y	N	N	9.5	11
	NOTES: Prior to production phase the Tx power setting is not set accurately.							

Table 11-16   Stone Peak 2 FCC/SAR SD, OFDM-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
1	2.412	Y	Y	Y	N	N	12.5	13	10.5
2	2.417	Y	Y	Y	N	N	13.5	13.5	12
3	2.422	Y	Y	Y	N	N	13.5	13.5	13.5
4	2.427	Y	Y	Y	N	N	13.5	13.5	13.5
5	2.432	Y	Y	Y	N	N	13.5	13.5	13.5

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
6	2.437	Y	Y	Y	N	N	13.5	13.5	13.5
7	2.442	Y	Y	Y	N	N	13.5	13.5	13.5
8	2.447	Y	Y	Y	N	N	13.5	13.5	13.5
9	2.452	Y	Y	Y	N	N	13.5	13.5	13.5
10	2.457	Y	Y	Y	N	N	13.5	13.5	12
11	2.462	Y	Y	Y	N	N	11	11	10.5
12	2.467	N	N	Y	N	N	8.5	7.5	5.5
13	2.472	N	N	Y	N	N	0	0	0
36	5.180	N	N	Y	N	Y	12	12	10
40	5.200	N	N	Y	N	Y	12	12	10
44	5.220	N	N	Y	N	Y	12	12	10
48	5.240	N	N	Y	N	Y	12	12	10
52	5.260	N	N	N	Y	N	12	12	12
56	5.280	N	N	N	Y	N	12	12	12
60	5.300	N	N	N	Y	N	12	12	12
64	5.320	N	N	N	Y	N	12	12	10
100	5.500	N	N	N	Y	N	12	12	9
104	5.520	N	N	N	Y	N	12	12	12
108	5.540	N	N	N	Y	N	12	12	12
112	5.560	N	N	N	Y	N	12	12	12
116	5.580	N	N	N	Y	N	12	12	12
120	5.600	N	N	N	Y	N	12	12	12
124	5.620	N	N	N	Y	N	12	12	12
128	5.640	N	N	N	Y	N	12	12	12
132	5.660	N	N	N	Y	N	12	12	12
136	5.680	N	N	N	Y	N	12	12	12
140	5.700	N	N	N	Y	N	11.5	11.5	9.5
144	5.720	N	N	N	Y	N	12	12	12
149	5.745	N	N	Y	N	Y	12	12	12
153	5.765	N	N	Y	N	Y	12	12	12
157	5.785	N	N	Y	N	Y	12	12	12
161	5.805	N	N	Y	N	Y	12	12	12
165	5.825	N	N	Y	N	Y	12	12	12
3n40	2.422	Y	Y	Y	N	N	12	12	8
4n40	2.427	Y	Y	Y	N	N	13	13	10.5

Regulatory

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
5n40	2.432	Y	Y	Y	N	N	13.5	13.5	11.5
6n40	2.437	Y	Y	Y	N	N	13.5	13.5	13.5
7n40	2.442	Y	Y	Y	N	N	13	12	11
8n40	2.447	Y	Y	Y	N	N	12	11	10
9n40	2.452	Y	Y	Y	N	N	11	10	8
10n40	2.457	N	N	Y	N	N	8.5	7.5	5.5
11n40	2.462	N	N	Y	N	N	0	0	0
38n40	5.190	N	N	Y	N	Y	10.5	12	8.5
46n40	5.230	N	N	Y	N	Y	12	12	12
54n40	5.270	N	N	N	Y	N	12	12	12
62n40	5.310	N	N	N	Y	N	12	12	10
102n40	5.510	N	N	N	Y	N	12	12	10
110n40	5.550	N	N	N	Y	N	12	12	12
118n40	5.590	N	N	N	Y	N	12	12	12
126n40	5.630	N	N	N	Y	N	12	12	12
134n40	5.670	N	N	N	Y	N	12	12	12
142n40	5.710	N	N	N	Y	N	12	12	12
151n40	5.755	N	N	Y	N	Y	12	12	12
159n40	5.795	N	N	Y	N	Y	12	12	12
42ac80	5.210	N	N	Y	N	N	12	12	10
58ac80	5.290	N	N	N	Y	N	12	12	10
106ac80	5.530	N	N	N	Y	N	12	12	10
122ac80	5.610	N	N	N	Y	N	12	12	12
138ac80	5.690	N	N	N	Y	N	12	12	12
155ac80	5.775	N	N	Y	N	Y	12	12	12

ROW SKU

Table 11-17   Stone Peak 2 ROW SD, CCK-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
1	2.412	Y	Y	Y	N	N	14.5	14.5
2	2.417	Y	Y	Y	N	N	14.5	14.5
3	2.422	Y	Y	Y	N	N	14.5	14.5
4	2.427	Y	Y	Y	N	N	14.5	14.5
5	2.432	Y	Y	Y	N	N	14.5	14.5
6	2.437	Y	Y	Y	N	N	14.5	14.5
7	2.442	Y	Y	Y	N	N	14.5	14.5
8	2.447	Y	Y	Y	N	N	14.5	14.5
9	2.452	Y	Y	Y	N	N	14.5	14.5
10	2.457	Y	Y	Y	N	N	14.5	14.5
11	2.462	Y	Y	Y	N	N	14.5	14.5
12	2.467	N	N	Y	N	N	14.5	14.5
13	2.472	N	N	Y	N	N	14.5	14.5
	NOTES: Prior to production phase the Tx power setting is not set accurately.							

Table 11-18   Stone Peak 2 ROW SD, OFDM-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
1	2.412	Y	Y	Y	N	N	15	15	12
2	2.417	Y	Y	Y	N	N	15	15	12
3	2.422	Y	Y	Y	N	N	15	15	12
4	2.427	Y	Y	Y	N	N	15	15	12
5	2.432	Y	Y	Y	N	N	15	15	12
6	2.437	Y	Y	Y	N	N	15	15	12
7	2.442	Y	Y	Y	N	N	15	15	12
8	2.447	Y	Y	Y	N	N	15	15	12
9	2.452	Y	Y	Y	N	N	15	15	12
10	2.457	Y	Y	Y	N	N	15	15	12
11	2.462	Y	Y	Y	N	N	15	15	12
12	2.467	N	N	Y	N	N	15	15	12
13	2.472	N	N	Y	N	N	15	15	12

Regulatory

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
36	5.180	N	N	Y	N	Y	14.5	14.5	11.5
40	5.200	N	N	Y	N	Y	14.5	14.5	11.5
44	5.220	N	N	Y	N	Y	14.5	14.5	11.5
48	5.240	N	N	Y	N	Y	14.5	14.5	11.5
52	5.260	N	N	N	Y	N	14.5	14.5	11.5
56	5.280	N	N	N	Y	N	14.5	14.5	11.5
60	5.300	N	N	N	Y	N	14.5	14.5	11.5
64	5.320	N	N	N	Y	N	14.5	14.5	11.5
100	5.500	N	N	N	Y	N	14.5	14.5	12
104	5.520	N	N	N	Y	N	14.5	14.5	12
108	5.540	N	N	N	Y	N	14.5	14.5	12
112	5.560	N	N	N	Y	N	14.5	14.5	12
116	5.580	N	N	N	Y	N	14.5	14.5	12
120	5.600	N	N	N	Y	N	14.5	14.5	12
124	5.620	N	N	N	Y	N	14.5	14.5	12
128	5.640	N	N	N	Y	N	14.5	14.5	12
132	5.660	N	N	N	Y	N	14.5	14.5	12
136	5.680	N	N	N	Y	N	14.5	14.5	12
140	5.700	N	N	N	Y	N	14.5	14.5	12
144	5.720	N	N	N	Y	N	15	15	12
149	5.745	N	N	Y	N	Y	15	15	12
153	5.765	N	N	Y	N	Y	15	15	12
157	5.785	N	N	Y	N	Y	15	15	12
161	5.805	N	N	Y	N	Y	15	15	12
165	5.825	N	N	Y	N	Y	15	15	12
3n40	2.422	Y	Y	Y	N	N	15	15	12
4n40	2.427	Y	Y	Y	N	N	15	15	12
5n40	2.432	Y	Y	Y	N	N	15	15	12
6n40	2.437	Y	Y	Y	N	N	15	15	12
7n40	2.442	Y	Y	Y	N	N	15	15	12
8n40	2.447	Y	Y	Y	N	N	15	15	12
9n40	2.452	Y	Y	Y	N	N	15	15	12
10n40	2.457	N	N	Y	N	N	15	15	12

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
11n40	2.462	N	N	Y	N	N	15	15	12
38n40	5.190	N	N	Y	N	Y	13.5	14	11.5
46n40	5.230	N	N	Y	N	Y	15	15	12
54n40	5.270	N	N	N	Y	N	15	15	12
62n40	5.310	N	N	N	Y	N	14	14.5	12
102n40	5.510	N	N	N	Y	N	13	14.5	11.5
110n40	5.550	N	N	N	Y	N	15	15	12
118n40	5.590	N	N	N	Y	N	15	15	12
126n40	5.630	N	N	N	Y	N	15	15	12
134n40	5.670	N	N	N	Y	N	15	15	12
142n40	5.710	N	N	N	Y	N	15	15	12
151n40	5.755	N	N	Y	N	Y	15	15	12
159n40	5.795	N	N	Y	N	Y	15	15	12
42ac80	5.210	N	N	Y	N	N	13	13	10.5
58ac80	5.290	N	N	N	Y	N	13.5	13.5	12
106ac80	5.530	N	N	N	Y	N	12.5	12.5	11.5
122ac80	5.610	N	N	N	Y	N	15	15	12
138ac80	5.690	N	N	N	Y	N	15	15	12
155ac80	5.775	N	N	Y	N	Y	15	15	12

Regulatory

Table 11-19   Stone Peak 2 ROW/SAR SD, CCK-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power (dBm)	SISO Ant B Tx power (dBm)
1	2.412	Y	Y	Y	N	N	13.5	13.5
2	2.417	Y	Y	Y	N	N	13.5	13.5
3	2.422	Y	Y	Y	N	N	13.5	13.5
4	2.427	Y	Y	Y	N	N	13.5	13.5
5	2.432	Y	Y	Y	N	N	13.5	13.5
6	2.437	Y	Y	Y	N	N	13.5	13.5
7	2.442	Y	Y	Y	N	N	13.5	13.5
8	2.447	Y	Y	Y	N	N	13.5	13.5
9	2.452	Y	Y	Y	N	N	13.5	13.5
10	2.457	Y	Y	Y	N	N	13.5	13.5
11	2.462	Y	Y	Y	N	N	13.5	13.5
12	2.467	N	N	Y	N	N	13.5	13.5
13	2.472	N	N	Y	N	N	13.5	13.5

NOTES: Prior to production phase the Tx power setting is not set accurately.

Table 11-20   Stone Peak 2 ROW/SAR SD, OFDM-mode configuration

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
1	2.412	Y	Y	Y	N	N	13.5	13.5	12
2	2.417	Y	Y	Y	N	N	13.5	13.5	12
3	2.422	Y	Y	Y	N	N	13.5	13.5	12
4	2.427	Y	Y	Y	N	N	13.5	13.5	12
5	2.432	Y	Y	Y	N	N	13.5	13.5	12
6	2.437	Y	Y	Y	N	N	13.5	13.5	12
7	2.442	Y	Y	Y	N	N	13.5	13.5	12
8	2.447	Y	Y	Y	N	N	13.5	13.5	12
9	2.452	Y	Y	Y	N	N	13.5	13.5	12
10	2.457	Y	Y	Y	N	N	13.5	13.5	12
11	2.462	Y	Y	Y	N	N	13.5	13.5	12
12	2.467	N	N	Y	N	N	13.5	13.5	12
13	2.472	N	N	Y	N	N	13.5	13.5	12
36	5.180	N	N	Y	N	Y	12	12	11.5
40	5.200	N	N	Y	N	Y	12	12	11.5

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
44	5.220	N	N	Y	N	Y	12	12	11.5
48	5.240	N	N	Y	N	Y	12	12	11.5
52	5.260	N	N	N	Y	N	12	12	11.5
56	5.280	N	N	N	Y	N	12	12	11.5
60	5.300	N	N	N	Y	N	12	12	11.5
64	5.320	N	N	N	Y	N	12	12	11.5
100	5.500	N	N	N	Y	N	12	12	12
104	5.520	N	N	N	Y	N	12	12	12
108	5.540	N	N	N	Y	N	12	12	12
112	5.560	N	N	N	Y	N	12	12	12
116	5.580	N	N	N	Y	N	12	12	12
120	5.600	N	N	N	Y	N	12	12	12
124	5.620	N	N	N	Y	N	12	12	12
128	5.640	N	N	N	Y	N	12	12	12
132	5.660	N	N	N	Y	N	12	12	12
136	5.680	N	N	N	Y	N	12	12	12
140	5.700	N	N	N	Y	N	12	12	12
144	5.720	N	N	N	Y	N	12	12	12
149	5.745	N	N	Y	N	Y	12	12	12
153	5.765	N	N	Y	N	Y	12	12	12
157	5.785	N	N	Y	N	Y	12	12	12
161	5.805	N	N	Y	N	Y	12	12	12
165	5.825	N	N	Y	N	Y	12	12	12
3n40	2.422	Y	Y	Y	N	N	13.5	13.5	12
4n40	2.427	Y	Y	Y	N	N	13.5	13.5	12
5n40	2.432	Y	Y	Y	N	N	13.5	13.5	12
6n40	2.437	Y	Y	Y	N	N	13.5	13.5	12
7n40	2.442	Y	Y	Y	N	N	13.5	13.5	12
8n40	2.447	Y	Y	Y	N	N	13.5	13.5	12
9n40	2.452	Y	Y	Y	N	N	13.5	13.5	12
10n40	2.457	N	N	Y	N	N	13.5	13.5	12
11n40	2.462	N	N	Y	N	N	13.5	13.5	12
38n40	5.190	N	N	Y	N	Y	12	12	11.5
46n40	5.230	N	N	Y	N	Y	12	12	12
54n40	5.270	N	N	N	Y	N	12	12	12

Ch	Channel center in GHz	Active scanning allowed	IBSS allowed	MWT in same channel mode allowed	DFS applicable	Uniform spreading	SISO Ant A Tx power	SISO Ant B Tx power	MIMO 2 chains Tx power
62n40	5.310	N	N	N	Y	N	12	12	12
102n40	5.510	N	N	N	Y	N	12	12	11.5
110n40	5.550	N	N	N	Y	N	12	12	12
118n40	5.590	N	N	N	Y	N	12	12	12
126n40	5.630	N	N	N	Y	N	12	12	12
134n40	5.670	N	N	N	Y	N	12	12	12
142n40	5.710	N	N	N	Y	N	12	12	12
151n40	5.755	N	N	Y	N	Y	12	12	12
159n40	5.795	N	N	Y	N	Y	12	12	12
42ac80	5.210	N	N	Y	N	N	12	12	10.5
58ac80	5.290	N	N	N	Y	N	12	12	12
106ac80	5.530	N	N	N	Y	N	12	12	11.5
122ac80	5.610	N	N	N	Y	N	12	12	12
138ac80	5.690	N	N	N	Y	N	12	12	12
155ac80	5.775	N	N	Y	N	Y	12	12	12

11.3 Regulatory and safety certification

The following regulatory and safety information is subject to change.

Table 11-21 Wi-Fi safety and regulatory USA

USA	Requirements	Criteria
	EMI	FCC Part 15, Subpart B, Class B (CISPR 22 Limits at 10 m)
	RF	FCC Part 15, Subpart C (Sections 15.205, 15.207, 15.209, and 15.247)
		FCC Part 15, Subpart E (Section 15.407)
	Safety	UL 60950-1

Table 11-22 Wi-Fi safety and regulatory Europe

Europe	Requirements	Criteria
	EMC	EN301489-1, EN 301489-17
	RF	EN300 328 and EN301-893 as DFS slave terminal
	Safety	EN60950-1 via CB Report (IEC60950-1)
		R&TTE Health Requirement referring to EN 50566-2013 & EN 62209-2:2010

Table 11-23 Wi-Fi safety and regulatory Japan

Japan	Requirements	Criteria
	EMI	VCCI Class B

Intel® Dual-Band Wireless (Stone Peak)
External Product Specification (EPS)
64   **Intel Confidential**

September 2018
Document Number: 538080-4.1

	RF	STD T66, STD T71, ARIB W52, W53, W56
	Safety	EN60950-1 via CB Report (IEC60950-1)
		R&TTE Health Requirement article 1(a) referring to EN 50566-2013 & EN 62209-2:2010

Table 11-24   Wi-Fi safety and regulatory Australia/New Zealand

Australia/ New Zealand	Requirements	Criteria
	EMC	EU test reports
	RF	Radio communications (EMR) Standard 2003; EU test reports + Delta AS-NZ4268
	Safety	CB Cert. and Report (IEC60950-1)

Table 11-25   Wi-Fi safety and regulatory other geographies

Other geographies	Requirements	Criteria
	Priority 2 Countries	To be covered in MWG Regulatory WW Country Coverage
	Priority 3 Countries	To be covered in MWG Regulatory WW Country Coverage

Note: Regulatory pre-scans and certification are tested using a combo Bluetooth/Wi-Fi reference antenna. For reference antenna characteristics, see Section 15.4.

§

12   Mechanical Specifications

This section provides information about the mechanical specifications.

12.1   Weight

Table 12-1   Weight

Product	Weight (g)
Stone Peak 2 (M.2 2230 card)	3.1
Stone Peak 2 (M.2 1216 solder down)	0.52
Stone Peak 1 (M.2 2230 card)	3.1

12.2   M.2 2230 mechanical specification

Stone Peak SKUs will be available in M.2 Type 2230-S3-A-E form factor.

See the M.2 specification document under the PCISIG releases:
http://www.pcisig.com/specifications/pciexpress/review_zone/#M.2.

The information in this document is complaint to the *M.2 specification* (Rev 1.0, Nov 2013)

All StP M.2 connectorized SKUs can be installed on a platform with either host connector Key A or Key E.

Figure 12-1   StP1 and StP 2 2230 SKU dimensions (Type 2230)[1]
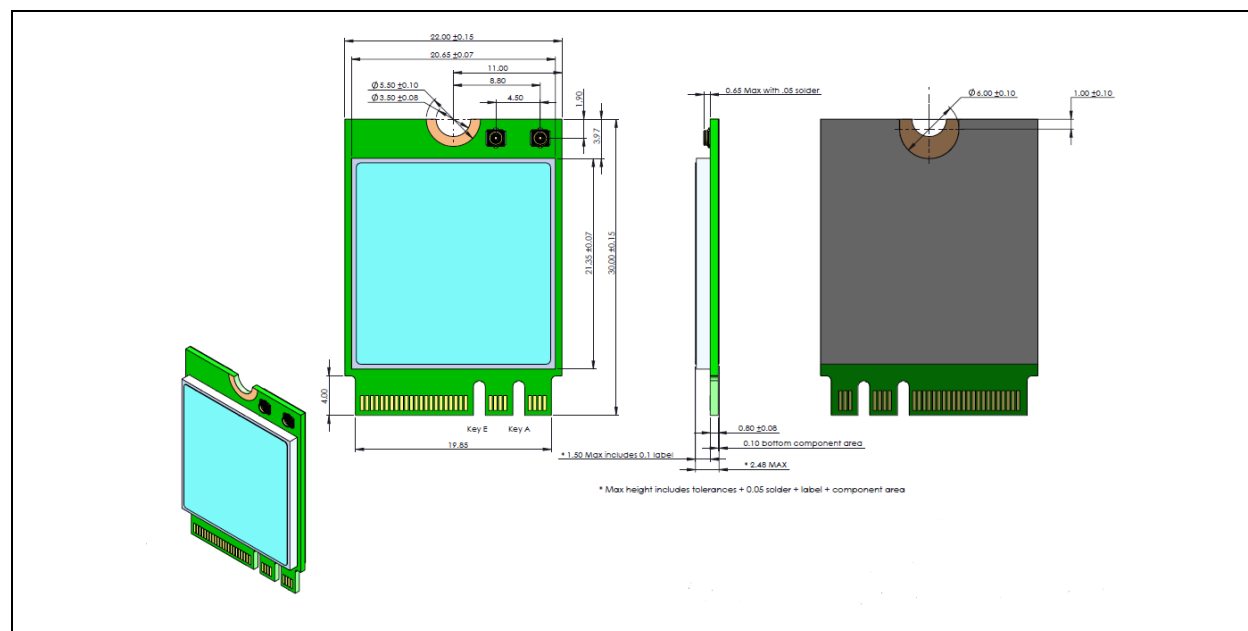
NOTES:
1. Max component heights include tolerance + .05 soldier + .10 for label height.
2. Dimensions are in mm.
3. Do not scale drawing.
4. Tolerances: angles +/– 1 degrees;
   X.X +/– 0.25 mm;
   X.XX +/– 0.150 mm;
   X.XXX +/– 0.100 mm

12.3   M.2 1216 mechanical specification

Stone Peak 2 and Stone Peak 1 soldered down module SKU will be available in M.2 Type 1216 form factor.

See the M.2 specification document under the PCISIG releases: *http://www.pcisig.com/specifications/pciexpress/review_zone/#M.2*.

This information in this document is complaint to the *M.2 specification* (Rev 1.0, Nov 2013)

For M.2 1216 specifications, see Section 2.3.6.2 in the *M.2 specifications.*

Figure 12-2   Stone Peak M.2 1216 SD SKU dimensions (Type 2216)
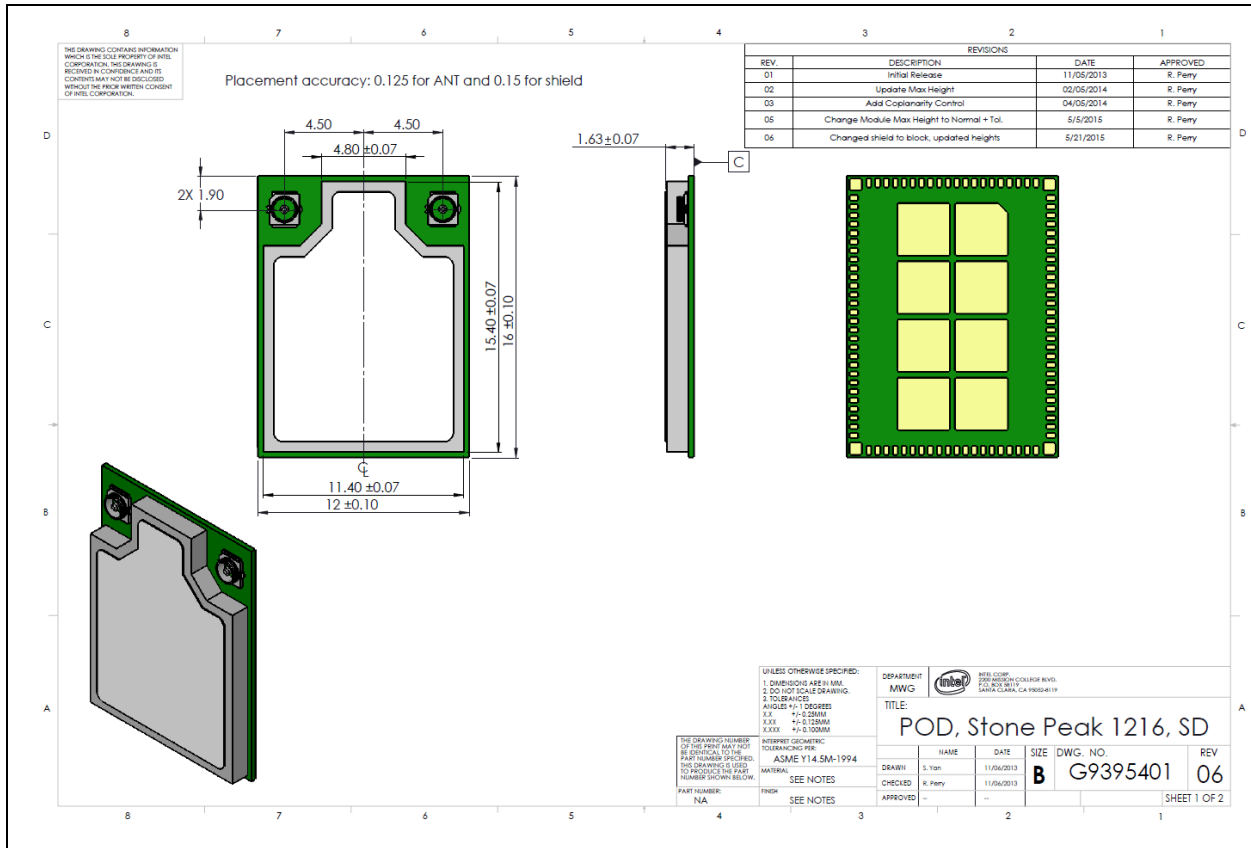
NOTES:
1. Dimensions are in mm.
2. Do not scale drawing.
3. Tolerances: angles +/− 1 degrees
     X.X +/− 0.25 mm
     X.XX +/− 0.150 mm
     X.XXX +/− 0.100 mm

12.4   Antenna receptacles

An M.2 compatible RF micro coax type connector (like I-PEX MHF4 connector) is used on the Stone Peak hardware.

The antenna connectors will be labeled 1 and 2 for 2230, and 1 and 3 for 1216. The definition of the antenna port is described in the below table.

Table 12-2   StP 1216 antennas definition

Antenna Port Definition	Function
3/Main	Wi-Fi Tx/Rx
1/Aux	Shared antenna: Wi-Fi Tx/Rx, Bluetooth Tx/Rx

Table 12-3   StP SD 2230 antennas definition

Antenna Port Definition	Function
2/Main	Wi-Fi Tx/Rx
1/Aux	Shared antenna: Wi-Fi Tx/Rx, Bluetooth Tx/Rx

Table 12-4   Antenna port impedance

Nominal Antenna Port Impedance	Value
Antenna Port Impedance	50 Ohm

For more information on guidelines how to design the platform antenna, please refer to the *Broadwell Platform Design Guidelines*.

12.4.1   Antenna connector insertion tool

Each connector supplier has their own tool they recommend. The OEM should contact their connector supplier for the recommended tool for the connector they are using.

12.5   M.2 antenna retention

12.5.1   Recommended method for retention of M.2 cable

- Intel recommends restraining the antenna cables of M.2 products within the first 25 mm or less of cable length leaving the RF connectors on the module.
- Intel recommends using a robust tape or adhesive to secure the cables so they do not move or pull on the RF connector during shock and vibration of the system.

Figure 12-3   M.2 cable retention

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13 Environmental Specifications

Table 13-1 and Table 13-2 provide operating condition and maximum rating requirements for the Stone Peak hardware.

Table 13-1 Operating conditions

Environment	Limits
Operating temperature	0 °C – 80 °C

NOTES: Environmental temperature is measured on the card shield cover.

Table 13-2 Storage conditions

Environment	Limits
Storage temperature (non-operational)	–40 °C to 70 °C
Humidity (non-operational)	50% to 90% non-condensing (at temperatures of 25 °C to 35 °C)

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14 Certification Requirements

A preliminary list of certification requirements includes the following:

Table 14-1 Certification requirements

Requirement	Detail description
Bluetooth USB-IF	All products shall pass chapter 9 of USB-IF in order get USB-IF certification for Microsoft Windows 8* logo requirements
WHQL	Microsoft Windows 7* and Microsoft Windows 8/8.1* WHQL/WHCK tests for networking device
Wi-Fi certification for Windows* OS	Microsoft Windows 7* and Microsoft Windows 8/8.1*
Bluetooth certifications	Bluetooth SIG certification for the device and the SW stack delivered with it
Android* certification	The products shall meet Android* CDD requirements and shall pass associated CTS
Chrome* certification	The device shall pass Chrome* AVL tests

NOTES: 1. Not submitted to external certification lab for PCI-SIG specification compliance, however PCI compliance is tested internally (within Intel Corporation).

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15 Antenna Design Considerations

15.1 Antenna port impedance

Nominal antenna port impedance specification is 50 ohm.

15.2 Antennas frequency bands

See the *Broadwell Platform Design Guide*.

15.3 Antenna gain

See the *Broadwell Platform Design Guide*.

15.4 Antenna characteristics

See the *Broadwell Platform Design Guide*.

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16 Wireless Features and Properties

16.1 HW RF kill considerations

If for some reason the platform doesn't support HW signal for wireless disable, Intel recommends not connecting any signal to the wireless disable pins on the module.

16.2 Data transmission

Data transmission is always initiated by software, which is then passed down through the MAC, through the digital and analog baseband, and finally to the RF chip. This is true for both Wi-Fi and Bluetooth.

Several special packets (for Wi-Fi: ACKs, CTS, PS Poll, etc.) are initiated by the MAC. These are the only ways the digital baseband portion will turn on the RF transmitter, which it then turns off at the end of the packet. Therefore, the transmitter will be *ON* only while one of the packets is transmitted.

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17 Platform Design Recommendation

17.1 Platform manufacturing guidelines

17.2 Good practice for low-noise design

Since the wireless module is susceptible to radio noise, it is important to make sure that under the module and in its vicinity there are no routing of signals which might interfere with the wireless module. Especially, high-speed logic (CPU clock, memory bus, etc.) should not be routed below or above and close to the wireless module, and also along the RF lines from the wireless module antenna port to the antenna.

17.3 Platform design points to consider

The below are important issues that need to be reviewed on the schematic design of every platform.

Table 17-1   Platform design issues

Topic	Item	Review comments
General	Which M.2 mechanical key is used?	Make sure it fits the product
	Antennas: if appear in the scheme, check if correct	
Interfaces: check that they are connected as they should be	Wi-Fi host I/F	
	BT host I/F	
	CLINK	Please follow Intel CLINK design guidelines to avoid noise on the CLINK interface. As a rule, CLINK interface needs to be isolated from high speed and noisy lines, and not using vias to route the interface signals.
	LTE coex	
	ISH UART	
	Discrete signals (W_Disable, LED, SUSCLK)	(1) LED is OD, can be wired-or if needed. (2) SUSCLK is not mandatory, can be left N/C
	Check for relevant interfaces correctness of Rx/Tx directions	
IOs	Pullups/Pulldowns: check for each signal correct usage of PU/PD according to table in EPS Verify no PU/PD on signals that should not have them	(1) W_DISABLE1# and W_DISABLE2# have an internal (in silicon) pull-ups as defined by PCIe spec. no need for platform pull-ups. (2) CLKREQ#, PERST# do not have internal pull-ups, and according to the PCIe spec there is a need to add pull-ups on the platform side (inside the PCH or on the motherboard for older systems)
	Voltage levels: check for each signal correct voltage level (3.3 V/1.8 V)	1216SD 1.8 V module requires that the following pins will be connected to matching 1.8 V GPIOs on the platform side: • SUSCLK(32 kHz) (1.8 V) • W_DISABLE1# (1.8 V) • W_DISABLE2# (1.8 V) • PEWAKE# (1.8 V)

Topic	Item	Review comments
		• CLKREQ# (1.8 V) • PERST# (1.8 V)
PCIe sideband signals (refer to EPS for guidelines)	Check if PERST is shared or not	
	Check how PERST is connected in the platform side	
	Check if PEWAKE is shared or not	
	Check how PEWAKE is connected in the platform side	
	Check that CLKREQ is not shared	
Power supply	Check how the power supply is controlled by the platform (can it be turned off by the platform)	
	Check existence of filtering caps on power supply	Recommended: a set of 4.7uF+0.1uF+0.01uF near pins 2 and 4, and another set near pins 72 and 74
PCIe guidelines	Check AC coupling caps on the differential lines according to PCIe spec	(1) The StP module has AC coupling caps on the PCIe TX signals as defined by the PCIe spec. no need for additional caps on the platform side for the PCIe Tx signals (direction: from the StP module to the host). (2) The platform should have AC coupling caps on the PCIe Tx signals from the host to the module as defined by the PCI spec. these caps should be located close to the transmitter.

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18 Platform and Host Interface Requirements

18.1 Mechanical directives

For M.2, see: *PCI Express M.2 Electromechanical Specification* electricals and signals connections directives.

18.1.1 USB signals

The BT functionality of the card operated using the USB signals as the host interface bas.

As defined by the USB standard, when the platform gets to stand-by mode the card operate its USB in a selective suspend mode. This means that the D+ signal is kept as logical 1 value by an internal pull-up.

18.1.2 CLINK signals

The CLINK signal are specific for Intel® AMT based platforms; for those that do not support AMT, those signals **must not** be used; and should be kept disconnected on the platform level.

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19 Appendix: Document References

Table 19-1   Document references

Document name	Location
Wireless LAN MAC and PHY Specifications, 802.11b	*http://standards.ieee.org/getieee802/download/802.11b-1999_Cor1-2001.pdf*
Wireless LAN MAC and PHY Specifications, 802.11g	*http://standards.ieee.org/getieee802*
Wireless LAN MAC and PHY Specifications, 802.11a	*http://standards.ieee.org/getieee802*
Wireless LAN MAC and PHY Specifications, 802.11n-2009	*http://standards.ieee.org/getieee802*
PCI Express Base Specification, Rev 1.2	*http://www.pcisig.com/specifications/pciexpress*
PCI Express Card Electromechanical Specification, Rev 1.2	*http://www.pcisig.com/specifications/pciexpress*
PCI Local Bus Specification Rev. 2.3	*http://www.pcisig.com/specifications/conventional/conventional_pci*
PCI Bus Power Management Interface Specification Rev 1.1	*http://www.pcisig.com/specifications/conventional/pci_bus_power_management_interface*
Advanced Configuration and Power Interface Version 3.0	*http://www.acpi.info/spec.htm*
Microsoft Hardware Device Class Power Management Specification	*http://www.microsoft.com/whdc/hwdev/resources/specs/pmref/default.mspx*
M.2 specification	*http://www.pcisig.com/apps/org/workgroup/pciexpress/miniexpress/documents.php*

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