Compal Confidential

Schematics Document

AUBURNDALE/CLARKSFIELD with Intel IBEX PEAK-M core logic

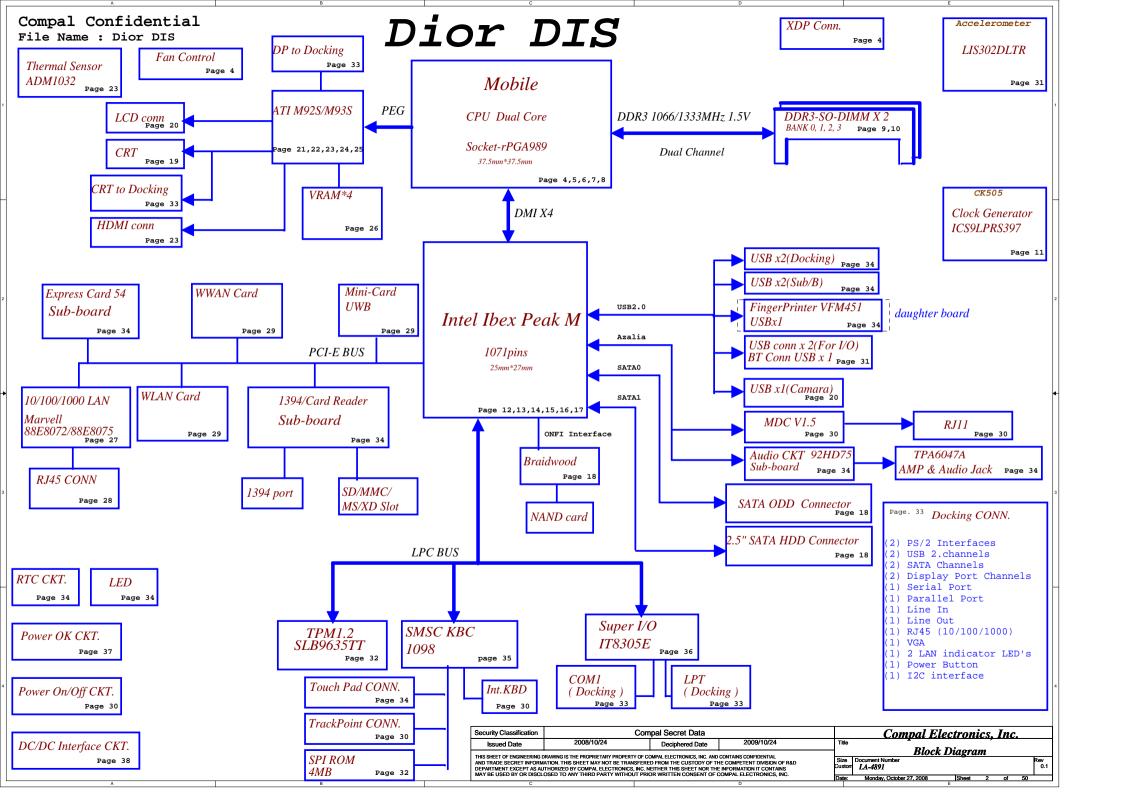
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Voltage Rails (O MEANS ON X MEANS OFF)

power plane	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +NVVDD +VCCP +CPU_CORE +1.05VS +1.8VS
so	0	0	0	0	0
s1	0	0	0	0	0
s3	0	0	0	0	X
S5 S4/AC	0	0	0	X	X
S5 S4/ Battery only	0	0	x	x	X
S5 S4/AC & Battery don't exist	0	X	X	х	x

SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	Х	Х	X	X	X	Х	Х	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	V	X	V
SML0CLK SML0DATA	Calpella	X	Х	Х	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	Х	Х	X	X	Х	Х	V	X

Symbol Note:

: means Digital Ground
: means Analog Ground

Install below 43 level BOM structure for ver. 0.1

DEBUG@: means just build when PCIE port 80 CARD function enable. Remove before MP

M92@: Install for M92 Graphic controller 8072@: Install for 8072 NIC controller 1098@: Install for 1098 KBC controller CK32@: Install for 32 pin CLOCK GEN

Install below 45 level BOM structure for ver. 0.1

45@: means just put it in the BOM of 45 level.

Reserve below BOM structure for ver. 0.1

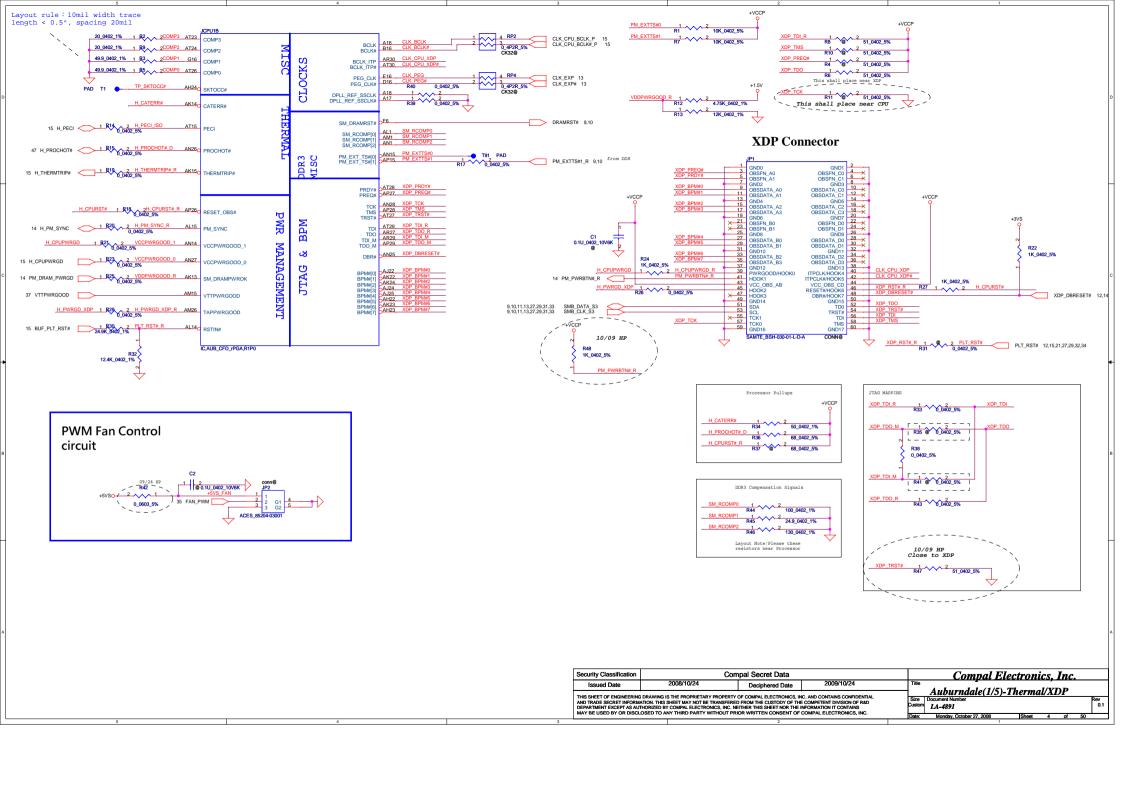
@: means just reserve, no buildCONN@: means ME part.

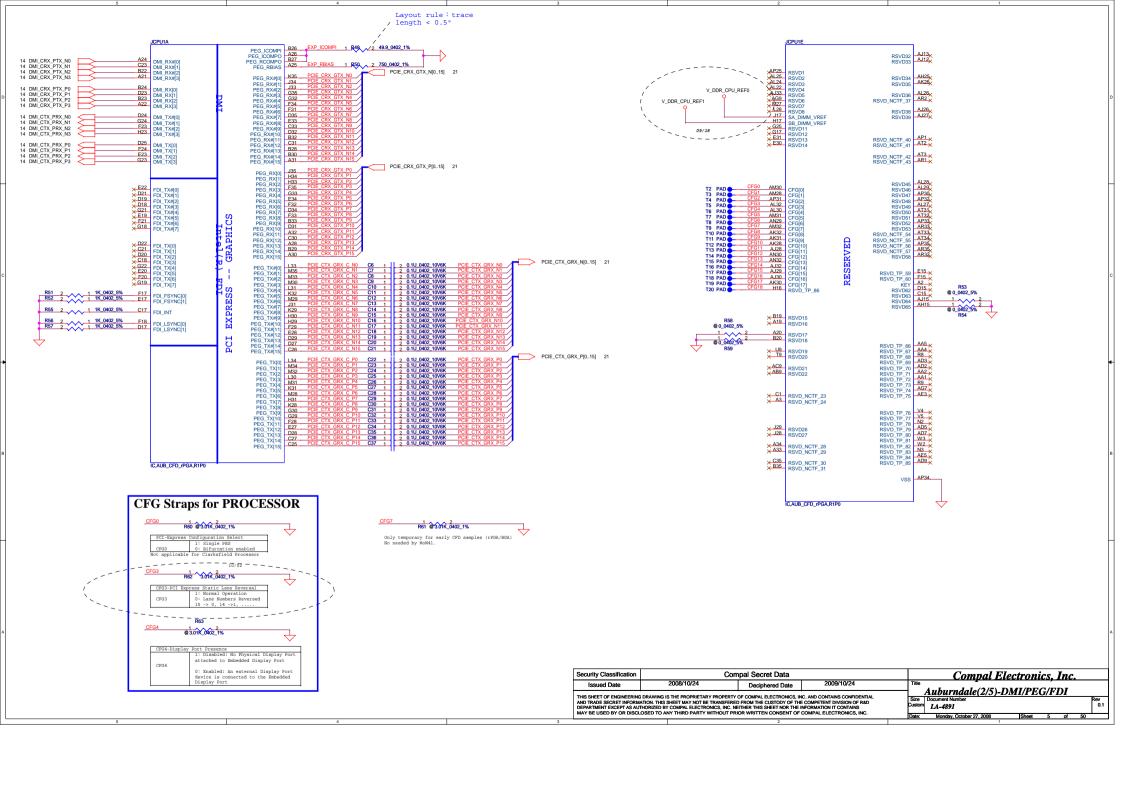
M93@: Install for M93 Graphic controller

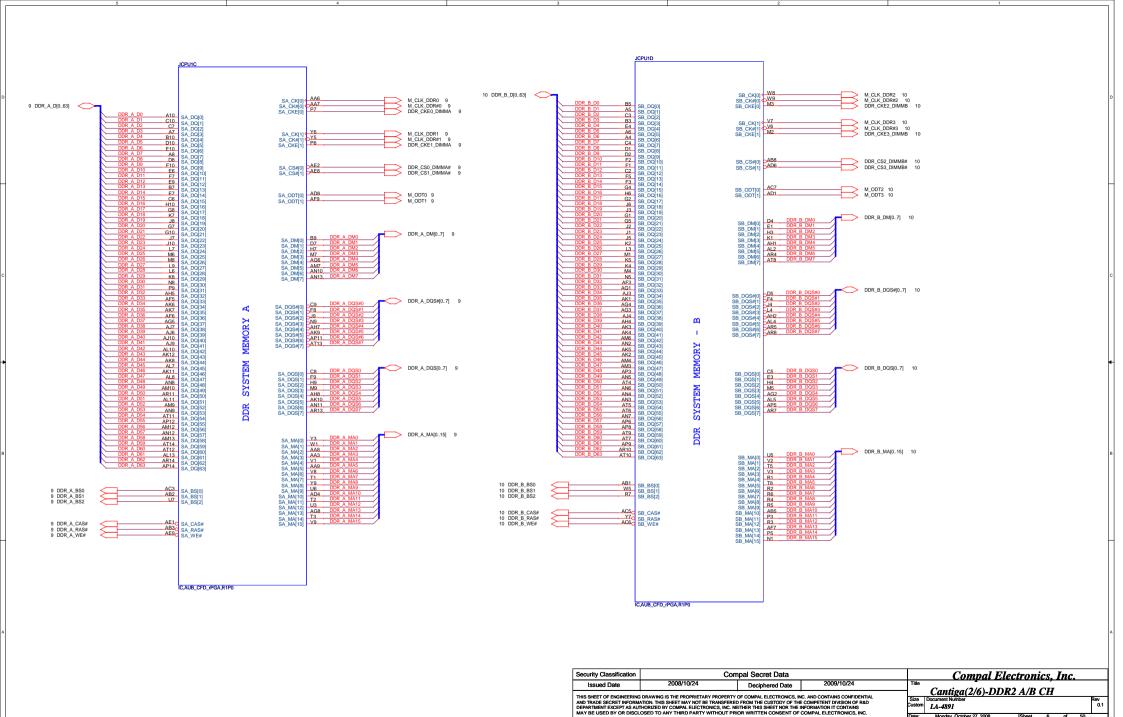
8075@: Install for 8075 NIC controller 1091@: Install for 1091 KBC controller

CK72@: Install for 72 pin CLOCK GEN

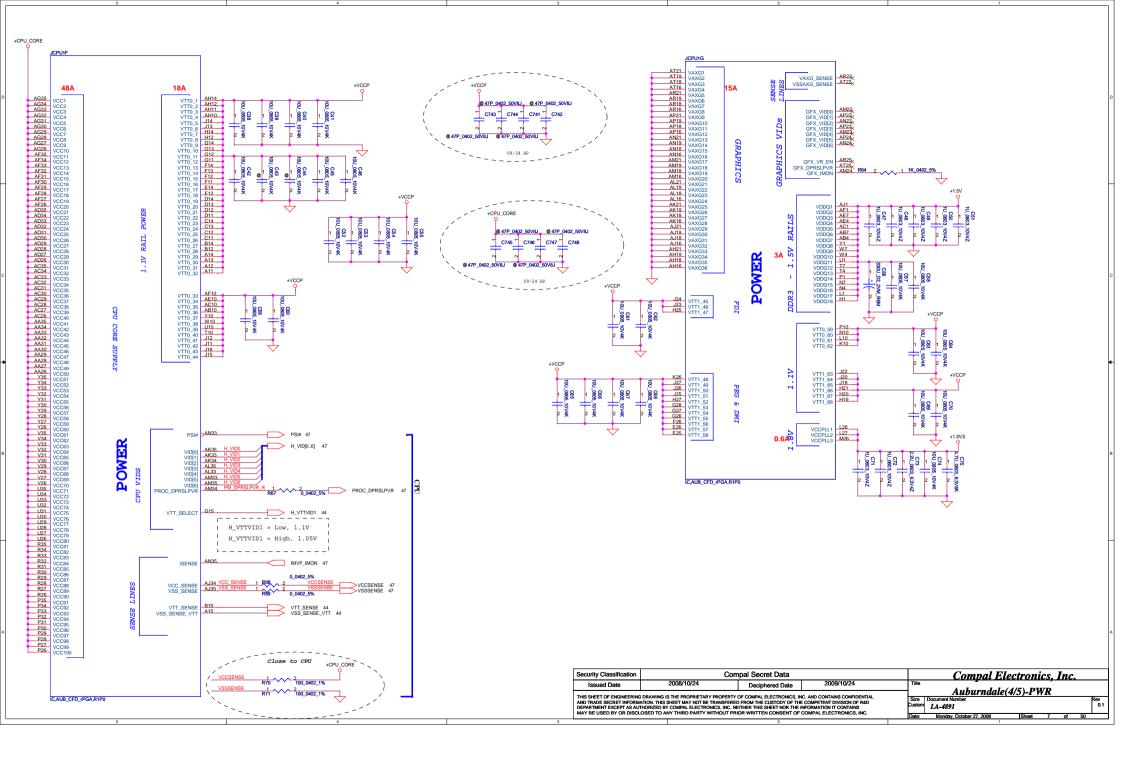
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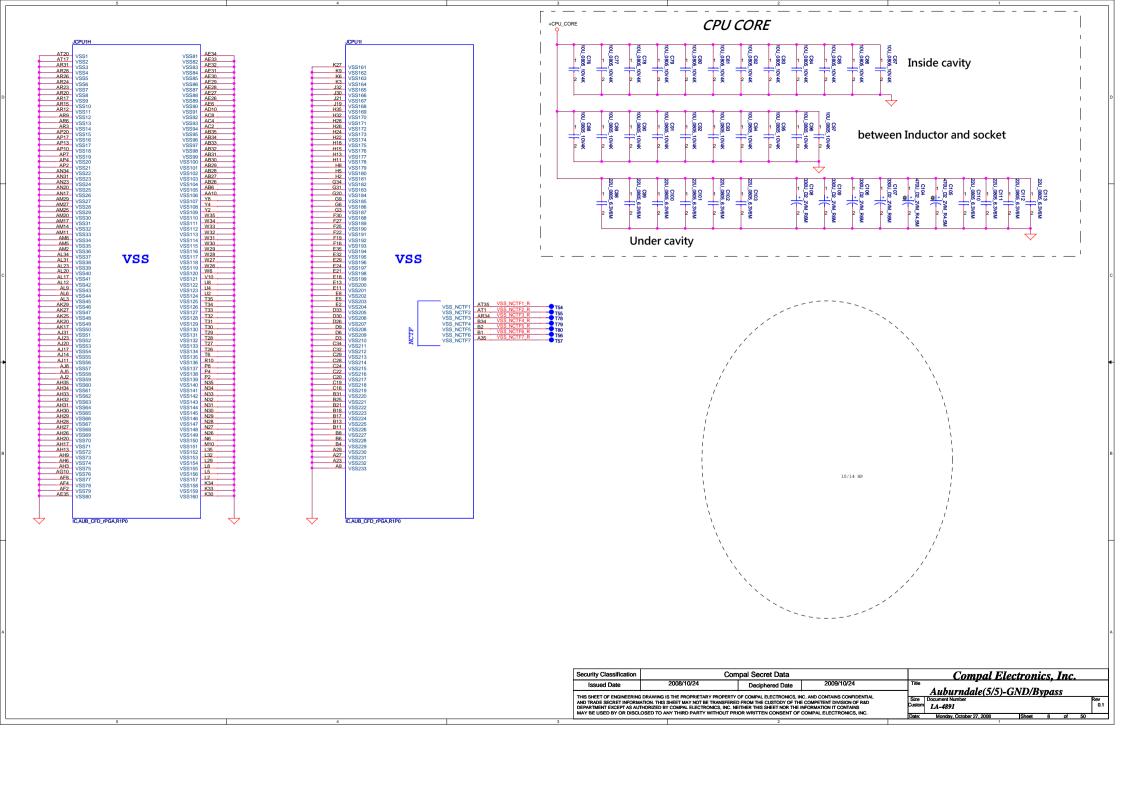


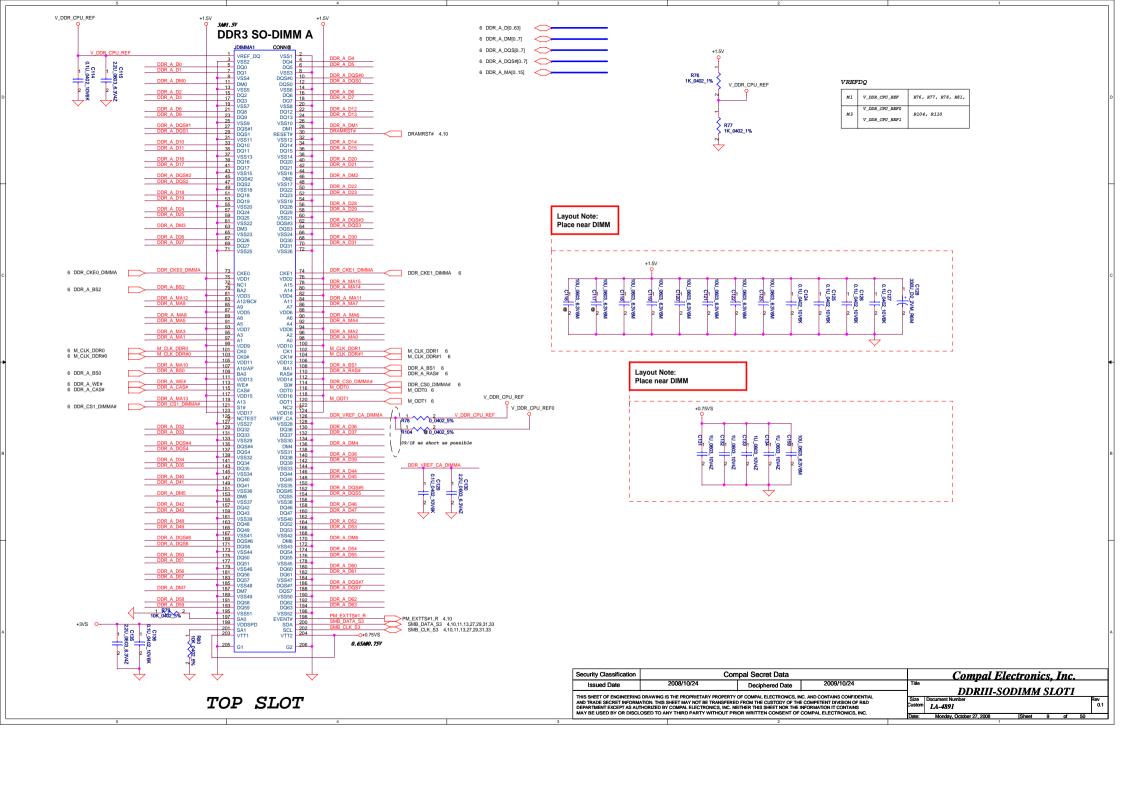


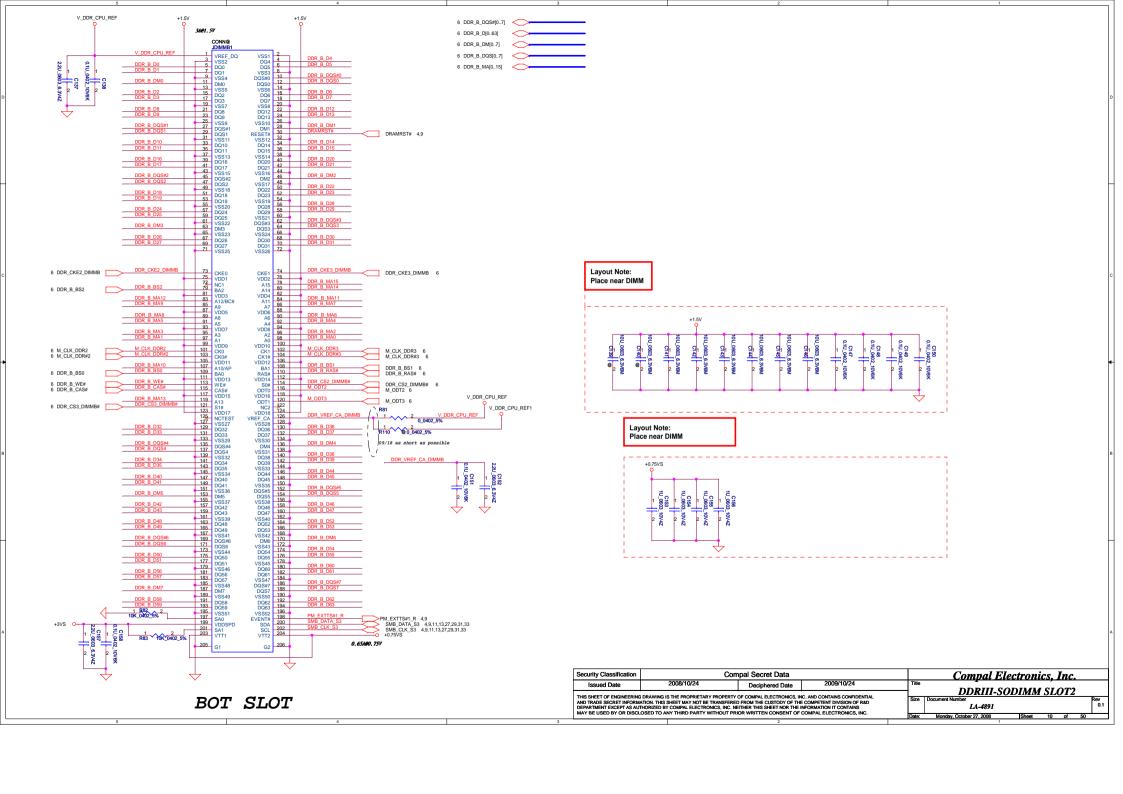


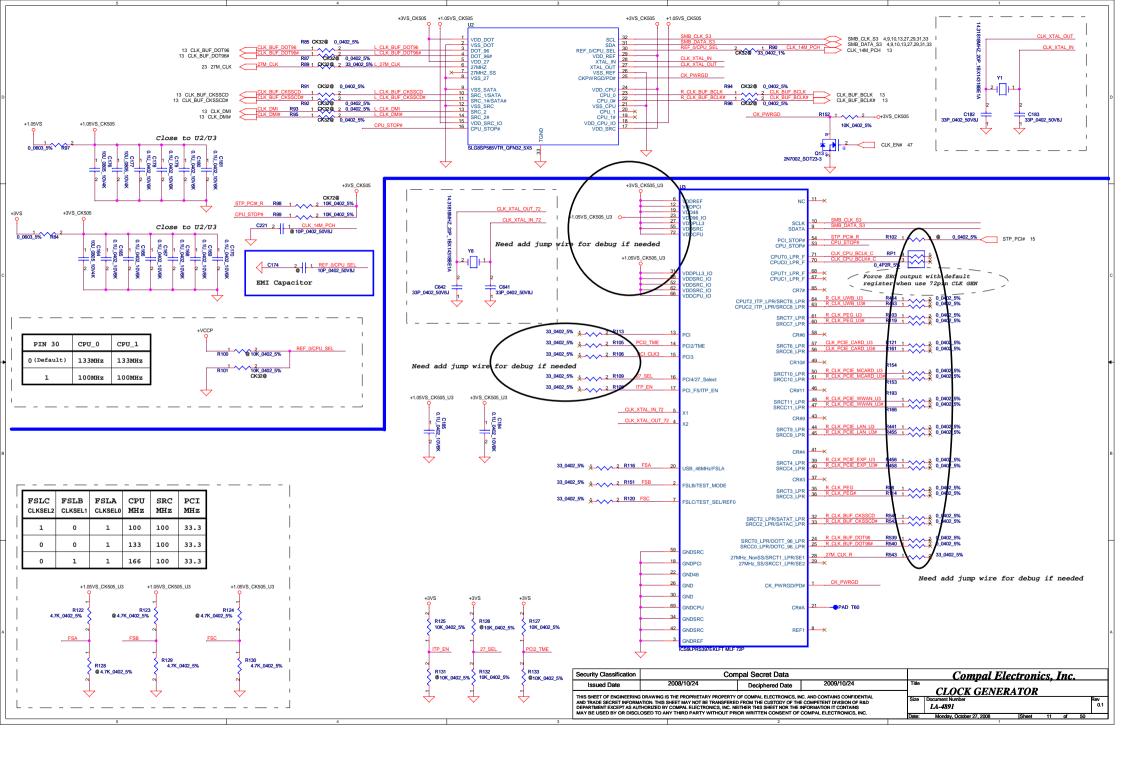
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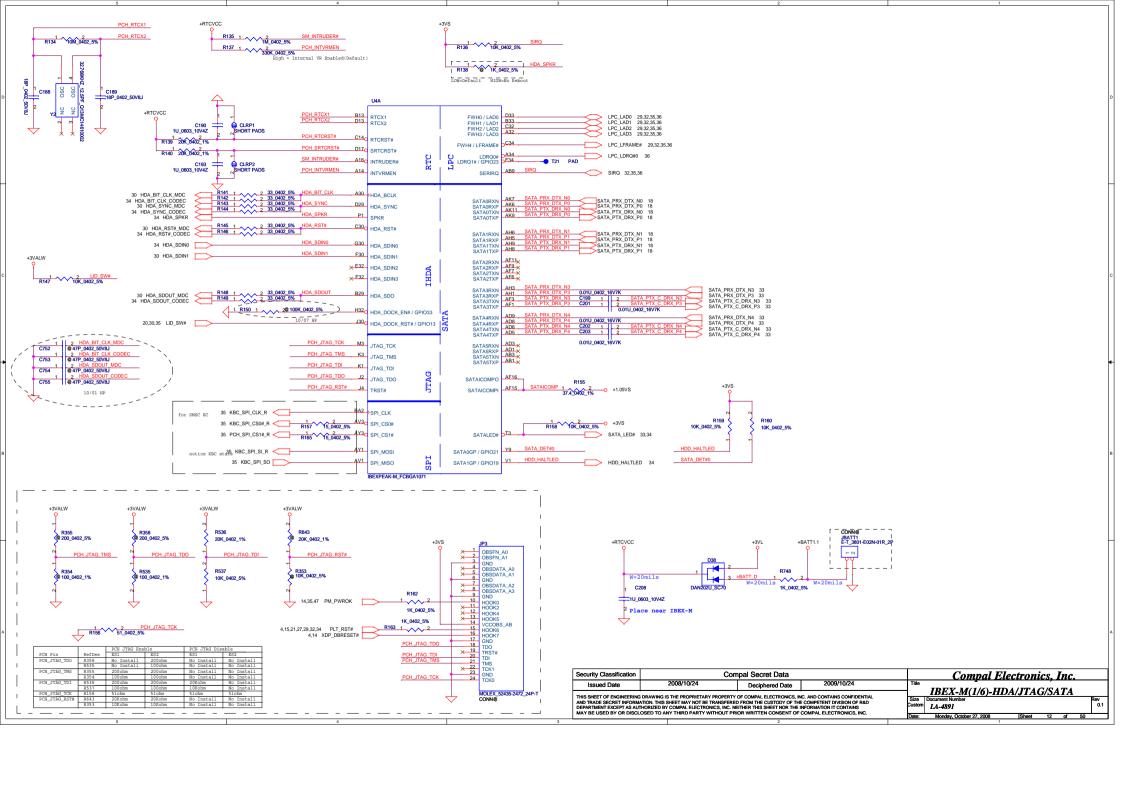


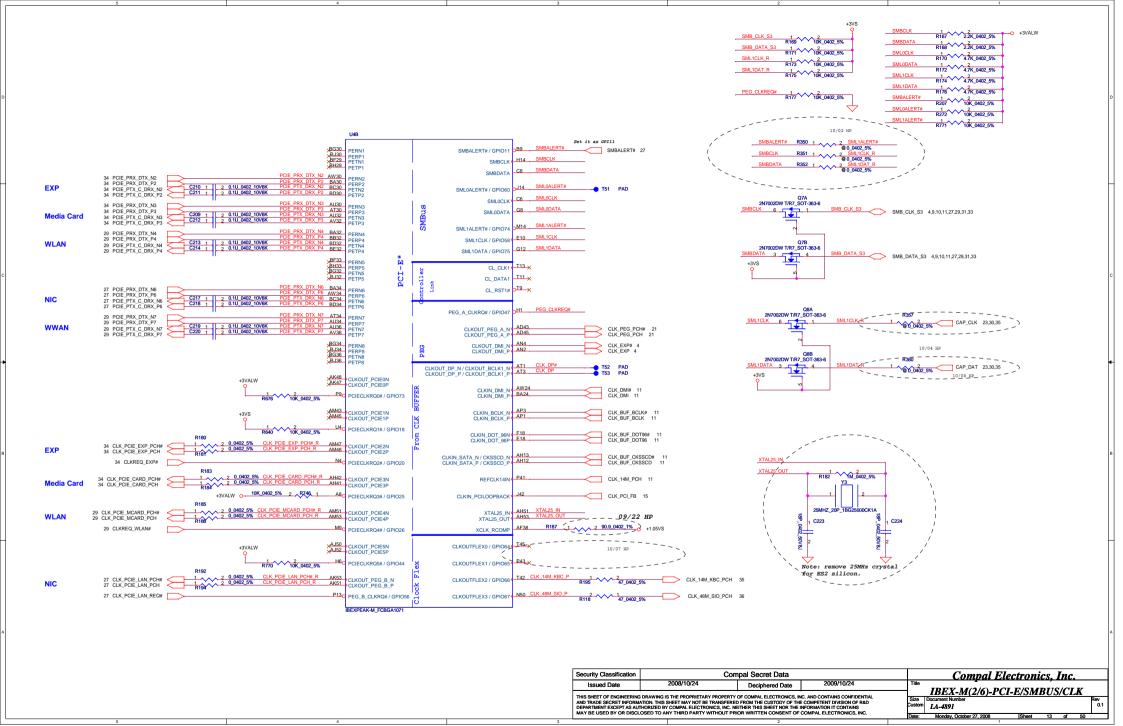


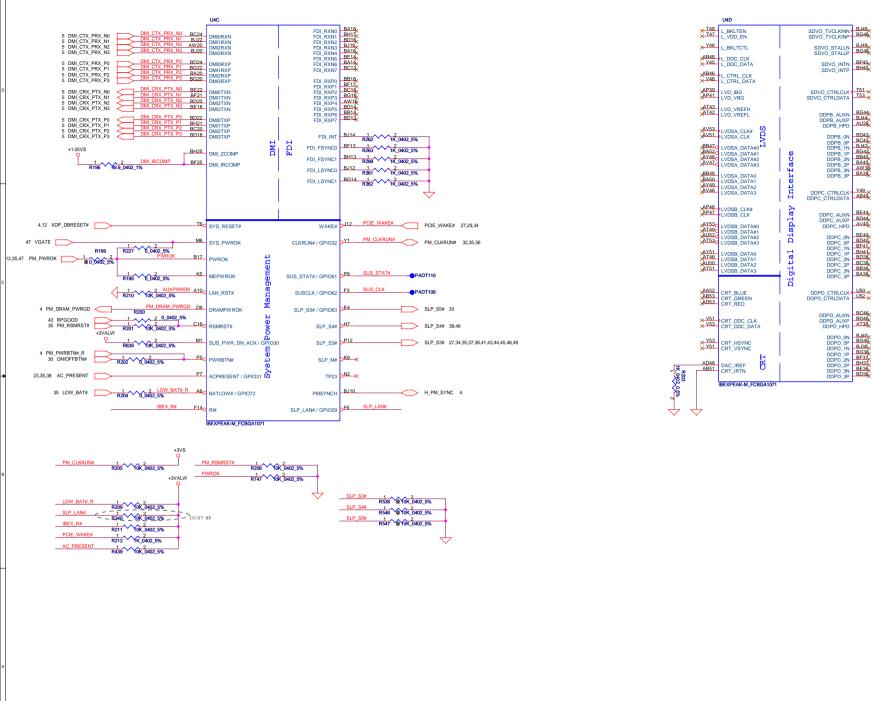










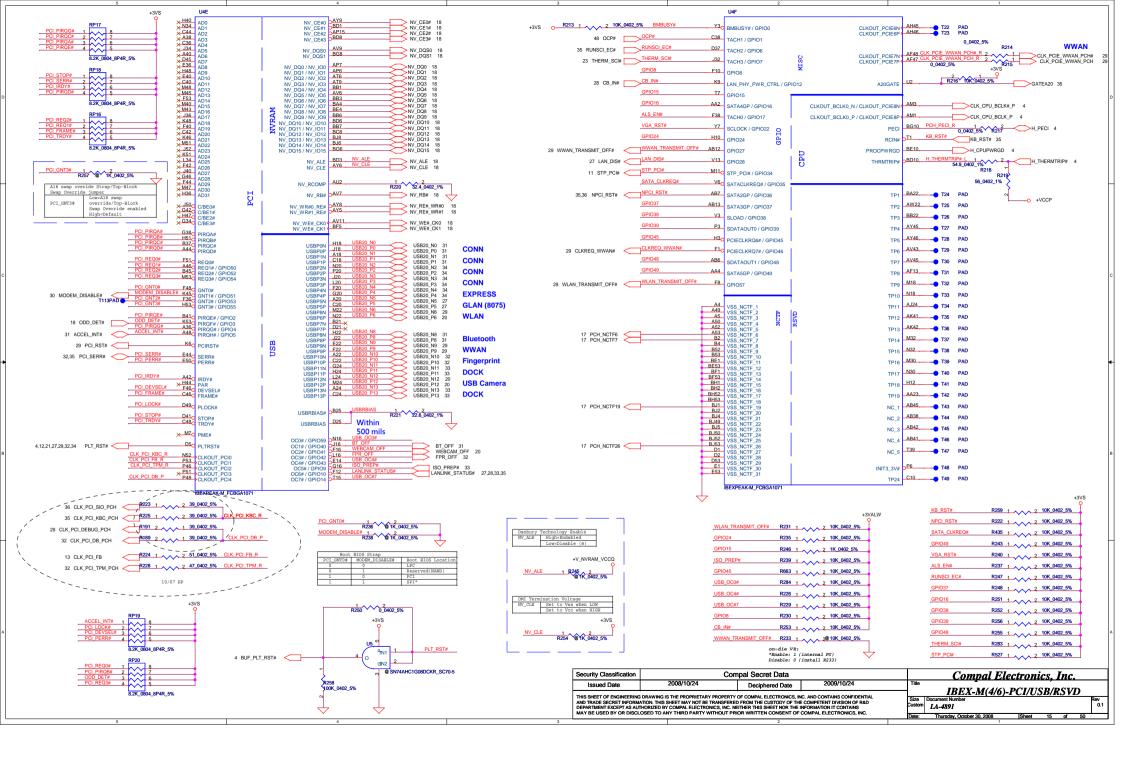


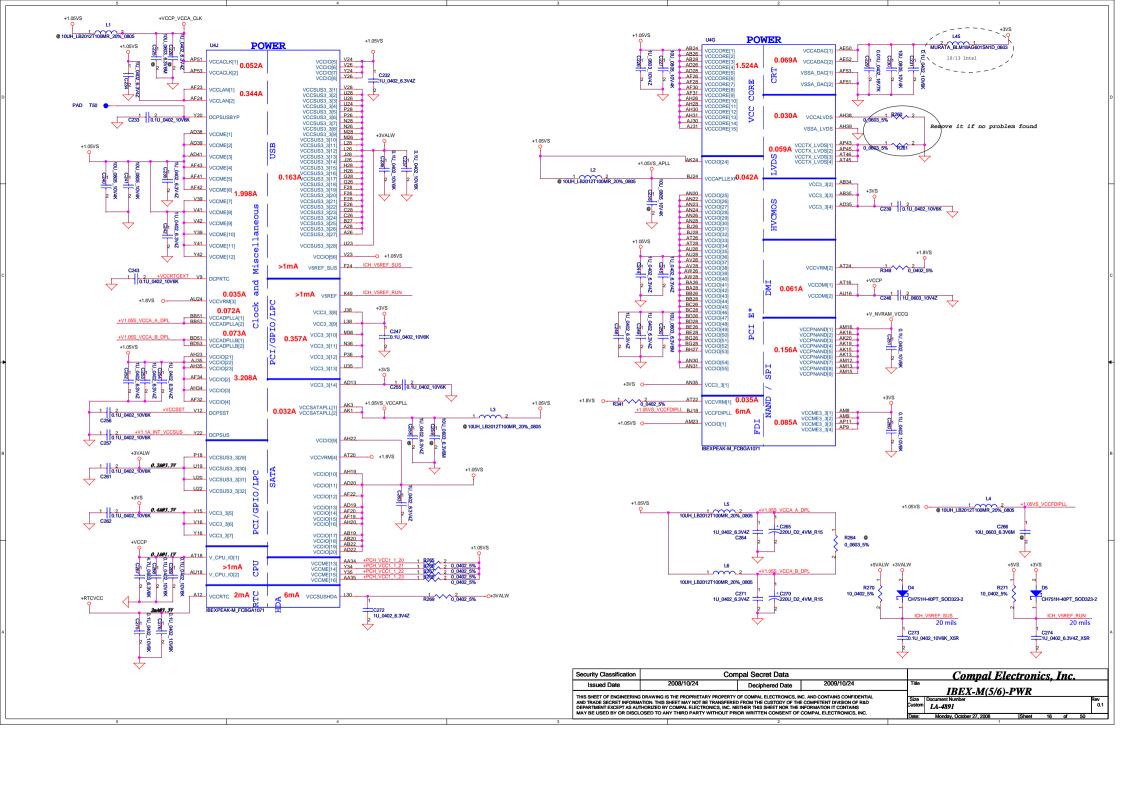
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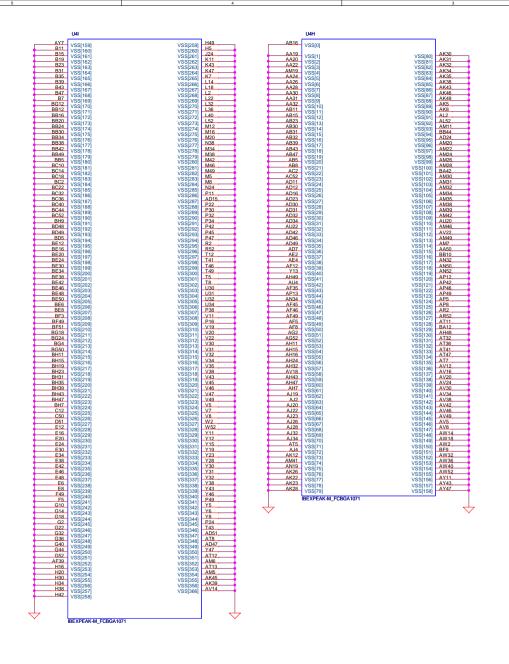
DDPB_0P BL42 DDPB_0P BL42 DDPB_1P BL42 DDPB_1P BB40 DDPB_2P BA40 DDPB_3P BA38 DDPB_3P BA38

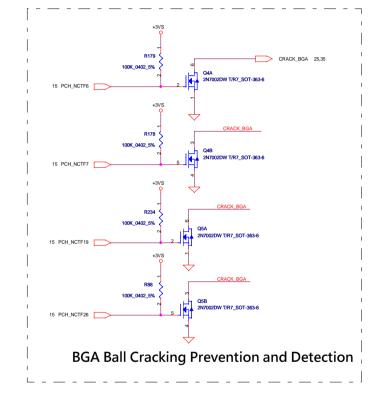
DDPC_NP B441 DDPC_1N B441 DDPC_1P B441 DDPC_1P B441 DDPC_2P B38 DDPC_2P B38 DDPC_3N B36 DDPC_3N BA36

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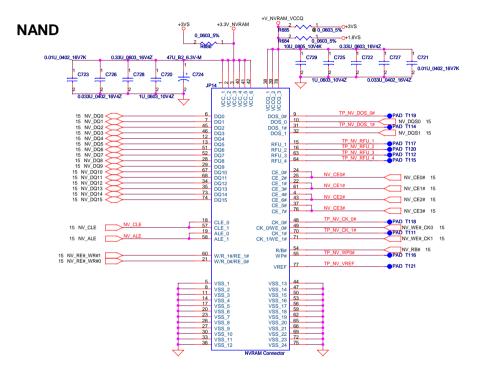


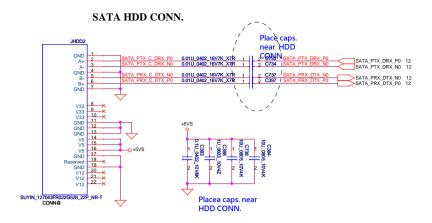


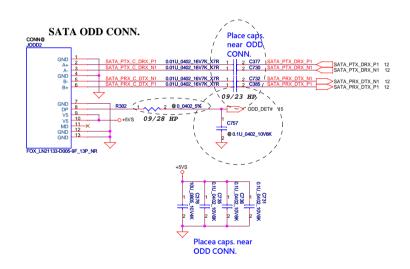




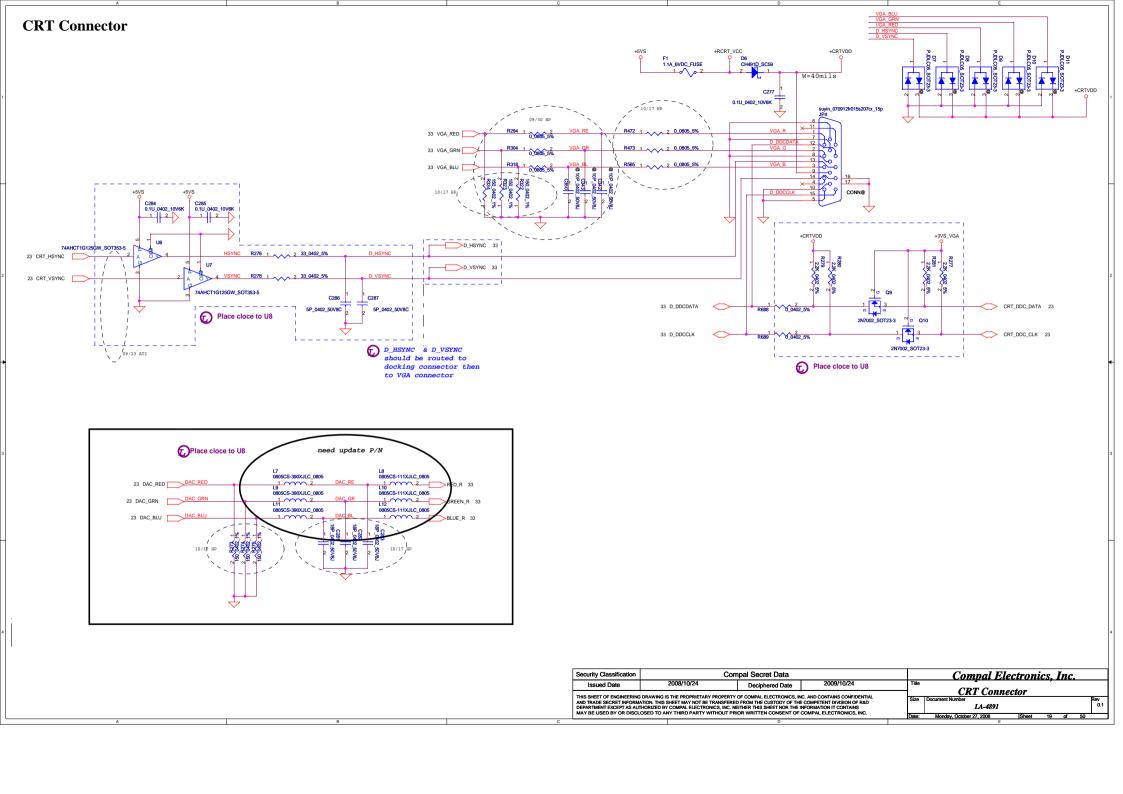
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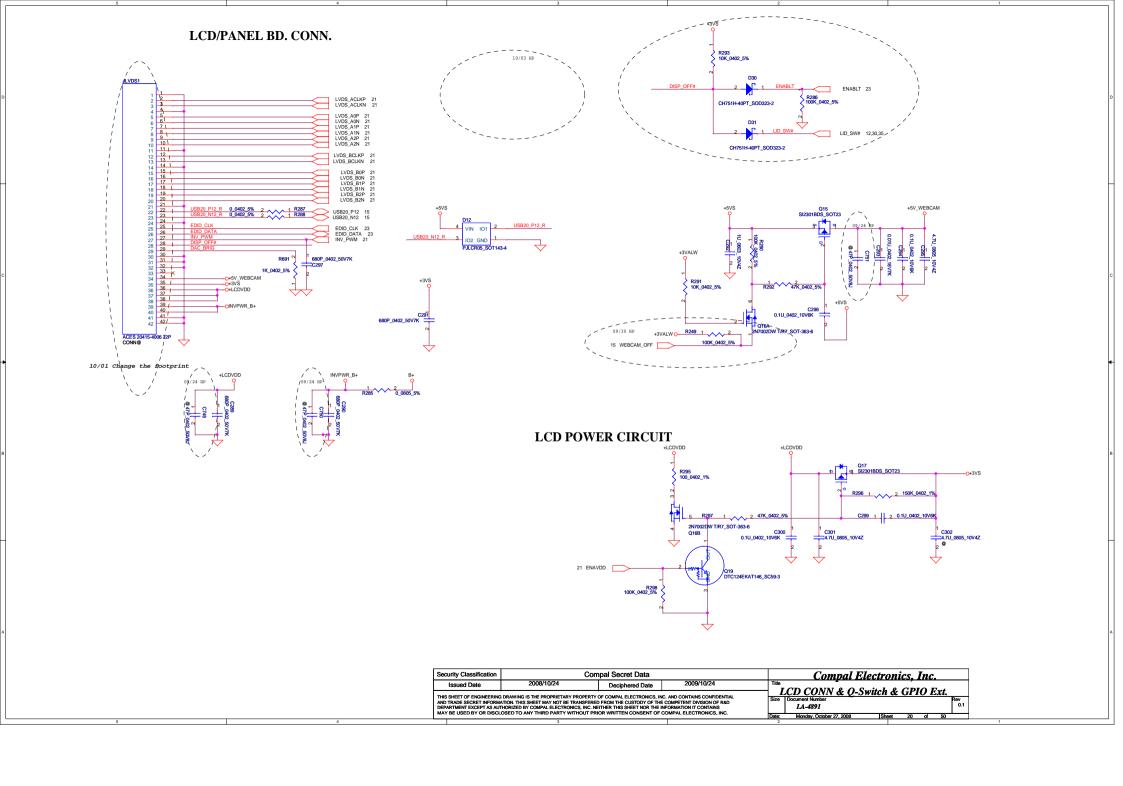






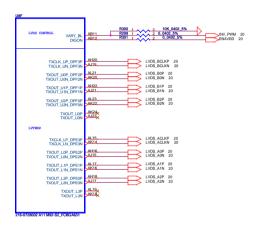
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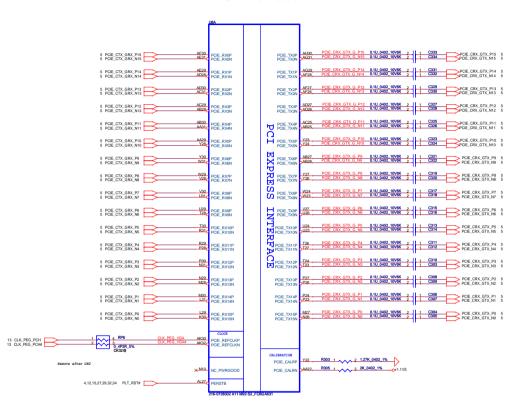




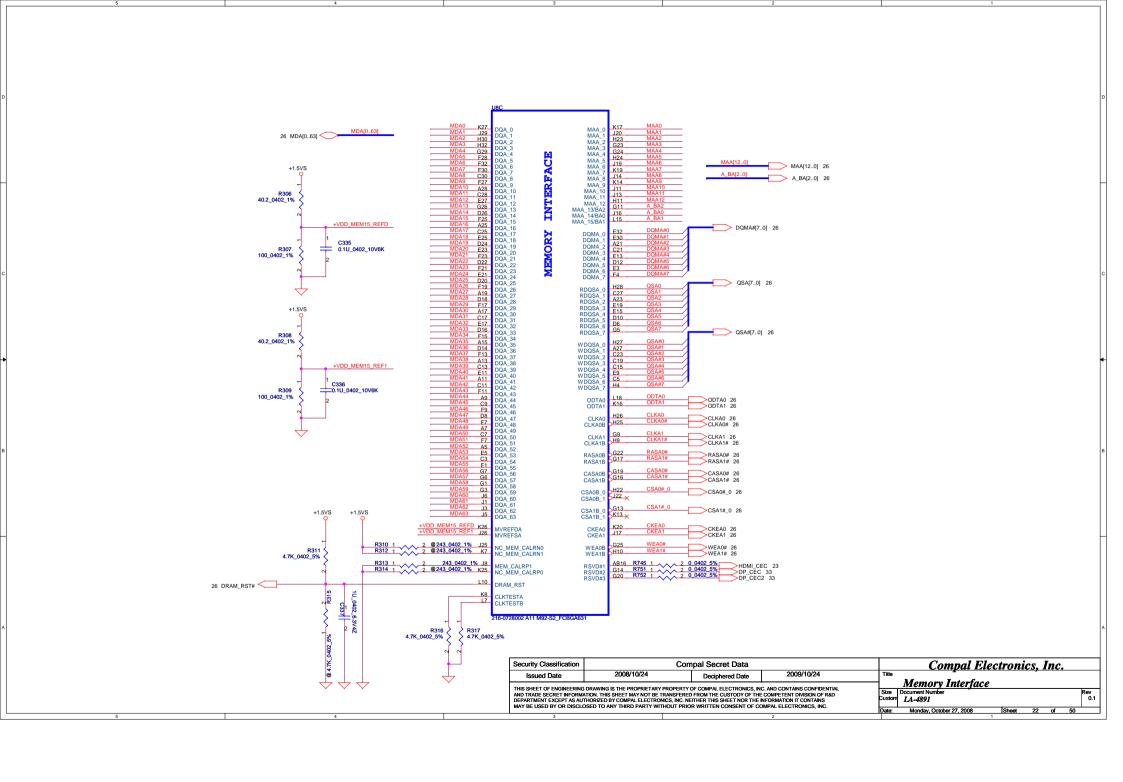
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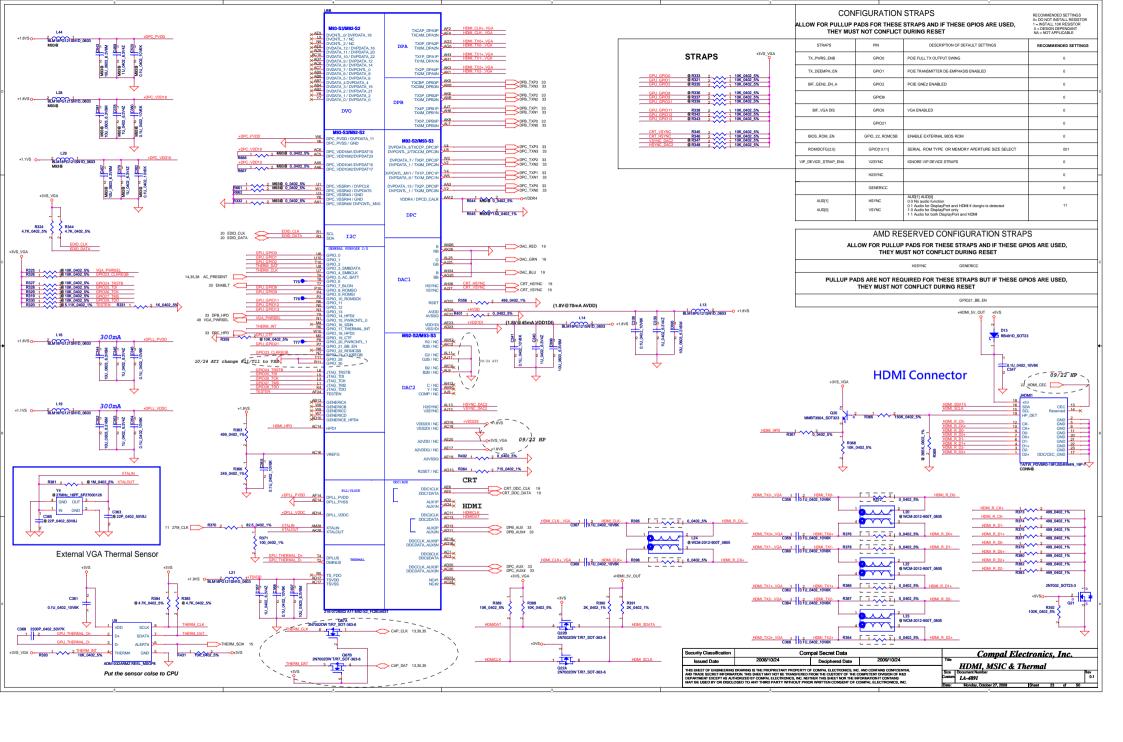
LVDS Interface

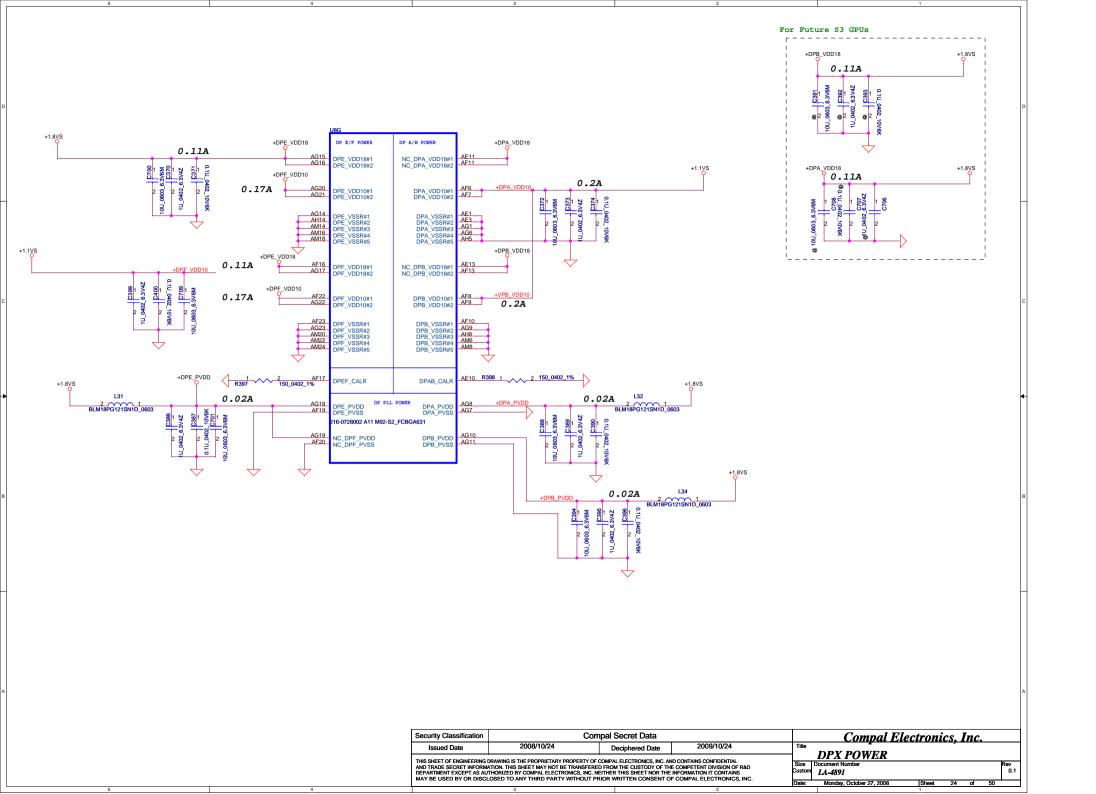


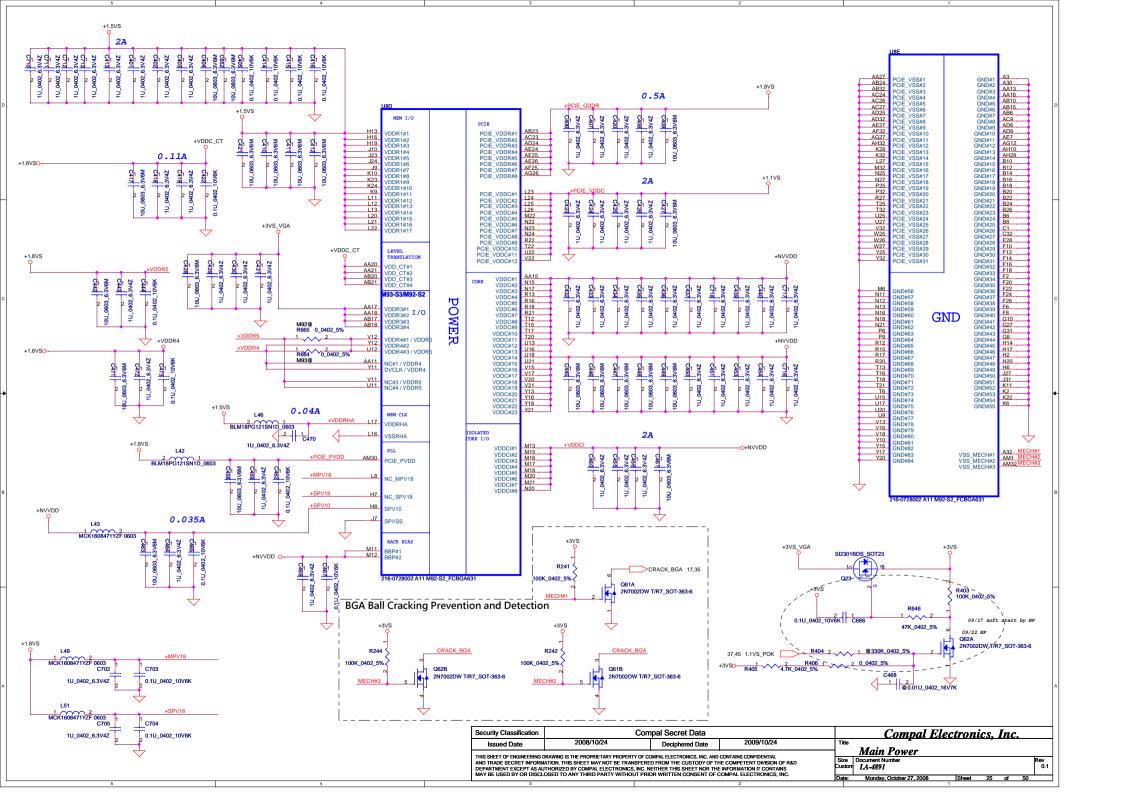


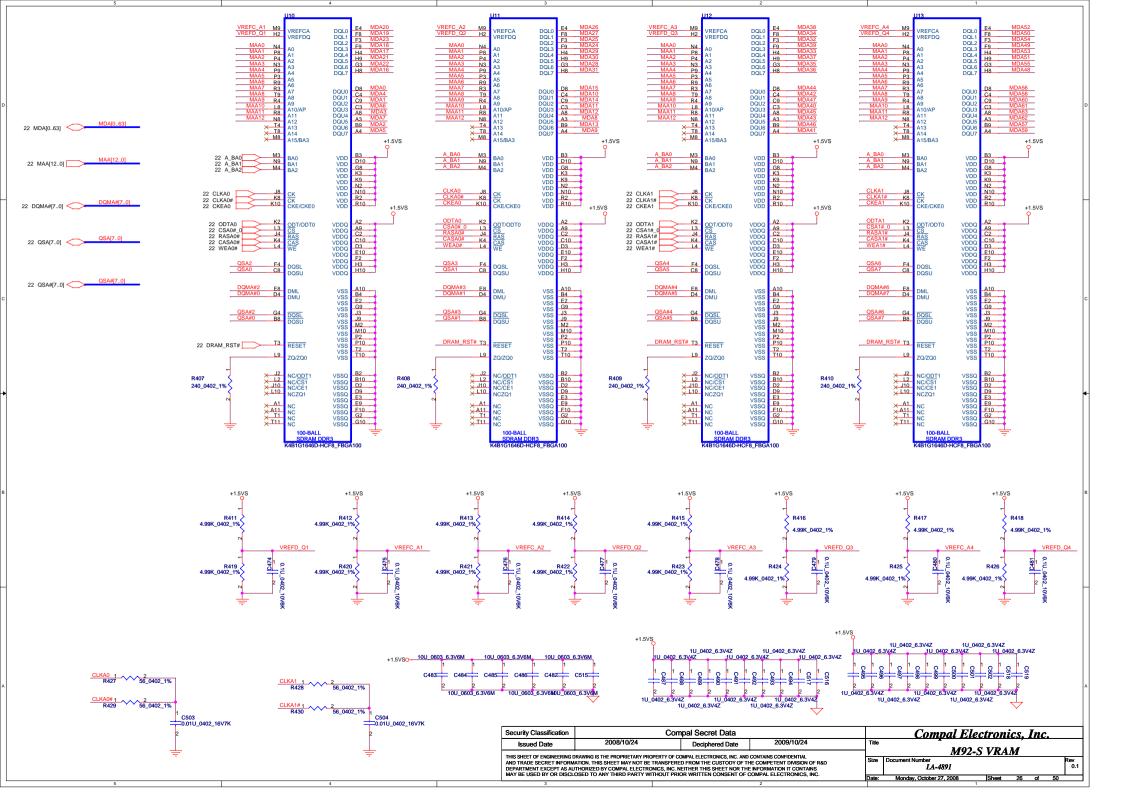
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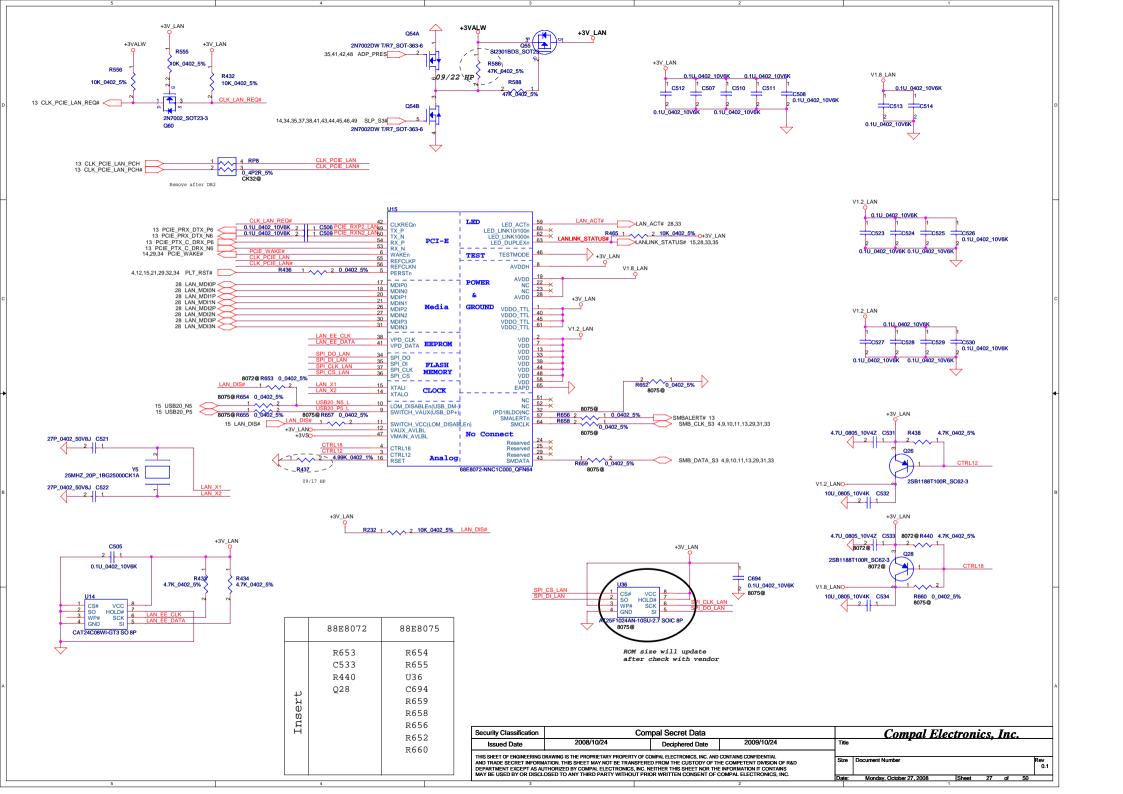


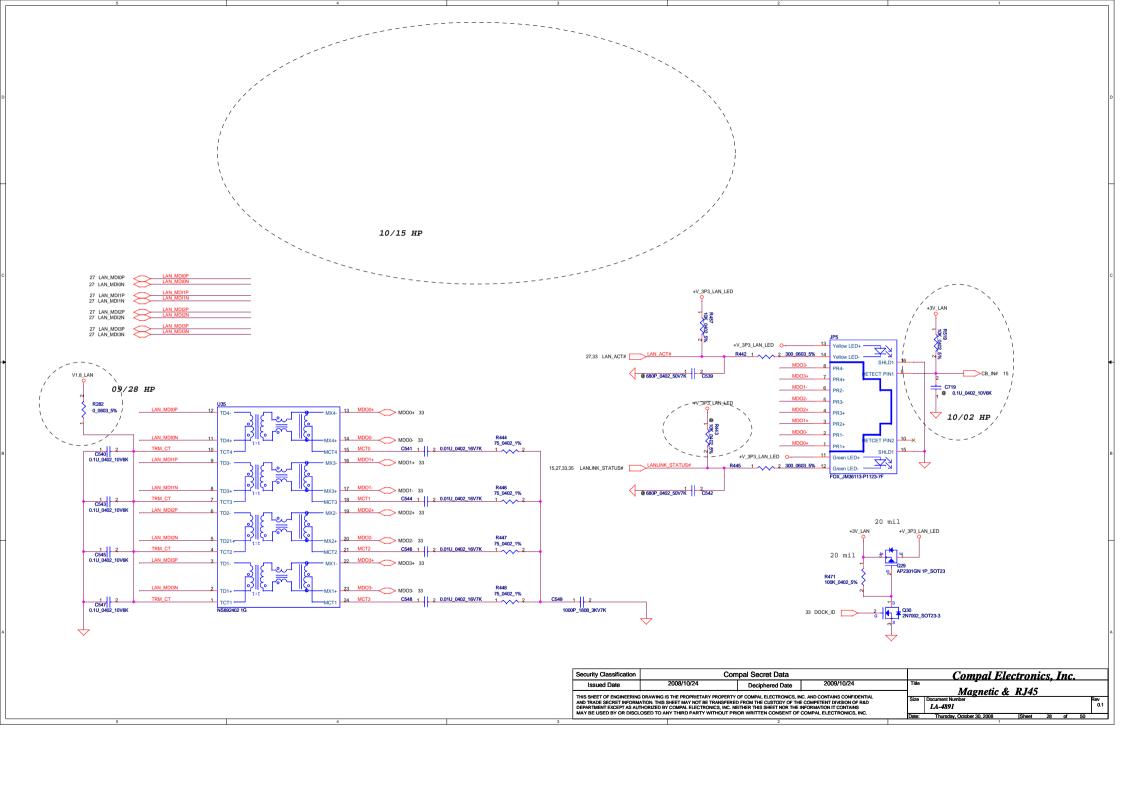


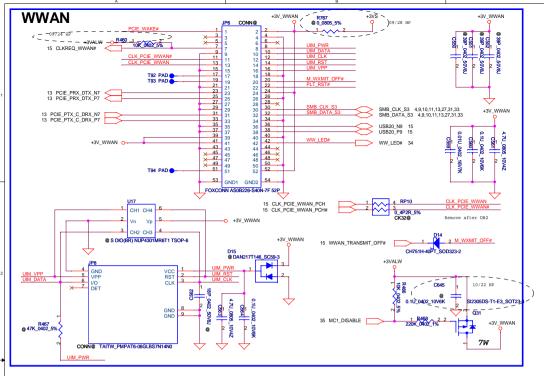


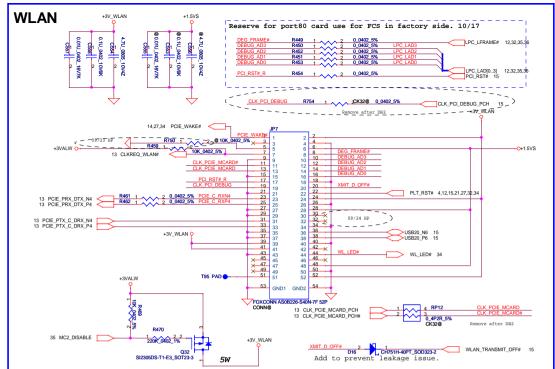


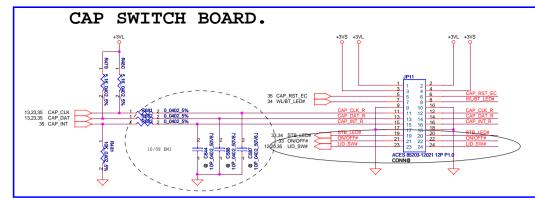


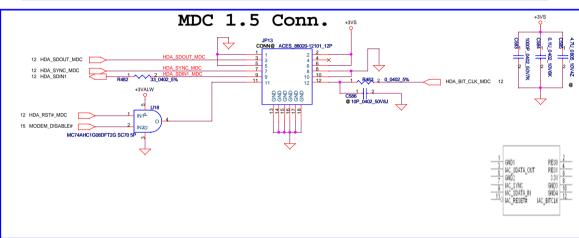


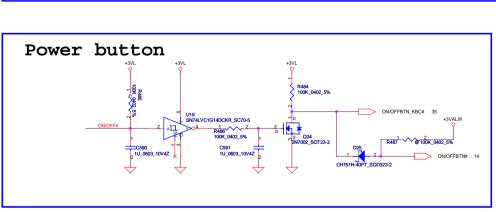


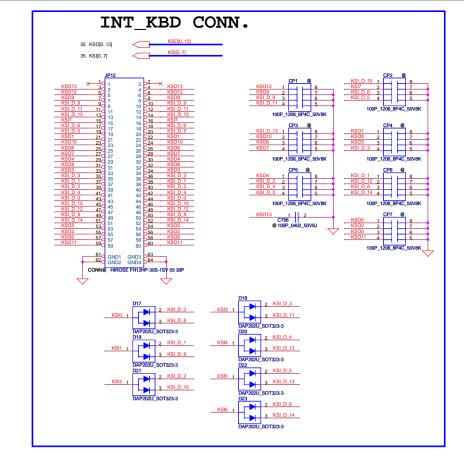


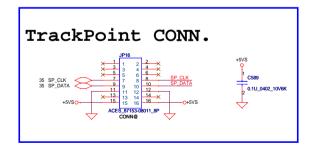




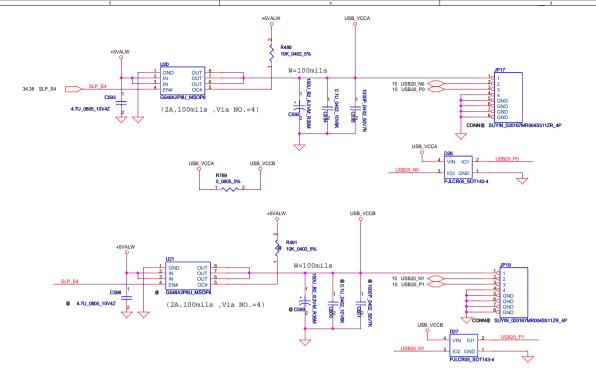


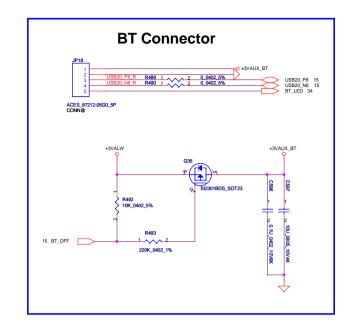


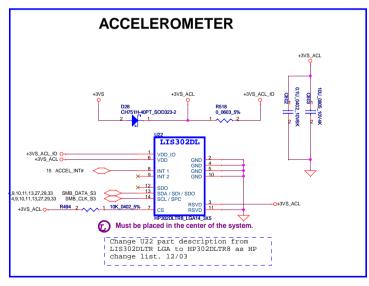




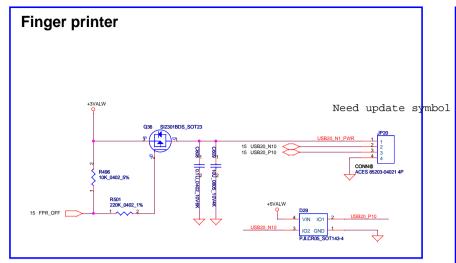
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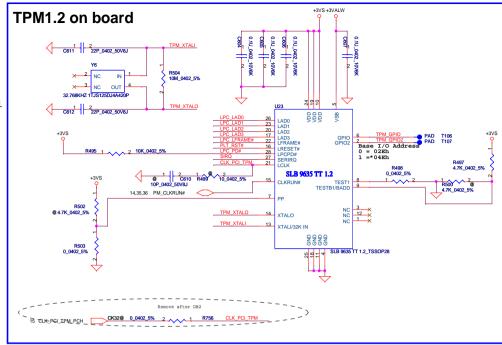


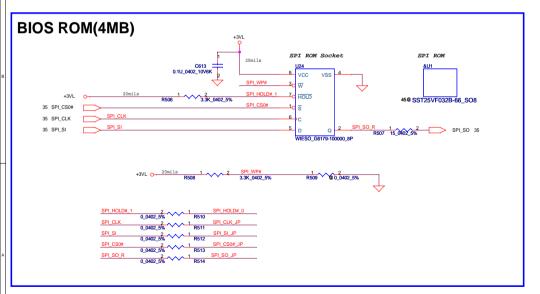


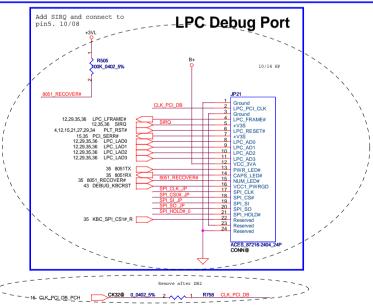


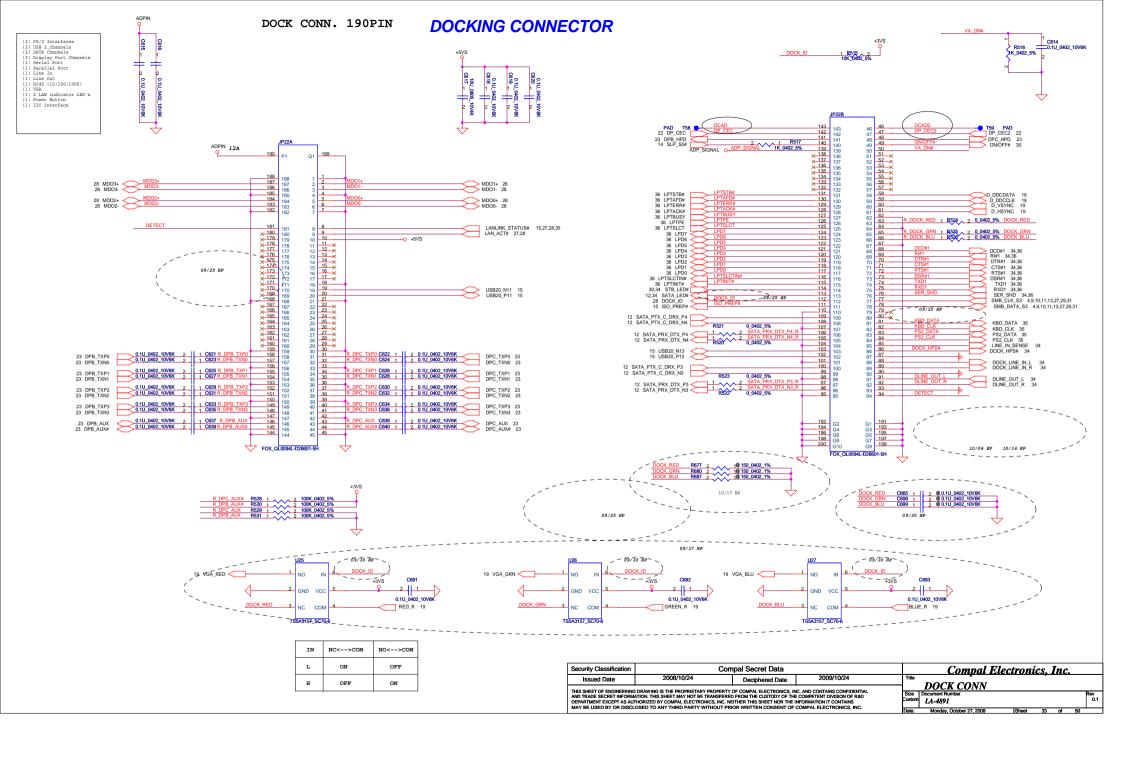
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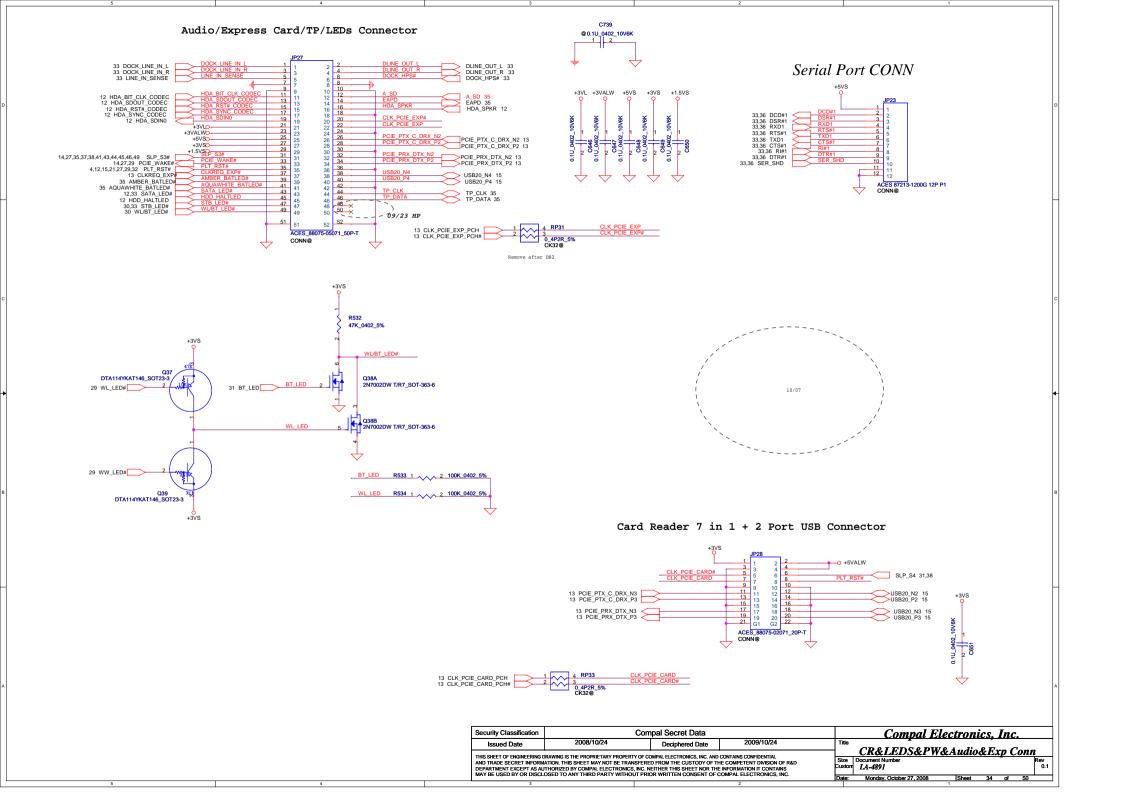


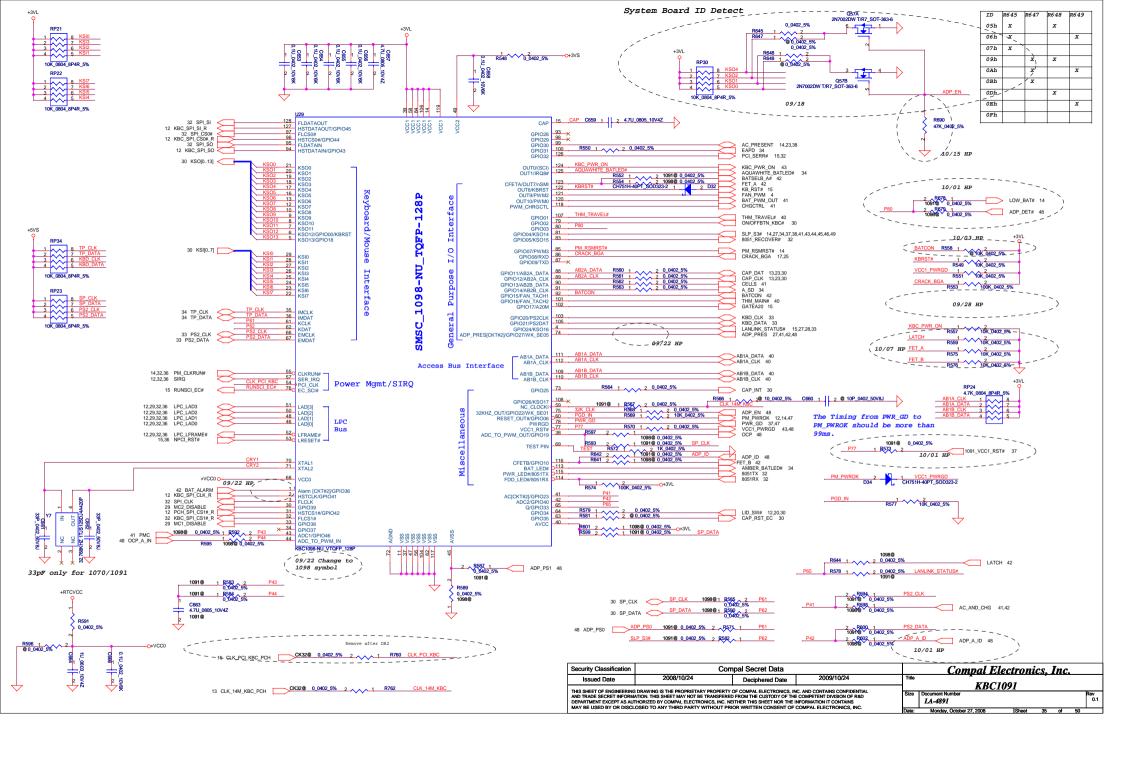


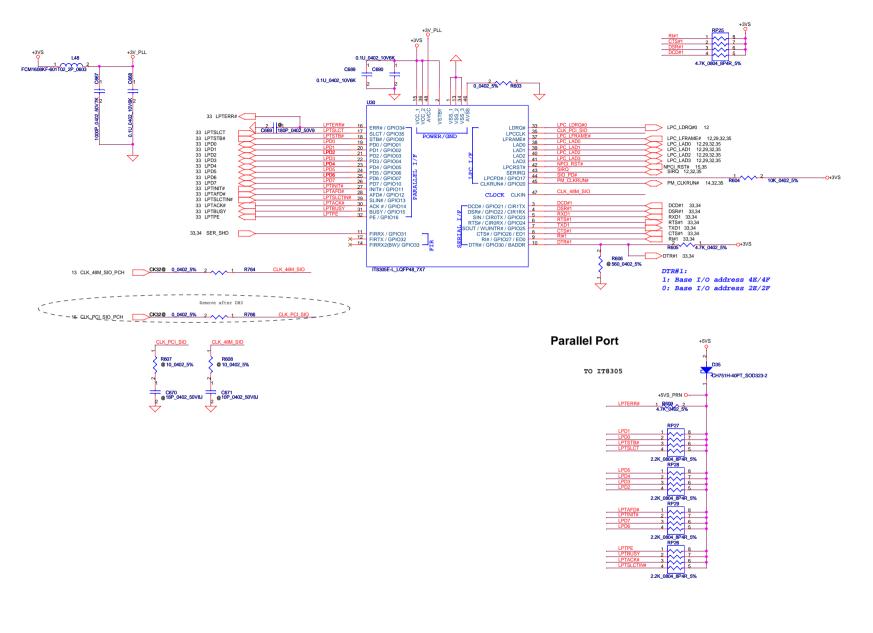




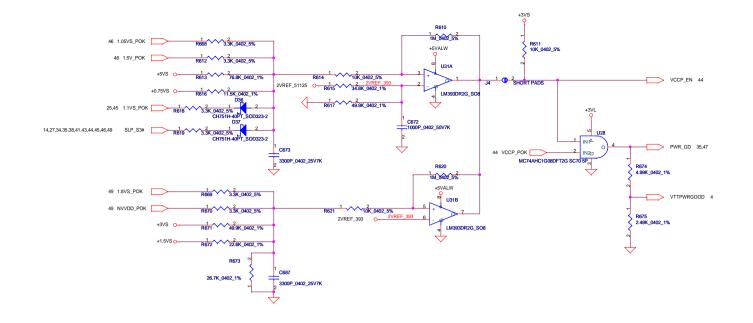


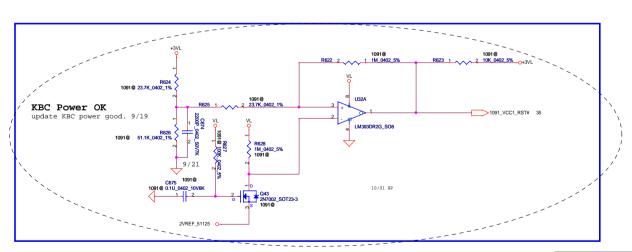


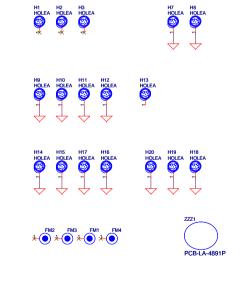




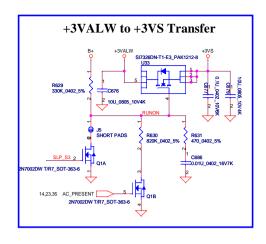
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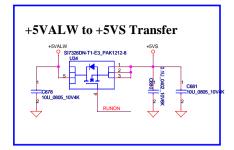


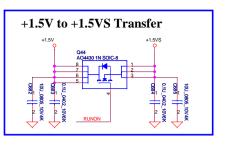


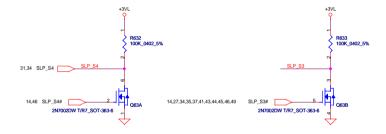


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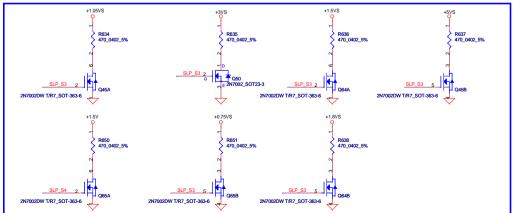




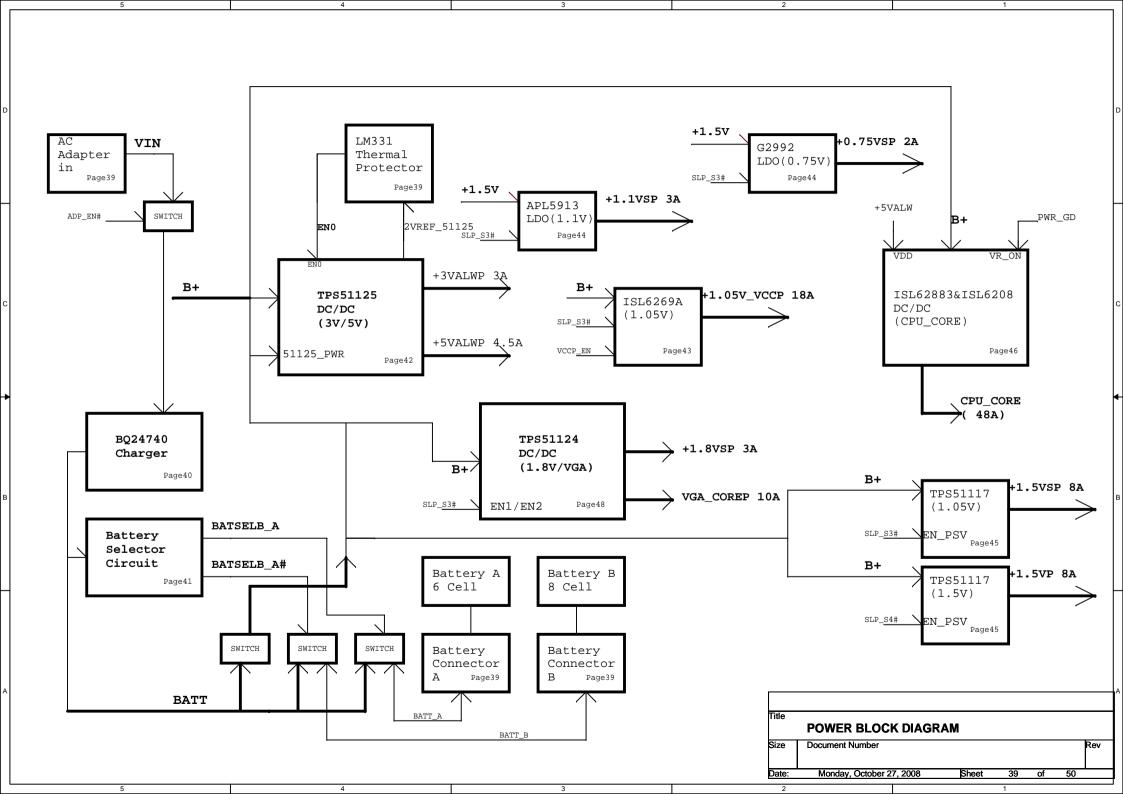


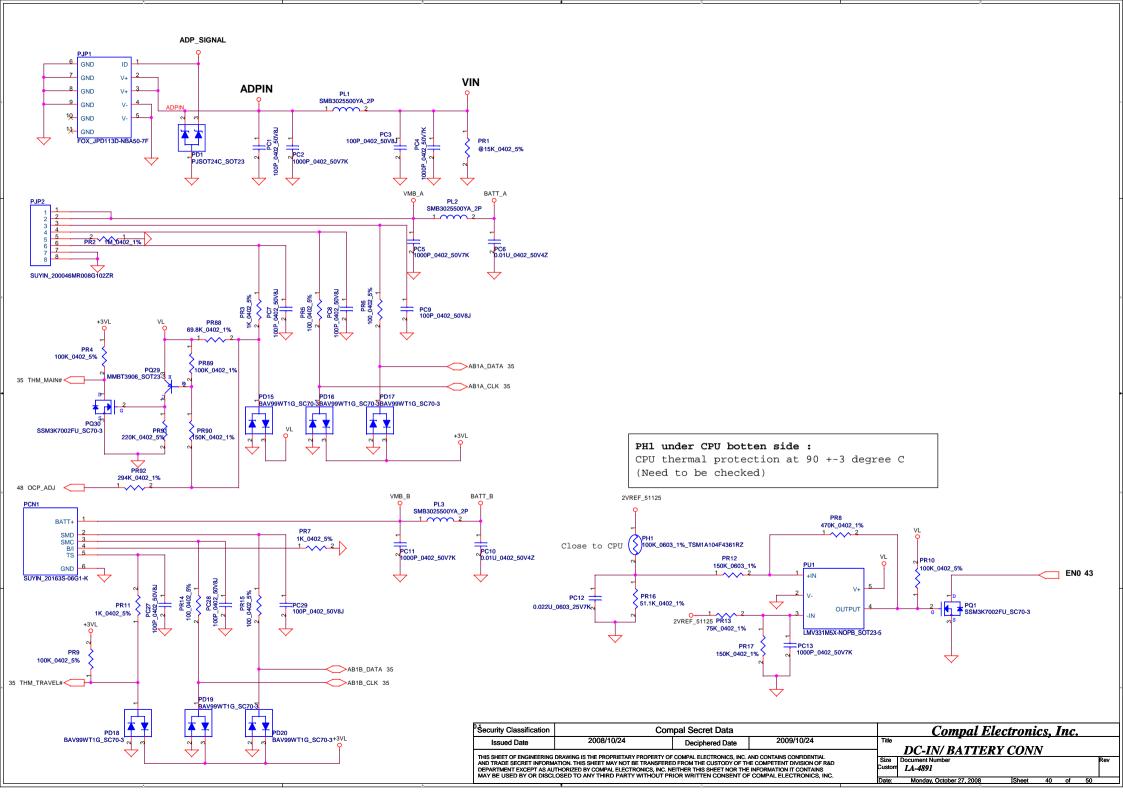


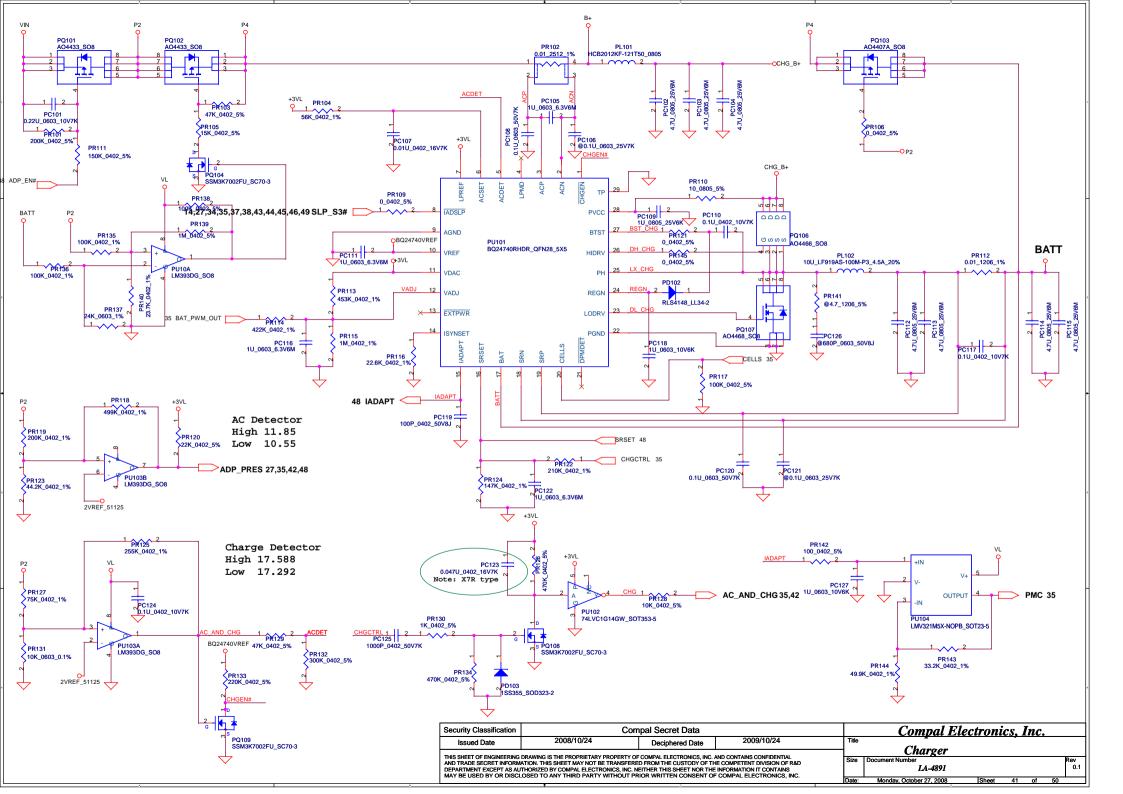
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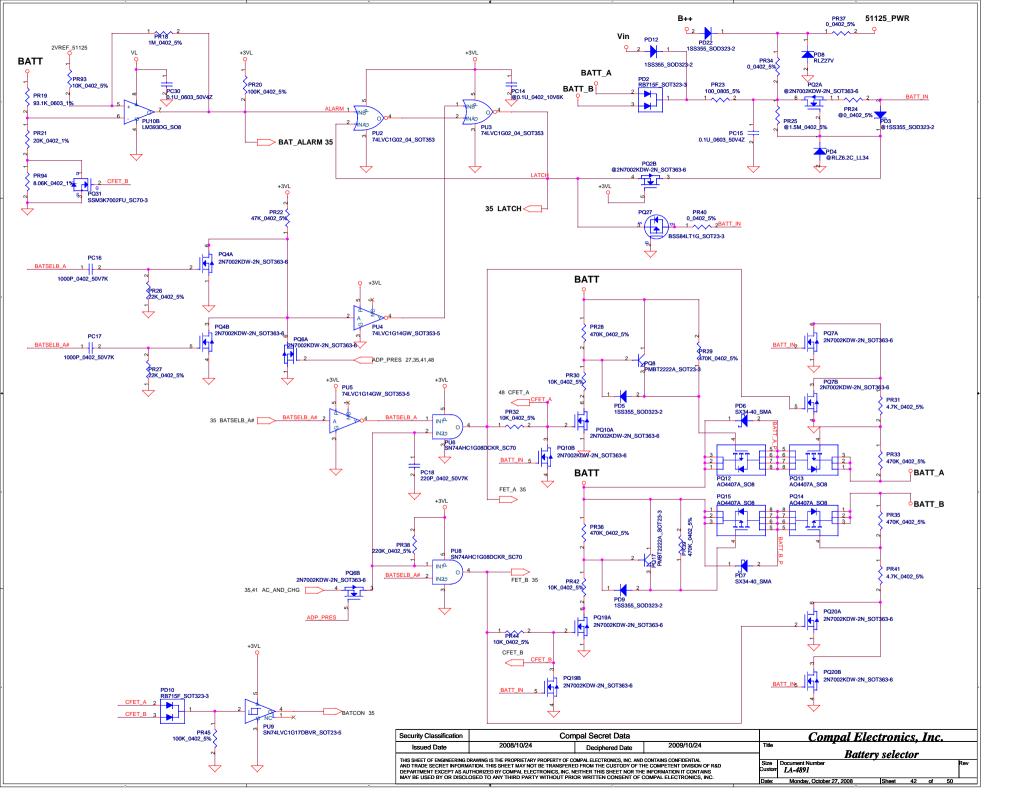


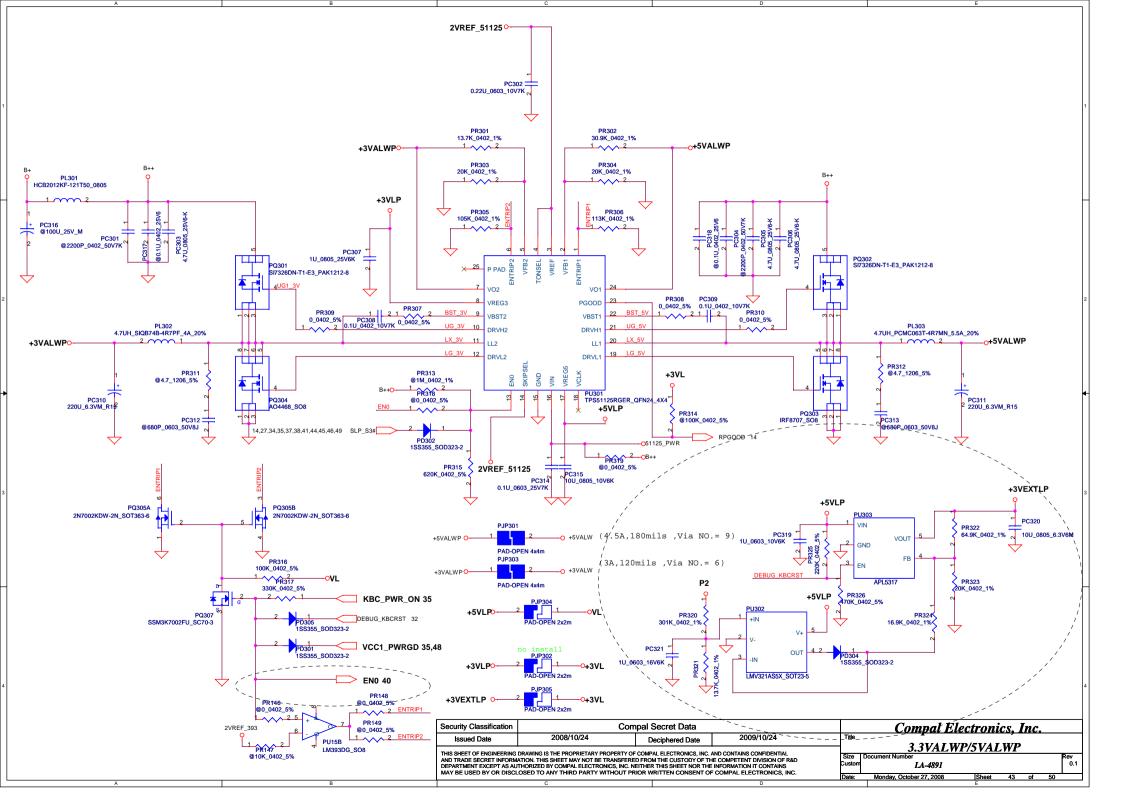
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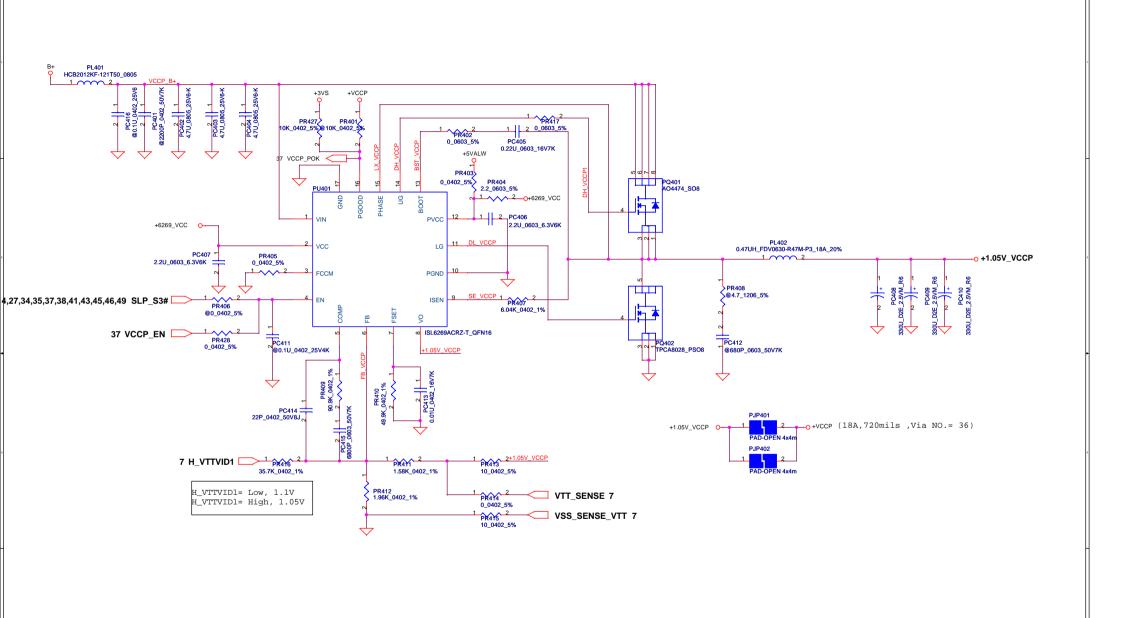




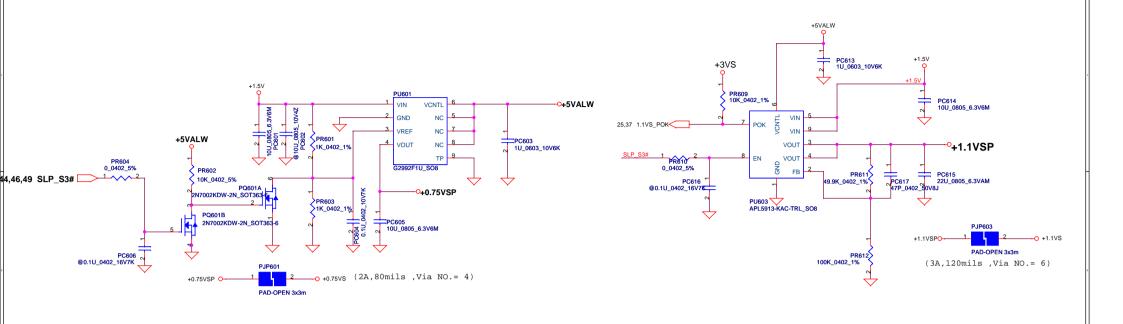




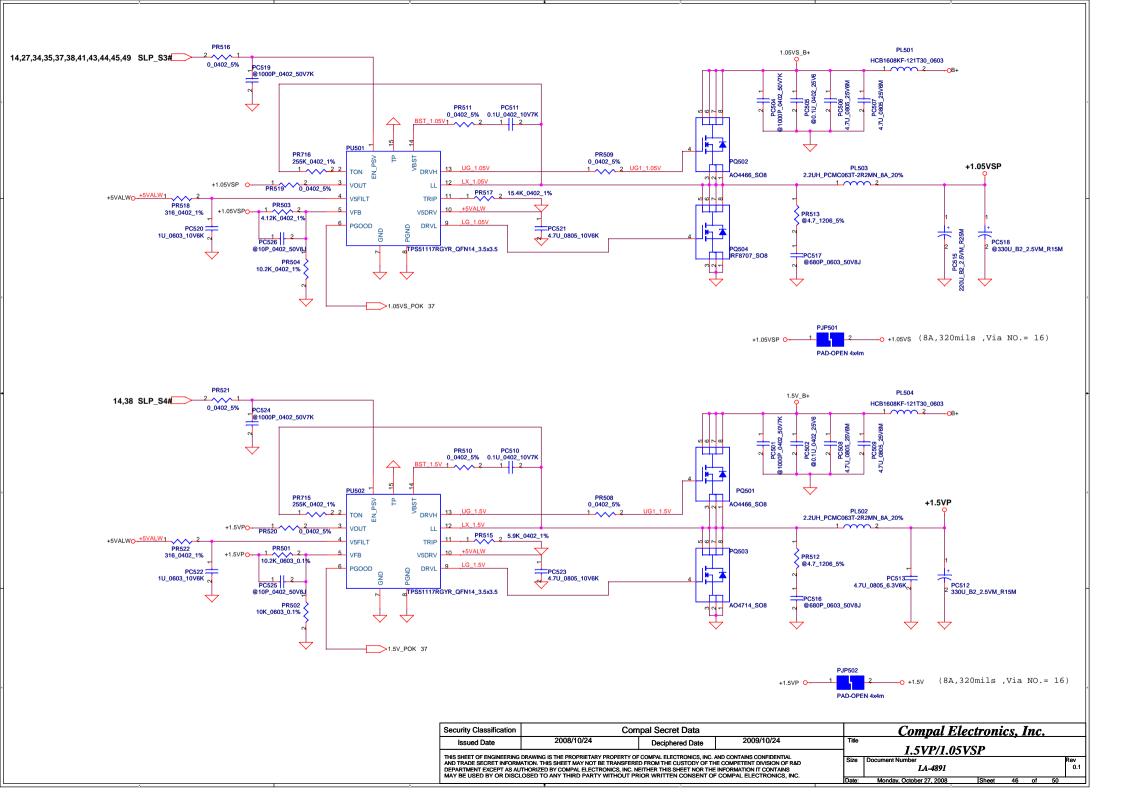


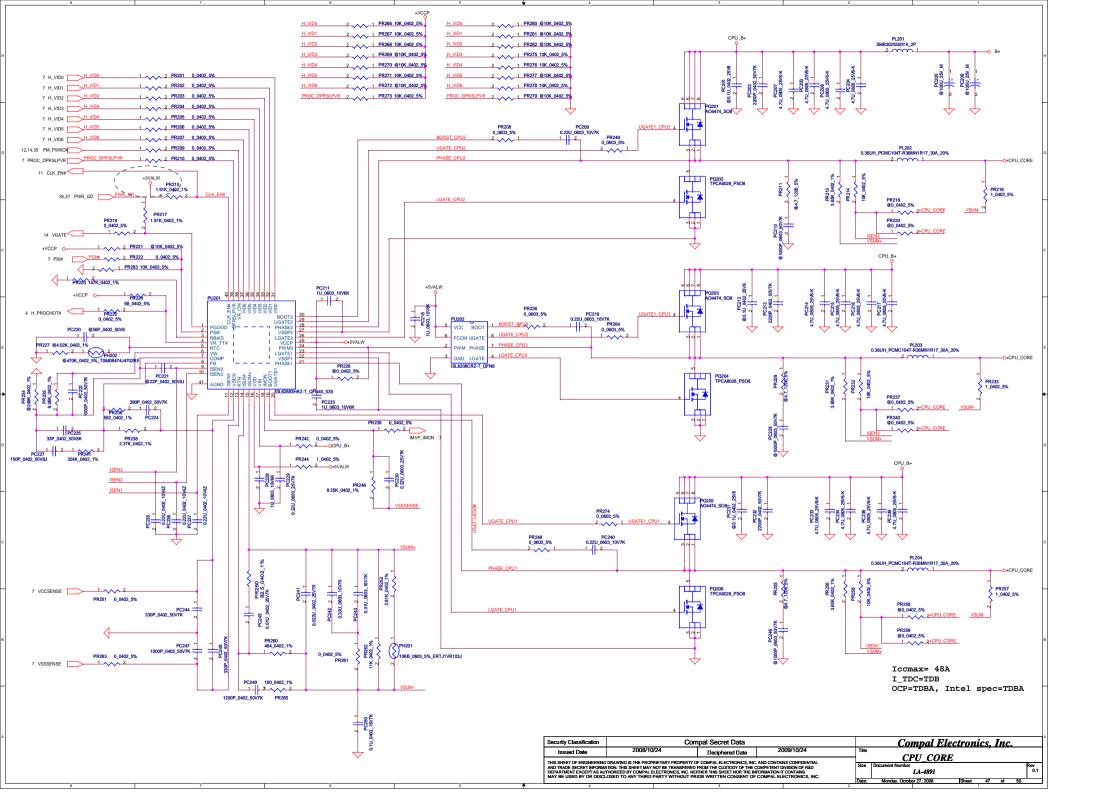


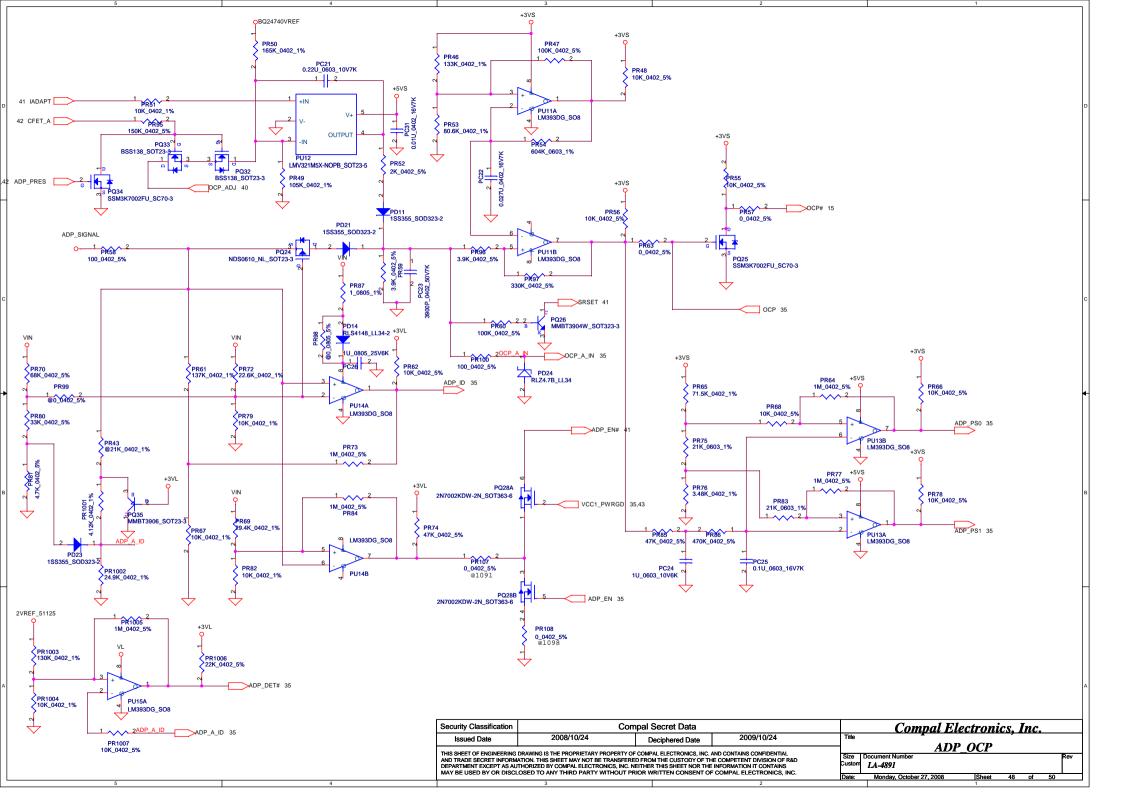
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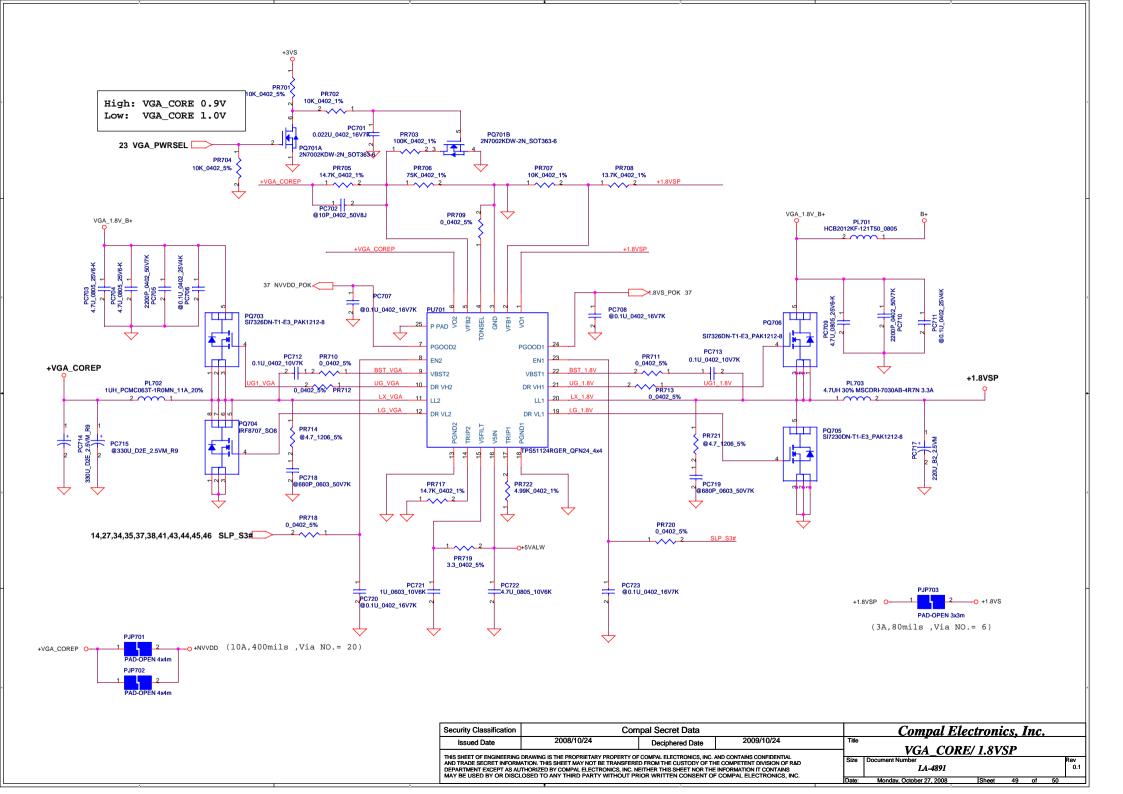


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Item	Reason for change	PG#		Modify List		Date	Phase
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