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# Performance Analysis of Fixed Point FIR Filter Architectures

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***Abstract*—In digital signal processing and communication systems, FIR filters have important role. One of the main challenges in Very Large Scale Integration(VLSI) signal processing is the FIR filter structure with optimized parameters. These filters made up of many adders and multipliers. In FIR filter, multiplier consumes high amount of power. The most important three areas in VLSI are power, area, and delay. This paper compares different types of fixed point FIR filter architectures and analyze the different perfomance parameters such as area, hardware utlization and delay. Different FIR filter architectures such as the conventional method, systolic architecture, associativity transformation and combination of systolic and associativity transformation architectures are considerd. We implemened a 4, 8 and 16 tap filters using the above mentioned architecures and compared their perfomance characteristics.**

***Index Terms*—Associativity, FiR filter, Systolic architecture, Systolic architecture with Associativity tarnsformation.**

## I. Introduction

FIR filters are broadly used in digital signal processing (DSP) applications. The difficulty of implementation increases with the filter order and computational accuracy. Realizing these filters in real time is a challenging task with the desired accuracy level [1]. Design optimization of one- and two-dimensional, fully pipeline computing structures for area-delay-efficient implementation of FIR filters by systolic decomposition of internal product computation based on distributed arithmetic (DA) performed. FIR filter can be used in many VLSI applications, such as applications in device detection using adaptive noise cancellation technique [2]. Systolic designs are an appealing architectural model for the efficient implementation of computation-intensive DSP applications with features such as simplicity, regularity and structure modularity. These also have considerable potential to deliver high-throughput through the use of high-competitiveness through pipeline or parallel processing or both. Many algorithms and architectures available in the literature for customization of FIR filters to leverage the advantages of systolic processing. However, multipliers need a significant portion of the chip area in these systems, thus reducing the maximum number of processing elements (PEs) and the highest filter order that can be accommodated. [1].

The fixed-point coefficients are modeled and represented in integer forms, binary forms, or canonical sign digit (CSD) forms. The fixed-point coefficients are then realized by method of subexpression sharing (CSS), or by a graph method that reduces the complexity of the hardware. A standard subexpression is defined among coefficients and processed only once. Thus, the number of adders can be reduced [3]. Multipliers with DA have significant popularity because of high-throughput processing capability, cost-effectiveness, and area-time sensitive computing structures [1].

## II. Litrature Review

Many FIR filter architectures are available in the literature, some of them are discussed in this section. A discrete space optimization technique was proposed for designing FIR filters with orders up to 256 in [4]. Their algorithm can be used to design filters that meets minimax requirements by changing the least square error weighting function. Another algorithm proposed by [5] was for the design of low-power and hardware-efficient linear-phase FIR filters.The algorithm identifies filter coefficients with a reduced number of signed-power-of-two (SPT) words given the filter frequency response characteristics. M.Potkonjak et.al [6]proposed an algorithm for solving the problem of multiple constant multiplications by using the technique of minimizing the number of operations in linear transformation and polynomial calculation.R.I.Hartley [7] proposed an alogotitm to imporve the CSD srchitecture by sharing the subexpressions to get 50 percntage reduction in total no operations. J Yli-Kaakinen and T Saramaki [8] proposed an algorithm in which the number of adders and subtractors are reduced by using a linear programming algorithm and finding the filter coefficients with the simplest coefficient representation. In [9] FIR filters with high-throughput and low-latency systolic structure.The input and output sequences are in bit-parallel LSB-first bit-skewed form, and the propagation delay of a complete gated adder and a latch limits the throughput. The bits of a full-bit sample start from the array three clock cycles after the bits of the respective input sample reach the array. L F Chao [10] proposed a transformation algorithm in which cyclic data-flow (DFG) graph, in which nodes represent operations, represents an algorithm with precedence relations between iterations.

Another algorithm proposed by [11] was a nonrecursive signed specific subexpression elimination (NR-SCSE) algo-

rithm that recursive use of a specific subexpression creates a high degree of complexity in the digital structure, the NR-SCSE algorithm enables the designer to overcome this problem by using subexpression space once. S S Jeng,H Chen Lin and S M Chang [12] proposed an architecture that symmetry filter is used for parallel-distributed M-bit arithmetic (M-bit PDA). In this architecture, the pre-calculated partial product is stored in the distributed RAM that reduces hardware required for multiplication hence it consume less area and power. The algorithm proposed by [13] based on mixed-integer linear programming (MILP), finds the minimum number of adders being implemented. In this, discrete coefficients are synthesized by continuously updated subexpression space. L D Van [14] proposed a 2-D systolic filter implementation algorithm that uses the same number of multipliers with lesser quantization error and zero latency.H Yin et.al [15] proposed a systolic array design folding theory which gives an increased throughput with a reduction of hardware. The FIR filters with a high-level transformation technique are taken into account in this paper to compare the delay, power, and area. Systolic architecture, along with the transformation of associativity, are the methods of transformation considered here.

## III. System Overview and working

A digital filter uses a finite number of bits to describe signals and coefficients. Stractures are required which can somehow retain the target filter specifications even after quantizing the coefficients. Conventional FIR filters require blocks such as adders, multipliers, and delay for constructing it. In the case of 4 Tap filter three adder blocks, three multiplier blocks and four filter coefficients are needed to construct it. Let x be the input of the filter, h be the filter coefficients,T be the delay, M will be the mulplier and a be the adders.Then for an N tap filter $h_0, h_1, h_2, ..., h_n$ filter coefficients, $A_0, A_1, ...., A_n - 1$ adders, $M_0, M_1, ...., Mn - 1$ multipliers and $T_0, T_1, , ....., T_n$ delay units are needed [2]. A 4 tap Conventional FIR filter is shown in Fig 1 and the simulation results of 4 tap, 8 tap and 16 tap filters are shown in Table 1.

The systolic decomposition scheme provides a versatile choice of the look-up-tables (LUT) address length for DA based computation to decide on the correct area-time trade-off. One way systolic pipeline array is possible to reduce the memory size by using smaller address lengths for DA-based computing units but on the other hand this compromises on complexity and delay [9]. Two-way systolic pipeline array has immediate response but includes the zero-word interplay between successive samples, both input and output sequences [1] [9]. The systolic architecture comprises several processing elements (PEs) that calculate and transfer data.We can get an array that combines two adjacent PE arrays to one. The operation of each PE performed by the new array is deduced from array operation over two consecutive operation cycles [9]. Fig.2 shows a 4 tap FIR Sytolic filter and the implenetion details of 4,8 and 16 tap filters are given in Table1

In the associativity transformation technique, a program is converted into a data flow graph to show the parallel in the description given. Every node in a data flow diagram belongs to an operation such as add and multiply [10]. The associativity technique can be used to reduce hardware utilization compared to the systolic architecture or conventional FIR architecture [2]. Fig.3 shows a 4 tap FIR filter architecture implementation using the associativity transformation technique.

Systolic architecture with associativity can be a better solution in which the critical path can be reduced with systolic architecture and the hardware utilization can be improved with the associativity transformation [2]. Fig 4 shows a 4 tap systolic with associativity transformation fixed-point FIR filter which utilizes the advantage of the systolic architecture and associativity transformation algorithm.

## IV. Experimental Results

The performance parameters such as Power consumption, hardware utilization, and delay of the different FIR filter architectures are simulated using Vivado design suite 2019.2 and results are listed in Table 1.

*1) Conventional FIR filter:* Conventional FIR filter with 4,8 and 16 tap are implemented and simulated and the performance parameters are observed. The FIR filter with 4 taps having a power consumption of 0.223 W and a delay of 16.034nS. The number of LUTs is 22 and slice resisters are 46. In the case of the 8 tap filter, the power consumption is 0.266 W and the delay is 26.045 nS. LUTs and slice registers used are 23 and 56 respectively. For a 16 tap filter the power consumption and delay are 0.458 W and 30.356 nS respectively. The hardware utilization is about 28 LUTs and 62 slice registers.

*2) Systolic FIR Filter:* Systolic FIR filters are implemented and simulated with 4,8 and 16 tap and the output parameters are observed. The FIR filter with 4 taps having a power consumption of 0.282 W and a delay of 12.065nS. The no of LUTs is 22 and slice resisters are 25. In the case of the 8 tap filter, the power consumption is 0.326 W and the delay is 20.066 nS. LUTs and slice registers used are 23 and 28 respectively. For a 16 tap filter the power consumption and delay are 0.688 W and 26.465 nS respectively. The hardware utilization is about 26 LUTs and 32 slice registers.

*3) Associavity transformation :* Associavity transformation FIR filter with 4,8 and 16 tap are implemented and simulated and the performance parameters are observed. The FIR filter with 4 taps having a power consumption of 0.227 W and a delay of 06.088ns.The number of LUTs is 17 and slice resisters are 24. In the case of the 8 tap filter, the power consumption is 0.255 W and the delay is 10.106 nS. LUTs and slice registers used are 21 and 23 respectively. For a 16 tap filter the power consumption and delay are 0.96 W and 18.015 nS respectively. The hardware utilization is about 24 LUTs and 25 slice registers.

*4) sytolic with associavity FIR Filter :* systolic with Associavity transformation FIR filter with 4,8 and 16 tap are implemented and simulated and the performance parameters are observed. The filter with 4 taps having a power consumption of 0.127 W and a delay of 05.998ns.The no of LUTs is

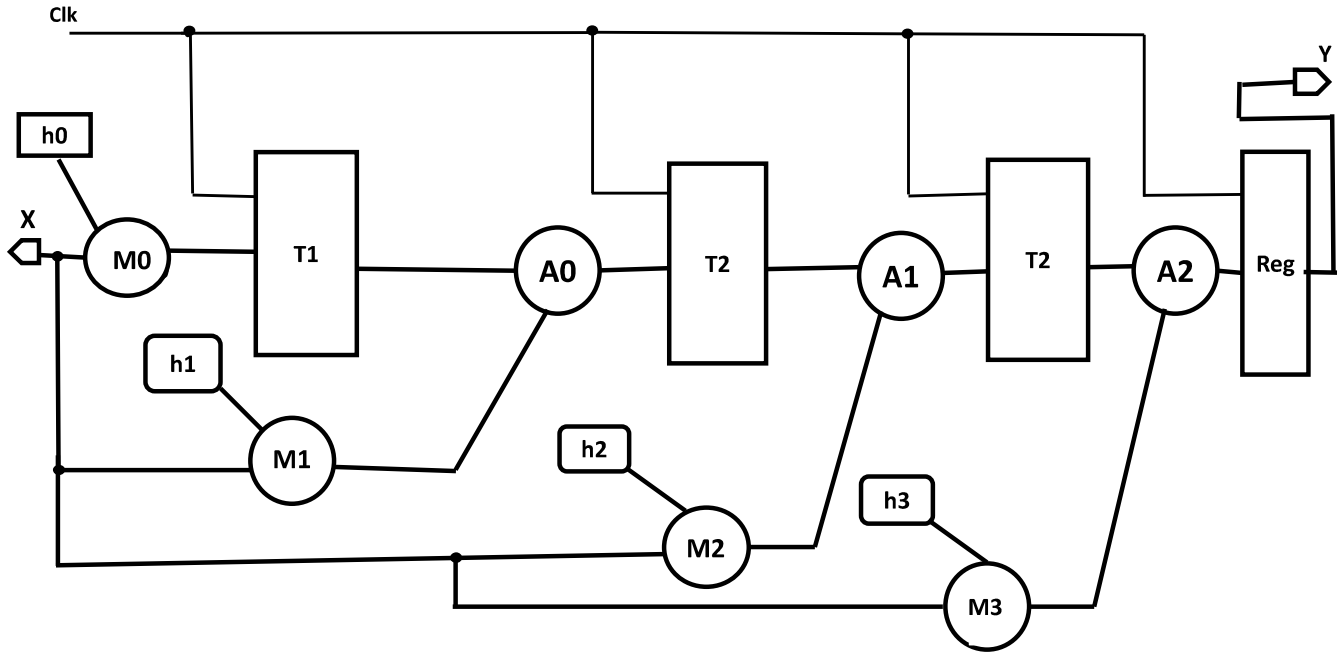


Fig. 1: Conventional FIR Filter architecture : $A_0, A_1, A_2$ are adders : $h_0, h_1, h_2.h_3$ are filter coefficients :$M_0, M_1, M_2, M_3$ are multipliers, $T_0, T_1, T_2$ are delay units: Similar notations are given for other figures also

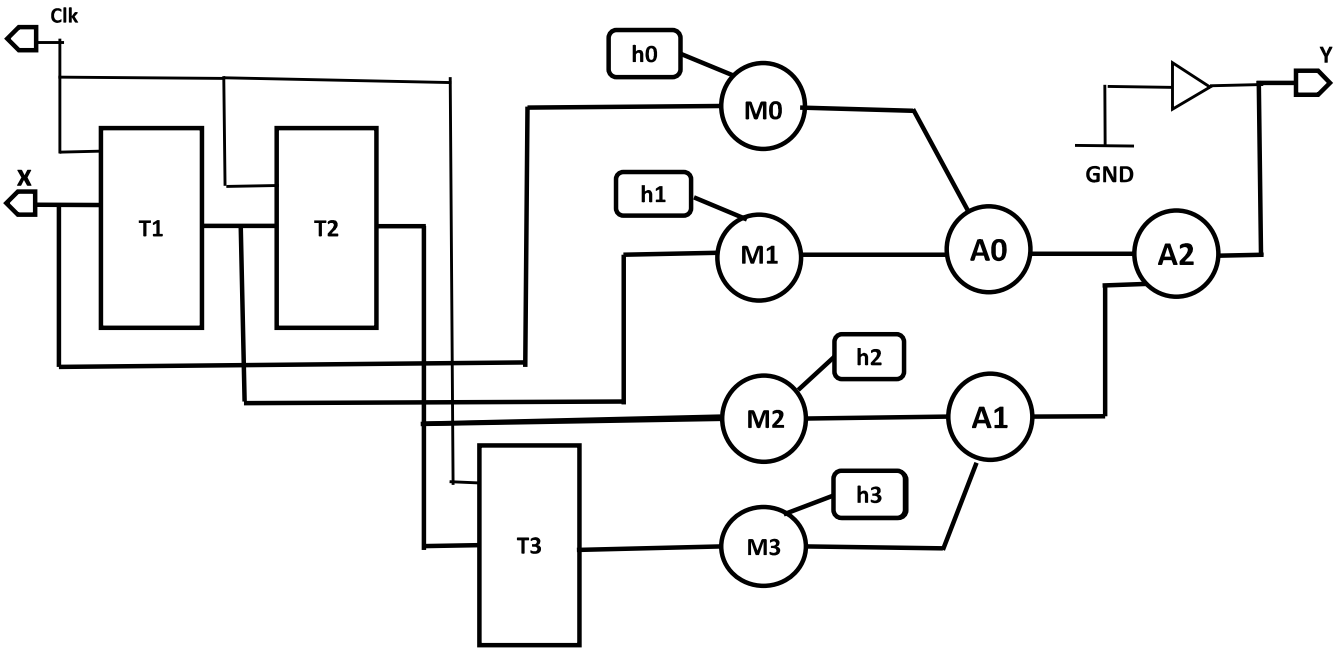


Fig. 2: Systolic FIR filter architecture

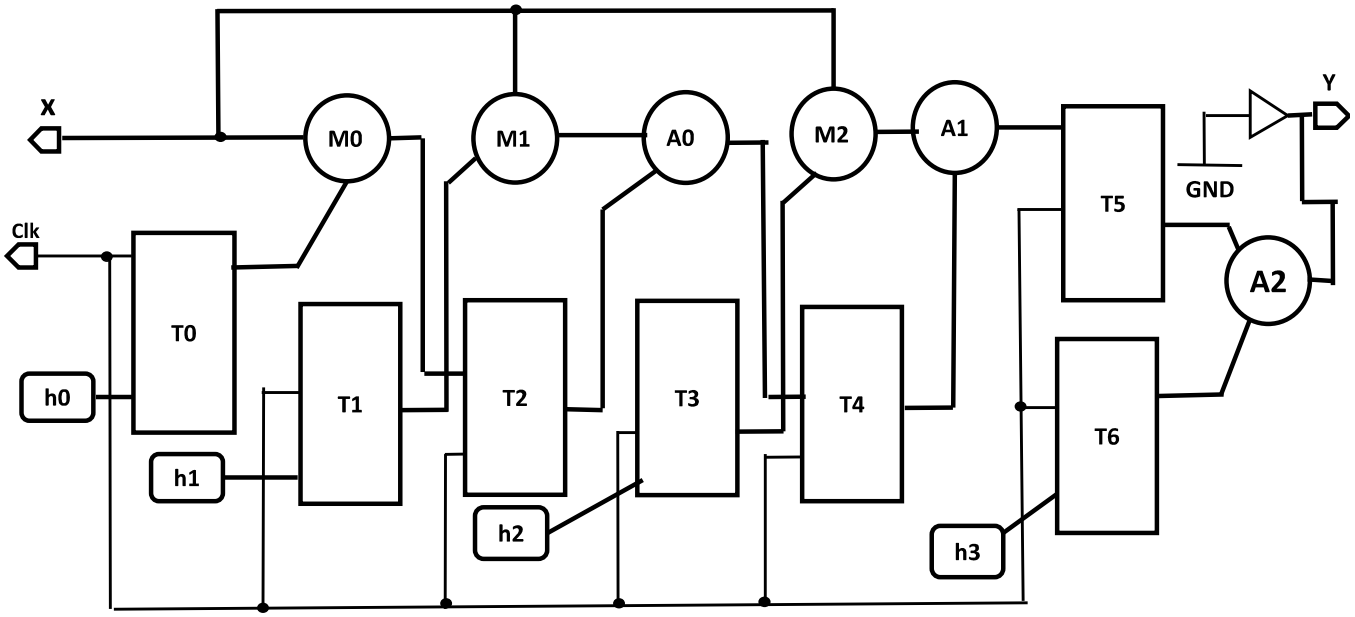


Fig. 3: Associavity transformation FIR filter

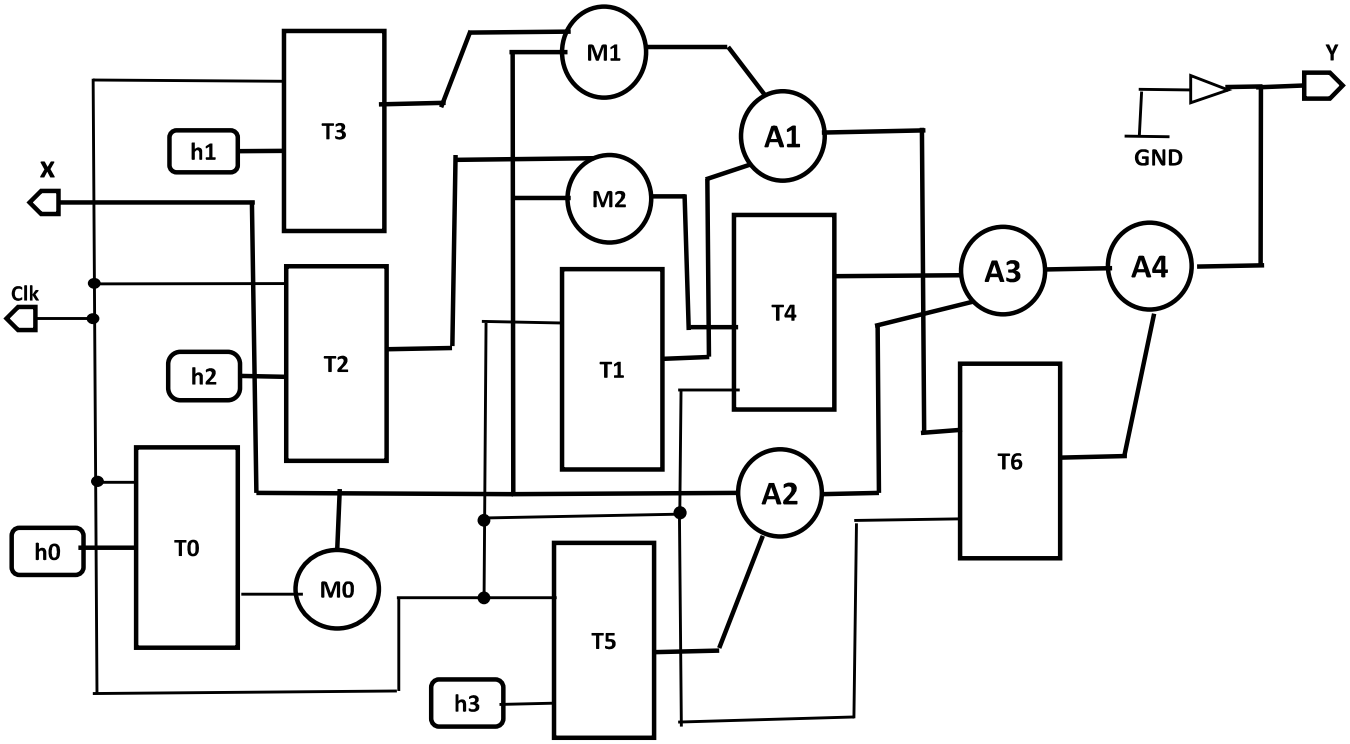


Fig. 4: systolic with Associavity transformation FIR filter

TABLE I: Performance comparison of FIR filter architectures

| Filter Architecture | 4 Tap | | | 8 Tap | | | 16 Tap | | |
|---|---|---|---|---|---|---|---|---|---|
| | Power (W) | Hardware utilization | Delay (nS) | Power (W) | Hardware utilization | Delay (nS) | Power (W) | Hardware utilization | Delay (nS) |
| Conventional | 0.223 | Slice LUTs : 22<br>Slice Registers: 46<br>Bonded IOB : 23 | 16.034 | 0.266 | Slice LUTs : 23<br>Slice Registers : 56<br>Bonded IOB : 23 | 26.045 | 0.458 | Slice LUTs : 28<br>Slice Registers : 62<br>Bonded IOB : 25 | 30.356 |
| Systolic | 0.282 | Slice LUTs : 22<br>Slice Registers : 25<br>Bonded IOB : 20 | 12.065 | 0.324 | Slice LUTs : 23<br>Slice Registers : 28<br>Bonded IOB : 20 | 20.066 | 0.688 | Slice LUTs : 26<br>Slice Registers : 32<br>Bonded IOB : 20 | 26.465 |
| Associavity | 0.227 | Slice LUTs : 17<br>Slice Registers : 24<br>Bonded IOB : 20 | 6.088 | 0.255 | Slice LUTs : 23<br>Slice Registers : 21<br>Bonded IOB : 20 | 10.106 | 0.496 | Slice LUTs : 24<br>Slice Registers : 23<br>Bonded IOB : 20 | 18.015 |
| Systolic with Associavity | 0.127 | Slice LUTs : 17<br>Slice Registers : 24<br>Bonded IOB : 20 | 5.998 | 0.240 | Slice LUTs : 23<br>Slice Registers : 21<br>Bonded IOB : 20 | 9.885 | 0.486 | Slice LUTs : 24<br>Slice Registers : 23<br>Bonded IOB : 20 | 16.185 |

17 and slice resisters are 24. In the case of the 8 tap filter, the power consumption is 0.240 W and the delay is 9.885 nS. LUTs and slice registers used are 21 and 23 respectively. For a 16 tap filter the power consumption and delay are 0.486 W and 16.18 nS respectively. The hardware utilization is about 24 LUTs and 25 slice registers.

Considering the systolic architecture with associavity transfomation it is clear that the hardware utilzation, delay and power are getting reduced.Better reduction of area, power and hardware ultization is achived with the combination of systolic architeture with associativity transformation.

## V. Conclusion

The article presents the implementation of different types of fixed-point FIR filter architectures. The power consumption hs a vital role in energy saving and the increase in speed provides better system performance. The major performance parameters such as power, hardware utilization, and delay in 4, 8, and 16 tap of various fixed-point FIR filter architectures are simulated. The systolic architecture with associativity transformation architecture provides better outcome in contrast to the other architectures. The aforesaid architecture gives better results in terms of power consumption and delay.The simulation results shows 33% power-saving and 5% speed improvement in systolic architecture with associativity transformation compared to associativity transformation in the case of 4 tap filter implementation. Similary the power consumtion and speed increase in 8 tap filter with the same arctitecture is 22% and 4% respectively, for 16 tap filter it is 12% and 4% respectively.

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