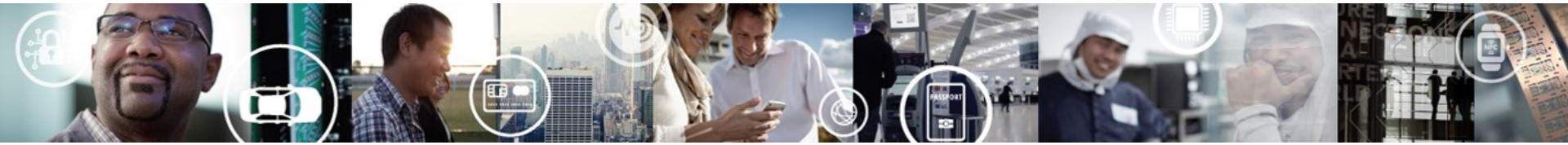
LPC82X 培训资料

省电模式

MAY, 2016



内容

- 低功耗模式
- 低功耗模式相关配置
- 如何进入低功耗模式

低功耗模式

LPC82x 低功耗模式

- LPC82x 支持4种低功耗模式:
  - 睡眠模式（Sleep Mode）
    - 典型功耗值 Idd: 1.85mA
    - 测试条件：system clock = 12 MHz; default mode; Vdd=3.3v
  - 深度睡眠模式（Deep-Sleep Mode）
    - 典型功耗值: 160uA
    - 测试条件： Vdd=3.3v
  - 掉电模式（Power-down Mode）
    - 典型功耗值: 1.6uA
    - 测试条件： Vdd=3.3v
  - 深度掉电模式（Deep Power-down Mode）
    - 典型功耗值: 0.2uA
    - 测试条件： Vdd=3.3v
    - 10 kHz LP oscillator 和 self-wake-up timer (WKT) 处于关闭状态

LPC82x低功耗模式 –睡眠模式（Sleep mode）

- 睡眠模式（Sleep mode）:
  - –通往内核的系统时钟停止工作
  - –处理器的状态和寄存器、外设寄存器和内部SRAM 的值都会保留，引脚的逻辑电平保持不变
  - –所有使能的时钟仍处于运行状态
  - –使能的外设功能继续运行，并可产生中断唤醒处理器
  - –和其它几种低功耗模式相比，睡眠模式的唤醒时间最短

LPC82x唤醒源 – 睡眠模式

- 睡眠模式 – 唤醒源:
  - 任何一种外式的中断（SCT、MRT、 Systick Timer 、 USARTs 、 SPI 、 I2C 、 Comparator ）
  - 管脚中断
  - 模式匹配引擎（PME - Pattern Match Engine）
  - 掉电检测（ BOD ）产生的中断和复位请求
  - 窗口看门狗定时器（WWDT）产生的中断和复位请求
  - 外部复位信号
  - 自唤醒定时器（ WKT ）
  - 唤醒后，程序从进入睡眠前的位置继续执行

LPC82x低功耗模式 –深度睡眠模式（Deep-sleep mode）

- 深度睡眠模式（Deep-sleep mode）：
  - –通往内核的系统时钟停止工作
  - –所有外设的时钟停止，除了：自唤醒定时器（ WKT ）和窗口看门狗定时器（WWDT）
  - –掉电检测（ BOD ）允许继续工作
  - –Flash处于待机状态，所以唤醒时间比掉电模式要快
  - –处理器的状态和寄存器、外设寄存器和内部SRAM 的值都会保留，引脚的逻辑电平保持不变
  - –在进入深度睡眠模式和掉电模式之前，必须将时钟切换到IRC以便顺利进入低功耗模式

LPC82x唤醒源 – 深度睡眠模式

- 深度睡眠模式 – 唤醒源:
  - –从USARTs来的中断（同步从属模式，外部时钟）
  - –从SPI来的中断（从属模式，外部时钟）
  - –从I2C来的中断（从属模式，外部时钟）
  - –管脚中断
  - –掉电检测（ BOD ）产生的中断和复位请求
  - –窗口看门狗定时器（WWDT）产生的中断和复位请求
  - –外部复位信号
  - –自唤醒定时器（ WKT ）
  - –唤醒后，程序从进入睡眠前的位置继续执行

LPC82x低功耗模式 –掉电模式（Power-down mode）

- 掉电模式（Power-down mode）:
  - 内核和所有外设的时钟停止，除了：自唤醒定时器（ WKT ）和窗口看门狗定时器（WWDT）
  - 掉电检测（ BOD ）允许继续工作
  - Flash关闭（和深度睡眠模式相比唤醒时需要化更多的时间）
  - 处理器的状态和寄存器、外设寄存器和内部SRAM 的值都会保留，引脚的逻辑电平保持不变
  - 在进入深度睡眠模式和掉电模式之前，必须将时钟切换到IRC以便顺利进入低功耗模式

LPC82x唤醒源 – 掉电模式

- 掉电模式 – 唤醒源：
  - 从USARTs来的中断（同步从属模式，外部时钟）
  - 从SPI来的中断（从属模式，外部时钟）
  - 从I2C来的中断（从属模式，外部时钟）
  - 管脚中断
  - 掉电检测（ BOD ）产生的中断和复位请求
  - 窗口看门狗定时器（WWDT）产生的中断和复位请求
  - 外部复位信号
  - 自唤醒定时器（ WKT ）
  - 唤醒后，程序从进入睡眠前的位置继续执行

LPC82x低功耗模式 – 深度掉电模式（Deep Power-down mode）

- 深度掉电模式（Deep Power-down mode）：
  - 除了PMU，所有的电源和时钟都关闭
  - 提供5个通用寄存器来存放临时数据
  - 自唤醒定时器（ WKT ）可以工作
  - 处理器的状态和寄存器、外设寄存器和内部SRAM 的值都不保留，引脚的逻辑电平不保持
  - 所需唤醒时间在所有低功耗模式中是最长的

LPC82x唤醒源 – 深度掉电模式

- 深度掉电模式 – 唤醒源：
  - 自唤醒定时器（ WKT ）
  - 唤醒管脚上出现由高到低的电平变化
  - 注意：
    - 不能用外部复位来唤醒
    - 唤醒后芯片将会复位并重新启动

LPC82x 各种低功耗模式对比

对比项 \ 低功耗模式	Sleep mode	Deep-sleep mode	Power-down mode	Deep Power-down mode
数字外设	可通过软件配置	关闭	关闭	关闭
IRC	可通过软件配置	打开	关闭	关闭
IRC 输出	可通过软件配置	关闭	关闭	关闭
Flash	可通过软件配置	打开	关闭	关闭
BOD	可通过软件配置	可通过软件配置	可通过软件配置	关闭
PLL	可通过软件配置	关闭	关闭	关闭
SysOsc	可通过软件配置	关闭	关闭	关闭
WDO	可通过软件配置	可通过软件配置	可通过软件配置	关闭
LPO	可通过软件配置	可通过软件配置	可通过软件配置	可通过软件配置
唤醒源	任意一个外设来的中断 管脚中断 模式匹配引擎 BOD 中断 / 复位 WWDT中断 / 复位 外部复位信号 WKT	从USARTs / SPI / I2C 来的中断 管脚中断 BOD 中断 / 复位 WWDT中断 / 复位 外部复位信号 WKT	从USARTs / SPI / I2C 来的中断 管脚中断 BOD 中断 / 复位 WWDT中断 / 复位 外部复位信号 WKT	WKT 专用唤醒管脚
Wake-up time (only for Ref.)	2.6us	4us	50us	215us

低功耗模式相关配置

LPC82x 执行唤醒

- 在sleep、deep-sleep和 power-down模式中，除了使能相关外设的中断，还应将这些外设中断源连接到NVIC

Connection of interrupt sources to the NVIC

Interrupt number	Name	Description	Flags
0	SPI0_IRQ	SPI0 interrupt	See Table 192 "SPI Interrupt Enable read and Set register (INTENSET, addresses 0x4005 800C (SPI0) , 0x4005 C00C (SPI1)) bit description".
1	SPI1_IRQ	SPI1 interrupt	Same as SPI0_IRQ
2	-	Reserved	-
3	UART0_IRQ	USART0 interrupt	See Table 161 "USART Interrupt Enable read and set register (INTENSET, address 0x4006 400C (USART0), 0x4006 800C (USART1), 0x4006 C00C (USART2)) bit description"
4	UART1_IRQ	USART1 interrupt	Same as UART0_IRQ
5	UART2_IRQ	USART2 interrupt	Same as UART0_IRQ
6	-	Reserved	-
7	-	Reserved	-
8	I2C0_IRQ	I2C0 interrupt	See Table 175 "Interrupt Enable Clear register (INTENCLR, address 0x4005 000C) bit description".
9	SCT_IRQ	State configurable timer interrupt	EVFLAG SCT event
10	MRT_IRQ	Multi-rate timer interrupt	Global MRT interrupt. GFLAG0 GFLAG1 GFLAG2 GFLAG3
11	CMP_IRQ	Analog comparator interrupt	COMPEDGE - rising, falling, or both edges can set the bit
12	WDT_IRQ	Windowed watchdog timer interrupt	WARNINT - watchdog warning interrupt
13	BOD_IRQ	BOD interrupts	BODINTVAL - BOD interrupt level
14	-	-	Reserved
15	WKT_IRQ	Self wake-up timer interrupt	ALARMFLAG
23:16	-	Reserved	-
24	PININT0_IRQ	Pin interrupt 0 or pattern match engine slice 0 interrupt	PSTAT - pin interrupt status
25	PININT1_IRQ	Pin interrupt 1 or pattern match engine slice 1 interrupt	PSTAT - pin interrupt status
26	PININT2_IRQ	Pin interrupt 2 or pattern match engine slice 2 interrupt	PSTAT - pin interrupt status
27	PININT3_IRQ	Pin interrupt 3 or pattern match engine slice 3 interrupt	PSTAT - pin interrupt status
28	PININT4_IRQ	Pin interrupt 4 or pattern match engine slice 4 interrupt	PSTAT - pin interrupt status
29	PININT5_IRQ	Pin interrupt 5 or pattern match engine slice 5 interrupt	PSTAT - pin interrupt status
30	PININT6_IRQ	Pin interrupt 6 or pattern match engine slice 6 interrupt	PSTAT - pin interrupt status
31	PININT7_IRQ	Pin interrupt 7 or pattern match engine slice 7 interrupt	PSTAT - pin interrupt status

Start Logic 0 管脚唤醒使能寄存器 - STARTERP0

- 通过管脚中断来唤醒
  - STARTERP0 管脚唤醒使能寄存器
  - 可用于deep-sleep 和 power-down 模式的唤醒

Start logic 0 pin wake-up enable register 0 (STARTERP0, address 0x4004 8204) bit description

Bit	Symbol	Value	Description	Reset value
0	PINT0		GPIO pin interrupt 0 wake-up	0
		0	Disabled	
		1	Enabled	
1	PINT1		GPIO pin interrupt 1 wake-up	0
		0	Disabled	
		1	Enabled	
2	PINT2		GPIO pin interrupt 2 wake-up	0
		0	Disabled	
		1	Enabled	
3	PINT3		GPIO pin interrupt 3 wake-up	0
		0	Disabled	
		1	Enabled	
4	PINT4		GPIO pin interrupt 4 wake-up	0
		0	Disabled	
		1	Enabled	
5	PINT5		GPIO pin interrupt 5 wake-up	0
		0	Disabled	
		1	Enabled	
6	PINT6		GPIO pin interrupt 6 wake-up	0
		0	Disabled	
		1	Enabled	
7	PINT7		GPIO pin interrupt 7 wake-up	0
		0	Disabled	
		1	Enabled	
31:8	-		Reserved	-

Start Logic 1 外设唤醒使能寄存器 – STARTERP1

- 通过外设中断来唤醒
  - STARTERP1 管脚唤醒使能寄存器
  - 可用于deep-sleep 和 power-down 模式的唤醒

Start logic 1 interrupt wake-up enable register (STARTERP1, address 0x4004 8214) bit description

Bit	Symbol	Value	Description	Reset value
0	SPI0		SPI0 interrupt wake-up	0
		0	Disabled	
		1	Enabled	
1	SPI1		SPI1 interrupt wake-up	0
		0	Disabled	
		1	Enabled	
2	-		Reserved	-
3	USART0		USART0 interrupt wake-up. Configure USART in synchronous slave mode.	0
		0	Disabled	
		1	Enabled	
4	USART1		USART1 interrupt wake-up. Configure USART in synchronous slave mode.	0
		0	Disabled	
		1	Enabled	
5	USART2		USART2 interrupt wake-up. Configure USART in synchronous slave mode.	0
		0	Disabled	
		1	Enabled	
7:6	-		Reserved	-
8	I2C		I2C interrupt wake-up.	0
		0	Disabled	
		1	Enabled	
11:9	-		Reserved	-
12	WWDT		WWDT interrupt wake-up	0
		0	Disabled	
		1	Enabled	
13	BOD		BOD interrupt wake-up	0
		0	Disabled	
		1	Enabled	
14	-		Reserved	-
15	WKT		Self wake-up timer interrupt wake-up	0
		0	Disabled	
		1	Enabled	
31:16			Reserved.	-

Deep-Sleep模式配置寄存器

- 可用于deep-sleep 和 power-down 模式
- 在deep-sleep 和 power-down 模式下，芯片内的模拟模块都被关闭，除了BOD 和 watchdog oscillator，它们可以在低功耗模式时被配置成运行状态
- WDTOSC 可以作为 Watchdog timer 的时钟源来产生需要的看门狗中断

Deep-sleep configuration register (PDSLEEPCFG, address 0x4004 8230) bit description

Bit	Symbol	Value	Description	Reset value
2:0			Reserved.	0b111
3	BOD_PD		BOD power-down control for Deep-sleep and Power-down mode	1
		0	Powered	
		1	Powered down	
5:4			Reserved.	11
6	WDTOSC_PD		Watchdog oscillator power-down control for Deep-sleep and Power-down mode. Changing this bit to powered-down has no effect when the LOCK bit in the WWDT MOD register is set. In this case, the watchdog oscillator is always running.	1
		0	Powered	
		1	Powered down	
15:7	-		Reserved	0b111111111
31:16	-	-	Reserved	0

唤醒配置寄存器 - PDAWAKECFG

- 可用于deep-sleep 和 power-down 模式
- 该寄存器可用来配置唤醒后的功耗状态
- 这样可以使得唤醒的速度加快，因为用户不用再去重新配置那些在进入低功耗模式前使用的寄存器

Wake-up configuration register (PDAWAKECFG, address 0x4004 8234) bit description

Bit	Symbol	Value	Description	Reset value
0	IRCOUT_PD		IRC oscillator output wake-up configuration	0
		0	Powered	
		1	Powered down	
1	IRC_PD		IRC oscillator power-down wake-up configuration	0
		0	Powered	
		1	Powered down	
2	FLASH_PD		Flash wake-up configuration	0
		0	Powered	
		1	Powered down	
3	BOD_PD		BOD wake-up configuration	0
		0	Powered	
		1	Powered down	
4	-		Reserved.	1
5	SYSOSC_PD		Crystal oscillator wake-up configuration	1
		0	Powered	
		1	Powered down	
6	WDTOSC_PD		Watchdog oscillator wake-up configuration. Changing this bit to powered-down has no effect when the LOCK bit in the WWDT MOD register is set. In this case, the watchdog oscillator is always running.	1
		0	Powered	
		1	Powered down	
7	SYSPLL_PD		System PLL wake-up configuration	1
		0	Powered	
		1	Powered down	
11:8	-		Reserved. Always write these bits as 0b1101	0b1101
14:12	-		Reserved. Always write these bits as 0b110	0b110
15	ACMP		Analog comparator wake-up configuration	1
		0	Powered	
		1	Powered down	
31:16	-	-	Reserved	0

LPC82x自唤醒定时器（WKT）

- 32位可重装载向下计数
  - 当计数值装载后计数器自动开始计数
  - 时间到后将产生一个中断唤醒请求
  - WKT的电源和芯片中其它电源是分开的，以保证可以一直处于工作状态
  - WKT可用来唤醒sleep、 deep-sleep、 power-down和 deep power-down模式
  - WKT也可用于普通的定时功能

- WKT的时钟源有两种
  - IRC
  - LP OSC

WKT时钟源

- 以IRC作为时钟源的WKT
  - 从IRC（WKT缺省时钟）来的750 kHz的时钟作为时钟源
  - 精度高
  - 可用于sleep模式的唤醒

- 以LP OSC作为时钟源的WKT
  - 从LP OSC来的10 kHz（+/- 40 %）时钟作为时钟源
  - 精度低
  - 可用于sleep、deep-sleep、power-down和deep power-down模式的唤醒

WKT 控制和赋值寄存器

- WKT中断必须在NVIC中被使能，才能利用所赋计数值来唤醒低功耗模式

Control register (CTRL, address 0x4000 8000) bit description

Bit	Symbol	Value	Description	Reset value
0	CLKSEL		Select the self wake-up timer clock source.	0
		0	Divided IRC clock. This clock runs at 750 kHz and provides time-out periods of up to approximately 95 minutes in 1.33 µs increments. **Remark:** This clock is not available in not available in Deep-sleep, power-down, deep power-down modes. Do not select this option if the timer is to be used to wake up from one of these modes.	
		1	Low power clock. This is the (nominally) 10 kHz clock and provides time-out periods of up to approximately 119 hours in 100 µs increments. The accuracy of this clock is limited to +/- 45 % over temperature and processing. **Remark:** This clock is available in all power modes. Prior to use, the low-power oscillator must be enabled. The oscillator must also be set to remain active in Deep power-down if needed.	
1	ALARMFLAG		Wake-up or alarm timer flag.	-
		0	No time-out. The self wake-up timer has not timed out. Writing a 0 to has no effect.	
		1	Time-out. The self wake-up timer has timed out. This flag generates an interrupt request which can wake up the part from any reduced power mode including Deep power-down if the clock source is the low power oscillator. Writing a 1 clears this status bit.	
2	CLEARCTR		Clears the self wake-up timer.	0
		0	No effect. Reading this bit always returns 0.	
		1	Clear the counter. Counting is halted until a new count value is loaded.	
31:3	-		Reserved.	-

Counter register (COUNT, address 0x4000 800C) bit description

Bit	Symbol	Description	Reset value
31:0	VALUE	A write to this register pre-loads start count value into the timer and starts the count-down sequence. A read reflects the current value of the timer.	-

Deep Power-Down模式控制寄存器DPDCTRL

- 寄存器DPDCTRL用来选择LP OSC用于WKT来将芯片从Deep power-down模式中唤醒
- 该寄存器也可用来配置唤醒管脚（管脚PIO0_4 ）

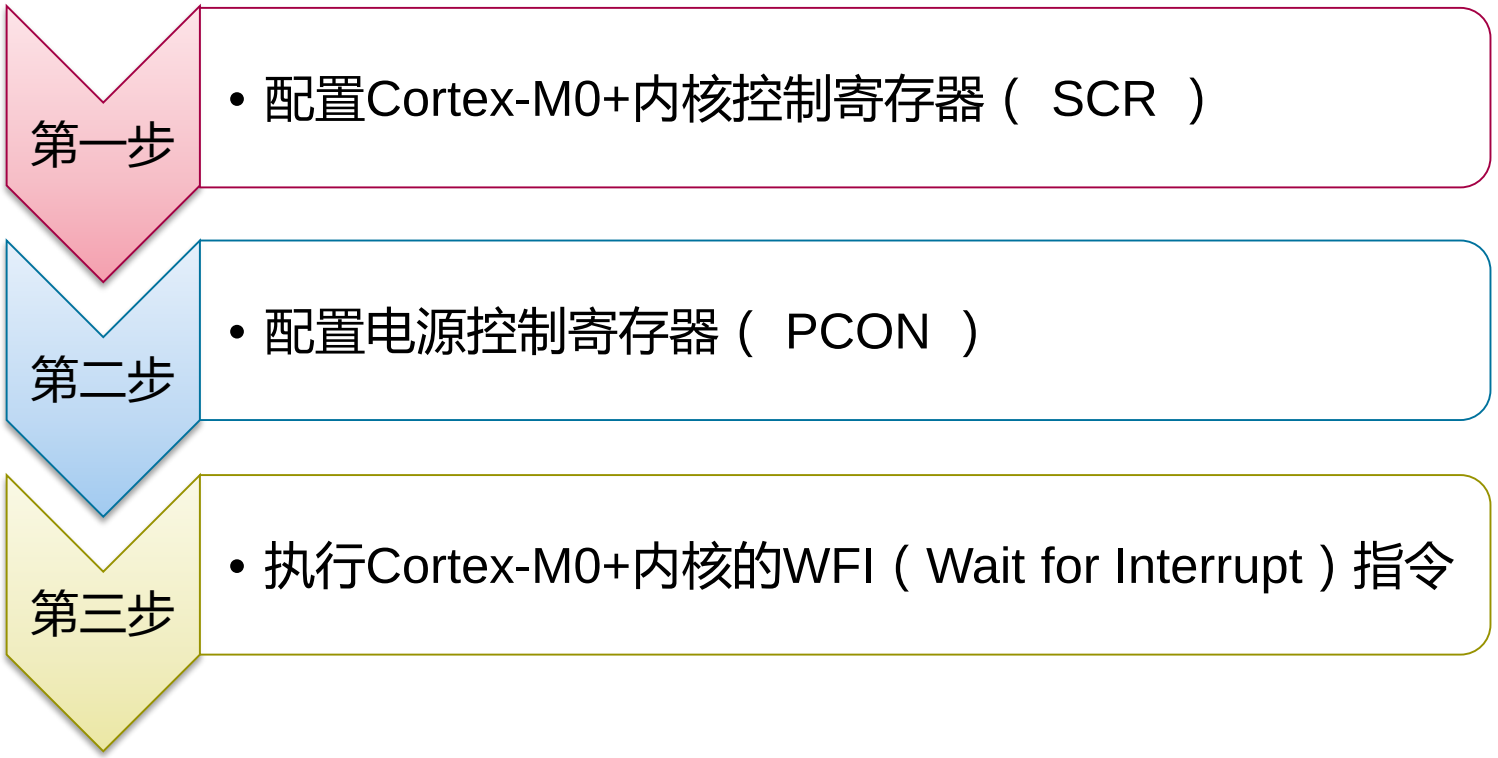
Deep power down control register (DPDCTRL, address 0x4002 0014) bit description

Bit	Symbol	Value	Description	Reset value
0	WAKEUPHYS		WAKEUP pin hysteresis enable	0
		0	Disabled. Hysteresis for WAKEUP pin disabled.	
		1	Enabled. Hysteresis for WAKEUP pin enabled.	
1	WAKEPAD_ DISABLE		WAKEUP pin disable. Setting this bit disables the wake-up pin, so it can be used for other purposes. **Remark:** Never set this bit if you intend to use a pin to wake up the part from Deep power-down mode. You can only disable the wake-up pin if the self wake-up timer is enabled and configured. **Remark:** Setting this bit is not necessary if Deep power-down mode is not used.	0
		0	Enabled. The wake-up function is enabled on pin PIO0_4.	
		1	Disabled. Setting this bit disables the wake-up function on pin PIO0_4.	
2	LPOSCEN		Enable the low-power oscillator for use with the 10 kHz self wake-up timer clock. You must set this bit if the CLKSEL bit in the self wake-up timer CTRL bit is set. Do not enable the low-power oscillator if the self wake-up timer is clocked by the divided IRC.	0
		0	Disabled.	
		1	Enabled.	
3	LPOSCDPDEN		Enable the low-power oscillator in Deep power-down mode. Setting this bit causes the low-power oscillator to remain running during Deep power-down mode provided that bit 12 in this register is set as well. You must set this bit for the self wake-up timer to be able to wake up the part from Deep power-down mode. **Remark:** Do not set this bit unless you use the self wake-up timer to wake up from Deep power-down mode.	0
		0	Disabled.	
		1	Enabled.	
31:4	-		Data retained during Deep power-down mode.	0x0

如何进入低功耗模式

LPC82x – 如何进入低功耗模式

- 进入低功耗模式一般需要经过如下三个步骤：

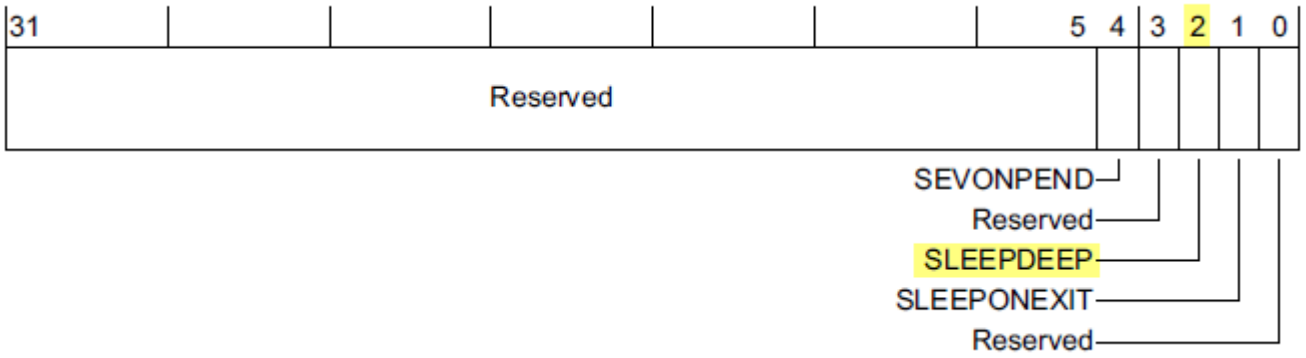


- 当WFI指令执行后，就开始进入低功耗模式

Cortex-M0+内核控制寄存器（ SCR ）

- Cortex-M0+内核控制寄存器（ SCR ）（ 0xE000ED10 ）*
- 除了sleep模式，其它低功耗模式都需要置高寄存器 SCR的第2位

* ARMv6-M 架构参考手册



电源控制寄存器（ PCON ）

- PCON 寄存器

Table 43. Power control register (PCON, address 0x4002 0000) bit description

Bit	Symbol	Value	Description	Reset value
2:0	PM		Power mode	000
		0x0	Default. The part is in active or sleep mode.	
		0x1	ARM WFI will enter Deep-sleep mode.	
		0x2	ARM WFI will enter Power-down mode.	
		0x3	ARM WFI will enter Deep-power down mode (ARM Cortex-M0+ core powered-down).	
3	NODPD		A 1 in this bit prevents entry to Deep power-down mode when 0x3 is written to the PM field above, the SLEEPDEEP bit is set, and a WFI is executed. This bit is cleared only by power-on reset, so writing a one to this bit locks the part in a mode in which Deep power-down mode is blocked.	0
7:4	-	-	Reserved. Do not write ones to this bit.	0
8	SLEEPFLAG		Sleep mode flag	0
		0	Read: No power-down mode entered. Part is in Active mode. Write: No effect.	
		1	Read: Sleep/Deep-sleep or Deep power-down mode entered. Write: Writing a 1 clears the SLEEPFLAG bit to 0.	
10:9	-	-	Reserved. Do not write ones to this bit.	0
11	DPDFLAG		Deep power-down flag	0
		0	Read: Deep power-down mode **not** entered. Write: No effect.	0
		1	Read: Deep power-down mode entered. Write: Clear the Deep power-down flag.	
31:12	-	-	Reserved. Do not write ones to this bit.	0

WFI（Wait for Interrupt）指令

- WFI（Wait for Interrupt）指令是一条Cortex-M0+内核指令
  - 当WFI指令执行后，就开始进入低功耗模式

- 这条指令不能用C语言来执行

- 在C语言中编译器提供宏命令来执行这条指令

```
__WFI();
```

如何进入 Sleep 模式

第一步

- 在NVIC中使能中断源

第二步

- 寄存器SCR的SLEEPDEEP位必须是“0x0”
- 寄存器PCON的PM位必须是“0x0”

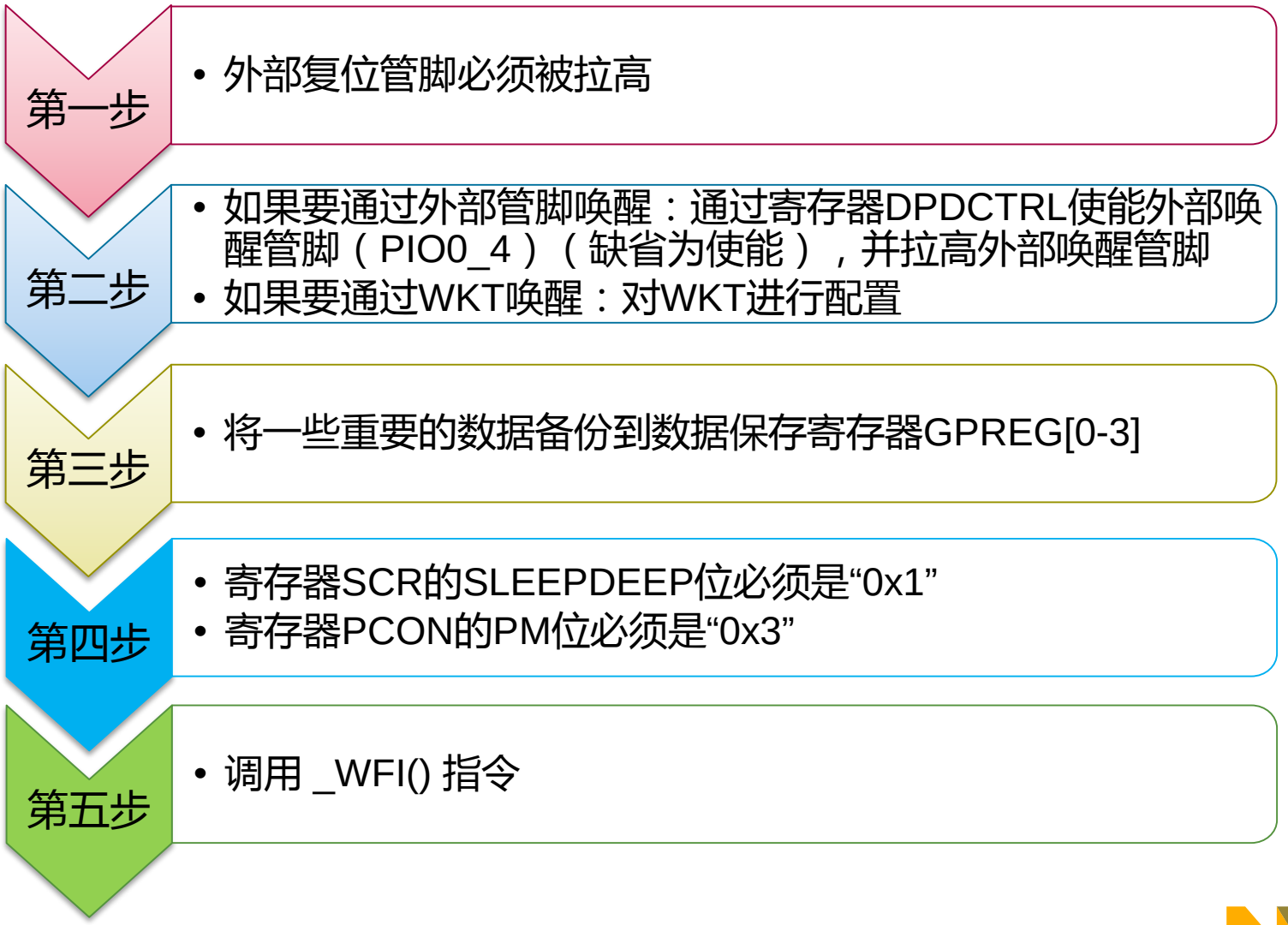
第三步

- 调用 _WFI() 指令

如何进入 Deep Sleep 模式

如何进入 Power Down 模式

如何进入 Deep Power Down 模式



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