# COVERSHEET

THE UNIVERSITY OF WESTERN AUSTRALIA

**Assignment, Report & Laboratory Coversheet for Individual & Group Assignment**

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# UWA ELEC5550

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## Table of Contents

**LIST OF FIGURES** ..... **VIII**

**LIST OF TABLES** ..... **IX**

**1. REPORT SUMMARY** ..... **10**

**2. INTRODUCTION** ..... **11**

2.1 PURPOSE ..... 11
2.2 PROJECT SCOPE ..... 11
2.3 DOCUMENT STRUCTURE ..... 11
2.4 DEFINITIONS, ACRONYMS, AND ABBREVIATIONS ..... 12
2.5 CONTRIBUTION SUMMARIES ..... 14
*2.5.1 Anamika Joby ..... 14*
*2.5.2 Ethan Tan ..... 15*
*2.5.3 Layla Kim ..... 16*
*2.5.4 Luisa Puliafito ..... 17*
*2.5.5 Sahan Pothupitiya ..... 18*
*2.5.6 Shirley Mziray ..... 19*

**3. FINAL DESIGN AND DESIGN PROCESS** ..... **20**

3.1 FINAL REQUIREMENTS PRIORITISED ..... 20
3.2 ARCHITECTURE OVERVIEW ..... 22
3.3 DESIGN PHILOSOPHY ..... 23
*3.3.1 Pillar 1: Performance and User Transparency ..... 23*
*3.3.2 Pillar 2: Reliability and Practicality ..... 23*
*3.3.3 Pillar 3: Safety ..... 23*
3.4 FINAL DESIGN ELEMENTS AND JUSTIFICATION ..... 24
*3.4.1 Manufacturer Selection and PCB Design ..... 25*
*3.4.2 MCU Selection and Justification ..... 25*
*3.4.3 MCU System ..... 27*
*3.4.4 Transmitter Module Architecture and Justification ..... 31*
*3.4.5 Receiver Module Architecture and Justification ..... 39*
*3.4.6 Chassis ..... 46*
*3.4.7 Firmware ..... 52*
3.5 PROCESS ASSEMBLY/CONSTRUCTION ..... 54
*3.5.1 PCB Fabrication and Component Assembly ..... 55*
*3.5.2 Firmware ..... 55*
*3.5.3 Issues Identified and Resolutions ..... 56*
3.6 SYSTEM INTEGRATION ..... 57
*3.6.1 Hardware Integration ..... 58*
*3.6.2 Firmware Integration ..... 61*
*3.6.3 End-to-End Integration ..... 63*
3.7 STAKEHOLDER ENGAGEMENT ETHAN ..... 64
*3.7.1 Key Stakeholder Engagement ..... 64*
*3.7.2 Preliminary and Critical Design Review ..... 65*
3.8 SAFETY ISSUES IDENTIFIED ..... 66
*3.8.1 Optical Safety: Eye Hazard from Laser Emission ..... 66*
*3.8.2 Electrical Safety: Shock and Fire Hazard ..... 66*
*3.8.3 Handling Safety: Component Damage During Assembly ..... 67*
3.9 ETHICAL ISSUES ..... 68
3.10 RISKS AND MITIGATION ..... 70
*3.10.1 Risk Evaluation ..... 70*
3.11 LIST OF DESIGN OUTPUTS ..... 71
*3.11.1 LMS Content ..... 72*
*3.11.2 Meeting Minutes ..... 72*

*3.11.3 Design Project Reports* ..... *72*
*3.11.4 Project Specs* ..... *73*
*3.11.5 Project Management* ..... *73*
3.12 FINAL COSTS ..... 74

**4. RECOMMENDATIONS FOR NEXT DESIGN ..... 76**

4.1 MCU ..... 76
4.2 TRANSCEIVER ..... 76
*4.2.1 Transmitter Module* ..... *76*
*4.2.2 Receiver Module* ..... *77*
4.3 CHASSIS ..... 77
*4.3.1 Wall and Ceiling Mounting* ..... *78*
*4.3.2 Using the Modules in Outdoor Environments* ..... *78*
*4.3.3 Renewable Energy Source* ..... *78*
4.4 FIRMWARE ..... 79
4.5 GENERAL RECOMMENDATIONS FOR FUTURE DESIGNS ..... 80

**5. DESIGN COMPLETION AND DEMONSTRATION ..... 80**

5.1 PCB DESIGN COMPLETION ..... 80
5.2 EXPECTATIONS ..... 82
5.3 DEMONSTRATION ..... 83

**6. OPERATION AND MAINTENANCE GUIDE ..... 84**

6.1 SYSTEM OVERVIEW ..... 84
6.2 SAFETY INFORMATION ..... 85
*6.2.1 Laser Safety* ..... *86*
*6.2.2 Electrical Safety* ..... *86*
*6.2.3 Thermal Considerations* ..... *87*
*6.2.4 Personal Protective Equipment (PPE) and Emergency Procedures* ..... *87*
6.3 OPERATING PROCEDURE ..... 87
*6.3.1 Step 1: Setup* ..... *87*
*6.3.2 Step 2: Module Alignment* ..... *88*
*6.3.3 Step 3: Connect a USB Peripheral* ..... *88*
*6.3.4 Step 4: Status Indicators* ..... *88*
*6.3.5 Step 5: Shutdown and Storage* ..... *88*
6.4 TROUBLESHOOTING GUIDE ..... 88
6.5 RECOMMENDED MAINTENANCE & TESTS ..... 89
*6.5.1 Maintenance* ..... *89*
*6.5.2 Operational Tests* ..... *89*
6.6 ETHICAL AND PROFESSIONAL STANDARDS ..... 90
6.7 DELIVERABLES AND SUPPORTING OUTPUTS ..... 90
*6.7.1 Firmware* ..... *90*
*6.7.2 Electronic Hardware* ..... *90*
*6.7.3 Mechanical Hardware* ..... *90*

**7. CONCLUSION ..... 91**

**8. REFERENCES ..... 92**

**9. APPENDICES ..... 93**

9.1 APPENDIX A ..... 93
9.2 APPENDIX B ..... 94
9.3 APPENDIX C ..... 99
*9.3.1 Technical Test T001.1 Host Communication (Verification)* ..... *99*
*9.3.2 Technical Test T002.1 Unidirectional FSO Link Test with 2m Distance* ..... *101*
*9.3.3 Technical Test T002.2 Bidirectional FSO Link Test with 2m Distance* ..... *103*
*9.3.4 Technical Test T002.3 UART-Based Character Transmission over 2 m FSO Link* ..... *105*
*9.3.5 Technical Test T003.1 UART-Based Character Transmission over 2 m FSO Link* ..... *107*

*9.3.6 Technical Test T004.1 Power and operation time - MCU Circuit Reliability and performance 109*
*9.3.7 Technical Test T004.2 Power and operation time - MCU Circuit Reliability and performance. 111*
*9.3.8 Technical Test T004.3 Power Endurance Test ..... 114*
*9.3.9 Technical Test T005.1 Auto Peripheral Detection and Data Rate Transfer – with wire ..... 116*
*9.3.10 Technical Test T005.2 Data Transfer Rate Test over FSO Link ..... 118*
*9.3.11 Technical Test T005.3 HID Hot Swapping Validation ..... 120*
*9.3.12 Technical Test T006.1 FSO HID Transmission Distance Validation ..... 122*
*9.3.13 Technical Test T007.1 Link Interruption Recovery Test ..... 124*
9.4 APPENDIX D: FINAL BILL OF MATERIALS ..... 126
9.5 APPENDIX E: VALIDATION AND VERIFICATION TABLE ..... 127
9.6 APPENDIX F: 850NM LASER DIODE CLASS 1M CALCULATIONS ..... 132
9.7 APPENDIX G: TRANSMITTER MODULE SIMULATIONS AND PROTOTYPE ..... 133
9.8 APPENDIX H: RECEIVER MODULE SIMULATIONS AND PROTOTYPE ..... 135
9.9 APPENDIX I: CHASSIS DESIGN ..... 139

**List of Figures**

Figure 1: System/Subsystem Architecture of the Design Project ..... 22
Figure 2: Hardware Design Structure ..... 25
Figure 3: Wroom1 ESP32 Module ..... 27
Figure 4: MCU WROOM1 ..... 27
Figure 5: MCU USB-To-Serial ..... 28
Figure 6: MCU USB OTG/UART ..... 28
Figure 7: MCU Reset/Boot Button ..... 29
Figure 8: Receiver/Transmitter Button ..... 29
Figure 9: MCU Auto Program ..... 30
Figure 10: Final MCU PCB design ..... 30
Figure 11: Laser Diode Driver Design 1 ..... 32
Figure 12: Transient Simulation of Design 1, with the addition of 50 Ω resistor ..... 33
Figure 13: Breadboard Prototype of Design 1 ..... 33
Figure 14: Laser Diode Driver Design 2 ..... 34
Figure 15: Showcasing the Difference in Gate Voltage after Addition of Diode ..... 34
Figure 16: Schematic of the transmitter circuit, will all components and their values ..... 36
Figure 17:Custom Laser Diode Driver Prototype Design 2 ..... 37
Figure 18: Laser Diode Driver PCB Design ..... 39
Figure 19: Initial receiver schematic ..... 40
Figure 20: Simulation Results for initial receiver design ..... 40
Figure 21: Simulation Result of the Initial Single-Stage TIA Design ..... 41
Figure 22: Design 2 of Receiver Circuit with increased frequency ..... 41
Figure 23: Output Voltage of Design 2 ..... 42
Figure 24: Final receiver schematic ..... 42
Figure 25: Receiver PCB design - with visible ground plane ..... 45
Figure 26: Receiver Circuit PCB -with visible divided power plane ..... 45
Figure 27: Initial Concept Sketch of the Chassis ..... 47
Figure 28: Initial Engineering Drawings of the Chassis ..... 47
Figure 29: First Version of the Chassis using TinkerCAD ..... 49
Figure 30: Engineering Sketches of the Second Version of the Chassis on Fusion ..... 50
Figure 31: Final Chassis design ..... 51
Figure 32: Firmware architecture overview ..... 52
Figure 33: FSO Communication System Architecture ..... 54
Figure 34: MCU circuit ..... 59
Figure 35: Power connectivity over the separate circuits ..... 60
Figure 36: LoS Interception: Eavesdropper near Receiver [3] ..... 69
Figure 37: Non-LoS Interception [3] ..... 70
Figure 38: Expenditure Analysis based on Purchasing Locations and Budget Remaining ..... 75
Figure 39: Concept Version of the Chassis for Outdoor Use ..... 79
Figure 40: Final MCU design ..... 81
Figure 41: Final Laser Diode Driver PCB design ..... 81
Figure 42: Final Receiver PCB design ..... 82
Figure 43: Schematic of the Inverting Amplifier Used to Correct Negative Output Voltage ..... 82
Figure 44: FSO Communication System ..... 85
Figure 45:MCU booting was tested and was successful ..... 113
Figure 46:MCU booting was tested and was successful ..... 113
Figure 48: Laser Diode Alternative Design ..... 133

Figure 49: Laser Diode Driver Final Design ..... 133
Figure 50: Transmitter Module Prototype ..... 134
Figure 51: Receiver Module Design 1 ..... 135
Figure 52: Receiver Circuit Design 2 ..... 135
Figure 53: Receiver Module 2 Stage non-inverting ..... 136
Figure 54: Receiver Module Three Stage non-inverting ..... 136
Figure 55: Receiver Circuit Two stage inverting ..... 136
Figure 56: Receiver Module Alternative Design I ..... 137
Figure 57: Receiver Circuit Alternative Design II ..... 137
Figure 58: Receiver Circuit Prototype ..... 138
Figure 59: Final Version of the Chassis on Fusion ..... 139

## List of Tables

Table 1: Acronyms and Abbreviations ..... 12
Table 2: Requirements Categories and IDs ..... 20
Table 3: Top 20 Requirements ..... 21
Table 4: Summary of Requirements Compliance ..... 38
Table 5: Requirement compliance ..... 46
Table 6: Functional Requirements to ESP Features ..... 54
Table 7: Stakeholder Management Matrix ..... 64
Table 8: Eye Hazard and Safety Measures from Laser Emission ..... 66
Table 9: Electrical Shock and Fire Hazard Safety ..... 66
Table 10: Component Handling and Assembly Safety ..... 67
Table 11: Code for Referencing Purchase Locations ..... 74
Table 12: Troubleshooting guide ..... 89
Table 13: Recommended Maintenance Tasks and Frequency ..... 89
Table 14: Other Requirements ..... 93
Table 15: Risk Level Classification and Action Priority Matrix ..... 94
Table 16: Qualitative Risk Assessment Matrix ..... 94
Table 17: Level of Likelihood Descriptive table ..... 94
Table 18: Project Risk Register ..... 96
Table 19: Final Bill of Materials ..... 126
Table 20: Validation and Verification Table ..... 127

## 1. Report Summary


This report presents the design, development, and validation of a 2-Way FSOCS constructed as part of the UWA ELEC5550 Design Project 2025 in collaboration with the ANFF. The project's primary objective was to design a compact, low-cost, and safe optical link capable of bidirectional USB data transmission between two microcontroller-based modules through free space, while satisfying Class 1M laser-safety compliance, low-latency communication, and error-free data integrity.

The FSOCS was implemented using custom-designed PCBs for the MCU, transmitter, and receiver modules. The MCU board, based on the ESP32-WROOM1 microcontroller, manages USB host and peripheral operations and coordinates data transfer between optical modules. The transmitter employs a laser-diode driver with an adjustable current clamp, ensuring the optical output remains within the IEC 60825-1 Class 1M emission limit. The receiver features a three-stage TIA chain that amplifies the weak optical signal to logic-level voltage compatible with the MCU. All modules are enclosed within a 3D-printed PLA chassis, providing stable mechanical alignment and electrical safety.

Firmware was developed using ESP-IDF to enable both HID and MSC communication over the optical channel. A structured integration approach, beginning with wired UART tests, followed by optical FSO validation, confirmed full end-to-end operation for USB mouse, keyboard, and flash driver.

Comprehensive testing verified the system's compliance with performance, safety, and functional requirements: the optical link achieved reliable bidirectional communication over 2m, maintained a latency below 50 ms, and demonstrated bit-error-free transmission under ambient-light conditions up to 1000 lux. Hardware and firmware integration tests also validated current-clamp reliability, optical alignment stability, and Class 1M safety limits.

In conclusion, the final design demonstrates a successful integration of hardware, firmware, and mechanical systems within the project's budget ($500 AUD), safety, and schedule constraints. Recommendations for future work include incorporating visual status indicators, enhanced environmental protection for outdoor operation, and exploration of 1550 nm VCSEL sources to further increase transmission distance and safety margins.

# 2. Introduction

In the 21st century, innovation through electrical and electronic engineering has resulted in communication technologies becoming faster, more efficient and more secure. This can be seen from the evolution of telecommunications using fibre optics, and the rise of the IoT.

Among various technologies, FSOCS that transmits information through free space using lasers, is a clear example of innovation through the years to improve data transfer speeds and security.

However, the use of FSOCS comes with different obstacles to overcome, such as maintaining safe laser output levels and ensuring low latency with effective data correction for reliable operation.

In this context, the 2025 ELEC5550 Design Project aims to develop a bidirectional FSOCS with a USB interface, tailored to meet the needs of the ANFF.

## 2.1 Purpose

The purpose of this document is to discuss the purpose of our designed solution, the responsibilities held by each team member, the final design and the design process leading to it, and recommendations for the next design iterations and prototypes.

## 2.2 Project Scope

The project being designed is a 2-way FSOCS that uses modules with USB interfaces at both ends.

The two modules in the system use custom designed laser diode drivers, which are current clamped to be maintained at Class 1M or below. The modules also use our own designed photodiode receivers, which can cope with the reflected light from their own source.

The system must perform well enough to support USB data transfer speeds and low latency sufficient for the use of a mouse, keyboard, or a USB stick. Additionally, the system must be able to implement data transfer correction for better reliability.

Furthermore, the final design of the system must use a MCU module, without a development board, with a custom-made PCB.

## 2.3 Document Structure

The document begins with a full overview of the project's requirements based on priority, an overview of the system/subsystem architecture and design philosophy.

Second, the report details elements of the final design based on the system architecture, alongside justifications for each design choice. In addition to the final design elements, the report also discusses the assembly process of the final designed product, reflects on stakeholder engagement, identifies and reflects on the mitigation of safety issues and risk mitigation and discusses potential ethical issues relating to the design project.

Lastly, the report summarises the design outputs from throughout the design process, analysis the expenditure from the design project, includes recommendations and further development opportunities based on the design project team's experience, and evaluates the completion level of final designed product and our expectations for future demonstration.

## 2.4 Definitions, Acronyms, and Abbreviations

*Table 1: Acronyms and Abbreviations*

| Item | Definition |
| --- | --- |
| ADC | Analog-to-Digital Converter |
| AEL | Accessible Emission Limit |
| AGC | Automatic Gain Control |
| ANFF | The Australian National Fabrication Facility |
| ARPANSA | Australian Radiation Protection and Nuclear Safety Agency |
| ARQ | Automatic Repeat Request |
| AS | Standards Australia |
| BER | Bit Error Rate |
| BJT | Bipolar Junction Transistor |
| BMS | Battery Management System |
| CAD | Computer Aided Design |
| CRC | Cyclic Redundancy Check |
| EMC | Electromagnetic Compatibility |
| EMI | Electro Magnetic Interference |
| ESD | Electrostatic Discharge |
| ESP-IDF | Espressif IoT Development Framework |
| FAQ | Frequently Asked Questions |
| FEC | Forward Error Correction |
| FPGA | Field Programmable Gate Array |
| FSO | Free Space Optical |
| FSOCS | Free Space Optical Communication System |

| | |
| --- | --- |
| GPIO | General Purpose Input/Output |
| HAL | Hardware Abstraction Layer |
| HID | Human Interface Device |
| I2C | Inter-Integrated Circuit |
| IEC | International Electrotechnical Commission |
| IEEE | Institute of Electrical and Electronics Engineers |
| IoT | Internet of Things |
| ISR | Interrupt Service Routine |
| LoS | Line of Sight |
| MCU | Microcontroller Unit |
| MDF | Medium-Density Fiberwood |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| MSC | Mass Storage Class |
| NRZI | Non-Return to Zero Inverted |
| NZS | Standards New Zealand |
| OS | Operating System |
| PC | Personal Computer |
| PCB | Printed Circuit Board |
| PLA | Polylactic Acid |
| PPE | Personal Protective Equipment |
| PPIR | Preliminary Performance Impact Report |
| PWM | Pulse Width Modulation |
| RF | Radio Frequency |
| RTOS | Real Time Operating System |
| RX | Receiver |
| SMD | Surface Mount Device |
| SWOT | Strength Weakness Opportunities Threats |
| TDD | Time Division Duplex |
| TIA | Transimpedance Amplifiers |
| TQ | Technical Query |
| TTL | Transistor-Transistor Logic |
| TX | Transmitter |
| USB | Universal Serial Bus |
| UWA | The University of Western Australia |
| VBUS | Voltage Bus |
| VCSEL | Vertical-Cavity Surface-Emitting Laser |
| VIH | Voltage Input High |
| VIL | Voltage Input Low |

## 2.5 Contribution Summaries

### *2.5.1 Anamika Joby*

The two-way FSO system project was initiated for me with an extensive literature review focused on FSO communication principles and previous designs in the area. I contributed to the primary LTSpice simulations for the laser diode driver circuit design and was involved in the breadboard prototyping that followed. At this stage also made procurement of electronic for circuit updation. Involved in the assembly, troubleshooting and testing of the laser diode driver module. Later, did the dot board prototype assembly for the transmitter circuit. Reviewed initial schematic for PCB, revised it and did the PCB design on EasyEDA.

For the receiver circuit, I was involved in the prototyping and troubleshooting throughout all the stages of design evolution of the circuit. Starting with single stage receiver breadboard tests to three stage dot board prototype testing. Prepared an initial receiver schematic on KiCAD then later moved to EasyEDA. Performed the PCB design on EasyEDA in the light of the lessons from the previous MCU design to meet system integration requirements and revised it after getting it collaboratively reviewed by the team. Handled the procurement of the laser diode driver and receiver PCBs from JLCPCB.

Involved in all the FSO link tests starting with Arduino based primary testing of the transceiver to the HID peripherals-based tests of the system. Compiled all the FSO based tests for documentation purposes. Made measurements of the PCBs to assist with chassis design.

Beyond hardware development, I served as the client liaison manager, posting technical queries and attending interactive sessions with clients. I chaired team meetings and took meeting minutes. I contributed significantly to the team documentation and supported quality control across submitted documentation. Throughout the project, I kept the team informed about key milestones and deliverables, helping maintain clarity of goals.

### *2.5.2 Ethan Tan*

Throughout the design process, my contributions were mainly on the development of the chassis to ensure the completion of the designed solution met the expectations of stakeholders. In addition to the development of the chassis, I would lead the project management side of the project ensuring documents were updates and superseded content was archived correctly.

In addition to document control, I would keep track of all financial activity ensuring costs remained within the $500 budget by creating a bill of materials, creating references for invoices and receipts and updating the team weekly of expenditures and budgeting.

Furthermore, I would lead most report writing sessions completed by the design team, and would begin report writing in advances for the design project team to ensure that the quality of the report was consistent to the work completed by the team.

Beyond the chassis and project management, I would act as the project chair and complete all minute taking for two weeks of the design project. Additionally, I have assisted in the testing and prototyping of the transmitter circuit simulations on LTSpice, helped with the construction and soldering of the receiver circuit during initial testing phases, and assisted in the testing of USB peripherals on a solder protoboard and in its final stages when using a PCB.

### *2.5.3 Layla Kim*

To ensure the successful implementation of the FSO communication system, I conducted an extensive literature review focusing on latency performance and Class 1M laser safety compliance. Based on this research, I selected appropriate components and calculated key parameters such as resistance values, current limits, and optical power thresholds to guarantee both reliable operation and compliance with Class 1M standards.

I designed and simulated the transmitter circuit using LTspice, developed the initial PCB schematic using EasyEDA, and built and tested the laser diode driver and receiver prototypes while verifying the current clamp functionality and laser safety.

During PCB testing, I participated in resolving several hardware issues, including removing the MCU board diode that blocked USB power input, correcting the reversed diode polarity in the transmitter circuit, and designing and soldering an additional inverting op-amp stage to fix the negative output voltage problem in the receiver circuit.

I also developed and debugged the FSO testing firmware to support end-to-end hardware validation. Furthermore, I participated in online technical meetings to discuss circuit performance, served as the liaison to ensure effective communication between team members, and contributed to report writing and quality review to maintain consistency and technical accuracy throughout the final submission.

### *2.5.4 Luisa Puliafito*

Throughout the development of the 2-Way FSOCS, my primary contributions focused on the hardware design, integration, and validation of the system's core control and communication architecture. I led the MCU circuit design, developing a fully custom PCB based on the ESP32-WROOM1 module. This included schematic capture, pin mapping, power distribution layout, and signal interfacing with the transmitter and receiver modules. I also conducted component analysis and model selection, justifying the choice of the ESP32 for its integrated USB functionality, wireless expandability, and cost efficiency compared to FPGA or Raspberry Pi alternatives.

Additionally, I managed the manufacturer selection process, evaluating options between JLCPCB and PCBWay based on fabrication quality, turnaround time, and cost. My decision ensured consistent production quality within the project's $500 AUD budget.

I contributed to the chassis design and 3D printing, creating modular enclosures that provided mechanical stability, optical alignment accuracy, and ease of assembly. Beyond technical design, I played a central role in testing and prototyping, performing key validation procedures to verify power integrity, bidirectional communication, and system safety. I also assisted in project management, coordinating documentation, test reporting, and ensuring all deliverables aligned with functional, safety, and design requirements.

Through these combined contributions, I helped ensure that the final FSOCS prototype achieved its intended performance, reliability, and safety goals within scope, schedule, and budget.

### *2.5.5 Sahan Pothupitiya*

As software lead within the collaborative team the remit centred on architecture, standards, and day-to-day technical coordination for the 2-Way FSOCS. The focus was on aligning software behaviour with system requirements, maintaining clear documentation, and ensuring that design decisions were traceable and reproducible.

Code was structured into coherent layers-hosting, emulation, and link transport-with stable interfaces and configuration conventions. Version control practices, review criteria, and lightweight release procedures were introduced early to reduce integration friction and make defects easier to localize. Integration progressed deliberately to manage risk and demonstrate evidence at each stage: baseline examples were validated. A wired UART bridge between two ESP32-S3 boards established reliable end-to-end behaviour, standalone FSO tests confirmed viability and finally, the optical path was combined with HID and MSC roles for full-path verification. For each phase, test plans, acceptance criteria and notes were prepared so results could be repeated and independently checked.

Beyond firmware, my support covered contributing on PCB design input, assisted with prototype assembly and test, and performed SMD and through-hole modifications in consultation with the hardware authors. In parallel, I maintained quality assurance for documentation by keeping defect and change logs, applying reviews and aligning report content with agreed acceptance criteria.

Taken together, these contributions helped the team converge on a working prototype that met the agreed functional and design requirements, while maintaining a constructive and respectful team environment.

### *2.5.6 Shirley Mziray*

For this project, contributed by leading the end-to-end design and delivery of the optical transmitter module, including research, LTSpice simulation, breadboard prototyping, PCB schematic design in EasyEDA, PCB layout drafts and final PCB bring-up and testing. I developed the custom laser-diode driver topology, implemented the adjustable current-clamp and contributed to verifying its behaviour across prototype and PCB stages, producing the measured results used in the safety documentation.

Additionally, I performed equivalent full-life-cycle work on the receiver module, including literature review, simulation and design iterations, prototype assembly and verification, EasyEDA schematic design and initial PCB layer routing. I wrote and executed FSO testing code used during optical link experiments and participated in various test sessions that validated bidirectional HID and MSC operation, latency, range (4.6 m) and link-loss recovery. I also reviewed MSC/firmware work and assisted with software debugging where needed to ensure end-to-end interoperability.

Beyond hardware and test activities, I contributed the transmitter and receiver documentation, the laser-driver design notes, and contributed substantially to the maintenance project risk register. I supported project administration by chairing meetings and taking minutes, contributed to relevant parts procurement and participated actively in prototype refinements, test log collection and the organisation of deliverables for repository handover.

# 3. Final Design and Design Process

## 3.1 Final Requirements Prioritised

As stated in our Requirements Analysis document, using the project brief, TQs, and extended research on the design project, we can define a list of requirements which when met, ensure that the designed solution meets the client's expectations and needs.

The Table 2 below details the six categories of requirements for the design project and includes the IDs of each category.

*Table 2: Requirements Categories and IDs*

| Requirements Category | ID |
| --- | --- |
| Functional Requirements | FR |
| Physical Requirements | PHY |
| Performance Requirements | PR |
| Power Requirements | PWR |
| Safety Requirements | SR |
| Design Constraints | DC |

The definition of each category is defined as follows:

1. Functional Requirements (FR) - Describes what the system must do, such as the core features and functions expected by the clients.
2. Physical Requirements (PHY) - Defines the qualities of the physical chassis of the design project to meet the needs of the client. These requirements are mostly team defined.
3. Performance Requirements (PR) - Describes how well the system must perform its functions. These are measurable criteria such as the latency, distance between modules, and reliability based on TQs with the clients.
4. Power Requirements (PWR) - Specifies how the system is powered and its energy consumption constraints such as expected operation times, and current constraints. These requirements are based on the design project brief and TQs.
5. Safety Requirements (SR) - Outlines the mandatory standards and features necessary to ensure the system does not harm users, the public, or the environment. This is based on the design project brief and standards upheld by AS/NZS.
6. Design Constraints (DC) - Imposes limitations on the design process itself, such as required components, development methods, or the final physical implementation. These constraints are mainly defined through the design project brief.

The requirements were categorised based on the six definitions and were ranked using our own multi-criteria scoring matrix. This ranking methodology resulted in the following requirements being ranked from most important to least.

**Error! Reference source not found.** highlights the top 20 requirements for the design project, while Appendix A highlights the remaining requirements that are ranked 21st or below.

*Table 3: Top 20 Requirements*

| Rank | Requirement ID | Description |
| --- | --- | --- |
| 1 | FR-02 | The system shall feature a standard USB (Type-A) interface on each module. |
| 2 | FR-01 | The system shall provide bidirectional data communication over a free-space optical link. |
| 3 | SR-1 | The system shall adhere to the Class 1M eye-safety standard as defined in AS/NSS IEC 60825.1:2022. |
| 4 | FR-07 | The system shall use a custom-designed laser diode driver. |
| 5 | FR-12 | The final design shall be implemented on a custom-designed Printed Circuit Board (PCB). |
| 6 | FR-08 | The system shall implement a CRC-based error detection scheme on all transmitted data packets. |
| 7 | FR-03 | The system shall support the operation of a single standard USB peripheral (keyboard, mouse, or data stick) at a time. |
| 8 | FR-05 | Each module shall be designed to mitigate interference from its own reflected laser light. |
| 9 | FR-11 | The laser driver shall incorporate a user-adjustable current clamp. |
| 10 | PR-1 | The system shall operate over a free-space distance of 2 meters with a Bit Error Rate (BER) of less than $10^{-9}$. |
| 11 | PR-2 | The system shall support a data transfer rate equivalent to USB 2.0 Full-Speed (12 Mbps). |
| 12 | PR-5 | The system shall implement an Automatic Repeat Request (ARQ) protocol to re-transmit corrupted or lost data packets. |
| 13 | PR-3 | The system shall exhibit a latency less than 50 ms for mouse and keyboard operations to allow for comfortable use of standard office peripherals. |
| 14 | FR-04 | The system shall automatically detect the type of peripheral connected without requiring manual user switching. |
| 15 | PWR-1 | The host-side module shall be powered entirely from the host's USB port. |
| 16 | FR-06 | The system shall automatically recover and re-establish the communication link after a temporary interruption |
| 17 | PWR-3 | The battery-powered module shall operate continuously for a minimum of 2 hours on a full charge. |

| | | |
|---|---|---|
| 18 | PWR-2 | The peripheral-side module shall be powered by a standard commercial USB and power bank. |
| 19 | PR-6 | The system shall maintain all performance requirements (including BER and latency) when operating under ambient indoor laboratory lighting conditions-up to 1000 lux. |
| 20 | FR-09 | The system shall enter a safe state (e.g., laser off) if the MCU firmware detects a critical fault. |

## 3.2 Architecture Overview

The final version of our design project's system/subsystem architecture is based on the requirements developed, the project brief by ANFF, and the TQs from weekly information sessions. This splits the project into three separate systems as shown in Figure 1 below.

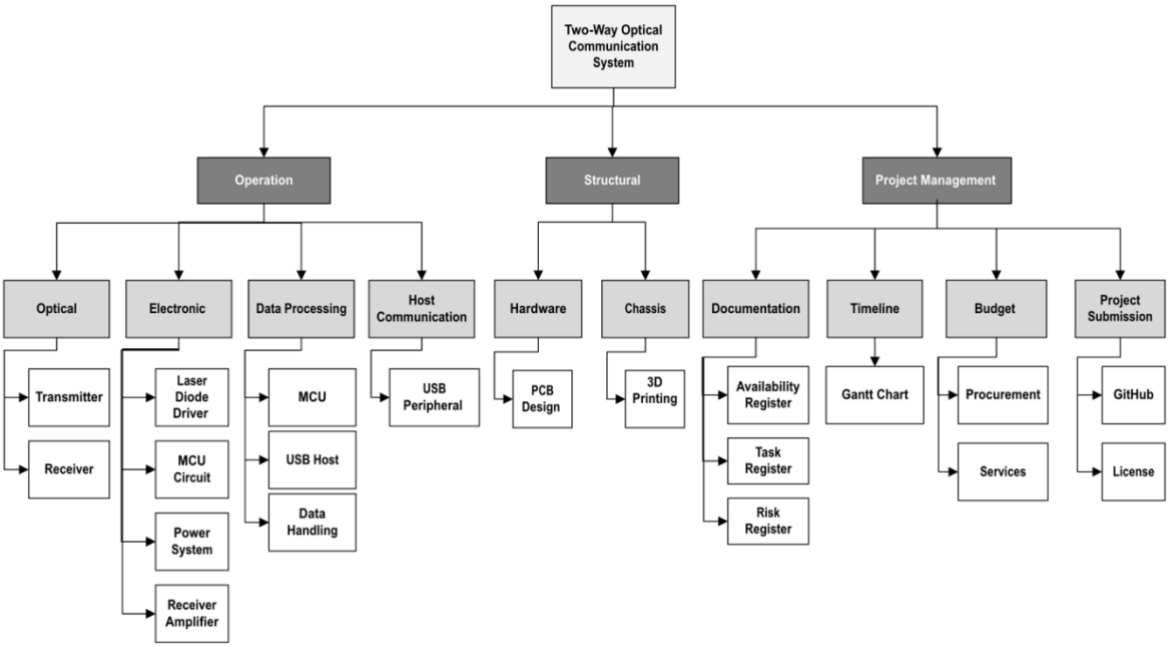


*Figure 1: System/Subsystem Architecture of the Design Project*

The project management system and the contents within this system are required for the documentation and administration of the design project. The documentation, timeline and budget subsystem contain files and management systems inspired by the Project Management Body of Knowledge [1]. While the project submission subsystem and its contents are based on the requirements sourced from the design project brief which requires the specifications of the final design to be licensed under an open-source license.

The operation and structural system of the architecture are based on the requirements from a combination of the design project brief, research, TQs and team defined objectives. This developed a list of requirements for both the Firmware and hardware of the design project which can be linked to the architecture we have created.

The operating system of the architecture fulfills the functional, power and performance requirements on the simulating, circuiting and coding of the design project. The structural system fulfills the safety and physical requirements on the PCB printing of the circuits and 3D printing of the chassis.

## 3.3 Design Philosophy

The functional design philosophy underpinning FSOCS is based on providing a transparent extension of USB connectivity over a free-space optical link. Central to the system's design is the goal of emulating the direct connection experience of a peripheral to a host, thereby enabling seamless operation of standard devices such as keyboards, mice, and flash drives without necessitating user intervention. The philosophy is built upon three foundational pillars: performance, reliability, and safety, which collectively justify the implementation of a custom designed architecture.

### *3.3.1 Pillar 1: Performance and User Transparency*

To deliver a “wired” user experience, the system prioritises low-latency, high-integrity, bidirectional data transfer. The architecture must support USB 2.0 Full-Speed (12 Mbps) data rates (PR-2) and ensure latency below 50 ms for HID (PR-3). Reliable error detection (FR-8) and automatic re-transmission protocols (PR-5) must maintain data integrity, making the optical link functionally transparent to both host and peripheral (FR-3). Critical interfaces between the MCU, transmitter, and receiver are designed to ensure precise timing and reliable signal processing.

### *3.3.2 Pillar 2: Reliability and Practicality*

From a functional point of view, the system is designed for resilience and practicality in its intended laboratory environment. It autonomously recovers from temporary link interruptions (FR-6) and detects peripheral type automatically (FR-4). The host-side module draws power solely from the host USB port (PWR-1), while the remote module operates for at least two hours on a standard commercial power bank (PWR-3). These design choices ensure consistent operation without user intervention, reducing failure risk.

### *3.3.3 Pillar 3: Safety*

User safety is a non-negotiable aspect of the design philosophy. The architecture adheres strictly to the Class 1M eye-safety standard (SR-1) and incorporates fail-safe logic to disable the laser if a critical fault is detected (FR-09). Ethical and professional obligations, including

user protection and compliance with IEC 60825.1:2022, were embedded throughout the design process, guiding laser power control and interface isolation.

Together, these functional imperatives delineate a design philosophy that harmonises performance, safety, and user transparency in meeting the operational requirements of the Australian National Fabrication Facility. A multi-stage custom receiver (FR-8) reliably detects weak, high-speed optical signals under ambient light conditions (PR-6). The entire system is implemented on a custom-designed PCB (FR-12). This approach harmonises high-speed performance, autonomous reliability, and uncompromising safety, which could not be achieved with off-the-shelf solutions.

This philosophy guided all stages of the project, including prototyping, component selection, simulation, and testing. Design decisions were continually evaluated against the pillars of performance, reliability, and safety to ensure compliance with requirements and feasibility for final implementation.

### 3.4 Final Design Elements and Justification

The following design elements implement the defined design philosophy in section 3.3, ensuring performance, reliability, and safety throughout the FSOCS. Central to this system is simplicity, modularity and efficient power management.

A portable power bank supplies energy to the ESP32 WROOM1 MCU, which serves as the central controller coordinating data flow between the receiver and transmitter modules. This arrangement allows for seamless bidirectional communication where the MCU processes incoming optical signals from the receiver and controls outgoing transmissions via the transmitter.

The transceiver employs a modular architecture, with physically independent transmitter and receiver modules circuits. This enhances flexibility, scalability and ease of customisation, whilst still maintaining high signal integrity by eliminating interfaces that could occur if both modules were integrated on a single PCB.

Additionally, using a single low power MCU reduces hardware complexity and energy consumption, thereby supporting the system's portability and functional efficiency for the required embedded or wireless communications applications.

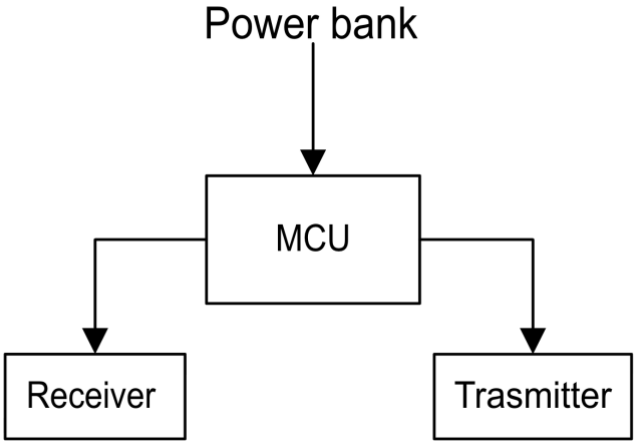


*Figure 2: Hardware Design Structure*

The use of independent modules also facilitates iterative design changes and simplified troubleshooting during development. Meaning each module can be tested and isolated individually, allowing quick identification and resolution of issues encountered during integration and dull system operation. This approach ensures that both functional performance and system reliability are maintained throughout the development lifecycle.

### *3.4.1 Manufacturer Selection and PCB Design*

Selecting a PCB manufacturer was crucial to ensuring precision, quality, and timely production within the $500 AUD budget (DC-1) and project timeline. JLCPCB was chosen for its excellent cost-performance ratio and seamless integration with EasyEDA, which streamlined design verification, Gerber generation, and instant quoting. Its express fabrication service delivered prototype boards within four business days, supporting rapid testing and iteration.

In comparison, PCBWay offered higher-end manufacturing but required manual file submission, had longer lead times, and involved greater costs, making it less practical for a university prototype project. JLCPCB's affordability, reliability, and speed made it the optimal choice for the FSOCS PCB fabrication.

### *3.4.2 MCU Selection and Justification*

One of the important design choices in the creation of the FSOCS was selecting the ESP32-WROOM1 MCU to act as the main processing platform. The MCU selection was based to directly met the project's functional and performance requirements:

- The system required bidirectional USB data transfer over free-space optical links with low latency (FR-1, PR-3).

- It also had to emulate USB host and peripheral roles, automatically detecting connected devices such as keyboards, mice, and flash drives (FR-4, FR-3).

This was determined after considering possible contenders such FPGA modules and Raspberry Pi systems based on technical, financial, and operational project specifications [2]. The STM32F4 (Cortex-M4) MCU was a close second, with high performance, several ADC channels, and USB OTG capability [2]. However, it had a more sophisticated firmware environment (STM32CubeIDE and HAL libraries), with only limited open-source USB stack options available for HID and MSC applications. Furthermore, it was more expensive and had higher power consumption, which decreased its viability in the portable peripheral module. While very accessible and very easy to program, the Arduino Mega only runs at 16 MHs, which was too slow to produce accurate high-frequency PWM pulses needed in 12 Mbps optical modulation [3]. It also has no integrated USB host capability, which necessitates external USB shield hardware adding cost, board space, and latency. It also only had limited RAM (8 KB), which limited real-time buffering capability to correct errors and perform packet retransmission (FR-6).

The ATmega328P was eliminated early due to its negligible processing capability, non-natural USB interface, and inadequate memory to support complex dual-role USB communication [4]. It was unable to satisfy the latency (<50 ms) and data rate (12 Mbps) specifications outlined in PR-1 and PR-3. FPGAs can have high precision timing control and parallel data processing that are useful in optical modulation. However, Firmware implementation of USB protocol and microcontroller-like behaviour requires a soft-core processor (MicroBlaze or Nios II), which increases the complexity significantly and adds much toolchain overhead. Power consumption (typically >500 mA) and cost (> $100) also went past project restrictions. FPGAs were technically superior then but impractical in this project scale and schedule.

The Raspberry Pi was considered due to ease of program and full OS environment [5]. However, being non-real-time, Linux adds unpredictable timing jitter that disqualifies it from deterministic laser control and high-speed ADC sampling. In addition, its high-power consumption and its dependency on SD card to boot made it incompatible with incorporation into embedded systems.

*Figure 3: Wroom1 ESP32 Module*

The ESP32-WROOM1 presented the best trade-off between performance, power efficiency, capability to integrate other peripherals, and cost and was hence the best MCU to utilise in the system with its assigned task. The MCU selection was based to directly met the project's functional and performance of the design. Furthermore, this allowed for other tasks to be commenced in early stages of the project by using a commercial prototyping Esp32 Board.

### *3.4.3 MCU System*

The principals governing the MCU design require to ensure the functionality, reliability and compatibility with the intended application. The main structure block that composes the design of a functional MCU include Power Supply Requirements, I/O Pin Configuration, Communication Interfaces, Reset Circuit. This design has been inspired and designed using technical advice and ESP32 Hardware Design Guidelines that are found on the WROOM 1 Module [2].

To avoid malfunction or damage, the MCU must function within its designated voltage range, which is normally 3.3V or 5V. Depending on efficiency and thermal requirements, switching converters or Low Dropout Regulators (LDOs) provide voltage regulation. Effective decoupling is crucial the larger capacitors (such as 10 µF) stabilise voltage during transient loads, while 0.1 µF ceramic capacitors should be positioned near the MCU's power pins for high-frequency noise suppression. The I/O pins in the WROOM1 need to be set up for input/output modes, proper voltage levels, and ESD protection.

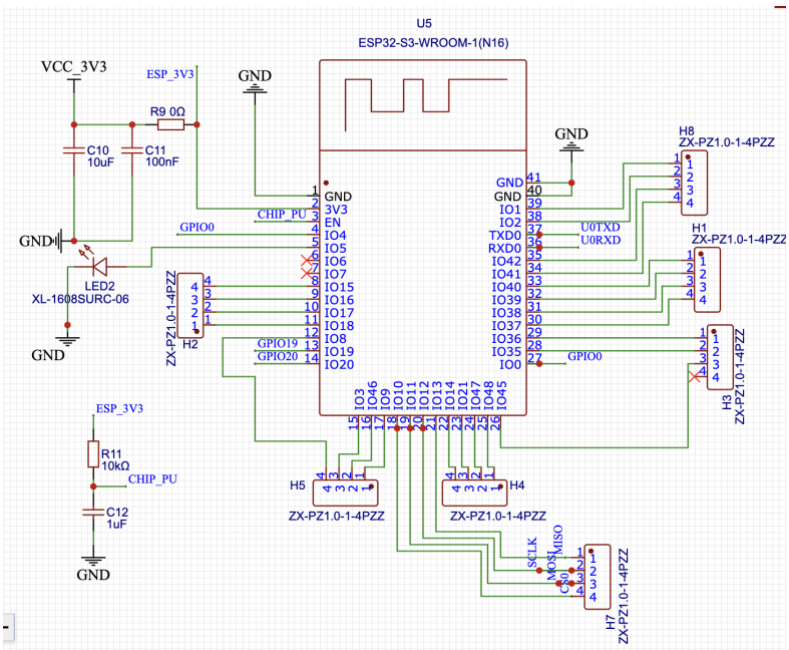


*Figure 4: MCU WROOM1*

To connect the MCU to external devices like sensors, memory modules, and other controllers, communication interfaces are essential [6]. The selection of common serial communication protocols, such as UART, SPI, and I²C, should be based on device compatibility and application requirements. To guarantee adherence to the USB standard, USB interfaces frequently call for extra parts like transceivers, pull-up resistors, and ESD protection devices. Level-shifting integrated circuits are commonly used in RS-232 interfaces to achieve the necessary voltage requirements.

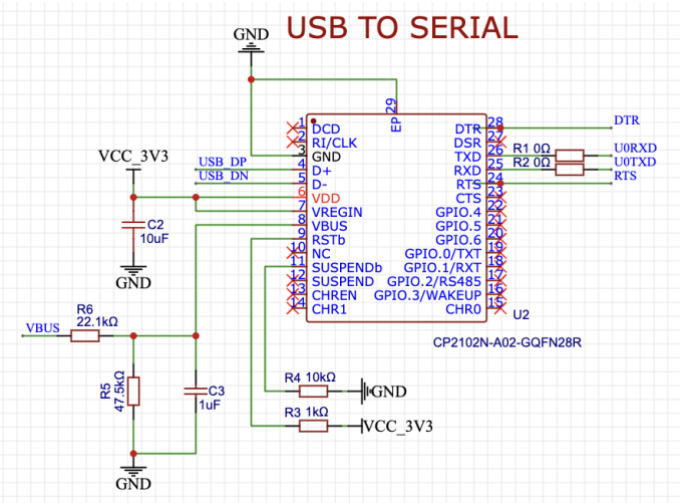


*Figure 5: MCU USB-To-Serial*

The USB-to-Serial interface, illustrated in Figure **6**, enables communication between a host computer and the microcontroller through a USB connection [6]. The circuit utilises the CP2102N-A02-GQFN28R USB-to-UART bridge IC (U2), which converts USB data signals into standard UART format. This allows the MCU to interface with PCs and other USB-equipped devices for programming, debugging, or data transmission.

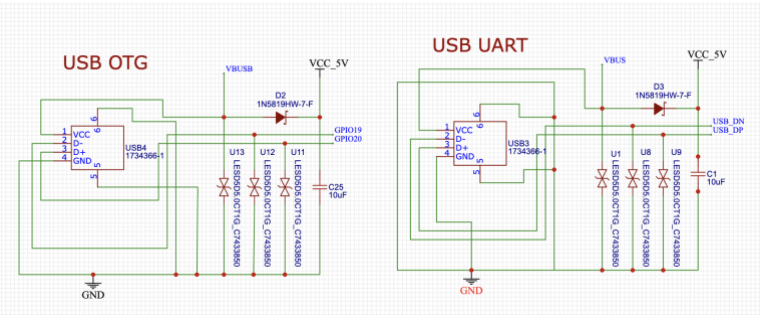


*Figure **6**: MCU USB OTG/UART*

The USB OTG interface utilises a Micro-B USB connector (USB4, 1734366-1) to establish the physical connection. The VBUS line from the connector is connected to the system 5 V rail (VCC_5V) through a Schottky diode (D2, 1N5819HW-7-F), which provides reverse-current protection. This prevents current backflow into the USB port when the system operates in host mode. While the ESD protection diodes (U11–U13, LESD5D5.0CT1G) are used to protect the USB data (D+ and D−) and power lines from voltage transients and electrostatic discharge.

The 10 µF capacitor (C25) is placed across the 5 V supply line to stabilise voltage levels and suppress noise. The microcontroller GPIO pins GPIO19 and GPIO20 are connected for OTG control, allowing firmware-based detection and management of host or device mode transitions. The pins are specifically identified from the specification of the ESP32 Technical Specifications.

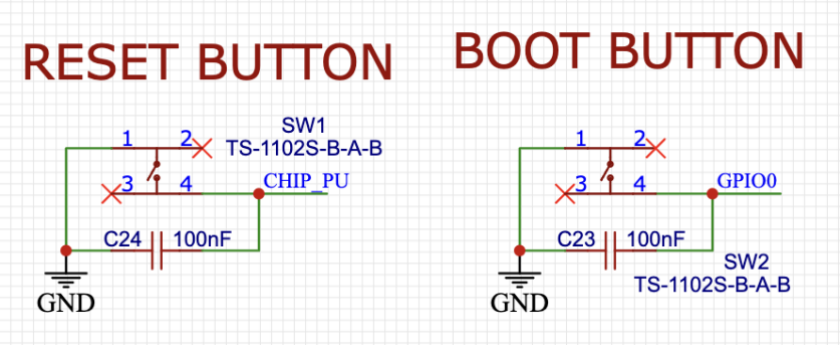


*Figure 7: MCU Reset/Boot Button*

A push-button reset circuit provides a convenient means for manually restarting the microcontroller. This feature is particularly valuable during system development and debugging, allowing for easy recovery from unexpected or unstable system states. A dependable reset circuit, which is frequently implemented using a pull-up resistor and capacitor network or a dedicated reset IC, guarantees that the MCU starts in a known state following power-up or fault conditions.

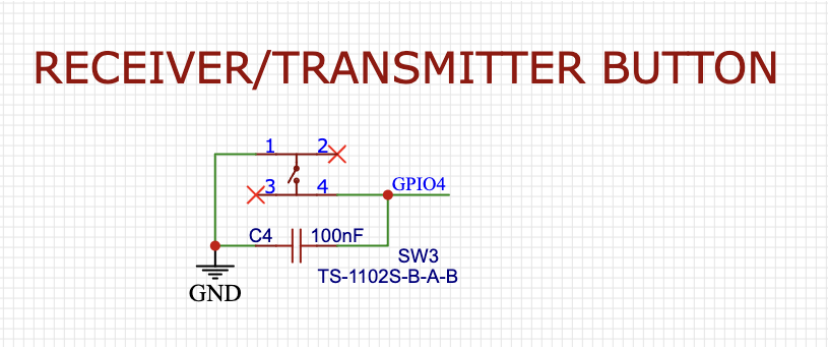


*Figure **8**: Receiver/Transmitter Button*

An additional Button has been included in the circuit to integrate the hardware system with the transceiver circuit. The Receiver/Transmitter Button circuit, shown in Figure **8**, provides a manual input interface for toggling communication nodes or initiating transmission and reception signal functions in the microcontroller system.

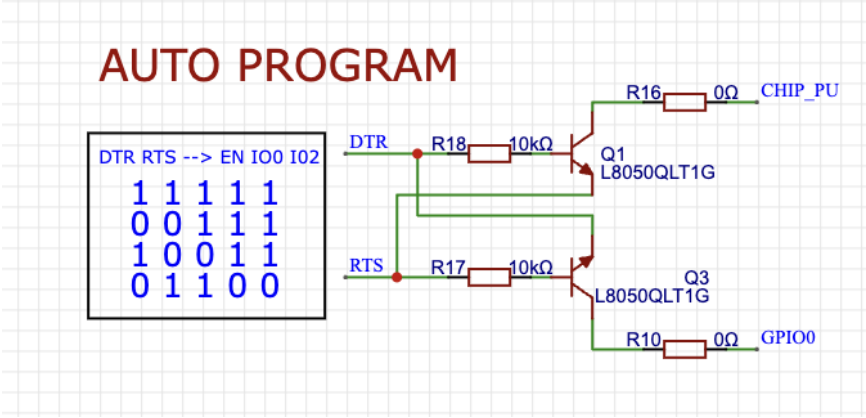


*Figure **9**: MCU Auto Program*

The Auto Program Circuit, shown in Figure **9**, provides an automated method to place the microcontroller into programming mode when connected via a USB-to-serial interface. This eliminates the need for manual button operation during firmware upload, streamlining both development and production processes.

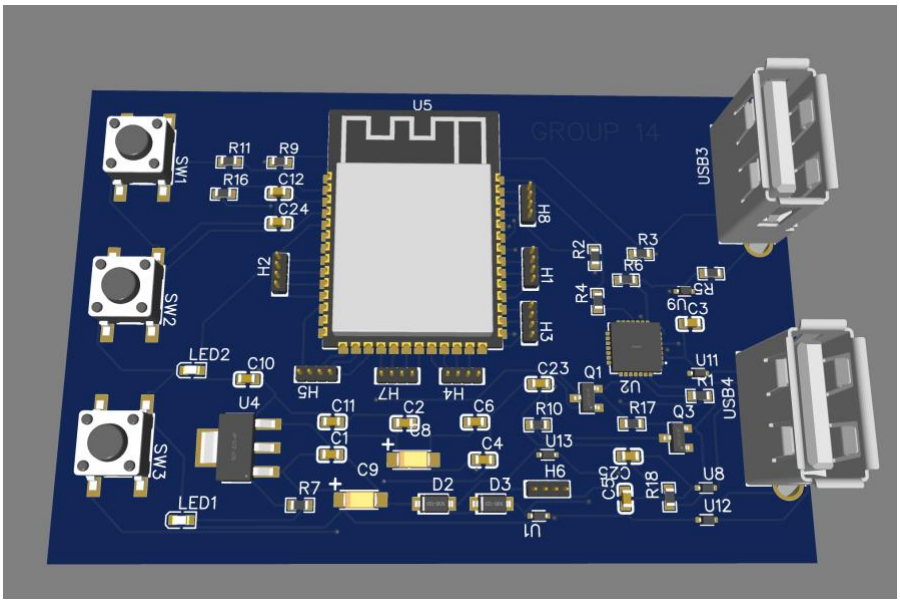


*Figure **10**: Final MCU PCB design*

The circuit interfaces with the DTR (Data Terminal Ready) and RTS (Request to Send) control signals from the USB-to-serial converter. These signals are manipulated by the host computer through the serial port control lines during programming. Thus, the control lines are connected to the bases of two NPN transistors through base resistors R18 and R17 (both 10 kΩ). In this way, the transistors function as level inverters that momentarily pull the microcontroller's CHIP_PU (EN) and GPIO0 lines low in a specific sequence, as required to initiate the bootloader mode. A 3D model design after finalising the circuit in the PCBCad Software is shown above in Figure **10**.

#### 3.4.3.1 Testing and validation

Test T004.1, titled “Power and Operation Time - MCU Circuit Reliability and Performance,”( refer to Appendix C section 9.3.6) evaluated the integrity, reliability, and electrical safety of the MCU circuit in the FSOCS. The test confirmed proper power sequencing, voltage regulation, and the absence of shorts or instability under nominal conditions.

The MCU’s soft-start behaviour was assessed using a bench power supply set 20-50% above idle current limits, verifying stable regulation across the 3.3 V, 1.8 V, and VUSB rails with acceptable ripple levels. The PCB was powered from a 4.5 V regulated supply on an ESD-safe surface, with oscilloscope and DMM probes monitoring key nodes.

During early trials, capacitor C9 failed due to reversed polarity, shared by capacitor C8 causing a short in the regulator circuit. After correcting their orientation, the MCU operated normally and met all criteria for PWR-1, PWR-2, and PWR-3, confirming a robust and reliable power subsystem for further system integration.

Test T004.2, titled "Power and Operation Time - MCU Circuit Reliability and Communication Performance" ( refer to Appendix C section 9.3.79.3.6) tested the power stability and USB connection of the DIY ESP32-S3 MCU used in the FSOCS. The aim was to confirm stable power control and communication of the MCU with a host computer. It was tested on an ESD-safe bench utilising the 5 V USB input of a modified USB-A to USB-A cable. The onboard regulator of the MCU delivered a steady 3.3 V output, validated by a multimeter and supported by oscilloscope test for signal integrity.

The board entered the programming mode correctly, performed firmware flashing using esptool.py, and booted up correctly, establishing a stable serial connection captured by the host PC. Power delivery and data transfer were steady during all testing.

All acceptance criteria of the PWR-1, PWR-2, and PWR-3 were achieved, guaranteeing the MCU's stable operation, power integrity, and reliable communication. These results confirmed the MCU circuit ready for full FSOCS system integration.

### *3.4.4 Transmitter Module Architecture and Justification*

The transmitter module constitutes the optical output stage of the transceiver, converting digital signals from the MCU into high-speed optical pulses. Its design followed a structured process of simulation, prototyping, and final PCB implementation, with each iteration refined to meet the performance and safety requirements of the project.

The transmitter was required to provide reliable On-Off Keying (OOK) modulation at up to 12 Mbps, operate from 3.3 V logic levels, and incorporate intrinsic hardware safety features to

comply with the Class 1M eye-safety standard (SR-1). To satisfy these, a custom laser diode driver (FR-7) was developed with a user-adjustable current clamp (FR-12).

#### 3.4.4.1 Design Evolution

The initial concept adopted a conventional low-side switching topology using a logic-level N-channel MOSFET and a series resistor for basic current limiting. While simple and suitable for proof-of-concept testing, simulations revealed current overshoot and lack of transient protection.

To address this, an active current clamp was integrated based on techniques from Texas Instruments notes [1]. This design used an op-amp feedback loop to monitor the voltage across a sense resistor and dynamically regulate the MOSFET gate drive, preventing the laser current from exceeding a defined threshold.

#### 3.4.4.2 Simulation Results

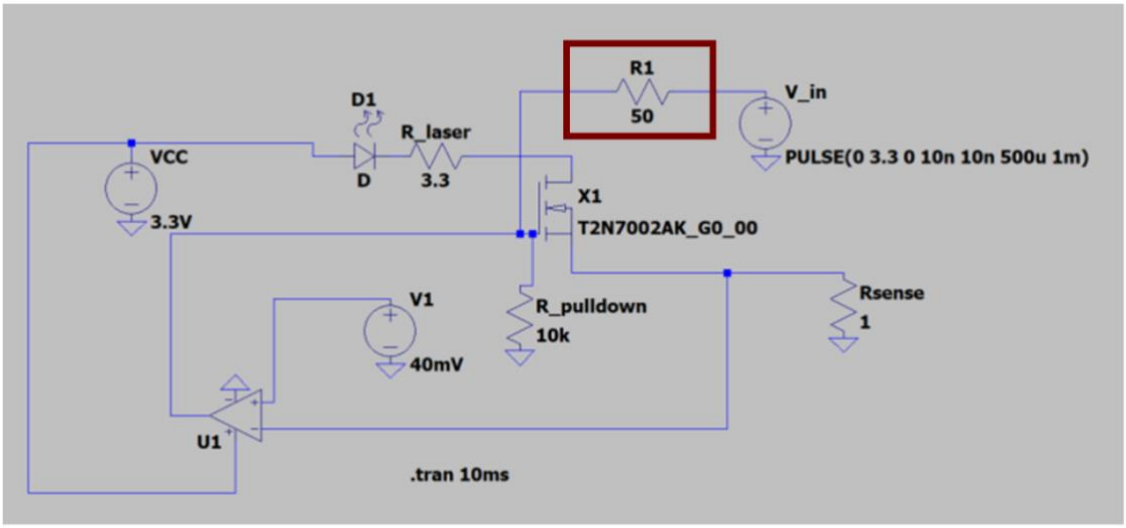


*Figure **11**: Laser Diode Driver Design 1*

Design 1 was simulated in LTSpice with the laser diode modelled using a diode + series resistance representation. The analysis showed transient overshoot and contention between the PWM and op-amp control signals. To address the contention and the gate control loop a 50 Ω resistor was added in series with the PWM input. This allowed for the correct clamping of the voltage.

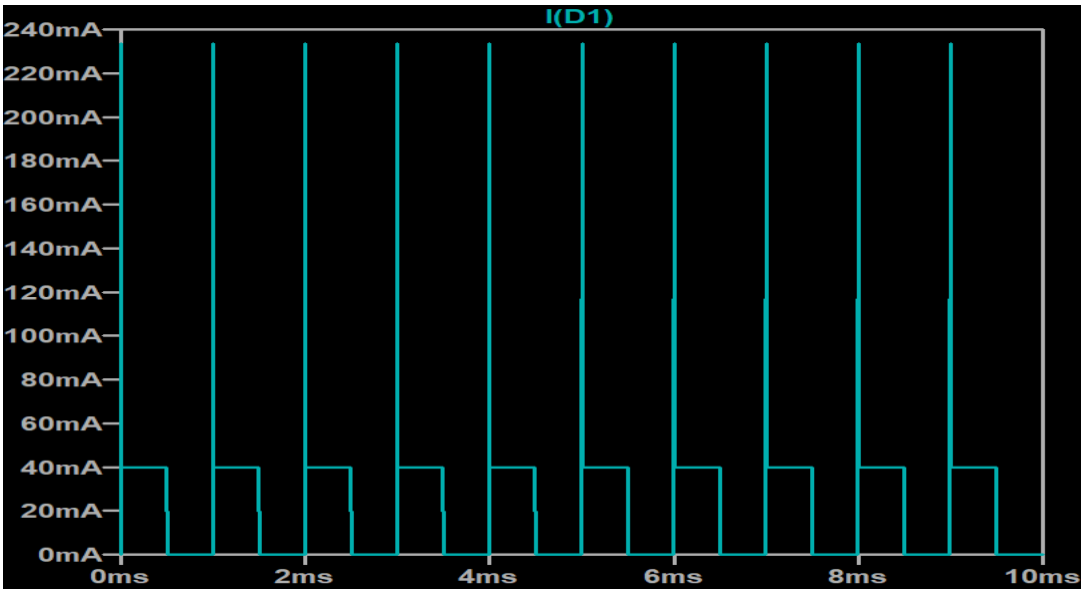


*Figure **12**: Transient Simulation of Design 1, with the addition of 50 Ω resistor*

A breadboard prototype (*Figure 13*) was assembled using readily available components to validate the simulations. The prototype confirmed the clamping functionality but revealed incomplete MOSFET turn-off, an issue that was later attributed to residual op-amp gate voltage.

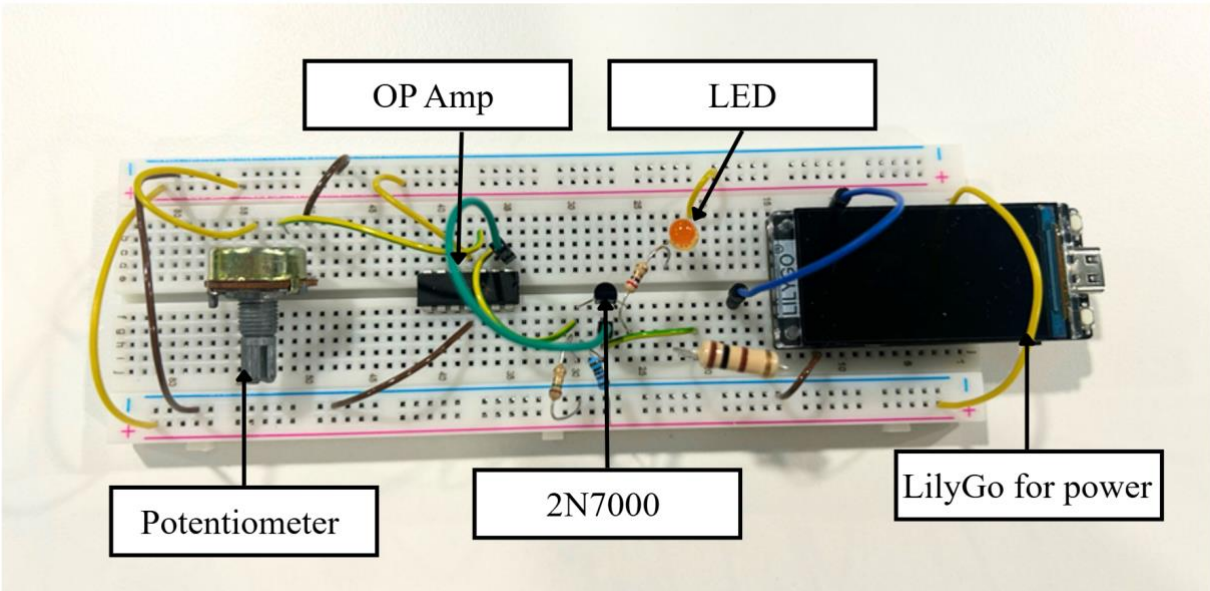


*Figure **13**: Breadboard Prototype of Design 1*

This was corrected by adding a small-signal diode between the op-amp output and the MOSFET gate, ensuring full discharge during the PWM low cycle. The final configuration allowed complete laser turn-off, verified both in simulation and in hardware.

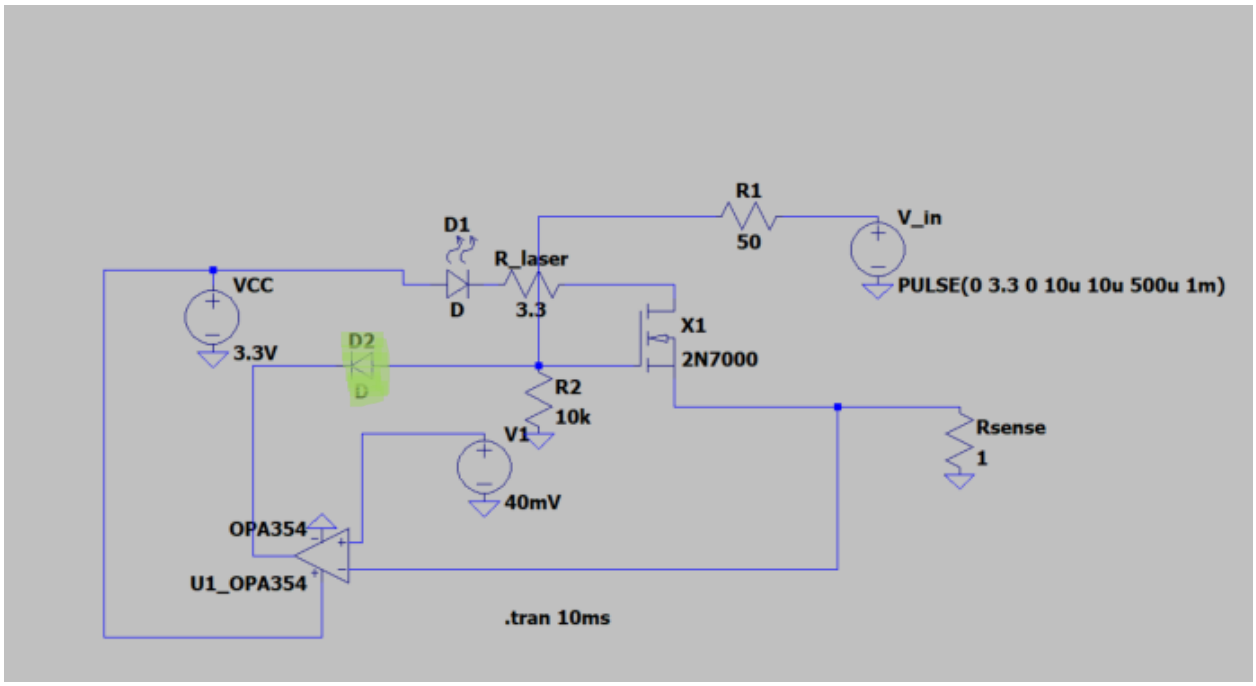


*Figure **14**: Laser Diode Driver Design 2*

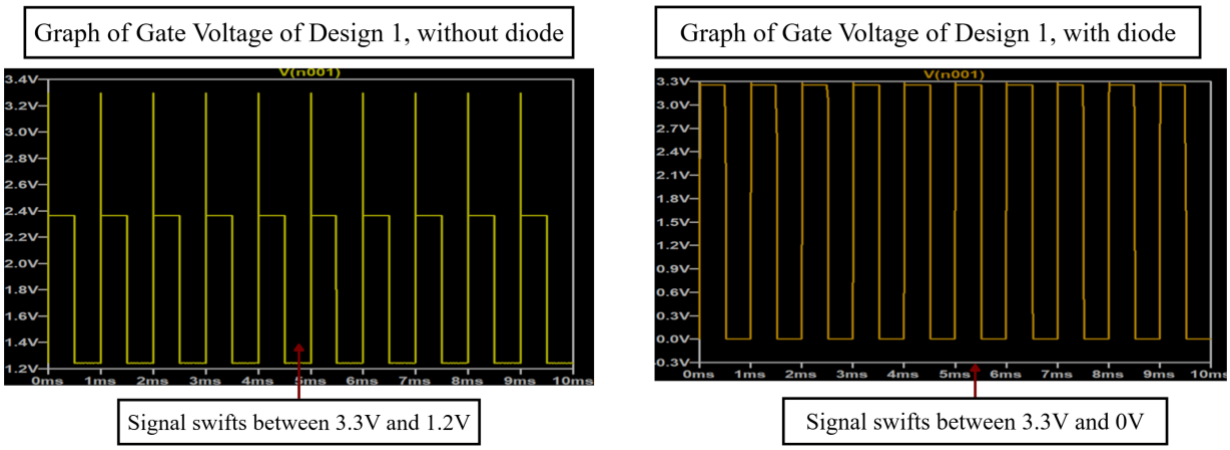


*Figure **15**: Showcasing the Difference in Gate Voltage after Addition of Diode*

#### 3.4.4.3 Key Components Selection and Justifications

I. Laser diode Selection

While the 1550 nm wavelength offers the highest eye-safety margin [3], it was excluded due to cost (DC-1). Instead, an 850 nm near-infrared VCSEL was initially selected for its low cost, high speed, capability and compatibility with silicon photodiode. The 850 nm wavelength represents an optimal compromise between safety, availability, and optical efficiency [4] (PR-6).

After extensive testing of the transmitter PCB, the originally selected 850 nm infrared laser was found to emit no optical output, making it unsuitable for use. In addition, visual alignment between the transmitter and receiver modules was not feasible due to the invisibility of the IR beam. To resolve this issue, the IR laser was replaced with a visible 650 nm red laser, which provided a clearly visible beam path. This modification significantly simplified alignment during system calibration and testing, ensuring accurate optical coupling and improved repeatability of results.

The design of the PCB had accounted for this contingency by including additional ports compatible with both laser types, allowing the substitution to be implemented without requiring any redesign of the hardware.

II. Collimating Lens

The OPV300 laser diodes 24° intrinsic beam divergence required a collimation to maintain proper received power at 2m (PR-1). A cost effective PMMA plano-convex lens with 38mm focal length was selected to ensure beam alignment and minimise the bit error rate (BER) without exceeding the project's budget constraints.

III. N-Channel MOSFET (2N7000)

The 2N7000 MOSFET is an inexpensive and widely available electronic switch. It was mainly chosen for its 3.3V logic compatibility and fast switching capability. Its drain current rating of 200mA exceeds the laser current requirements (0.39 mA), ensuring safe operation and low thermal stress.

IV. Operational Amplifier (OPA354)

OPA354 implements the current-regulating feedback loop. It was chosen for its high-speed characteristics, including 100 MHz GBW, 150 V/µs slew rate and rail-to-rail I/O, making it suitable for precision current regulation at MHz-scale PWM frequencies.

#### 3.4.4.4 Safety Clamp Design and Calculation

To comply with SR-1 and AS/NZS IEC 60825.1:2022, the driver current must be physically clamped to a level that keeps the laser's average optical power below the Class 1M limit. For a laser modulated with a high-frequency PWM signal, the output is treated as continuous-wave (CW) emission for safety calculations.

Class 1M Accessible Emission Limit (AEL) at 650 nm from IEC 60825-1, At $\lambda = 650\ nm$:

$$AEL = 3.9 \times 10^{-4} = 0.39\ \text{mW}$$

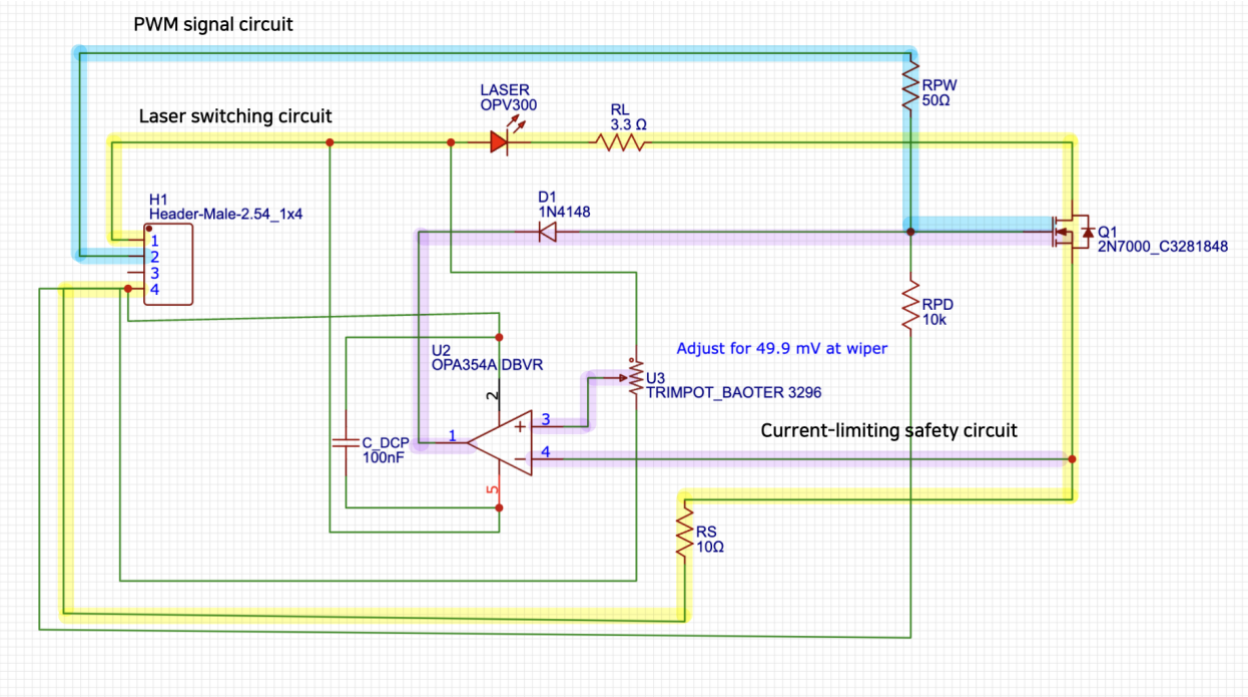


*Figure 16: Schematic of the transmitter circuit, will all components and their values*

#### 3.4.4.5 Validation and Testing

The final design was validated on a breadboard and thereafter on a PCB.

Test T-003.1 ( refer to Appendix C section 9.3.5), tested the OPV300 (850 nm infrared laser) using an IR camera; however, no emission was detected. This confirmed that the laser was not operating, although the lack of visible light was expected. Given the rated forward voltage of the laser diode is 2.2 V, while the measured voltage was 3.3 V, it is likely that excessive voltage caused permanent damage to the diode.
Therefore, a visible red laser (650 nm) was used for subsequent testing and alignment verification. However, since the red laser's datasheet did not provide a current-power characteristic curve, the current clamp was manually adjusted so that the optical output satisfied

the Class 1M AEL. The output voltage and current were measured using a multimeter and a clamp meter, respectively. At a forward voltage of 1.9 V and a drive current of 19 mA, the optical output power was measured to be approximately 0.36 mW. Since the AEL for a 650 nm Class 1M laser is 0.39 mW, this confirms that the transmitter complies with the safety standards**.**

Test T-002.1 (refer to Appendix C section 9.3.2), validated ability of system to transmit and receive PWM-modulated optical signals across 2 m (PR-1, FR-1). Using custom designed prototype transmitter (Figure 17) and receiver modules, the setup confirmed reliable communication by sending PWM signal from the transmitter end and monitoring signal integrity at receiver end. The receiver output replicated the 50 % duty PWM waveform, confirming signal integrity and stable optical modulation without link resets.

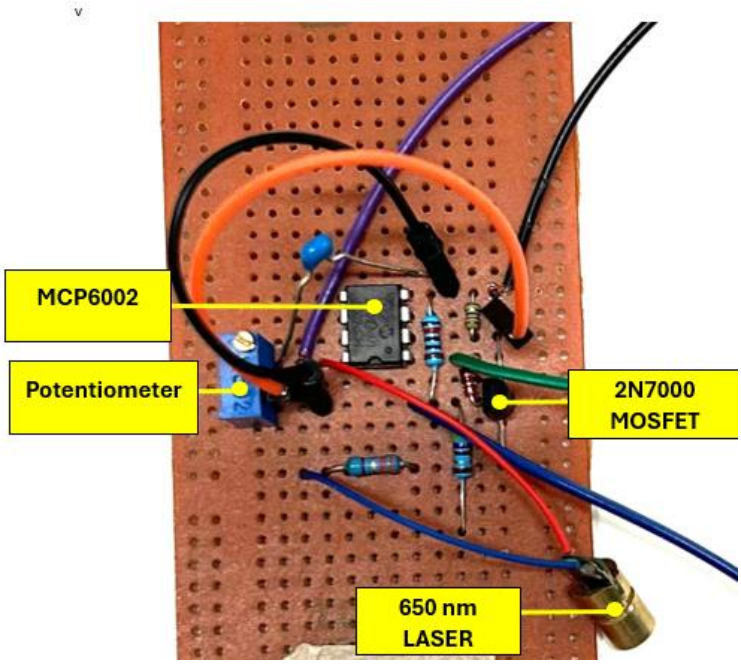


*Figure 17:Custom Laser Diode Driver Prototype Design 2*

#### 3.4.4.6 Requirements Compliance Summary

Based on the above tests, the final design of the transmitted module meets its key requirements as summarised below.

*Table 4: Summary of Requirements Compliance*

| Requirement ID | Description | Compliance Method |
| --- | --- | --- |
| FR-7 | Use a custom designed laser driver. | Implemented and validated via simulation and T-002.1 |
| FR-11 | Include a user-adjustable current clamp | Verified via op-amp feedback clamp engaging at 4 mA |
| SR-1 | Adhere to Class 1M eye-safety standard. | Achieved through hardware current limiting and laser selection |

#### 3.4.4.7 Design Refinement and Final PCB

The final transmitter module employs a hybrid digital-analogy topology combining direct PWM gate control with analogue feedback current limiting.

Alternative architectures, including op-amp-only gate drives and passive current-limiting networks, were evaluated but ultimately rejected due to their inadequate high-speed performance and limited control over optical power and eye-safety compliance.

LTspice simulations demonstrated that the op-amp-only configuration exhibited significant slew-rate limiting and waveform distortion when driving the MOSFET gate at the targeted MHz-range switching frequencies. This behaviour occurs because typical op-amps cannot source or sink the high transient gate-charge currents required to achieve fast rise and fall times.

Similarly, passive current-limiting methods reduced switching speed and prevented precise modulation control, making them unsuitable for the desired high-data-rate optical transmission and safety regulation requirements.

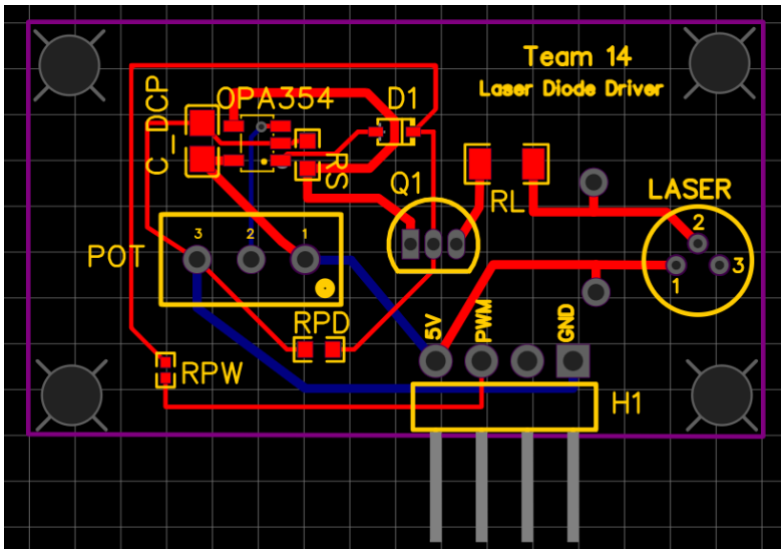


*Figure **18**: Laser Diode Driver PCB Design*

The final PCB for the laser diode driver is a two-layer FR-4 board (40.8 mm × 23 mm, 1.6 mm thick) made from flame-retardant, glass-reinforced epoxy laminate. The layout adheres to standard design rules with signal traces being 0.254 mm wide, power traces 0.5 mm wide, minimum clearance 0.152 mm, and via diameter 0.61 mm. Components and headers are clearly labelled; 3.3 mm diameter mounting holes are provided at the four corners, and 2.54 mm pin-headers are used for module interconnection.

Top copper layer carries most power and signal traces; the bottom copper layer carries the ground plane and select signal routing (to avoid interference near the OPA354). Component placements separate the power section from the analogue/op-amp section to minimize noise coupling. The board footprint also accommodates a visible 650 nm laser port as a contingency alongside the primary 850 nm IR VCSEL.

### *3.4.5 Receiver Module Architecture and Justification*

The receiver module's primary function is to convert the high-speed optical pulses transmitted by the laser diode into clean logic level electrical signals that can be processed by the MCU. The design approach was guided by the TIA principles [5]. The objective was to develop a TIA circuit capable of achieving both high sensitivity and fast response, suitable enough for the data rate required by the system.

In a standard TIA configuration, the gain is determined by the feedback resistor $R_F$, while the bandwidth is inversely proportional to $R_F$and the total input capacitance (dominated by the photodiode). This creates an inherent trade-off between gain and speed where higher gain limits bandwidth, but higher bandwidth reduces gain.

Using design equations from [5], component values ($R_f$ *and* $C_2$) were iteratively selected through simulation to achieve an output voltage of approximately 3 V. The design 1 network (Figure **19**) consists of a 1 kΩ resistor and a 10 pF compensation capacitor to suppress ringing and ensure stable high-speed operation.18) consists of a 60 kΩ resistor and a 3.1 pF compensation capacitor to suppress ringing and ensure stable high-speed operation.

#### 3.4.5.1 Receiver Design Evolution

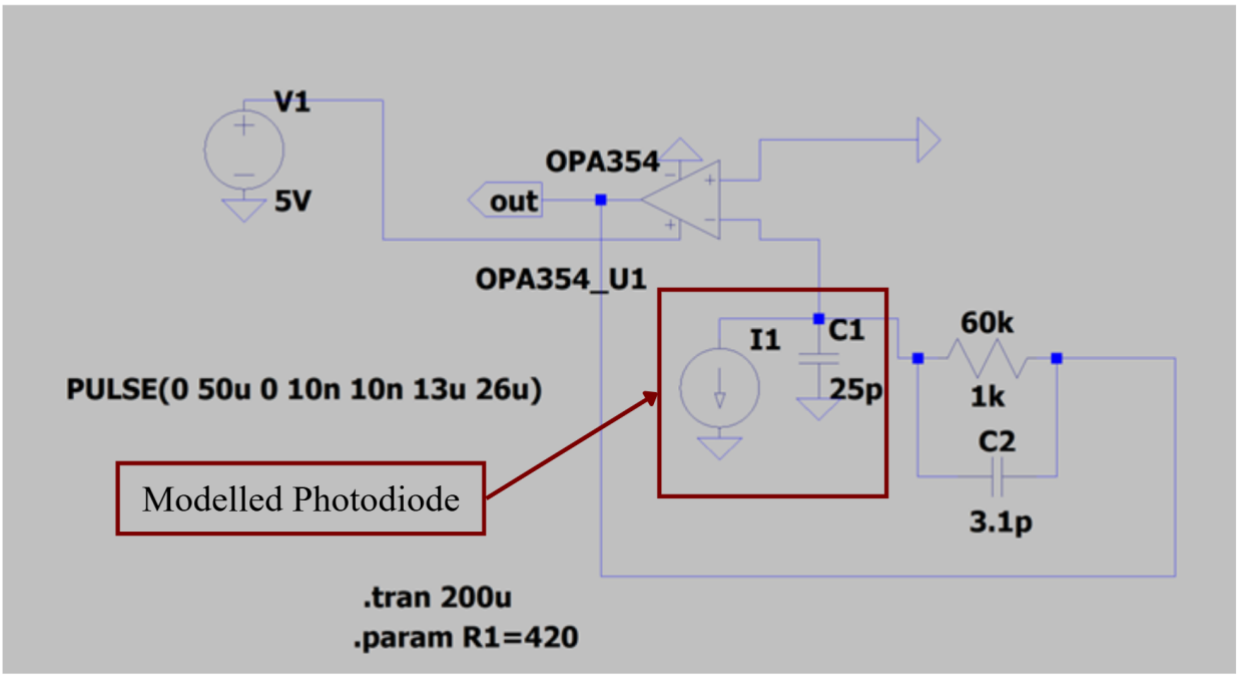


*Figure **19**: Initial receiver schematic*

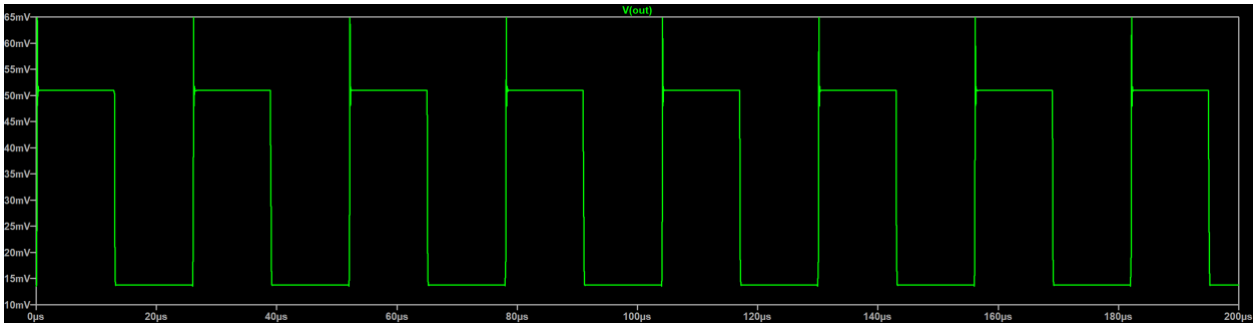


*Figure 20: Simulation Results for initial receiver design*

This initial TIA design successfully demonstrated proof-of-concept operation at 38.5 kHz (Figure **19**), a frequency typical for low-speed optical systems but insufficient for USB-rate signals. To meet the required data rate (PR-2), the modulation frequency was increased to

12 MHz. At this higher frequency, however, the TIA exhibited instability, as shown in Figure 20, characterised by sustained high-frequency oscillations at the output.

This behaviour is attributed to the combined effect of the op-amp's finite gain-bandwidth product and the photodiode's junction capacitance, which together create a high-frequency pole in the feedback loop. When driven at 12 MHz, the phase lag introduced by this pole approaches 180° while loop gain remains significant, resulting in ringing and oscillation. This phenomenon is common in high-speed TIAs.

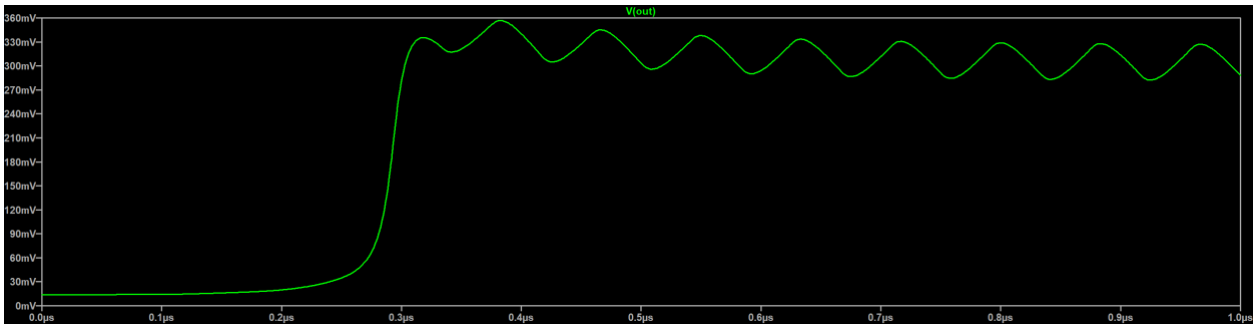


*Figure **21**: Simulation Result of the Initial Single-Stage TIA Design*

To resolve this, the gain was lowered and the capacitance increased as needed. After multiple iterations of the RC circuit values, a maximum stable output of 11 mV (Figure 22) was achieved using a 1 kΩ feedback resistor and 10 pF capacitor (Figure **21**: Simulation Result of the Initial Single-Stage TIA Design), but this was still insufficient for MCU detection for which the minimum 3 V. However, all attempts to increase the gain led to instability in the circuit.

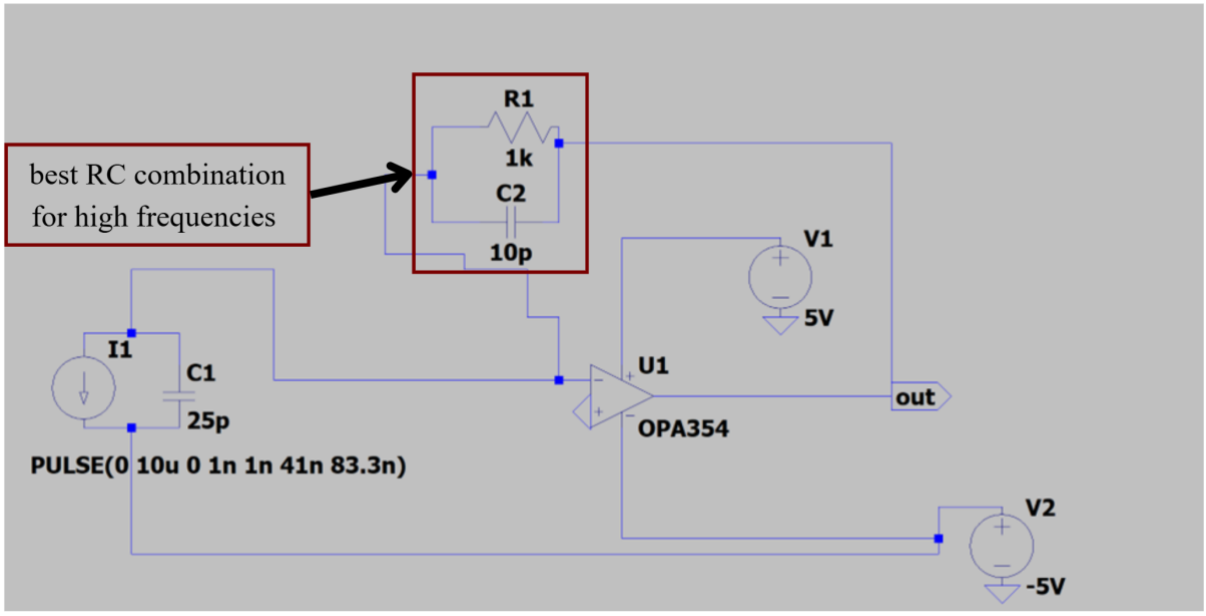


*Figure 22: Design 2 of Receiver Circuit with increased frequency*

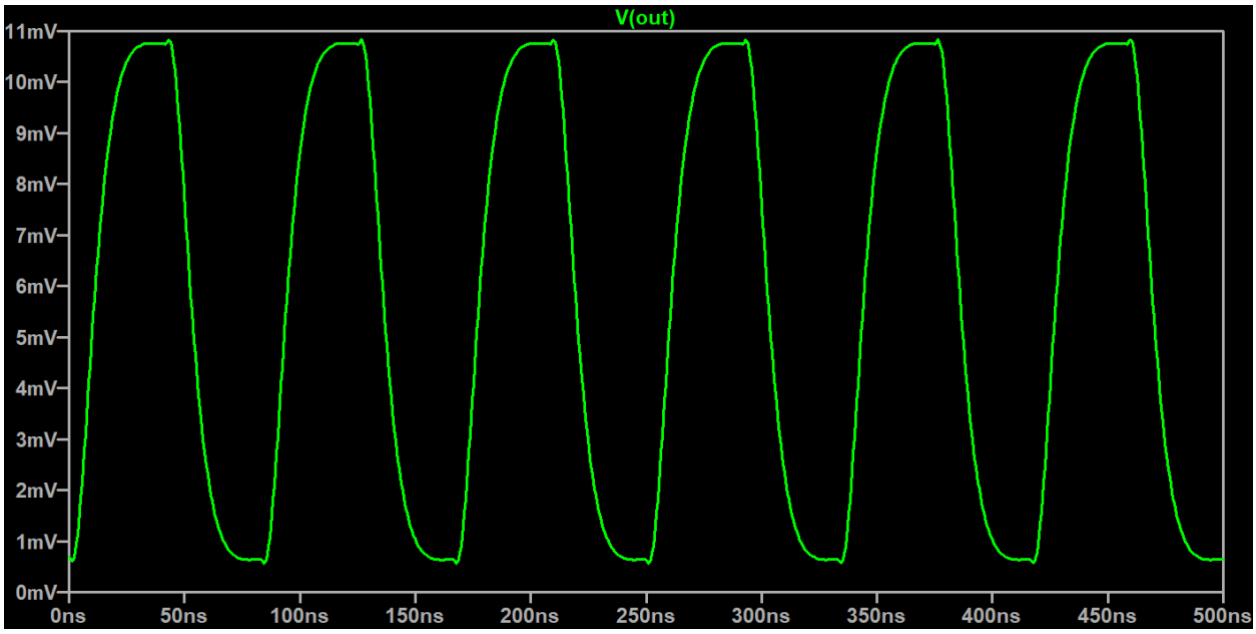


*Figure 23: Output Voltage of Design 2*

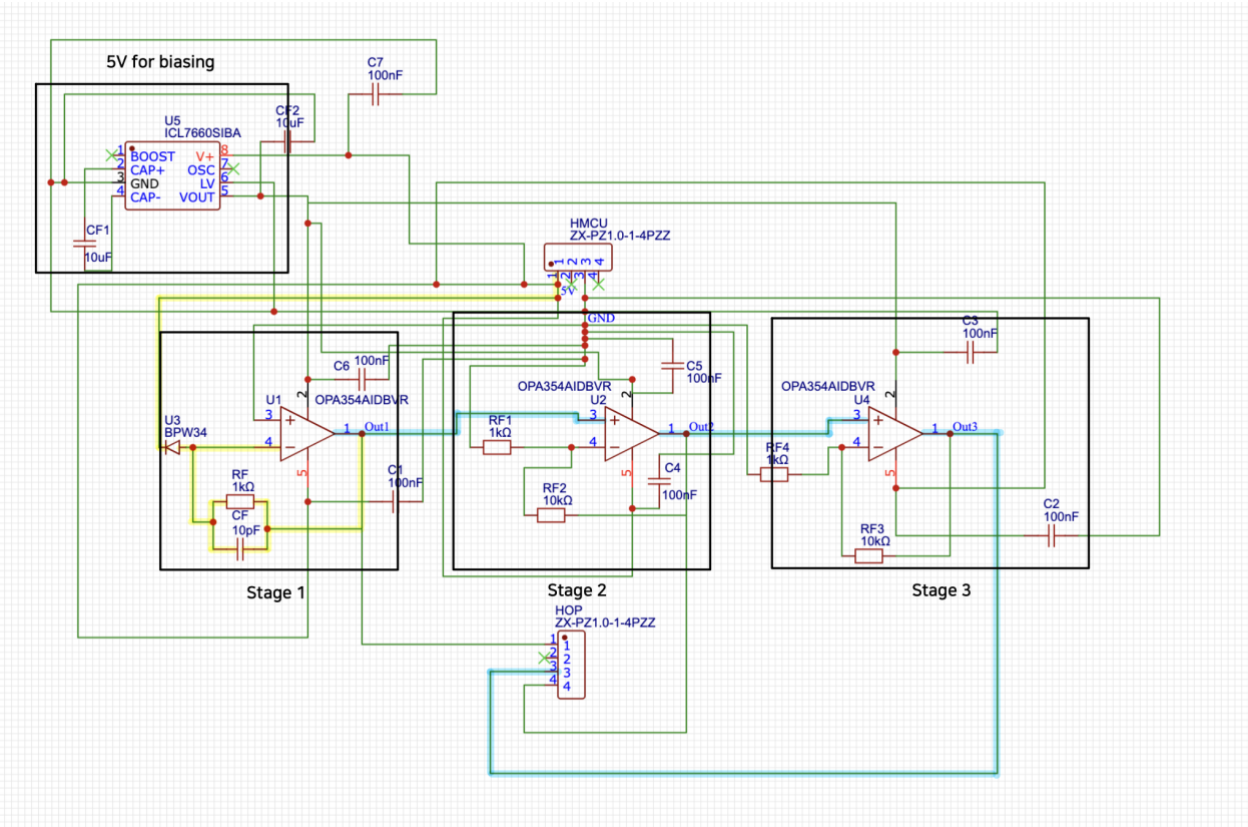


*Figure 24: Final receiver schematic*

I. Stage 1: High-Speed TIA

The TIA initial stage was designed for low gain, high bandwidth TIA. Its sole role is to perform stably convert the photocurrent to a voltage signal. The design prioritises speed over gain, using a low feedback resistor (1 kΩ) to maximise bandwidth and a small feedback capacitor (10 pF) for phase compensation to prevent oscillation.

II. Stage 2 & 3: Cascaded Voltage Amplifier Stages

Two subsequent OPA354 amplifiers provide voltage gains of approximately ×10 and ×6, respectively, amplifying the TIA output to the required 3.3 V logic level. Distributing the gain across multiple stages preserved bandwidth and avoided oscillation, ensuring compatibility with 12 Mbps data transmission.

This modular, multi-stage approach resulted in a reliable and stable receiver capable of meeting the project's performance targets.

#### 3.4.5.2 Key Component Selection and Justification

I. Photodiode (BPW34)

The photodiode is a critical component as it detects the incident laser light and converts it into a proportional photocurrent. The silicon PIN BPW34 was selected for its low junction capacitance (70 pF at 0V bias), which is essential for a fast response time. To further enhance speed, the photodiode is operated in reverse bias, which reduces its capacitance (25 pF at 3 V) and shortens the carrier transit time. This minimises input capacitance at the TIA input improving stability and bandwidth at high frequencies.

II. Operational Amplifier (OPA354)

The OPA354 offers a 100 MHz gain-bandwidth product and 150 V/µs slew rate, essential for high-speed amplification. Its rail-to-rail I/O and single-supply operation make it ideal for compact, low-power embedded systems [6].

III. Voltage Generator (ICL7660)

Provides a −5 V supply rail via charge-pump inversion from the +5 V input, enabling dual-supply operation for the OPA354 stages. This improves linearity and ensures symmetrical signal swing [7].

3.4.5.3 Testing and Validation

A series of tests were performed to confirm the working and evaluate performance of the receiver circuit.

Test T-002.3 (refer to Appendix C, 9.3.4), confirmed the ability of the FSO system to transmit structured character data over a 2-meter optical link using a custom UART protocol. The FSO system transmitter end the modulated laser pulses to which was encoded to UART frames by the transmitter side MCU, while the receiver decoded them using precise timing.

The system maintained a 9600 baud rate, and the demo message “Yuki!” was successfully received every 2 seconds. During instances of misalignment of the laser and the photoreceiver, the message “Framing Error” was displayed on the serial monitor.

Test T-005.2 (refer to Appendix C section 9.3.10) validated the transmission of structured messages at a high baud rate of 230400 bps using UART-style signalling. The transmitter sent the predefined message “Yuki” through FSO link as observed in Test T-002.3, and the receiver verified message integrity using a success and error counter.

During misalignment, the system displayed “ERROR!” messages on the serial monitor while aligned test cases reconstructed the message sent from the transmitter end, confirming sensitivity to optical path stability. The counter included as part of the code ensured that the number of successful receptions and errors were logged on the serial monitor since physical observation at a high baud rate is unreliable.

#### 3.4.5.3 PCB Design and Implementation

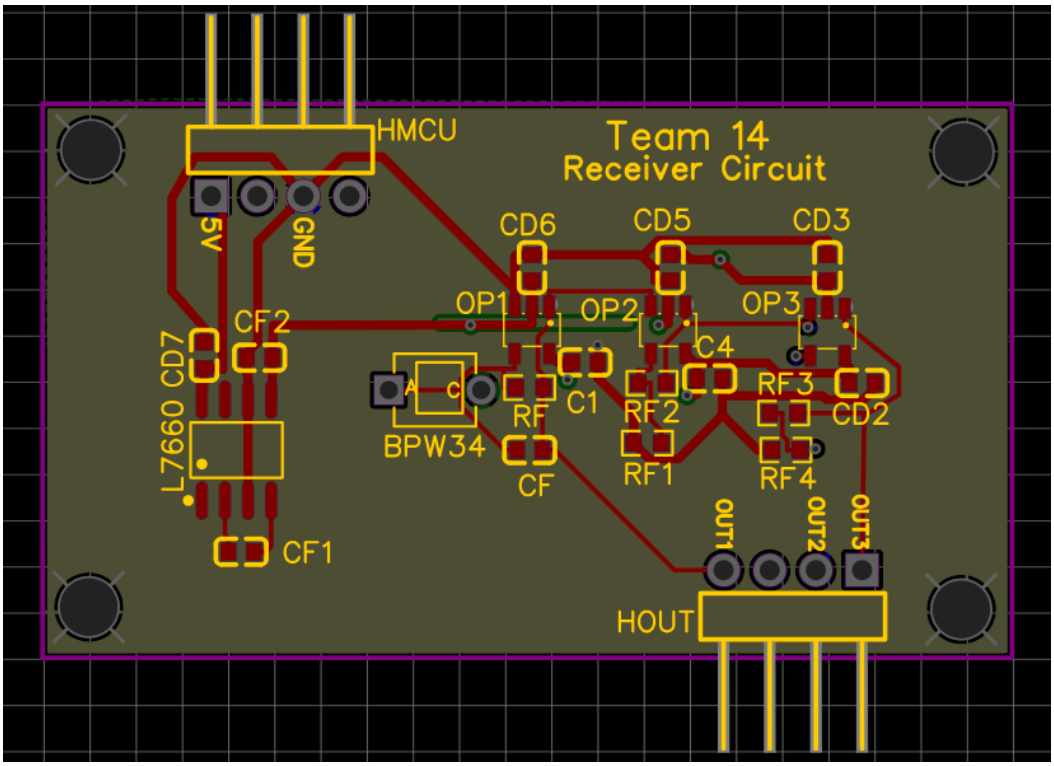


*Figure **25**: Receiver PCB design - with visible ground plane*

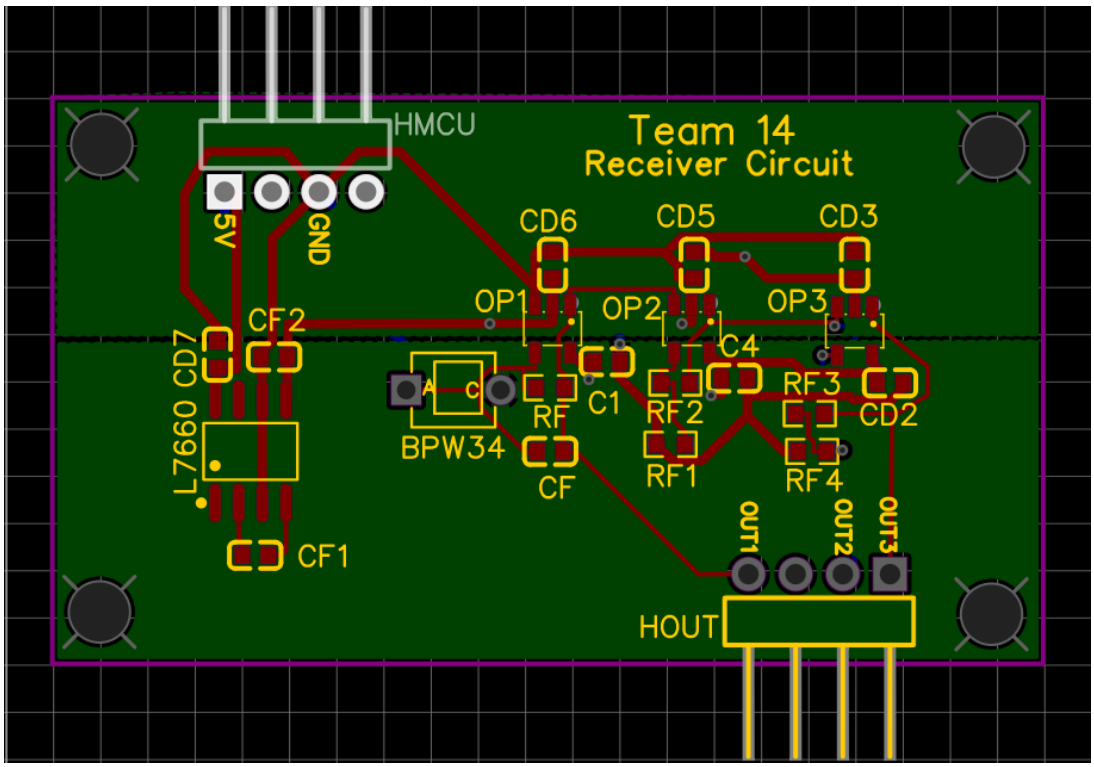


*Figure **26**: Receiver Circuit PCB -with visible divided power plane*

The final receiver PCB (53.3 mm × 30.5 mm, 1.6 mm FR-4) employs a four-layer layout to accommodate the three-stage topology and ensure clean power distribution. Separate ground

and power planes were implemented to minimise crosstalk and electromagnetic interference. The power plane was divided into +5 V and −5 V regions to support the OPA354's dual-supply configuration.

Header pins were included for MCU interfacing and test-point access from each amplifier stage. Component placement isolated high-current power circuitry from the analogue amplifier network, reducing noise coupling.

*Table 5: Requirement compliance*

| Requirement ID | Description | Compliance Method |
| --- | --- | --- |
| FR-02 | Implement receiver for modulated light for bidirectional communication | Achieved using BPW34 photodiode and OPA354-based TIA circuit |
| FR-02 | Output logic-level signal for bidirectional communication | Verified in Test T-002.1, where MCU successfully detected the receiver output |

### *3.4.6 Chassis*

The purpose of the design project's chassis was to protect all electrical components by providing stable and rigid mounting onto the surface of the chassis (PHY-4), and by ensuring all electrical components were stored in an enclosed environment (PHY-2).

Based on the finalised list of the design project's physical requirements, the chassis would also need achieve an IP rating of at least IP 51, which ensured that minimal amount of dust would be able to enter in inside of the chassis, and ensured that vertical rainfall would not damage internal electronics (PHY-1). Additionally, external ports, where power, USB peripherals and a USB data stick could be connected needed to be labelled (PHY-5), and visual status indicators needed to be implemented to clearly identify is power was being supplied to the internal electronic components, if a link was achieved from the transmitter and receiver circuits, and if data activity was recognised (PHY-6).

While none of the physical requirements for the chassis are within the top 20 highlighted, the chassis of the FSOCS would guarantee that the final designed product could highlight the quality of the team's design process. The chassis would not as well ensure that the build looked complete aesthetically but would allow the full functionality of the final designed product to be completely assembled and demonstrated to the relevant stakeholders of the design project. Furthermore, a completed chassis would be commensurate with the design team's stakeholders' expectations regarding the design outputs based on the design project brief.

#### 3.4.6.1 Concept Sketches and Engineering Drawings

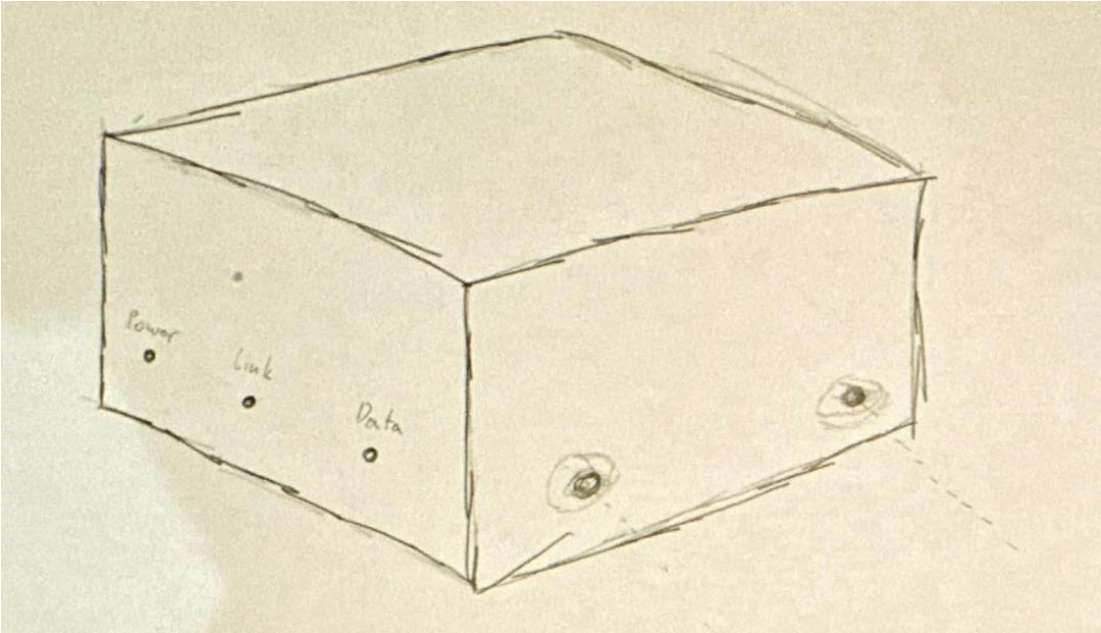


*Figure **27**: Initial Concept Sketch of the Chassis*

Initial concept sketches and engineering drawings were completed on paper after the physical requirements of the chassis were finalised. As shown in the figure above, the initial rough sketch detailed the location of the receiver and transmitter components and provided an idea of where visual status indicators could be placed. The orthogonal view of the concept shows that the chassis was shaped as a box, which would allow the chassis to sit comfortably on a table.

Initial discussions regarding the chassis amongst the design project team highlighted concerns regarding the construction and assembly of all sides of the chassis if it was assembled as a box. To ensure that the box was easily assembled while allowing electrical components to be easily accessible, the chassis would be composed of multiple flat sides, which then could relate to nuts and bolts. Initial drawings of the sides of the chassis can be seen in the figure below.

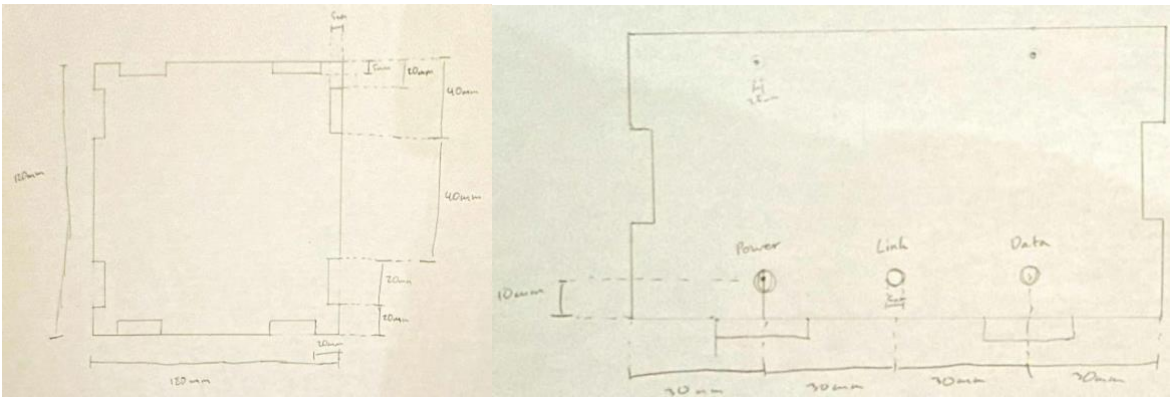


*Figure **28**: Initial Engineering Drawings of the Chassis*

### 3.4.6.2 Construction Methods

Alongside initial discussions and sketches of the chassis, two construction methods were also considered.

The first construction method considered was the use of MDF through laser cutting. This would allow the chassis to be quickly constructed considering that the initial sketches of the chassis depicted it being shaped as a box, made of multiple flat sides.

The second construction method was the use of PLA filament and 3D-printing. While the construction method was slower than laser cutting, the method would allow the designed chassis to include complex shapes if needed and was more easily accessible compared to the laser cutting equipment.

Both MDF and PLA are nonelectrically and thermally conductive materials and are recyclable. Furthermore, both a laser cutter and a 3D-printer were accessible through UWA laboratories, however, while 3D-printers only required basic induction and training, the laser cutter was only accessible through high-risk area training.

Access to PLA filament for 3D-printing was more convenient compared to MDF as the Makers laboratory at UWA provided the filament and would charge $2 per hour for the use of the 3D-printer and filament, while MDF needed to be purchased through external vendors. Additionally, choosing to use the laser cutter was considered a risk compared to the 3D-printers. This was because the laboratories provided only one laser cutter at one of UWA's laboratories.

Finally, while technical queries with the design project clients revealed that the designed solution would be used in indoor lab environment, the physical requirements outline by the design team raised concerns about wood expansion from rain exposure, which would prevent the chassis from achieving an IP51 rating.

After taking into consideration the different advantages and concerns with both construction methods, it was decided by the design project team that the chassis should be completely constructed using PLA filament and 3D-printing.

#### 3.4.6.3 CAD Firmware

Throughout the creation of the chassis, two different CAD software were used. While both CAD software was made by Autodesk, one was web-based program used to introduce users to 3D design, while the other was more advanced and allowed for complex designs to be made more conveniently.

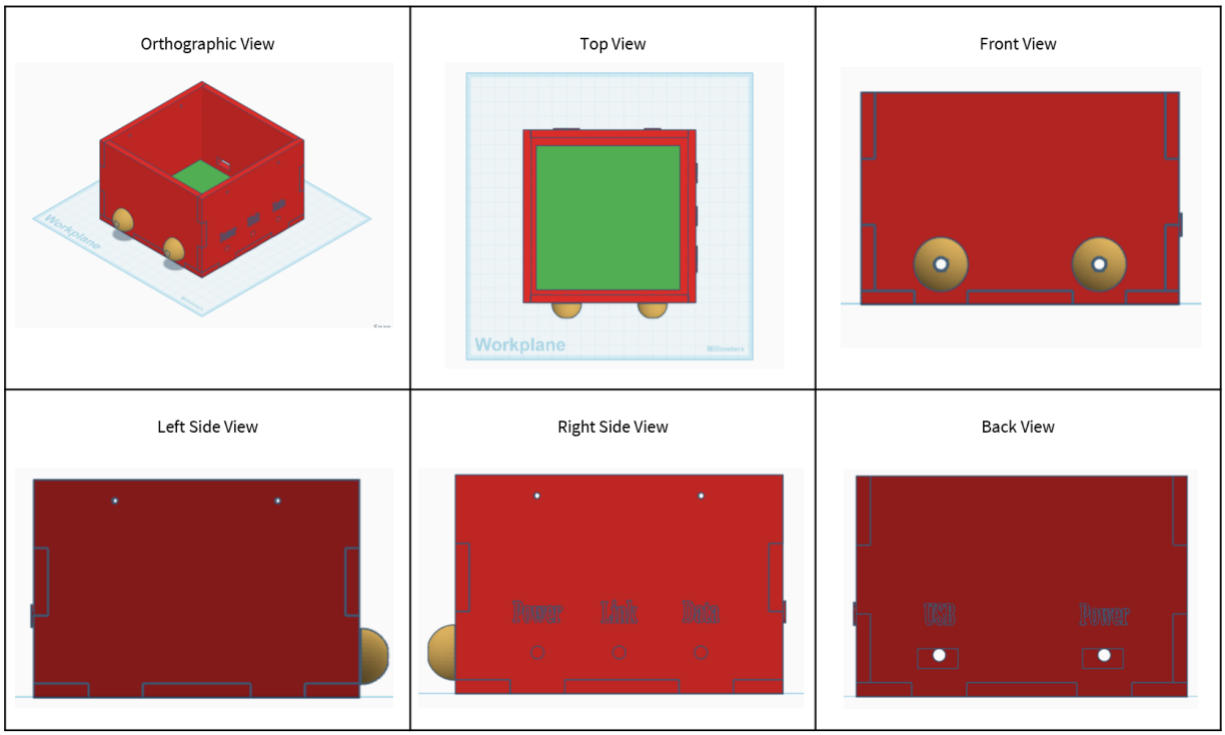


*Figure **29**: First Version of the Chassis using TinkerCAD*

The first CAD software used to design the preliminary design was TinkerCAD, a web-based platform which is commonly used by beginners for home-based projects. As shown in the figure above, while TinkerCAD allowed us to design the chassis using basic drag-and-drop shapes, it was harder to create more complex shapes unless it was made from multiple basic shapes. Furthermore, TinkerCAD had no engineering sketching functions, meaning all the first version of the chassis was made without formal measurements and constraints.

Due to the downside of using TinkerCAD, a second CAD software, Fusion, was used for all remaining designs of the chassis.

While some training through tutorials, videos and referring to FAQ pages was needed to understand the functionalities of Fusion, the software both had the same benefits as TinkerCAD, and had additional features, which allowed designing the chassis to be more efficient and effective.

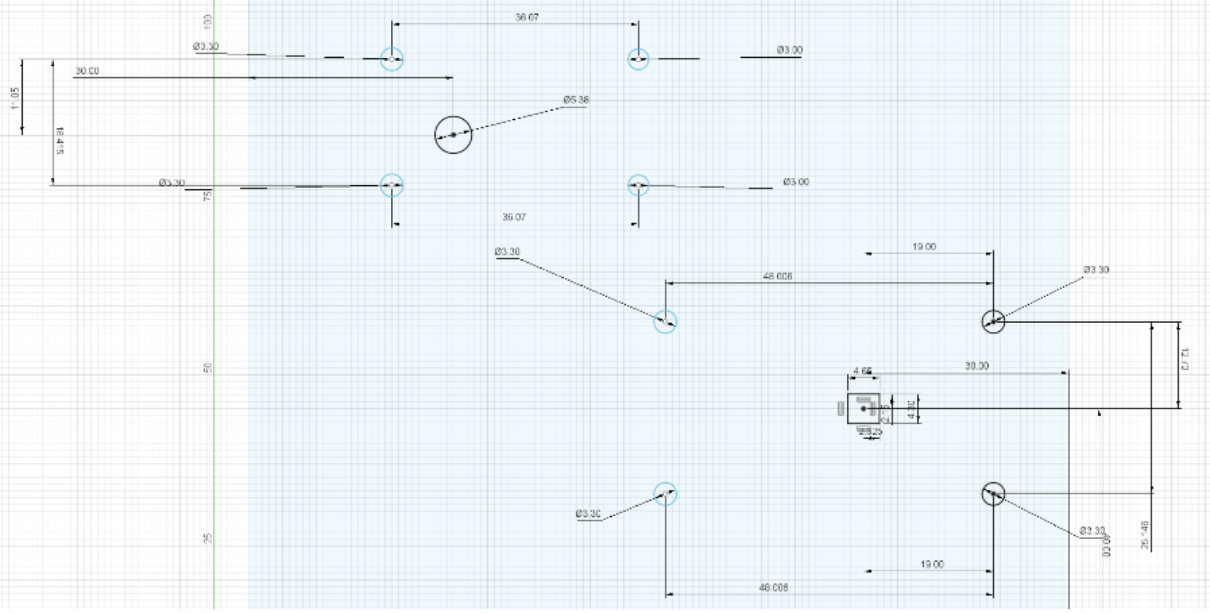


*Figure **30**: Engineering Sketches of the Second Version of the Chassis on Fusion*

Fusion's sketching functions allowed all parts of the chassis to be measured and constraint, allowing for PCBs to be easily mounted onto the chassis as shown in the figure above. Additionally, Fusion allowed PCB designs to be integrated into the software by letting emulations of the PCB to be imported into the design. This means PCBs can be seen on the chassis before being printed.

Fusion would also allow other users, when shared the designs, to open, view and download designs created by other users. This would make exporting the chassis design into a .stl file to be significantly easier than downloading designs on TinkerCAD, which made progress tracking and file sharing more convenient for the design project team.

#### 3.4.6.4 Final Version of the Chassis

As shown in the figure below, the final version of the chassis was developed on Fusion and can meet almost every physical requirement. The PCBs were emulated into the software to represent an accurate depiction of the chassis when printed for the final designed product.

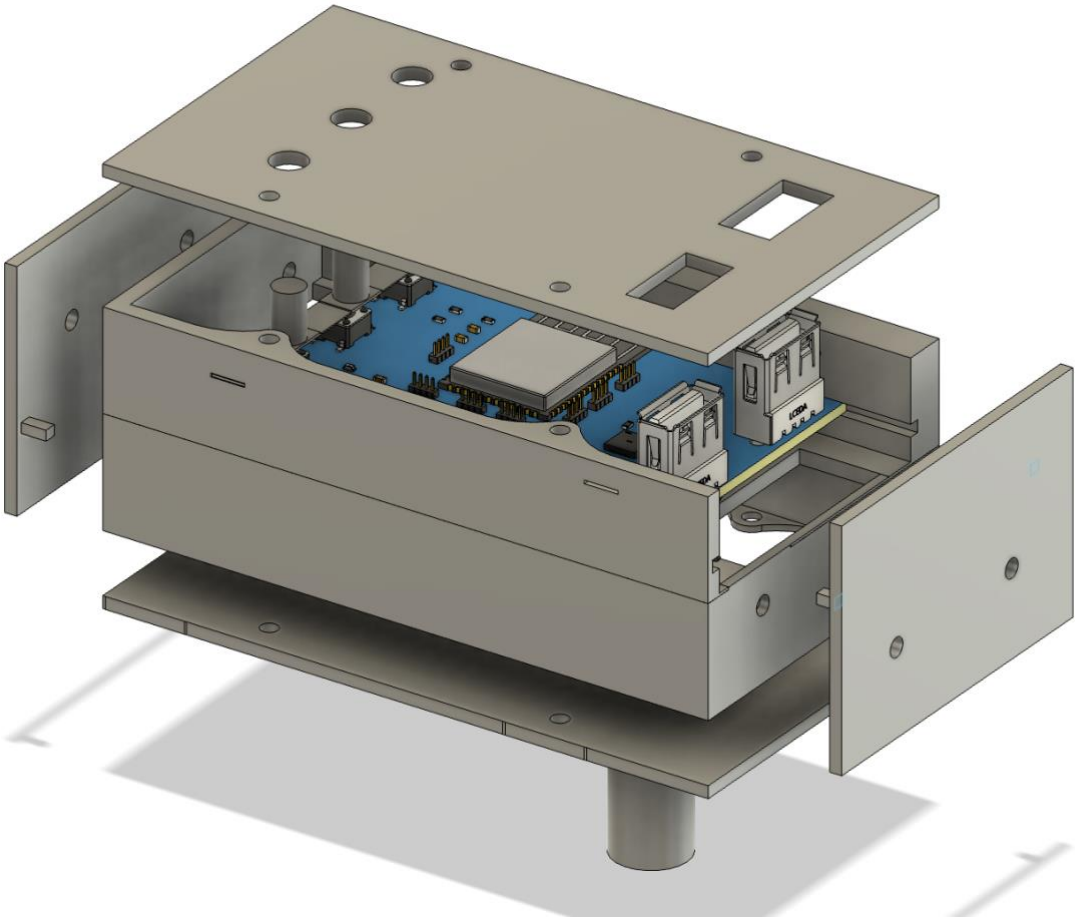

*Figure 31: Final Chassis design*

The chassis is made of PLA filament and used nuts and bolts to secure the sides, meaning the chassis is constructed from non-conductive material (PHY-3) fully encloses all internal electronic components (PHY-2). The chassis provides stable, rigid mounting for all optical components as the laser diode can be secured through a hold in the bottom piece, and the receiver is mounted on the inside of the chassis (PHY-4). Furthermore, the external ports on the chassis are labelled to clarify the purpose of the two USB ports on each module (PHY-5).

While the chassis fulfills most physical requirements, two are not met. First, the chassis does not meet an IP rating of IP51 (PHY-1), as the USB ports are secured on the top of the chassis,

meaning the USB port, and the rest of the MCU PCB, is vulnerable to vertical rainfall. Second, the chassis does not provide visual status indicators for power, link status and data activity (PHY-6). While visual indicators are mounted on the MCU PCB, it is not visible from the outside of the chassis when the sides are secured.

### *3.4.7 Firmware*

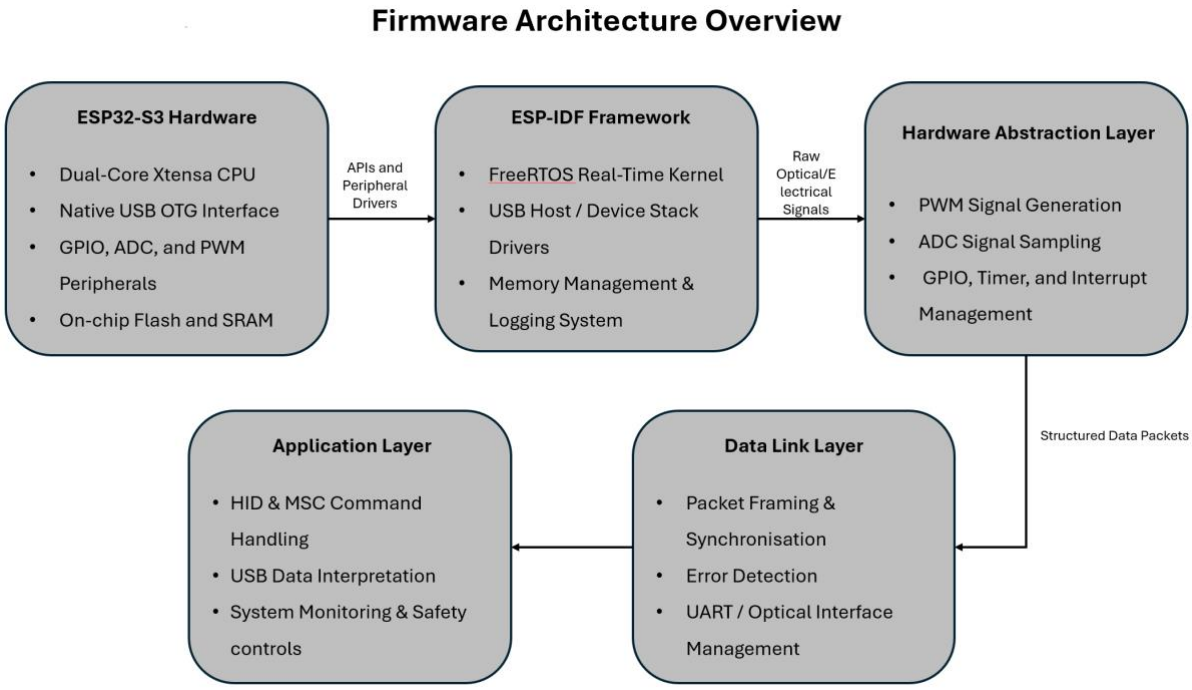


*Figure 32: Firmware architecture overview*

The firmware was structured in modular layers, separating hardware control, USB protocol handling, and optical communication logic. The HAL manages low-level GPIO, PWM, and ADC control for the laser driver and receiver photodiode, ensuring precise timing and consistent signal generation.

Next, the USB Host Layer uses ESP-IDF's built-in HID and MSC USB Host libraries to emulate a host and interface with USB devices. This layer handles command-response protocols, device enumeration, and error handling. There is also a data link layer that encodes and decodes data packets for transmission over the FSO link. It also implements error checking and synchronisation, ensuring data integrity.

Finally, the application layer implements peripheral-specific behaviours, such as HID input aggregation or MSC read/write command handling, integrating seamlessly with USB Host and optical layers.

By utilizing/leveraging ESP-IDF's FreeRTOS environment, tasks such as USB host polling, PWM modulation, and optical data capture run concurrently with deterministic timing, critical for maintaining reliable high-speed communication.

#### 3.4.7.1 Development and Validation Process

I. Library Verification

Before any custom development/coding, the foundational capabilities of the ESP32-S3 were validated using the official ESP-IDF examples for USB Host emulation of HID (Human interface devices) and MSC (Mass Storage Devices) peripherals. These examples such as [maybe mention specific examples here/or put ss of code excerpt here] were compiled and assessed on a ESP32-S3 board to ensure the USB Host and device stack functionality. This initial prototype/code confirmed the operation and capabilities of ESP32-S3's USB Hosting.

II. Wired Protocol Testing

To develop and debug the USB communication protocol without the complexities of optical hardware, a wired connection was employed. Two ESP32-S3 boards were connected via UART, with one configured as the USB Host and the other as the peripheral emulator. This UART connections between ESP32-S3 boards allowed early debugging of data-link logic before introducing optical hardware, reducing integration risk

III. FSO Integration

The final layer involves replacing the wired UART link with the custom FSO transmitter and receiver prototypes. This was done incrementally. Firstly, the transmitter and receiver code was used to verify that a simple 'HIGH' or 'LOW' signal could be reliably detected over the optical link. Next, a data link test was conducted with data packets being transmitted and received confirming the integrity of the data over the optical link. Finally, a full system test was conducted with the complete USB Host and peripheral emulation firmware was integrated with the FSO hardware, and the system was successfully tested, demonstrating end-to-end functionality for both HID (mouse/keyboard) and MSC (USB stick) peripherals over the optical link.

This staged integration allowed for system testing and validation, allowing for the identification and resolution of issues at each layer before progressing to the next. It also confirmed that the system met the specified functional and safety requirements.

ESP-IDF's for USB, PWM, GPIO, and FreeRTOS task scheduling directly maps to all functional requirements:

*Table 6: Functional Requirements to ESP Features*

| Functional Requirement | ESP32-S3 / ESP-IDF Feature |
|---|---|
| HID communication | USB Host stack with HID class support |
| MSC communication | USB MSC Host stack, file system support |
| High-speed PWM | Resolute timers and PWM peripherals |
| Real-time task handling | FreeRTOS-based task scheduling |
| System monitoring | GPIO and interrupt-driven status signals |

The firmware was structured with clear modular boundaries to simplify debugging and future scalability. Each layer, from the ESP-IDF core to the application logic, operates independently, allowing updates or replacements (e.g., swapping the UART link for optical, or adding Wi-Fi telemetry) without disrupting lower layers. This modularity aligns with industry best practices for embedded systems design, ensuring long-term maintainability and adaptability for future FSO system enhancements.

## 3.5 Process Assembly/Construction

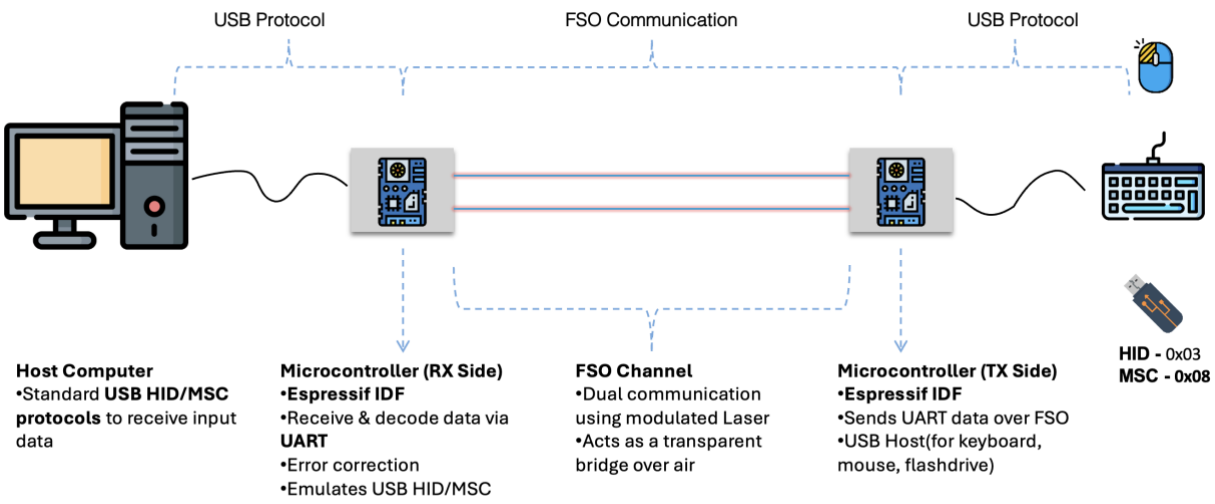


*Figure 33: FSO Communication System Architecture*

The FSO Communication System was assembled using a modular workflow, dividing the system into three independent PCBs: the MCU, transmitter, and receiver modules. This approach enabled isolated testing of each module before full system integration, reducing integration risk and facilitating iterative development.

### *3.5.1 PCB Fabrication and Component Assembly*

The PCB fabrication process began with schematic design and PCB layout in EasyEDA. A single, controlled Bill of Materials (BOM) was maintained to track components. Critical parts, including the OPV300 VCSEL and OPA354 op-amps, were sourced from reputable suppliers (DigiKey), with all datasheets archived in the project repository.

All PCBs were fabricated by JLCPCB using standard FR-4 material with a thickness of 1.6 mm. The transmitter PCB has a two-layer stack-up, while the receiver PCB, due to its three-stage amplifier topology, was fabricated as a four-layer PCB with separate ground and power planes for noise isolation.

Components were partially machine-assembled by JLCPCB, with critical elements, including the OPA354 op-amps, OPV300 VCSEL, MOSFETs, and potentiometer, manually soldered by the team to ensure correct orientation and prevent thermal damage. Standard soldering tools were used, including a controlled hot-air flow station for SMD components and soldering irons for through-hole parts. Flux was applied as needed to reduce bridging, particularly for fine-pitch ICs. All solder joints were inspected visually and electrically verified using a multimeter to ensure continuity.

Headers were installed to provide modular connectivity between the MCU and the transceiver modules, allowing each module to be individually tested or replaced without affecting the overall system.

One enclosure including all the modules were designed in Autodesk Fusion 360 and fabricated using PLA filament on a Bamboo Carbon X1 3D-printer. PLA was selected for its non-conductive properties, rigidity, and opacity, which minimises external light interference. The chassis design incorporated high-tolerance mounts to secure PCBs and optical components, ensuring repeatable alignment and structural stability.

### *3.5.2 Firmware*

The firmware for the FSO communication system was developed for the ESP32-S3 using ESP-IDF library, providing low-level access to GPIO, PWM, ADC, and USB peripherals.

Development began by establishing basic UART communication between two ESP32-S3 development boards with a wired connection between UART RX, TX. This step verified the core data-link logic and allowed debugging of timing, synchronization, and error handling in a simpler wired environment before introducing the optical channel.

The final firmware supports two operational modes to accommodate different USB device types: Firstly, unidirectional HID communication designed for devices such as keyboards and

mice, where data mainly flows from the peripheral to the host. Secondly, the bidirectional MSC communication, which is designed for USB flash drives, requires a full command-response protocol to reliably perform file read and write operations.

This structured approach allowed incremental testing and ensured reliable operation over both wired and optical links.

### *3.5.3 Issues Identified and Resolutions*

During the assembly and integration of the FSO communication system, several challenges were encountered that required iterative design refinement. For the MCU PCB**,** initial inspection revealed power and data delivery issues, as documented in Test Report T001.2. A polarity error in an electrolytic capacitor was corrected to resolve the power issue, while communication problems with standard USB cables were addressed by designing a custom USB-A to USB-A cable, enabling proper two-way data transfer.

Additionally, minor adjustments were made to the header pin connections for the WROOM1 module, ensuring reliable power and ground delivery to the transmitter and receiver circuits.
On the transmitter PCB, a persistent issue was observed where the laser did not fully turn off during the low PWM cycle. Investigation revealed a reversed polarity SMD diode in the driver circuit, which was corrected by reorienting the diode. This adjustment ensured proper modulation and stable operation of the laser source.

For the receiver PCB, negative voltage outputs were initially produced, which the MCU could not interpret. This was mitigated by implementing another amplifier stage but this time an inverting one, ensuring that the received signal remained within the MCU's input voltage range. Furthermore, the optical alignment process was challenging due to the invisible 850 nm laser beam, which made tracking difficult even with an IR-sensitive camera. The team replaced the source with a visible 650 nm red laser diode for alignment purposes, adjusting the current clamp to maintain compliance with Class 1M laser safety standards.

During integration of HID and MSC firmware, identification conflicts arose when emulating devices, as the ESP32-S3 misclassified device types during initial tests. The issue was traced to older ESP-IDF firmware, and the correct device order and updated library resolved the conflict, enabling reliable HID and MSC operation over the optical link.

Another issue arose when connecting a mouse to the UART USB-A port, as the MCU failed to detect the correct voltage threshold from the device. Investigation revealed that diode D3 was restricting current flow in towards the device connected, preventing proper device powering up. The issue was resolved by removing D3 from the circuit and restore a direct connection, which restored the power path and allowed the devices to function correctly.

Lastly, a low data transfer rate was observed during early testing, which was addressed through a combination of optimised PWM timing, reduced parasitic, and incremental firmware refinement. Baud-rate sweeps across multiple orders identified the best of the BER–throughput curve, and the operating point was set accordingly. In parallel, the transfer data structure was simplified from a complex, nested format to fixed-length frames with minimal headers, cutting per-packet overhead and parser load.

Through iterative testing and careful resolution of these issues, the FSO communication system achieved reliable functionality, with all modules successfully integrated and validated for end-to-end operation, meeting the project's functional and safety requirements.

### 3.6 System Integration

This section describes how the FSOCS hardware, firmware and mechanical subsystems were integrated into a single, operational two-way Free Space Optical Communication System. It presents the staged integration strategy, the critical interfaces and dependencies, acceptance evidence, and residual technical risks.

Integration activities were organised such to minimise confounding faults, produce reproductible artefacts and trace verification of prioritised requirements (notably FR-1/2/2/3/4/7/10, PR-1/2/3/5/6, PWR-1/2/3, SR-1).

Integration followed four controlled stages including component level simulations, bench prototype where breadboarded TX/RX and MCU functions verified basic modulation, detection and timing prior to PCB layout. Then the populated TX, RX and MCU PCBs were powered and smoke tested; pin level logic thresholds, regulator outputs and TIA bias were verified points.

The system integration terminates in the assembled PLA chassis and tested end to end (HID and MSC operation, latency, throughput, link-loss recovery) with each stage producing test protocols, measurement logs and firmware identifiers to maintain traceability between test evidence and the requirements list.

Successful integration of the system modules depends on a small set of critical electrical and mechanical interfaces. Electrically, the MCU modules provides the primary control and timing signals to the TX and receives the conditioned detector output. Mechanically, the PLA chassis and lens mounts define the optical baseline and repeatable alignment.

Important electrical interfaces for consideration are the 5V VBUS and ground header, and the receiver demodulated output routed into an interrupt-capable MCU pin (GPIO9). These three

signals alongside local regulators such as 3.3V for logic and - 5V for the analogue front end, form the minimum interface set required for transparent USB operation and safety.

### *3.6.1 Hardware Integration*

The hardware integration task bound the MCU board to the custom transmitter and receiver PCBs while preserving signal integrity and Class 1M safety pathways. The TX path couples an MCU GPIO configured for high-speed push-pull to the MOSFET gate through a series gate resistor, with a unidirectional diode in the op-amp path to ensure clean turn-off. The RX path delivers a rail-to-rail logic output from the final gain/slicer stage into an interrupt-capable MCU input, maintaining VIH/VIL margins under worst-case supply tolerance.

Power rails (VBUS 5 V, local 3.3 V, and -5 V for the analogue front-end) share the same ground plane. Noise containment is achieved via: (i) short return loops under each high-speed signal so the displacement current returns directly beneath the trace; (ii) localised LC filtering on the −5 V inverter output to prevent charge-pump ripple from entering the TIA passband; (iii) series ferrites on noisy digital supplies feeding into mixed-signal areas; and (iv) dense stitching-via fences around the TIA/gain cluster to keep return paths compact. This approach preserves BER robustness under ambient light without the drawbacks of split-plane impedance discontinuities (PR-1/PR-6).

#### 3.6.1.1 Wiring and connections

The MCU schematic allowed for pin header to be used to connect the receiver and transmitter circuit, as well as several IO pins were made available to account for the signal input and output to the WROOM1 module. One circuit limitation includes that only one pin header was made available for 5V power and Ground. Thus, a set of custom wires 1:3 have been used to split the one header into 3 possible connections.

The transmitter and receiver (GND) connections were routed from the MCU's solitary 5 V and GND header to the receiver and transmitter circuits, respectively, by the custom 1-to-3 splitter cable. By so doing, all the subsystems had a common reference potential and a stable 5 V supply from the MCU board. The transmitter circuit applied the 5 V line to the laser diode through its current-limiting stage, while the receiver circuit powered the amplifier of the photodiode and signal-conditioning elements. The common ground connection preserved signal integrity and reduced noise coupling among the modules, providing reliable function and consistent communication over the optical connection.

Two signal wires went to the MCU headers on GPIO9 and GPIO18. The GPIO9 wire went to the Receiver Output 4 of the Photodiode circuit, delivering the receiver's demodulated signal to the MCU for digital processing. The GPIO18 wire went to the laser driver's PWM input, so the MCU could provide modulated data signals for the laser output. These, in combination,

provided bidirectional communication, where the received optical data was at GPIO9 and the laser modulation was at GPIO18 for the output of the data.

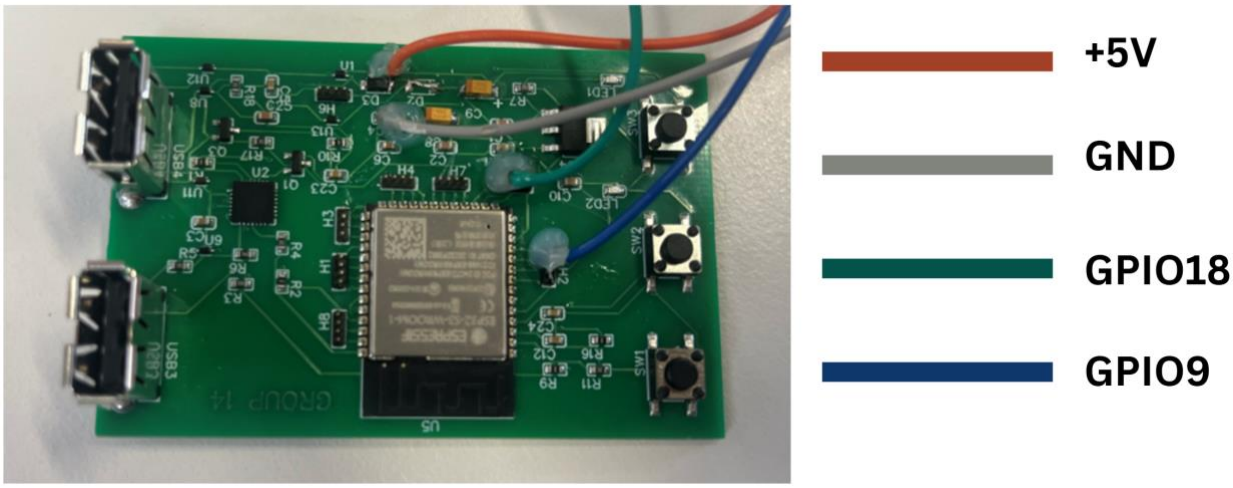


*Figure 34: MCU circuit*

Following Test T004.2 describe section 3.4, a custom two-way USB-A to USB-A cable was fabricated to facilitate bidirectional communication between the host and peripheral modules. The data cable enabled USB communication between the ESP32-WROOM1 module and the host PC, allowing for firmware flashing, serial monitoring, and bidirectional data exchange. All wiring connections were mechanically reinforced using hot glue, as shown in figure above, to secure the terminations on the MCU PCB. A non-insulating adhesive was selected to prevent strain on solder joints and ensure long-term connection stability during handling and testing.

#### 3.6.1.2 Chassis and physical circuits Integration

The chassis design of the FSOCS was guided by the principles of precision, durability, and modularity. Its primary purpose is to maintain accurate optical alignment between the transmitter and receiver while providing mechanical protection and ease of assembly.
The structure's rigidity, accuracy, and ease of fabrication led to its 3D printing in PLA+. System stability is increased, optical path deviation is decreased, and assembly complexity is minimised thanks to the compact design. Effective prototyping and testing are supported by the chassis' complete accessibility for power, USB, and optical interfaces despite its compact size.

The enclosed form also protects against dust, vibration, and mechanical stress while guaranteeing laser safety compliance (Class 1M). In a compact form factor, the outcome is a lightweight, robust, and precisely engineered chassis that embodies the project's performance, safety, and practicality principles.

#### 3.6.1.3 Power Integrity

As shown in Figure below, the system uses two independent USB-A sources, the host-side unit is powered from a portable power bank over USB-A VBUS, while the emulation-side unit is powered directly from the PC's USB-A port. There is no electrical interconnect between the two supplies across the optical span, each unit maintains its own single, continuous ground plane. Within each unit, VBUS (red in the Figure 35) is locally regulated to 3.3 V for the MCU and logic and to -5 V (charge-pump inverter) only within the receiver analogue cluster. All returns (black in the Figure 35) reference the same uninterrupted ground connection to provide the shortest possible return for displacement currents, avoiding the impedance and EMI penalties of split grounds. Within the circuits, the power lines are isolated as much as possible or completely moved to separate layers to maintain the power integrity considering the theoretical speed which we are planning to achieve.

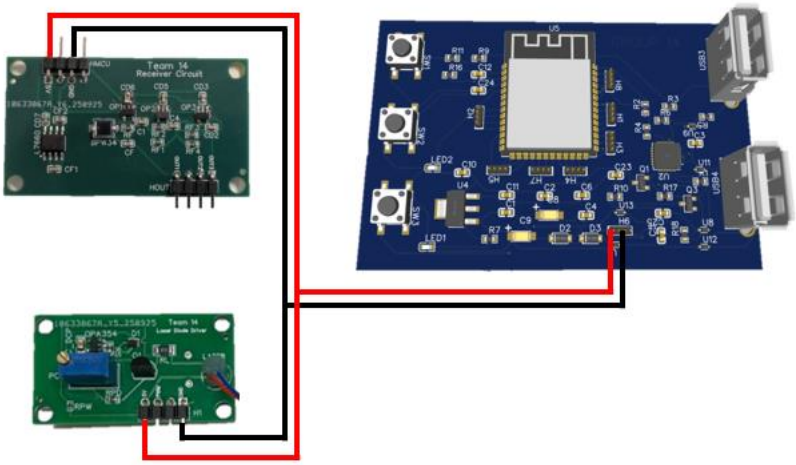

*Figure 35: Power connectivity over the separate circuits*

The PC-powered emulation side observes the default USB 2.0 current allocation. The load profile (MCU, FSO RX/TX circuits) is kept within the port's budget with headroom. The power-bank-powered host side accommodates higher transient demand and decouples the optical link from PC rail noise, however, power-bank auto-sleep at very light loads is common, so a keep-alive load (periodic MCU activity) is maintained to prevent unintended shut-off.

Test T004.3 Power Endurance Test, (refer to Appendix C section 9.3.8) was conducted to show that the FSO system could run smoothly for two hours using a portable power bank on one end. Throughout the session, HID functionality was left running and stayed stable the entire time. There were no resets or power issues. The result confirms that the system is meets the endurance requirement under PWR-3.

### *3.6.2 Firmware Integration*

This subsection describes the data path, framing and timing disciplines that make the optical link USB-transparent for HID and MSC. Safety interlocks and watchdogs ensure fail-safe behaviour on fault or loss-of-light. The firmware manages all the communication in a way the maximum possible speed is achieved while making sure the requirements were achieved listed in section 3.1.

#### 3.6.2.1 Stack Overview

The firmware is split across two peers to make the free-space hop USB-transparent; the Hosting unit runs a USB Host stack for the real peripheral (HID/MSC), packages traffic into framed link messages and schedules half-duplex transmission via an FSO. The Emulation unit enumerates as a composite USB Device, reverses framing and presents standard HID/MSC endpoints to the PC. A shared link layer provides CRC integrity with selective retransmit and sequence control for relink safety, while a laser-safe FSM and watchdog handlers ensure the laser is only enabled in a verified ACTIVE state and is immediately de-asserted on any integrity or timing fault.

#### 3.6.2.2 Hosting

The Hosting unit operates strictly one peripheral at a time (FR-3) either a HID device (keyboard/mouse) or an MSC device (USB flash drive). On attach, the host stack enumerates the device, inspects class/interface descriptors, and locks the firmware into a mode HID *or* MSC until the device is detached. This mutual-exclusion model reduces firmware complexity and jitter, only one class driver, one endpoint set, and one link framing profile are active at any instant, and all buffers/ARQ budget are dedicated to that class.

In HID mode, the host arms the interrupt-IN endpoint, timestamps each report at arrival, and hands it to the link layer to serialize into {preamble | len | seq | payload | CRC-16} frames. The guarded TDD scheduler transmits these frames in the next uplink slot with no competing MSC traffic, HID reports traverse in order with bounded latency to satisfy PR-3. In MSC mode, the host runs Bulk-Only Transport for the flash drive and tunnels each phase as CRC-32–protected link frames with sequence and selective retransmit. Because HID is not present in this mode, the TDD scheduler allocates contiguous slots to storage bursts within the ARQ window, improving effective throughput without violating link-layer reliability (PR-2/PR-5).

Mode transitions are explicit and safe. A detach event (or link fault) drains in-flight frames, flushes class state, and returns the system to idle (laser off) before a new device can be attached. Hot swap from HID→MSC or MSC→HID therefore proceeds as, detach → SAFE/ARMED → re-enumerate → lock new mode. Throughout, power and optical safety are enforced locally

by the FSM, rails must be in tolerance and receiver unsaturated before any transition to activate. Any watchdog, brownout, CRC burst, or timing-guard violation forces SAFE (laser off) with a logged fault ticket. This single-device design meets the requirement for a single standard USB peripheral while keeping timing predictable and the implementation auditable.

#### 3.6.2.3 Emulation

The emulation unit enforces single-device operation (FR-3) and presents itself to the PC as either a HID or an MSC device never both at once. On link-up, it reads the mode flag from the hosting peer and binds a single USB device profile accordingly. In HID mode it enumerates as a standard keyboard or mouse interface with a fixed report descriptor. In MSC mode it exposes USB Bulk-Only Transport. This mutual-exclusion keeps endpoint scheduling deterministic and avoids composite-device timing edge cases on the host OS.

In HID emulation each framed HID report arriving over the optical link (CRC-16 verified, in-sequence) is written directly to the pre-armed HID driver, so that the PC's HID class driver receives events at the next poll interval with minimal software overhead. There are no competing endpoints in this mode, so the device stack maintains bounded end-to-end latency (PR-3) while preserving ordering and debouncing semantics expected by the OS.

MSC emulation, in storage mode, the unit implements the device side of bulk only transport. It accepts command block wrappers from the PC, maps each command to framed transactions over the link, and returns command status wrappers only after data integrity (CRC-32, sequence) is confirmed. Bulk IN/OUT pacing respects the host controller's max-packet cadence to avoid OS timeouts. Because no HID endpoints are active, bulk bursts can fully utilize the allocated TDD receive windows while remaining within the CRC budget (PR-2/PR-5).

Mode transitions & safety. If the link drops or the PC issues a bus reset, the Emulation unit tears down the active class cleanly, drives the laser-gate low via the safety FSM, and returns to IDLE/ARMED before re-enumeration. Switching HID↔MSC therefore follows: link or bus reset → SAFE/ARMED (laser off) → enumerate selected class. Any integrity or timing fault (watchdog, brownout, CRC burst, guard violation) forces SAFE immediately and persists a fault ticket for post-mortem, ensuring that optical output is never enabled outside a verified ACTIVE state while keeping the PC's view of the device stable and standards compliant.

#### 3.6.2.4 FSO integration

Transceiver FSO testing done proving HID hosting and emulation along with integrated FSO system performance was done stages of several tests as described below.

Test T006.1 FSO HID Transmission Distance Validation (refer to Appendix C section 9.3.12) evaluated the maximum transmission distance the custom designed FSO system (FR-7) can accommodate while emulating the HID peripherals (mouse and keyboard) from the transmitter end at the receiver end (FR-3, FR-4). Based on prior results from HID functionality and latency tests conducted, the system was programmed using ESP-IDF (PR-2, PR-3). Both the transmitter module and peripherals were powered using a power bank (PWR-2), enabling portable operation.

The maximum reliable distance achieved was 4.6 meters under indoor lab conditions, verified using a tape measure. HID events were accurately emulated at the receiver end. Precise laser alignment to the photoreceiver was critical for maintaining the optical link which when disturbed resulted in noise and disconnection. The end-to-end HID responsiveness below 50 ms was met the latency performance expectations.

### *3.6.3 End-to-End Integration*

System-level end-to-end integration tests were conducted to validate the full operation of the FSOCS. These tests included verification of HID functionality, including hot swapping between devices, as well as MSC read and write operations over the optical link. Additionally, latency and throughput measurements were performed to ensure compliance with the prioritised requirements (PR-2, PR-3, PR-5, PR-7), while power stability across both units was assessed under transient load conditions. The results of these tests confirmed that the integrated system met all design requirements, demonstrating reliable operation for both HID and MSC USB peripherals and validating the effectiveness of the staged integration strategy.

Test T002.2 Bidirectional FSO Link Test at 2 m (refer to Appendix C section 9.3.3) evaluated the integrated transceiver pair operating simultaneously in opposite directions to satisfy the bidirectional requirement (FR-1). The setup positioned transmitter-receiver apertures at a fixed 2 m separation with coarse mechanical alignment; ambient indoor lighting and nominal supply conditions were maintained. MSC endpoint was enumerated over the optical link in both directions, confirming device identification and descriptor exchange. The link maintained stable operation without re-enumeration, and throughput remained within the expected range for the selected baud and framing. Overall, the test validated bidirectional MSC functionality and confirmed the FSO path's readiness for longer-range trials.

Test T005.3 HID Hot Swapping Validation (refer to Appendix C section 9.3.11) verifies the ability of the FSO system to swap the HID peripherals mid-operation and identify the change and continue operation without having for a system reboot or significant delay. Upon disconnection of keyboard and connection of the mouse, the system resumed decoding seamlessly. Thus, HID data integrity and continuity were ascertained during the test.

Test T007.1 Link Interruption Recovery Test (refer to Appendix C section 9.3.13), was conducted to verify that the FSO system can recover from temporary link interruptions during HID peripheral operation. A keyboard connected to the transmitter module was used to send characters through optical link (FR-3), with emulated output displayed on the receiver-side PC. During the test, the laser path was intentionally blocked using an opaque surface for 5–10 seconds.

Observations made during test T007.1 were that keystrokes made after the interruption were not recorded which implied that HID output ceased immediately upon interruption. The system remained powered and stable even during link obstruction. Once the obstruction was removed, communication resumed automatically without requiring manual reset or system reboot (FR-6). The emulated output continued from the point of interruption, confirming the expected recovery behaviour.

## 3.7 Stakeholder Engagement Ethan

### *3.7.1 Key Stakeholder Engagement*

Table below highlights the stakeholders, information provided by each stakeholder, the medium used to engage with each stakeholder and the frequency of engagement between the stakeholders and the design team.

*Table 7: Stakeholder Management Matrix*

| Stakeholders | Information Provided | Medium | Frequency |
| --- | --- | --- | --- |
| Project Partner/Clients: ANFF | Project briefs and TQs | Written reports, emails, presentations and scheduled meetings | Weekly, or when required |
| End Users – ANFF Staff | TQs | Written reports and discussion forums | When required |
| Current Design Team | Meeting minutes and technical assistance | Meetings and emails | Daily |
| UWA Staff – Design Project Coordinators | Lecture slides, workshop relevant to the design project | Workshops, scheduled consultation and emails | Weekly, or when required |
| Meeting Facilitator | Feedback on the design team's professionalism, | Presentations, scheduled meetings and emails | Weekly |

| | | | |
| --- | --- | --- | --- |
| | teamwork and contribution. | | |
| Regulatory and Standard Bodies: AS/NZS | Regulations and standards relevant to the design project. | Written reports and emails | When required |
| Components Supplier | Components, part numbers and data sheets for hardware. | Calls, voicemails, emails and impromptu meetings | When required |

Compared to the stakeholder management matrix made, communication between the design project team and stakeholders was nearly identical. Throughout the design process, project clients communicated with the design project team through schedules technical queries. UWA staff and the meeting facilitator were communicated with through weekly schedule meetings, workshops and emails. Additionally, the design team communicated with each other daily through MS Teams and meetings with and without the meeting facilitator.

Only the regulatory and standard bodies were not communicated with, as the documents provided by AS/NZS documents were utilised to ensure all design met regulatory standards. Furthermore, component suppliers were only communicated with through impromptu meetings, as all components were bought in store or online.

### *3.7.2 Preliminary and Critical Design Review*

The preliminary design review highlighted the initial work for the operation and structural systems from the design project's architecture and discussed the progress in the respective subsystems.

Elements of the design process discussed in the preliminary design review included the concepts for the 3D printed chassis of the FSOCS, provided the optioneering of hardware for the design project such as the MCU, op amps and capacitors, simulations and breadboarding results for the laser diode transmitter and receiver circuits and the Firmware layers and flow overview.

The critical design review highlighted work on the operation and structural systems which had now reached its final iterations of prototyping.

Content from the critical design review included a new version of the chassis, technical designs of the MCU, transmitter and receiver PCB, and the simulation results and validation of board prototypes using the actual components for the final design product.

## 3.8 Safety Issues Identified

The key safety risks in the project and the specific design choices and procedures used to mitigate them are covered in this section. The focus is on three main areas: Optical, Electrical and Handling safety.

### *3.8.1 Optical Safety: Eye Hazard from Laser Emission*

*Table 8: Eye Hazard and Safety Measures from Laser Emission*

| Hazard | Mitigation |
| --- | --- |
| The primary safety concern is the potential eye damage from the laser.<br><br>In case of an IR laser, the beam is invisible, users lack a natural aversion response, increasing the risk of accidental exposure. | The safety measure is our custom-designed laser diode driver; (FR-7). It incorporates a potentiometer based current clamp that physically limits the current to the laser diode (FR- 12) As stated in section 3.4.2. This ensures the optical output power is always maintained at or below the Class 1M eye-safety limit fulfilling SR-1.<br><br>Additionally, the initial design used an 850 nm IR laser diode which was later replaced by a 650 nm visible red laser in the final product, ensuring users are aware of the path of light, reducing the risk. |

### *3.8.2 Electrical Safety: Shock and Fire Hazard*

*Table 9: Electrical Shock and Fire Hazard Safety*

| Hazard | Mitigation |
| --- | --- |
| The risk of electrical shock from exposed live circuits or a potential fire hazard from short circuits, particularly with the use of battery in the power bank. | The system is fully enclosed within a custom-designed chassis (PHY-2). This enclosure is constructed from a non-conductive material (PLA), preventing any accidental user contact with internal electronics (PHY-3).<br><br>All electronic circuits and PCBs were tested to ensure no short circuits, especially after SMD mounting of components.<br><br>While it is required to power the remote module using a standard commercial USB power bank (PWR-2). These certified devices have built-in safety features like |

| | |
| --- | --- |
| | overcurrent protection and short-circuit prevention, mitigating the risks associated with the battery. |

### *3.8.3 Handling Safety: Component Damage During Assembly*

In addition to the safety considerations of the final design, several procedural hazards were identified and mitigated during the prototyping and assembly phases.

*Table 10: Component Handling and Assembly Safety*

| Hazard | Mitigation |
| --- | --- |
| **Risk of damaging sensitive electronic components during the assembly process.**<br><br>Specifically, the VCSEL laser diode and MOSFETs are vulnerable to ESD, while the VCSEL is also susceptible to thermal damage during soldering. | During assembly, strict ESD precautions were enforced, especially when handling the VCSEL and MOSFETs.<br><br>To prevent thermal damage, low-thermal-mass soldering techniques and a temperature-controlled soldering iron were used to mount the heat-sensitive optical components.<br><br>Use of soldering paste and flux ensured improving heat transfer and preventing oxidation and allowed for completion of the solder joint faster and at a lower temperature. |
| **Toxic Fumes from Soldering.**<br><br>During the initial assembly of the through board prototypes, it was noted that soldering generated fumes in the workspace. | To address this, all subsequent soldering for the final PCBs was conducted in a designated well-ventilated area using a fume extractor. This procedural change ensured a safe working environment for all team members, in line with UWA laboratory safety guidelines. |
| **Risk of Burns from Hot Air Reflow**<br><br>The process of using a hot air reflow station for soldering SMD components presented a risk of burns. | A clear exclusion zone was established around the reflow station during operation. Team members used thermal-resistant gloves when handling recently heated PCBs, eliminating the risk of accidental burns. |
| **Risk of burns from overheating of circuit components** | Resistors of higher value were introduced in the path to limit current. The use of high performance OPA354 in the actual circuit significantly reduced the risk of overheating. Further, the final receiver PCB has four layers |

| | |
| --- | --- |
| The overheating of the MCP6002 integrated circuit during prototype testing presented a risk of burns. | and allows for better thermal dissipation as opposed to the through board base in the prototype. |
| **Risk of Cuts from Sharp Chassis Edges**<br><br>The initial version of the chassis featured sharp edges and unrounded corners, posing a potential safety hazard during handling and assembly. These features increased the risk of accidental cuts or abrasions for team members. | The design was revised collaboratively to include edge fillets and rounded corners. This modification significantly reduced sharp contact points, improving both safety and ergonomic handling during integration. |
| **Material Instability from Laser-Cut Construction**<br><br>There were concerns regarding potential splintering or dimensional expansion if laser cutting had been used for chassis fabrication. These risks could compromise structural integrity and precision fit. | The team opted for high-precision 3D printing using carefully calibrated measurements. This approach eliminated splintering risks and maintained consistent tolerances across all chassis components. |

### 3.9 Ethical Issues

While the design project is an innovative and prominent step forward in communication technologies in terms of security and high-speed data transfer, there are still ethical issues and concerns with FSOCS.

While ethical issues may not directly impact on the functionality and performance of a product, how an ethical issue can impact on the wellbeing of people's lives or affect society's trust in technology influences the credibility of our final design project.

One concern raised by society is the current applications of FSOCS, mainly the application of FSOCS in a military environment. Currently, the unique characteristics of FSOCS makes the communication system useful in a military environment due to laser communication providing large bandwidths, high data transfer rates and easy and quick deployment [2].

The concerns with the use of FSOCS introduce mistrust in the product, despite the efficiencies and innovations from the communication system. This is influenced by society's disapproval of using engineered products in actions that are deemed immoral or indirectly harmful to people's safety and wellbeing.

Another ethical issue raised by others is related to the security of FSOCS [3]. Despite being advantageous regarding security in communication technology, data privacy concerns and security issues persist in FSOCS due to its nature of being a LoS communication system.

FSOCS are still vulnerable to potential eavesdropping and interception and is hard to detect since it involves no physical tempering to either the transmitter or receiver. This is due to atmospheric scattering from wide divergence angles; the optical beam may wander from its desired path and can be intercepted by eavesdropper away from FSOCS receiver modules.

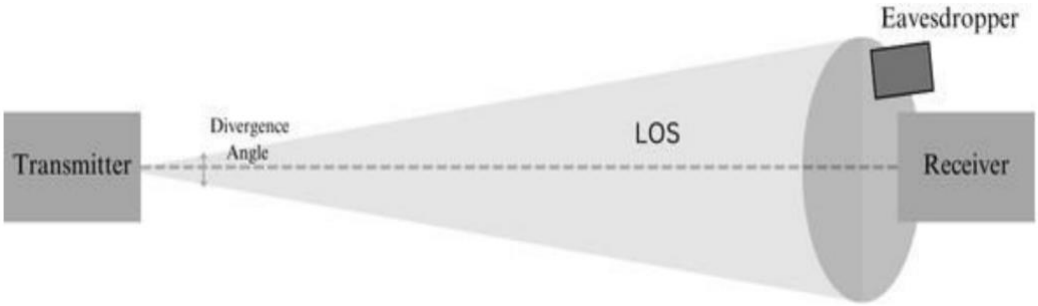


*Figure **36**: LoS Interception: Eavesdropper near Receiver [3]*

Furthermore, FSOCS are vulnerable to interception by multiple non-LoS links. While it may be more difficult to achieve since light captured may be weaker, interception may pose a significant threat to data security.

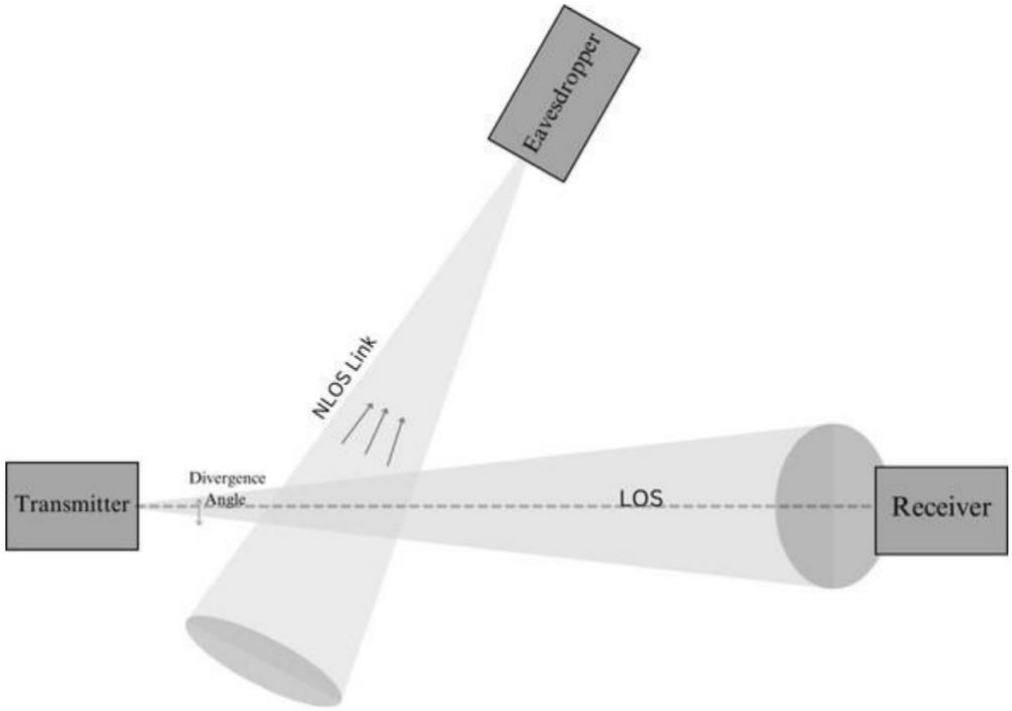


*Figure 37: Non-LoS Interception [3]*

## 3.10 Risks and Mitigation

Risk management is a critical aspect of engineering projects, ensuring that potential threats to scope, schedule, quality, and performance are identified early and addressed through proactive mitigation strategies. The project team maintained a structured Risk Register to document risks, assess their likelihood and consequence, assign responsibility, and propose mitigation measures. This approach ensured alignment with the project's requirements while maintaining transparency for stakeholders.

One of the most significant risks identified was the lack of clarity in the initial scope. Ambiguity in deliverables created the potential for divergence between stakeholder expectations and the prototype delivered. The potential impact of this risk was classified as *Major*, with a *Likely* occurrence, producing an Extreme risk rating. Without clear definition, the project could deviate substantially, resulting in unmet objectives or costly rework.

### *3.10.1 Risk Evaluation*

As shown in table 14, the project adopted a structured risk management methodology, guided by the principles of early identification, systematic assessment, and proactive mitigation. To provide consistency in evaluation, a series of standardised tables were applied to classify risks according to their consequence, likelihood, and required response. This ensured that project decisions were informed by objective assessments rather than subjective judgement, while

maintaining alignment with best practice in engineering risk management, refer to Appendix B.

The Descriptive Risk Levels provide actionable guidance by translating abstract ratings into specific management responses, refer to table 15 in appendix B. This ensures consistency in decision-making, as similar risks across different domains (e.g., technical, schedule, or resource risks) are treated with the same urgency. For example, a High risk in technical design complexity and a High risk in supplier delays would both be escalated to management attention and corrective action, despite originating from different causes.

The Likelihood Criteria add further implementation value by grounding assessments in observable frequencies rather than subjective impressions, refer to table 16 in Appendix B. This improves reliability by ensuring that risks are evaluated based on past evidence or realistic projections. For example, an "Unlikely" event is treated differently from a "Possible" event, even if their consequences are similar, ensuring that mitigation strategies remain proportional and evidence based.

This Risk Register outlines potential factors that may impact the successful delivery of the project. It records each identified risk, its likelihood, impact, and mitigation measures to ensure effective monitoring and control. The purpose is to proactively manage risks and support timely, high-quality, and cost-effective project outcomes. The detailed risk analysis and corresponding mitigation strategies can be found in Appendix B, ensuring transparency and traceability of project risk management.

### 3.11 List of Design Outputs

All design outputs were stored on a SharePoint folder which originates from the design team's MS Teams channel, making outputs readily available to the members of the design team, our meeting facilitator and UWA staff.

All files were organised into the following five folders:

I. LMS Content
II. Meeting Minutes
III. Design Project Reports
IV. Project Specs
V. Project Management

Throughout the design project's lifetime, 136 files (Excluding files from LMS Content and superseded content) were created to ensure that the final design product would fulfill all previously mention requirements and meet the expectations of stakeholders. Furthermore, multiple revisions of different documents were made throughout the design process. Because

of this, many files were stored in additional folders within the SharePoint called, “0 - Superseded Content” to ensure outdated files were not mistakenly referred to, while allowing members of the design project team to check through previous versions of documents in case.

### *3.11.1 LMS Content*

The documents located in the LMS Content folder are lecture slides provided by the design project’s coordinators and templates for documents and spreadsheets used in workshops throughout the design project’s lifetime.

The purpose of compiling all templates and documents provided by our design project coordinators was to be able to easily refer to previous content to ensure high quality documentation and reports.

### *3.11.2 Meeting Minutes*

The second folder in the SharePoint contained meeting minutes written by members of the design team. Meetings with the design team occurred once or twice a week, while meetings with the design team and our meeting facilitator occurred once a week.

The purpose of documenting the design teams meetings through the meeting minutes was to ensure that the team could maintain accountability and transparency between the other stakeholders. Furthermore, it helped provide continuity for members of the design team, with regards to previous decisions on the final design product, and the action items assigned to individual members of the team.

### *3.11.3 Design Project Reports*

The Design Project Reports folder not as well contained but also contained presentation materials from the design team’s preliminary and critical design review and supporting documents regarding the content to the reports. Supporting documents for the reports include research papers regarding FSOCS, standards from the AS/NSS that needed to be considered, and specifications/datasheets of certain components used in the final design product.

The purpose of the folder and its contents was to be able to conveniently provide requested documents and their sources to the design project stakeholders. This is since specific stakeholders, such as the design project coordinator and ANFF staff use written reports from the design team as a medium of communication, ensuring stakeholders with higher interest are well informed throughout the project’s lifetime.

### *3.11.4 Project Specs*

The Project Specs folder contained technical designs, prototypes, simulations, and testing documents. Additionally, the folder also contained answers to submitted technical queries to the project clients, ANFF, and safety and risk documents.

The purpose of the technical queries and the safety and risk documents was to ensure that any uncertainties throughout the design process were answered and shared conveniently. Additionally, the safety and risk documentation ensured that safe practices were used in laboratory environments and safety issues and risk that were identified by members of the design team were shared, making the rest of the design team aware of potential hazards.

The purpose of the simulation files was to test the performance of the transmitter and receiver circuit, specifically the output voltage from the receiver circuit, and the signal frequency achievable using different types of Op-Amps and resistor and capacitor values.

Prototyping files contained schematics and designs for the MCU, transmitter and receiver PCB. Additionally, it contained the 3D CAD files used to design and print the chassis, and the code for the three circuits to integrate all the separate components functionality. The purpose of compiling all the prototyping files for different aspects of the design projects architecture was to ensure designs and simulations were easily accessible to each member of the team, improving transparency and accountability. Furthermore, it would allow team member to easily assist other members of the design project when assistance was required.

### *3.11.5 Project Management*

The last folder in SharePoint contained files relating to managing the design team. This includes the design team's availability, roster for roles, the design project Gantt chart and action register, the design project's initial risk assessment, a SWOT exercise, and PPIR.

The purpose of the project management files was to ensure that the performance of the design project team was as efficient as possible, based on the design team's declared strengths, availability for meetings and work sessions, and level of willingness to learn new skills for the design project. This would allow the design project team to assign roles to individuals, tasks for the progression of the design project through the action register and reflect on the progression of the design project alongside the Gantt chart produced.

In addition to the project management files, the bill of materials, regarding the expenditure of the team to create the final design product, including supporting screenshots and downloads of invoices and receipts were included into the folder.

### 3.12 Final Costs

Based on the design project brief, the design project team needed to be constrained within a hard budget limit of $500 AUD for all prototyping activities to satisfy requirements made by the design project coordinators. To ensure that the final design product was created within the outline budget, the design project team recorded all receipts and invoices related to the design project and generated a bill of materials based on the final costs of the design project.

For the design project, most purchases were made for the final designed product, as most materials and components for prototyping, such as breadboards, male-to-male wires or resistors and capacitors for breadboards were readily available in laboratories such as the UWA Makers Lab and the UWA Robotics Lab.

All receipts and invoices provided by design team members were names using an alphanumerical code, where the first four letters referred to the location or website the purchase was made, and the number referred to the order the invoice or receipt was recorded.
The table below details the locations and websites from where additional components and PCBs were purchased for the design project, and the code used for each location referenced.

*Table 11: Code for Referencing Purchase Locations*

| Code | Location Reference |
| --- | --- |
| ALEX | AliExpress |
| ALTR | Altronics |
| JAYC | JayCar |
| DIGI | DigiKey |
| JLCP | JLCPCB |

The table in Appendix D details all items purchased by the design project team, the date of purchase, their costs per item alongside the total cost and reference receipt code. Based on Appendix D, the total expenditure for the design project was $465.75, which is 93.15% of the total budget given.

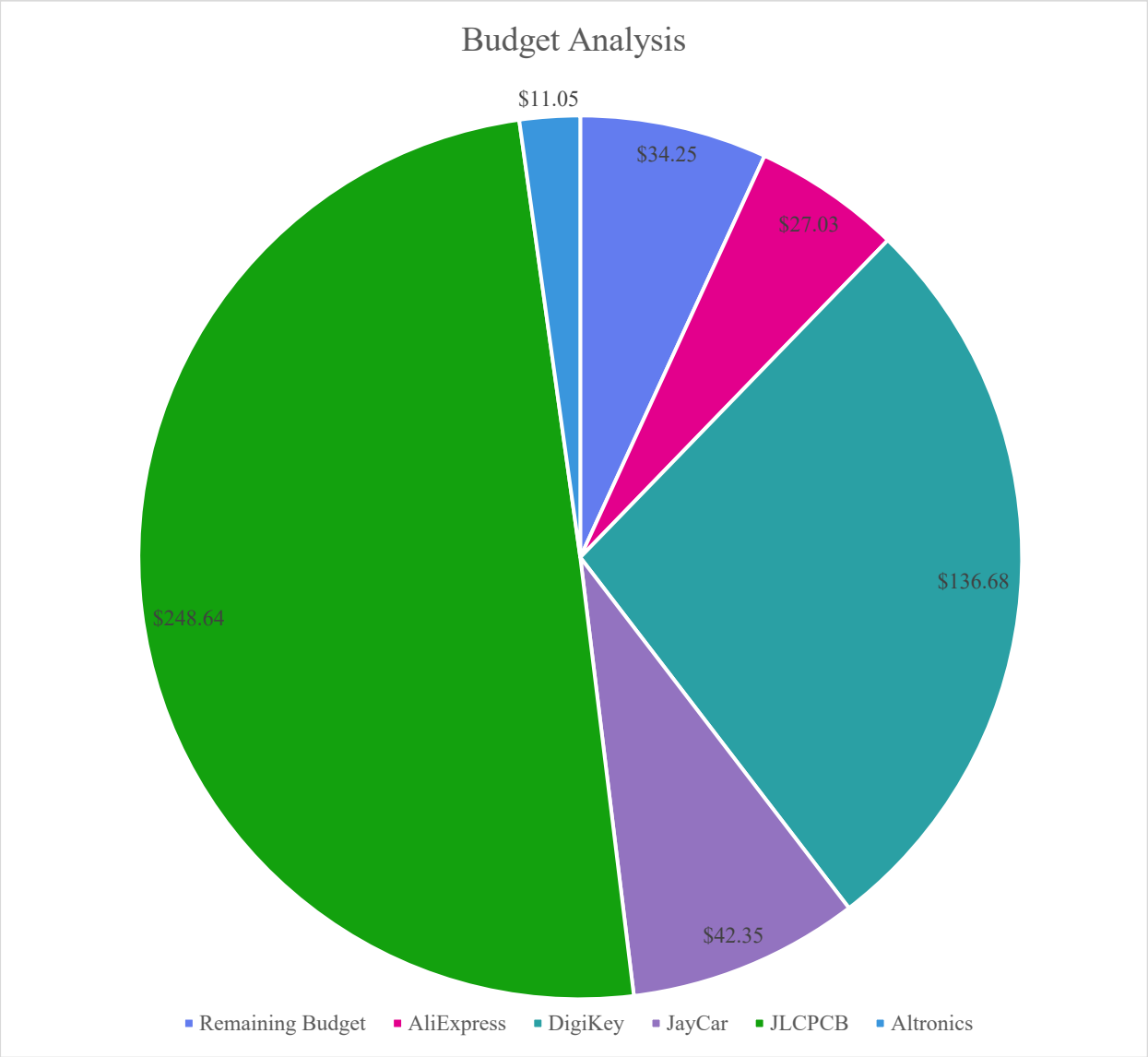


*Figure 38: Expenditure Analysis based on Purchasing Locations and Budget Remaining*

Based on list of items and their referenced receipts, most items were purchased from DigiKey. Most purchases for smaller components were made on DigiKey due to the stores' quick delivery time compared to other stores such as AliExpress owing to DigiKey already having stock of required components domestically.

Based on the figure above, the most expensive purchases, were made to JLCPCB. This is because purchases were for custom PCBs, with some small SMD soldered components such as resistors, capacitors and MCU already assembled onto the board. Additionally, JLCPCB required that any purchases had a minimum of five item, meaning even if the final design product only needed two MCU PCBs, we were still required to print and purchase three more. Furthermore, since JLCPCB is a manufacturing company residing overseas, costs were in international currency and included more substantial shipping.

# 4. Recommendations for Next Design

## 4.1 MCU

The MCU Circuit design followed standard while implementing personalised circuitry for the specific design application. The main improvements identified upon implementation would be to replace the headers to a standardised size to allow a better connection and more secure wiring to the separate boards.

Since the MCU board was the first design to be submitted to manufacturing aspects like the mounting to the chassis or additional copper connection were details not incorporated to the design. Progression to the next design phases allowed for the next PCB submission to incorporate the new design requirements and carry include lessons learned from the first design implementation.

Furthermore, while the design structure philosophy provided great benefit for the implementation of the first design, moving forward to a second design implementation with less time constraints, a single board design would be more provide a more sophisticated, compacted and less cost-effective design.

## 4.2 Transceiver

The current transceiver design successfully met the core project requirements, serving as a reliable proof-of-concept. The following recommendations aim to improve performance, reliability, and manufacturability in a future iteration.

### *4.2.1 Transmitter Module*

A key improvement would be upgrading the 2N7000 MOSFET to a dedicated high-speed, logic-level SMD MOSFET such as the BSS138 or IRLML6344. These devices offer lower gate charge and faster switching speeds, improving signal integrity and reducing propagation delay.

The current current-clamping method relies on a potentiometer as a voltage reference, which can fluctuate with supply variations. Replacing this with a precision voltage reference IC (e.g., TL431) would stabilise the clamp voltage, ensuring consistent compliance with Class 1M eye-safety standards under varying environmental and supply conditions.

#### *4.2.2 Receiver Module*

The receiver could benefit from reconfiguring amplification stages 2 and 3 to an inverting configuration, converting the photodiode's negative output to a positive signal suitable for MCU GPIO inputs.

Alternatively, the architecture could be simplified by reducing the three-stage design to two stages, with the final stage being a high-speed comparator. This would produce a clean digital output, improving timing accuracy and noise immunity.

Implementing an AGC circuit would further improve usability and reliability. The current fixed-gain receiver is highly sensitive to module alignment and distance. AGC would dynamically adjust the gain based on signal strength, preventing saturation at close distances and boosting weak signals at longer distances.

Finally, the ICL7660 charge pump, while effective, can inject switching noise into the negative supply rail, potentially degrading the TIA stage performance. Adding an LC filter on the output of the ICL7660 would suppress high-frequency noise, providing a cleaner supply and maximising receiver sensitivity.

Beyond these component-level improvements of the transmitter and receiver circuit, other recommendations include the fabrication and assembly processes being tendered to a professional contract manufacturer to ensure consistency, quality, and scalable throughput. Component sourcing should also transition from prototyping suppliers, such as DigiKey, to volume distributors or direct manufacturer supply, which would significantly reduce per-unit costs for critical components such as the OPA354 op-amps and OPV300 VCSELs.

Finally, to prepare the FSOCS for market deployment in Australia, formal regulatory compliance must be considered. The system should undergo testing and certification to obtain the Regulatory Compliance Mark, confirming that it meets all applicable electrical safety, EMC, and environmental standards.

By implementing these technical upgrades, production process enhancements, and regulatory measures, the next-generation FSOCS can move beyond proof-of-concept to a commercially viable, reliable, and safe product.

### 4.3 Chassis

The current version of the chassis meets most physical requirements made by the design project team. However, to the expand the functionality of the FSOCS, changes to the chassis would need to be made.

The designed final solution meets the expectations of the project's clients and ANFF staff for indoor laboratory use. But to make FSOCS more suitable for commercial use, modifying the chassis for outdoor environments, and unique placements and mounting would be needed.

### *4.3.1 Wall and Ceiling Mounting*

The first recommendation for the next design of the chassis would be to modify the chassis so that it can be mounted on walls and ceilings. By doing so, it would reduce the number of times an object or person may disrupt the operation of the modules.

This mitigates the risk of a person being impacted from the laser of the modules. Furthermore, moving the modules from a table to a wall mount or ceiling mount would ensure that the designed solution maintains the ergonomics of the working environment by allowing the modules to be distant from areas of large foot traffic or objects.

Mounting the chassis could be completed by securing brackets into the outside of the chassis, allowing the modules to be drilled into the wall or ceiling. Additionally, the chassis could be secured through suction mounting, which would allow the modules to be secured without having to modify any walls or ceilings.

### *4.3.2 Using the Modules in Outdoor Environments*

More practical uses for FSOCS, especially if used commercially, would have the modules placed at further distances and in an outdoor environment.

To ensure that a new iteration of the designed solution is more practical and suitable for commercial use, creating the chassis with regards to using the module in an outdoor environment would be needed.

A recommendation for the next iteration of the chassis would be to ensure that the chassis is able to achieve an IP53 rating or better, since it would ensure that the electrical components would have interference from dust particles or heavy rainfall. Additionally, the next version of the chassis design would also need to ensure that external lighting would not interfere with the operation of the photodiode.

### *4.3.3 Renewable Energy Source*

Using the modules in an outdoor environment provides more opportunities to power the modules instead of just using an external power bank. For example, solar and wind resource could be utilized to power the module during daylight or windy times, and external battery

storage could be connected to be charged during times of excess energy resource and be utilized when wind or solar resource are not available.

The figure below shows a larger version of the chassis which includes larger spacing between the PCBs and the edge of the chassis, preventing external lighting from interfering with the operation of the modules.

*Figure 39: Concept Version of the Chassis for Outdoor Use*

## 4.4 Firmware

To decrease retransmission cycles and increase throughput in variable optical conditions, future firmware versions may incorporate a more sophisticated error correction protocol, such as FEC or CRC optimisation.

Implementing a stable communication in dynamic environments would be ensured by the system's automatic modulation speed adjustment based on signal strength, ambient light, or optical interference using adaptive baud rate control and real-time link quality monitoring. To improve timing accuracy and lower latency, the firmware could be improved to use multi-threaded FreeRTOS tasks to separate signal processing, safety monitoring, and USB handling.

Adding temperature sensing, voltage/current monitoring, and laser output feedback to safety logic would improve dependability and guarantee complete adherence to Class 1M safety regulations in all circumstances.

### 4.5 General Recommendations for Future Designs

In addition to the specific improvements suggested for the MCU, transceiver, chassis, and firmware, several broader recommendations can be made to guide next-generation FSOCS designs.

Incorporating standard mounting points and enhanced modularity would streamline assembly and improve repeatability, while designing a single, compact enclosure could reduce alignment errors and increase portability.

Future designs would also benefit from implementing more comprehensive automated testing routines that cover power stability, latency, and optical signal integrity. Such testing would reduce integration time, catch early faults, and improve confidence in system performance before deployment.

Safety and reliability can be further enhanced by integrating overcurrent, overvoltage, and optical interlocks at both the hardware and firmware levels. These measures would ensure fail-safe operation and minimise the risk of damage to the system or connected peripherals.

From a manufacturability perspective, optimising PCB layouts for standard components and SMD footprints would facilitate automated assembly, reduce production costs, and minimise reliance on custom cables, thereby simplifying assembly and maintenance.

Finally, adopting a modular firmware architecture would allow the system to support additional communication protocols, such as wireless backup or higher-speed optical links, and enable easy hardware upgrades without requiring a full system redesign. This approach would enhance scalability and future-proof the FSOCS platform for evolving applications.

## 5. Design Completion and Demonstration

### 5.1 PCB Design Completion

The final MCU design incorporates the removal of diode D3 from the circuit to enable proper bidirectional communication. The 5 V power line, previously routed through D2, was reconfigured to include a 1-to-3 wire extension, distributing power to all connected modules and providing an additional spare line for future expansion. Similarly, the ground connection, formerly linked through D3, was modified to a 1-to-3 splitter, ensuring a common ground reference across the transmitter, receiver, and MCU circuits, with an extra spare lead available for potential system upgrades. These modifications improved power distribution flexibility and simplified future hardware integration. Furthermore, the signal wires attached to GPIO9 and GPIO18 to the signal output of the receiver and transmitter devices.

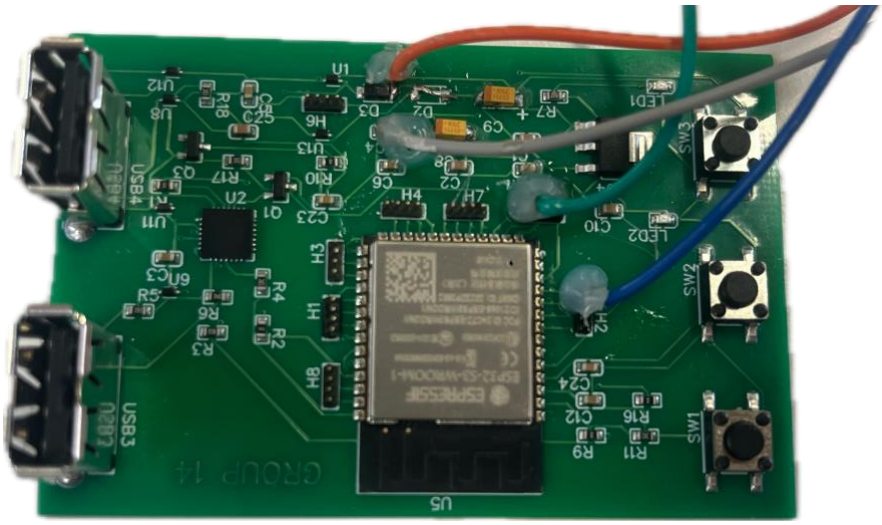


*Figure 40: Final MCU design*

The final transceiver PCBs incorporated into the design are shown in Figure **41** and Figure **42** below. Details on the design evolution and construction of the PCBs has been discussed in detail in section **Error! Reference source not found.**.

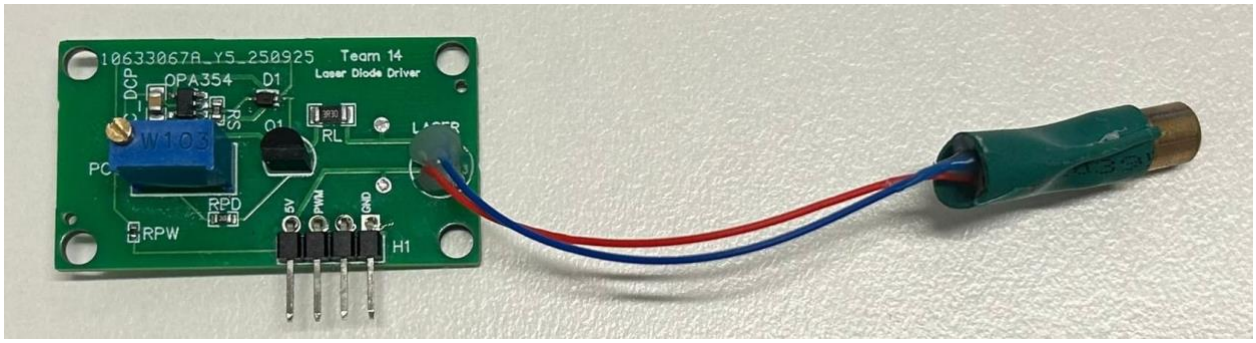


*Figure **41**: Final Laser Diode Driver PCB design*

The testing of the transmitter PCB for troubleshooting revealed that the diode D1 had been placed in opposite polarity, which was fixed by reversing the polarity and resoldering. The replacement of the IR laser with the visible red laser in the final design is also evident from figure above.

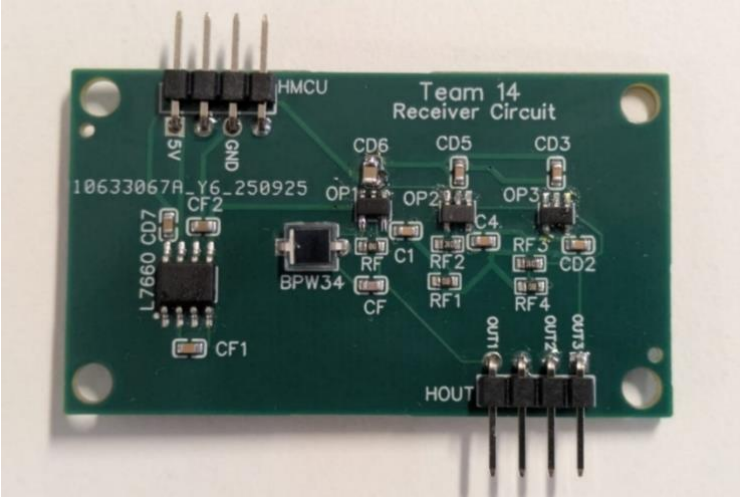


*Figure **42**: Final Receiver PCB design*

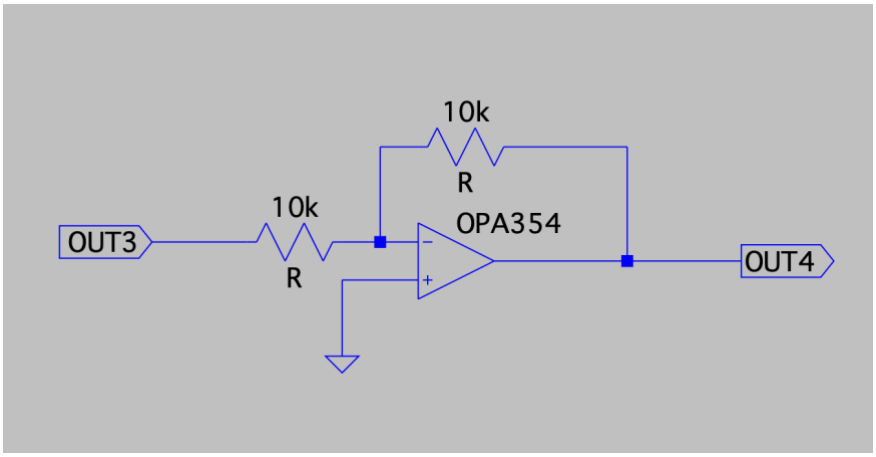


*Figure **43**: Schematic of the Inverting Amplifier Used to Correct Negative Output Voltage*

As described earlier, to address the issue of negative output voltage observed in the PCB, a simple op-amp inverting amplifier was added, as shown in figure above. This additional stage was mounted on the rear side of the final PCB to ensure the output polarity aligned with the MCU's input voltage range. The output signal (OUT3) from the receiver PCB was fed into the op-amp's inverting input through one 10 kΩ resistor, while another 10 kΩ resistor connected the inverting input to the op-amp output (OUT4). This configuration successfully inverted the signal polarity, thereby correcting the negative voltage issue in the receiver PCB.

## 5.2 Expectations

Based on our design, prototyping, and testing, we expect the final system achieve full functional bidirectional link, meaning the system will provide a stable, bidirectional free-space optical link capable of transparently extending a USB connection over a 2 m distance. Our testing indicates the hardware can achieve a maximum range of up to 4.6 m, exceeding the core requirement.

The system will also showcase complete HID Peripheral Support, fully supporting the seamless, low-latency operation of standard HID, specifically a mouse and keyboard, meeting the sub-50 ms latency target for comfortable use. Additional to this, the system is expected to automatically recover and re-establish the communication link after a temporary interruption, fulfilling requirement FR-6.

It is also expected that the system will successfully support a MSC device, allowing the host computer to recognise the drive and perform file read/write operations. Due to challenges identified during development, we anticipate that the data transfer rate may not steadily achieve the full 12 Mbps target of USB 2.0 Full-Speed.

The system is anticipated to be fully compliant with the Class 1M eye-safety standard. This is guaranteed by the custom-designed laser driver with its hardware-level current clamp, which has been calibrated and verified with a clamp meter and power calculations.

### 5.3 Demonstration

During the final demonstration, we will showcase the system's capabilities through a series of live, end-to-end tests. We will start with hardware demonstration by presenting the two fully assembled modules, highlighting the custom-designed PCBs (FR-13) and the 3D-printed chassis (PHY-2, PHY-3).

Next, we will connect a mouse to the remote module and demonstrate smooth, real-time cursor control on the host PC's screen to prove low-latency operation (PR-3).

We will then hot-swap to a keyboard and type in a text editor to show immediate, lag-free text input, further verifying HID support (FR-3). We will also connect a USB flash drive, showing it appears as a storage device on the host PC and perform a file transfer to and from the drive to demonstrate functional bidirectional data communication and error checking (FR-1, FR-6).

While moving the mouse, we will physically block the optical path with an object to simulate a link interruption. We will then remove the obstruction and show that the system automatically re-establishes the link and restores mouse functionality without any user intervention, demonstrating the autonomous recovery protocol (FR-6).

Most importantly we will explain the hardware-based safety mechanisms, pointing to the custom laser driver circuit (FR-7) and presenting the documented results from our optical power meter tests that confirm Class 1M compliance (SR-1). All the technical tests performed to verify the top 20 requirements identified, have been compiled in Appendix C with the verification and validation table in Appendix E.

# 6. Operation and Maintenance Guide

The FSOCS developed in this project enables for data transfer using light as the communication medium. The system consists of two modules that establish a two-way optical link using modulated laser signals. Each module connects to a USB interface, allowing the transmission of HID data, such as mouse and keyboard inputs, and general USB data between two computers through a free space optical channel.

This manual is intended to guide engineers, students, and technicians on how to effectively and safely operate and maintain the FSOCS. As such its main purpose is to ensure that users can set up, operate, and maintain the system to achieve reliable optical communication performance while maintaining compliance with safety standards.

## 6.1 System Overview

The FSOCS achieve its function by modulating light from a laser diode to transmit data though free space, while a photodiode in an amplifier circuit receives and convert the optical signals back into electrical form.

The system consists of two transceiver modules, with one powered from a USB port and the other powered from a portable power bank. Each module functions as both transmitter and receiver, allowing full duplex communication for devices such as keyboards, mice and USB data ticks. Below is a simple labelled diagram of one end of the whole FSOCS.

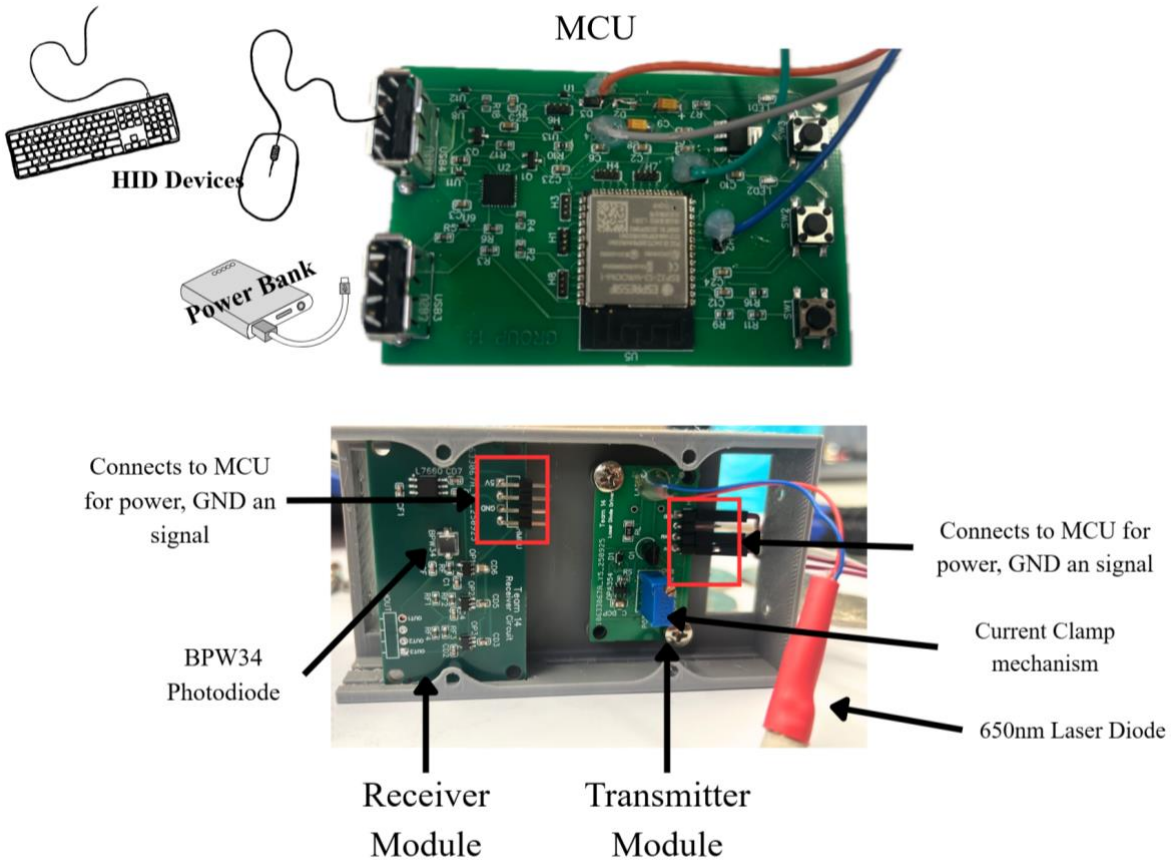


*Figure 44: FSO Communication System*

Consider the figure above, the main components of the FSOCS include the MCU, which handles all data encoding, decoding and USB communication. The laser diode driver converts digital signals into modulated current to control optical output; it includes an adjustable current clamp to maintain Class 1M laser safety compliance. The system also includes a photodiode in a transimpedance amplifier circuit that detects and amplifies incoming optical signals.

The entire system is enclosed within a PLA 3D-printed chassis that houses the sensitive electronic modules and provides structural support for optical alignment. The chassis incorporates mounting points for the laser and photodiode lenses, ensuring that the two modules can be precisely aligned for optimal light transmission and capture.

To operate the FSOCS, users will also need standard USB peripherals such as a keyboard, mouse, or data stick, as well as USB-A to USB-A cables for connection to the modules. One module connects to a computer via USB, while the other is powered using a portable power bank.

## 6.2 Safety Information

For your safety, please read and follow all instructions in this section before operating or maintaining the FSOCS. Failure to do so may result in personal injury or equipment damage.

### *6.2.1 Laser Safety*

Although the 650-laser diode operates under Class 1M safety limits, it must still be treated with caution:

- **Never look directly** into the laser beam or reflection paths.
- **Wear appropriate laser safety goggles** during alignment or testing procedure.
- **Avoid exposure** to the beam through optical instruments.
- **DO NOT** view the transmitter lens with magnifying optical instruments such as binoculars, telescopes, or microscopes. Viewing the beam through such instruments may pose an eye hazard.
- **DO NOT bypass** the laser driver's current clamp; it limits optical output to maintain Class 1M safety compliance.
- Always keep the **protective enclosure in place** during normal operation.

### *6.2.2 Electrical Safety*

- To prevent electrical damage, only use the specified power sources. The host module must be powered by a computer's USB port. The remote module must be powered by a standard, **certified commercial power bank**.
- **Disconnect all power** before performing wiring or maintenance to prevent any accidental discharge of power.
- **DO NOT open** the module enclosure while powered. Internal circuits may store charge even after disconnection.
- Ensure all cables are **securely connected** and free from damage before use.
- **DO NOT** modify or remove it, the 3D-printed PLA chassis provides **non-conductive protection** for internal components.

#### *6.2.3 Thermal Considerations*

The laser driver and MOSFET may reach elevated temperatures during prolonged operation. Therefore, allow the system to cool for at least 5 minutes after extended use before handling and avoid placing the modules on heat-sensitive or flammable surfaces.

#### *6.2.4 Personal Protective Equipment (PPE) and Emergency Procedures*

Operators must always wear appropriate personal protective equipment when working with the FSOCS system. Safety glasses or laser-rated goggles are required during optical alignment or any open-beam testing to prevent eye injury.

ESD-safe tools and grounding straps should be used when handling exposed circuit boards, to avoid electrostatic damage. The workspace should remain well-lit, dry, and free of clutter to minimise the risk of accidental contact or component damage.

In addition to PPE requirements, users must be familiar with emergency procedures including immediately disconnecting power and covering the optical aperture if the laser module becomes damaged or misaligned to prevent accidental laser exposure. Additionally, in the event of an electrical fault, smoke, or burning smell, disconnecting all power sources at once and allowing the system to cool completely before inspection or repair.

The design and operation of the FSOCS system comply with established standards and best practices to ensure safety, reliability, and proper functionality. Specifically, the system adheres to AS/NZS 3000, IEC 60825-1, IEC 61508, and AS/NZS ISO 45001.

### 6.3 Operating Procedure

The FSOCS system is designed to function as a transparent “wireless USB cable,” providing straightforward operation for standard USB peripherals. To ensure correct setup and safe operation, follow the steps below:

#### *6.3.1 Step 1: Setup*

Start by connecting the Host Module (labelled “HOST”) to an available USB port on the host computer. The red POWER LED should illuminate, indicating proper power. Next, connect the Remote Module (labelled “REMOTE”) to a charged USB power bank; its red POWER LED should also illuminate.

#### *6.3.2 Step 2: Module Alignment*

Place the two modules facing each other with a clear line of sight. The system is designed for a reliable operating range of at least 2 meters. Adjust the modules' orientation and distance as needed until the optical link is correctly aligned.

#### *6.3.3 Step 3: Connect a USB Peripheral*

Plug a single standard USB device, a keyboard, mouse, or USB flash drive into the USB-A port on the Remote Module. The system will automatically detect the device type and configure itself. Once connected, the peripheral should function as if it were directly attached to the host computer.

#### *6.3.4 Step 4: Status Indicators*

The system features a single red LED on the MCU PCB that serves as the power and status indicator. When the LED is illuminated, the module is receiving power correctly and the MCU is operational. If the LED is off, the module is not powered; users should check the USB connection, the power bank, or the host computer port.

In the event of abnormal LED behaviour, such as flickering, this may indicate power instability or a hardware fault, and the module should be disconnected immediately while following the emergency procedures outlined in section 6.2.4.

No additional configuration is required, as the system automatically manages device detection and data transfer once power is applied.

#### *6.3.5 Step 5: Shutdown and Storage*

After use, disconnect the modules from the computer and the power bank. Store the modules in a clean, dry location to protect the optics and electronics. Ensure the system has cooled if it was in operation for an extended period

### 6.4 Troubleshooting Guide

In the occasion of issues occurring with the system, please reference Table 12 which outlines common problems, possible causes and recommended solutions for quick troubleshooting.

*Table 12: Troubleshooting guide*

| Problem | Possible Cause | Solution |
|---|---|---|
| Peripheral is not working. | Optical Misalignment | Re-align the two modules until the proper alignment is established. Ensure the path is not obstructed. |
| | Link Interruption | The system is designed to automatically recover from interruptions, simply wait up to 10 seconds for the link to re-establish. |
| Remote module "POWER" LED is off. | The power bank is drained. | Recharge or replace the USB power bank. |
| Data transfer is slow or unreliable. | The optical lenses are dirty. | Power down the modules and gently clean the lenses with a soft, lint-free microfiber cloth. |

## 6.5 Recommended Maintenance & Tests

### *6.5.1 Maintenance*

Performing routine maintenance will ensure the system's lifetime and performance is prolonged and consistent. Refer to Table 13 for summaries of recommended maintenance tasks, descriptions and frequency.

*Table 13: Recommended Maintenance Tasks and Frequency*

| Task | Description | Frequency |
|---|---|---|
| Optical Cleaning | Clean laser and photodiode lenses using optical-grade microfiber cloths | Monthly or as needed |
| Electrical Inspection | Check solder joints, wiring, and connectors for wear or damage | Every 3 months |
| Firmware Updates | Update firmware using ESP-IDF Flash Tool | As updates become available |
| Alignment Check | Verify and re-align optical path using the visible laser | Before long-range testing |
| Visual Inspection | Check that the chassis is undamaged and that the optical lenses free of dust or fingerprints. | Monthly |

### *6.5.2 Operational Tests*

To confirm that the system is functioning properly, perform the following operational tests.

a) Functional Test: If the system has been in storage, perform a quick functional test by connecting a mouse and verifying smooth cursor movement. This confirms both power and link integrity.

b) Laser Driver Current Verification: Measure current draw to confirm it remains below design threshold.

c) Signal Strength Test: Use an oscilloscope to measure the optical output and received signal and ensure consistent performance and reliable data transmission.

## 6.6 Ethical and Professional Standards

While the system link is inherently secure against RF eavesdropping, it is a LoS technology. Users must ensure that the physical environment prevents unauthorised interception of the optical beam to maintain data privacy.

For precaution, avoid transmitting sensitive or personal data across the optical link. Always follow IEEE ethical engineering principles, prioritising user safety, system transparency, and environmental responsibility.

## 6.7 Deliverables and Supporting Outputs

The project deliverables include a complete set of design outputs which culminate in a functional physical prototype. The core system components include:

### *6.7.1 Firmware*

Developed in C/C++ using the ESP-IDF framework, the firmware features modular architecture with layers for USB Host/Device functionality, UART communication, and optical data handling. This design ensures scalability for future enhancements.

### *6.7.2 Electronic Hardware*

Custom PCBs designed in EasyEDA include full circuit schematics, labelled test points, and component values for easy verification.

### *6.7.3 Mechanical Hardware*

Module housing and optical alignment mounts were designed in Fusion 360 to support precise lens positioning and system protection.

All hardware and software outputs are structured to facilitate testing, maintenance, and future development, supporting open-source collaboration and reproducibility.

## 7. Conclusion

The 2-Way FSOCS meets its design objective, which is to provide a transparent USB extension by means of a free-space optical connection that functions with similar efficiency and reliability as a wired interface, very effectively. The system met or surpassed almost all the primary functional, performance, power, safety, design, and physical requirements set at the beginning of the project thanks to thorough engineering and iterative testing.

With a latency of less than 50 ms, the 2-Way FSOCS was able to provide smooth, user-transparent communication. While the host ran exclusively on USB power and the remote module ran for more than two hours on a regular power bank, features like error detection, automatic retransmission, and link recovery protected dependability.

Hardware interlocks provided fault protection, and the system complied with IEC 60825-1:2022 and Class 1M laser safety standards. While changes like removing diodes D2 and D3 and adding 1-to-3 power and ground splitters improved current distribution and communication integrity, the custom PCB increased signal accuracy and power stability.

The FSOCS connects the flexibility of optical communication with the dependability of wired USB by fusing performance, security, and usefulness. It is a safe, economical, and energy-efficient way to turn conceptual design into working reality. In addition to fulfilling all design specifications, the project establishes a solid basis for upcoming optical systems that will have scalable multi-channel operation, automatic alignment, and higher data rates.

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# 9. Appendices

## 9.1 Appendix A

*Table 14: Other Requirements*

| No. | Requirement ID | Description |
| --- | --- | --- |
| 21 | PHY-1 | The chassis shall meet an Ingress Protection rating of at least IP51. |
| 22 | PR-7 | The system should operate reliably within an ambient laboratory temperature range of 15° C to 30°C. |
| 23 | FR-10 | The system shall re-establish a communication link within 5 seconds of the optical path being restored after an interruption. |
| 24 | PHY-6 | The system shall provide visual status indicators on each module for Power, Link Status, and Data Activity. |
| 25 | PHY-5 | All external ports on the chassis shall be clearly labelled. |
| 26 | PR-4 | The system shall complete its power-on self-test and be ready for operation within 10 seconds of being powered on. |
| 27 | PHY-2 | The chassis shall fully enclose all internal electronic components. |
| 28 | PHY-3 | The chassis shall be constructed from a non-conductive material (3D-printed PLA or ABS). |
| 29 | PHY-4 | The chassis shall provide stable, rigid mounting for the optical components to maintain alignment during normal handling. |
| 30 | DC-1 | The project team shall remain within a hard budget limit of $500 AUD for all prototyping activities. |
| 31 | DC-2 | All project deliverables shall be submitted via a shared Git repository. |
| 32 | DC-3 | All project deliverables shall be licensed under the CERN-OHL-P open-source license. |
| 33 | DC-4 | The team shall return all physical components purchased for the project to the university upon completion. |
| 34 | DC-5 | The team shall submit only a single, consolidated reimbursement claim for all project expenses. |

## 9.2 Appendix B

*Table 15: Risk Level Classification and Action Priority Matrix*

| Risk Level | Priority | Example Action |
|---|---|---|
| Extreme | 1 | Cease activity or task; detailed research and planning required. |
| High | 2 | Senior management attention; immediate corrective and preventative action required |
| Moderate | 3 | Management responsibility assigned; corrective and preventative action plan developed |
| Low | 4 | Manage by routine procedures; accept risk |

*Table 16: Qualitative Risk Assessment Matrix*

| | Consequences | | | | |
|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 |
| **Likelihood** | Insignificant | Minor | Moderate | Major | Catastrophic |
| Always | H | H | E | E | E |
| Likely | M | H | H | E | E |
| Possible | L | M | H | E | E |
| Unlikely | L | L | M | H | H |
| Rare | L | L | L | M | H |

*Table 17: Level of Likelihood Descriptive table*

**Criteria should be read as 'either/or'**

| ***Level*** | ***Description*** | ***Criteria*** |
|---|---|---|
| A | Always/Certain | The impact will occur<br>The impact occurs in all circumstances<br>The impact occurs daily |
| B | Likely | The impact is expected to occur<br>The impact will occur in most circumstances<br>The impact occurs weekly/monthly |
| C | Possible | The impact will probably occur<br>The impact has occurred before<br>The impact will occur under some circumstances<br>The impact occurs annually |

| | | |
| --- | --- | --- |
| D | Unlikely | The impact could occur at some time<br>The impact has happened elsewhere (possibly recently)<br>The impact occurs every 10 years or so |
| E | Rare | The impact may occur in very exceptional circumstances.<br><br>A similar incident has occurred elsewhere.<br>Almost impossible. |

\

*Table 18: Project Risk Register*

**PROJECT RISK REGISTER**
A risk is any factor, event or influence that threatens the successful completion of the project.

| RISK DESCRIPTION (Adjust sub headings to suit your project) | | POTENTIAL IMPACT | RISK ASSESSMENT | | | RISK TREATMENT / MITIGATION | RESPONSIBILITY | Mitigation Risk |
|---|---|---|---|---|---|---|---|---|
| | | | Consequence | Likelihood | Risk Rating- from risk matrix | | | Risk Rating- from risk matrix |
| **NO** | **Project Scope** | | | | | | | |
| 1 | Initial scope provided is unclear in several areas. | Project delivered varies significantly from what the client wanted. | Major | Likely | Extreme | Clarify scope at next project partner meeting and confirm via detailed reverse brief. | Current PM | High |
| 2 | Design complexity underestimated | Incomplete or non-functional prototype | Major | Possible | High | Break into subsystems; validate each incrementally | PM + Tech Lead | Moderate |
| 3 | Incomplete requirement documentation | Misalignment between project outputs and expectations | Major | Likely | Extreme | Conduct requirement workshops and maintain a traceability matrix | PM | Moderate |
| 4 | Overly ambitious scope for given timeframe | Project delays, incomplete features | Major | Possible | High | Perform feasibility analysis, prioritise MVP | PM + Client | Moderate |
| 5 | Changing requirements mid-project | Time wasted re-designing | Moderate | Possible | High | Lock scope after review; document all changes formally | PM | Moderate |
| | **Project Quality** | | | | | | | |
| 6 | Insufficient testing before submission | Undetected defects, system failures | Major | Likely | Extreme | Develop and execute detailed test plan | QA / Test Lead | High |
| 7 | Lack of peer review for design documents | Design flaws not identified early | Moderate | Likely | High | Implement mandatory peer review process | PM + Team members | Moderate |
| 8 | Poor version control practices | Lost work, integration conflicts | Major | Possible | High | Use Git branching strategy and regular merges | Team members | Moderate |
| 9 | Project Team has no experience with the nominated CAD drafting package. | CAD design output is not polished. | Moderate | Possible | High | Get up to speed with CAD asap. | Team members | Moderate |
| 10 | PCB/Layout errors | Prototype unusable | Major | Possible | High | Peer review schematics & PCB before fabrication | Hardware Lead | Moderate |
| 11 | Simulation not matching real-world | Circuit fails on breadboard/PCB | Major | Possible | High | Validate sim with datasheets + prototype tests | Simulation Lead | Moderate |
| 12 | Op-amp speed too low (slew-rate/GBW) | Distorted signals, comms failure | Major | Possible | High | Use high-speed op-amps (OPA354, LT1800) | Analog Lead | Moderate |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **Project Schedule** | | | | | | | |
| 13 | Timeline management | Missing key deadlines | Major | Possible | Extreme | Gantt chart tracking; weekly check-ins | PM | High |
| 14 | Team member illness or unavailability | Delays in key deliverables | Major | Possible | High | Cross-train team members, maintain backups | PM | Moderate |
| 15 | Unforeseen technical challenges | Delays in implementation | Major | Possible | High | Allocate contingency buffer in timeline | PM | Moderate |
| 16 | Delivery delays of components | Testing phase shortened | Major | Likely | Extreme | Order early; use local suppliers (RS, Element14) | Procurement | High |
| 17 | PCB fabrication delays | No time left for testing | Major | Likely | Extreme | Order PCB early; use fast-turn services (JLCPCB express) | PM | High |
| | **Project Cost** | | | | | | | |
| 18 | Supplier price changes | Exceeds budget | Moderate | Possible | Moderate | Lock supplier quotes early, compare multiple vendors | Procurement | Low |
| 19 | Unexpected rework costs | Reduced available budget | Major | Possible | High | Validate designs early, maintain review gates | PM | Moderate |
| 20 | Limited cost | unbudgeted material, and penalty in the final grade | Moderate | Unlikely | Moderate | Budgeting control document and quality assurance | Budget control | Low |
| | **Project Stakeholders** | | | | | | | |
| 21 | Stakeholder unavailability | Delayed approvals or feedback | Moderate | Likely | High | Establish escalation path and alternate contacts | PM | Moderate |
| 22 | Misalignment between internal and client priorities | Conflicting expectations | Major | Possible | High | Regular alignment meetings, documented agreements | PM | Moderate |
| 23 | Miscommunication with lecturer/client | Wrong deliverables | Moderate | Possible | High | Regular updates + meeting notes | PM | Moderate |
| 24 | Poor internal communication (between team members) | Missed deadlines, duplicated work, inconsistent results. | Moderate | Likely | High | Weekly stand-up meetings, Slack/Teams channel, assign responsibilities clearly. | All team members | Moderate |
| | **Firmware & Hardware Integration** | | | | | | | |
| 25 | Incompatible firmware versions | System instability | Minor | Possible | High | Version control with tagged releases | Firmware Lead | Moderate |
| 26 | Communication protocol mismatch between modules | Data loss, system errors | Major | Possible | High | Define protocol specs early; simulate with test data | Firmware Lead | Moderate |
| 27 | Power rail dropouts under load | System reset or failure | Major | Likely | Extreme | Include bulk decoupling capacitors and power monitoring | Hardware Lead | Moderate |
| 28 | Overheating of power components | Hardware damage, safety risk | Minor | Possible | Extreme | Include thermal sensors and heat sinks | Hardware Lead | Moderate |
| | **External factors** | | | | | | | |
| 29 | Supply chain disruptions | Delay in materials | Major | Possible | High | Identify alternate vendors | Procurement | Moderate |
| 30 | Power outages during testing | Interrupted experiments, data loss | Moderate | Possible | Moderate | Use UPS backup system | PM | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 31 | Environmental interference (temperature, humidity) | Inconsistent test results | Moderate | Possible | Moderate | Test in controlled conditions | Hardware Lead | Low |
| | **Safety in Design** | | | | | | | |
| 32 | Laser usage (Class 1M) | Eye hazard | Minor | Possible | Moderate | Use safety glasses, beam blocks, test in controlled space | Safety Officer | Low |
| 33 | High-current electronics | Shock, burns | Major | Possible | Extreme | Limit voltages, fuse protection, simulation before testing | Safety Officer | Moderate |
| 34 | Soldering risks | Burns, toxic fumes | Major | Possible | Extreme | Use fume extractor, PPE | Safety Officer | Moderate |
| | **Other** | | | | | | | |
| 40 | EMI/Noise in receiver circuit | Signal corruption | Moderate | Likely | High | Shielding, proper grounding, low-noise op-amp | Analog Lead | Moderate |
| 41 | Overshoot in driver (ringing) | Laser diode damage | Major | Possible | Extreme | Add gate resistor/ferrite bead; simulation verification | Driver Lead | Moderate |
| 42 | MCU–driver–receiver timing mismatch | Link unstable | Major | Possible | High | Timing tests, scope verification | Firmware Lead | Moderate |
| 43 | Firmware Integration: Integrating the USB Host stack, TDD protocol, and data link protocol is complex | Real-time performance issues, dropped data packets, or system instability. | Major | Possible | Extreme | Develop and test each Firmware module independently before integration. | Firmware Lead | Moderate |
| 44 | Power Supply Noise: Digital switching noise from the ESP32 couples into the sensitive analogue TIA and clamp circuits. | The receiver's signal-to-noise ratio is poor, leading to a high bit-error rate. | Major | Possible | Extreme | Use separate power planes for analogue and digital sections on the PCB, with decoupling capacitors at every IC. | Hardware Lead | Moderate |

## 9.3 Appendix C

**TECHNICAL TEST FORMS**
Please find the video recordings of the tests in the Github link attached - https://github.com/luipulaus02-dev/UWA-Design-Unit-Team-14-2025/tree/Proof-Videos

### *9.3.1 Technical Test T001.1 Host Communication (Verification)*

| **Test No:** T001.1 | Date: | 2/10/2025 |
| --- | --- | --- |
| | Location: | UWA Makers Lab |

**Test Title:** Host Communication (Verification)

**Test Objective**

The objective of this test is to verify that each module has a functional USB I/O interface capable of successful host communication. This includes confirmation of physical wiring integrity, device recognition by the host computer, and successful transfer of a test data file.

Covering requirements: **FR-2, PR-5, PR-3**

**Test Environment**

Test involves using the Prototypes Transmitter and receiver circuit:

- Hardware:
  - FSOCS Host module
  - FSOCS Peripheral module
  - Standard USB cable(s)
- Software/Tools:
  - Device Manager (Windows) or equivalent USB diagnostic tool (Linux/macOS)
  - File transfer utility (e.g., drag-and-drop, command-line copy)
- Measurement Tools:
  - Digital Multimeter (for continuity/wiring check)
- Conditions:
  - Stable bench power supply (5 V USB input)
  - Ambient temperature ~22 ± 5 °C

**Test Cases**

T001 includes:
1) Wiring connection test
2) Run device manager and test
3) Transfer test data file

Included in T001.1:

1. Wiring Connection Test

- Inspect physical USB wiring and perform continuity check with DMM.

**2.** Device Recognition Test

- Connect module to host PC.
- Confirm module is detected in Device Manager (Windows) or via lsusb (Linux).

**3.** Data Transfer Test

- Transfer a known test data file (e.g., 10 MB).
- Observe for successful completion and data integrity.

**Acceptance Criteria**

For T001:

1. No internal short or incorrect connection between ports.
2. Host PC successfully detects module as a USB device.
3. Test file transfers successfully with no corruption.

Additional Included in T001.1:

**Reporting**

- Continuity checks passed.
- Device was recognized in host device manager.
- Transfer success confrimed.
- Anomalies, such as connection failures, driver issues, or corrupted transfers noted.

### *9.3.2 Technical Test T002.1 Unidirectional FSO Link Test with 2m Distance*

| **Test No:** T002.1 | Date: | 02/10/2025 |
| --- | --- | --- |
| | Location: | UWA Makers Lab |

**Test Title:** Unidirectional FSO Link Test with 2m Distance

**Test Objective**

The objective of this test is to verify that the Free Space Optical (FSO) system can transmit and receive data reliably over a 2 m optical link. The test validates optical communication by transferring files between modules, confirming data integrity, and assessing error performance.

Covering Requirements: **FR-1, PR-1, FR-5**

**Test Environment**

Test involves using the Prototypes Transmitter and receiver circuit:

- Hardware:
  - FSOCS host module – MCU + Transmitter circuit prototype (A)
  - FSOCS peripheral module – MCU + Receiver Circuit prototype (B)
  - Optical alignment setup ensuring 2 m separation
- Software/Tools:
  - Serial monitor for link verification
  - Arduino IDE for development and verification
- Measurement Equipment:
  - Tape measure / iOS measure App for transmission distance
  - Serial monitor for display and verification
- Conditions:
  - Indoor lab setting with controlled artificial lighting (~22 ± 5 °C)
  - No obstructions between transmitter and receiver modules

**Test Cases**

T002.1 includes:

1. Connect modules and keep them 2m away from each other
2. Program A to send PWM signal through Laser and B to detect signal
3. Send signal from A→B, by powering both A and B
4. Confirm the reception by verifying serial monitor display “HIGH” or “LOW” corresponding to signal from A
5. Repeat steps 2–5 to validate repeatability.

**Acceptance Criteria**

For T002.1:

1. On the receiver side, serial monitor shows the original signal
2. No link oscillations or resets
3. Successful data transfer without errors

**Reporting**

- Recorded transfer success at 2 m
- No anomalies, such as connection failures, driver issues, or corrupted transfers.

### *9.3.3 Technical Test T002.2 Bidirectional FSO Link Test with 2m Distance*

| | | |
|---|---|---|
| **Test No:** T002.2 | Date: | 18/10/2025 |
| | Location: | UWA Makers Lab |

**Test Title:** Bidirectional FSO Link Test with 2m Distance

**TestObjective**

This test evaluated the integrated transceiver pair operating simultaneously in opposite directions to satisfy the bidirectional communication requirement. The goal was to confirm that the Free Space Optical (FSO) system can reliably support Mass-Storage-Class (MSC) endpoint enumeration and data exchange over a 2-meter optical link in both directions.

Covering Requirements: **FR-1**

**Test Environment**

Test involves using the Prototypes Transmitter and receiver circuit:

- Hardware:
  - FSOCS transmitter module
  - FSOCS receiver module
  - Laser diode and photoreceiver pair (bidirectional configuration)
  - PC host for MSC endpoint enumeration

- Software/Tools:
  - ESP-IDF framework for firmware development
  - USB protocol stack with MSC support
  - Serial monitor and USB descriptor inspection tools
- Conditions:
  - Indoor lab setting with controlled artificial lighting (~22 ± 5 °C)
  - No obstructions between transmitter and receiver modules
  - Coarse mechanical alignment of transmitter and receiver apertures

**Test Cases**

T002.2 includes:

1. Position transmitter and receiver modules at a fixed 2-meter separation.
2. Enable bidirectional optical communication using dual laser-photoreceiver pairs.
3. Enumerate MSC endpoint over the optical link in both directions.
4. Confirm device identification and descriptor exchange.
5. Monitor for re-enumeration events or link instability.
6. Measure throughput and verify framing integrity.

**Acceptance Criteria**

For T002.2:

1. MSC endpoint successfully enumerates in both directions.
2. Device descriptors are exchanged without error.
3. Link remains stable with no re-enumeration or resets.
4. Throughput remains within expected range for selected baud rate and framing.
5. Communication integrity is maintained across both channels.

**Reporting**

- Transmitter and receiver modules operated simultaneously in opposite directions over a 2-meter FSO link.
- MSC endpoint was successfully enumerated in both directions, confirming bidirectional descriptor exchange.
- No re-enumeration or link resets occurred during the test.
- Throughput remained within expected range for the configured baud rate.
- The test validated bidirectional MSC functionality and confirmed the FSO path's readiness for longer-range trials.

### *9.3.4 Technical Test T002.3 UART-Based Character Transmission over 2 m FSO Link*

| **Test No:** T002.3 | Date: | 02/10/2025 |
| --- | --- | --- |
| | Location: | UWA Makers Lab |

**Test Title:** UART-Based Character Transmission over 2 meter FSO Link

**Test Objective**

This test validates the ability of the FSO system to transmit structured character data using UART emulation over a 2-meter optical link. The transmitter and receiver modules were programmed using ESP32-S3 boards and ESP-IDF/Arduino framework. The goal was to confirm reliable character-level communication using a custom optical UART protocol at 9600 baud rate.

Covering Requirements: **FR-1, FR-5, PR-1**

**Test Environment**

Test involves using the Prototypes Transmitter and receiver circuit:

- Hardware:
  - FSOCS transmitter module
  - FSOCS receiver module
  - PC host for serial monitoring
- Software/Tools:
  - ESP-IDF framework for firmware development
  - Arduino framework with ESP-IDF backend
  - Serial monitor for output monitoring
- Measurement Equipment:
  - Tape measure / iOS measure App for transmission distance
  - Serial monitor for display and verification
- Conditions:
  - Indoor lab setting with controlled artificial lighting (~22 ± 5 °C)
  - No obstructions between transmitter and receiver modules
  - Fixed 2-meter separation between modules

**Test Cases**

T002.3 includes:

1. Program transmitter to send UART-style optical signals
2. Program receiver to decode optical signals
3. Transmit demo message ("Yuki!") periodically.
4. Forward UART input from PC to transmitter and observe receiver output.
5. Monitor for framing errors, signal loss, or distortion.

**Acceptance Criteria**

For T002.3:

1. Receiver accurately reconstructs transmitted characters.

2. No framing errors or corrupted characters under stable alignment.
3. Data transfer rate matches expected baud rate (9600 bps).
4. Communication remains stable over 2-meter link.

**Reporting**

- Transmitter successfully sent structured character data using UART-style optical signalling.
- Receiver decoded and printed characters with no framing errors under proper alignment.
- Data transfer rate confirmed at 9600 bits per second (bps)
- Communication frequency per bit: 9.6 kHz.
- Demo message "Yuki! " transmitted every 2 seconds.
- During instances of laser-photoreceiver misalignment, the receiver displayed “Framing Error” on the serial monitor, indicating loss of synchronization and confirming sensitivity to optical path stability
- Test confirms reliable character-based data transfer over FSO link using ESP32-S3 modules.

### *9.3.5 Technical Test T003.1 UART-Based Character Transmission over 2 m FSO Link*

| **Test No:** T003.1 | Date: | 07/08/2025 |
| --- | --- | --- |
| | Location: | Makers Lab |

**Test Title:** Optical Safety & Driver Controls

**Test Objective**

The objective of this test is to confirm Class 1M laser safety compliance (SR-1) and validate the functionality of the custom-designed laser driver (FR-7) equipped with an adjustable current clamp (FR-12). This test ensures that the current-limiting function operates correctly and that the optical output remains within the Class 1M AEL limit under controlled laboratory conditions.

Covering Requirements: **SR-1, FR-7, FR-12**

**Test Environment**

Transmitter Circuit: Both visible (650 nm, red) and infrared (850 nm, OPV300) lasers were tested.

- Hardware:
  - Completed the PCB transmitter circuit
  - Used a 650 nm visible laser instead of the OPV300 (850 nm) for comparison tests
- Software/Tools: Hardware:
  - ESP-IDF
- Measurement Equipment:
  - Multimeter for voltage measurement and clamp meter for current measurement
- Conditions:
  - Indoor lab setting with controlled artificial lighting (~22 ± 5 °C)

**Test Cases**

The purpose of Test T003 is to verify the electrical and optical performance of the laser module to ensure compliance with Class 1M laser safety standards.

- Measure the voltage across the laser diode terminals.
- Measure the current flowing through the laser diode.
- Calculate the optical power output and verify whether it satisfies the Class 1M Accessible Emission Limit (AEL).

**Acceptance Criteria**

1. Voltage and Current Range:

- The measured voltage across the laser terminals must not exceed the rated value specified in the datasheet.

- For the invisible (IR, 850 nm) laser, the maximum rated voltage is 2.2 V.
- For the visible red (650 nm) laser, the maximum rated voltage is 2.3 V.
- The operating current must remain within the safe range defined by the current clamp setting (within ± 5%).

**2.** Power Calculation:

The calculated optical output power (P = V × I) must remain below the Class 1M AEL limit for the given wavelength and aperture size (per IEC 60825-1 standard).

- For the invisible (IR, 850 nm) laser, the AEL is approximately 0.78 mW.
- For the visible red (650 nm) laser, the AEL is approximately 0.39 mW.

**3.** System Integrity:

- No abnormal heating, flickering, or current spikes should occur during operation.
- The laser should emit a stable beam without visible degradation or instability.

**Reporting**

- The OPV300 (850 nm infrared laser) was tested using an IR camera, but no emission was detected, confirming that the device was not operating.
- The measured forward voltage was approximately 3.3 V, which exceeds the rated range of 1.6–2.2 V. This suggests either:
  - an insufficient current-limiting circuit, or
  - permanent damage caused by overvoltage stress.

- Optical alignment was challenging because the IR beam is invisible.
- Therefore, a visible red laser (650 nm) was used for subsequent testing and alignment verification.
- Since the current–power curve of the red laser was not provided in the datasheet, its optical power was experimentally estimated.
- The forward voltage and current were measured using a multimeter and clamp meter, respectively, and the drive current was adjusted to stay within the Class 1M Accessible Emission Limit (AEL).
- At a measured forward voltage of 1.9 V and current of 19 mA, the optical output power was approximately 0.36 mW, confirming compliance with Class 1M safety requirements.

### *9.3.6 Technical Test T004.1 Power and operation time - MCU Circuit Reliability and performance*

| | | |
|---|---|---|
| **Test No:** T004.1 | Date: | 11/09/2025 |
| | Location: | UWA Makers Lab |

**Test Title:** Power and operation time - MCU Circuit Reliability and performance

**Test Objective**

Verify the MCU Continuity/Shorts DMM resistance between each rail and GND (e.g., 3V3–GND, 5V–GND); check key nets (USB D+/D− not shorted; SWD/JTAG pins not shorted).

Verify that the MCU circuit soft-starts Bench PSU at nominal VIN with 20–50% current limit above expected idle.
Verify the regulator connection by Measuring all rails (e.g., 3V3, 1V8, VUSB); ripple via scope under idle and light load.
Verify the Power/Reset by probe RESET/EN and PGOOD/PG lines during power-up.

Covering requirements: **PWR-1, PWR-2, PWR-3**

**Test Environment**

**Location:** Electronics Lab / Makerspace bench with ESD protection (ESD mat, wrist strap, grounded workbench).
**Power Supply:** Bench DC power supply with adjustable voltage/current (set to nominal VIN, current limit 20–50% above expected idle).

**Measurement Tools:**
Digital Multimeter (DMM) for continuity, resistance, and rail voltage checks.
Oscilloscope (≥100 MHz, 2+ channels) with 10× probes for ripple and reset/PGOOD timing measurements.

**Support Equipment:**
Logic analyzer or USB-to-SWD/JTAG programmer (optional, for reset pin activity).
Known-good USB cable (for VUSB rail testing if present).

**Test Board Setup:**
MCU PCB under test placed on ESD-safe surface.
Test points, headers, or exposed pads accessible for DMM and oscilloscope probes.

**Ambient Conditions:**
Room temperature ~22 ± 5 °C.
Stable mains power supply to equipment.

**Test Cases**

T004 includes:

1) Fully charge battery
2) Run workload (HID + intermittent file copy)
3) Time until shutdown
4) For host module, run workload on host USB power only

Included in T004.1:

5) MCU circuit performance and reliability
6) reset button function
7) Power Step down

**Acceptance Criteria**

T004:

Battery module ≥2 h continuous operation and host module fully functional from host port only

**Included in T004.1:**

1. No hard shorts; power rails, USB lines, and SWD/JTAG pins show >10 Ω after capacitor charging.
2. On power-up, current draw stays within ±20% of expected and no smoke, latch-up, or overheating occurs.
3. All regulator rails measure within spec with ripple ≤50 mVpp.
4. Reset/PGOOD assert and release cleanly, and the MCU enters a known boot state.

**Reporting**

During initial testing, capacitor C9, which is connected to the voltage regulator, was found to have burned out. Upon investigation, it was determined that the polarized capacitors C8 and C9 had been installed with reversed polarity, resulting in a short circuit within the regulator circuit.

The issue was resolved by desoldering both capacitors, correcting their orientation, and resoldering them in the proper polarity. After this fix, the circuit operated as expected.

After fixing the issue, the PCB was left powered by a voltage generator with 4.5V input for about 20 min. The PCB did not show any signs of warming up or failures.

### *9.3.7 Technical Test T004.2 Power and operation time - MCU Circuit Reliability and performance*

| | | |
|---|---|---|
| **Test No:** T004.2 | Date: | 11/09/2025 |
| | Location: | Makers Lab |

**Test Title:** Power and operation time - MCU Circuit Reliability and performance

**Test Objective**

The objective of this test is to validate the proper operation of the custom ESP32-S3 board by:

1. Verifying the correct installation and functionality of power regulation components.
2. Ensuring stable power delivery through proper capacitor polarity and regulator performance.
3. Confirming reliable communication between the board and a host computer by establishing and testing data connectivity via a modified cable.

Covering requirements: **PWR-1, PWR-2, PWR-3**

**Test Environment**

**Location:** Electronics Lab / Makerspace bench with ESD protection (ESD mat, wrist strap, grounded workbench).
**Power Supply:** Bench DC power supply with adjustable voltage/current (set to nominal VIN, current limit 20–50% above expected idle).

**Hardware:** Custom-built ESP32-S3 development board with onboard voltage regulator and communication interfaces.
**Power Supply:** USB connection (5 V input) via modified cable; onboard voltage regulator providing 3.3 V output.
**Peripherals:** Polarized capacitors (C8, C9) connected to the regulator circuit; standard headers for connectivity.
**Computer/Host System:** PC running Windows/Linux with USB support for flashing and serial communication.
**Software Tools:**

- esptool.py for flashing firmware
- Arduino IDE / ESP-IDF for development and verification
- Serial monitor for communication testing
- Test Instruments: Multimeter (for voltage verification), continuity tester (for connectivity), and oscilloscope (optional, for signal integrity checks).

**Ambient Conditions:**
Room temperature ~22 ± 5 °C.
Stable mains power supply to equipment.

**Test Cases**

T004 includes:
1) Fully charge battery
2) Run workload (HID + intermittent file copy)
3) Time until shutdown
4) For host module, run workload on host USB power only

Included in T004.2:

4) For host module, run workload on host USB power only
5) MCU circuit performance and reliability
6) reset button function

**Acceptance Criteria**

T004:

Battery module ≥2 h continuous operation and host module fully functional from host port only

**Included in T004.2:**

1. Connectivity
   - The board must establish successful communication with the host computer via the USB connection.
   - The modified cable must provide reliable power and data transfer.
   - Serial communication should be detected on the host (COM port / device node visible).
2. Functional Verification
   - The ESP32-S3 must enter programming mode and accept firmware flashing without errors.
   - After flashing, the board must boot successfully and respond to serial commands.

**Reporting**

| Cable created by connecting two USB-A to USB-A end communication cable, both power and communication was successful. |
| --- |

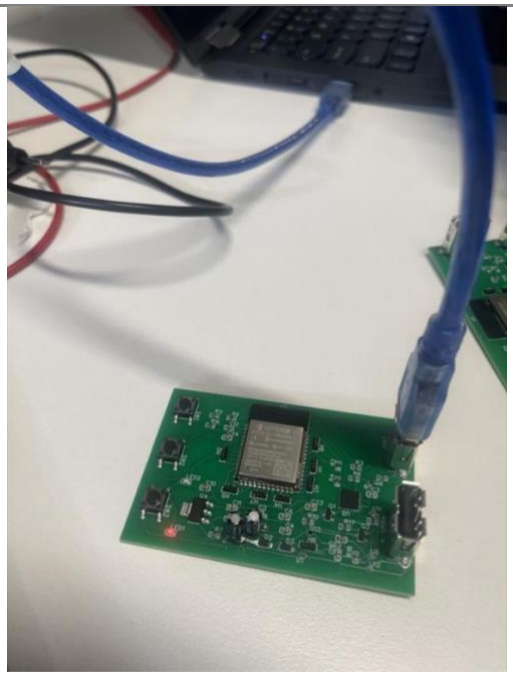


*Figure 45:MCU booting was tested and was successful*

.

*Figure 46:MCU booting was tested and was successful*

### *9.3.8 Technical Test T004.3 Power Endurance Test*

| **Test No:** T004.3 | Date: | 02/10/2025 |
| --- | --- | --- |
| | Location: | Makers Lab |

**Test Title:** Power Endurance Test

**Test Objective**

This test validates the ability of the Free Space Optical (FSO) system to operate continuously for 2 hours when powered solely by a portable power bank. HID functionality was passively monitored during the session to confirm that the system remained responsive and stable.

Covering requirements: PWR-3

**Test Environment**

Test involves using the Prototypes Transmitter and receiver circuit:

- Hardware:
  - FSOCS transmitter module
  - FSOCS receiver module
  - PC host for serial monitoring
  - Mouse and Keyboard HID Peripherals
  - Portable Power Bank
- Software/Tools:
  - ESP-IDF framework for firmware development
  - Serial monitor for output monitoring
- Conditions:
  - Indoor lab setting with controlled artificial lighting (~22 ± 5 °C)
  - Stable laser-photoreceiver alignment
  - Power bank connected to both transmitter and HID peripheral

**Test Cases**

1. Connect transmitter and HID peripheral to power bank.
2. Begin normal HID operation and monitor receiver output.
3. Maintain continuous power for 2 hours without interruption.
4. Observe system behavior and HID responsiveness passively.

**Acceptance Criteria**

1. System remains powered and operational for full 2-hour duration.
2. No power-related interruptions observed.
3. HID events continue to be received and emulated without degradation.

**Reporting**

1. FSOCS transmitter and HID peripheral were powered continuously from a portable power bank for 2 hours.
2. No system resets, dropouts, or instability were observed.
3. HID functionality remained responsive and stable throughout the session.

### *9.3.9 Technical Test T005.1 Auto Peripheral Detection and Data Rate Transfer – with wire*

| | | |
|---|---|---|
| **Test No:** T005.1 | Date: | 08/09/2025 |
| | Location: | UWA Makers Lab |

**Test Title:** Auto Peripheral Detection and Data Rate Transfer – with wire

**Test Objective**

Test automatic device type detection and Verify data rate supports mouse/keyboard/USB stick

Covering requirements: FR-4, FR-3, PR-2, PR-3

**Test Environment**

Hardware:
- ESP32-based test platform configured for USB host functionality
- USB mouse, USB keyboard, USB flash drive (≥ 100 MB capacity)
- Standard USB cables/adapters for connection
- Multimeter/oscilloscope (optional) for power and signal verification

Software / Firmware:
- ESP-IDF (with TinyUSB host stack enabled)
- Firmware supporting automatic USB device class detection (HID, MSC)
- Logging enabled via UART console for debug and event capture

Support Equipment:
- Laptop/PC for monitoring UART logs and performance data
- Stopwatch or software timer for latency and throughput measurement
- Stable 5 V power supply to ensure VBUS is within USB specification

Test Data:
- 40 MB test file stored on the USB stick for transfer validation

**Test Cases**

T005: Connect different devices, observe behaviour and transfer test and latency check.

1) Plug mouse, keyboard and stick
2) Operate mouse, keyboard
3) Transfer 100 MB file from stick

**Included in T005.1:**
3) Transfer 100 MB file from stick

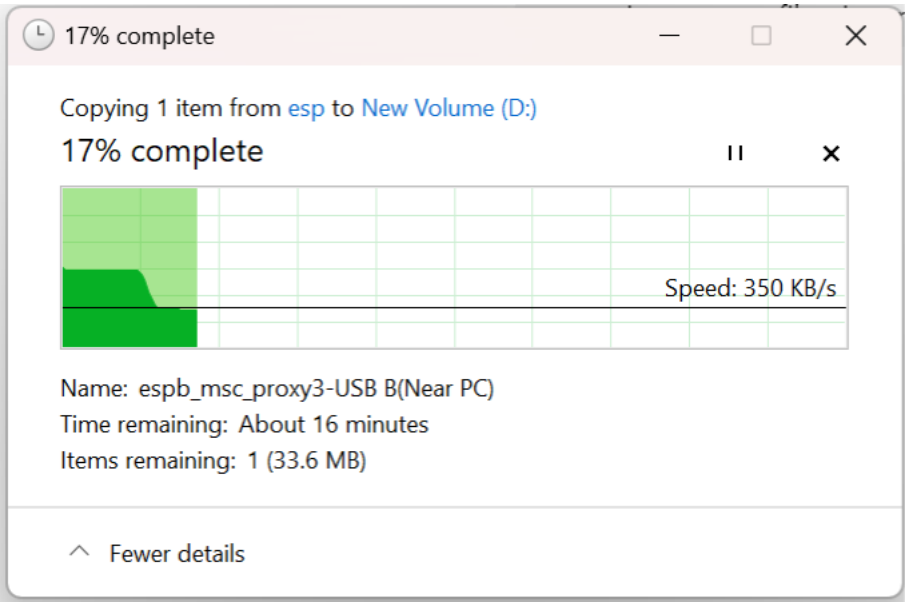
**Acceptance Criteria**

**T005.1:**
1) System correctly identifies and configures without manual switching
2) All operate smoothly; file transfer completes within expected time

3) Operates with one device; rejects multiple

**Reporting**

Data transfer takes 40Mbs message received “16min” time to copy zip file into the flash took 20min.



### *9.3.10 Technical Test T005.2 Data Transfer Rate Test over FSO Link*

| **Test No:** T005.2 | Date: | 15/09/2025 |
| --- | --- | --- |
| | Location: | Makers Lab |

**Test Title:** Data Transfer Rate Test over FSO Link

**Test Objective**

This test validates ability of FSO system to reliably transmit structured messages at a high baud rate of 230400 bps using UART-style signalling. The transmitter sends a predefined message "Yuki" optically, and the receiver verifies message integrity using a success/error counter. The goal is to confirm that the system supports higher speed data transfer than 100 kHz with minimal errors under stable alignment.

Covering requirements: FR-4, FR-3

**Test Environment**

Test involves using the Prototypes Transmitter and receiver circuit:

- Hardware:
  - FSOCS transmitter module
  - FSOCS receiver module
  - PC host for serial monitoring
- Software/Tools:
  - ESP-IDF framework for firmware development
  - Arduino framework with ESP-IDF backend
  - Custom receiver code with success/error counters
  - Serial monitor for output monitoring
- Measurement Equipment:
  - Tape measure / iOS measure App for transmission distance
  - Serial monitor for display and verification
- Conditions:
  - Indoor lab setting with controlled artificial lighting (~22 ± 5 °C)
  - Stable laser-photoreceiver alignment
  - Optical UART protocol at 230400 baud

**Test Cases**

1. Program transmitter to send "Yuki" message optically at 230400 baud.
2. Program receiver to validate incoming messages
3. Compare received message against expected message.
4. Increment success or error counters accordingly.
5. Monitor serial output for baud rate and output.

## Acceptance Criteria

**T005.2:**

1. Receiver accurately reconstructs transmitted message.
2. Success count increases consistently under stable conditions.
3. Error count remains minimal or zero.
4. Communication remains stable at 230400 bps.
5. No framing errors or corrupted messages under proper alignment

## Reporting

1. Transmitter sent the message "Yuki" optically at 230400 bps.
2. Receiver validated message integrity using a success/error counter.
3. Under proper alignment, the message was consistently received.
4. Success rate remained high, confirming reliable high-speed transmission.
5. The system displayed “ERROR!” messages on the serial monitor when misalignment occurred.

### *9.3.11 Technical Test T005.3 HID Hot Swapping Validation*

| | | |
|---|---|---|
| **Test No:** T005.3 | Date: | 02/10/2025 |
| | Location: | Makers Lab |

**Test Title:** HID Hot Swapping Validation

**Test Objective**

Test T005.3 verifies the ability of the FSO system to swap the HID peripherals mid-operation and identify the change and continue operation without having for a system reboot or significant delay

Covering requirements: FR-4, FR-3

**Test Environment**

Test involves using the Prototypes Transmitter and receiver circuit:

- Hardware:
  - FSOCS transmitter module
  - FSOCS receiver module
  - PC host for serial monitoring
- Software/Tools:
  - ESP-IDF framework for firmware development
  - Serial monitor for output monitoring
- Conditions:
  - Indoor lab setting with controlled artificial lighting (~22 ± 5 °C)
  - Stable laser-photoreceiver alignment
  - Optical UART protocol at 9600 baud
  - HID keyboard disconnected and mouse connected mid-sessio

**Test Cases**

1. Connect HID keyboard to transmitter module and begin transmitting keystrokes
2. Disconnect keyboard and connect HID mouse during active FSO session.
3. Observe receiver output for continuity and decoding accuracy.
4. Monitor for framing errors

**Acceptance Criteria**

**T005.3:**

1. Receiver accurately decodes HID packets before and after hot-swap.
2. HID output resumes without requiring system reboot.
3. No persistent framing errors or decoding failures.
4. Session integrity is maintained across peripheral reconnection.

**Reporting**

1. HID peripherals were successfully swapped mid-operation without requiring a system reboot.
2. Upon disconnection of the keyboard and connection of the mouse, the receiver resumed decoding seamlessly.
3. No framing errors were observed during the transition.
4. The system maintained session continuity and HID responsiveness throughout the swap.

### *9.3.12 Technical Test T006.1 FSO HID Transmission Distance Validation*

| **Test No:** T006.1 | Date: | 04/10/2025 |
| --- | --- | --- |
| | Location: | Makers Lab |

**Test Title:** FSO HID Transmission Distance Validation

**Test Objective**

The objective of this test is to determine the maximum reliable transmission distance of the custom-designed Free Space Optical (FSO) system (FR-07) while emulating HID peripherals (mouse and keyboard) from the transmitter end to the receiver end (FR-03, FR-04). The test also validates portable operation using external power sources. Latency performance was also observed to confirm responsiveness below 50 ms (PR-2, PR-3).

Covering Requirements: FR-03, FR-04, FR-07, PWR-2, PR-2, PR-3

**Test Environment**

Test involves using the Prototypes Transmitter and receiver circuit:

- Hardware:
  - FSOCS transmitter module
  - HID peripherals (mouse and keyboard)
  - FSOCS receiver module
  - PC for HID response tracking
  - Power bank supplying transmitter module and peripherals
- Software/Tools:
  - ESP-IDF framework for transmitter and receiver programming
- Measurement Equipment:
  - Tape measure for distance validation
  - Serial monitor for latency tracking
- Conditions:
  - Indoor lab setting with controlled artificial lighting (~22 ± 5 °C)
  - No obstructions between transmitter and receiver modules

**Test Cases**

T006.1 includes:

1. Connect mouse and keyboard to transmitter module powered via power bank
2. Program transmitter to send HID events via laser modulation
3. Program receiver to emulate HID input and reflect actions on display.
4. Gradually increase distance between modules to identify maximum reliable transmission.
5. Measure final working distance using tape
6. Record HID responsiveness and any signal degradation.

**Acceptance Criteria**

- HID events (mouse movement, clicks, keystrokes) are accurately received and emulated.
- System maintains reliable communication up to maximum distance .
- Latency remains below 50 ms during HID operation.
- No missed or corrupted HID events during stress test.

**Reporting**

- HID peripherals successfully controlled receiver display from transmitter end.
- Maximum reliable transmission distance recorded at 4.6 meters, measured using tape.
- ESP-IDF used for firmware development and testing.
- Transmitter module and peripherals were powered using a power bank
- System required precise laser alignment to maintain link; misalignment caused signal loss and noise.
- End-to-end HID responsiveness remained below 50 ms, meeting latency performance expectations.
- Test confirms long-range viability of HID over FSO with portable powering

### *9.3.13 Technical Test T007.1 Link Interruption Recovery Test*

| **Test No:** T007.1 | Date: | 04/10/2025 |
| --- | --- | --- |
| | Location: | Makers Lab |

**Test Title:** Link Interruption Recovery Test

**Test Objective**

This test validates the ability of the Free Space Optical (FSO) system to recover from a temporary link interruption during HID peripheral operation. The system was tested using a keyboard connected to the transmitter module which was the HID peripheral of choice for test validation, with emulated output displayed on the receiver-side PC. The goal was to confirm that the system maintains session integrity and resumes communication without manual intervention or reboot after the optical path is blocked and restored.

Covering Requirements: FR-6, FR-3

**Test Environment**

Test involves using the Prototypes Transmitter and receiver circuit:

- Hardware:
  - FSOCS transmitter module
  - HID peripheral (keyboard)
  - FSOCS receiver module
  - PC for HID response tracking
  - Opaque surface used to interrupt optical path
- Software/Tools:
  - ESP-IDF framework for transmitter and receiver programming
  - Serial Monitor to track HID events
- Conditions:
  - Indoor lab setting with controlled artificial lighting (~22 ± 5 °C

**Test Cases**

T007.1 includes:

1. Connect keyboard to transmitter module
2. Program transmitter to send keyboard characters via laser modulation
3. Program receiver to emulate HID input and reflect actions on display.
4. Block laser path using opaque surface for 5 –10 seconds
5. Continue typing to monitor changes at the receiver display
6. Remove obstruction and observe reinstated emulation

**Acceptance Criteria**

- Keystrokes are accurately received and emulated.
- HID output stops immediately upon link interruption.
- System remains powered and stable during interruption.
- Communication resumes from the point of interruption after obstruction is removed.
- HID output resumes without manual reset or system reboot.

**Reporting**

- HID peripheral (Keyboard) successfully emulated on receiver display .
- Upon blocking the laser path, HID output ceased immediately.
- System remained powered and stable during the interruption.
- Once the obstruction was removed, communication resumed automatically.
- HID output continued from the point of interruption.
- No system reboot was required.

## 9.4 Appendix D: Final Bill of Materials

*Table 19: Final Bill of Materials*

| Item | Material | Date of Purchase | Qty. | Unit Price | Total Price | Ref Receipt |
|---|---|---|---|---|---|---|
| 1 | AliExpress - Adjustable Mini Laser Pointer Diode RED | 8/02/2025 | 1 | $4.61 | $4.61 | ALEX0001 |
| 2 | AliExpress - IR infrared Transmitter | 8/02/2025 | 4 | $1.77 | $7.08 | ALEX0002 |
| 3 | AliExpress - Push Potentiometer | 8/02/2025 | 1 | $7.31 | $7.31 | ALEX0003 |
| 4 | AliExpress - Trimmer Potentiometer | 8/02/2025 | 1 | $8.03 | $8.03 | ALEX0004 |
| 5 | JayCar - LED IR RK Photoresistor 5mm CLR | 31/7/2025 | 2 | $1.75 | $3.50 | JAYC0001 |
| 6 | JayCar - Filament PLA Black 1.75mm 1kg Roll | 31/7/2025 | 1 | $9.95 | $9.95 | JAYC0001 |
| 7 | JayCar - 2N7000 N-Channel MOSFET T092 | 8/07/2025 | 5 | $0.75 | $3.75 | JAYC0002 |
| 8 | JayCar - BP104 Photodiode | 18/8/2025 | 5 | $3.45 | $17.25 | JAYC0003 |
| 9 | JayCar - NE5534NP Lo-Noise High Speed Op Amp | 18/8/2025 | 2 | $3.95 | $7.90 | JAYC0004 |
| 10 | DigiKey - Sensor Photodiode 900nm 2DIP | 27/8/2025 | 10 | $1.38 | $13.80 | DIGI0001 |
| 11 | DigiKey - IC Op Amp GP 2 Circuit 8SOIC | 27/8/2025 | 10 | $0.65 | $6.50 | DIGI0001 |
| 12 | DigiKey - IC Op Amp GP 2 Circuit 8DIP | 27/8/2025 | 10 | $0.70 | $7.00 | DIGI0001 |
| 13 | DigiKey - IC Op Amp VFB 1 Circuit SOT23-5 | 27/8/2025 | 10 | $2.82 | $28.18 | DIGI0001 |
| 14 | DigiKey - Ferrite Bead 600 Ohm 0805 1LN | 27/8/2025 | 10 | $0.12 | $1.16 | DIGI0001 |
| 15 | DigiKey - CAP CER 0.1 uF 50 V X7R 0805 | 27/8/2025 | 10 | $0.03 | $0.30 | DIGI0001 |
| 16 | DigiKey - MOSFET T0-92 60 V 0.2 A | 27/8/2025 | 10 | $0.22 | $2.24 | DIGI0001 |
| 17 | DigiKey - Conn Header Vert 5POS 2.54 mm | 27/8/2025 | 10 | $0.27 | $2.71 | DIGI0001 |
| 18 | Digikey - Laser Diode 850 NM 1.5 MW T046 | 31/8/2025 | 3 | $24.93 | $74.79 | DIGI0002 |
| 19 | JLCPCB - Receiver and Transmitter PCB | 24/09/2025 | 1 | $87.38 | $87.38 | JLCP0001 |
| 20 | JLCPBC - MCU Circuit PCB | 4/09/2025 | 1 | $161.26 | $161.26 | JLCP0002 |
| 21 | Altronics - H/Shrink Red 1.5mm 2m | 13/10/2025 | 1 | $1.75 | $1.75 | ALTR0001 |
| 22 | Altronics - Laser Diode Module <1 MW | 13/10/2025 | 1 | $4.65 | $4.65 | ALTR0001 |
| 23 | Altronics - Laser Diode Module <1 MW | 13/10/2025 | 1 | $4.65 | $4.65 | ALTR0002 |
| | | | | **TOTAL** | **$465.75** | |

## 9.5 Appendix E: Validation and Verification Table

All the files related to the project updated to this GitHub link- https://github.com/luipulaus02-dev/UWA-Design-Unit-Team-14-2025

*Table 20: Validation and Verification Table*

| ID | Requirement description | Test | Passed | Learnings |
|---|---|---|---|---|
| DC-1 | The project team shall remain within a hard budget limit of $500 AUD for all prototyping activities. | N/A | Yes | Overall expenditure for the design project comes to less than $500 |
| DC-2 | All project deliverables shall be submitted via a shared Git repository. | N/A | Yes | Project deliverables were imported into a GitHub repository |
| DC-3 | All project deliverables shall be licensed under the CERN-OHL-P open-source license. | N/A | Yes | Project deliverables are downloadable and editable on the GitHub repository |
| DC-4 | The team shall return all physical components purchased for the project to the university upon completion. | N/A | Yes | Components purchased are returned after the demonstration |
| DC-5 | The team shall submit only a single, consolidated reimbursement claim for all project expenses. | N/A | Yes | Single submission including invoices and bill of materials has been submitted |
| FR-01 | The system shall provide bidirectional data communication over a free-space optical link. | T002: Verify system can send and receive data over FSO link which is 2m long | Yes | Bidirectional link verified at 2 m; baseline established for range upsizing. |
| FR-02 | The system shall feature a standard USB (Type-A) interface on each module. | T001: Confirm each module has a functional I/O USB interface | Yes | System can perform and access USB enabled HID or MSC devices. |
| FR-03 | The system shall support the operation of a single standard USB peripheral (keyboard, mouse, or data stick) at a time. | T005: Test automatic device type detection and Verify data rate supports mouse/keyboard/USB stick | Yes | System has hot swapping capability with automatic detection of the devices. |
| FR-04 | The system shall automatically detect the type of peripheral connected without requiring manual user switching. | T005: Test automatic device type detection and Verify data rate supports mouse/keyboard/USB stick | Yes | System has automatic detection of the devices without changing or selecting any on the system. |

| | | | | |
|---|---|---|---|---|
| FR-05 | Each module shall be designed to mitigate interference from its own reflected laser light. | T002: Verify system can send and receive data over FSO link which is 2m long | Yes | Self-reflection mitigation adequate at 2 m, maintain mechanical barrier. |
| FR-06 | The system shall automatically recover and re-establish the communication link after a temporary interruption | T007: It validates that the system can rectify the issue of a broken connection by re-establishing the USB session without requiring manual user intervention. | Yes | Link self-recovery worked; resume times consistently below target. |
| FR-07 | The system shall use a custom-designed laser diode driver. | T003: Confirm Class 1M safety compliance; verify custom laser driver with adjustable current clamp limiting output. | Yes | Adjustable clamp eased safety tuning and made the operation safe at class 1M. |
| FR-08 | The system shall implement a CRC-based error detection scheme on all transmitted data packets. | T002: Verify system can send and receive data over FSO link which is 2m long | Yes | No error detected over 2m communication link meaning, the CRC works fine. |
| FR-09 | The system shall enter a safe state (e.g., laser off) if the MCU firmware detects a critical fault. | N/A | Yes | Fault-safe laser-off there through hardware layer. A 10k ohm pulldown resister makes sure of this. |
| FR-10 | The system shall re-establish a communication link within 5 seconds of the optical path being restored after an interruption. | T007: It validates that the system can rectify the issue of a broken connection by re-establishing the USB session without requiring manual user intervention. | Yes | System can do a continues operation even with smaller interruptions. |
| FR-11 | The laser driver shall incorporate a user-adjustable current clamp. | T003: Confirm Class 1M safety compliance; verify custom laser driver with adjustable current clamp limiting output. | Yes | User can decide the power of the laser. Based on the application and environment, can achieve higher distances. |
| FR-12 | The final design shall be implemented on a custom-designed Printed Circuit Board (PCB). | N/A | Yes | All circuits were made and assembled on a custom PCB |
| PHY-1 | The chassis shall meet an Ingress Protection rating of at least IP51. | N/A | No | USB Port placement makes chassis vulnerable to vertical rainfall |

| | | | | |
|---|---|---|---|---|
| PHY-2 | The chassis shall fully enclose all internal electronic components. | N/A | Yes | All PCBs and components are stored inside the chassis |
| PHY-3 | The chassis shall be constructed from a non-conductive material (3D-printed PLA or ABS). | N/A | Yes | Chassis is made using PLA filament, which is electrically insulative |
| PHY-4 | The chassis shall provide stable, rigid mounting for the optical components to maintain alignment during normal handling. | N/A | Yes | All PCBs are mounted on the inside of the chassis and secured through slits that allows the PCB to be slotted and fitted into the chassis. |
| PHY-5 | All external ports on the chassis shall be clearly labelled. | N/A | Yes | Stickers labelled onto the chassis |
| PHY-6 | The system shall provide visual status indicators on each module for Power, Link Status, and Data Activity. | N/A | No | Visual status indicators on PCBs are not visible when chassis is enclosed |
| PR-1 | The system shall operate over a free-space distance of 2 meters with a Bit Error Rate (BER) of less than $10^{-9}$. | T002: Verify system can send and receive data over FSO link which is 2m long | Yes | System meets requirement of bidirectional communication over 2m distance. |
| PR-2 | The system shall support a data transfer rate equivalent to USB 2.0 Full-Speed (12 Mbps). | T005: Test automatic device type detection and Verify data rate supports mouse/keyboard/USB stick<br><br>T006: Oscilloscope measurements confirm end-to-end latency for HID operations is less than 50 ms | No | 12 Mbps not met; simplify framing and improve clock/analogy bandwidth. |
| PR-3 | The system shall exhibit a latency less than 50 ms for mouse and keyboard operations to allow for comfortable use of standard office peripherals. | T001: Confirm each module has a functional I/O USB interface<br>T005: Test automatic device type detection and Verify data rate supports mouse/keyboard/USB stick<br>T006: Oscilloscope measurements confirm | Yes | HID latency <50 ms achieved and naked eye cannot identify a slowness over HID devices |

| | | | | |
|---|---|---|---|---|
| | | end-to-end latency for HID operations is less than 50 ms | | |
| PR-4 | The system shall complete its power-on self-test and be ready for operation within 10 seconds of being powered on. | T001: Confirm each module has a functional I/O USB interface | Yes | System boots in less than 10s and devices are already for the operation immediate after powering |
| PR-5 | The system shall implement an Automatic Repeat Request (ARQ) protocol to re-transmit corrupted or lost data packets. | T001: Confirm each module has a functional I/O USB interface | | ARQ unverified; add lightweight retry (e.g., seq/ACK) and test. |
| PR-6 | The system shall maintain all performance requirements (including BER and latency) when operating under ambient indoor laboratory lighting conditions-up to 1000 lux. | T002: Verify system can send and receive data over FSO link which is 2m long | Yes | System perform accurately under laboratory conditions. |
| PR-7 | The system should operate reliably within an ambient laboratory temperature range of 15° C to 30°C. | T002: Verify system can send and receive data over FSO link which is 2m long | Yes | Operated reliably at 15–30 °C range |
| PWR-1 | The host-side module shall be powered entirely from the host's USB port. | T004: Verify battery-powered module operation from USB power bank for at least 2 h and host-side module operation solely from host USB port | Yes | Host module powered from USB reliably, no device resetting or voltage error detected. |
| PWR-2 | The peripheral-side module shall be powered by a standard commercial USB and power bank. | T004: Verify battery-powered module operation from USB power bank for at least 2 h and host-side module operation solely from host USB port | Yes | Power-bank strategy viable; add brown-out recovery procedure. |

| | | | | |
|---|---|---|---|---|
| PWR-3 | The battery-powered module shall operate continuously for a minimum of 2 hours on a full charge. | T004: Verify battery-powered module operation from USB power bank for at least 2 h and host-side module operation solely from host USB port | Yes | ≥2 h runtime confirmed; implement low-battery indication. |
| SR-1 | The system shall adhere to the Class 1M eye-safety standard as defined in AS/NSS IEC 60825.1:2022. | T003: Confirm Class 1M safety compliance; verify custom laser driver with adjustable current clamp limiting output. | Yes | Class 1M pathway established; maintain calibration and test records. |

## 9.6 Appendix F: 850nm Laser Diode Class 1M Calculations

According to the standard, the Class 1M allowable average optical power over 10 seconds at 850 nm is approximately 0.78 mW.

The maximum current is calculated using the laser diodes Light-Current (L-I) curve from its datasheet [1]. To ensure a reliable safety margin, a design target current of 4 mA was chosen. The calculation process is as follows:

**Class 1M Accessible Emission Limit (AEL) at 850 nm**

From IEC 60825-1 (Table 3 and Table 9, $700 \leq \lambda \leq 1050\ nm$):

$$AEL = 3.9 \times 10^{-4} C_4 C_7 \text{ W}, C_4 = 10^{0.002(\lambda - 700)}, C_7 = 1$$

At $\lambda = 850\ nm$:

$$AEL = 3.9 \times 10^{-4} \times 10^{0.002(150)} = 0.78 \text{ mW}$$

*Target Current (OPV300 VCSEL)*

From datasheet (25 °C):

- $I_{th} = 2.2$ mA
- $P_{ref} = 1.50$ mW@ $I_{ref} = 7$ mA
- Linear region slope $\approx 0.28 - 0.60\ mW/mA$

$$I_{clamp} = I_{th} + (I_{ref} - I_{th}) \times \frac{AEL}{P_{ref}}$$

$$I_{clamp} = 2.2 + (7 - 2.2) \times \frac{0.78}{1.50} = 4.70 \text{ mA}$$

To provide a 15% safety margin:

$$I_{op} = 0.85 \times I_{clamp} = 3.99 \text{ mA} \approx 4 \text{ mA}$$

Sense-Resistor and Clamp Voltage

For current clamp feedback $V_{ref} = I_{op} \times R_{sense}$, thus

$$R_{sense} = 10\Omega \rightarrow V_{ref} \approx 39.9 \text{ mV}$$

To account for the possibility that the 850 nm laser may not operate correctly, the Class 1M AEL for the 650 nm laser was also calculated.

## 9.7 Appendix G: Transmitter Module Simulations and Prototype

This appendix contains examples of some simulation iterations.

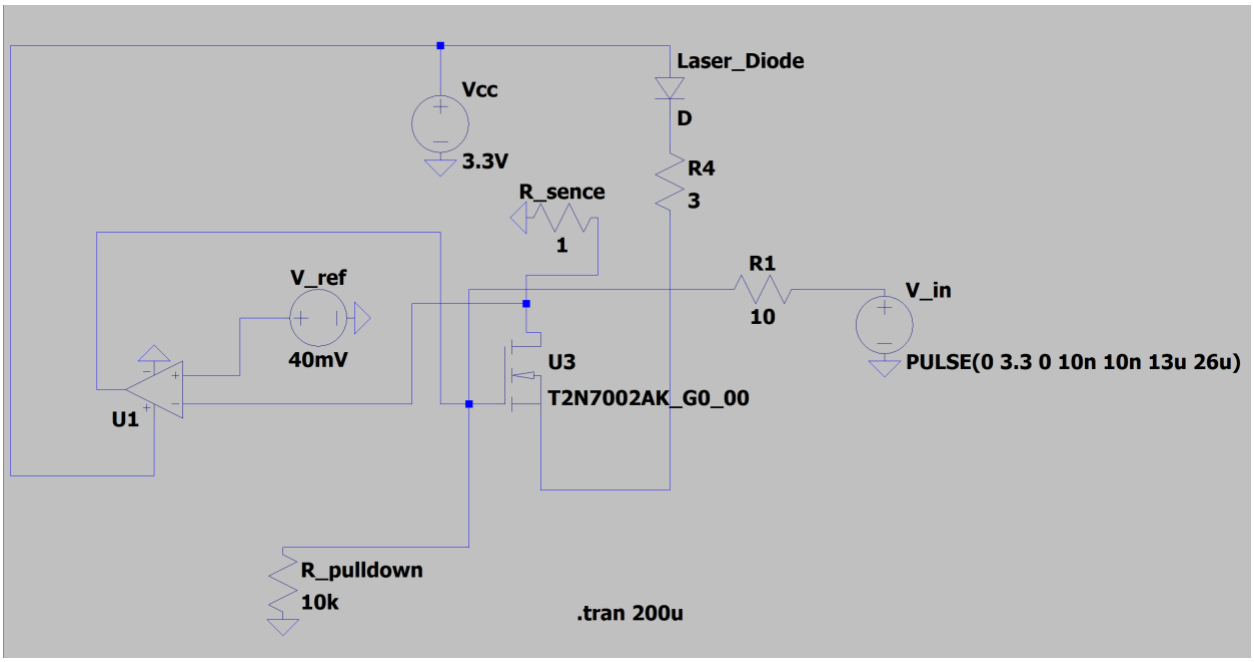



*Figure 47: Laser Diode Alternative Design*

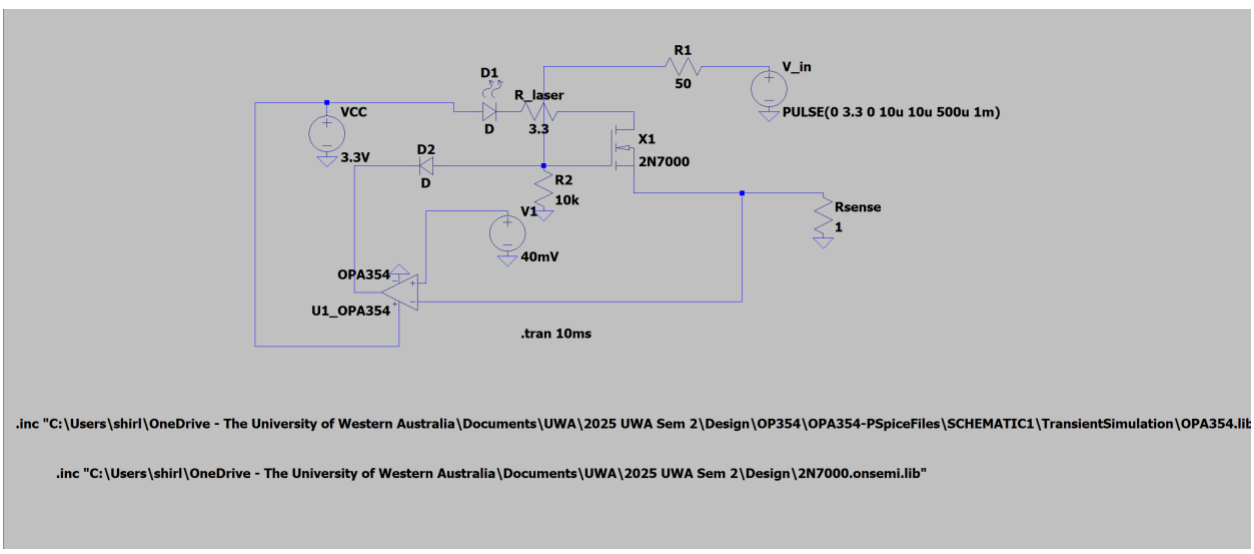



*Figure 48: Laser Diode Driver Final Design*

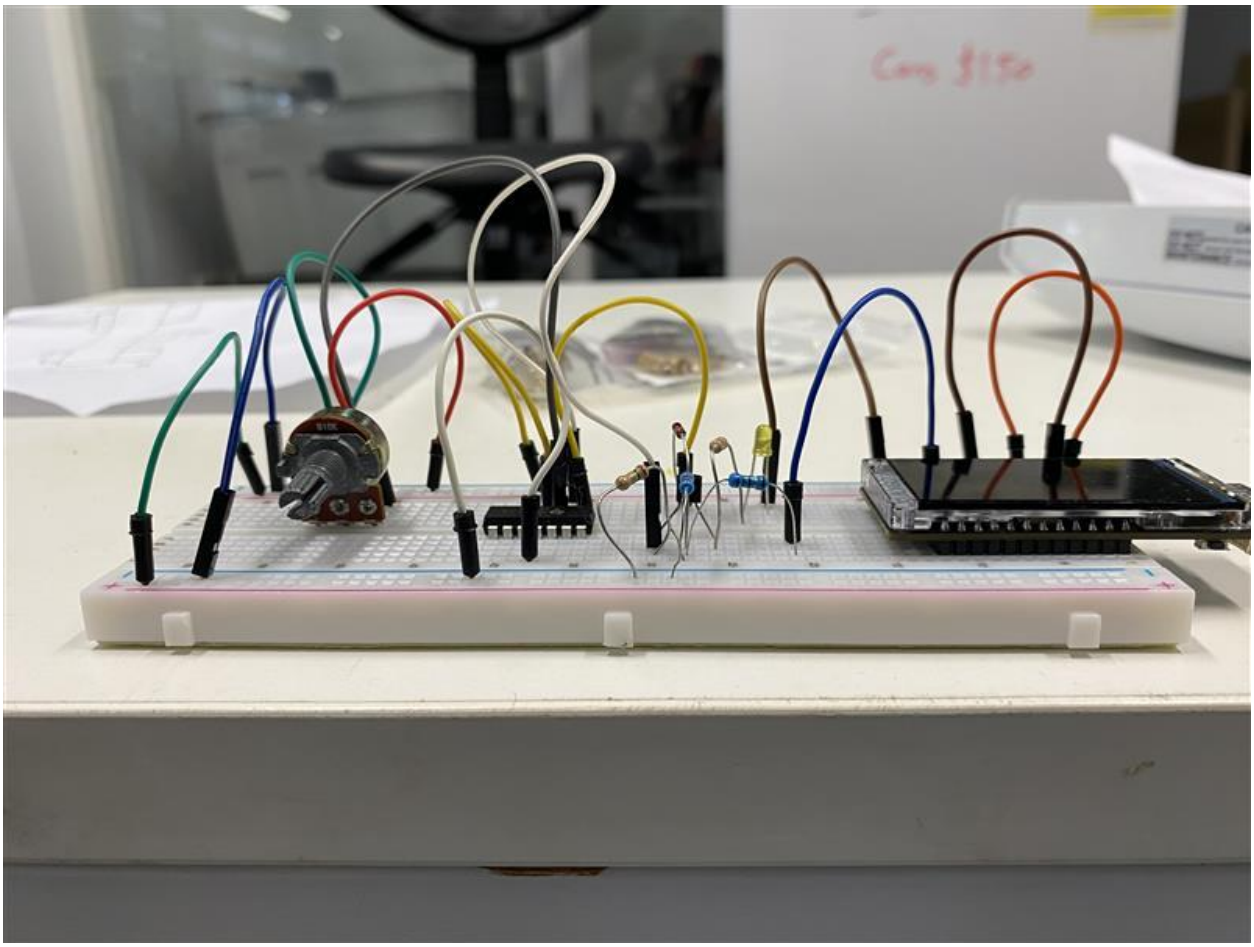


*Figure 49: Transmitter Module Prototype*

## 9.8 Appendix H: Receiver Module Simulations and Prototype

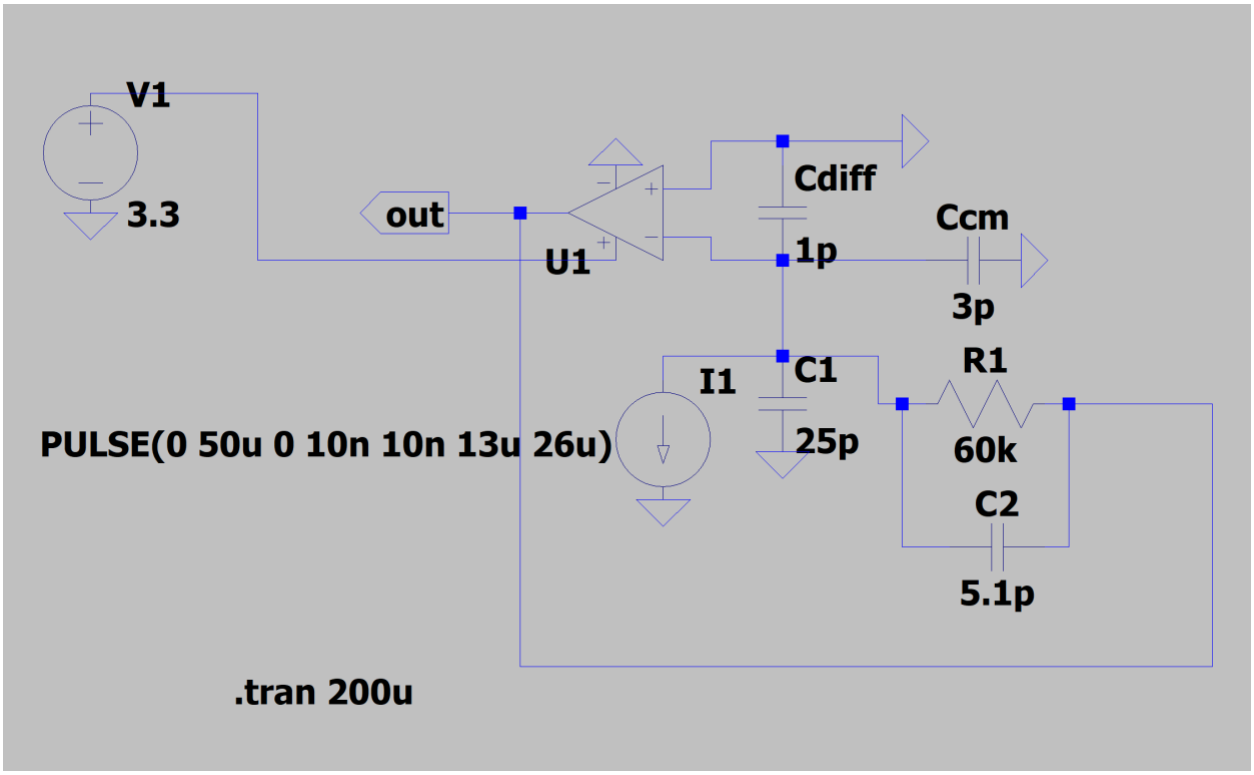



*Figure 50: Receiver Module Design 1*

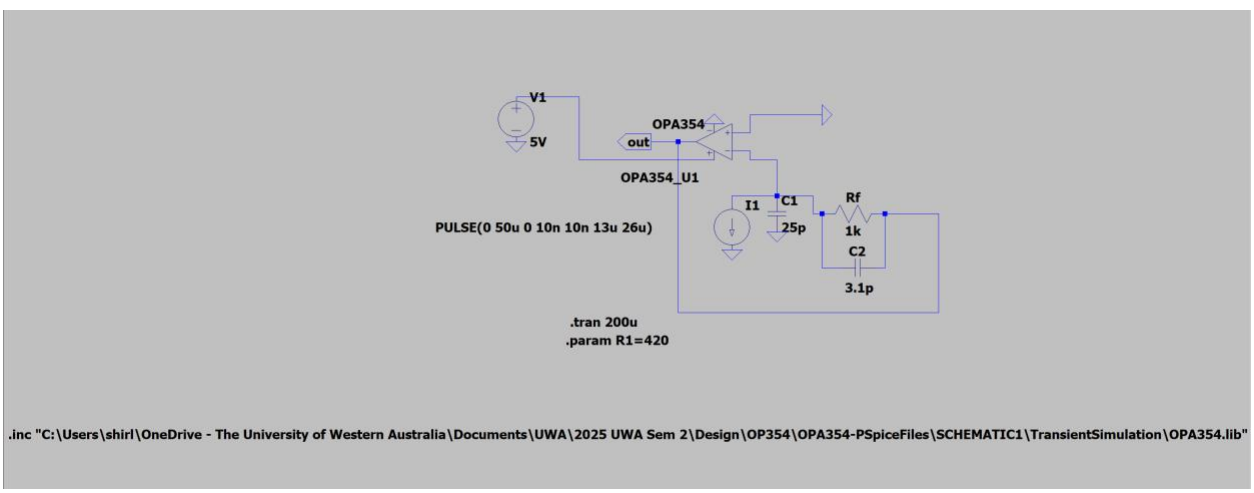



*Figure 51: Receiver Circuit Design 2*

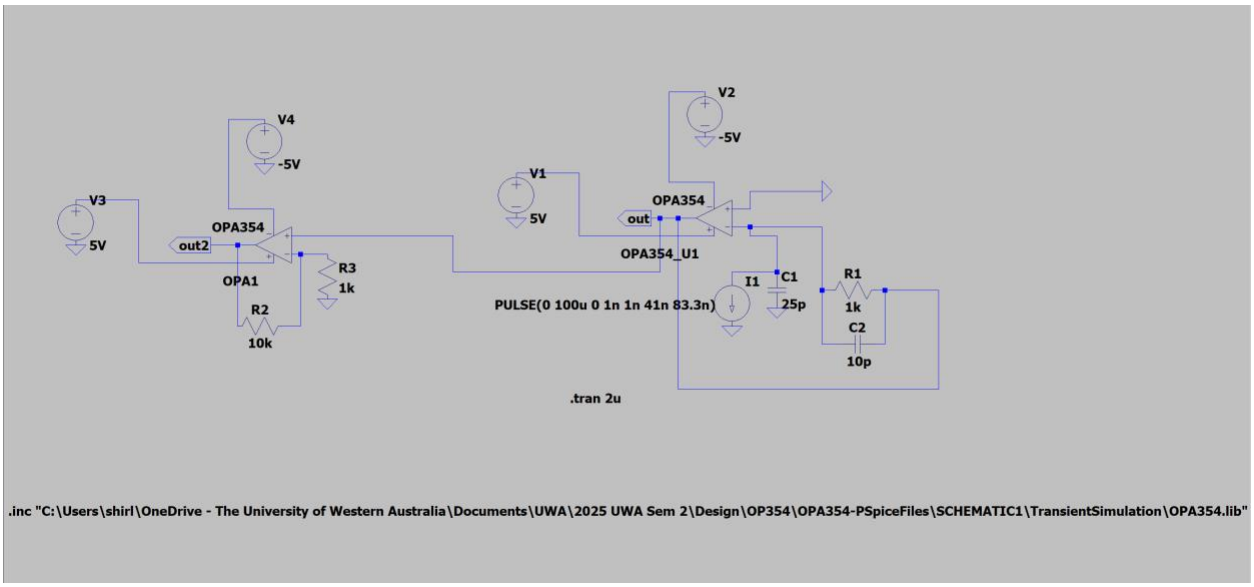



*Figure 52: Receiver Module 2 Stage non-inverting*

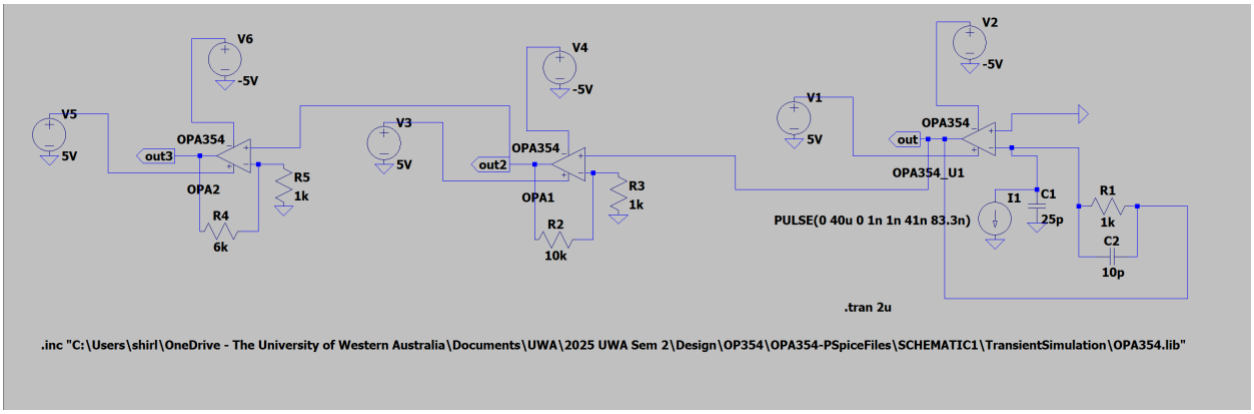



*Figure 53: Receiver Module Three Stage non-inverting*

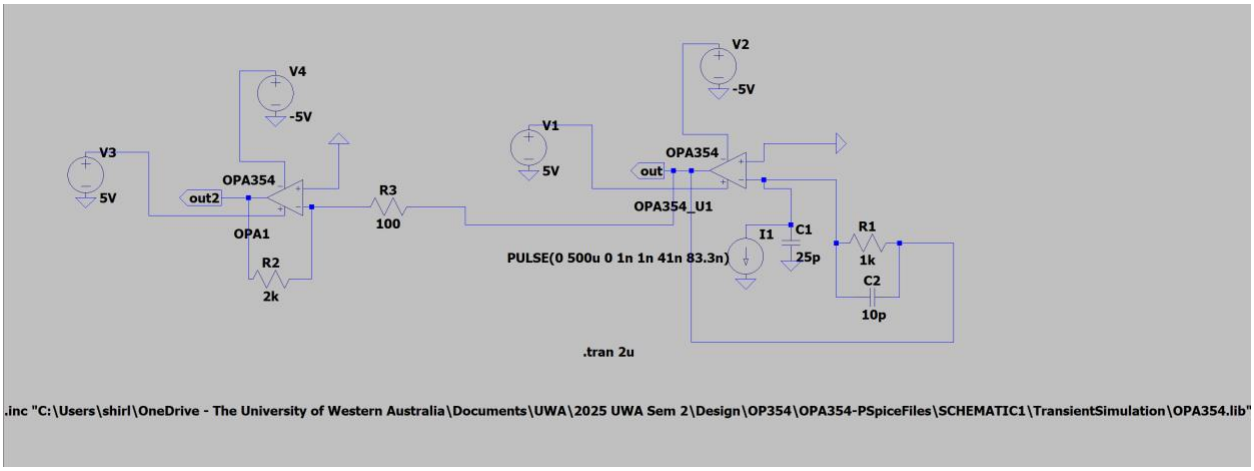



*Figure 54: Receiver Circuit Two stage inverting*

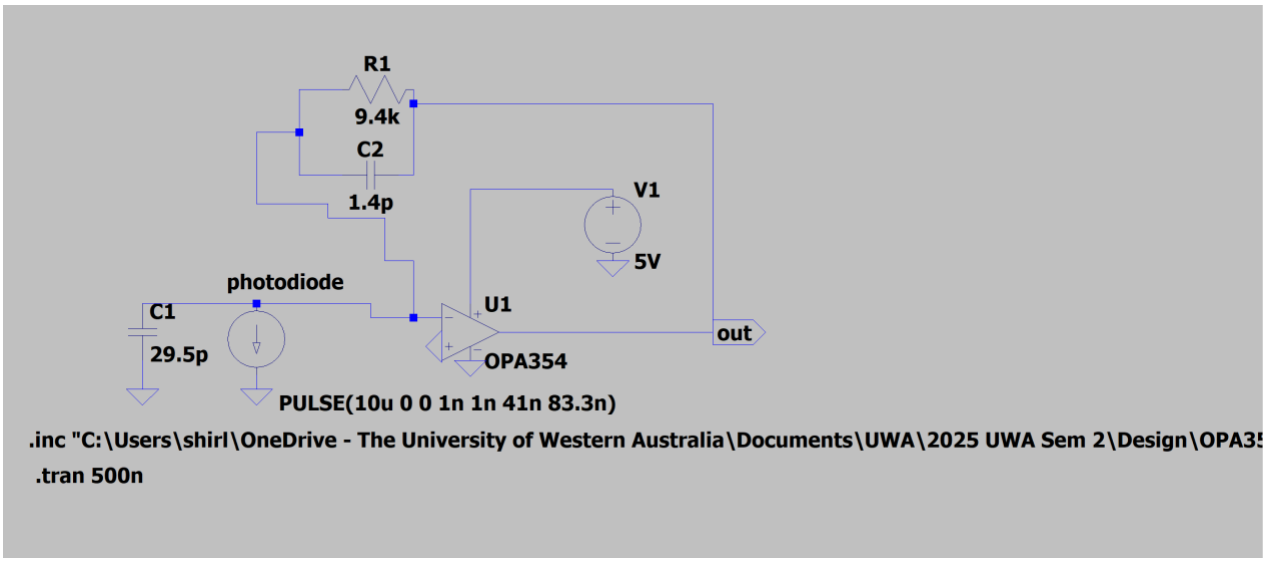



*Figure 55: Receiver Module Alternative Design I*

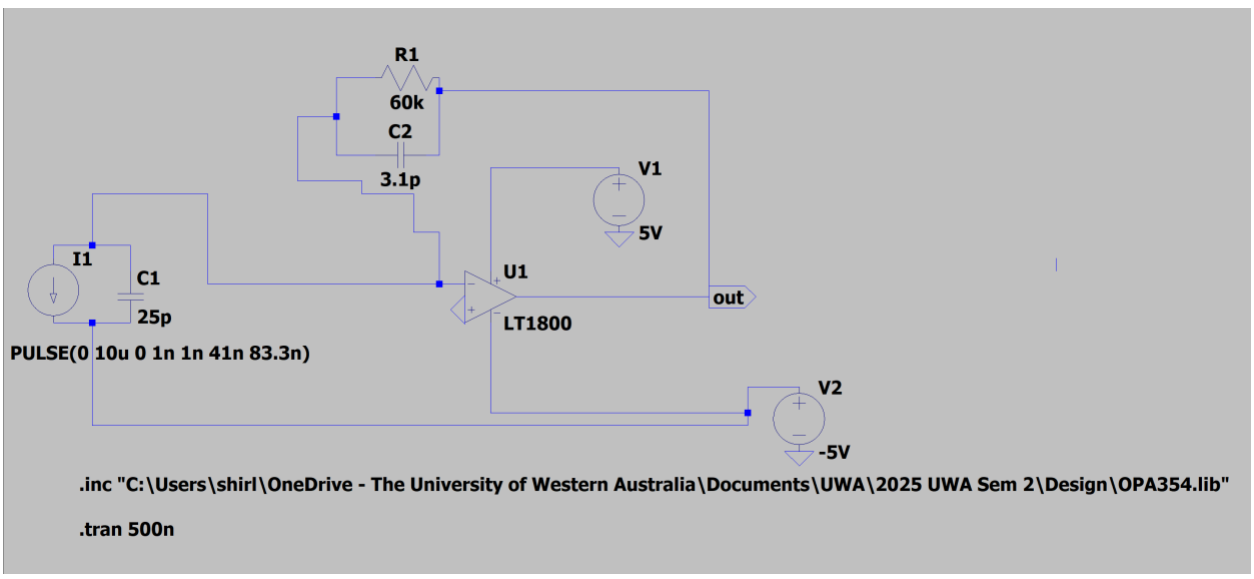



*Figure 56: Receiver Circuit Alternative Design II*

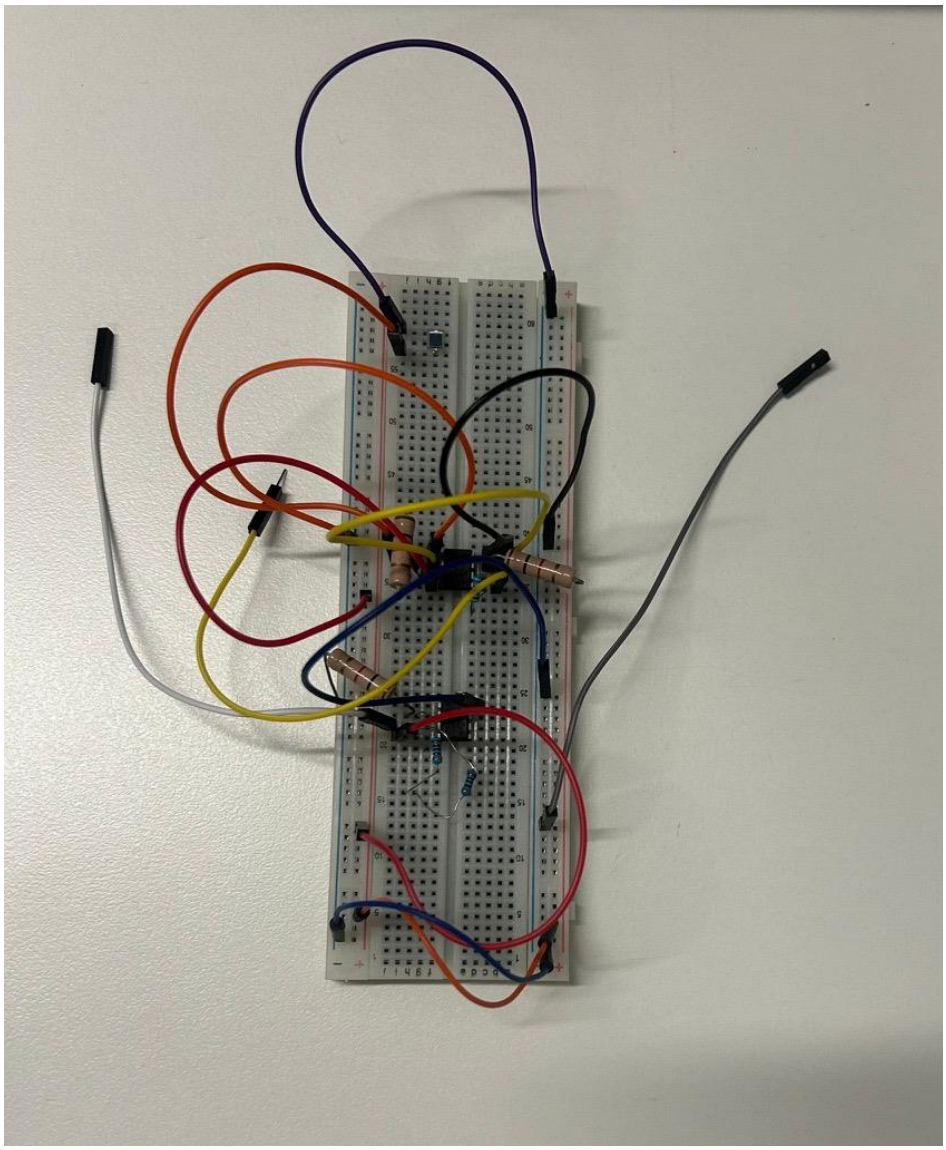


*Figure 57: Receiver Circuit Prototype*

## 9.9 Appendix I: Chassis design

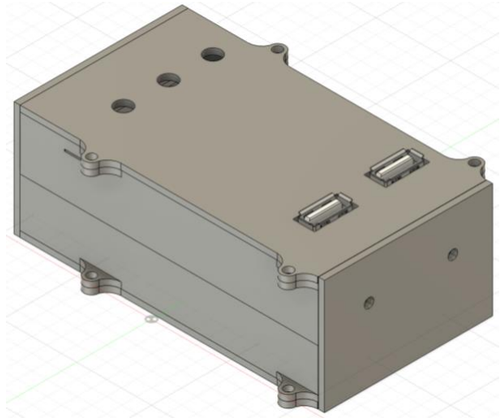
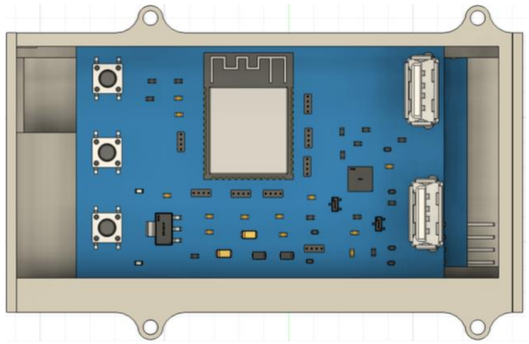
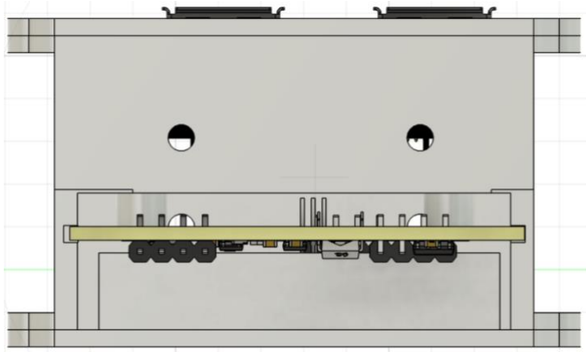
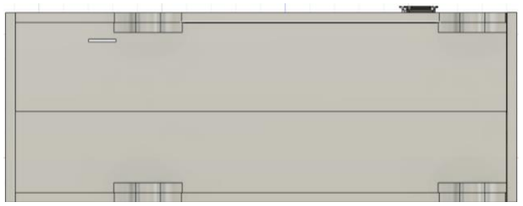
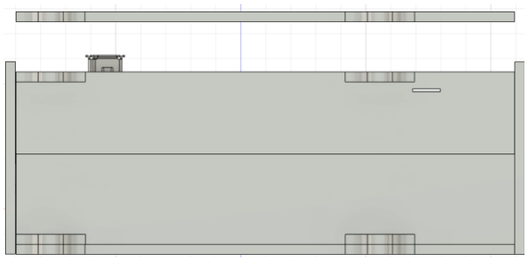
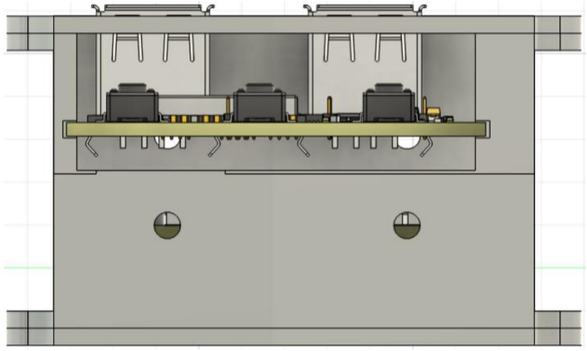
| Orthographic View | Top View (No Top Piece) | Front View (No Front Piece) |
|---|---|---|
|  |  |  |
| **Left Side View** | **Right Sde View (Lifted Top Piece)** | **Back View (No Back Piece)** |
|  |  |  |

*Figure 58: Final Version of the Chassis on Fusion*