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Thread: Unconstrained ports, port paths - what to do with them?

January 25th, 2010, 05:03 AM #1

yume
Altera Beginner

Join Date: Jan 2010
Posts: 2
Rep Power: 1

Unconstrained ports, port paths - what to do with them?

hi to all

i am wondering such a question - how exactly to constrain input & output ports & paths (i've already read some manuals, but cannot imagine how to do it in steps)
with clocks it seems to be all OK - they are constrained, but do i need to use set_clock_latency & set_clock_uncertainty either?

may be such a newbi question have been asked - then give, pls, a link to answer

p.s. i use The Quartus II TimeQuest Timing Analyzer

thanks

January 25th, 2010, 10:34 PM #2

KxAlpha
Altera Scholar

Join Date: Feb 2009
Posts: 28
Rep Power: 1

Re: Unconstrained ports, port paths - what to do with them?

I've had the same problems originally. I found that looking for help on TimeQuest in paper form is quite hard, the manuals are all a bit fuzzy. However, I stumbled over the Altera video training on their webpage and it does give you quite a good overview how to constrain stuff, at least the stuff that needs to be constrained in every project:

This one is the basic on TimeQuest analyser, you can skip most of the basic stuff, if you've been working with it for a while (even though I found stuff in there I didn't know yet). This is

the one, that explains how to set up clocks (internal/external):
http://www.altera.com/education/trai...urses/ODSW1115

I admit, setting virtual clocks didn't work for me, somehow, so I managed without.

This one explains to you, how to constrain inputs and outputs (at least source synchronous ones). This has the examples I used to successfully constrain my I/O's:
http://www.altera.com/education/trai...urses/OMEM1120

The second one is based on an older version of Quartus II I think, but it works nonetheless.

Hope that helps. Above two video trainings I found to be elemental to understand why and which constraints are needed and how to implement then. Ah yes, training's free of course.

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January 25th, 2010, 11:00 PM #3

yume
Altera Beginner

Join Date: Jan 2010
Posts: 2
Rep Power: 1

Re: Unconstrained ports, port paths - what to do with them?

thank you very much **KxAlpha** for your reply
i'll look up this links

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September 23rd, 2013, 11:04 PM #4

naceradsky
Altera Teacher

Join Date: Jun 2009
Posts: 123
Rep Power: 1

Re: Unconstrained ports, port paths - what to do with them?

Hi KxAlpha,

please, could you repair the links:
http://www.altera.com/education/trai...urses/OMEM1120

It write me, that the page not found and i solve now the same problem unconstrained ports, Input / Output port paths .

Thank you very much.

Jan

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September 23rd, 2013, 11:28 PM #5

KxAlpha
Altera Scholar

Join Date: Feb 2009
Posts: 28
Rep Power: 1

Re: Unconstrained ports, port paths - what to do with them?

> Originally Posted by **naceradsky**
>
> *Hi KxAlpha,*
>
> *please, could you repair the links:*
> *http://www.altera.com/education/trai...urses/OMEM1120*
>
> *It write me, that the page not found and i solve now the same problem unconstrained ports, Input / Output port paths .*
>
> *Thank you very much.*
>
> *Jan*

Hi Jan,

I do not know if these are the same tutorials I originally mentioned and I hope there not, since those left still a lot of open questions when you look at your own designs, but here you go:

http://www.altera.com/education/trai...urses/OCSS1000
http://www.altera.com/education/trai...urses/ODDR1000

A full list of all the other tutorials can be found here:

http://www.altera.com/servlets/searc...rsetype=Online

You simply need to register for them in order to start them, but they're free to use.

It really is kind of sad, that there are still no decent GUI based constraining wizards around that'll allow you to make the constraints, as it really is hard to keep track of all the formulas. Yeah you can use the input forms for constraints, but what I mean is a graphical representation of an external source/sink and my FPGA where you put in the delay for each part of the equation and get a better feel for what is really important. I really never use the formulas given to their full extent, but instead use some values I feel should work and usually that works OK. The most important thing to have is input and output delay constraints for all I/Os even if you set them to min/max 0, at least this way Quartus will know to what clock those signals are related to. That solves almost all of those works after every second compile even without me changing anything problems. After that a few multicycles where applicable and even if you get tons of warnings, your compilation results will almost always remain the same (if the design itself is working in silicon).

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September 24th, 2013, 12:26 AM #6

naceradsky
Altera Teacher

Join Date:	Jun 2009
Posts:	123
Rep Power:	1

Re: Unconstrained ports, port paths - what to do with them?

Hi KxAlpha,

great, I finally understand (perhaps) understanded the basics of inputs / outputs constraints,

which i must describe, how you write.
Yes, it is sad, that is no GUI based wizard. Before Altera FPGA i use Xilinx FPGA and in every .ucf (something like .qsf nad .sdc file in one) has from Project wizard text example, how to set clock paths, input/output paths, pin alocation, ignored paths etc. ... like remark and one neednt read some tutorial or pdf notes.
Is possible download this training curses on local disk ? Or save like pdf document ?

Thank you.

Jan

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September 24th, 2013, 05:17 AM #7

naceradsky
Altera Teacher

Join Date: Jun 2009
Posts: 123
Rep Power: 1

Re: Unconstrained ports, port paths - what to do with them?

But it is strange still. When i use basic constraints from:

http://www.altera.com/support/exampl...-template.html
```
==========================================
# Constrain clock port clk with a 10-ns requirement
create_clock -name {TS_clk} -period 10 [get_ports {clk}]

# Automatically apply a generate clock on the output of phase-locked loops (PLLs)
# derive_pll_clocks

# This command can be safely left in the SDC even if no PLLs exist in the design
derive_clock_uncertainty

# Constrain the input I/O path
set_input_delay -clock {TS_clk} -max 3 [all_inputs]
set_input_delay -clock {TS_clk} -min 2 [all_inputs]

# Constrain the output I/O path
set_output_delay -clock {TS_clk} 2 [all_outputs]
==========================================
```

I am not able to increase fmax up to 120MHz.
But when i dont use constrains for input output, i achieve nearly 200MHz.

You can see my 2 designs. The differences are only in sdc file .... and the differences of fmax is massive.

How it is possible ? How can i increase fmax, when i use constrains to all inputs and outputs ?

Thank you.

Jan

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September 24th, 2013, 05:19 AM #8

naceradsky
Altera Teacher

Join Date: Jun 2009
Posts: 123
Rep Power: 1

Re: Unconstrained ports, port paths - what to do with them?

Sorry, only projects in attachments....

Attached Files
File Type: qar pokus_timing_all_constraints_ok.qar (36.6 KB, 20 views)
File Type: qar pokus_timing_183MHz_no_input_output_constraints.qar (36.7 KB, 9 views)

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September 30th, 2013, 09:09 AM #9

davka
Altera Teacher

Join Date: Apr 2007
Posts: 115
Rep Power: 1

Re: Unconstrained ports, port paths - what to do with them?

> Originally Posted by **naceradsky**
>
> *I am not able to increase fmax up to 120MHz.*
> *But when i dont use constrains for input output, i achieve nearly 200MHz.*
>
> *You can see my 2 designs. The differences are only in sdc file .... and the differences of fmax is massive.*
>
> *How it is possible ? How can i increase fmax, when i use constrains to all inputs and outputs ?*
> *Jan*

Running at 200MHz inside the FPGA does not matter if you cannot get signals in and out of the FPGA at that speed.

Set input and output delay is used to model the paths from the external driving device to the FPGA, and from the FPGA to whatever device it is driving. TimeQuest is telling you that at 200MHz, you will not be able to get the signals in and/or out of the FPGA.

Adding more pipe-lining may be one solution to use an extra clock cycle to fix this problem.

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