universidade de aveiro

PROJETO 8

CALENDÁRIO DIGITAL

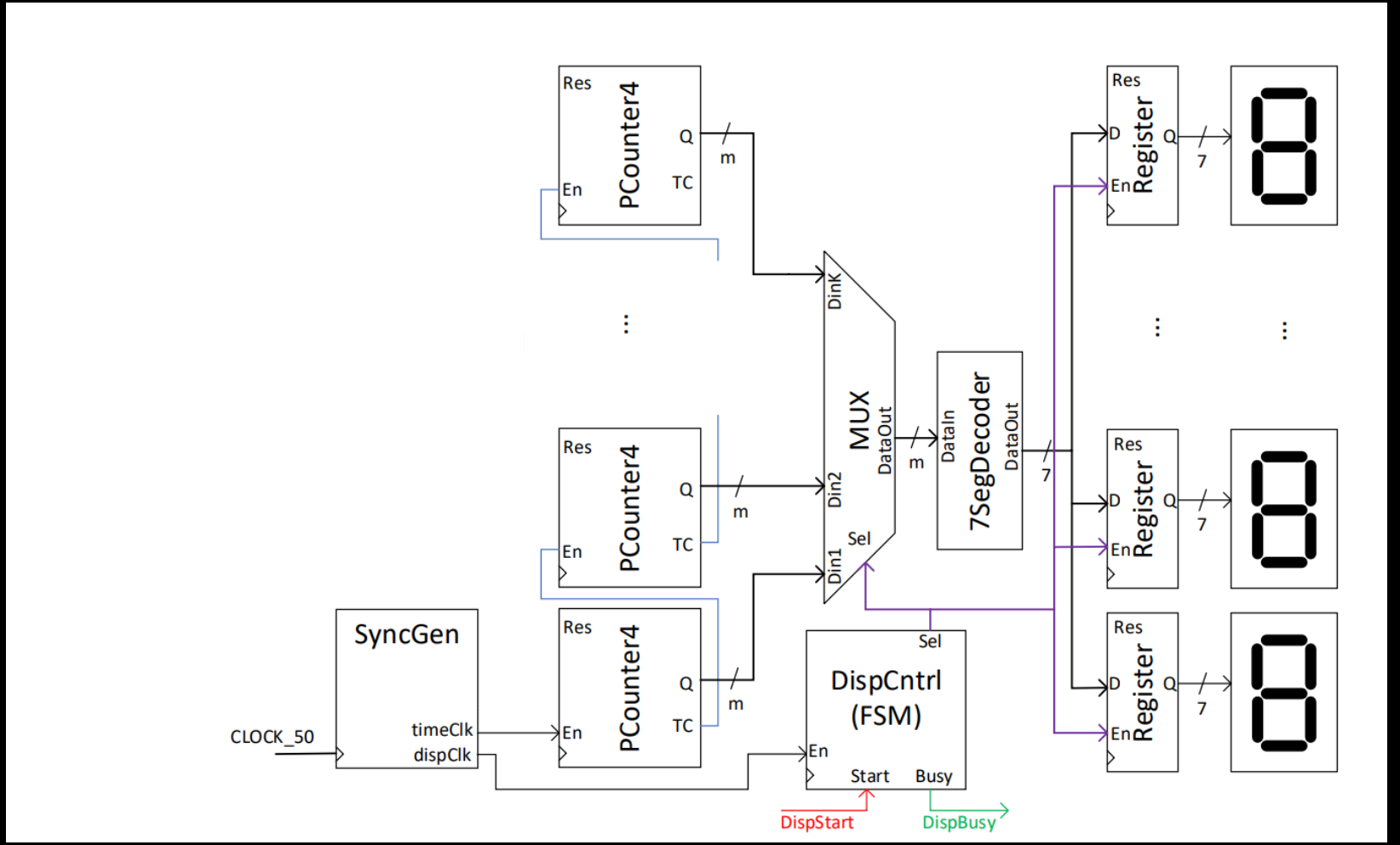
※ 98543 | LUIS OLIVEIRA
※ 102618 | JUAN BARROS

21 06 2021

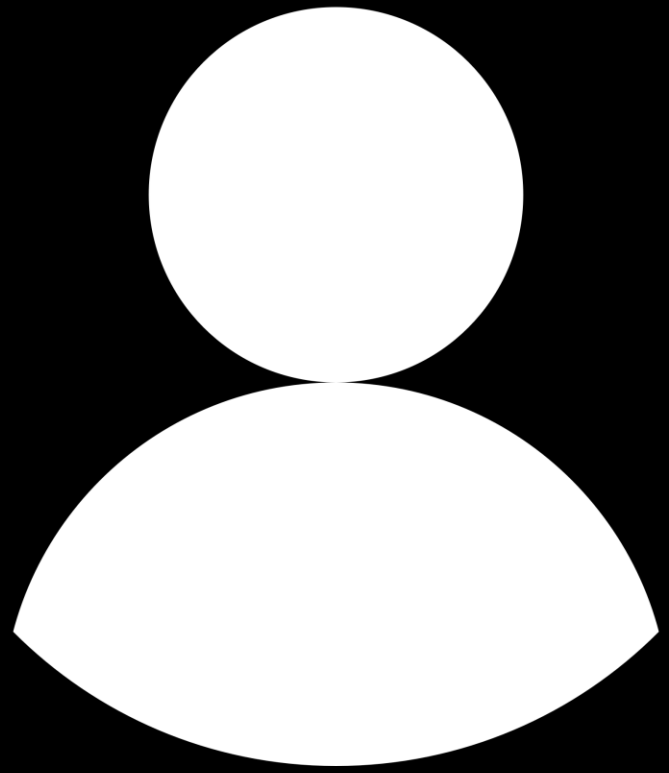
Introdução e objetivos

- Programar um calendário digital;
- Introduzir uma interação com o user;
- Aprofundar os conhecimentos da disciplina.

Arquitetura



Para o utilizador



File Edit View Project Assignments Processing Tools Window Help

Calendario1

Project Navigator | Files

- Mux.vhd
- Reg.vhd
- RegPulseGenerator.vhd
- Counter4Bits.vhd
- Bin7SegDecoder.vhd
- Mux.vwf
- Reg.vwf
- RegPulseGenerator.vwf
- Counter4Bits.vwf
- Bin7SegDecoder.vwf
- Counter5Bits.vhd
- DiasDoMes.vhd
- MeuCalendario.vhd
- BCD.vhd
- DispCntrl.vhd

Tasks | Compilation

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming files)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

MeuCalendario.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3  use IEEE.NUMERIC_STD.all;
4
5  entity MeuCalendario is
6     port(SW       : in  std_logic_vector(0 downto 0);
7          CLOCK_50 : in  std_logic;
8          KEY      : in  std_logic_vector(2 downto 0);
9          HEX0     : out std_logic_vector(6 downto 0);
10         HEX1     : out std_logic_vector(6 downto 0);
11         HEX2     : out std_logic_vector(6 downto 0);
12         HEX3     : out std_logic_vector(6 downto 0);
13         HEX4     : out std_logic_vector(6 downto 0);
14         HEX5     : out std_logic_vector(6 downto 0);
15         HEX6     : out std_logic_vector(6 downto 0);
16         HEX7     : out std_logic_vector(6 downto 0);
17         LEDG     : out std_logic_vector(8 downto 0);
                    ic_vector(17 downto 0));

                    alendario is

                    e, ano2Enable, ano3Enable, ano4Enable : std_logic;

32    signal diaOut, mesOut : std_logic_vector(4 downto 0);
33    signal ano1Out, ano2Out, ano3Out, ano4Out : std_logic_vector(3 downto 0);
34
35    --Terms
36    signal diaTerms, mesTerms, ano1Terms, ano2Terms, ano3Terms : std_logic;
37
38    --Max day of month
39    signal DayMonth : std_logic_vector(4 downto 0);
```

Open
Remove File from Project
Set as Top-Level Entity Ctrl+Shift+V
Create AHDL Include Files for Current File
Create Symbol Files for Current File
Create Verilog Instantiation Template Files for Current File
Create VHDL Component Declaration Files for Current File
Properties...

IP Catalog

Insta
Proje
Libra
Ba
DS
In
M
Pr
Un
Sear
Add...

All | <<Filter>> | Find... | Find Next

Type	ID	Message

Messages

System | Processing

Sets the current file entity as the top-level entity for the next compilation

File Edit View Project Assignments Processing Tools Window Help

Calendario1

Project Navigator | Files

- Mux.vhd
- Reg.vhd
- RegPulseGenerator.vhd
- Counter4Bits.vhd
- Bin7SegDecoder.vhd
- Mux.vwf
- Reg.vwf
- RegPulseGenerator.vwf
- Counter4Bits.vwf
- Bin7SegDecoder.vwf
- Counter5Bits.vhd
- DiasDoMes.vhd
- MeuCalendario.vhd
- BCD.vhd
- DispCntrl.vhd

Tasks | Compilation

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programm
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
- Edit Settings
- Program Device (Open Programme

MeuCalendario.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3  use IEEE.NUMERIC_STD.all;
4
5  entity MeuCalendario is
6     port(SW       : in  std_logic_vector(0 downto 0);
7          CLOCK_50 : in  std_logic;
8          KEY      : in  std_logic_vector(2 downto 0);
9          HEX0     : out std_logic_vector(6 downto 0);
10         HEX1     : out std_logic_vector(6 downto 0);
11         HEX2     : out std_logic_vector(6 downto 0);
12         HEX3     : out std_logic_vector(6 downto 0);
13         HEX4     : out std_logic_vector(6 downto 0);
14         HEX5     : out std_logic_vector(6 downto 0);
15         HEX6     : out std_logic_vector(6 downto 0);
16         HEX7     : out std_logic_vector(6 downto 0);
17         LEDG     : out std_logic_vector(8 downto 0);
18         LEDR     : out std_logic_vector(17 downto 0));
19
20 end MeuCalendario;
21
22
23 architecture Structural of MeuCalendario is
24
25    --Clocks
26    signal tC, dC : std_logic;
27
28    --Enables
29    signal mesEnable, ano1Enable, ano2Enable, ano3Enable, ano4Enable : std_logic;
30
31    --ValOut
32    signal diaOut, mesOut : std_logic_vector(4 downto 0);
33    signal ano1Out, ano2Out, ano3Out, ano4Out : std_logic_vector(3 downto 0);
34
35    --Terms
36    signal diaTerms, mesTerms, ano1Terms, ano2Terms, ano3Terms : std_logic;
37
38    --Max day of month
39    signal DayMonth : std_logic_vector(4 downto 0);
```

IP Catalog

- Installe
- Project
- Library
  - Basi
  - DSP
  - Inte
  - Mer
  - Proc
  - Univ
- Search

+ Add...

Messages

All | <<Filter>> | Find... | Find Next

Type	ID	Message

System | Processing

File Edit View Project Assignments Processing Tools Window Help

Device...
Settings... Ctrl+Shift+E
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
Logic Lock Regions Window Alt+L
Design Partitions Window Alt+D

Project Navigator | File

Mux.vhd
Reg.vhd
RegPulseGenerator.vh
Counter4Bits.vhd
Bin7SegDecoder.vhd
Mux.vwf
Reg.vwf
RegPulseGenerator.vw
Counter4Bits.vwf
Bin7SegDecoder.vwf
Counter5Bits.vhd
DiasDoMes.vhd
MeuCalendario.vhd
BCD.vhd
DispCntrl.vhd

Tasks | Compilation

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programn
TimeQuest Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programme

MeuCalendario.vhd

```
GIC_1164.all;
C_STD.all;

dario is
   : in  std_logic_vector(0 downto 0);
0 : in  std_logic;
   : in  std_logic_vector(2 downto 0);
   : out std_logic_vector(6 downto 0);
   : out std_logic_vector(6 downto 0);
   : out std_logic_vector(6 downto 0);
   : out std_logic_vector(6 downto 0);
   : out std_logic_vector(6 downto 0);
   : out std_logic_vector(6 downto 0);
14          HEX5     : out std_logic_vector(6 downto 0);
15          HEX6     : out std_logic_vector(6 downto 0);
16          HEX7     : out std_logic_vector(6 downto 0);
17          LEDG     : out std_logic_vector(8 downto 0);
18          LEDR     : out std_logic_vector(17 downto 0));
19
20  end MeuCalendario;
21
22
23  architecture Structural of MeuCalendario is
24
25      --Clocks
26      signal tC, dC : std_logic;
27
28      --Enables
29      signal mesEnable, ano1Enable, ano2Enable, ano3Enable, ano4Enable : std_logic;
30
31      --ValOut
32      signal diaOut, mesOut : std_logic_vector(4 downto 0);
33      signal ano1Out, ano2Out, ano3Out, ano4Out : std_logic_vector(3 downto 0);
34
35      --Terms
36      signal diaTerms, mesTerms, ano1Terms, ano2Terms, ano3Terms : std_logic;
37
38      --Max day of month
39      signal DayMonth : std_logic_vector(4 downto 0);
```

IP Catalog

All <<Filter>> Find... Find Next

Type ID Message

Messages

System Processing

Imports assignments from other sources

File Edit View Project Assignments Processing Tools Window Help

Calendario1

Project Navigator | Files

- Mux.vhd
- Reg.vhd
- RegPulseGenerator.vhd
- Counter4Bits.vhd
- Bin7SegDecoder.vhd
- Mux.vwf
- Reg.vwf
- RegPulseGenerator.vwf
- Counter4Bits.vwf
- Bin7SegDecoder.vwf
- Counter5Bits.vhd
- DiasDoMes.vhd
- MeuCalendario.vhd
- BCD.vhd
- DispCntrl.vhd

Tasks | Compilation

Task
- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programn
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
- Edit Settings
- Program Device (Open Programme

MeuCalendario.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3  use IEEE.NUMERIC_STD.all;
4
5  entity MeuCalendario is
6     port(SW       : in  std_logic_vector(0 downto 0);
7          CLOCK_50 : in  std_logic;
8          KEY      : in  std_logic_vector(2 downto 0);
9          HEX0     : out std_logic_vector(6 downto 0);
10         HEX1     : out std_logic_vector(6 downto 0);
11         HEX2     : out std_logic_vector(6 downto 0);
12         HEX3     : out std_logic_vector(6 downto 0);
13         HEX4     : out std_logic_vector(6 downto 0);
14         HEX5     : out std_logic_vector(6 downto 0);
15         HEX6     : out std_logic_vector(6 downto 0);
16         HEX7     : out std_logic_vector(6 downto 0);
17         LEDG     : out std_lo
18         LEDR     : out std_lo
19
20 end MeuCalendario;
21
22
23 architecture Structural of Me
24
25    --Clocks
26    signal tC, dC : std_logic;
27
28    --Enables
29    signal mesEnable, ano1Enable, ano2Enable, ano3Enable, ano4Enable : std_logic;
30
31    --ValOut
32    signal diaOut, mesOut : std_logic_vector(4 downto 0);
33    signal ano1Out, ano2Out, ano3Out, ano4Out : std_logic_vector(3 downto 0);
34
35    --Terms
36    signal diaTerms, mesTerms, ano1Terms, ano2Terms, ano3Terms : std_logic;
37
38    --Max day of month
39    signal DayMonth : std_logic_vector(4 downto 0);
```

Import Assignments

Specify the source and categories of assignments to import.

File name: [ ] [...] Categories...

Copy existing assignments into Calendario1.qsf.bak Advanced...

OK Cancel Help

IP Catalog

Instal
Proje
No
Librar
Ba
DS
Int
Me
Pr
Un
Searc
+ Add...

All <<Filter>> Find... Find Next

Type ID Message

Messages

System Processing

File Edit View Project Assignments Processing Tools Window Help

Calendario1

Project Navigator | Files

- Mux.vhd
- Reg.vhd
- RegPulseGenerator.vhd
- Counter4Bits.vhd
- Bin7SegDecoder.vhd
- Mux.vwf
- Reg.vwf
- RegPulseGenerator.vwf
- Counter4Bits.vwf
- Bin7SegDecoder.vwf
- Counter5Bits.vhd
- DiasDoMes.vhd
- MeuCalendario.vhd
- BCD.vhd
- DispCntrl.vhd

Tasks | Compilation

Task

- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programn
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programme

MeuCalendario.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3  use IEEE.NUMERIC_STD.all;
4
5  entity MeuCalendario is
6     port(SW       : in  std_logic_vector(0 downto 0);
7          CLOCK_50 : in  std_logic;
8          KEY      : in  std_logic_vector(2 downto 0);
9          HEX0     : out std_logic_vector(6 downto 0);
10         HEX1     : out std_logic_vector(6 downto 0);
11         HEX2     : out std_logic_vector(6 downto 0);
12         HEX3     : out std_logic_vector(6 downto 0);
13         HEX4     : out std_logic_vector(6 downto 0);
14         HEX5     : out std_logic_vector(6 downto 0);
15         HEX6     : out std_logic_vector(6 downto 0);
16         HEX7     : out std_logic_vector(6 downto 0);
17         LEDG     : out std_logic_vector(8 downto 0);
18         LEDR     : out std_logic_vector(17 downto 0));
19
20 end MeuCalendario;
21
22
23 architecture Structural of MeuCalendario is
24
25    --Clocks
26    signal tC, dC : std_logic;
27
28    --Enables
29    signal mesEnable, ano1Enable, ano2Enable, ano3Enable, ano4Enable : std_logic;
30
31    --ValOut
32    signal diaOut, mesOut : std_logic_vector(4 downto 0);
33    signal ano1Out, ano2Out, ano3Out, ano4Out : std_logic_vector(3 downto 0);
34
35    --Terms
36    signal diaTerms, mesTerms, ano1Terms, ano2Terms, ano3Terms : std_logic;
37
38    --Max day of month
39    signal DayMonth : std_logic_vector(4 downto 0);
```

IP Catalog

All | <<Filter>> | Find... | Find Next

Type	ID	Message
i	140120	Import completed. 519 assignments were written (out of 1123 read). 598 non-global assignments were skipped because of entity name mismatch.

Messages

System (1) | Processing

File Edit View Project Assignments Processing Tools Window Help

Calendario1

Project Navigator | Files

- Mux.vhd
- Reg.vhd
- RegPulseGenerator.vhd
- Counter4Bits.vhd
- Bin7SegDecoder.vhd
- Mux.vwf
- Reg.vwf
- RegPulseGenerator.vwf
- Counter4Bits.vwf
- Bin7SegDecoder.vwf
- Counter5Bits.vhd
- DiasDoMes.vhd
- MeuCalendario.vhd
- BCD.vhd
- DispCntrl.vhd

Tasks | Compilation

Task
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programn
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programme

MeuCalendario.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3  use IEEE.NUMERIC_STD.all;
4
5  entity MeuCalendario is
6     port(SW       : in  std_logic_vector(0 downto 0);
7          CLOCK_50 : in  std_logic;
8          KEY      : in  std_logic_vector(2 downto 0);
9          HEX0     : out std_logic_vector(6 downto 0);
10         HEX1     : out std_logic_vector(6 downto 0);
11         HEX2     : out std_logic_vector(6 downto 0);
12         HEX3     : out std_logic_vector(6 downto 0);
13         HEX4     : out std_logic_vector(6 downto 0);
14         HEX5     : out std_logic_vector(6 downto 0);
15         HEX6     : out std_logic_vector(6 downto 0);
16         HEX7     : out std_logic_vector(6 downto 0);
17         LEDG     : out std_logic_vector(8 downto 0);
18         LEDR     : out std_logic_vector(17 downto 0));
19
20 end MeuCalendario;
21
22
23 architecture Structural of MeuCalendario is
24
25    --Clocks
26    signal tC, dC : std_logic;
27
28    --Enables
29    signal mesEnable, ano1Enable, ano2Enable, ano3Enable,
30
31    --ValOut
32    signal diaOut, mesOut : std_logic_vector(4 downto 0);
33    signal ano1Out, ano2Out, ano3Out, ano4Out : std_logic
34
35    --Terms
36    signal diaTerms, mesTerms, ano1Terms, ano2Terms, ano3
37
38    --Max day of month
39    signal DayMonth : std_logic_vector(4 downto 0);
```

IP Catalog

Programmer - C:/intelFPGA_lite/17.1/.LSD/Projeto/Fase1/Calendario1 - Calendario1 - [C...

File Edit View Processing Tools Window Help

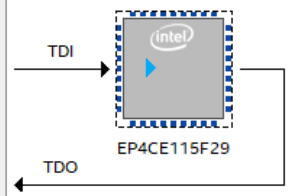
Search altera.com

Hardware Setup... | No Hardware | Mode: JTAG | Progress:

Enable real-time ISP to allow background programming when available

Start
Stop
Auto Detec
Delete
Add File...
Change File
Save File
Add Device
Up
Down

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank-Check	Examine
output_files/Cale...	EP4CE115F29	0059847D	0059847D	☑	☐	☐	☐

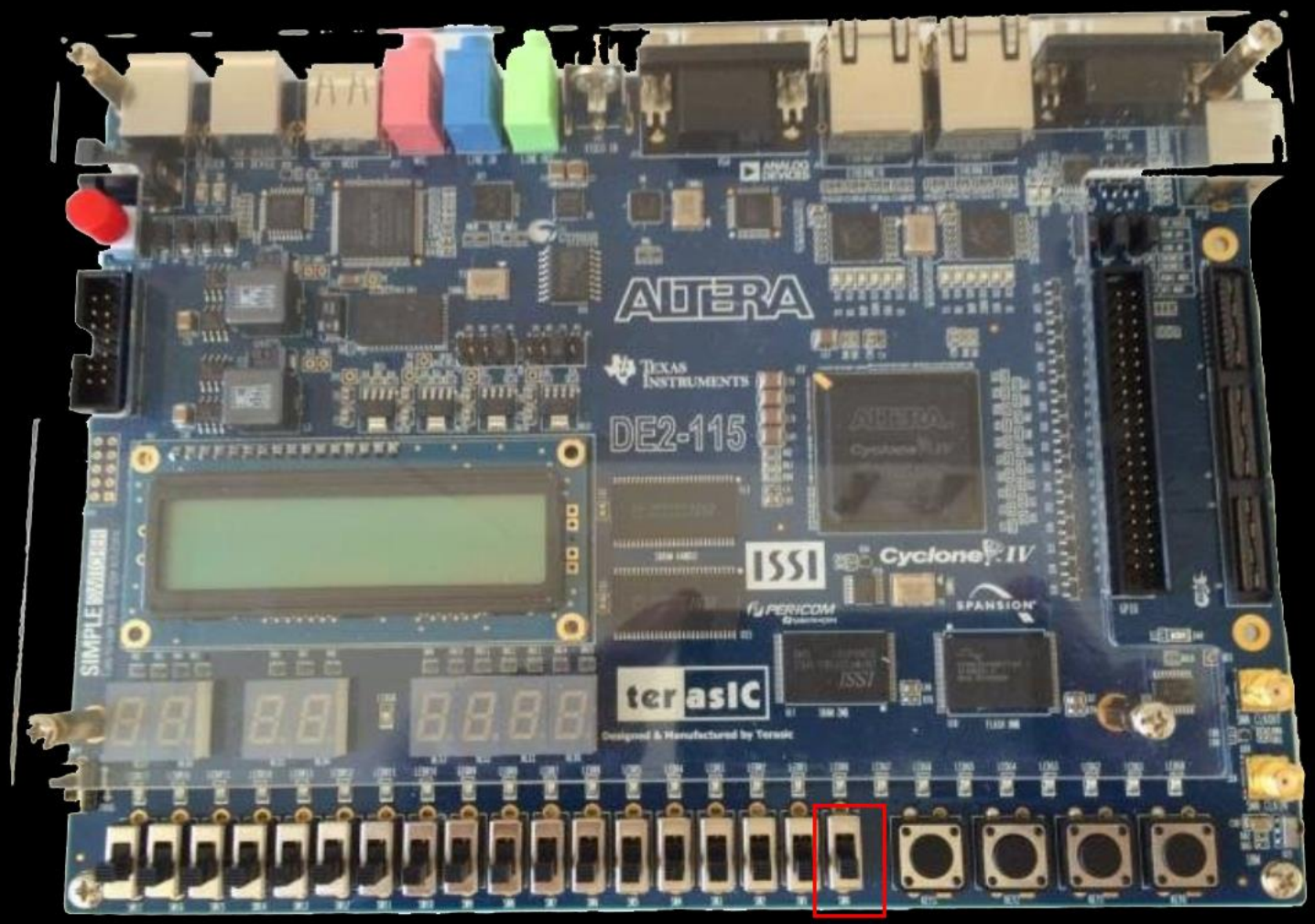


All | <<Filter>> | Find... | Find Next

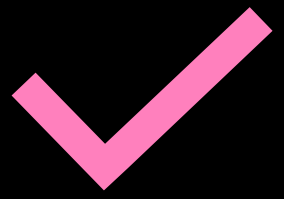
Type	ID	Message
ℹ	140120	Import completed. 519 assignments were written (out of 1123 read). 598 non-global assignments were skipped because of entity name mismatch.

Messages

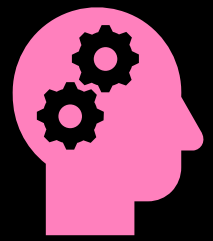
System (1) | Processing


ALTERA
DE2-115
ISSI
Cyclone IV
terasIC

Aspetos finais



Fase 1 desenvolvida



Melhor compreensão da matéria lecionada

Melhoria na relação entre colegas