



INSTITUTO POLITÉCNICO NACIONAL

ESCUELA SUPERIOR DE CÓMPUTO

CARACTERÍSTICAS REALES DE LOS
AMPLIFICADORES OPERACIONALES

ELECTRÓNICA ANALÓGICA

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INSTITUTO POLITÉCNICO NACIONAL



Características Reales de los Amplificadores Operacionales

Electrónica Analógica

Utilizando **ÚNICA Y EXCLUSIVAMENTE** los datos de las datasheet anexadas, tenemos que:

	LM741	TL071	LM308	LM311
Resistencia o Impedancia de Entrada	Min 0.3 MOhm TYP 2MOhm	10^{12} Ohm	Min 10 MOhm TYP 40MOhm	N/A
Resistencia o Impedancia de salida	-	-	-	N/A
Ganancia en Voltaje	Min50-TYP 200 V/mv (TA=25C) Min 25 V/mV (TAMIN < TA < TAMAX)	-	Min80-TYP 300 V/mv (TA=25C+-15V) Min 40 V/mV (10RL>10kohm)	Min40 -TYP 200 V/mv
Ancho de Banda	Min 0.437 MHz TYP 15MHz	5.25 MHz	250kHz	
Voltaje de Offset	TYP 1 mV Max 5mV	1 mV	10mV	2 - 7.5 - 10 mV
Voltaje de Drift	15 microVolts / °C	2 mV/C	TYP 2mV Max 7mV	
Tiempo de Formación (Tf)	-	-	-	-
Tiempo de Decaimiento (Tr)	-	-	-	-
Slew Rate	0.5 V/microSegs.	20 V/ms	10V/mS	18V/ms
Configuración de sus pines	Figura 1	Figura 2	Figura 3	Figura 4

Cuadro 1: Características Reales de los Amplificadores Operacionales

1. Configuración de sus pines en el encapsulado

Configuración de pines de LM741



Función de pines

PIN	NO.	I/O	Descripción
Nombre			
INVERTING INPUT	2	I	Invertidor de señal de entrada
NC	8	N/A	No conectar, dejarse flotando
NONINVERTING INPUT	3	I	Señal de entrada sin invertir
OFFSET NULL	1, 5	I	Pin nulo usado para eliminar la señal de voltaje de offset y balancear v. de ent.
OFFSET NULL	6	O	Amplificador de señal de salida
V+	7	I	Suplidor de voltaje positivo
V-	4	I	Suplidor de voltaje negativo

Figura 1: Configuración de sus pines en el encapsulado de LM741

Configuración de pines de TL071

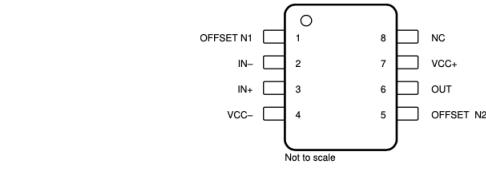


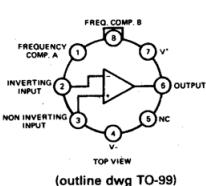
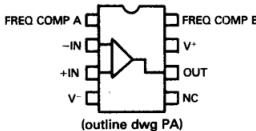
Figure 5-1. TL071x D, P, and PS Package
8-Pin SOIC, PDIP, and SO
Top View

Table 5-1. Pin Functions: TL071x

PIN	NAME	NO.	I/O	DESCRIPTION
IN-	IN-	2	I	Invertidor de señal de entrada
IN+	IN+	3	I	Señal de entrada sin invertir
NC	NC	8	—	No conectar, dejarse flotando
OFFSET N1	OFFSET N1	1	—	Input offset adjustment
OFFSET N2	OFFSET N2	5	—	Input offset adjustment
OUT	OUT	6	O	Output
VCC-	VCC-	4	—	Suplidor de voltaje negativo
VCC+	VCC+	7	—	Suplidor de voltaje positivo

Figura 2: Configuración de sus pines en el encapsulado de TL071

Configuración de pines del LM308



DUAL-IN-LINE PACKAGE

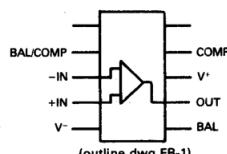
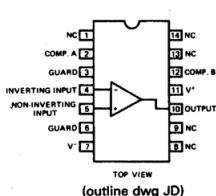
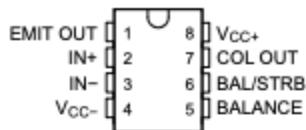


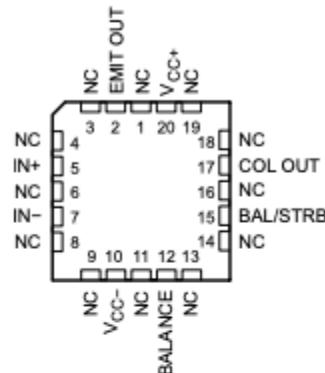
Figura 3: Configuración de sus pines en el encapsulado de LM308

Configuración del LM311

LMx11 D, JG, P, PS, or PW Package
8-Pin SOIC, CDIP, PDIP, SO or TSSOP
Top View



LM111 FK Package
20-Pin LCCC⁽¹⁾
Top View



(1) NC = No internal connection

Pin Functions

NAME	PIN				I/O ⁽¹⁾	DESCRIPTION
	LM211, LM311	LM311	LM111	LM111		
SOIC, PDIP, TSSOP	SO	CDIP	LCCC			
IN+	2	2	2	5	I	Comparador sin inversor
IN-	3	3	3	7	I	Comparador con inversor
BALANCE	5	5	5	12	I	Balance
BAL/STRB	6	6	6	15	I	Strobe
COL OUT	7	7	7	17	O	Salida del colector comparador
EMIT OUT	1	1	1	2	O	Salida del emisor comparador
VCC-	4	4	4	10	—	Fuente negativar
VCC+	8	8	8	20	—	Fuente Positivar
				1		
				3		
				4		
				6		
				8		
				9		
				11		
				13		
				14		
				16		
				18		
				19		
NC	—	—	—	—	—	No conectar

(1) I = Input, O = Output

Figura 4: Configuración de sus pines en el encapsulado de LM308

2. Datasheet

A continuación y en el siguiente orden:

- LM741
- TL071
- LM308
- LM311

Se anexan las hojas de especificaciones o datasheet con las que se realizó este trabajo.

LM741 Operational Amplifier

1 Features

- Overload Protection on the Input and Output
- No Latch-Up When the Common-Mode Range is Exceeded

2 Applications

- Comparators
- Multivibrators
- DC Amplifiers
- Summing Amplifiers
- Integrator or Differentiators
- Active Filters

3 Description

The LM741 series are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439, and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common-mode range is exceeded, as well as freedom from oscillations.

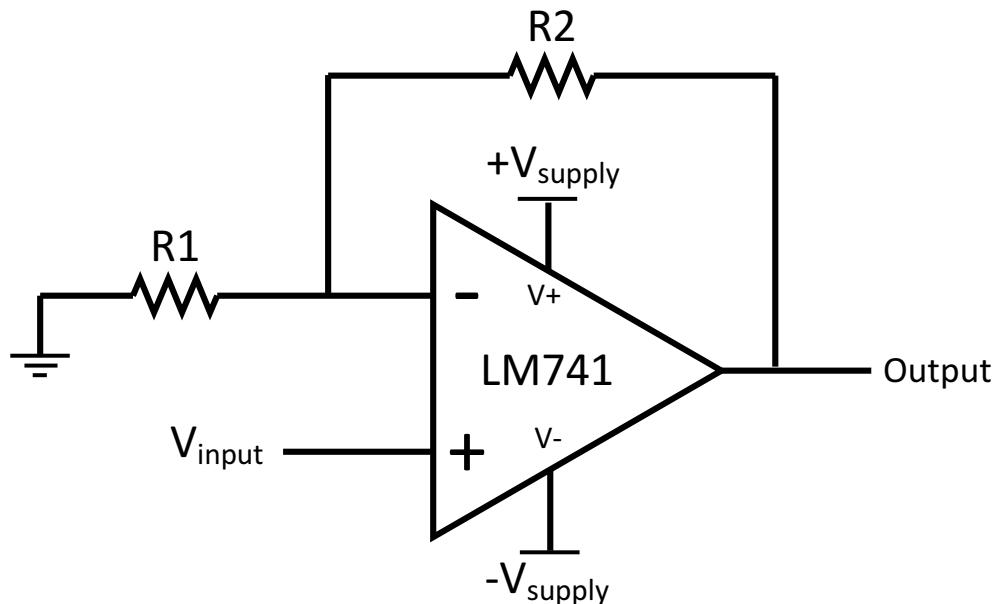
The LM741C is identical to the LM741 and LM741A except that the LM741C has their performance ensured over a 0°C to +70°C temperature range, instead of -55°C to +125°C.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM741	TO-99 (8)	9.08 mm × 9.08 mm
	CDIP (8)	10.16 mm × 6.502 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features	1	7.3 Feature Description.....	7
2 Applications	1	7.4 Device Functional Modes.....	8
3 Description	1	8 Application and Implementation	9
4 Revision History.....	2	8.1 Application Information.....	9
5 Pin Configuration and Functions	3	8.2 Typical Application	9
6 Specifications.....	4	9 Power Supply Recommendations	10
6.1 Absolute Maximum Ratings	4	10 Layout.....	11
6.2 ESD Ratings.....	4	10.1 Layout Guidelines	11
6.3 Recommended Operating Conditions	4	10.2 Layout Example	11
6.4 Thermal Information	4	11 Device and Documentation Support	12
6.5 Electrical Characteristics, LM741.....	5	11.1 Community Resources.....	12
6.6 Electrical Characteristics, LM741A	5	11.2 Trademarks	12
6.7 Electrical Characteristics, LM741C	6	11.3 Electrostatic Discharge Caution	12
7 Detailed Description	7	11.4 Glossary	12
7.1 Overview	7	12 Mechanical, Packaging, and Orderable	
7.2 Functional Block Diagram	7	Information	12

4 Revision History

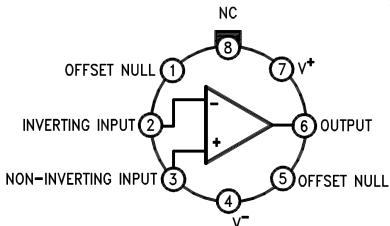
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2004) to Revision D	Page
• Added <i>Applications</i> section, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Removed NAD 10-Pin CLGA pinout	3
• Removed obselete M (S0-8) package from the data sheet	4
• Added recommended operating supply voltage spec	4
• Added recommended operating temperature spec	4

Changes from Revision C (March 2013) to Revision D	Page
• Added <i>Applications</i> section, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
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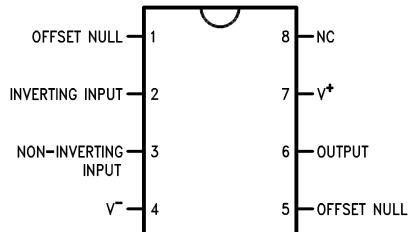
5 Pin Configuration and Functions

**LMC Package
8-Pin TO-99
Top View**



LM741H is available per JM38510/10101

**NAB Package
8-Pin CDIP or PDIP
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INVERTING INPUT	2	I	Inverting signal input
NC	8	N/A	No Connect, should be left floating
NONINVERTING INPUT	3	I	Noninverting signal input
OFFSET NULL	1, 5	I	Offset null pin used to eliminate the offset voltage and balance the input voltages.
OFFSET NULL			
OUTPUT	6	O	Amplified signal output
V+	7	I	Positive supply voltage
V-	4	I	Negative supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

		MIN	MAX	UNIT
Supply voltage	LM741, LM741A		±22	V
	LM741C		±18	
Power dissipation ⁽⁴⁾		500		mW
Differential input voltage		±30		V
Input voltage ⁽⁵⁾		±15		V
Output short circuit duration		Continuous		
Operating temperature	LM741, LM741A	-50	125	°C
	LM741C	0	70	
Junction temperature	LM741, LM741A		150	°C
	LM741C		100	
Soldering information	PDIP package (10 seconds)		260	°C
	CDIP or TO-99 package (10 seconds)		300	
Storage temperature, T _{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) For military specifications see RETS741X for LM741 and RETS741AX for LM741A.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (4) For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). T_j = T_A + (θ_{JA} P_D).
- (5) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±400 V

- (1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage (VDD-GND)	LM741, LM741A	±10	±15	±22	V
	LM741C	±10	±15	±18	
Temperature	LM741, LM741A	-55		125	°C
	LM741C	0		70	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LM741			UNIT
	LMC (TO-99)	NAB (CDIP)	P (PDIP)	
	8 PINS	8 PINS	8 PINS	
R _{θJA} Junction-to-ambient thermal resistance	170	100	100	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	25	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics, LM741⁽¹⁾

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \leq 10 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$		1	5	mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$			6	mV
Input offset voltage adjustment range	$T_A = 25^\circ\text{C}, V_S = \pm 20 \text{ V}$		± 15			mV
Input offset current	$T_A = 25^\circ\text{C}$ $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		20	200		nA
			85	500		
Input bias current	$T_A = 25^\circ\text{C}$ $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		80	500	nA	μA
					1.5	
Input resistance	$T_A = 25^\circ\text{C}, V_S = \pm 20 \text{ V}$		0.3	2		M Ω
Input voltage range	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		± 12	± 13		V
Large signal voltage gain	$V_S = \pm 15 \text{ V}, V_O = \pm 10 \text{ V}, R_L \geq 2 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	50	200		V/mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	25			
Output voltage swing	$V_S = \pm 15 \text{ V}$	$R_L \geq 10 \text{ k}\Omega$	± 12	± 14		V
		$R_L \geq 2 \text{ k}\Omega$	± 10	± 13		
Output short circuit current	$T_A = 25^\circ\text{C}$		25			mA
Common-mode rejection ratio	$R_S \leq 10 \text{ }\Omega, V_{CM} = \pm 12 \text{ V}, T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		80	95		dB
Supply voltage rejection ratio	$V_S = \pm 20 \text{ V}$ to $V_S = \pm 5 \text{ V}, R_S \leq 10 \text{ }\Omega, T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		86	96		dB
Transient response	Rise time Overshoot	$T_A = 25^\circ\text{C}$, unity gain		0.3		μs
				5%		
Slew rate	$T_A = 25^\circ\text{C}$, unity gain		0.5			V/ μs
Supply current	$T_A = 25^\circ\text{C}$		1.7	2.8		mA
Power consumption	$V_S = \pm 15 \text{ V}$	$T_A = 25^\circ\text{C}$	50	85		mW
		$T_A = T_{A\text{MIN}}$	60	100		
		$T_A = T_{A\text{MAX}}$	45	75		

(1) Unless otherwise specified, these specifications apply for $V_S = \pm 15 \text{ V}, -55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$.

6.6 Electrical Characteristics, LM741A⁽¹⁾

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \leq 50 \text{ }\Omega$	$T_A = 25^\circ\text{C}$		0.8	3	mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$			4	mV
Average input offset voltage drift			15			$\mu\text{V}/^\circ\text{C}$
Input offset voltage adjustment range	$T_A = 25^\circ\text{C}, V_S = \pm 20 \text{ V}$		± 10			mV
			3	30		nA
Input offset current	$T_A = 25^\circ\text{C}$ $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$				70	
Average input offset current drift			0.5			$\text{nA}/^\circ\text{C}$
Input bias current	$T_A = 25^\circ\text{C}$ $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		30	80	nA	μA
					0.21	
Input resistance	$T_A = 25^\circ\text{C}, V_S = \pm 20 \text{ V}$ $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}, V_S = \pm 20 \text{ V}$		1	6		M Ω
			0.5			
Large signal voltage gain	$V_S = \pm 20 \text{ V}, V_O = \pm 15 \text{ V}, R_L \geq 2 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	50			V/mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	32			
		$V_S = \pm 5 \text{ V}, V_O = \pm 2 \text{ V}, R_L \geq 2 \text{ k}\Omega, T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	10			

(1) Unless otherwise specified, these specifications apply for $V_S = \pm 15 \text{ V}, -55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$.

Electrical Characteristics, LM741A⁽¹⁾ (continued)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT		
Output voltage swing	$V_S = \pm 20 \text{ V}$	$R_L \geq 10 \text{ k}\Omega$	± 16		± 15	V		
		$R_L \geq 2 \text{ k}\Omega$	± 15					
Output short circuit current	$T_A = 25^\circ\text{C}$		10	25	35	mA		
	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		10		40			
Common-mode rejection ratio	$R_S \leq 50 \Omega$, $V_{CM} = \pm 12 \text{ V}$, $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		80	95	dB			
Supply voltage rejection ratio	$V_S = \pm 20 \text{ V}$ to $V_S = \pm 5 \text{ V}$, $R_S \leq 50 \Omega$, $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		86	96	dB			
Transient response	Rise time	$T_A = 25^\circ\text{C}$, unity gain		0.25	0.8	μs		
	Overshoot			6%	20%			
Bandwidth ⁽²⁾	$T_A = 25^\circ\text{C}$		0.437	1.5	MHz			
Slew rate	$T_A = 25^\circ\text{C}$, unity gain		0.3	0.7	V/ μs			
Power consumption	$V_S = \pm 20 \text{ V}$	$T_A = 25^\circ\text{C}$	80	150	mW			
		$T_A = T_{A\text{MIN}}$						
		$T_A = T_{A\text{MAX}}$						

(2) Calculated value from: BW (MHz) = 0.35/Rise Time (μs).**6.7 Electrical Characteristics, LM741C⁽¹⁾**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \leq 10 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	2		6	mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	7.5		mV	
Input offset voltage adjustment range	$T_A = 25^\circ\text{C}$, $V_S = \pm 20 \text{ V}$		± 15		mV	
Input offset current		$T_A = 25^\circ\text{C}$	20	200	nA	
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	300			
Input bias current		$T_A = 25^\circ\text{C}$	80	500	nA	
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	0.8		μA	
Input resistance	$T_A = 25^\circ\text{C}$, $V_S = \pm 20 \text{ V}$		0.3	2	M Ω	
Input voltage range	$T_A = 25^\circ\text{C}$		± 12	± 13	V	
Large signal voltage gain	$V_S = \pm 15 \text{ V}$, $V_O = \pm 10 \text{ V}$, $R_L \geq 2 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	20	200	V/mV	
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	15			
Output voltage swing	$V_S = \pm 15 \text{ V}$	$R_L \geq 10 \text{ k}\Omega$	± 12	± 14	V	
		$R_L \geq 2 \text{ k}\Omega$	± 10	± 13		
Output short circuit current	$T_A = 25^\circ\text{C}$		25		mA	
Common-mode rejection ratio	$R_S \leq 10 \text{ k}\Omega$, $V_{CM} = \pm 12 \text{ V}$, $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		70	90	dB	
Supply voltage rejection ratio	$V_S = \pm 20 \text{ V}$ to $V_S = \pm 5 \text{ V}$, $R_S \leq 10 \Omega$, $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		77	96	dB	
Transient response	Rise time	$T_A = 25^\circ\text{C}$, Unity Gain		0.3	μs	
	Overshoot			5%		
Slew rate	$T_A = 25^\circ\text{C}$, Unity Gain		0.5		V/ μs	
Supply current	$T_A = 25^\circ\text{C}$		1.7		2.8	mA
Power consumption	$V_S = \pm 15 \text{ V}$, $T_A = 25^\circ\text{C}$		50		85	mW

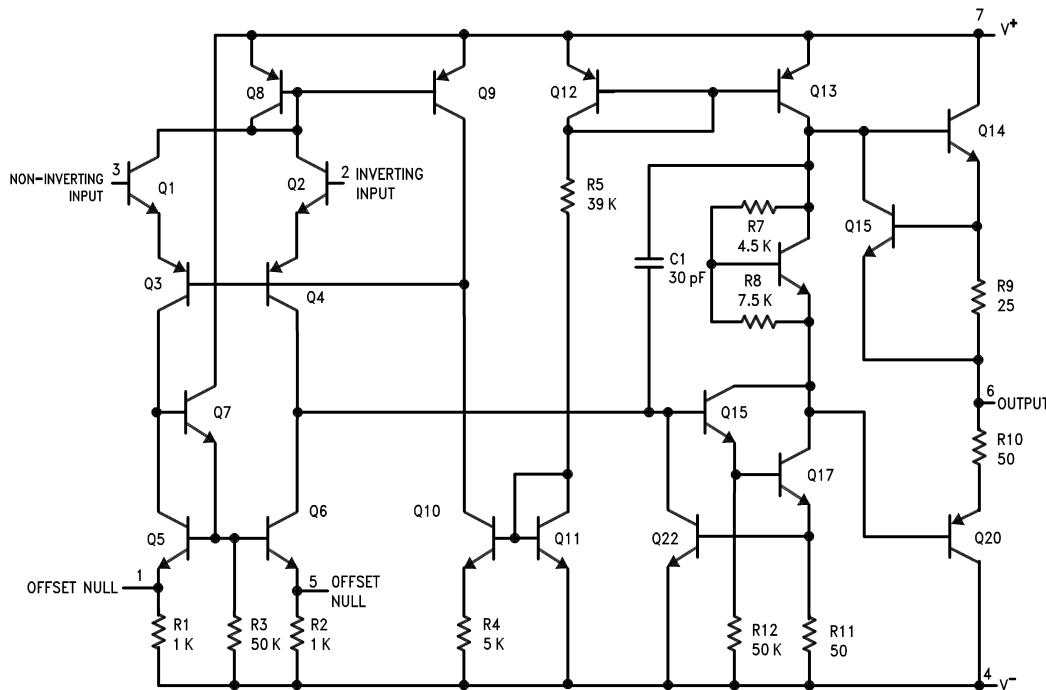
(1) Unless otherwise specified, these specifications apply for $V_S = \pm 15 \text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$.

7 Detailed Description

7.1 Overview

The LM74 devices are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. It is intended for a wide range of analog applications. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications. The LM741 can operate with a single or dual power supply voltage. The LM741 devices are direct, plug-in replacements for the 709C, LM201, MC1439, and 748 in most applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Overload Protection

The LM741 features overload protection circuitry on the input and output. This prevents possible circuit damage to the device.

7.3.2 Latch-up Prevention

The LM741 is designed so that there is no latch-up occurrence when the common-mode range is exceeded. This allows the device to function properly without having to power cycle the device.

7.3.3 Pin-to-Pin Capability

The LM741 is pin-to-pin direct replacements for the LM709C, LM201, MC1439, and LM748 in most applications. Direct replacement capabilities allows flexibility in design for replacing obsolete parts.

7.4 Device Functional Modes

7.4.1 Open-Loop Amplifier

The LM741 can be operated in an open-loop configuration. The magnitude of the open-loop gain is typically large thus for a small difference between the noninverting and inverting input terminals, the amplifier output will be driven near the supply voltage. Without negative feedback, the LM741 can act as a comparator. If the inverting input is held at 0 V, and the input voltage applied to the noninverting input is positive, the output will be positive. If the input voltage applied to the noninverting input is negative, the output will be negative.

7.4.2 Closed-Loop Amplifier

In a closed-loop configuration, negative feedback is used by applying a portion of the output voltage to the inverting input. Unlike the open-loop configuration, closed loop feedback reduces the gain of the circuit. The overall gain and response of the circuit is determined by the feedback network rather than the operational amplifier characteristics. The response of the operational amplifier circuit is characterized by the transfer function.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM741 is a general-purpose amplifier than can be used in a variety of applications and configurations. One common configuration is in a noninverting amplifier configuration. In this configuration, the output signal is in phase with the input (not inverted as in the inverting amplifier configuration), the input impedance of the amplifier is high, and the output impedance is low. The characteristics of the input and output impedance is beneficial for applications that require isolation between the input and output. No significant loading will occur from the previous stage before the amplifier. The gain of the system is set accordingly so the output signal is a factor larger than the input signal.

8.2 Typical Application

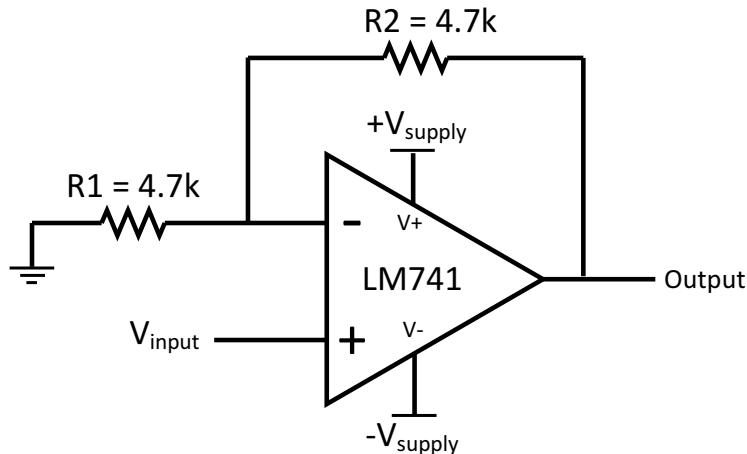


Figure 1. LM741 Noninverting Amplifier Circuit

8.2.1 Design Requirements

As shown in Figure 1, the signal is applied to the noninverting input of the LM741. The gain of the system is determined by the feedback resistor and input resistor connected to the inverting input. The gain can be calculated by Equation 1:

$$\text{Gain} = 1 + (R2/R1) \quad (1)$$

The gain is set to 2 for this application. R1 and R2 are 4.7-k resistors with 5% tolerance.

8.2.2 Detailed Design Procedure

The LM741 can be operated in either single supply or dual supply. This application is configured for dual supply with the supply rails at ± 15 V. The input signal is connected to a function generator. A 1-Vpp, 10-kHz sine wave was used as the signal input. 5% tolerance resistors were used, but if the application requires an accurate gain response, use 1% tolerance resistors.

Typical Application (continued)

8.2.3 Application Curve

The waveforms in [Figure 2](#) show the input and output signals of the LM741 non-inverting amplifier circuit. The blue waveform (top) shows the input signal, while the red waveform (bottom) shows the output signal. The input signal is 1.06 V_{pp} and the output signal is 1.94 V_{pp}. With the 4.7-k Ω resistors, the theoretical gain of the system is 2. Due to the 5% tolerance, the gain of the system including the tolerance is 1.992. The gain of the system when measured from the mean amplitude values on the oscilloscope was 1.83.

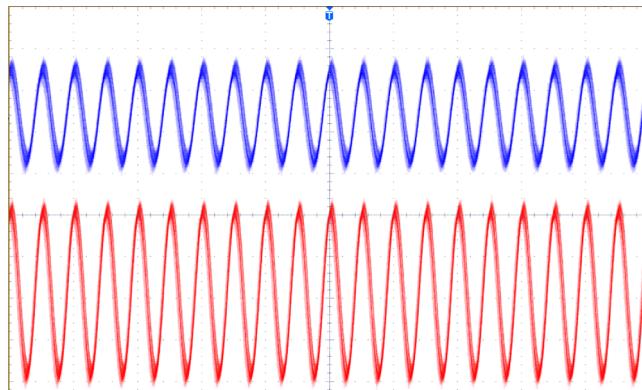


Figure 2. Waveforms for LM741 Noninverting Amplifier Circuit

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, a 0.1- μ F capacitor is recommended and should be placed as close as possible to the LM741 power supply pins.

10 Layout

10.1 Layout Guidelines

As with most amplifiers, take care with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize pick-up and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground. As shown in [Figure 3](#), the feedback resistors and the decoupling capacitors are located close to the device to ensure maximum stability and noise performance of the system.

10.2 Layout Example

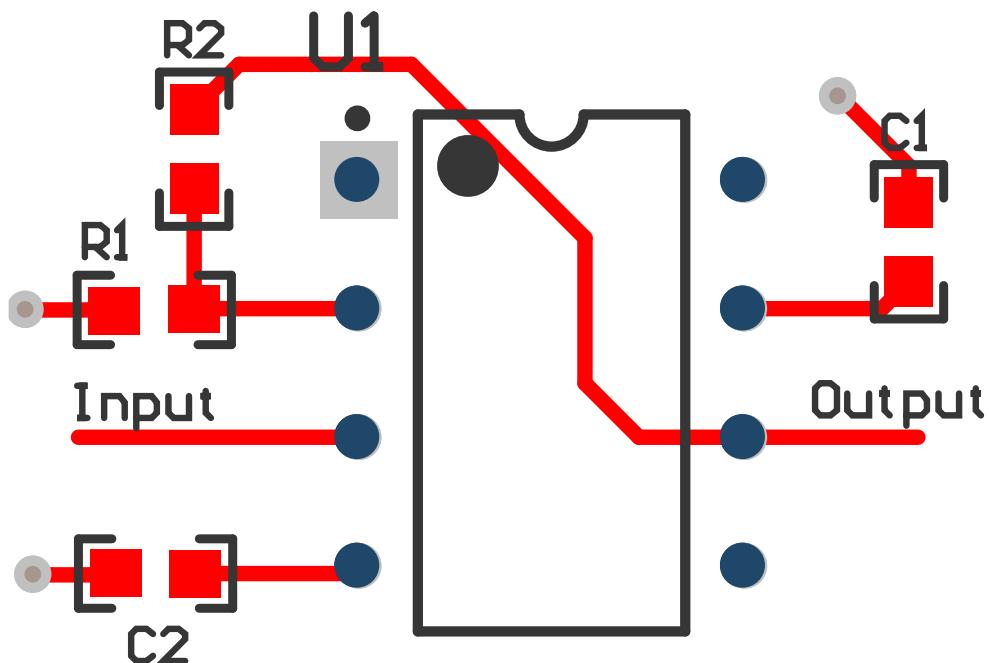


Figure 3. LM741 Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022 — TI Glossary.](#)

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C) (4/5)	Device Marking	Sample (7)
LM741C-MWC	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-40 to 85		Sample
LM741CN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	Call TI / SN	Level-1-NA-UNLIM	0 to 70	LM 741CN	Sample

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.**OBSOLETE:** TI has discontinued the production of the device.

(2) **Rohs:** TI defines "Rohs" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "Rohs" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a ";" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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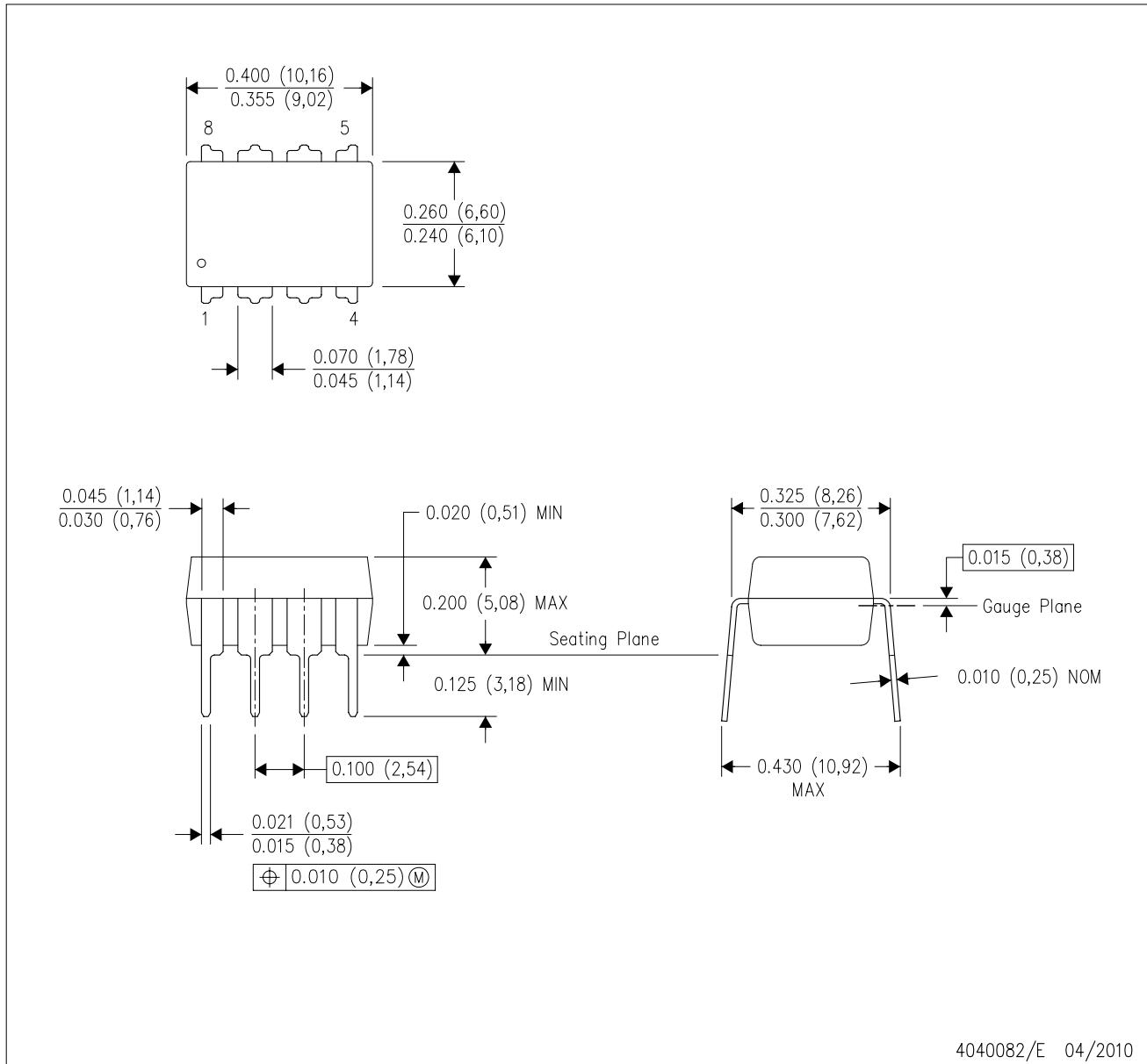
PACKAGE OPTION ADDENDUM

10-Dec-2020

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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TL07xx Low-Noise FET-Input Operational Amplifiers

1 Features

- High slew rate: 20 V/ μ s (TL07xH, typ)
- Low offset voltage: 1 mV (TL07xH, typ)
- Low offset voltage drift: 2 μ V/ $^{\circ}$ C
- Low power consumption: 940 μ A/ch (TL07xH, typ)
- Wide common-mode and differential voltage ranges
 - Common-mode input voltage range includes V_{CC+}
- Low input bias and offset currents
- Low noise:
 $V_n = 18 \text{ nV}/\sqrt{\text{Hz}}$ (typ) at $f = 1 \text{ kHz}$
- Output short-circuit protection
- Low total harmonic distortion: 0.003% (typ)
- Wide supply voltage:
 $\pm 2.25 \text{ V}$ to $\pm 20 \text{ V}$, 4.5 V to 40 V

2 Applications

- Solar energy: string and central inverter
- Motor drives: AC and servo drive control and power stage modules
- Single phase online UPS
- Three phase UPS
- Pro audio mixers
- Battery test equipment

3 Description

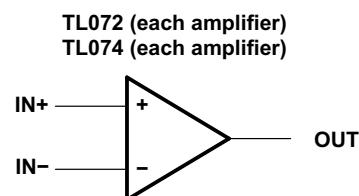
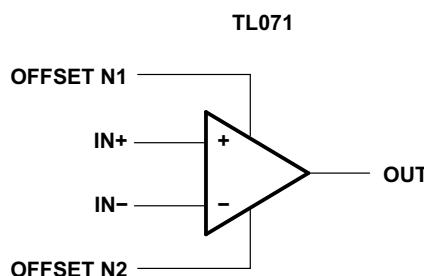
The TL07xH (TL071H, TL072H, and TL074H) family of devices are the next-generation versions of the industry-standard TL07x (TL071, TL072, and TL074) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1 mV, typical), high slew rate (20 V/ μ s), and common-mode input to the positive supply. High ESD

(1.5 kV, HBM), integrated EMI and RF filters, and operation across the full -40°C to 125°C enable the TL07xH devices to be used in the most rugged and demanding applications.

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
TL071x	PDIP (8)	9.59 mm \times 6.35 mm
	SC70 (5)	2.00 mm \times 1.25 mm
	SO (8)	6.20 mm \times 5.30 mm
	SOIC (8)	4.90 mm \times 3.90 mm
	SOT-23 (5)	1.60 mm \times 1.20 mm
TL072x	PDIP (8)	9.59 mm \times 6.35 mm
	SO (8)	6.20 mm \times 5.30 mm
	SOIC (8)	4.90 mm \times 3.90 mm
	SOT-23 (8)	2.90 mm \times 1.60 mm
	TSSOP (8)	4.40 mm \times 3.00 mm
	VSSOP (8)	3.00 mm \times 3.00 mm
TL072M	CDIP (8)	9.59 mm \times 6.67 mm
	CFP (10)	6.12 mm \times 3.56 mm
	LCCC (20)	8.89 mm \times 8.89 mm
TL074x	PDIP (14)	19.30 mm \times 6.35 mm
	SO (14)	10.30 mm \times 5.30 mm
	SOIC (14)	8.65 mm \times 3.91 mm
	SOT-23 (14)	4.20 mm \times 2.00 mm
	SSOP (14)	6.20 mm \times 5.30 mm
	TSSOP (14)	5.00 mm \times 4.40 mm
TL074M	CDIP (14)	19.56 mm \times 6.92 mm
	CFP (14)	9.21 mm \times 6.29 mm
	LCCC (20)	8.89 mm \times 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Logic Symbols



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features.....	1	6.23 Electrical Characteristics: TL071M, TL072M.....	22
2 Applications.....	1	6.24 Electrical Characteristics: TL074M.....	23
3 Description.....	1	6.25 Switching Characteristics: TL07xM.....	24
4 Revision History.....	2	6.26 Switching Characteristics: TL07xC, TL07xAC, TL07xBC, TL07xI.....	24
5 Pin Configuration and Functions.....	4	6.27 Electrical Characteristics, TL07xM.....	25
6 Specifications.....	10	6.28 Switching Characteristics.....	25
6.1 Absolute Maximum Ratings: TL07xH	10	6.29 Typical Characteristics: TL07xH.....	26
6.2 Absolute Maximum Ratings: All Devices Except TL07xH.....	10	6.30 Typical Characteristics: All Devices Except TL07xH.....	33
6.3 ESD Ratings: TL07xH	10	7 Parameter Measurement Information.....	37
6.4 ESD Ratings: All Devices Except TL07xH.....	11	8 Detailed Description.....	38
6.5 Recommended Operating Conditions: TL07xH	11	8.1 Overview.....	38
6.6 Recommended Operating Conditions: All Devices Except TL07xH.....	11	8.2 Functional Block Diagram.....	38
6.7 Thermal Information for Single Channel: TL071H	11	8.3 Feature Description.....	39
6.8 Thermal Information: TL071x.....	12	8.4 Device Functional Modes.....	39
6.9 Thermal Information for Dual Channel: TL072H	12	9 Application and Implementation.....	40
6.10 Thermal Information: TL072x.....	12	9.1 Application Information.....	40
6.11 Thermal Information: TL072x (cont.).....	13	9.2 Typical Application.....	40
6.12 Thermal Information for Quad Channel: TL074H	13	9.3 Unity Gain Buffer.....	41
6.13 Thermal Information: TL074x.....	13	9.4 System Examples.....	42
6.14 Thermal Information: TL074x (cont).....	14	10 Power Supply Recommendations.....	43
6.15 Thermal Information: TL074x (cont).....	14	11 Layout.....	43
6.16 Thermal Information.....	14	11.1 Layout Guidelines.....	43
6.17 Electrical Characteristics: TL07xH	15	11.2 Layout Example.....	44
6.18 Electrical Characteristics: TL071C, TL072C, TL074C.....	17	12 Device and Documentation Support.....	45
6.19 Electrical Characteristics: TL071AC, TL072AC, TL074AC.....	18	12.1 Related Links.....	45
6.20 Electrical Characteristics: TL071BC, TL072BC, TL074BC.....	19	12.2 Receiving Notification of Documentation Updates.....	45
6.21 Electrical Characteristics: TL071I, TL072I, TL074I.....	20	12.3 Support Resources.....	45
6.22 Electrical Characteristics, TL07xC, TL07xAC, TL07xBC, TL07xI.....	21	12.4 Trademarks.....	45

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (October 2020) to Revision P (November 2020)	Page
• Added SOIC and TSSOP package thermal information in <i>Thermal Information for Quad Channel: TL074H section</i>	13
• Added <i>Typical Characteristics: TL07xH</i> section in <i>Specifications</i> section.....	26

Changes from Revision N (July 2017) to Revision O (October 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Features of TL07xH added to the <i>Features</i> section.....	1
• Added link to applications in the <i>Applications</i> section.....	1
• Added TL07xH in the <i>Description</i> section.....	1
• Added TL07xH device in the <i>Device Information</i> section.....	1
• Added SOT-23 (14), VSSOP (8), SOT-23 (8), SC70 (5), and SOT-23 (5) packages to the <i>Device Information</i> section.....	1
• Added TSSOP, VSSOP and DDF packages to TL072x in <i>Pin Configuration and Functions</i> section.....	4

• Added DYY package to TL074x in <i>Pin Configuration and Functions</i> section.....	4
• Removed Table of Graphs from the <i>Typical Characteristics</i> section.....	33
• Deleted reference to obsolete documentation in <i>Layout Guidelines</i> section.....	43
• Removed <i>Related Documentation</i> section.....	45

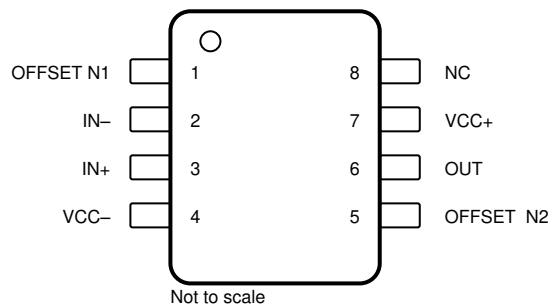
Changes from Revision M (February 2014) to Revision N (July 2017)	Page
• Updated data sheet text to latest documentation and translation standards.....	1
• Added TL072M and TL074M devices to data sheet	1
• Rewrote text in <i>Description</i> section	1
• Changed TL07x 8-pin PDIP package to 8-pin CDIP package in <i>Device Information</i> table	1
• Deleted 20-pin LCCC package from <i>Device Information</i> table	1
• Added 2017 copyright statement to front page schematic.....	1
• Deleted TL071x FK (LCCC) pinout drawing and pinout table in <i>Pin Configurations and Functions</i> section	4
• Updated pinout diagrams and pinout tables in <i>Pin Configurations and Functions</i> section	4
• Deleted differential input voltage parameter from <i>Absolute Maximum Ratings</i> table	10
• Deleted table notes from <i>Absolute Maximum Ratings</i> table	10
• Added new table note to <i>Absolute Maximum Ratings</i> table	10
• Changed minimum supply voltage value from –18 V to –0.3 V in <i>Absolute Maximum Ratings</i> table.....	10
• Changed maximum supply voltage from 18 V to 36 V in <i>Absolute Maximum Ratings</i> table.....	10
• Changed minimum input voltage value from –15 V to $V_{CC} - 0.3$ V in <i>Absolute Maximum Ratings</i> table.....	10
• Changed maximum input voltage from 15 V to $V_{CC} + 36$ V in <i>Absolute Maximum Ratings</i> table.....	10
• Added input clamp current parameter to <i>Absolute Maximum Ratings</i> table	10
• Changed common-mode voltage maximum value from $V_{CC+} - 4$ V to V_{CC+} in the <i>Recommended Operating Conditions</i> table.....	11
• Changed devices in <i>Recommended Operating Conditions</i> table from TL07xA and TL07xB to TL07xAC and TL07xBC	11
• Added TL07xl operating free-air temperature minimum value of –40°C to <i>Recommended Operating Conditions</i> table	11
• Added U (CFP) package thermal values to <i>Thermal Information: TL072x (cont.)</i> table.....	13
• Added W (CFP) package thermal values to <i>Thermal Information: TL074x (cont.)</i> table.....	14
• Added Figure 6-59 to <i>Typical Characteristics</i> section.....	33
• Added second <i>Typical Application</i> section application curves	41
• Reformatted document references in <i>Layout Guidelines</i> section	43

Changes from Revision L (February 2014) to Revision M (February 2014)	Page
• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section.....	1

Changes from Revision K (January 2014) to Revision L (February 2014)	Page
• Moved T_{stg} to <i>Handling Ratings</i> table	11

Changes from Revision J (March 2005) to Revision K (January 2014)	Page
• Updated document to new TI datasheet format - no specification changes.....	1

5 Pin Configuration and Functions

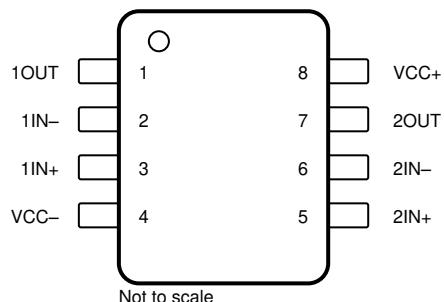


NC- no internal connection

**Figure 5-1. TL071x D, P, and PS Package
8-Pin SOIC, PDIP, and SO
Top View**

Table 5-1. Pin Functions: TL071x

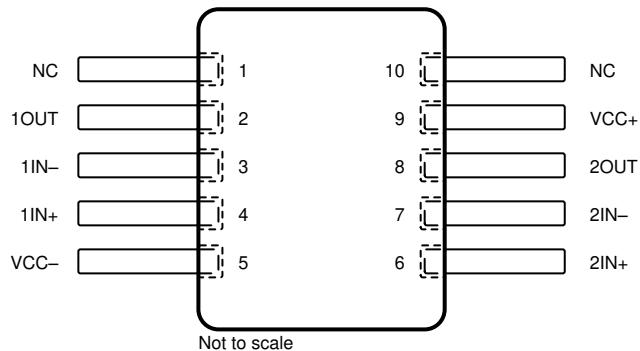
PIN		I/O	DESCRIPTION
NAME	NO.		
IN-	2	I	Inverting input
IN+	3	I	Noninverting input
NC	8	—	Do not connect
OFFSET N1	1	—	Input offset adjustment
OFFSET N2	5	—	Input offset adjustment
OUT	6	O	Output
VCC-	4	—	Power supply
VCC+	7	—	Power supply



**Figure 5-2. TL072x D, DDF, DGK, JG, P, PS, and PW Package
8-Pin SOIC, SOT-23 (8), VSSOP, CDIP, PDIP, SO, and TSSOP
Top View**

Table 5-2. Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN-	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN-	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
VCC-	4	—	Power supply
VCC+	8	—	Power supply

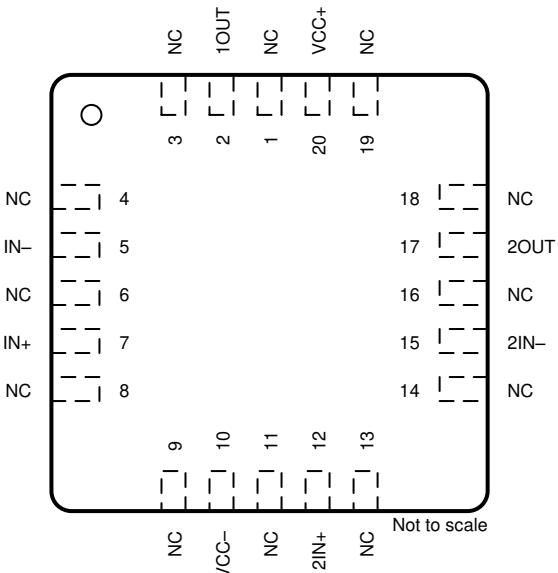


NC- no internal connection

**Figure 5-3. TL072x U Package
10-Pin CFP
Top View**

Table 5-3. Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN-	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN-	7	I	Inverting input
2IN+	6	I	Noninverting input
2OUT	8	O	Output
NC	1, 10	—	Do not connect
VCC-	5	—	Power supply
VCC+	9	—	Power supply



NC- no internal connection

**Figure 5-4. TL072 FK Package
20-Pin LCCC
Top View**

Table 5-4. Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN-	5	I	Inverting input
1IN+	7	I	Noninverting input
1OUT	2	O	Output
2IN-	15	I	Inverting input
2IN+	12	I	Noninverting input
2OUT	17	O	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC-	10	—	Power supply
VCC+	20	—	Power supply

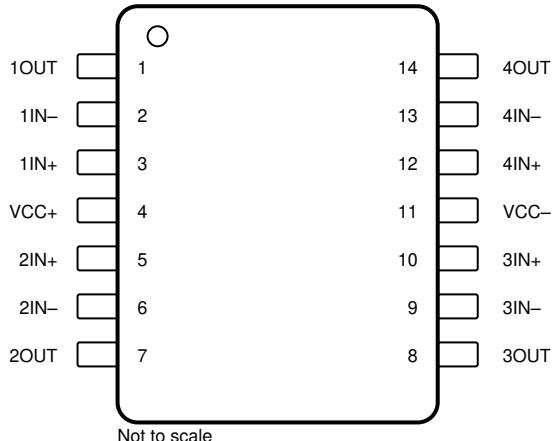
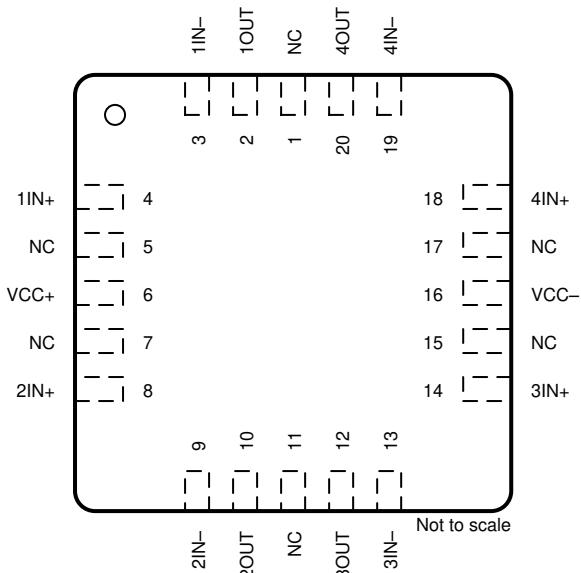


Figure 5-5. TL074x D, N, NS, PW, J, DYY, and W Packages
14-Pin SOIC, PDIP, SO, TSSOP, CDIP, SOT-23 (14), and CFP
Top View

Table 5-5. Pin Functions: TL074x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN-	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN-	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
3IN-	9	I	Inverting input
3IN+	10	I	Noninverting input
3OUT	8	O	Output
4IN-	13	I	Inverting input
4IN+	12	I	Noninverting input
4OUT	14	O	Output
V _{CC} -	11	—	Power supply
V _{CC} +	4	—	Power supply



NC- no internal connection

**Figure 5-6. TL074 FK Package
20-Pin LCCC
Top View**

Table 5-6. Pin Functions: TL074x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN-	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN-	9	I	Inverting input
2IN+	8	I	Noninverting input
2OUT	10	O	Output
3IN-	13	I	Inverting input
3IN+	14	I	Noninverting input
3OUT	12	O	Output
4IN-	19	I	Inverting input
4IN+	18	I	Noninverting input
4OUT	20	O	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC-	16	—	Power supply
VCC+	6	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings: TL07xH

over operating ambient temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, $V_S = (V_{CC+}) - (V_{CC-})$		0	42	V
Signal input pins	Common-mode voltage ⁽³⁾	$(V_{CC-}) - 0.5$	$(V_{CC+}) + 0.5$	V
	Differential voltage ⁽³⁾		$V_S + 0.2$	V
	Current ⁽³⁾	-10	10	mA
Output short-circuit ⁽²⁾		Continuous		
Operating ambient temperature, T_A		-55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.
- (3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

6.2 Absolute Maximum Ratings: All Devices Except TL07xH

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage	-0.3	36	V
V_I	Input voltage ⁽³⁾	$V_{CC-} - 0.3$	$V_{CC-} + 36$	V
I_{IK}	Input clamp current		-50	mA
	Duration of output short circuit ⁽²⁾	Unlimited		
T_J	Operating virtual junction temperature		150	°C
	Case temperature for 60 seconds - FK package		260	°C
	Lead temperature 1.8 mm (1/16 inch) from case for 10 seconds		300	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The output may be shorted to ground or to either supply. Temperature and supply voltages must be limited to ensure that the dissipation rating is not exceeded.
- (3) Differential voltage only limited by input voltage.

6.3 ESD Ratings: TL07xH

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 ESD Ratings: All Devices Except TL07xH

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.5 Recommended Operating Conditions: TL07xH

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _S	Supply voltage, (V _{CC+}) – (V _{CC-})	4.5	40	V
V _I	Input voltage range	(V _{CC-}) + 2	(V _{CC+}) + 0.1	V
T _A	Specified temperature	–40	125	°C

6.6 Recommended Operating Conditions: All Devices Except TL07xH

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC+}	Supply voltage ⁽¹⁾	5	15	V
V _{CC-}	Supply voltage ⁽¹⁾	–5	–15	V
V _{CM}	Common-mode voltage	V _{CC-} + 4	V _{CC+}	V
T _A	Operating free-air temperature	TL07xM	–55	125
		TL08xQ	–40	125
		TL07xI	–40	85
		TL07xAC, TL07xBC, TL07xC	0	70

(1) V_{CC+} and V_{CC-} are not required to be of equal magnitude, provided that the total V_{CC} (V_{CC+} – V_{CC-}) is between 10 V and 30 V.

6.7 Thermal Information for Single Channel: TL071H

THERMAL METRIC ⁽¹⁾		TL071H		UNIT
		D ⁽²⁾ (SOIC)	DBV ⁽²⁾ (SOT-23)	
		8 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	TBD	TBD	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) This package option is preview for TL071H.

6.8 Thermal Information: TL071x

THERMAL METRIC ⁽¹⁾		TL071x			UNIT
		D (SOIC)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	97	85	95	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	—	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.9 Thermal Information for Dual Channel: TL072H

THERMAL METRIC ⁽¹⁾		TL072H			UNIT
		D ⁽²⁾ (SOIC)	DGK ⁽²⁾ (VSSOP)	PW ⁽²⁾ (TSSOP)	
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	TBD	TBD	TBD	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	TBD	TBD	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	TBD	TBD	TBD	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	TBD	TBD	TBD	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	TBD	TBD	TBD	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	TBD	TBD	TBD	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report, [SPRA953](#).
- (2) This package option is preview for TL072H.

6.10 Thermal Information: TL072x

THERMAL METRIC ⁽¹⁾		TL072x				UNIT
		D (SOIC)	JG (CDIP)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	97	—	85	95	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	—	15.05	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.11 Thermal Information: TL072x (cont.)

THERMAL METRIC ⁽¹⁾	TL072x			UNIT
	PW (TSSOP)	U (CFP)	FK (LCCC)	
	8 PINS	10 PINS	20 PINS	
R _{θJA} Junction-to-ambient thermal resistance	150	169.8	—	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	—	62.1	5.61	°C/W
R _{θJB} Junction-to-board thermal resistance	—	176.2	—	°C/W
Ψ _{JT} Junction-to-top characterization parameter	—	48.4	—	°C/W
Ψ _{JB} Junction-to-board characterization parameter	—	144.1	—	°C/W
R _{θJC(bot)} Junction-to-case (bottom) thermal resistance	—	5.4	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.12 Thermal Information for Quad Channel: TL074H

THERMAL METRIC ⁽¹⁾	TL074H			UNIT
	D (SOIC)	PW (TSSOP)		
	14 PINS	14 PINS		
R _{θJA} Junction-to-ambient thermal resistance	114.2	134.4	°C/W	
R _{θJC(top)} Junction-to-case (top) thermal resistance	70.3	62.6	°C/W	
R _{θJB} Junction-to-board thermal resistance	70.2	77.6	°C/W	
Ψ _{JT} Junction-to-top characterization parameter	28.8	13.0	°C/W	
Ψ _{JB} Junction-to-board characterization parameter	69.8	77.0	°C/W	
R _{θJC(bot)} Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report, [SPRA953](#).

6.13 Thermal Information: TL074x

THERMAL METRIC ⁽¹⁾	TL074x			UNIT
	D (SOIC)	N (PDIP)	NS (SO)	
	14 PINS	14 PINS	14 PINS	
R _{θJA} Junction-to-ambient thermal resistance	86	80	76	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.14 Thermal Information: TL074x (cont).

THERMAL METRIC ⁽¹⁾		TL074x			UNIT
		J (CDIP)	PW (TSSOP)	W (CFP)	
		14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	—	113	128.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	14.5	—	56.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	—	—	127.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	—	—	29	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	—	—	106.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	0.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.15 Thermal Information: TL074x (cont.).

THERMAL METRIC ⁽¹⁾		TL074x		UNIT	
		FK (LCCC)			
		20 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	—	—	°C/W	
R _{θJC(top)}	Junction-to-case (top) thermal resistance	5.61	—	°C/W	

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.16 Thermal Information

THERMAL METRIC ⁽¹⁾	TL071/TL072/TL074										UNIT	
	D (SOIC)		FK (LCCC)	J (CDIP)		N (PDIP)		NS (SO)		PW (TSSOP)		
	8 PINS	14 PINS	20 PINS	8 PINS	14 PINS	8 PINS	14 PINS	8 PINS	14 PINS	8 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	97	86	—	—	—	85	80	95	76	150	113 °C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	—	—	5.61	15.05	14.5	—	—	—	—	—	— °C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.17 Electrical Characteristics: TL07xH

For $V_S = (V_{CC+}) - (V_{CC-}) = 4.5 \text{ V}$ to 40 V ($\pm 2.25 \text{ V}$ to $\pm 20 \text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O\ UT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage		$T_A = -40^\circ\text{C}$ to 125°C	± 1	± 4	μV	
					± 5		
dV _{OS} /dT	Input offset voltage drift		$T_A = -40^\circ\text{C}$ to 125°C		± 2		$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage versus power supply	$V_S = 5 \text{ V}$ to 40 V , $V_{CM} = V_S / 2$	$T_A = -40^\circ\text{C}$ to 125°C		± 1	± 10	$\mu\text{V/V}$
	Channel separation	$f = 0 \text{ Hz}$			10		$\mu\text{V/V}$
INPUT BIAS CURRENT							
I _B	Input bias current		$T_A = -40^\circ\text{C}$ to 125°C (1)	± 1	± 120	pA	
					± 5		
I _{os}	Input offset current		$T_A = -40^\circ\text{C}$ to 125°C (1)		± 0.5	± 120	pA
						± 5	nA
NOISE							
E _N	Input voltage noise	$f = 0.1 \text{ Hz}$ to 10 Hz			9.2	μV_{PP}	
					1.4		
e _N	Input voltage noise density	$f = 1 \text{ kHz}$			37	$\text{nV}/\sqrt{\text{Hz}}$	
					21		
i _N	Input current noise	$f = 1 \text{ kHz}$			80		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range			$(V_{CC-}) + 1.5$	(V_{CC+})		V
CMRR	Common-mode rejection ratio	$V_S = 40 \text{ V}$, $(V_{CC-}) + 2.5 \text{ V} < V_{CM} < (V_{CC+}) - 1.5 \text{ V}$		100	105		dB
CMRR	Common-mode rejection ratio		$T_A = -40^\circ\text{C}$ to 125°C		95		dB
CMRR	Common-mode rejection ratio	$V_S = 40 \text{ V}$, $(V_{CC-}) + 2.5 \text{ V} < V_{CM} < (V_{CC+})$			90	105	dB
CMRR	Common-mode rejection ratio		$T_A = -40^\circ\text{C}$ to 125°C		80		dB
INPUT CAPACITANCE							
Z _{ID}	Differential				100 2		$\text{M}\Omega \text{pF}$
Z _{ICM}	Common-mode				6 1		$\text{T}\Omega \text{pF}$
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	$V_S = 40 \text{ V}$, $V_{CM} = V_S / 2$, $(V_{CC-}) + 0.3 \text{ V} < V_O < (V_{CC+}) - 0.3 \text{ V}$	$T_A = -40^\circ\text{C}$ to 125°C	118	125		dB
A _{OL}	Open-loop voltage gain	$V_S = 40 \text{ V}$, $V_{CM} = V_S / 2$, $R_L = 2 \text{ k}\Omega$, $(V_{CC-}) + 1.2 \text{ V} < V_O < (V_{CC+}) - 1.2 \text{ V}$	$T_A = -40^\circ\text{C}$ to 125°C	115	120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.25		MHz
SR	Slew rate	$V_S = 40 \text{ V}$, $G = +1$, $C_L = 20 \text{ pF}$			20		$\text{V}/\mu\text{s}$

For $V_S = (V_{CC+}) - (V_{CC-}) = 4.5 \text{ V}$ to 40 V ($\pm 2.25 \text{ V}$ to $\pm 20 \text{ V}$) at $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O_UT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_S	Settling time	To 0.1%, $V_S = 40 \text{ V}$, $V_{STEP} = 10 \text{ V}$, $G = +1$, $CL = 20 \text{ pF}$		0.63		μs
		To 0.1%, $V_S = 40 \text{ V}$, $V_{STEP} = 2 \text{ V}$, $G = +1$, $CL = 20 \text{ pF}$		0.56		
		To 0.01%, $V_S = 40 \text{ V}$, $V_{STEP} = 10 \text{ V}$, $G = +1$, $CL = 20 \text{ pF}$		0.91		
		To 0.01%, $V_S = 40 \text{ V}$, $V_{STEP} = 2 \text{ V}$, $G = +1$, $CL = 20 \text{ pF}$		0.48		
	Phase margin	$G = +1$, $R_L = 10\text{k}\Omega$, $C_L = 20 \text{ pF}$		56		°
	Overload recovery time	$V_{IN} \times \text{gain} > V_S$		300		ns
THD+N	Total harmonic distortion + noise	$V_S = 40 \text{ V}$, $V_O = 6 \text{ V}_{RMS}$, $G = +1$, $f = 1 \text{ kHz}$		0.00012		%
EMIRR	EMI rejection ratio	$f = 1 \text{ GHz}$		53		dB

OUTPUT

	Voltage output swing from rail	Positive rail headroom	$V_S = 40 \text{ V}$, $R_L = 10 \text{ k}\Omega$	115	210	mV
			$V_S = 40 \text{ V}$, $R_L = 2 \text{ k}\Omega$	520	965	
		Negative rail headroom	$V_S = 40 \text{ V}$, $R_L = 10 \text{ k}\Omega$	105	215	
			$V_S = 40 \text{ V}$, $R_L = 2 \text{ k}\Omega$	500	1030	
I_{SC}	Short-circuit current			±26		mA
C_{LOAD}	Capacitive load drive			300		pF
Z_O	Open-loop output impedance	$f = 1 \text{ MHz}$, $I_O = 0 \text{ A}$		125		Ω

POWER SUPPLY

I_Q	Quiescent current per amplifier	$I_O = 0 \text{ A}$		937.5	1125	μA
			$T_A = -40^\circ\text{C}$ to 125°C		1130	
Turn-On Time		At $T_A = 25^\circ\text{C}$, $V_S = 40 \text{ V}$, V_S ramp rate $> 0.3 \text{ V}/\mu\text{s}$		60		μs

(1) Max I_B and I_{os} data is specified based on characterization results.

6.18 Electrical Characteristics: TL071C, TL072C, TL074C

$V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS ^{(1) (2)}		MIN	TYP	MAX	UNIT	
V_{IO} Input offset voltage	$V_O = 0$	$T_A = 25^\circ C$		3	10	mV	
	$R_S = 50 \Omega$	$T_A = \text{Full range}$			13		
α Temperature coefficient of input offset voltage	$V_O = 0$	$T_A = \text{Full range}$		18		$\mu V/^\circ C$	
I_{IO} Input offset current	$R_S = 50 \Omega$	$T_A = 25^\circ C$		5	100	pA	
		$T_A = \text{Full range}$			10	nA	
I_{IB} Input bias current ⁽³⁾	$V_O = 0$	$T_A = 25^\circ C$		65	200	pA	
		$T_A = \text{Full range}$			7	nA	
V_{ICR} Common-mode input voltage range	$T_A = 25^\circ C$		± 11	$-12 \text{ to } 15$		V	
V_{OM} Maximum peak output voltage swing	$R_L = 10 k\Omega$	$T_A = 25^\circ C$	± 12	± 13.5		V	
	$R_L \geq 10 k\Omega$	$T_A = \text{Full range}$	± 12				
	$R_L \geq 2 k\Omega$		± 10				
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10 V$	$T_A = 25^\circ C$	25	200		V/mV	
	$R_L \geq 2 k\Omega$	$T_A = \text{Full range}$	15				
B_1 Utility-gain bandwidth	$T_A = 25^\circ C$			3		MHz	
r_I Input resistance	$T_A = 25^\circ C$			10^{12}		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR(\min)}$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	70	100		dB	
k_{SVR} Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9 V \text{ to } \pm 15 V$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	70	100		dB	
I_{CC} Supply current (each amplifier)	$V_O = 0$; no load	$T_A = 25^\circ C$		1.4	2.5	mA	
V_{O1} / V_{O2} Crosstalk attenuation	$A_{VD} = 100$	$T_A = 25^\circ C$		120		dB	

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

(2) Full range is $T_A = 0^\circ C$ to $70^\circ C$.

(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 6-40](#). Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.19 Electrical Characteristics: TL071AC, TL072AC, TL074AC

$V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT	
V_{IO} Input offset voltage	$V_O = 0$	$T_A = 25^\circ C$		3	6	mV	
	$R_S = 50 \Omega$	$T_A = \text{Full range}$			7.5		
α Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50 \Omega$	$T_A = \text{Full range}$		18		$\mu V/^\circ C$	
I_{IO} Input offset current	$V_O = 0$	$T_A = 25^\circ C$		5	100	pA	
		$T_A = \text{Full range}$			2	nA	
I_{IB} Input bias current ⁽³⁾	$V_O = 0$	$T_A = 25^\circ C$		65	200	pA	
		$T_A = \text{Full range}$			7	nA	
V_{ICR} Common-mode input voltage range	$T_A = 25^\circ C$		± 11	$-12 \text{ to } 15$		V	
V_{OM} Maximum peak output voltage swing	$R_L = 10 \text{ k}\Omega$	$T_A = 25^\circ C$	± 12	± 13.5		V	
	$R_L \geq 10 \text{ k}\Omega$	$T_A = \text{Full range}$	± 12				
	$R_L \geq 2 \text{ k}\Omega$		± 10				
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10 \text{ V}$ $R_L \geq 2 \text{ k}\Omega$	$T_A = 25^\circ C$	50	200		V/mV	
		$T_A = \text{Full range}$	25				
B_1 Utility-gain bandwidth	$T_A = 25^\circ C$			3		MHz	
r_I Input resistance	$T_A = 25^\circ C$			10^{12}		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR(\min)}$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	75	100		dB	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC} = \pm 9 \text{ V to } \pm 15 \text{ V}$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	80	100		dB	
I_{CC} Supply current (each amplifier)	$V_O = 0$; no load	$T_A = 25^\circ C$		1.4	2.5	mA	
V_{O1} / V_{O2} Crosstalk attenuation	$A_{VD} = 100$	$T_A = 25^\circ C$		120		dB	

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

(2) Full range is $T_A = 0^\circ C$ to $70^\circ C$.

(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 6-40](#). Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.20 Electrical Characteristics: TL071BC, TL072BC, TL074BC

$V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT	
V_{IO} Input offset voltage	$V_O = 0$	$T_A = 25^\circ C$		2	3	mV	
	$R_S = 50 \Omega$	$T_A = \text{Full range}$			5		
α Temperature coefficient of input offset voltage	$V_O = 0$	$T_A = \text{Full range}$		18		$\mu V/^\circ C$	
I_{IO} Input offset current	$V_O = 0$	$T_A = 25^\circ C$		5	100	pA	
		$T_A = \text{Full range}$			2	nA	
I_{IB} Input bias current (3)	$V_O = 0$	$T_A = 25^\circ C$		65	200	pA	
		$T_A = \text{Full range}$			7	nA	
V_{ICR} Common-mode input voltage range	$T_A = 25^\circ C$		± 11	$-12 \text{ to } 15$		V	
V_{OM} Maximum peak output voltage swing	$R_L = 10 k\Omega$	$T_A = 25^\circ C$	± 12	± 13.5		V	
	$R_L \geq 10 k\Omega$	$T_A = \text{Full range}$	± 12				
	$R_L \geq 2 k\Omega$		± 10				
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10 V$	$T_A = 25^\circ C$	50	200		V/mV	
		$T_A = \text{Full range}$		25			
B_1 Utility-gain bandwidth	$T_A = 25^\circ C$			3		MHz	
r_I Input resistance	$T_A = 25^\circ C$			10^{12}		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR(\min)}$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	75	100		dB	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9 V \text{ to } \pm 15 V$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	80	100		dB	
I_{CC} Supply current (each amplifier)	$V_O = 0$; no load	$T_A = 25^\circ C$		1.4	2.5	mA	
V_{O1} / V_{O2} Crosstalk attenuation	$A_{VD} = 100$	$T_A = 25^\circ C$		120		dB	

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

(2) Full range is $T_A = 0^\circ C$ to $70^\circ C$.

(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 6-40](#). Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.21 Electrical Characteristics: TL071I, TL072I, TL074I

$V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT	
V_{IO} Input offset voltage	$V_O = 0$	$T_A = 25^\circ C$		3	6	mV	
	$R_S = 50 \Omega$	$T_A = \text{Full range}$			8		
α Temperature coefficient of input offset voltage	$V_O = 0$	$T_A = \text{Full range}$		18		$\mu V/^\circ C$	
I_{IO} Input offset current	$R_S = 50 \Omega$	$T_A = 25^\circ C$		5	100	pA	
		$T_A = \text{Full range}$			2	nA	
I_{IB} Input bias current (3)	$V_O = 0$	$T_A = 25^\circ C$		65	200	pA	
		$T_A = \text{Full range}$			7	nA	
V_{ICR} Common-mode input voltage range	$T_A = 25^\circ C$		± 11	-12 to 15		V	
V_{OM} Maximum peak output voltage swing	$R_L = 10 k\Omega$	$T_A = 25^\circ C$	± 12	± 13.5		V	
	$R_L \geq 10 k\Omega$	$T_A = \text{Full range}$	± 12				
	$R_L \geq 2 k\Omega$		± 10				
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10 V$	$T_A = 25^\circ C$	50	200		V/mV	
	$R_L \geq 2 k\Omega$	$T_A = \text{Full range}$	25				
B_1 Utility-gain bandwidth	$T_A = 25^\circ C$			3		MHz	
r_I Input resistance	$T_A = 25^\circ C$			10^{12}		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR(\min)}$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	75	100		dB	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9 V$ to $\pm 15 V$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	80	100		dB	
I_{CC} Supply current (each amplifier)	$V_O = 0$; no load	$T_A = 25^\circ C$		1.4	2.5	mA	
V_{O1} / V_{O2} Crosstalk attenuation	$A_{VD} = 100$	$T_A = 25^\circ C$		120		dB	

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

(2) $T_A = -40^\circ C$ to $85^\circ C$.

(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-40. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.22 Electrical Characteristics, TL07xC, TL07xAC, TL07xBC, TL07xI

$V_{CC} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	T_A ⁽²⁾	TL071C, TL072C, TL074C			TL071AC, TL072AC, TL074AC			TL071BC, TL072BC, TL074BC			TL071I, TL072I, TL074I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage $V_O = 0$, $R_S = 50 \Omega$	25°C	3	10	13	3	6	7.5	2	3	5	3	6	8	mV
		Full range													
ΔV_{IO}	Temperature coefficient of input offset voltage $V_O = 0$, $R_S = 50 \Omega$	Full range		18			18			18			18		μV/°C
I_{IO}	Input offset current $V_O = 0$	25°C	5	100	10	5	100	2	5	100	2	5	100	2	pA
		Full range													nA
I_{IB}	Input bias current ⁽³⁾ $V_O = 0$	25°C	65	200	7	65	200	7	65	200	7	65	200	7	pA
		Full range													nA
V_{ICR}	Common-mode input voltage range	25°C	±11	-12 to 15		±11	-12 to 15		±11	-12 to 15		±11	-12 to 15		V
V_{OM}	Maximum peak output voltage swing $R_L = 10 \text{ k}\Omega$	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		$R_L \geq 10 \text{ k}\Omega$			±12		±12		±12		±12		±12		
		$R_L \geq 2 \text{ k}\Omega$			±10		±10		±10		±10		±10		
A_{VD}	Large-signal differential voltage amplification $V_O = \pm 10 \text{ V}$, $R_L \geq 2 \text{ k}\Omega$	25°C	25	200	15	50	200	25	50	200	25	50	200		V/mV
		Full range													
B_1	Utility-gain bandwidth	25°C		3			3			3			3		MHz
r_I	Input resistance	25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio $V_{IC} = V_{ICR\min}$, $V_O = 0$, $R_S = 50 \Omega$	25°C	70	100	75	100	75	100	75	100	75	100	75	100	dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_O$) $V_{CC} = \pm 9 \text{ V to } \pm 15 \text{ V}$, $V_O = 0$, $R_S = 50 \Omega$	25°C	70	100	80	100	80	100	80	100	80	100	80	100	dB
I_{CC}	Supply current (each amplifier) $V_O = 0$, No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation $A_{VD} = 100$	25°C		120			120			120			120		dB

- (1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
- (2) Full range is $T_A = 0^\circ\text{C}$ to 70°C for TL07_C, TL07_AC, TL07_BC and is $T_A = -40^\circ\text{C}$ to 85°C for TL07_I.
- (3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-40. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.23 Electrical Characteristics: TL071M, TL072M

$V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT	
V_{IO} Input offset voltage	$V_O = 0$	$T_A = 25^\circ C$		3	6	mV	
	$R_S = 50 \Omega$	$T_A = \text{Full range}$			9		
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 0$	$T_A = \text{Full range}$		18		$\mu V/^\circ C$	
I_{IO} Input offset current	$V_O = 0$	$T_A = 25^\circ C$		5	100	pA	
		$T_A = \text{Full range}$			20	nA	
I_{IB} Input bias current	$V_O = 0$	$T_A = 25^\circ C$		65	200	pA	
		$T_A = \text{Full range}$			50	nA	
V_{ICR} Common-mode input voltage range	$T_A = 25^\circ C$		± 11 to -12 to 15			V	
V_{OM} Maximum peak output voltage swing	$R_L = 10 k\Omega$	$T_A = 25^\circ C$	± 12	± 13.5		V	
	$R_L \geq 10 k\Omega$	$T_A = \text{Full range}$	± 12				
	$R_L \geq 2 k\Omega$		± 10				
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10 V$	$T_A = 25^\circ C$	35	200		V/mV	
		$T_A = \text{Full range}$	15				
B_1 Unity-gain bandwidth				3		MHz	
r_i Input resistance				10^{12}		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR(\min)}$, $V_O = 0$, $R_S = 50 \Omega$	$T_A = 25^\circ C$	80	86		dB	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9 V$ to $\pm 15 V$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	80	86		dB	
I_{CC} Supply current (each amplifier)	$V_O = 0$; no load	$T_A = 25^\circ C$		1.4	2.5	mA	
V_{O1} / V_{O2} Crosstalk attenuation	$A_{VD} = 100$	$T_A = 25^\circ C$		120		dB	

- (1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 6-40](#). Pulse techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.
- (2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is $T_A = -55^\circ C$ to $+125^\circ C$.

6.24 Electrical Characteristics: TL074M

$V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT	
V_{IO} Input offset voltage	$V_O = 0$	$T_A = 25^\circ C$		3	9	mV	
	$R_S = 50 \Omega$	$T_A = \text{Full range}$			15		
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50 \Omega$	$T_A = \text{Full range}$		18		$\mu V/^\circ C$	
I_{IO} Input offset current	$V_O = 0$	$T_A = 25^\circ C$		5	100	pA	
		$T_A = \text{Full range}$			20	nA	
I_{IB} Input bias current	$V_O = 0$	$T_A = 25^\circ C$		65	200	pA	
		$T_A = \text{Full range}$			20	nA	
V_{ICR} Common-mode input voltage range	$T_A = 25^\circ C$		± 11	-12 to 15		V	
V_{OM} Maximum peak output voltage swing	$R_L = 10 k\Omega$	$T_A = 25^\circ C$	± 12	± 13.5		V	
	$R_L \geq 10 k\Omega$	$T_A = \text{Full range}$	± 12				
	$R_L \geq 2 k\Omega$		± 10				
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10 V$ $R_L \geq 2 k\Omega$	$T_A = 25^\circ C$	35	200		V/mV	
		$T_A = \text{Full range}$	15				
B_1 Unity-gain bandwidth				3		MHz	
r_i Input resistance				10^{12}		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR(\min)}$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	80	86		dB	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9 V$ to $\pm 15 V$ $V_O = 0$ $R_S = 50 \Omega$	$T_A = 25^\circ C$	80	86		dB	
I_{CC} Supply current (each amplifier)	$V_O = 0$; no load	$T_A = 25^\circ C$		1.4	2.5	mA	
V_{O1} / V_{O2} Crosstalk attenuation	$A_{VD} = 100$	$T_A = 25^\circ C$		120		dB	

- (1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 6-40](#). Pulse techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.
- (2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is $T_A = -55^\circ C$ to $+125^\circ C$.

6.25 Switching Characteristics: TL07xM

$V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Slew rate at unity gain	$V_I = 10$ V $C_L = 100$ pF	5	13		V/ μ s
t_r Rise-time overshoot factor	$V_I = 20$ V $C_L = 100$ pF	$R_L = 2$ k Ω See Figure 7-1	0.1		μ s
			20%		
V_n Equivalent input noise voltage	$R_S = 20$ Ω	$f = 1$ kHz	18		nV/ $\sqrt{\text{Hz}}$
		$f = 10$ Hz to 10 kHz	4		μ V
I_n Equivalent input noise current	$R_S = 20$ Ω	$f = 1$ kHz	0.01		pA/ $\sqrt{\text{Hz}}$
THD Total harmonic distortion	$V_{I\text{rms}} = 6$ V $R_L \geq 2$ k Ω $f = 1$ kHz	$A_{VD} = 1$ $R_S \leq 1$ k Ω	0.003%		

6.26 Switching Characteristics: TL07xC, TL07xAC, TL07xBC, TL07xI

$V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Slew rate at unity gain	$V_I = 10$ V $C_L = 100$ pF	8	13		V/ μ s
t_r Rise-time overshoot factor	$V_I = 20$ V $C_L = 100$ pF	$R_L = 2$ k Ω See Figure 7-1	0.1		μ s
			20%		
V_n Equivalent input noise voltage	$R_S = 20$ Ω	$f = 1$ kHz	18		nV/ $\sqrt{\text{Hz}}$
		$f = 10$ Hz to 10 kHz	4		μ V
I_n Equivalent input noise current	$R_S = 20$ Ω	$f = 1$ kHz	0.01		pA/ $\sqrt{\text{Hz}}$
THD Total harmonic distortion	$V_{I\text{rms}} = 6$ V $R_L \geq 2$ k Ω $f = 1$ kHz	$A_{VD} = 1$ $R_S \leq 1$ k Ω	0.003%		

6.27 Electrical Characteristics, TL07xM

$V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	T_A ⁽²⁾	TL071M, TL072M			TL074M			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO} Input offset voltage	$V_O = 0$, $R_S = 50$ Ω	25°C		3	6		3	9	mV	
		Full range			9			15		
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50$ Ω	Full range		18			18		$\mu\text{V}/^\circ\text{C}$	
I_{IO} Input offset current	$V_O = 0$	25°C		5	100		5	100	pA	
		Full range		20			20			
I_{IB} Input bias current	$V_O = 0$	25°C		65	200		65	200	pA	
				50			20			
V_{ICR} Common-mode input voltage range		25°C	± 11	−12 to 15		± 11	−12 to 15		V	
V_{OM} Maximum peak output voltage swing	$R_L = 10$ k Ω	25°C	± 12	± 13.5		± 12	± 13.5		V	
	$R_L \geq 10$ k Ω	Full range	± 12	± 12		± 12	± 12			
	$R_L \geq 2$ k Ω		± 10	± 10		± 10	± 10			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2$ k Ω	25°C	35	200		35	200		V/mV	
			15	15		15	15			
B_1 Unity-gain bandwidth				3			3		MHz	
r_i Input resistance				10^{12}			10^{12}		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\min}$, $V_O = 0$, $R_S = 50$ Ω	25°C	80	86		80	86		dB	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$, $R_S = 50$ Ω	25°C	80	86		80	86		dB	
I_{CC} Supply current (each amplifier)	$V_O = 0$, No load	25°C		1.4	2.5		1.4	2.5	mA	
V_{O1}/V_{O2} Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB	

- (1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 6-40](#). Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.
- (2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is $T_A = -55^\circ\text{C}$ to 125°C .

6.28 Switching Characteristics

$V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL07xM			TL07xC, TL07xAC, TL07xBC, TL07xI TL075			UNIT		
		MIN	TYP	MAX	MIN	TYP	MAX			
SR Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ k Ω , See Figure 7-1	5	13		8	13		V/ μ s	
t_r Rise-time overshoot factor	$V_I = 20$ V, $C_L = 100$ pF,	$R_L = 2$ k Ω , See Figure 7-1		0.1			0.1		μ s	
				20%			20%			
V_n Equivalent input noise voltage	$R_S = 20$ Ω	$f = 1$ kHz		18			18		nV/ $\sqrt{\text{Hz}}$	
		$f = 10$ Hz to 10 kHz		4			4		μ V	
I_n Equivalent input noise current	$R_S = 20$ Ω ,	$f = 1$ kHz		0.01			0.01		pA/ $\sqrt{\text{Hz}}$	
THD Total harmonic distortion	$V_{Irms} = 6$ V, $R_L \geq 2$ k Ω , $f = 1$ kHz,	$A_{VD} = 1$, $R_S \leq 1$ k Ω ,		0.003%			0.003%			

6.29 Typical Characteristics: TL07xH

at $T_A = 25^\circ\text{C}$, $V_S = 40 \text{ V}$ ($\pm 20 \text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10 \text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 20 \text{ pF}$ (unless otherwise noted)

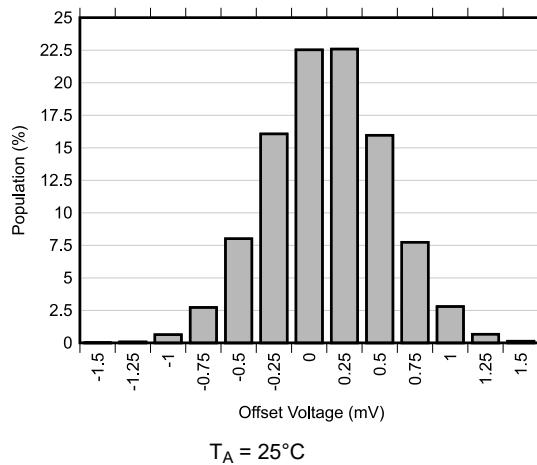


Figure 6-1. Offset Voltage Production Distribution

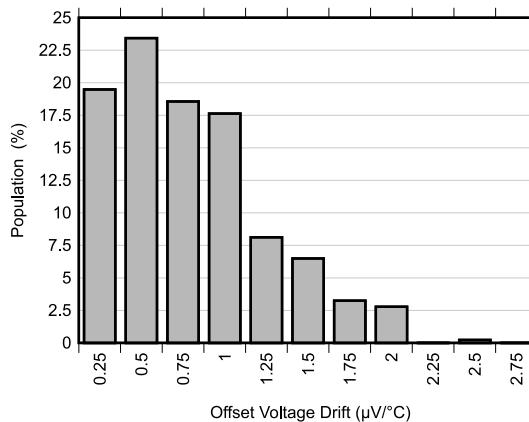


Figure 6-2. Offset Voltage Drift Distribution

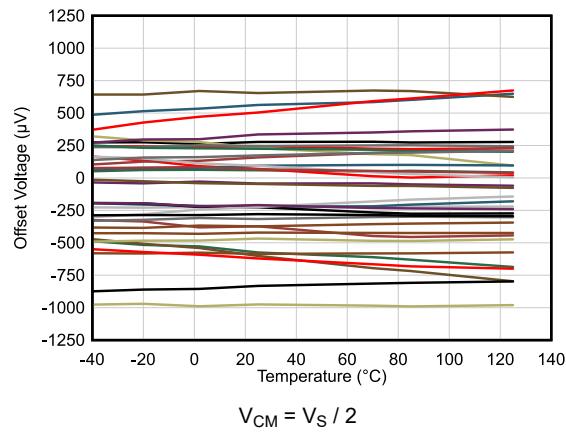


Figure 6-3. Offset Voltage vs Temperature

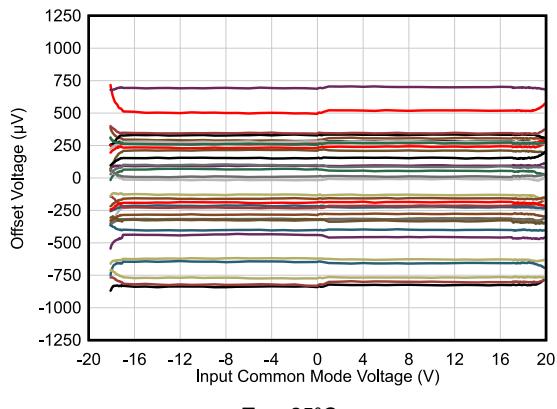


Figure 6-4. Offset Voltage vs Common-Mode Voltage

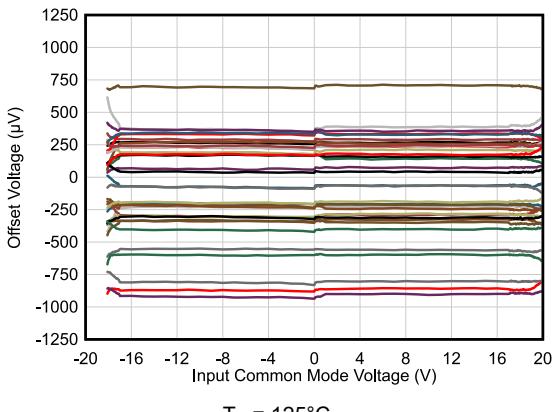


Figure 6-5. Offset Voltage vs Common-Mode Voltage

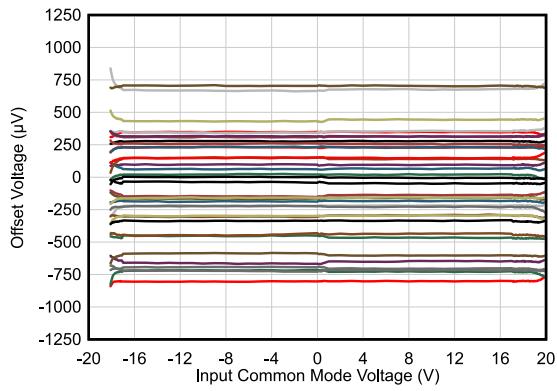


Figure 6-6. Offset Voltage vs Common-Mode Voltage

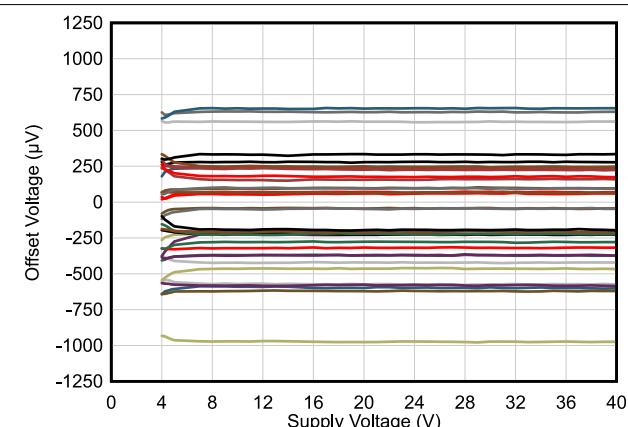


Figure 6-7. Offset Voltage vs Power Supply

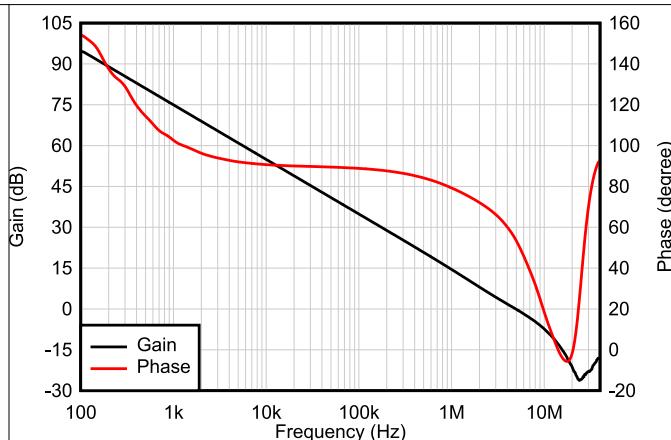


Figure 6-8. Open-Loop Gain and Phase vs Frequency

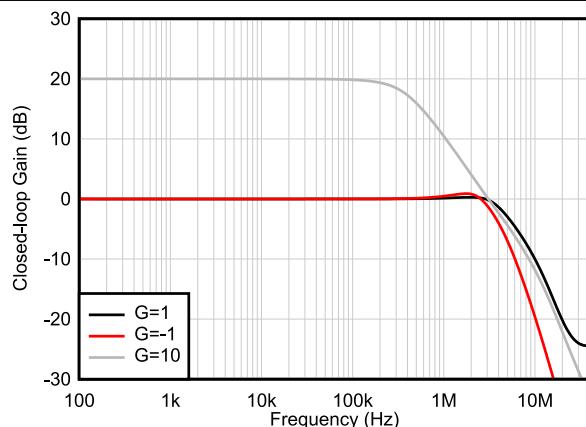


Figure 6-9. Closed-Loop Gain vs Frequency

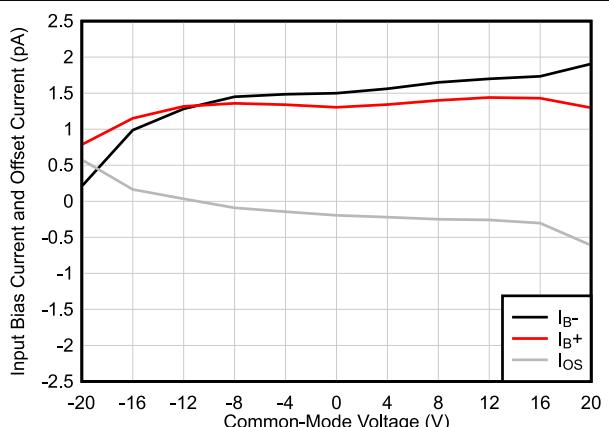


Figure 6-10. Input Bias Current vs Common-Mode Voltage

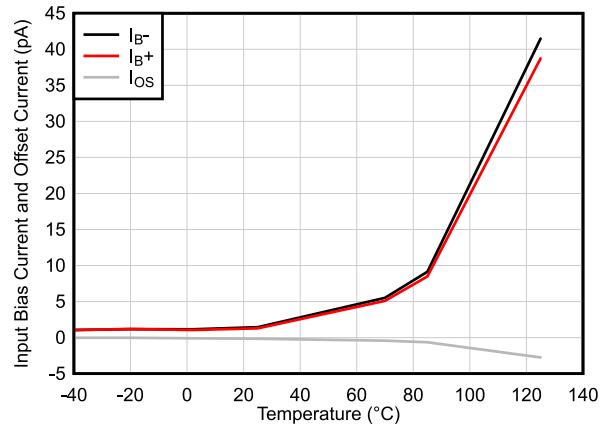


Figure 6-11. Input Bias Current vs Temperature

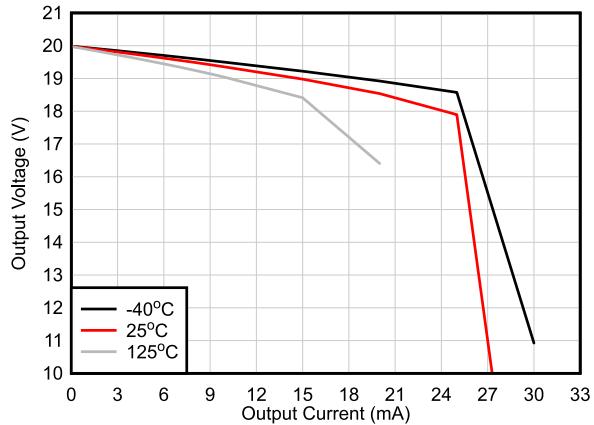


Figure 6-12. Output Voltage Swing vs Output Current (Sourcing)

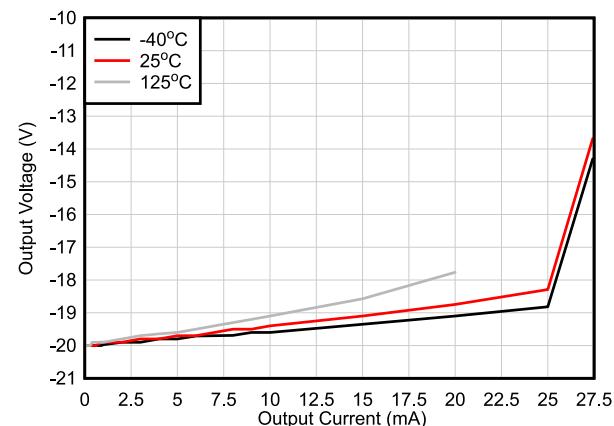


Figure 6-13. Output Voltage Swing vs Output Current (Sinking)

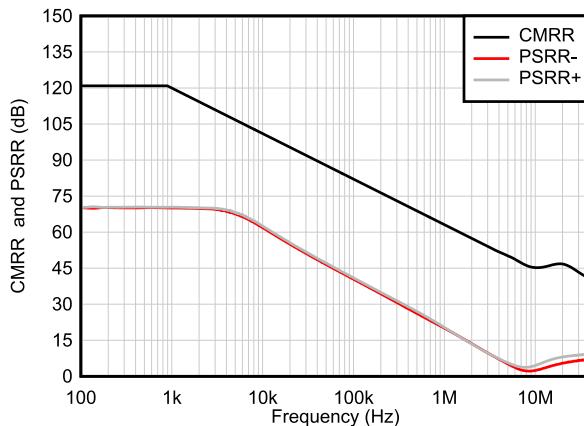


Figure 6-14. CMRR and PSRR vs Frequency

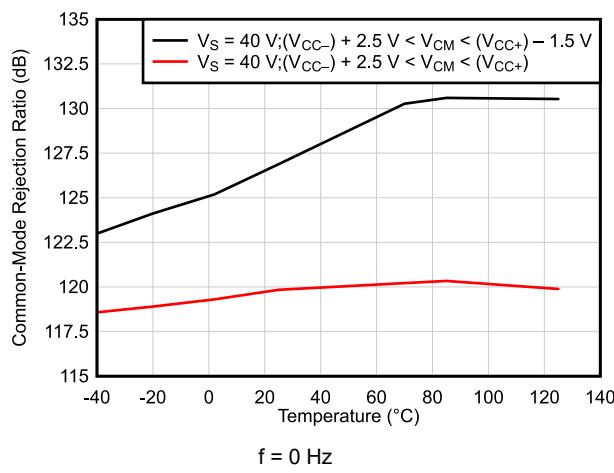


Figure 6-15. CMRR vs Temperature (dB)

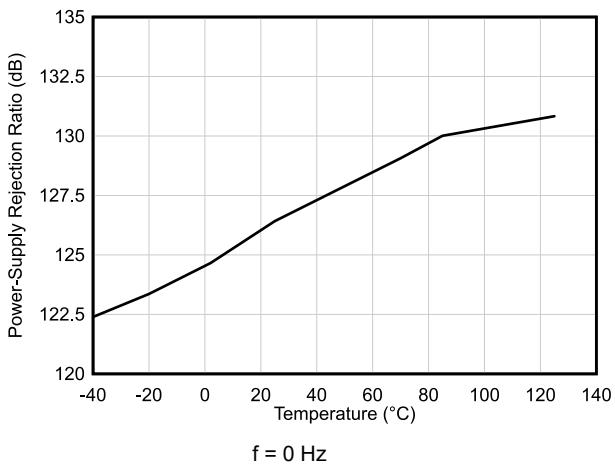


Figure 6-16. PSRR vs Temperature (dB)

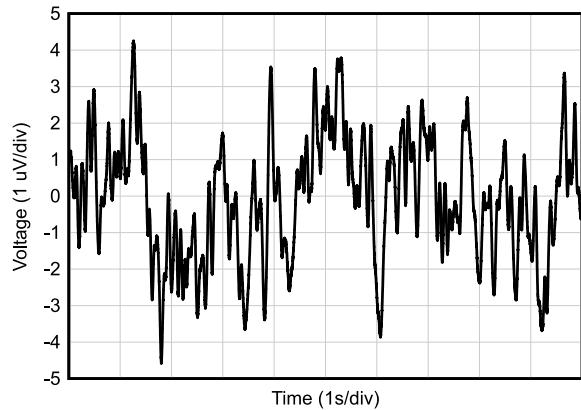


Figure 6-17. 0.1-Hz to 10-Hz Noise

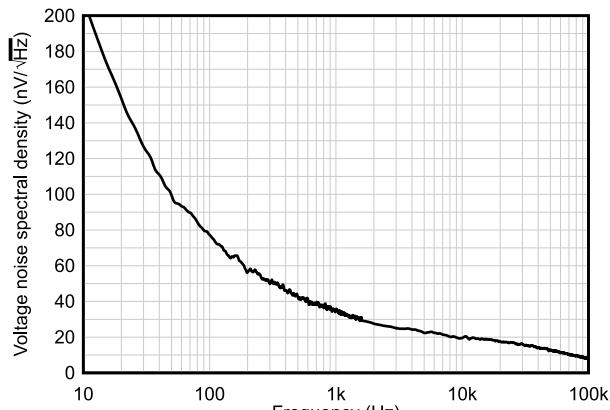
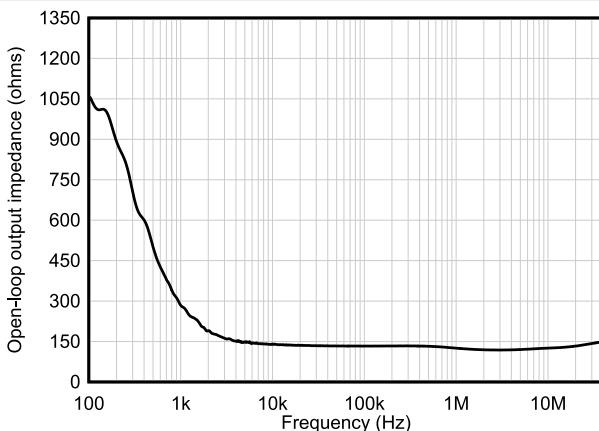
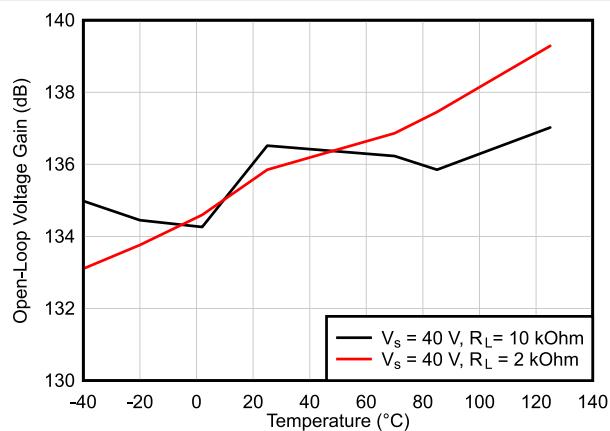
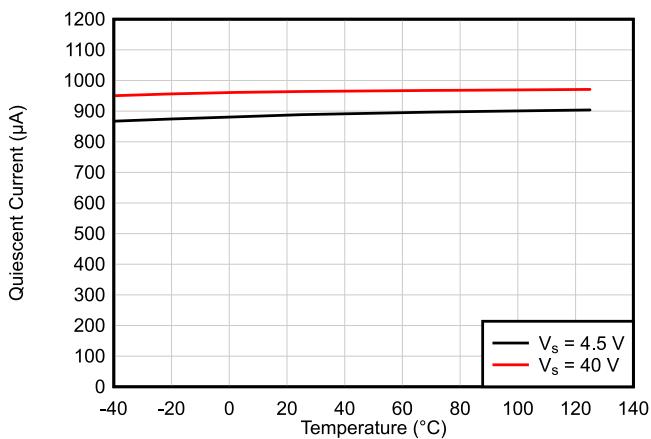
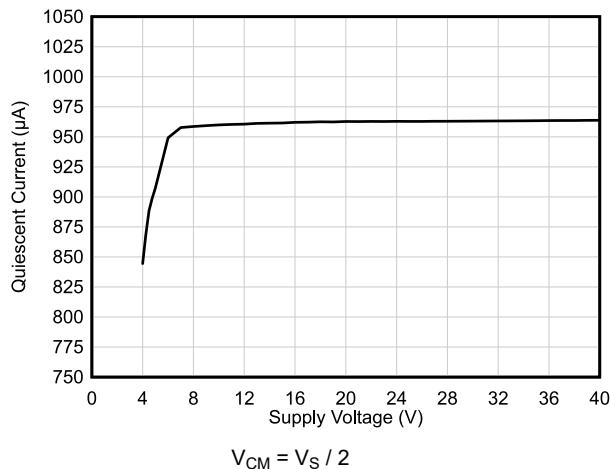
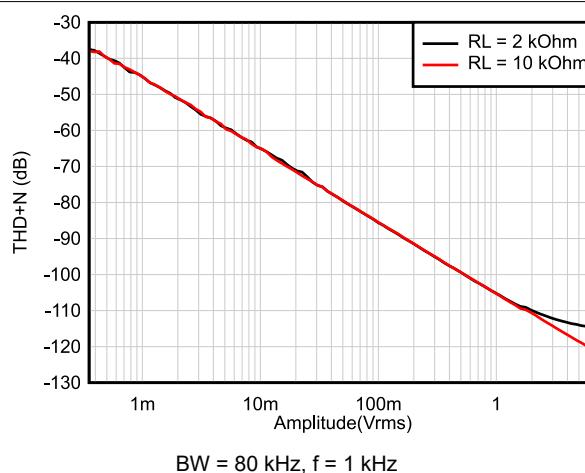
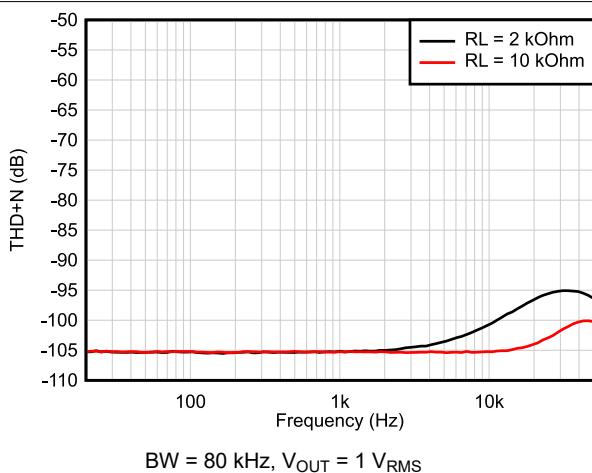


Figure 6-18. Input Voltage Noise Spectral Density vs Frequency



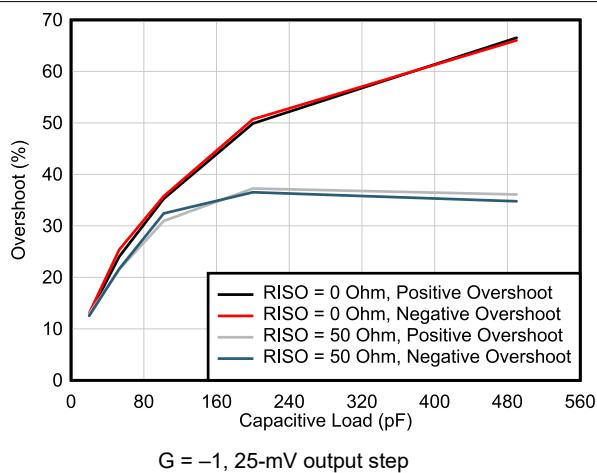


Figure 6-25. Small-Signal Overshoot vs Capacitive Load

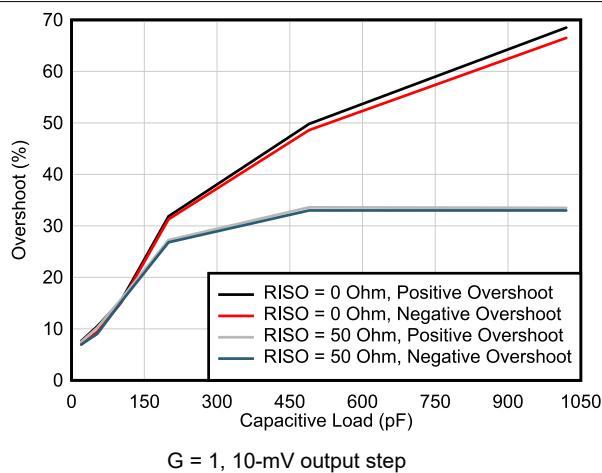


Figure 6-26. Small-Signal Overshoot vs Capacitive Load

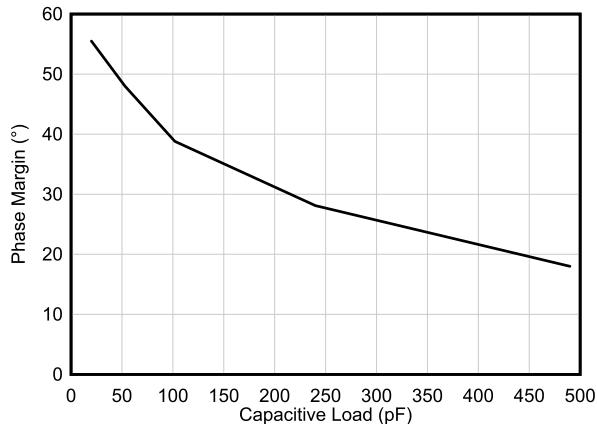


Figure 6-27. Phase Margin vs Capacitive Load

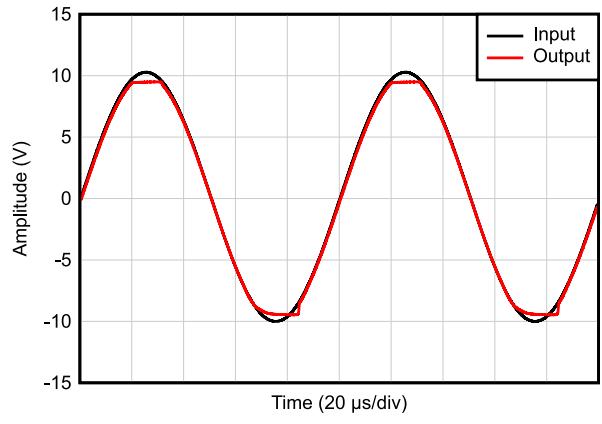


Figure 6-28. No Phase Reversal

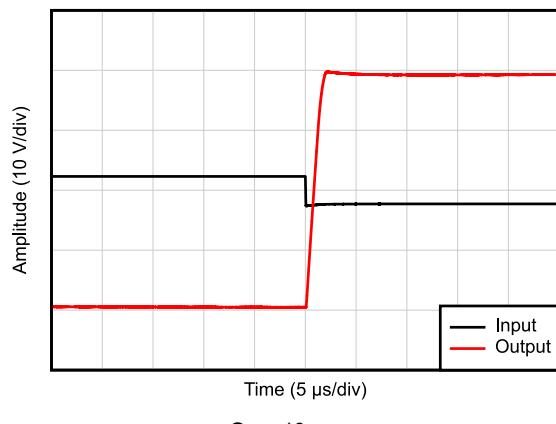


Figure 6-29. Positive Overload Recovery

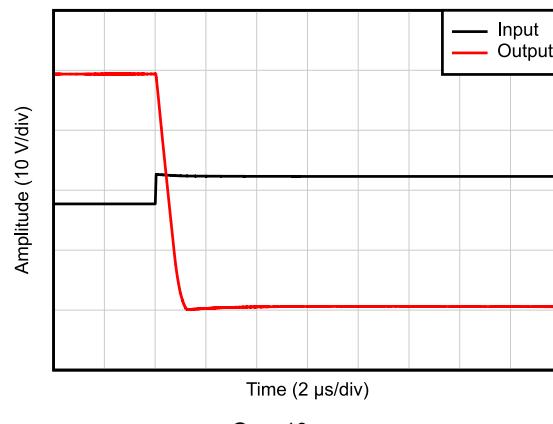
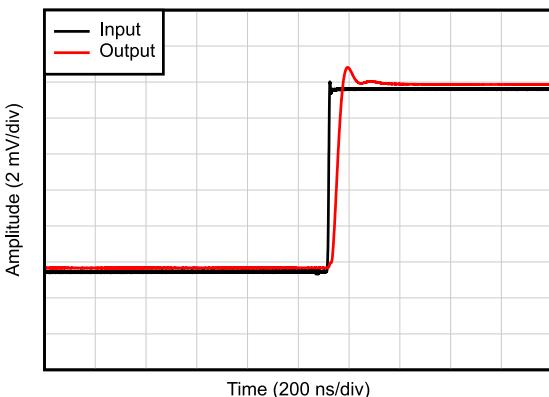
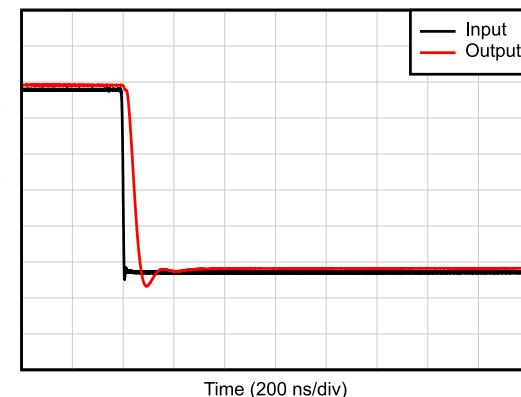


Figure 6-30. Negative Overload Recovery



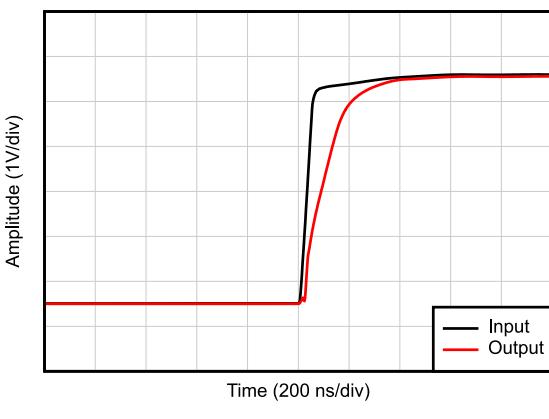
$C_L = 20 \text{ pF}, G = 1, 10\text{-mV step response}$

Figure 6-31. Small-Signal Step Response, Rising



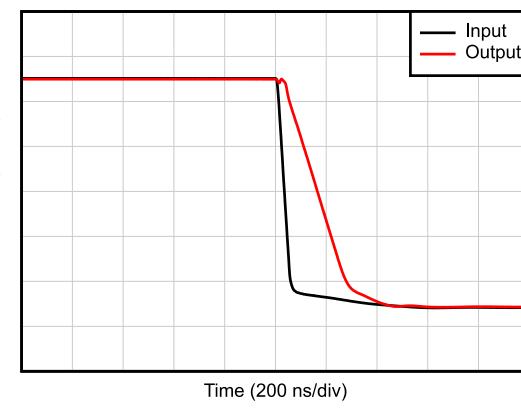
$C_L = 20 \text{ pF}, G = 1, 10\text{-mV step response}$

Figure 6-32. Small-Signal Step Response, Falling



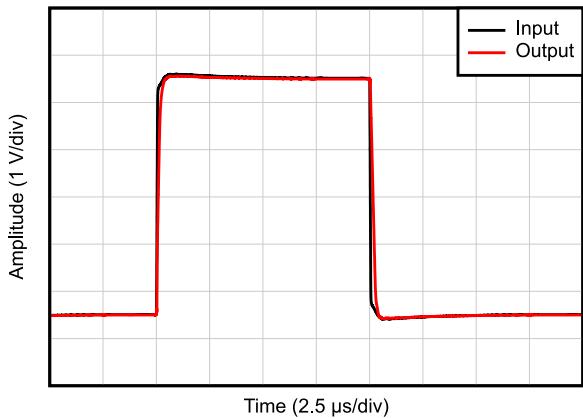
$C_L = 20 \text{ pF}, G = 1$

Figure 6-33. Large-Signal Step Response (Rising)



$C_L = 20 \text{ pF}, G = 1$

Figure 6-34. Large-Signal Step Response (Falling)



$C_L = 20 \text{ pF}, G = 1$

Figure 6-35. Large-Signal Step Response

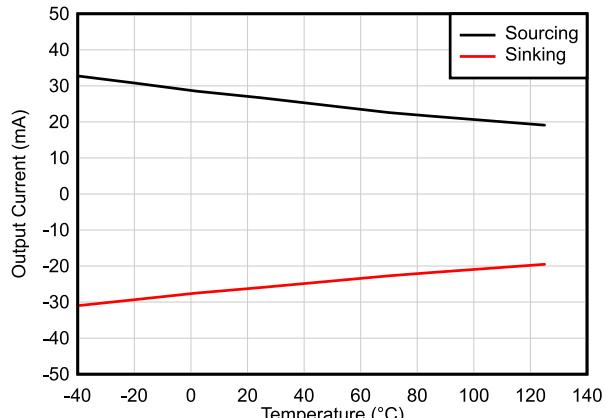


Figure 6-36. Short-Circuit Current vs Temperature

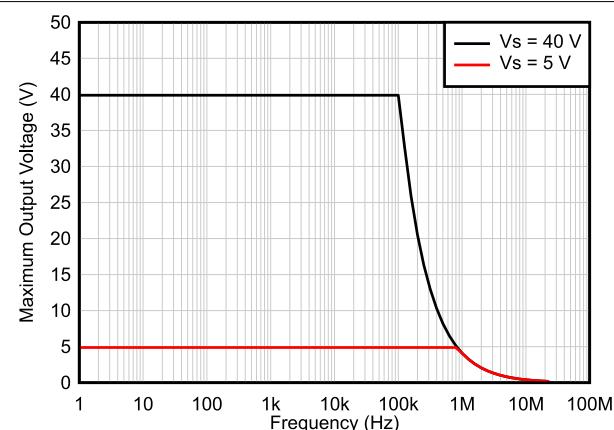


Figure 6-37. Maximum Output Voltage vs Frequency

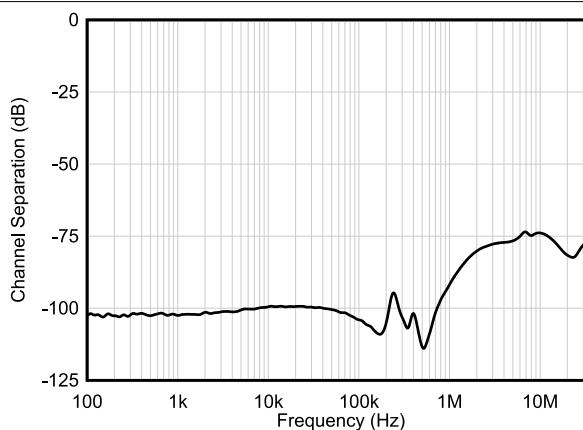


Figure 6-38. Channel Separation vs Frequency

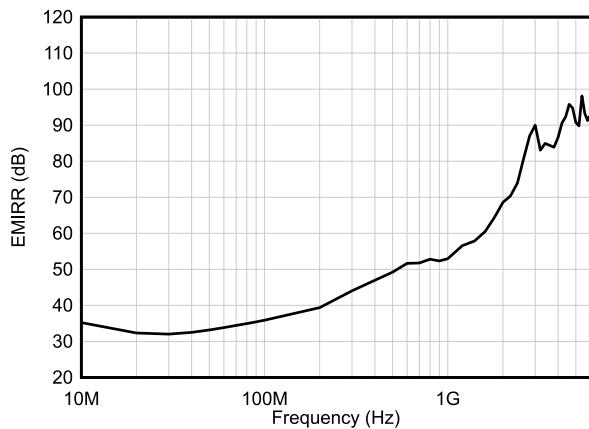


Figure 6-39. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6.30 Typical Characteristics: All Devices Except TL07xH

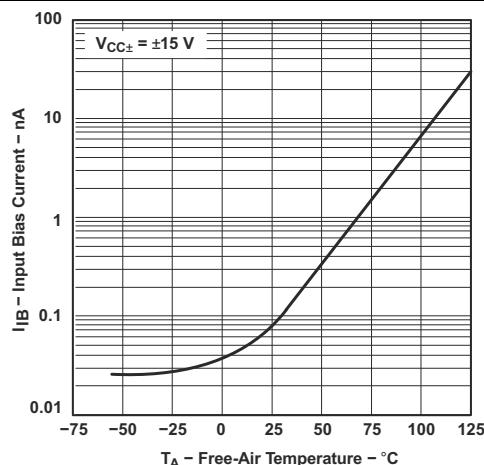


Figure 6-40. Input Bias Current vs Free-Air Temperature

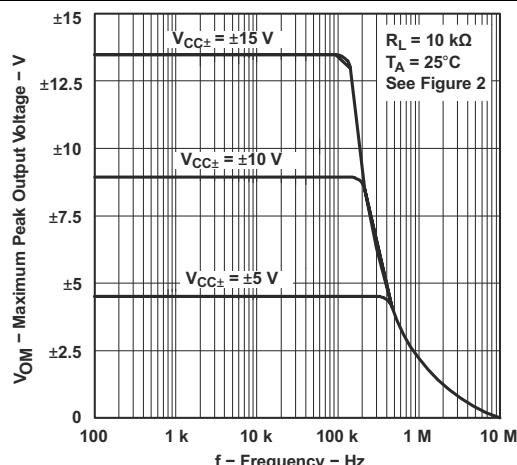


Figure 6-41. Maximum Peak Output Voltage vs Frequency

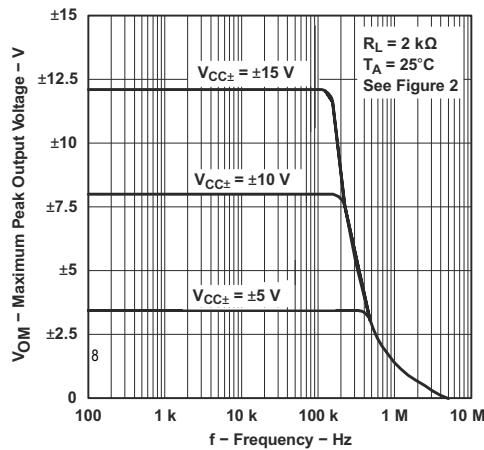


Figure 6-42. Maximum Peak Output Voltage vs Frequency

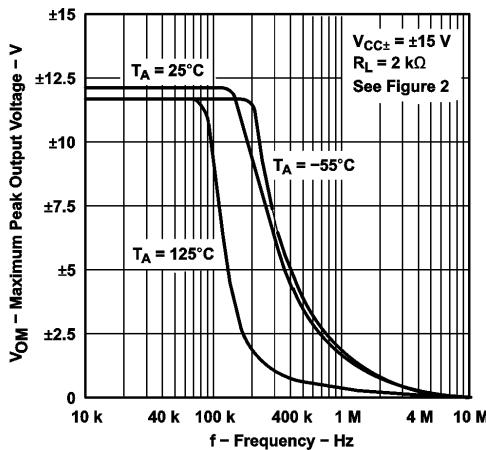


Figure 6-43. Maximum Peak Output Voltage vs Frequency

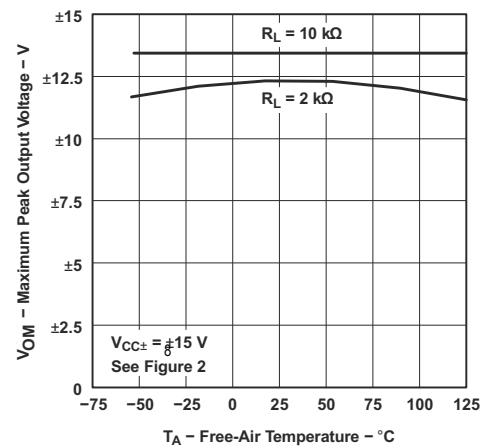


Figure 6-44. Maximum Peak Output Voltage vs Free-Air Temperature

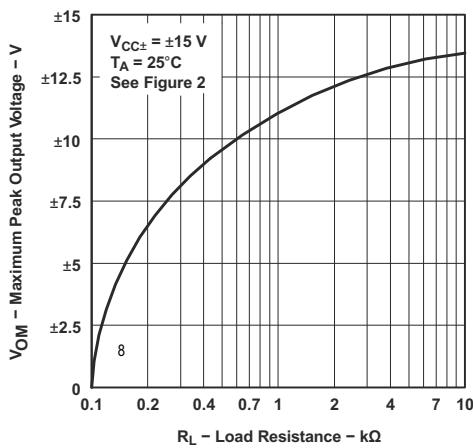


Figure 6-45. Maximum Peak Output Voltage vs Load Resistance

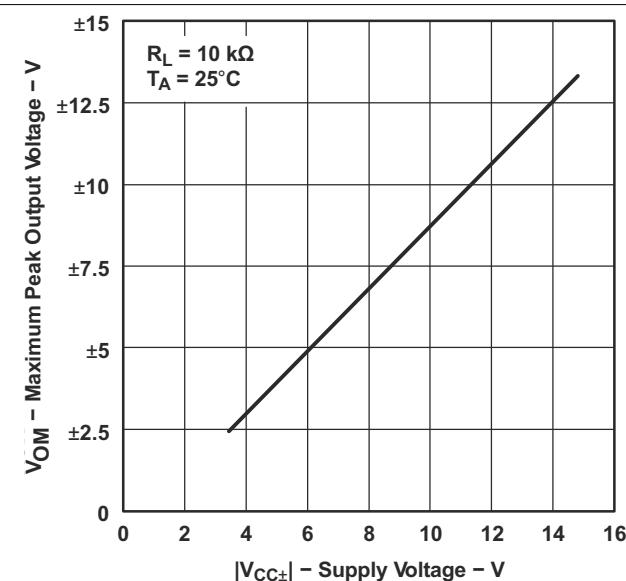


Figure 6-46. Maximum Peak Output Voltage vs Supply Voltage

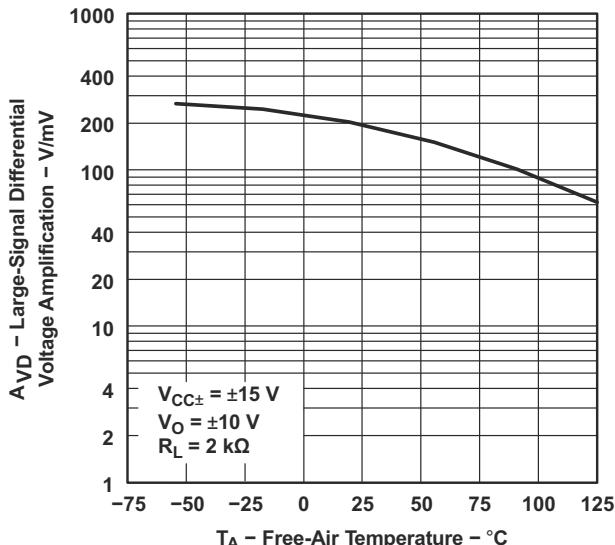


Figure 6-47. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

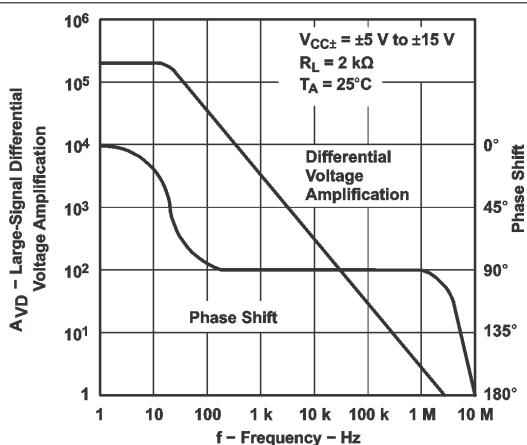


Figure 6-48. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

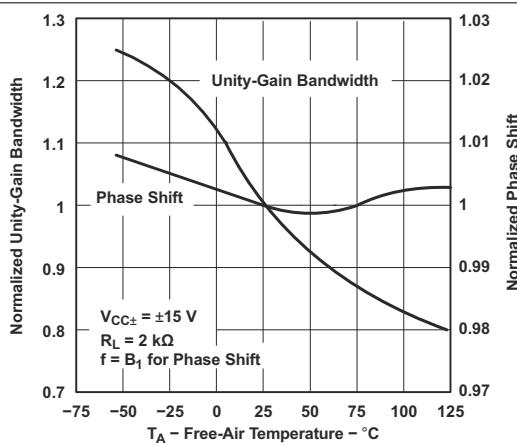


Figure 6-49. Normalized Unity-Gain Bandwidth and Phase Shift vs Free-Air Temperature

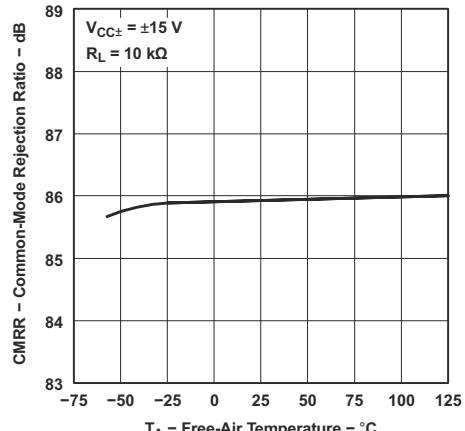


Figure 6-50. Common-Mode Rejection Ratio vs Free-Air Temperature

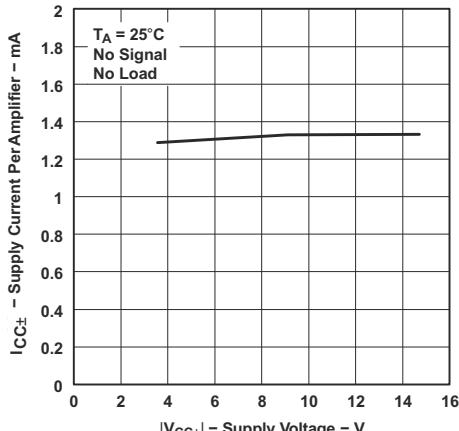


Figure 6-51. Supply Current Per Amplifier vs Supply Voltage

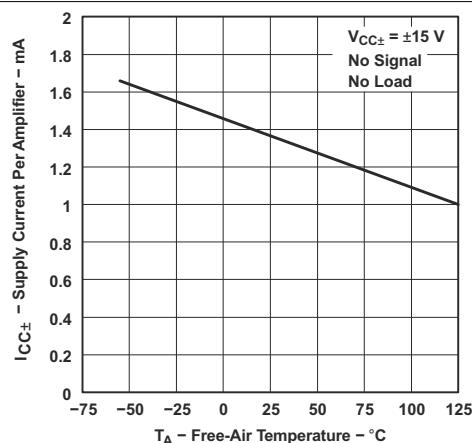


Figure 6-52. Supply Current Per Amplifier vs Free-Air Temperature

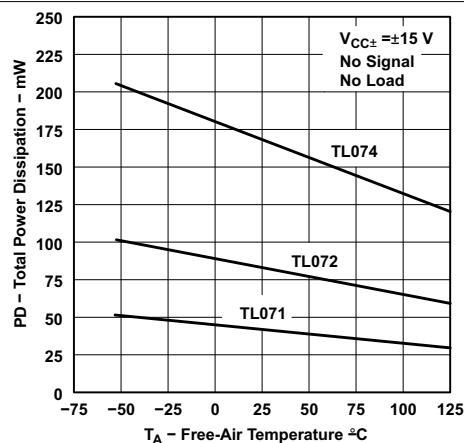


Figure 6-53. Total Power Dissipation vs Free-Air Temperature

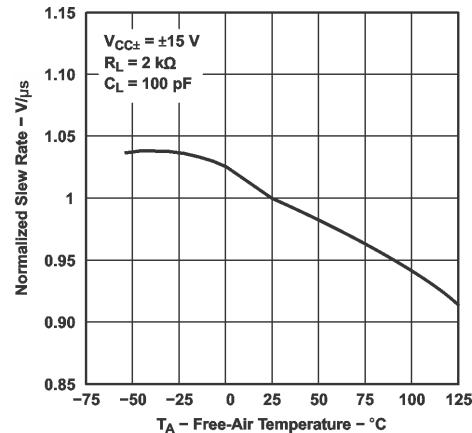


Figure 6-54. Normalized Slew Rate vs Free-Air Temperature

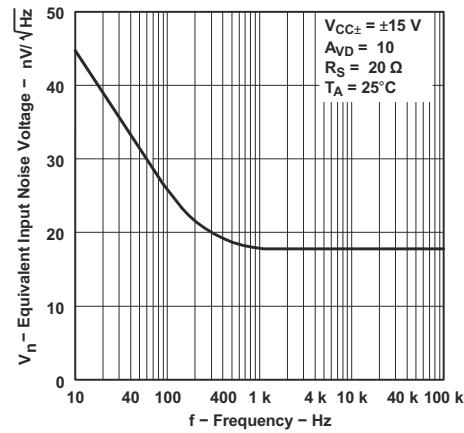


Figure 6-55. Equivalent Input Noise Voltage vs Frequency

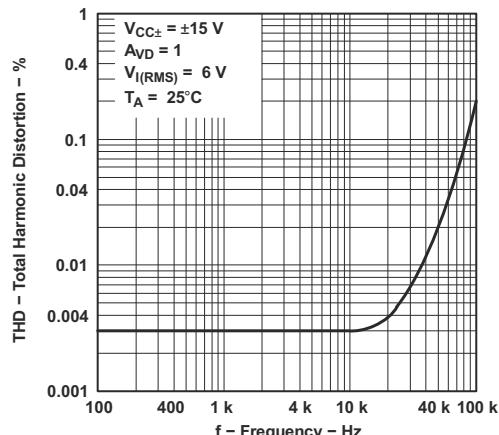


Figure 6-56. Total Harmonic Distortion vs Frequency

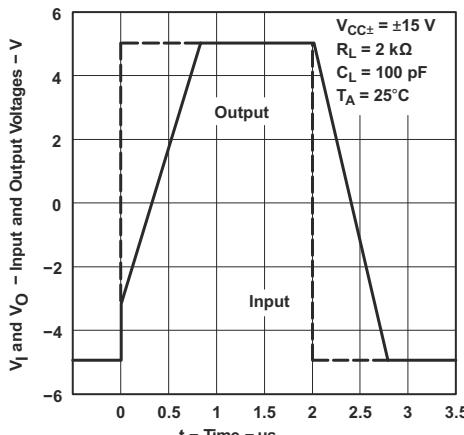


Figure 6-57. Voltage-Follower Large-Signal Pulse Response

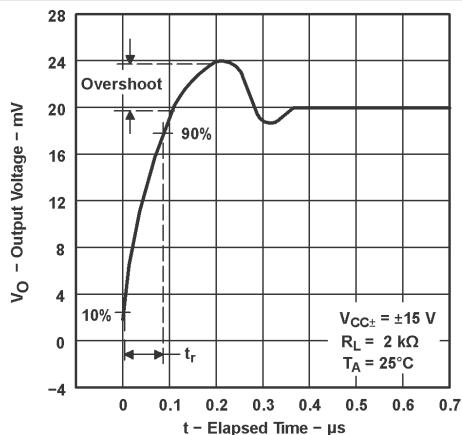


Figure 6-58. Output Voltage vs Elapsed Time

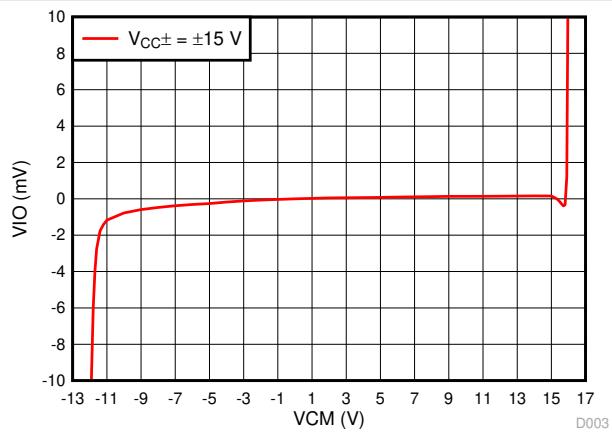


Figure 6-59. V_{IO} vs V_{CM}

7 Parameter Measurement Information

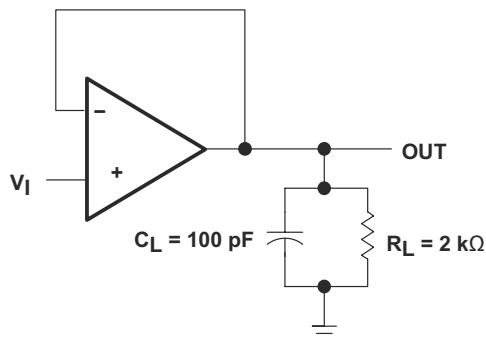


Figure 7-1. Unity-Gain Amplifier

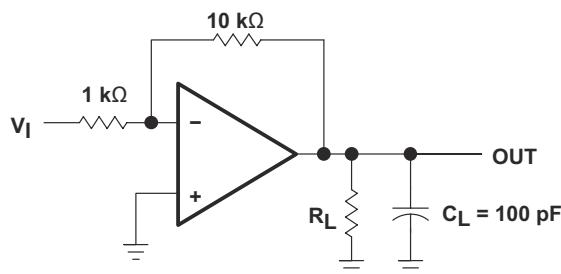


Figure 7-2. Gain-of-10 Inverting Amplifier

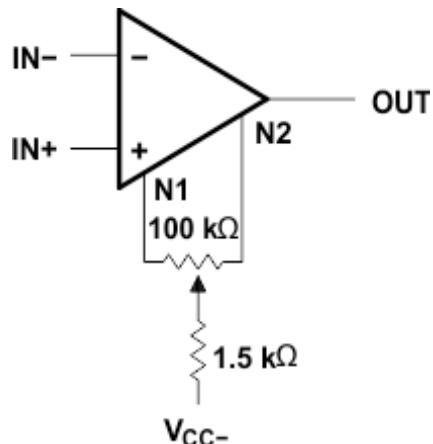


Figure 7-3. Input Offset-Voltage Null Circuit

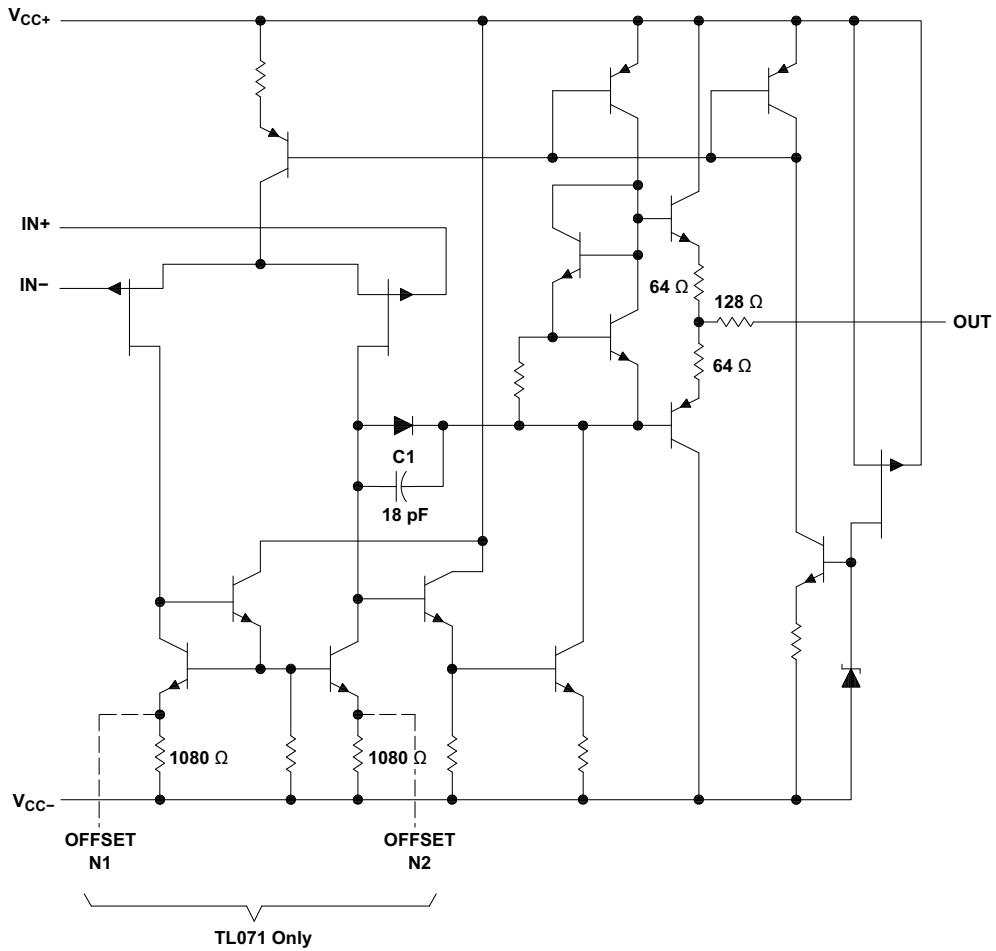
8 Detailed Description

8.1 Overview

The TL07xH (TL071H, TL072H, and TL074H) family of devices are the next-generation versions of the industry-standard TL07x (TL071, TL072, and TL074) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1 mV, typ), high slew rate (25 V/ μ s, typ), and common-mode input to the positive supply. High ESD (1.5 kV, HBM), integrated EMI and RF filters, and operation across the full -40°C to 125°C enable the TL07xH devices to be used in the most rugged and demanding applications.

The C-suffix devices are characterized for operation from 0°C to 70°C . The I-suffix devices are characterized for operation from -40°C to $+85^{\circ}\text{C}$. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to $+125^{\circ}\text{C}$.

8.2 Functional Block Diagram



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

8.3 Feature Description

The TL07xH family of devices improve many specifications as compared to the industry-standard TL07x family. Several comparisons of key specifications between these families are included below to show the advantages of the TL07xH family.

8.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL07x device adds little harmonic distortion when used in audio signal applications.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. These devices have a 13-V/ μ s slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. These devices can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes the voltage a negative voltage. In the same manner, the amplifier makes negative voltages positive.

9.2 Typical Application

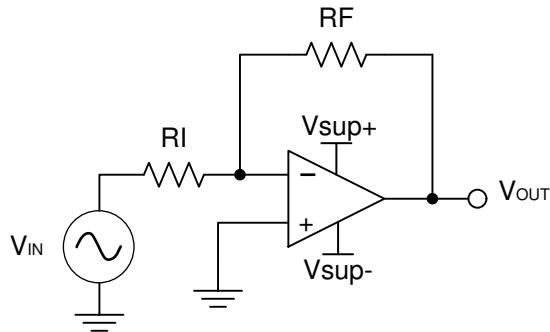


Figure 9-1. Inverting Amplifier

9.2.1 Design Requirements

The supply voltage must be selected so the supply voltage is larger than the input voltage range and output range. For instance, this application scales a signal of ± 0.5 V to ± 1.8 V. Setting the supply at ± 12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

$$V_o = (V_i + V_{i_o}) * \left(1 + \frac{1 \text{ M}\Omega}{1 \text{ k}\Omega}\right) \quad (1)$$

Determine the gain required by the inverting amplifier:

$$A_v = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \quad (2)$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \quad (3)$$

Once the desired gain is determined, select a value for R_I or R_F . Selecting a value in the kilohm range is desirable because the amplifier circuit uses currents in the millamp range. This ensures the part does not draw too much current. This example uses $10 \text{ k}\Omega$ for R_I which means $36 \text{ k}\Omega$ is used for R_F . This is determined by Equation 4.

$$A_v = -\frac{R_F}{R_I} \quad (4)$$

9.2.3 Application Curve

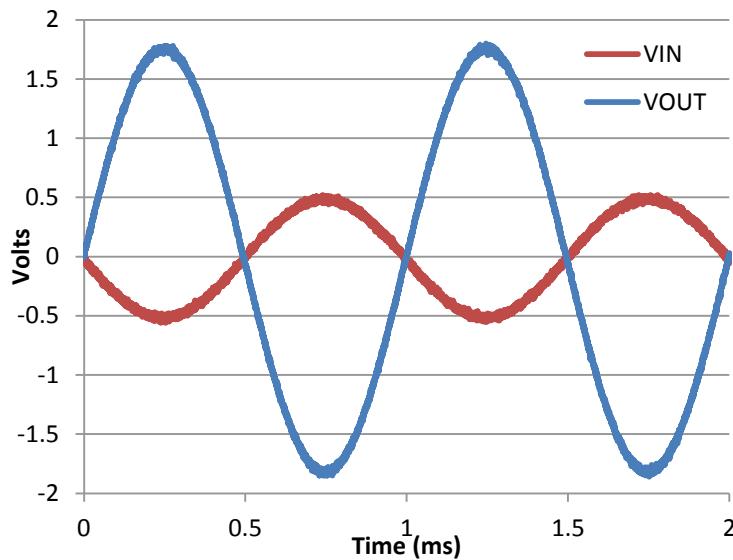
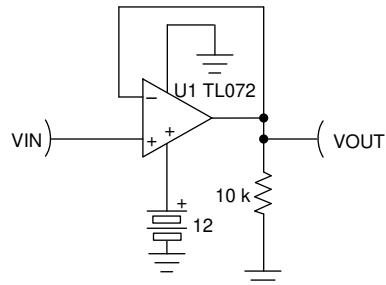


Figure 9-2. Input and Output Voltages of the Inverting Amplifier

9.3 Unity Gain Buffer



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Figure 9-3. Single-Supply Unity Gain Amplifier

9.3.1 Design Requirements

- V_{CC} must be within valid range per [Section 6.6](#). This example uses a value of 12 V for V_{CC} .
- Input voltage must be within the recommended common-mode range, as shown in [Section 6.6](#). The valid common-mode range is 4 V to 12 V ($V_{CC-} + 4$ V to V_{CC+}).
- Output is limited by output range, which is typically 1.5 V to 10.5 V, or $V_{CC-} + 1.5$ V to $V_{CC+} - 1.5$ V.

9.3.2 Detailed Design Procedure

- Avoid input voltage values below 1 V to prevent phase reversal where output goes high.
- Avoid input values below 4 V to prevent degraded V_{IO} that results in an apparent gain greater than 1. This may cause instability in some second-order filter designs.

9.3.3 Application Curves

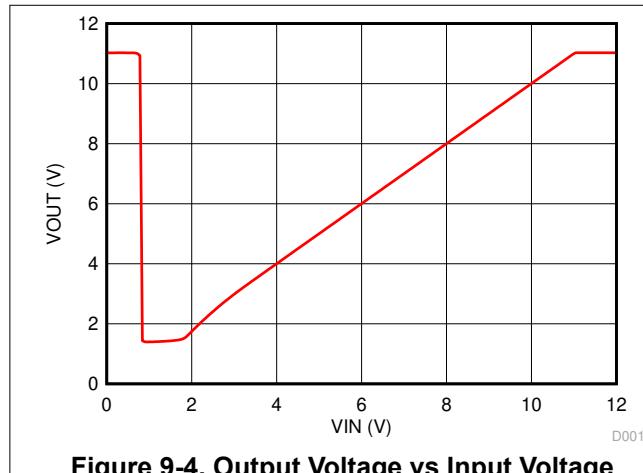


Figure 9-4. Output Voltage vs Input Voltage

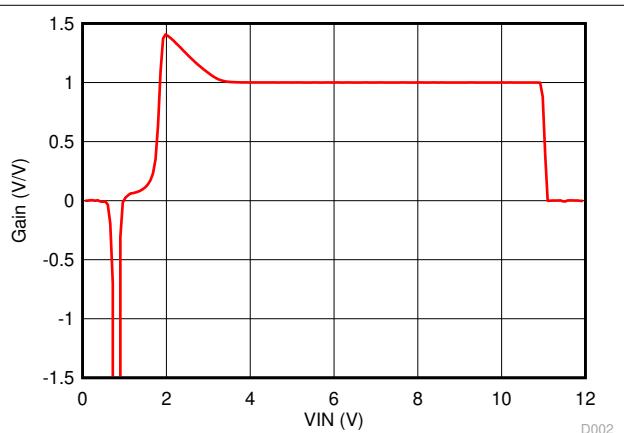


Figure 9-5. Gain vs Input Voltage

9.4 System Examples

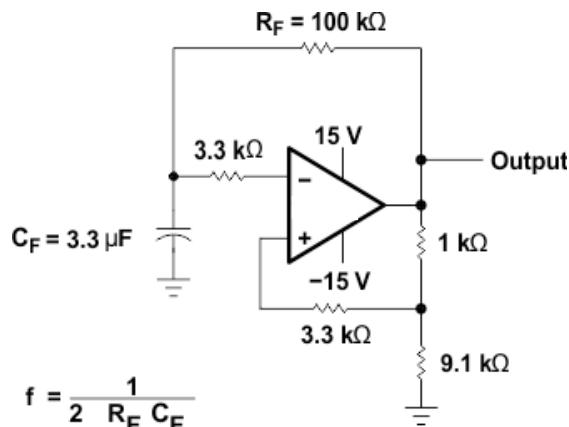


Figure 9-6. 0.5-Hz Square-Wave Oscillator

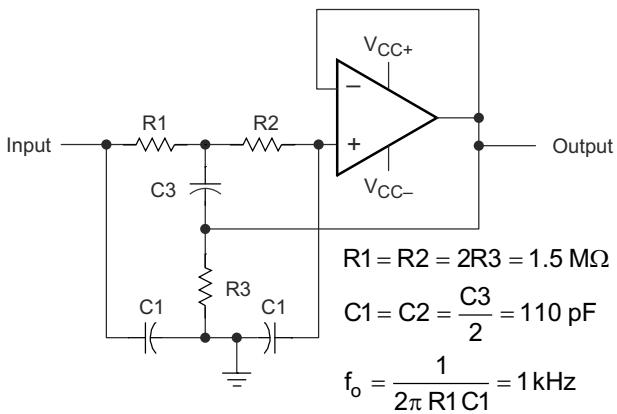


Figure 9-7. High-Q Notch Filter

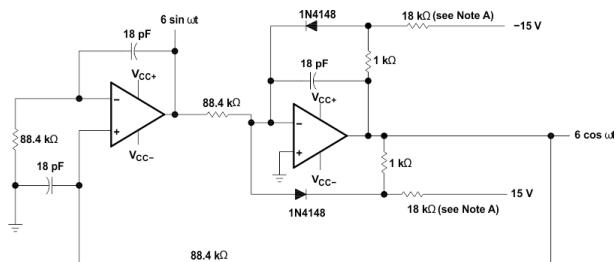


Figure 9-8. 100-kHz Quadrature Oscillator

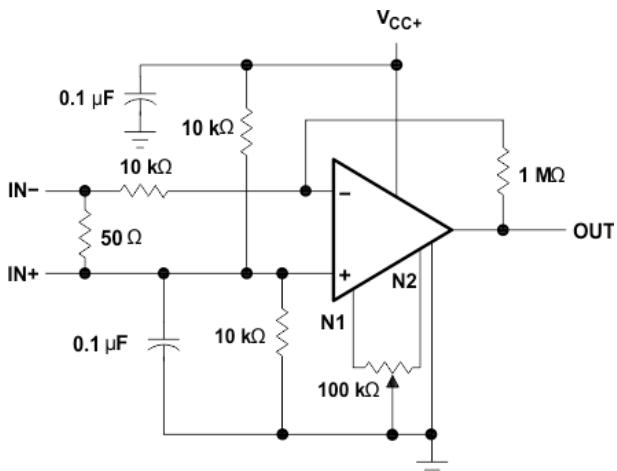


Figure 9-9. AC Amplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ± 18 V for a dual-supply can permanently damage the device (see [Section 6.2](#)).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Section 11](#).

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V_{CC+} to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Section 11.2](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

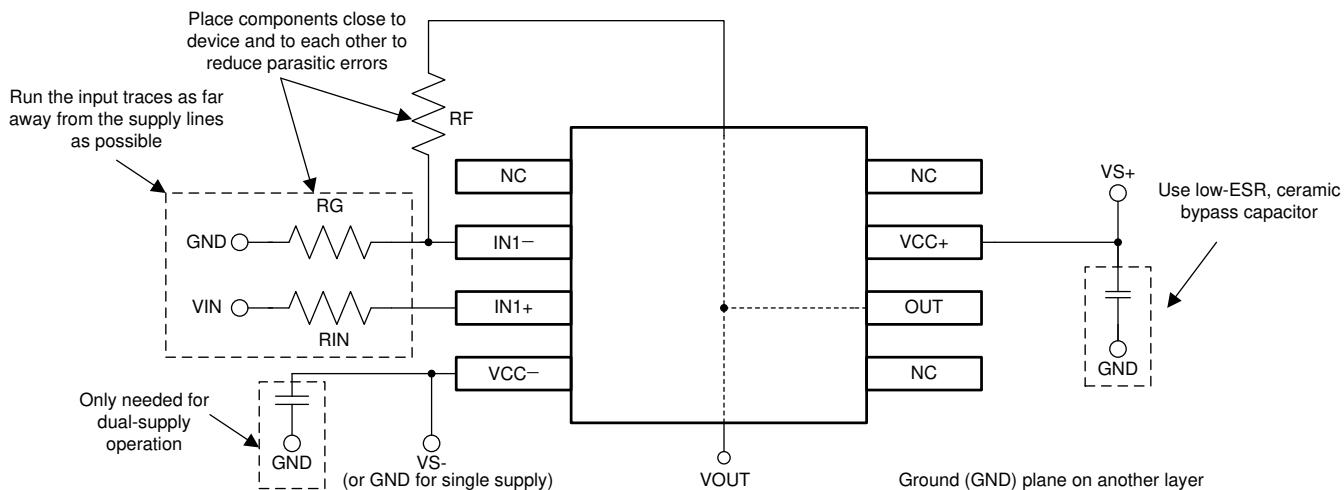


Figure 11-1. Operational Amplifier Board Layout for Noninverting Configuration

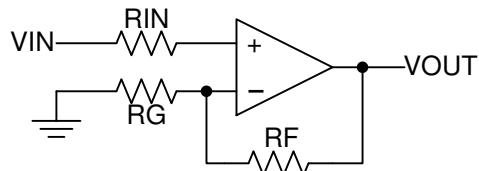


Figure 11-2. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL071	Click here				
TL071A	Click here				
TL071B	Click here				
TL072	Click here				
TL072A	Click here				
TL072B	Click here				
TL072M	Click here				
TL074	Click here				
TL074A	Click here				
TL074B	Click here				
TL074M	Click here				

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.



ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.



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PACKAGE OPTION ADDENDUM

9-Mar-2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C) (4/5)	Device Marking (4/5)	Sample
81023052A	ACTIVE	LCOC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Sample
8102305HA	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Sample
8102305PA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Sample
81023062A	ACTIVE	LCOC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Sample
8102306CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Sample
8102306DA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Sample
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Sample
M38510/11905BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Sample
TL071ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Sample
TL071ACDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Sample
TL071ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Sample
TL071ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071ACP	Sample
TL071BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Sample
TL071BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Sample
TL071BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071BCP	Sample
TL071CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Sample
TL071CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Sample
TL071CDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Sample

Orderable Device	Status	Package Type	Package Drawing	Pins Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp (⁵)	Op Temp (°C)	Device Marking (^{4/5})	Sample
(1)	(1)	(1)	(1)	(2)	(2)	(6)	(3)	(4)	(4/5)	(1)
TL071CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C
TL071CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071CP
TL071CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071CP
TL071CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071
TL071ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL071IP
TL072ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP
TL072ACPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP
TL072BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC
TL072BCDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC
TL072BCDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC
TL072BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC
TL072BCDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC
TL072BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP

Orderable Device	Status	Package Type	Package Drawing	Pins Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp (⁽⁵⁾)	Op Temp (°C)	Device Marking (^(4/5))	Sample
(1)	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
TL072BCPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP
TL072CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C
TL072CDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C
TL072CDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C
TL072CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C
TL072CDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C
TL072CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C
TL072CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072CP
TL072CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072CP
TL072CP	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPSRE4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPWWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I
TL072IDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I
TL072IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I
TL072IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I
TL072DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I



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PACKAGE OPTION ADDENDUM

9-Mar-2021

Orderable Device	Status	Package Type	Package Drawing	Pins Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp (S)	Op Temp (°C)	Device Marking (4/5)	Sample
(1)	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
TL0721DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL0721I
TL0721P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL0721P
TL0721PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL0721P
TL0721MFKB	ACTIVE	LOCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023052A TL0721MFKB
TL0721MUG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL0721MUG
TL0721MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305PA TL0721M
TL0721MUB	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305HA TL0721M
TL074ACD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC
TL074ACDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC
TL074ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC
TL074ACDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC
TL074ACDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC
TL074ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN
TL074ACNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN
TL074ACNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A
TL074BCD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC

Orderable Device	Status	Package Type	Package Drawing	Pins Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp (⁵)	Op Temp (°C)	Device Marking (^{4/5})	Sample
(1)	(1)	(1)	(1)	(2)	(2)	(6)	(3)	(3)	(4/5)	(1)
TL074BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN
TL074BCNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN
TL074CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
TL074CDBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
TL074CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
TL074CDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
TL074CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074CN
TL074CNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074CN
TL074CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074
TL074CNSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074
TL074CPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074HIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL074HID
TL074HIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL074PW
TL074ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I

Orderable Device	Status	Package Type	Package Drawing	Pins Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp (S)	Op Temp (°C)	Device Marking (4/5)	Sample
(1)	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
TL074IDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL074IN
TL074MFK	ACTIVE	LOCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL074MFK
TL074MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB
TL074MJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL074MJ
TL074MJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB
TL074MWB	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JESD09B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a ";" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :

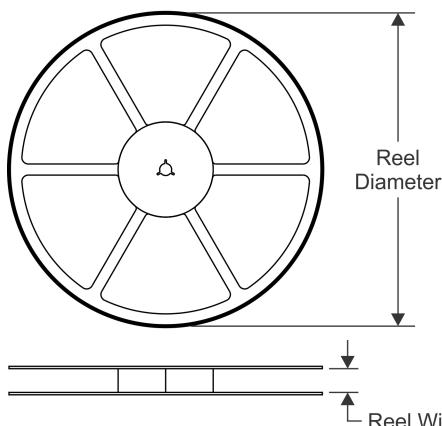
- Catalog: [TL072](#), [TL074](#)
- Enhanced Product: [TL072-EP](#), [TL072-EP](#), [TL074-EP](#), [TL074-EP](#)
- Military: [TL072M](#), [TL074M](#)

NOTE: Qualified Version Definitions:

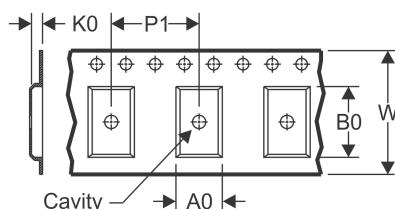
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

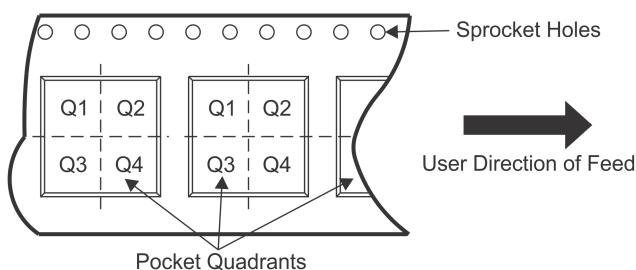


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

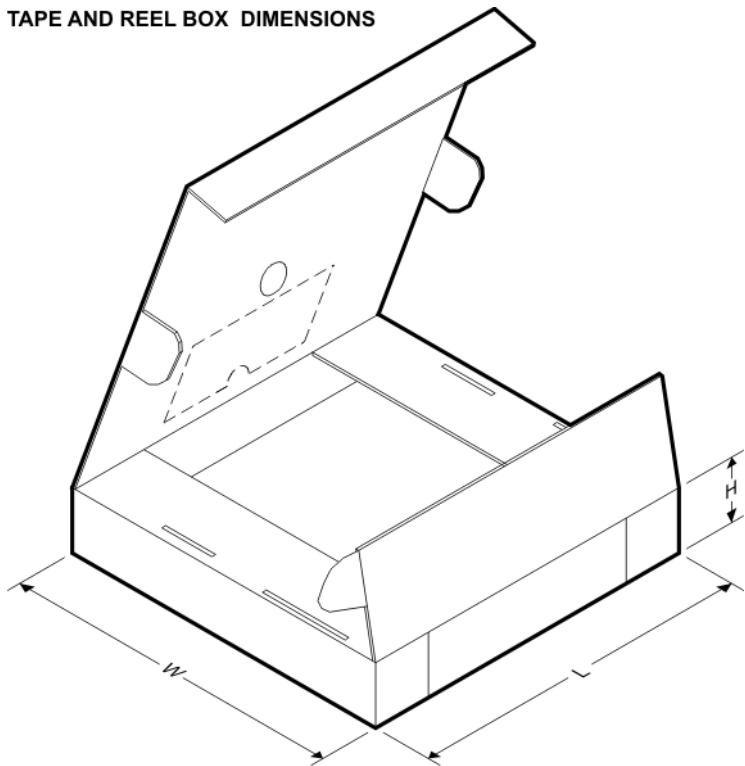
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074HIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	853.0	449.0	35.0
TL071IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072CDR	SOIC	D	8	2500	853.0	449.0	35.0
TL072CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072CPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TL072IDR	SOIC	D	8	2500	853.0	449.0	35.0
TL072IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL074ACDR	SOIC	D	14	2500	333.2	345.9	28.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL074ACNSR	SO	NS	14	2000	853.0	449.0	35.0
TL074BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074CDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074CDRG4	SOIC	D	14	2500	333.2	345.9	28.6
TL074CNSR	SO	NS	14	2000	853.0	449.0	35.0
TL074CPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
TL074HIDR	SOIC	D	14	2500	853.0	449.0	35.0
TL074HIPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
TL074IDR	SOIC	D	14	2500	333.2	345.9	28.6

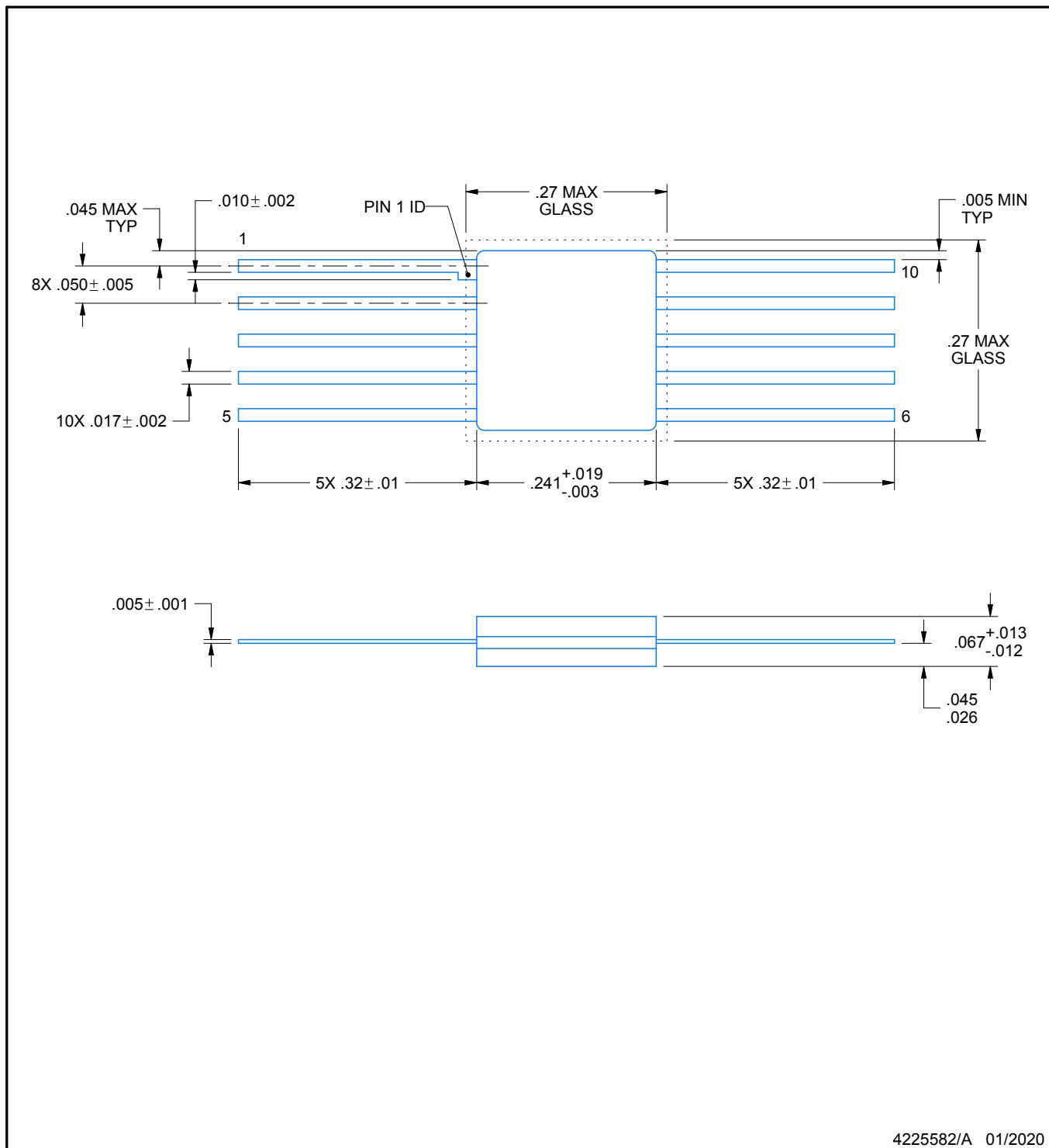
U0010A



PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK



4225582/A 01/2020

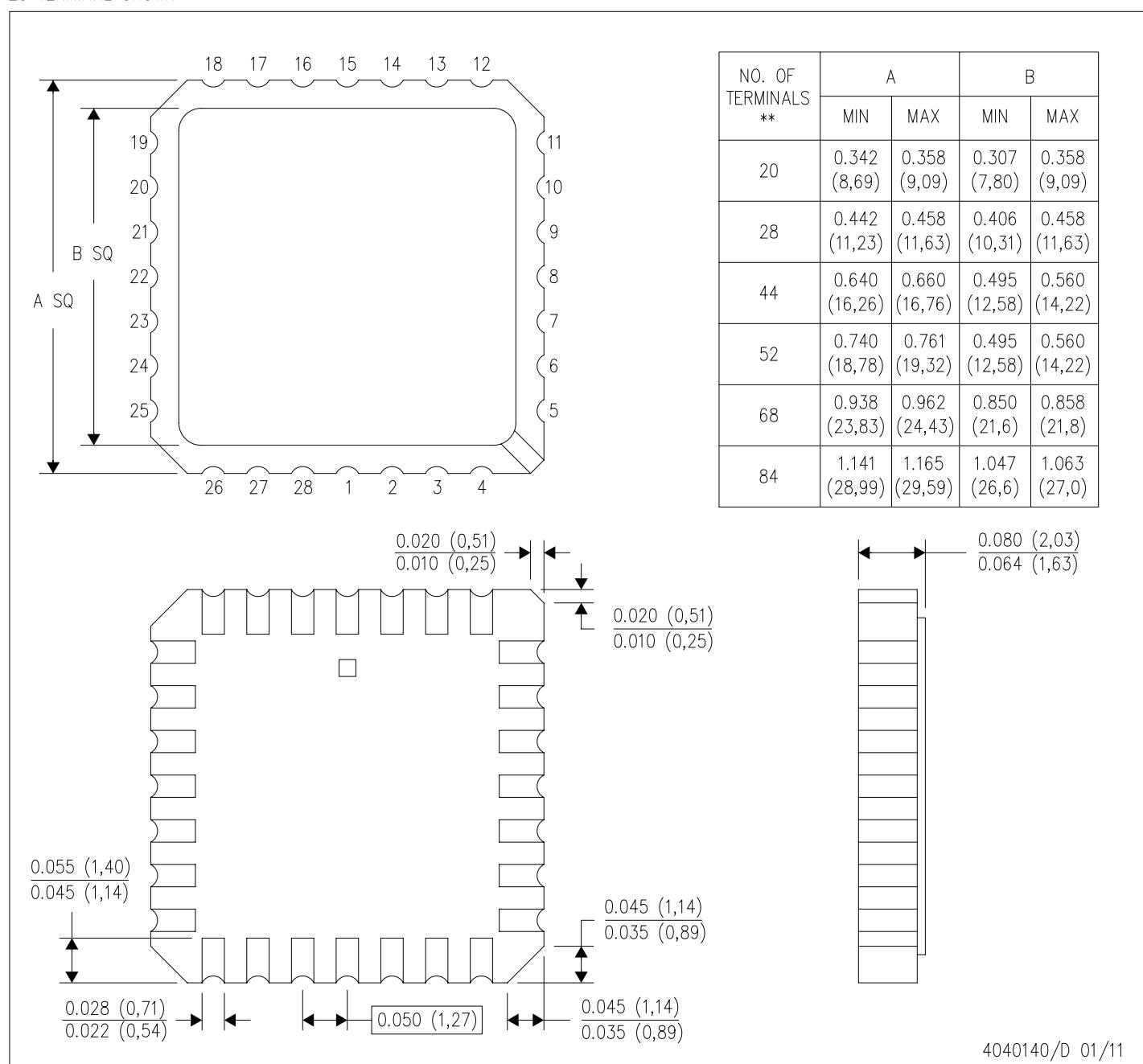
NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



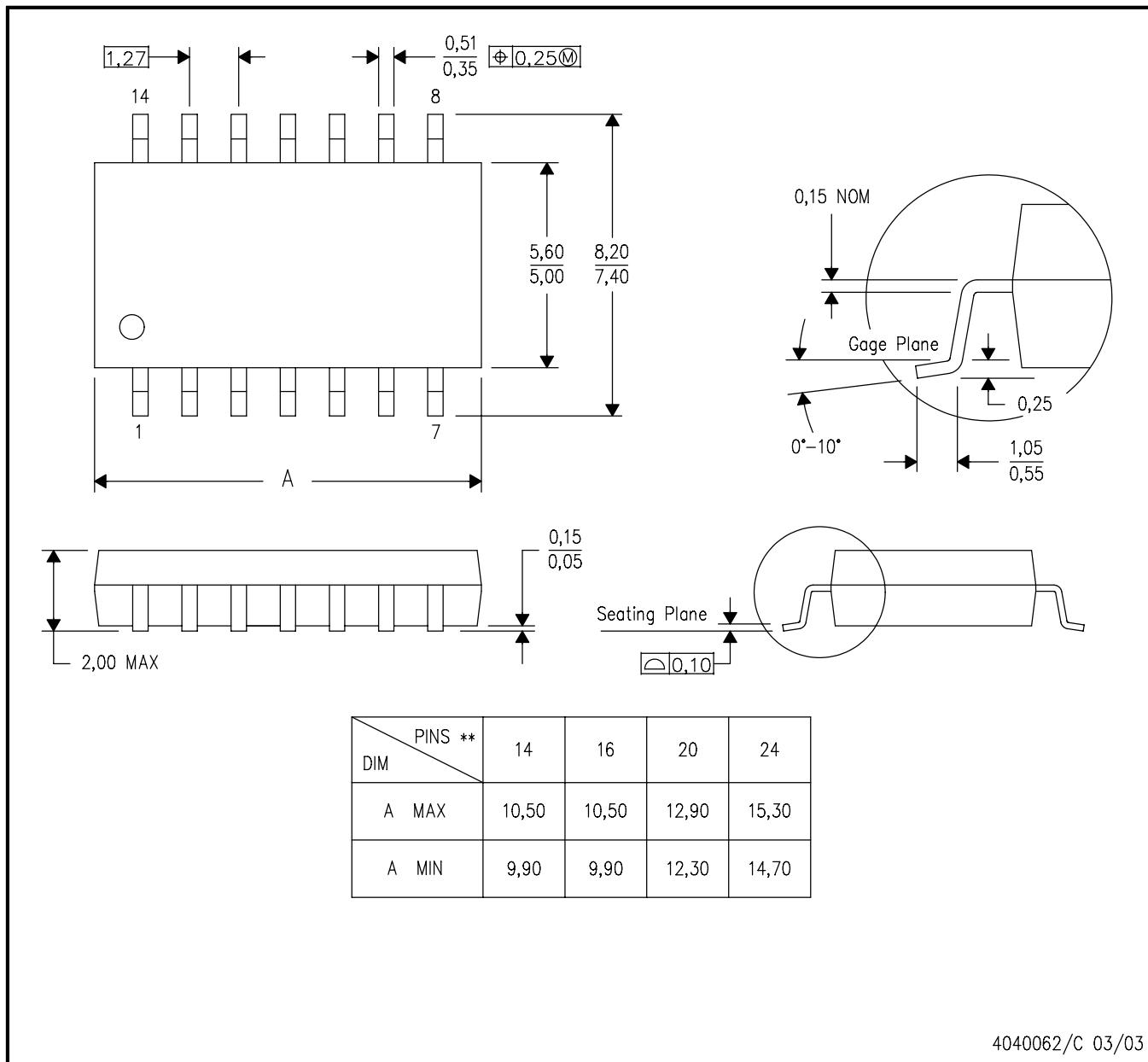
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

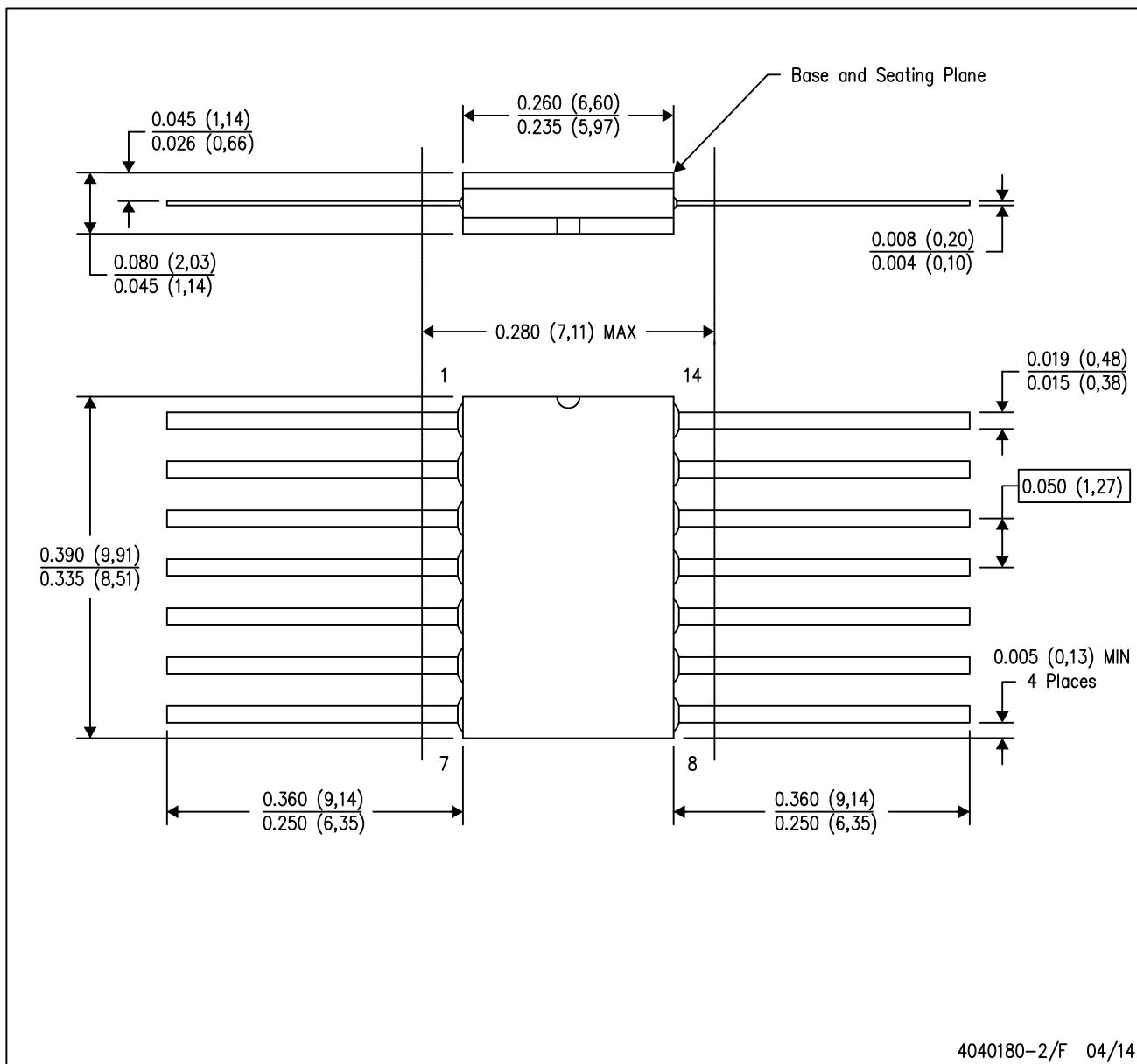


4040062/C 03/03

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

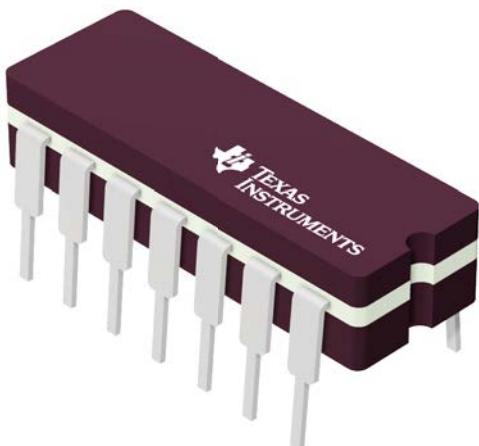
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

J 14

CDIP - 5.08 mm max height

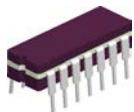
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

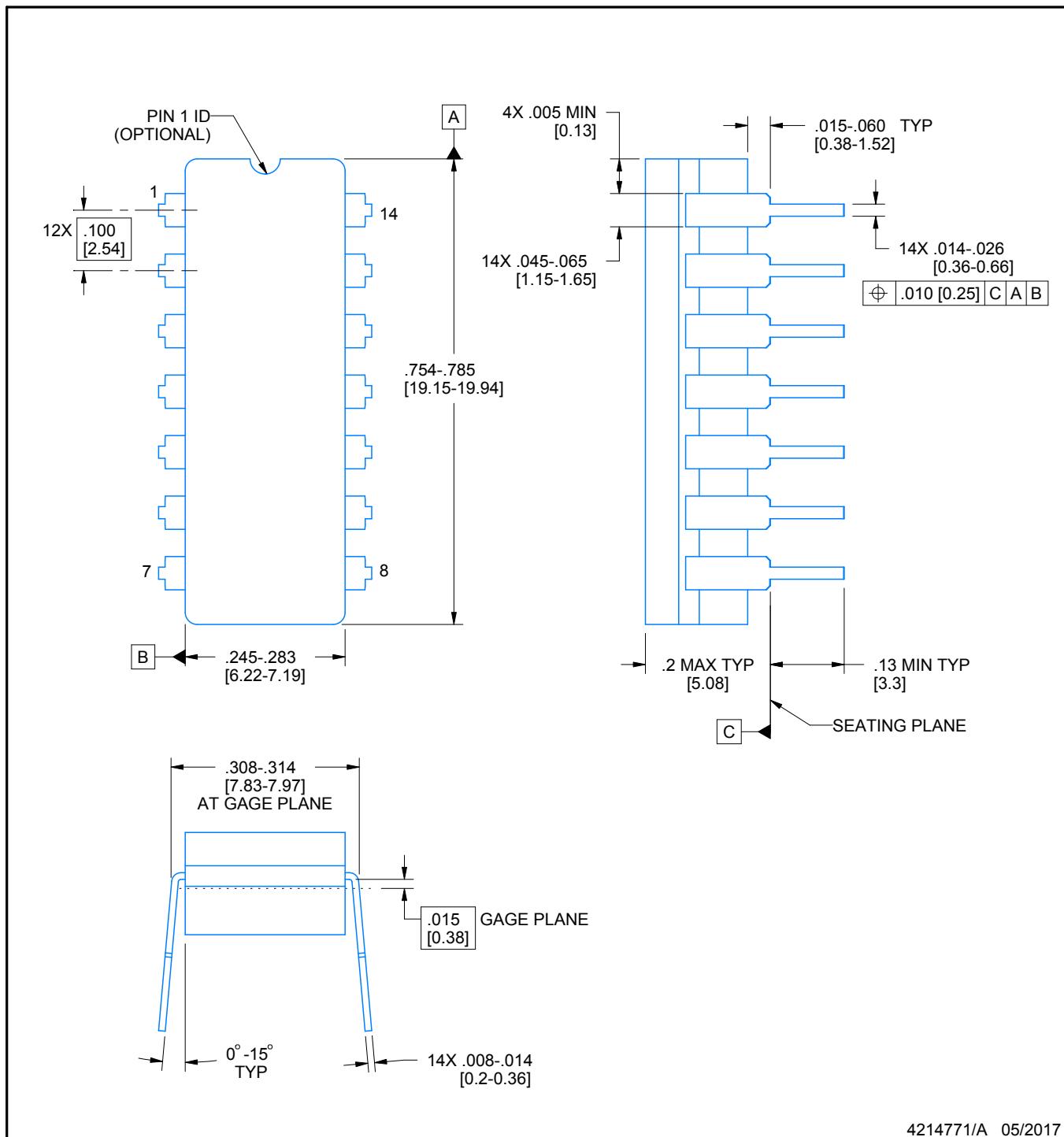
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

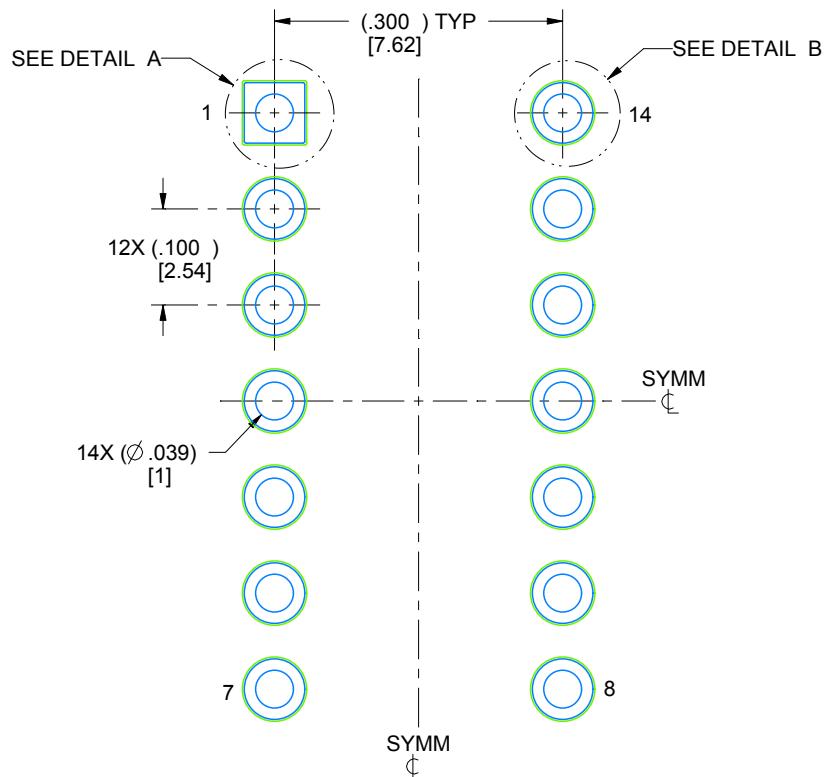
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

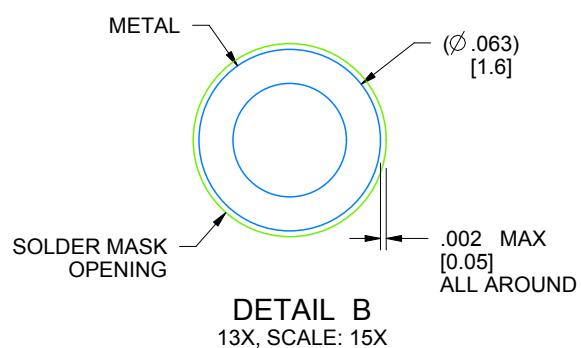
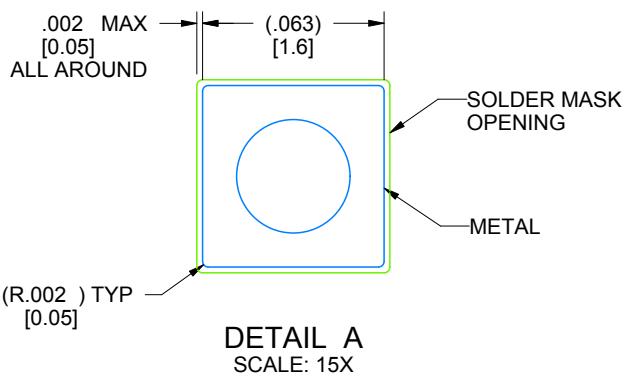
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



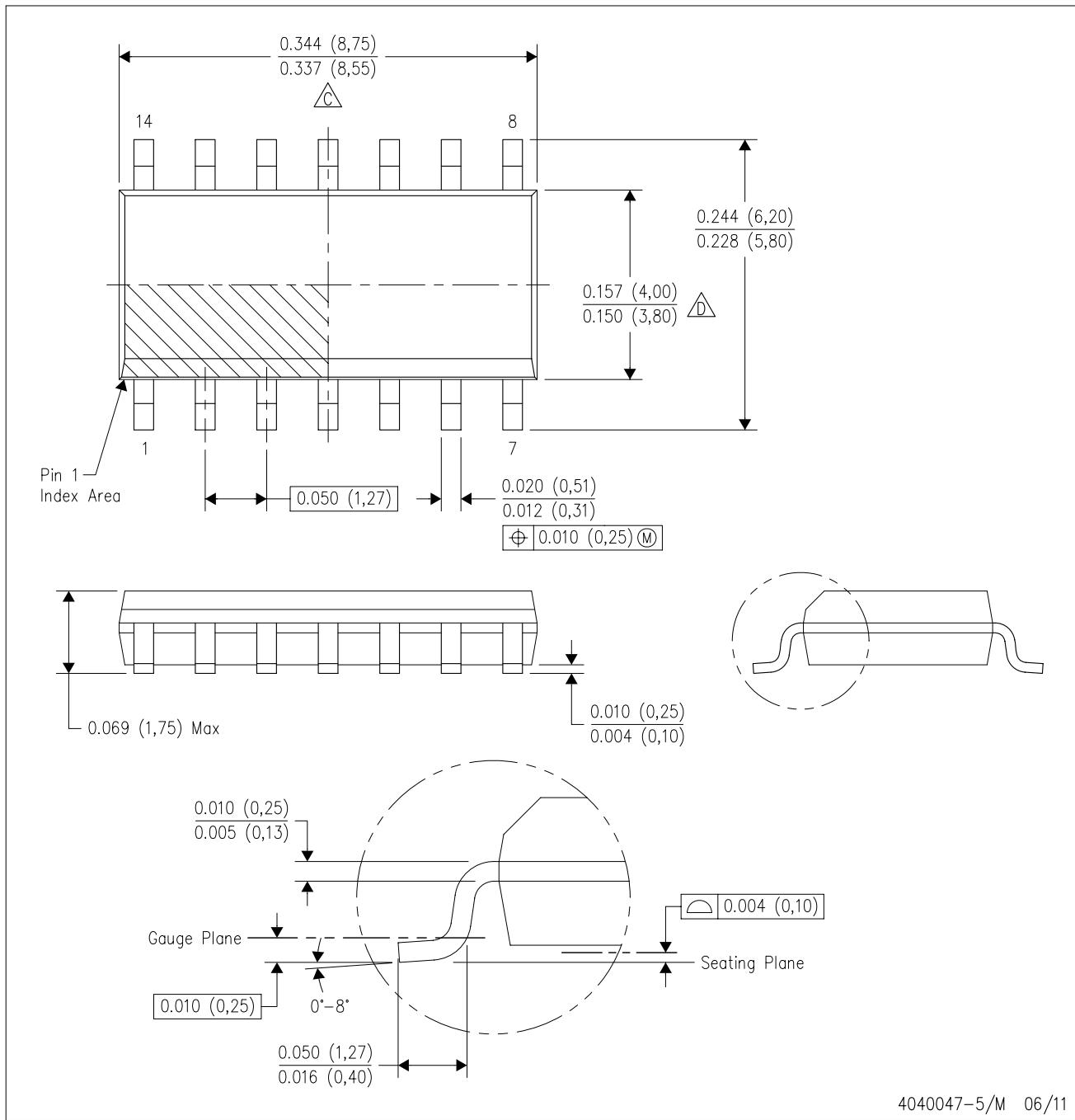
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

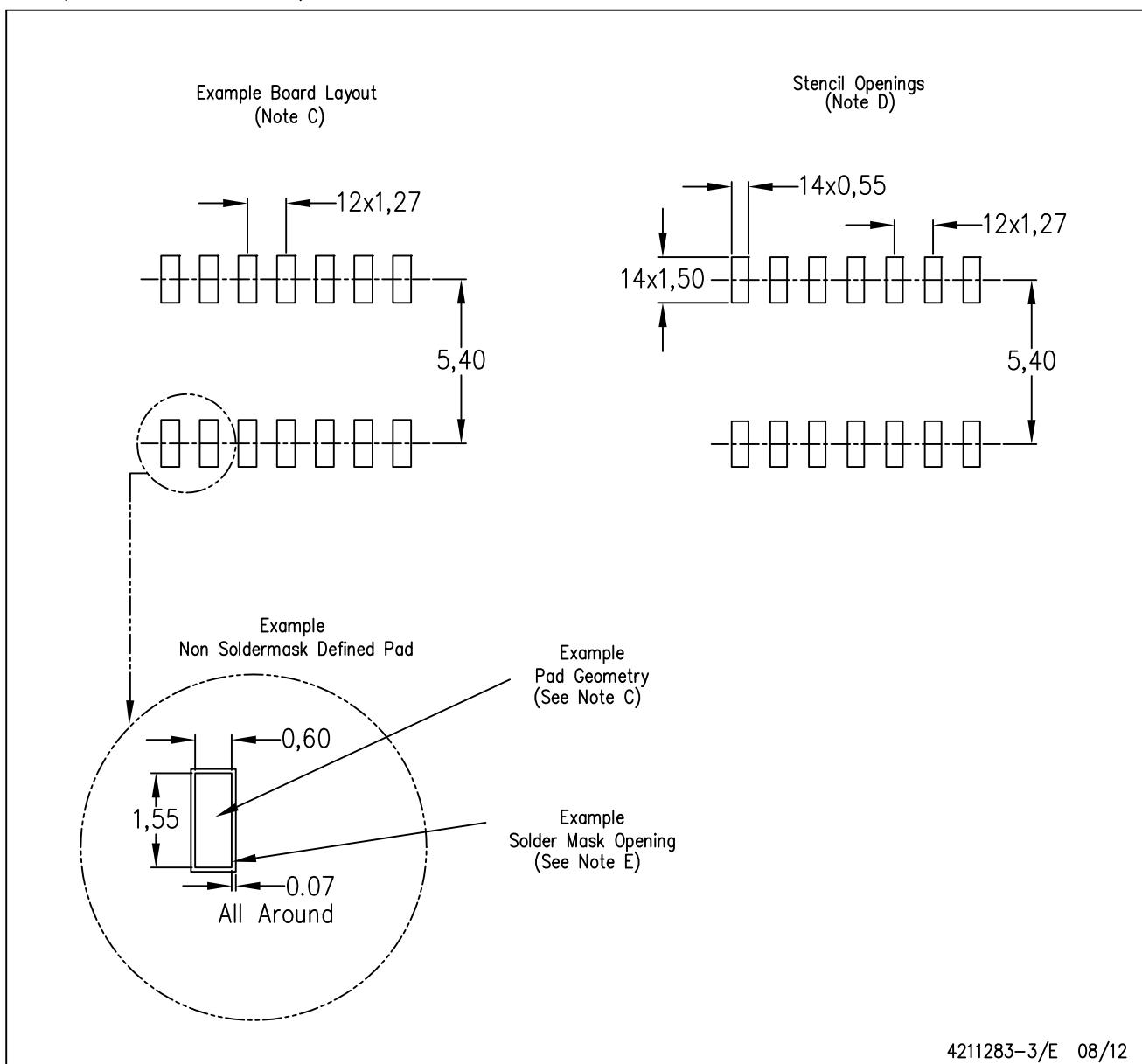
B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



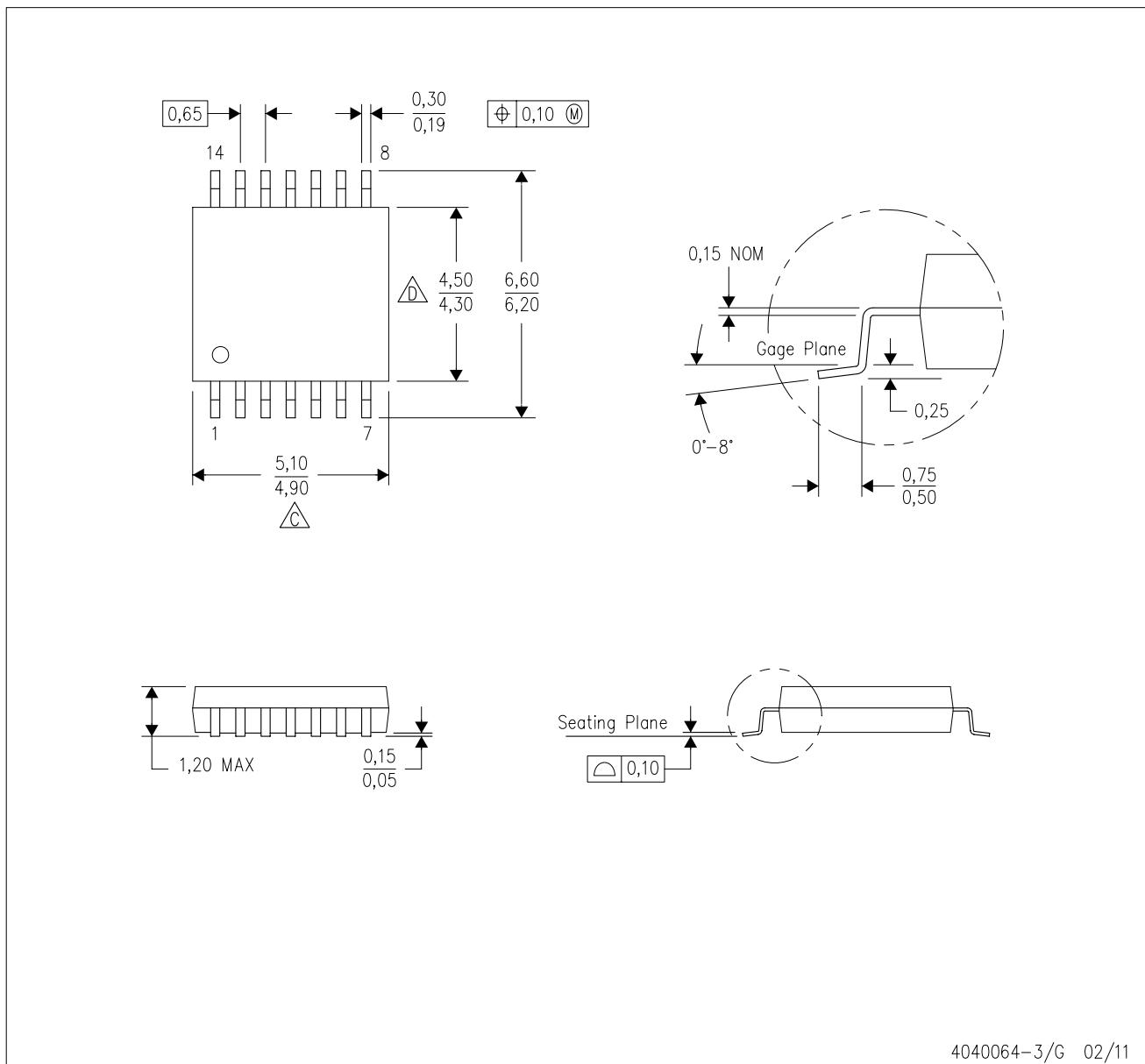
4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

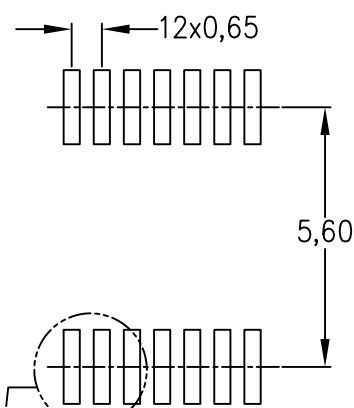
4040064-3/G 02/11

LAND PATTERN DATA

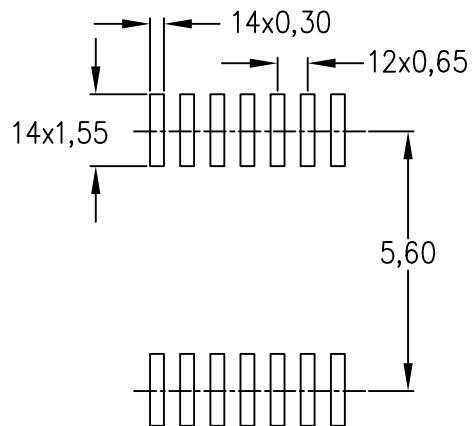
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

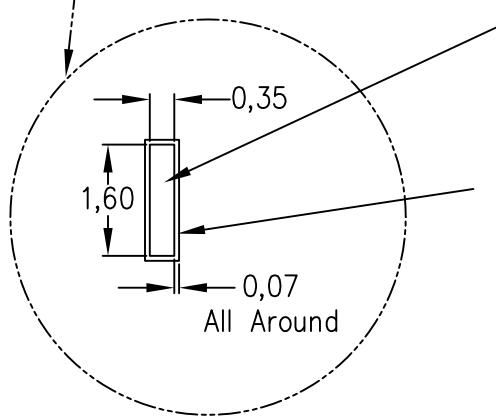
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



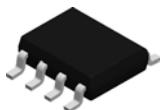
Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

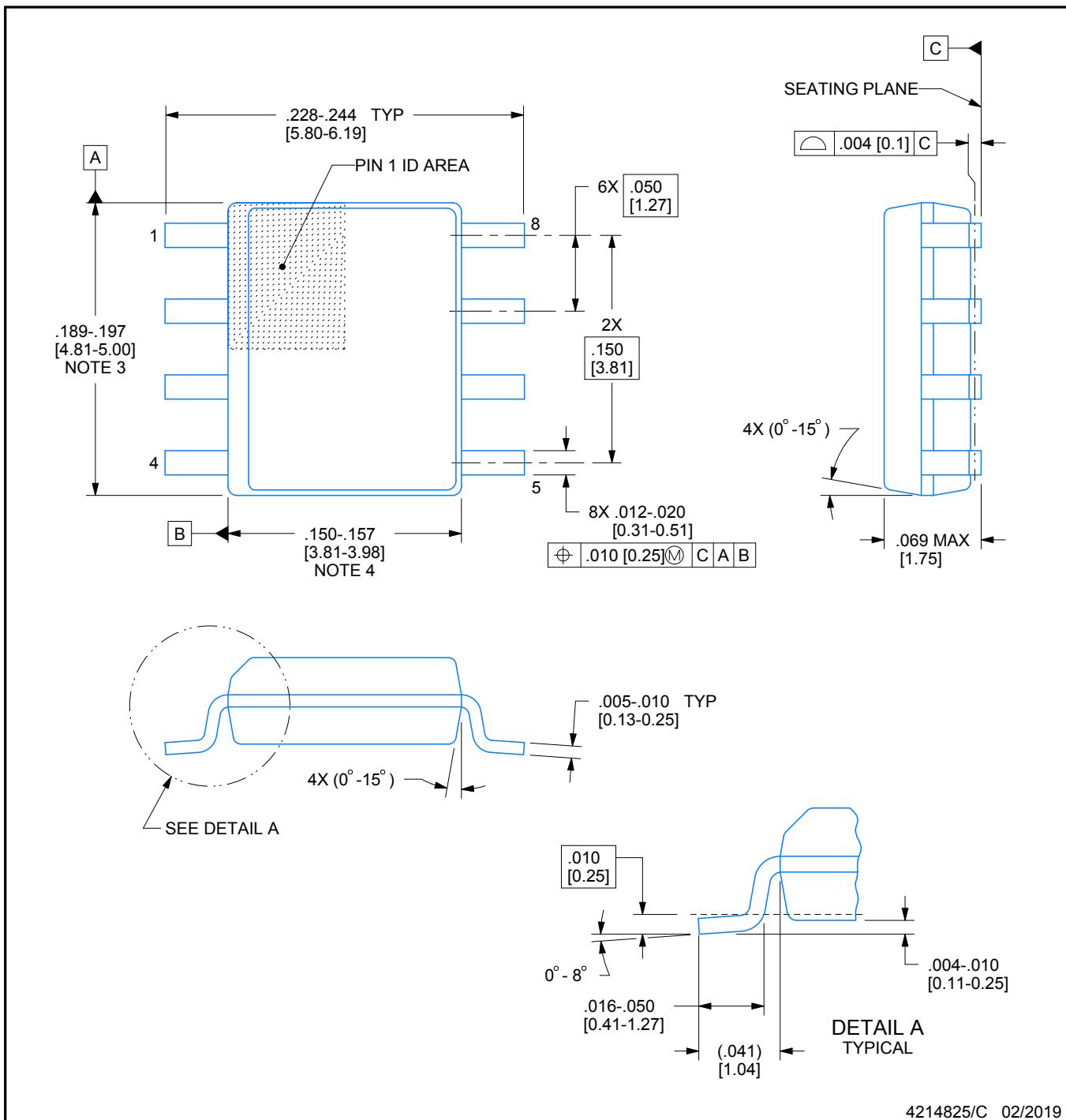
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

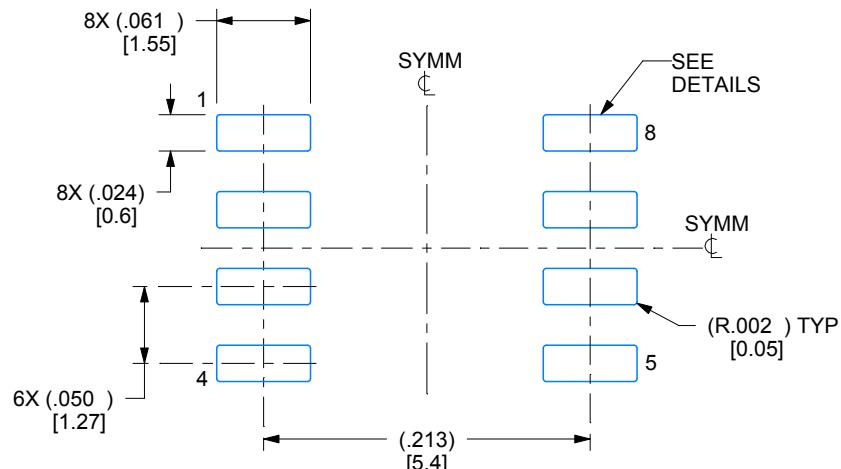
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

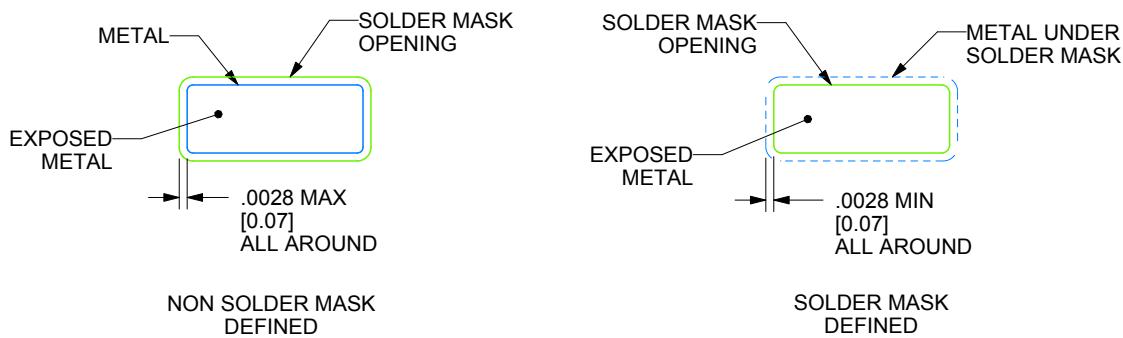
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

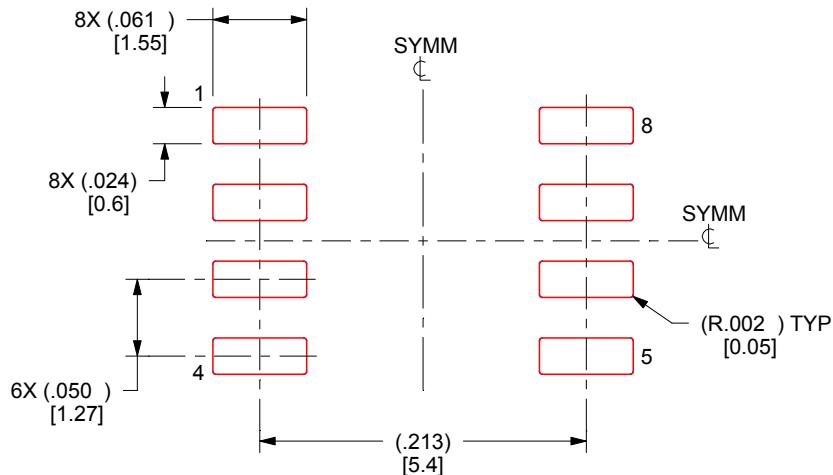
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

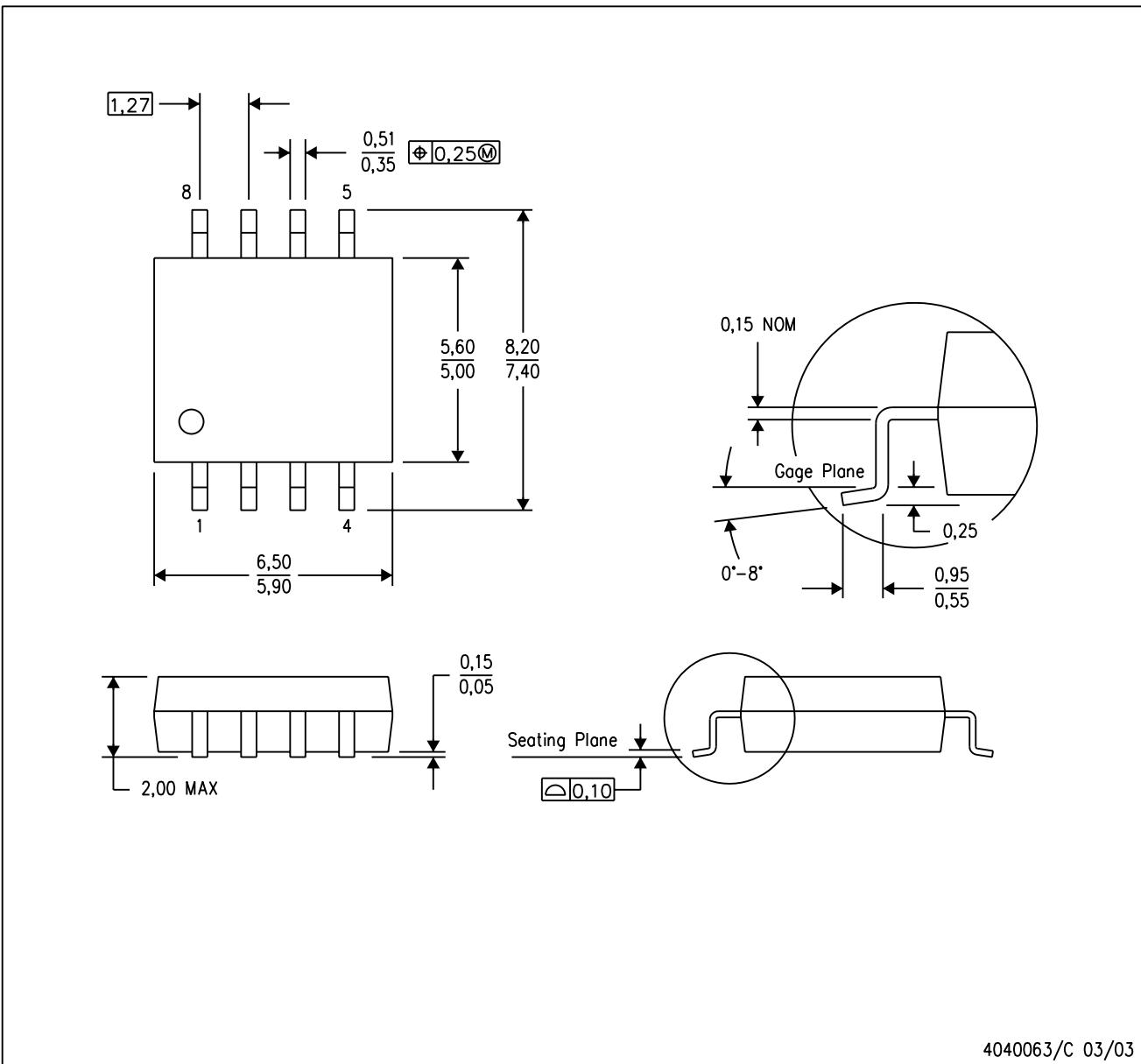
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

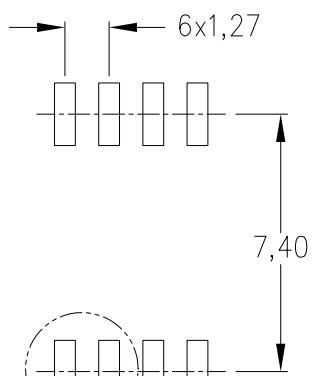
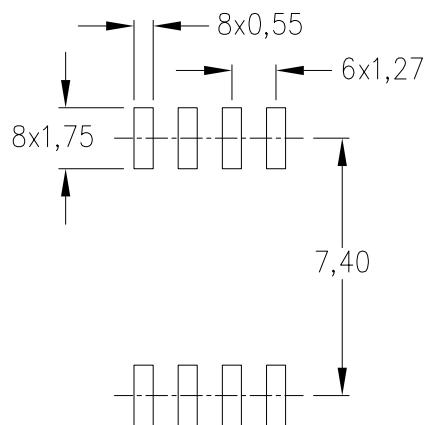
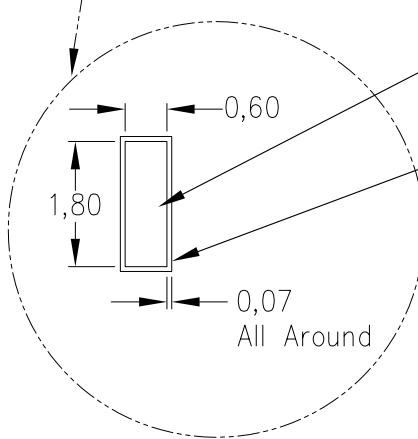


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE

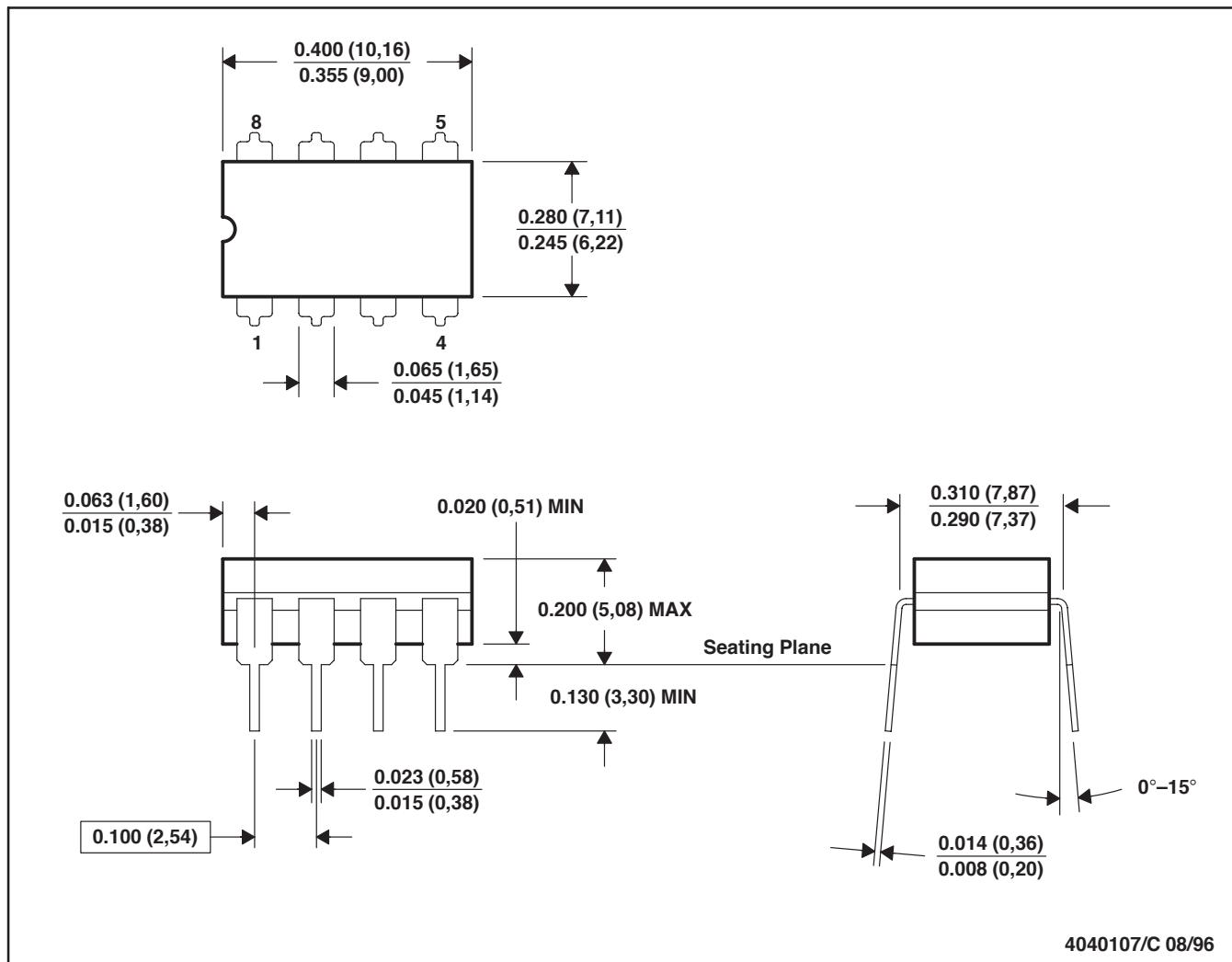
Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Non-Solder Mask Opening
(See Note E)

4212188/A 09/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

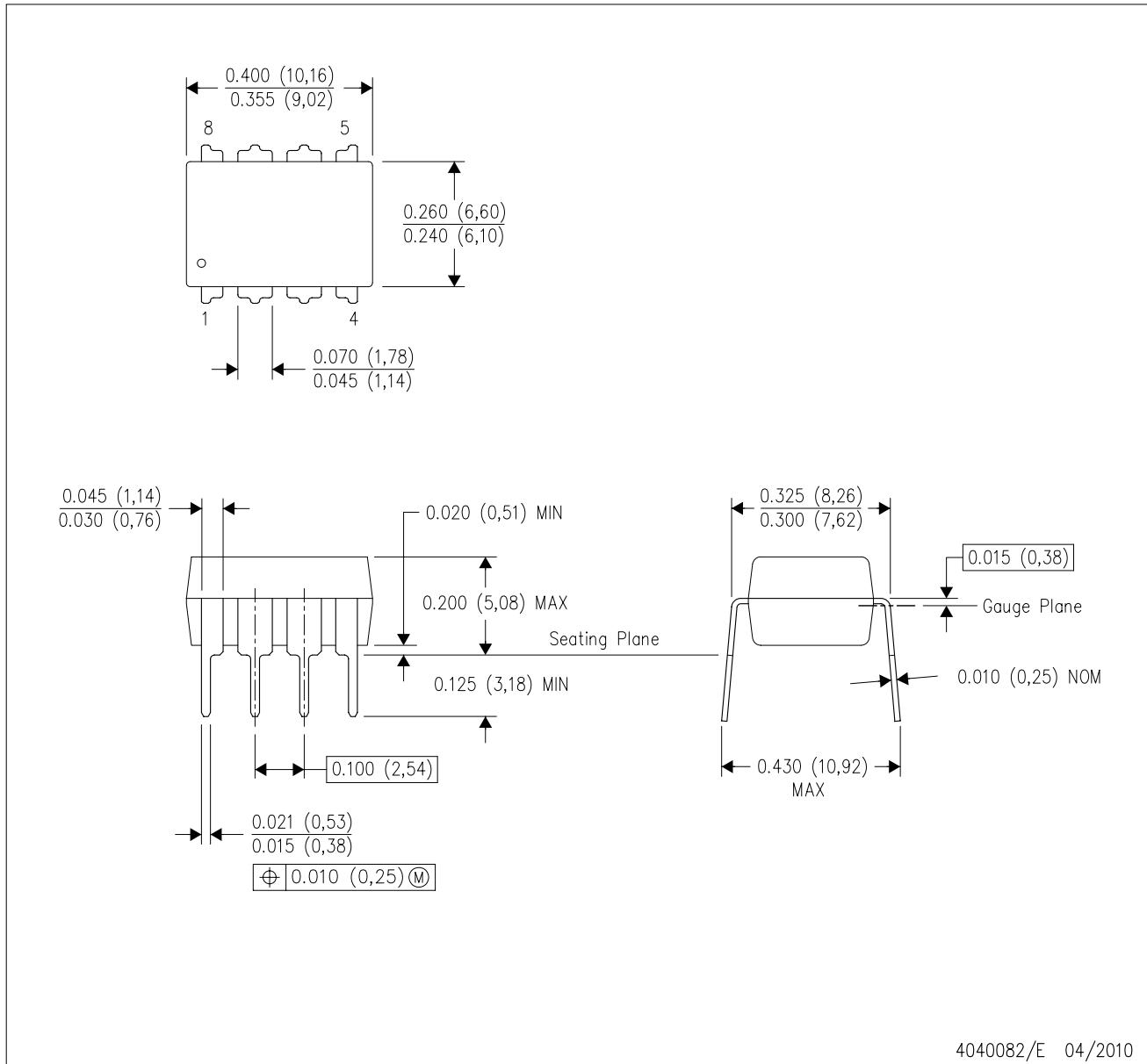


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



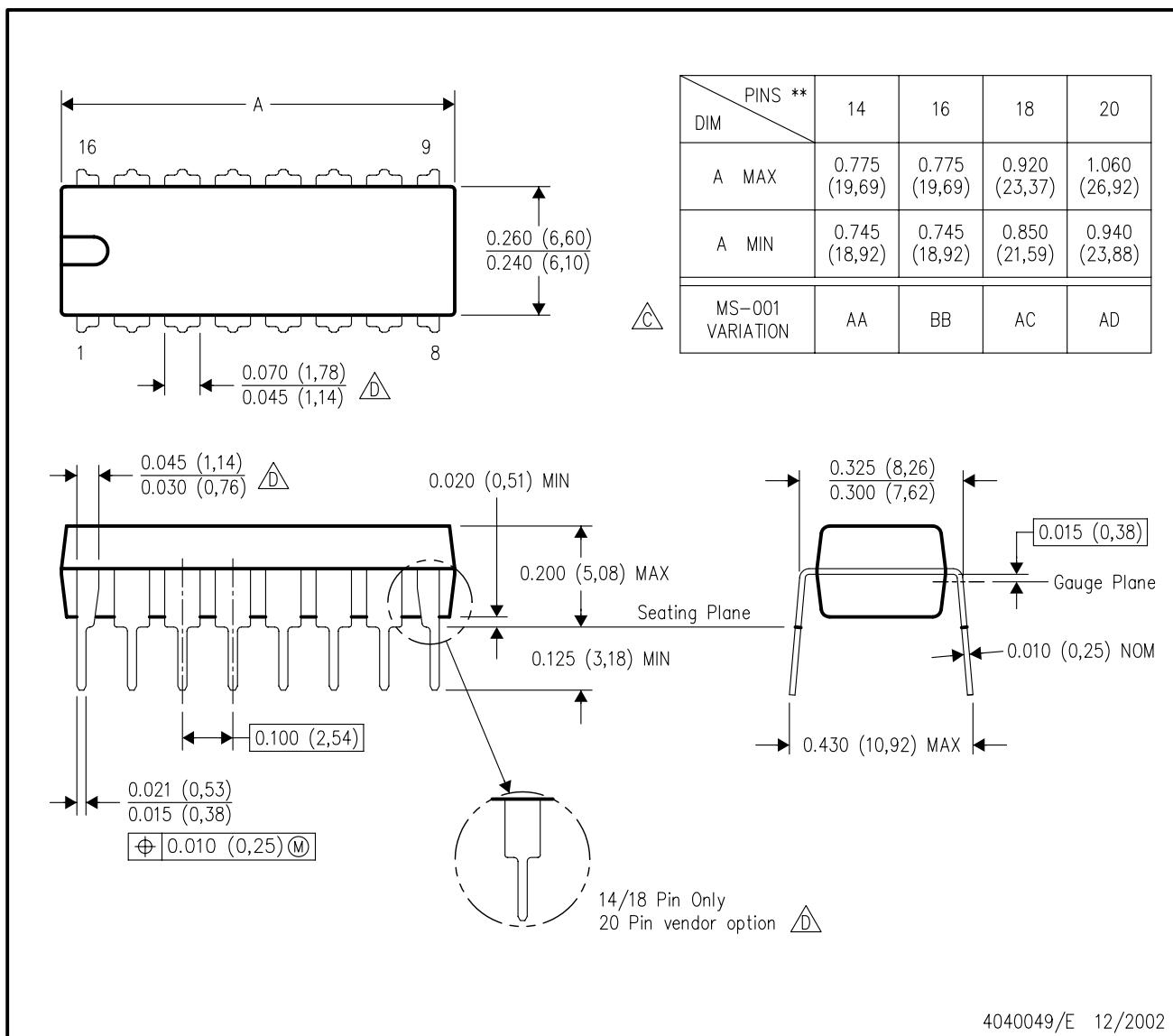
4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

Symbol C: Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

Symbol D: The 20 pin end lead shoulder width is a vendor option, either half or full width.

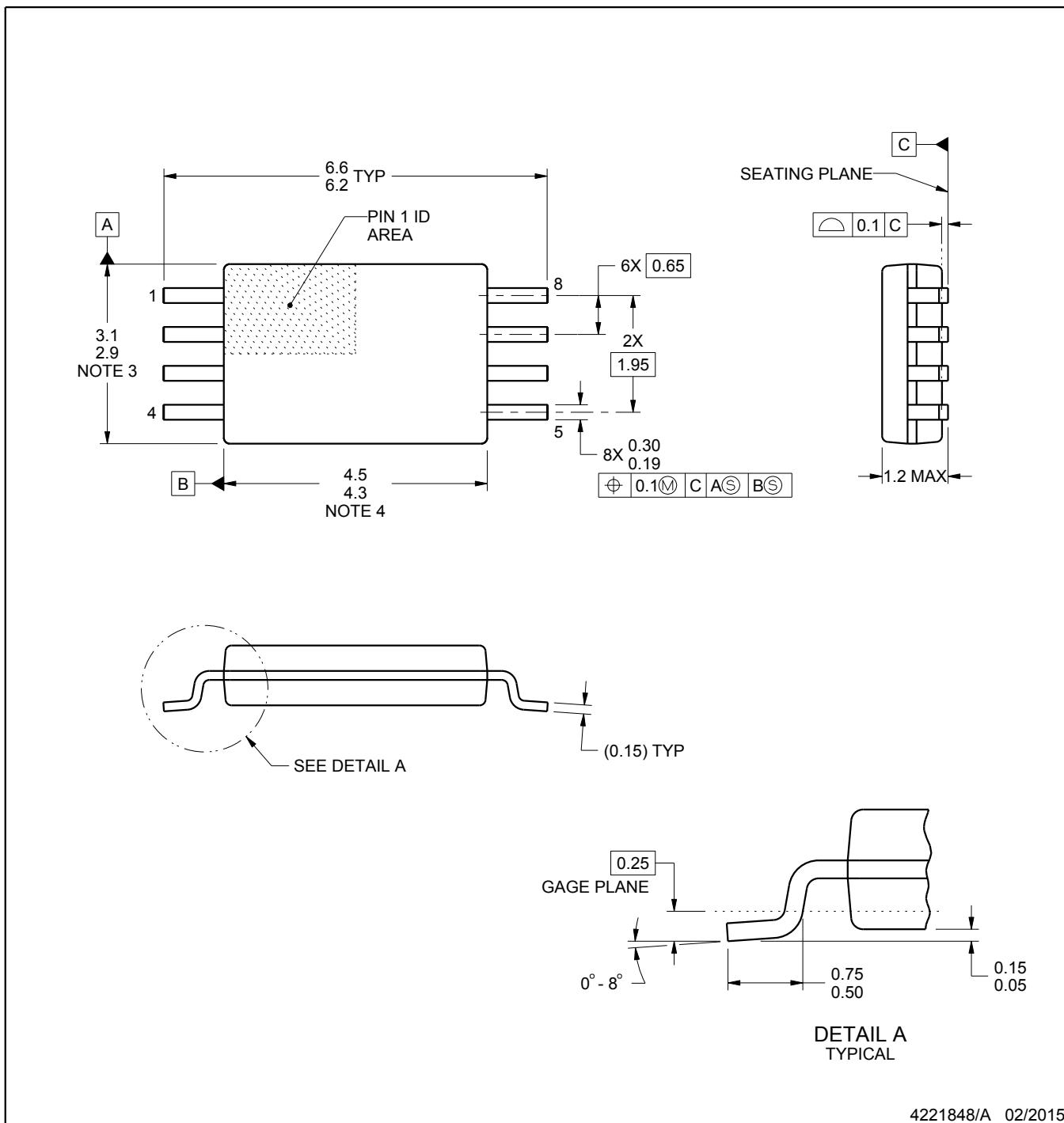
PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

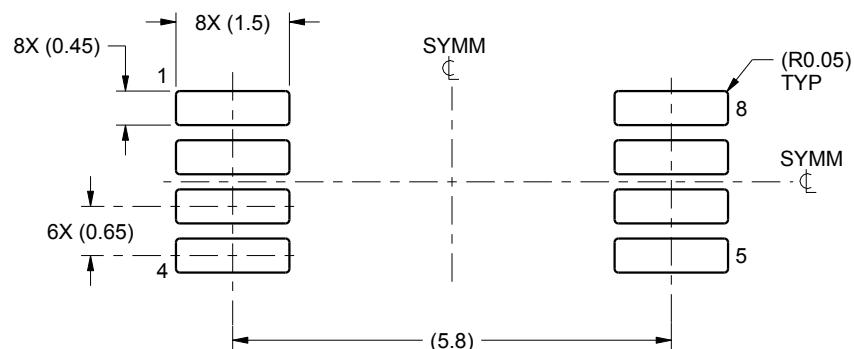
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

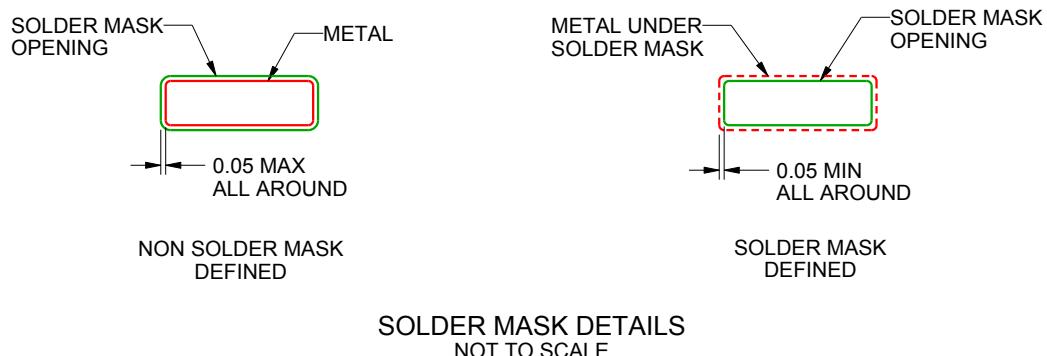
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

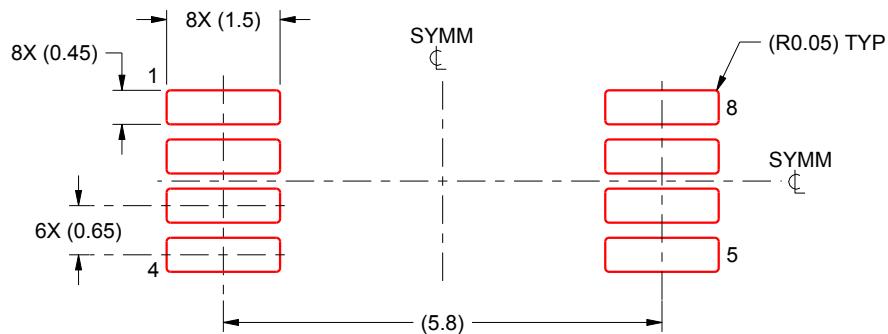
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

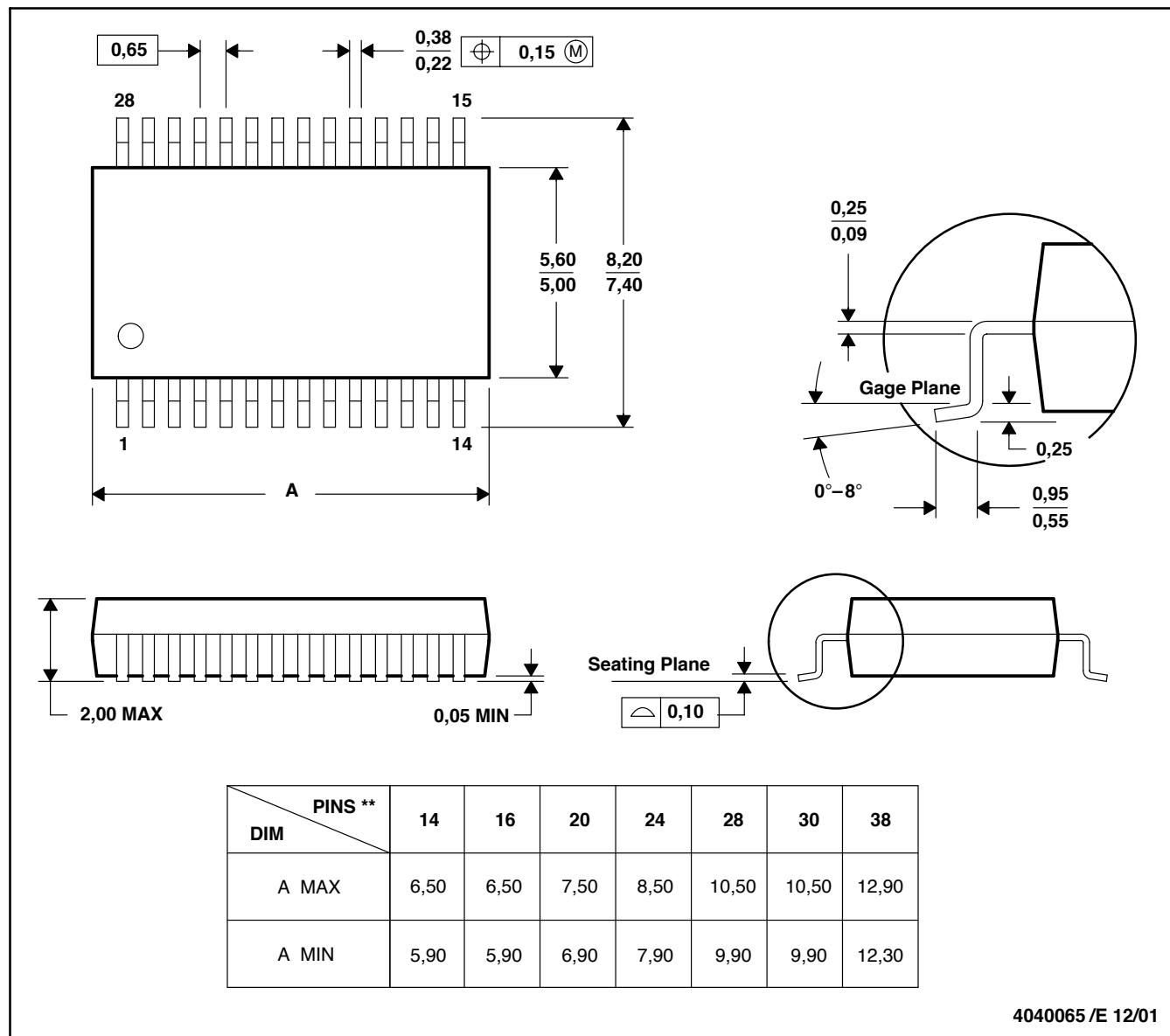
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-150

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FEATURES

- Guaranteed 200pA max. input offset current
- Guaranteed 2nA max. input bias current
- Guaranteed 600 μ A max. supply current
- Guaranteed 0.5mV max. offset voltage
- Guaranteed 5 μ V/ $^{\circ}$ C max. drift
- Wide supply voltage range: \pm 2V to \pm 18V

APPLICATIONS

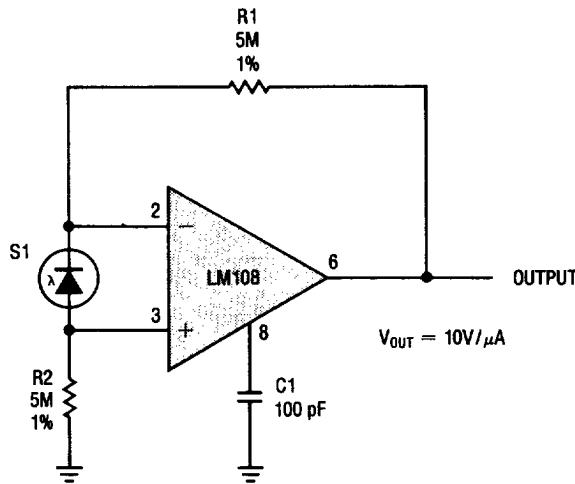
- Integrators
- Transducer amplifiers
- Analog memories
- Light meters

DESCRIPTION

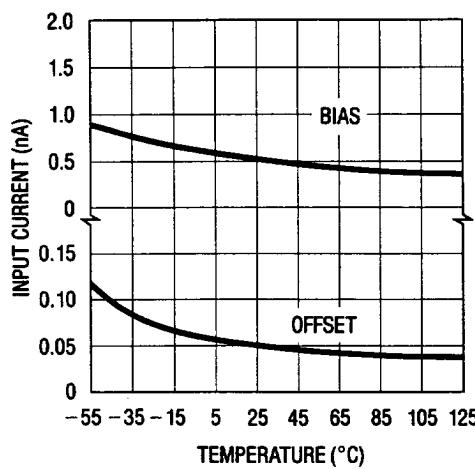
The LM108 series of precision operational amplifiers are particularly well-suited for high source impedance applications requiring low offset and bias currents as well as low power dissipation. Unlike FET input amplifiers, the offset and bias currents of the LM108 do not change significantly with temperature variations. Advanced design, processing and testing techniques make Linear's LM108 a superior choice over previous devices.

A photodiode sensor application is shown below. For applications requiring higher performance, see the LT1008, and LT1012. 2

Amplifier For Photodiode Sensor



Input Currents



ABSOLUTE MAXIMUM RATINGS

Supply Voltage

LM108A/LM108 $\pm 20V$

LM308A/LM308 $\pm 18V$

Differential Input Current (Note 1) $\pm 10mA$

Input Voltage (Note 2) $\pm 15V$

Output Short Circuit Duration Indefinite

Operating Temperature Range

LM108A/LM108 $-55^{\circ}C$ to $125^{\circ}C$

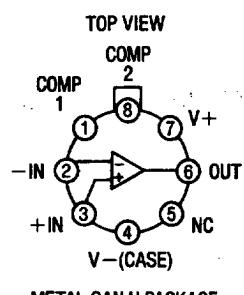
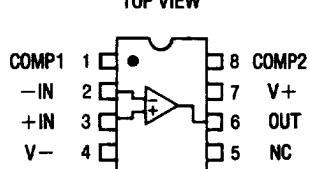
LM308A/LM308 $0^{\circ}C$ to $70^{\circ}C$

Storage Temperature Range

All Devices $-65^{\circ}C$ to $150^{\circ}C$

Lead Temperature (Soldering, 10 sec.) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

ORDER PART NO.
 METAL CAN H PACKAGE
 PLASTIC DIP N8 PACKAGE

ELECTRICAL CHARACTERISTICS $\pm 5V \leq V_S \leq \pm 20V$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LM108A			LM108			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$T_A = 25^{\circ}C$	●	0.3	0.5	0.7	2.0	3.0	mV
●				1.0	1.0	3.0	15	15	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Voltage		●	1.0	5.0	3.0	15	15	$\mu V/^{\circ}C$
I_{OS}	Input Offset Current	$T_A = 25^{\circ}C$	●	0.05	0.2	0.05	0.2	0.4	nA
●				0.4	0.4	0.4	0.4	0.4	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Current		●	0.5	2.5	0.5	2.5	2.5	pA/ $^{\circ}C$
I_B	Input Bias Current	$T_A = 25^{\circ}C$	●	0.5	2.0	0.5	2.0	3.0	nA
●				3.0	3.0	3.0	3.0	3.0	nA
A_{VOL}	Large Signal Voltage Gain	$T_A = 25^{\circ}C, V_S \pm 15V, V_{OUT} = \pm 10V, R_L \geq 10k\Omega$	●	80	300	50	300	25	V/mV
●				40	40	25	25	25	V/mV
CMRR	Common Mode Rejection Ratio		●	96	110	85	100	85	dB
PSRR	Power Supply Rejection Ratio		●	96	110	80	96	80	dB
V_S	Input Voltage Range	$V_S = \pm 15V$	●	± 13.5		± 13.5		± 13.5	V
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V, R_L = 10k\Omega$	●	± 13	± 14	± 13	± 14	± 13	V
R_{IN}	Input Resistance	$T_A = 25^{\circ}C$ (Note 3)		30	70	30	70	30	M Ω
I_S	Supply Current	$T_A = 25^{\circ}C$ $T_A = 125^{\circ}C$		0.3	0.6	0.3	0.6	0.3	mA
				0.15	0.4	0.15	0.4	0.15	mA

ELECTRICAL CHARACTERISTICS $\pm 5V \leq V_s \leq \pm 15V$ and $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LM308A			LM308			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$T_A = 25^\circ C$	●	0.3	0.5	2.0	7.5	10	mV
●				0.73					mV
$\Delta V_{OS}/\Delta Temp$	Average Temperature Coefficient of Input Offset Voltage		●	2.0	5.0	6.0	30		$\mu V/^\circ C$
I_{OS}	Input Offset Current	$T_A = 25^\circ C$	●	0.2	1.0	0.2	1.0	1.5	nA
●				1.5					nA
$\Delta I_{OS}/\Delta Temp$	Average Temperature Coefficient of Input Offset Current		●	2.0	10	2.0	10		pA/°C
I_B	Input Bias Current	$T_A = 25^\circ C$	●	1.5	7.0	1.5	7.0	10	nA
●				10					nA
A_{VOL}	Large Signal Voltage Gain	$T_A = 25^\circ C, V_s = \pm 15V, V_{OUT} = \pm 10V, R_L \geq 10k\Omega$	●	80	300	25	300		V/mV
●				60		15			V/mV
CMRR	Common Mode Rejection Ratio		●	96	110	80	100		dB
PSRR	Power Supply Rejection Ratio		●	96	110	80	96		dB
Input Voltage Range	$V_s = \pm 15V$		●	±14		±14			V
V_{OUT}	Output Voltage Swing	$V_s = \pm 15V, R_L = 10k\Omega$	●	±13	±14	±13	±14		V
R_{IN}	Input Resistance	$T_A = 25^\circ C$ (Note 3)		10	40	10	40		MΩ
I_S	Supply Current	$T_A = 25^\circ C$			0.3	0.8	0.3	0.8	mA

2

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC 883 data sheet for test listing and parameters.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless current limiting resistance is used.

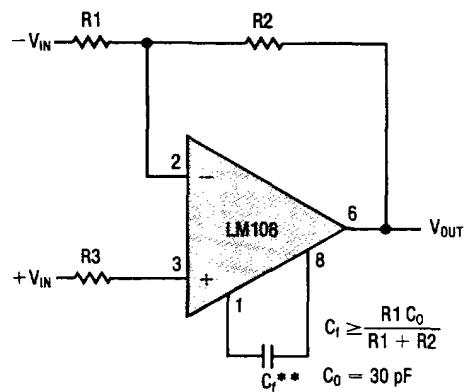
Note 2: For supply voltages less than $\pm 15V$, the maximum input voltage is equal to the supply voltage.

Note 3: Guaranteed by design.

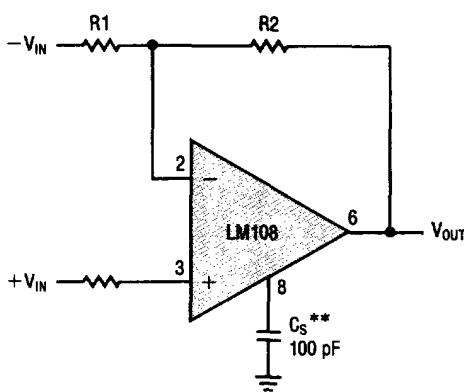
TYPICAL APPLICATIONS

COMPENSATION CIRCUITS

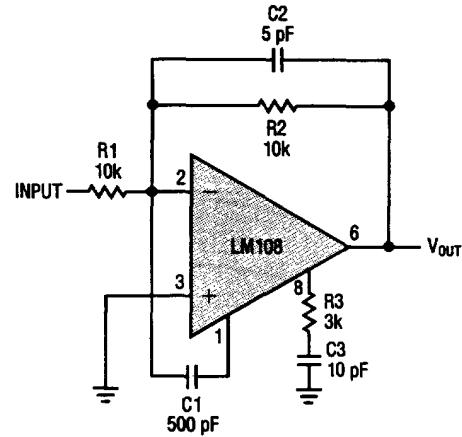
Standard Compensation Circuit



Alternate* Frequency Compensation



Feedforward Compensation



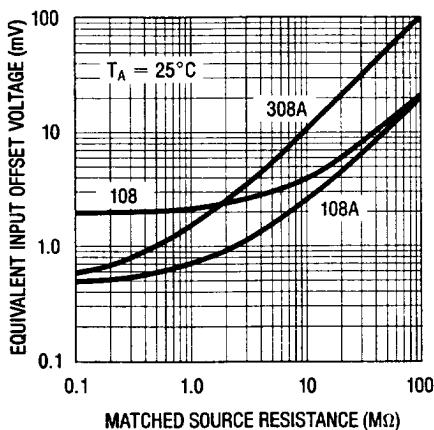
** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO $1/C_1$

* IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TEN.

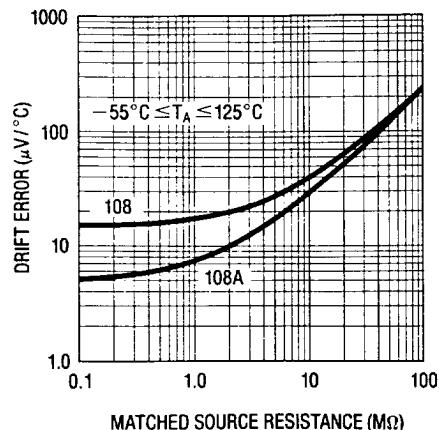
** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO $1/C_s$

TYPICAL PERFORMANCE CHARACTERISTICS

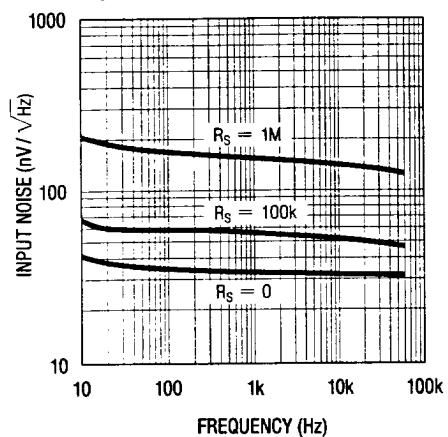
Guaranteed Offset Error



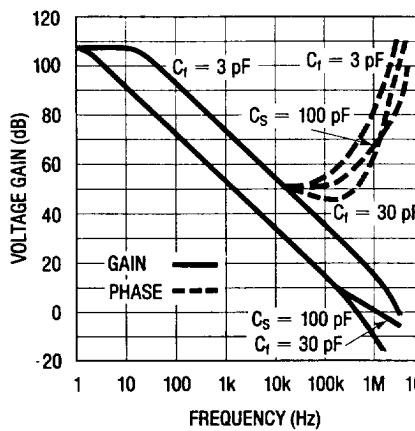
Guaranteed Drift Error



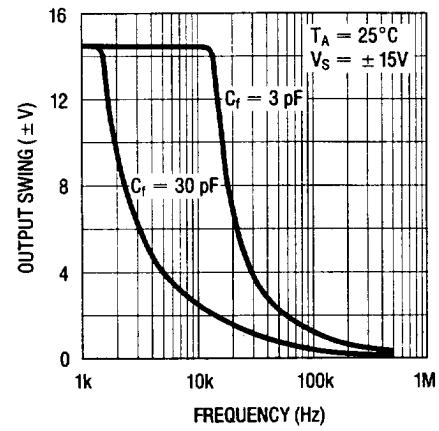
Input Noise Voltage



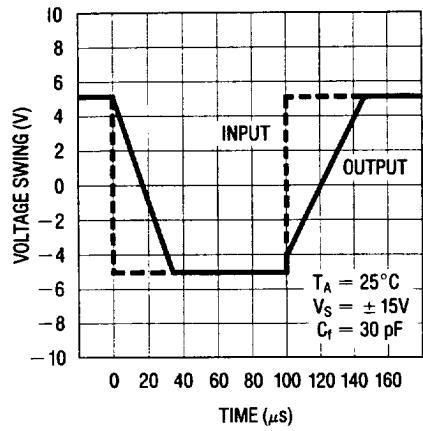
Open Loop Frequency Response



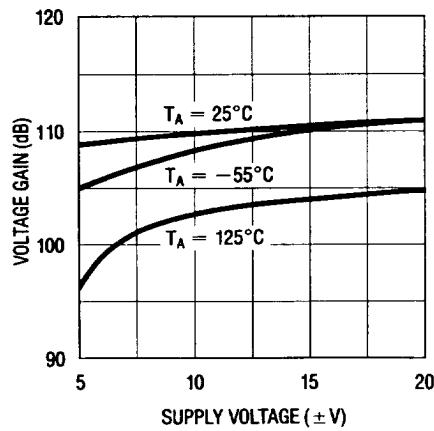
Large Signal Frequency Response



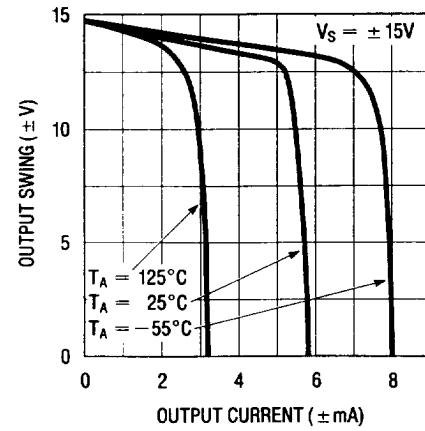
Voltage Follower Pulse Response



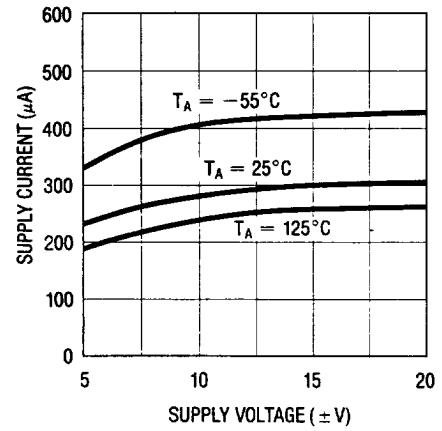
Voltage Gain



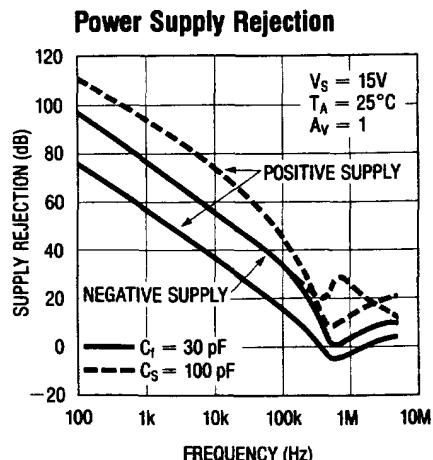
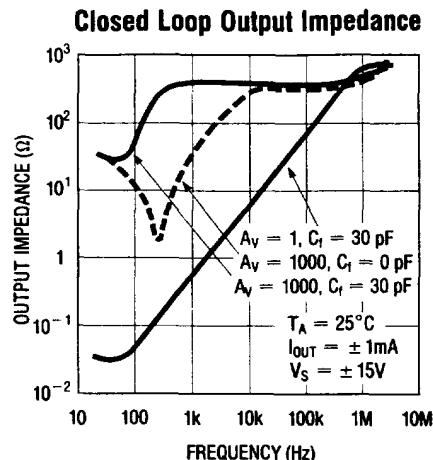
Output Swing



Supply Current



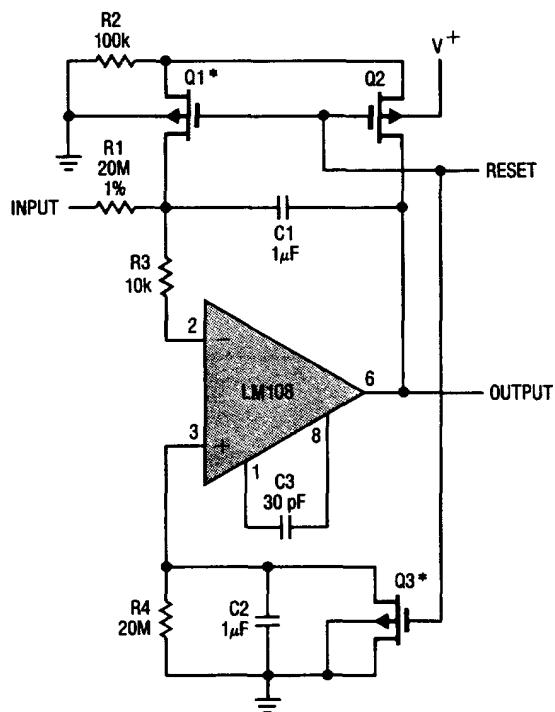
TYPICAL PERFORMANCE CHARACTERISTICS



2

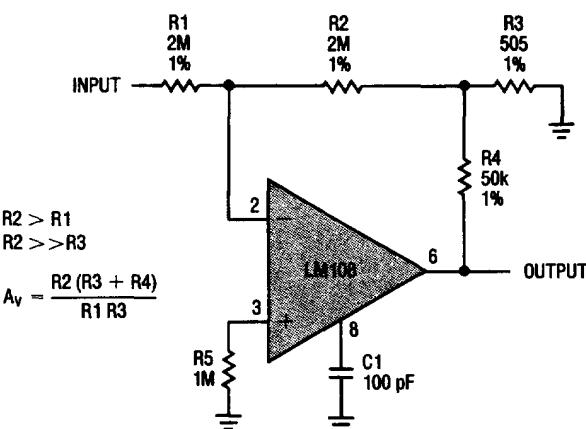
TYPICAL APPLICATIONS

Low Drift Integrator With Reset



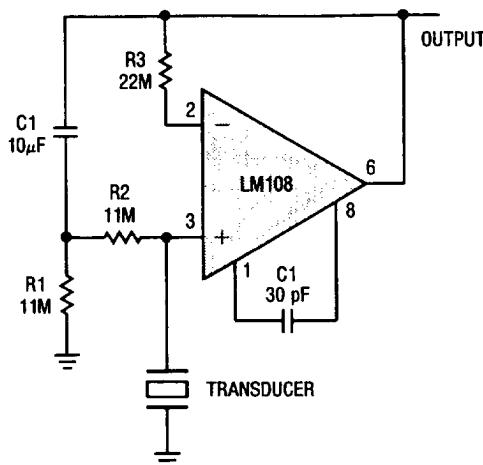
* Q1 AND Q3 SHOULD NOT HAVE INTERNAL GATE-PROTECTION DIODES.

Inverting Amplifier With High Input Resistance

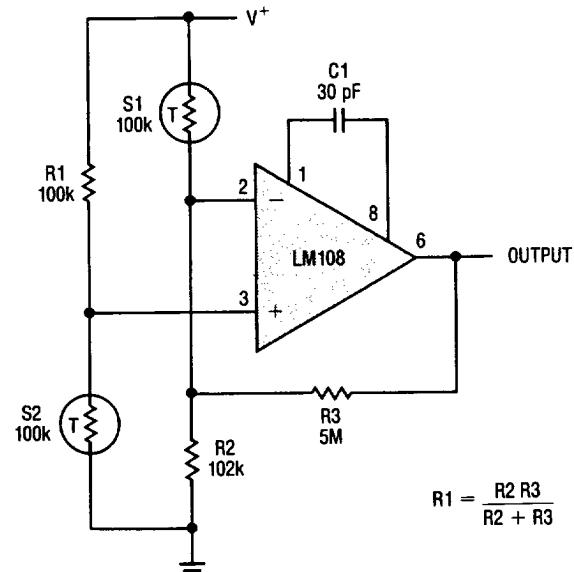


TYPICAL APPLICATIONS

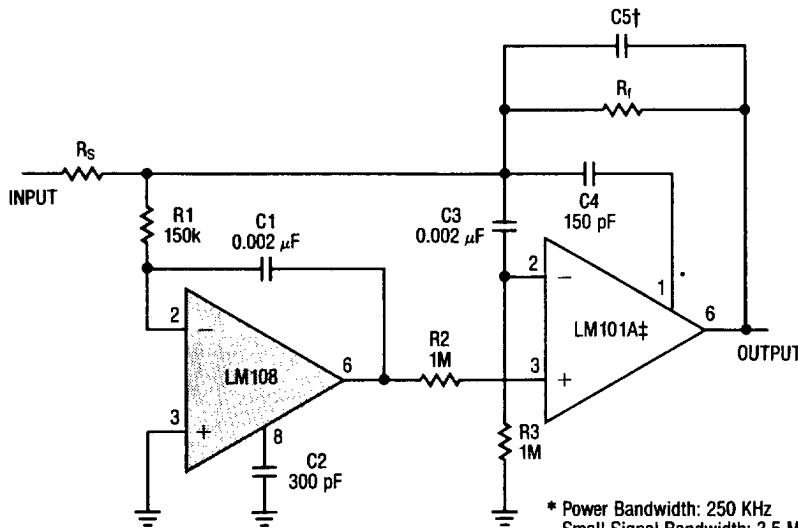
Amplifier For Piezoelectric Transducers



Amplifier For Bridge Transducers



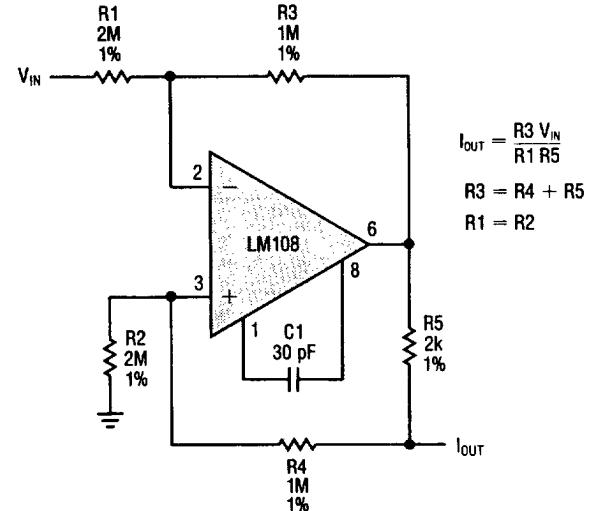
Fast* Summing Amplifier



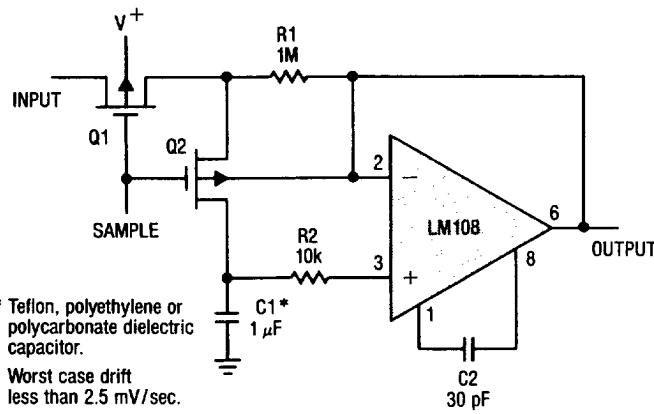
* Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μS
 $\dagger C_5 = \frac{6 \times 10^{-8}}{R_f}$

‡ In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

Bilateral Current Source



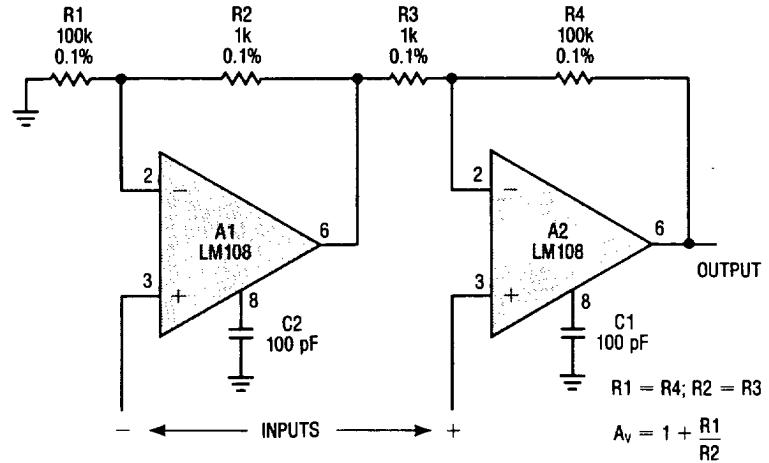
Sample and Hold



* Teflon, polyethylene or polycarbonate dielectric capacitor.

Worst case drift less than 2.5 mV/sec.

Differential Input Instrumentation Amplifier

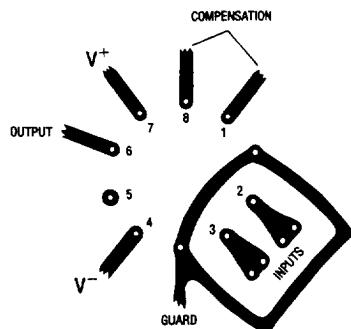


$$A_v = 1 + \frac{R_1}{R_2}$$

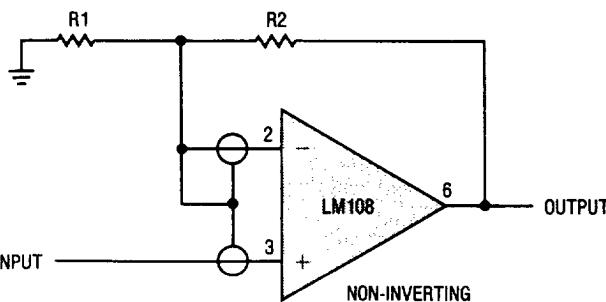
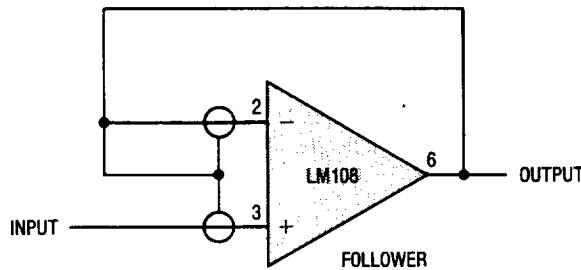
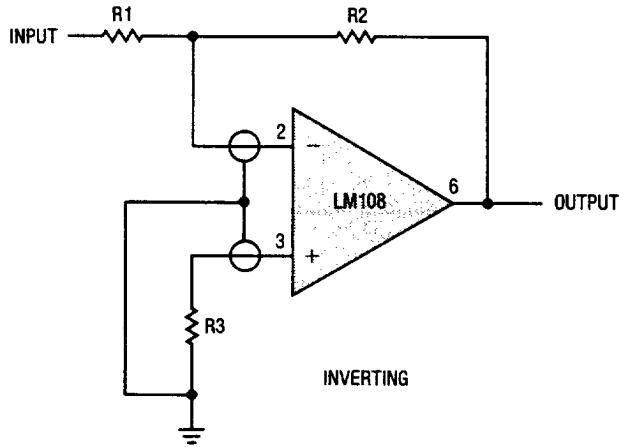
APPLICATIONS INFORMATION

Input guarding

Input guarding is used to reduce surface leakage. Guarding both sides of the board is required. Bulk leakage reduction is less and depends on the guard ring width.

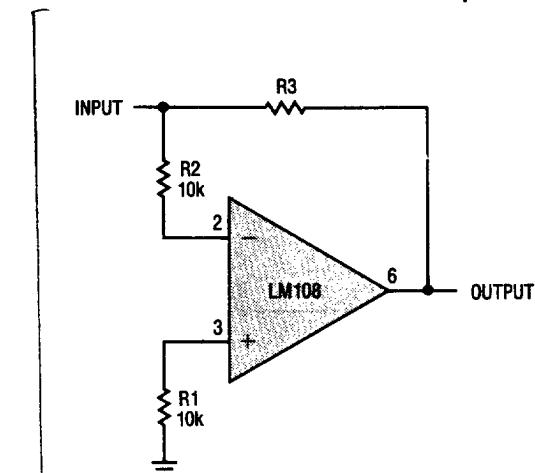


The guard ring is connected to a low impedance point at same potential as the sensitive input leads. Connections for various op amp configurations are shown below.

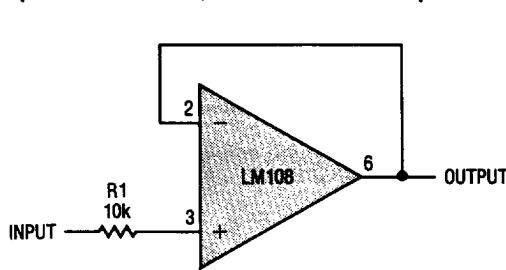


Input protection

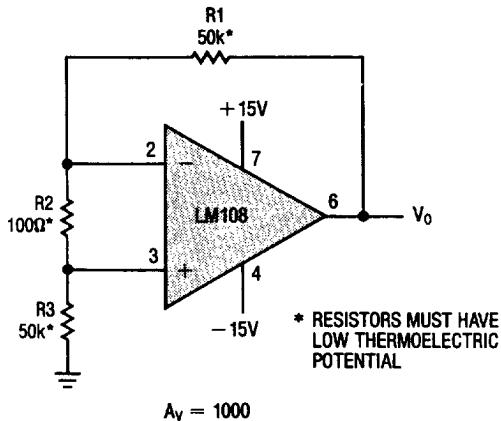
Current is limited by R2 even when input is connected to a voltage source outside the common mode range. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation.



The input resistor controls the current when the input exceeds the supply voltages, when the power for the op amp is turned off, or when the output is shorted.

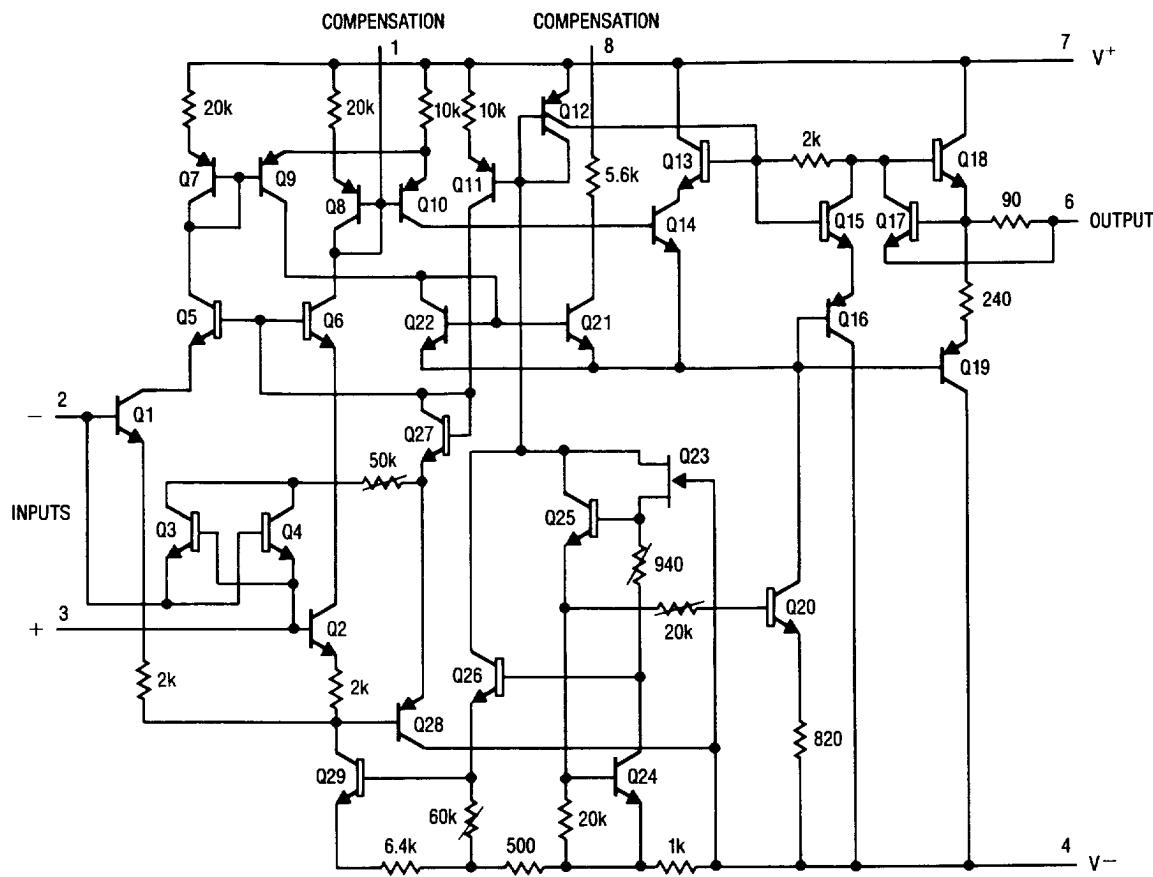


Offset Voltage Test Circuit†



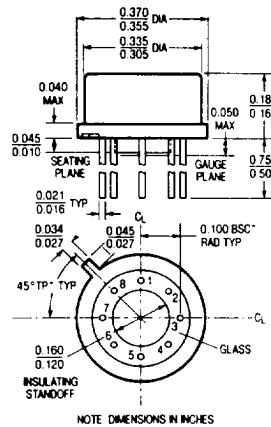
† THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION WITH SUPPLY VOLTAGES EQUAL TO $\pm 20V$, $R_1 = R_3 = 10k$, $R_2 = 200\Omega$, $A_v = 100$.

SCHEMATIC DIAGRAM



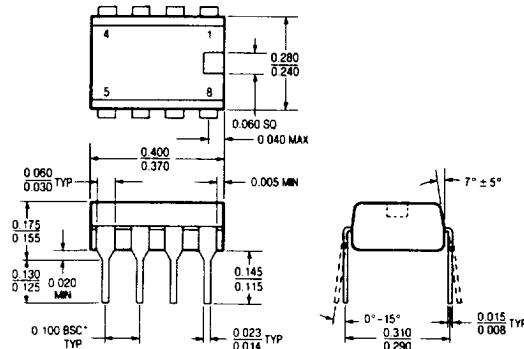
PACKAGE DESCRIPTION

H Package
Metal Can



T _j max	θ _{ja}	θ _{jc}
150°C	150°C/W	45°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

T _j max	θ _{ja}
100°C	130°C/W

LM111, LM211, LM311 Differential Comparators

1 Features

- Fast Response Time: 165 ns
- Strobe Capability
- Maximum Input Bias Current: 300 nA
- Maximum Input Offset Current: 70 nA
- Can Operate From Single 5-V Supply
- Available in Q-Temp Automotive
 - High-Reliability Automotive Applications
 - Configuration Control and Print Support
 - Qualification to Automotive Standards
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Desktop PCs
- Body Control Modules
- White Goods
- Building Automation
- Oscillators
- Peak Detectors

3 Description

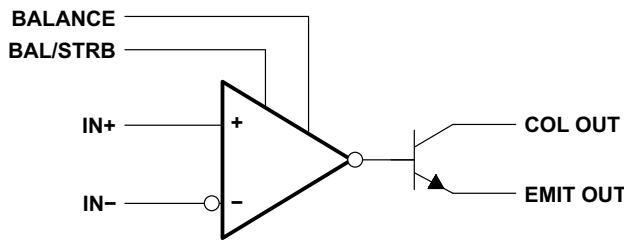
The LM111, LM211, and LM311 devices are single high-speed voltage comparators. These devices are designed to operate from a wide range of power-supply voltages, including $\pm 15\text{-V}$ supplies for operational amplifiers and 5-V supplies for logic systems. The output levels are compatible with most TTL and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 V at 50 mA. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, V_{CC+} or V_{CC-} . Offset balancing and strobe capabilities are available, and the outputs can be wire-OR connected. If the strobe is low, the output is in the off state, regardless of the differential input.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE
LM111FK	LCCC (20)	8.89 mm x 8.89 mm
LM111JG	CDIP (8)	9.60 mm x 6.67 mm
LM311PS	SO (8)	6.20 mm x 5.30 mm
LM211D	SOIC (8)	4.90 mm x 3.91 mm
LM311D		
LM211P	PDIP (8)	9.81 mm x 6.35 mm
LM311P		
LM211PW	TSSOP (8)	3.00 mm x 4.40 mm
LM311PW		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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Table of Contents

1 Features	1	
2 Applications	1	
3 Description	1	
4 Revision History.....	2	
5 Pin Configuration and Functions	3	
6 Specifications.....	4	
6.1 Absolute Maximum Ratings	4	
6.2 ESD Ratings.....	4	
6.3 Recommended Operating Conditions	4	
6.4 Thermal Information (8-Pin Packages)	5	
6.5 Thermal Information (20-Pin Package)	5	
6.6 Electrical Characteristics.....	6	
6.7 Switching Characteristics	6	
6.8 Typical Characteristics	7	
7 Parameter Measurement Information	9	
8 Detailed Description	10	
8.1 Overview	10	
8.2 Functional Block Diagram	10	
8.3 Feature Description.....	11	
8.4 Device Functional Modes.....	11	
9 Application and Implementation	12	
9.1 Application Information.....	12	
9.2 Typical Application	12	
9.3 System Examples	14	
10 Power Supply Recommendations	22	
11 Layout.....	22	
11.1 Layout Guidelines	22	
11.2 Layout Example	22	
12 Device and Documentation Support	23	
12.1 Related Links	23	
12.2 Receiving Notification of Documentation Updates	23	
12.3 Community Resources.....	23	
12.4 Trademarks	23	
12.5 Electrostatic Discharge Caution	23	
12.6 Glossary	23	
13 Mechanical, Packaging, and Orderable Information	23	

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

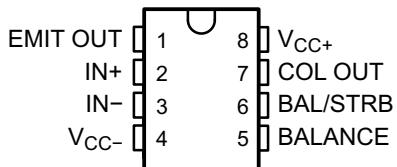
Changes from Revision J (January 2017) to Revision K	Page
• Changed Human body model (HBM) from: ± 1000 to: ± 500 in <i>ESD Ratings</i> table	4

Changes from Revision I (June 2015) to Revision J	Page
• Changed the data sheet title From: LMx11 Quad Differential Comparators To: LM111, LM211, LM311 Differential Comparators	1
• Updated the <i>Applications</i> list	1
• Updated the <i>Thermal Information (8-Pin Packages)</i> table	5
• Changed text From: "over a -25°C to $+85^{\circ}\text{C}$ temperature range..." To: ""over a -40°C to $+85^{\circ}\text{C}$ temperature range..." in the <i>Overview</i> section	10
• Added text "The LM311 has a temperature range of -40°C to $+125^{\circ}\text{C}$." to the <i>Overview</i> section.....	10

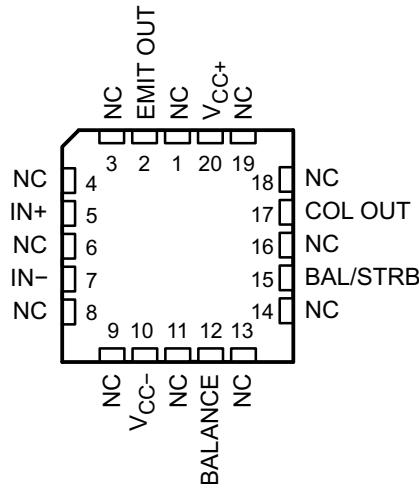
Changes from Revision H (August 2003) to Revision I	Page
• Updated <i>Features</i> with Military Disclaimer	1
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. No specification changes.	1

5 Pin Configuration and Functions

**LMx11 D, JG, P, PS, or PW Package
8-Pin SOIC, CDIP, PDIP, SO or TSSOP
Top View**



**LM111 FK Package
20-Pin LCCC⁽¹⁾
Top View**



(1) NC = No internal connection

Pin Functions

NAME	PIN				I/O ⁽¹⁾	DESCRIPTION
	LM211, LM311	LM311	LM111	LM111		
SOIC, PDIP, TSSOP	SO	CDIP	LCCC			
IN+	2	2	2	5	I	Noninverting comparator
IN-	3	3	3	7	I	Inverting input comparator
BALANCE	5	5	5	12	I	Balance
BAL/STRB	6	6	6	15	I	Strobe
COL OUT	7	7	7	17	O	Output collector comparator
EMIT OUT	1	1	1	2	O	Output emitter comparator
V _{CC-}	4	4	4	10	—	Negative supply
V _{CC+}	8	8	8	20	—	Positive supply
NC	—	—	—	1	—	No connect (No internal connection)
				3		
				4		
				6		
				8		
				9		
				11		
				13		
				14		
				16		
				18		
				19		

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Supply voltage	V_{CC+} ⁽²⁾		18		V
	V_{CC-} ⁽²⁾		-18		
	$V_{CC+} - V_{CC-}$		36		
V_{ID}	Differential input voltage ⁽³⁾		±30		V
V_I	Input voltage (either input) ⁽²⁾⁽⁴⁾		±15		V
	Voltage from emitter output to V_{CC-}		30		V
Voltage from collector output to V_{CC-}	LM111		50		V
	LM211		50		
	LM211Q		50		
	LM311		40		
	Duration of output short circuit to ground		10		s
T_J	Operating virtual-junction temperature		150		°C
	Case temperature for 60 s	FK package	260		°C
	Lead temperature 1,6 mm (1/16 inch) from case, 10 s	JG package	300		°C
	Lead temperature 1,6 mm (1/16 inch) from case, 60 s	D, P, PS, or PW package	260		°C
T_{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or ±15 V, whichever is less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage		3.5	30	V
V_I	Input voltage ($ V_{CC+} \leq 15$ V)		$V_{CC-} + 0.5$	$V_{CC+} - 1.5$	V
T_A	Operating free-air temperature range	LM111	-55	125	°C
		LM211	-40	85	
		LM211Q	-40	125	
		LM311	0	70	

6.4 Thermal Information (8-Pin Packages)

THERMAL METRIC ⁽¹⁾	LM211, LM311		LM311	LM111	UNIT		
	D (SOIC)	P (PDIP)	PW (TSSOP)	PS (SO)			
	8 PINS	8 PINS	8 PINS	8 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	114.3	57.5	162	—	°C/W	
R _{θJC(top)}	Junction-to-case (top) thermal resistance	60.7	47.3	44.6	81.6	14.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	54.5	34.6	93	66.5	—	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	17.4	24.9	2.6	31.4	—	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	54	34.5	90.8	65.8	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information (20-Pin Package)

THERMAL METRIC ⁽¹⁾	LM111	UNIT	
	FK (LCCC)		
	20 PINS		
R _{θJC(top)}	Junction-to-case (top) thermal resistance	5.61	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	LM111 LM211 LM211Q			LM311			UNIT
			MIN	TYP ⁽²⁾	MAX	MIN	TYP ⁽²⁾	MAX	
V_{IO} Input offset voltage	See ⁽³⁾	25°C	0.7	3		2	7.5		mV
		Full range		4			10		
I_{IO} Input offset current	See ⁽³⁾	25°C	4	10		6	50		nA
		Full range		20			70		
I_{IB} Input bias current	1 V $\leq V_O \leq 14$ V	25°C	75	100		100	250		nA
		Full range		150			300		
$I_{IL(S)}$ Low-level strobe current ⁽⁴⁾	$V_{(strobe)} = 0.3$ V, $V_{ID} \leq -10$ mV	25°C		-3			-3		mA
V_{ICR} Common-mode input-voltage range ⁽³⁾	Lower range	Full range		-14.7	-14.5		-14.7	-14.5	V
	Upper range		13	13.8		13	13.8		
A_{VD} Large-signal differential-voltage amplification	5 V $\leq V_O \leq 35$ V, $R_L = 1$ k Ω	25°C	40	200		40	200		V/mV
I_{OH} High-level (collector) output leakage current	$I_{(strobe)} = -3$ mA, $V_{ID} = 5$ mV	25°C	0.2	10					nA
		Full range		0.5					μ A
	$V_{ID} = 5$ mV, $V_{OH} = 35$ V	25°C				0.2	50		nA
V_{OL} Low-level (collector-to- emitter) output voltage	$I_{OL} = 50$ mA	$V_{ID} = -5$ mV	25°C	0.75	1.5				V
		$V_{ID} = -10$ mV	25°C				0.75	1.5	
	$V_{CC+} = 4.5$ V, $V_{CC-} = 0$ V, $I_{OL} = 8$ mA	$V_{ID} = -6$ mV	Full range	0.23	0.4				
		$V_{ID} = -10$ mV	Full range				0.23	0.4	
I_{CC+} Supply current from V_{CC+} output low	$V_{ID} = -10$ mV,	No load	25°C	5.1	6		5.1	7.5	mA
I_{CC-} Supply current from V_{CC-} output high	$V_{ID} = 10$ mV,	No load	25°C	-4.1	-5		-4.1	-5	mA

(1) Unless otherwise noted, all characteristics are measured with BALANCE and BAL/STRB open and EMIT OUT grounded. Full range for LM111 is -55°C to 125°C, for LM211 is -40°C to 85°C, for LM211Q is -40°C to 125°C, and for LM311 is 0°C to 70°C.

(2) All typical values are at $T_A = 25^\circ\text{C}$.

(3) The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pullup resistor of 7.5 k Ω to V_{CC+} . These parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

(4) The strobe must not be shorted to ground; it must be current driven at -3 mA to -5 mA (see Figure 18 and Figure 31).

6.7 Switching Characteristics

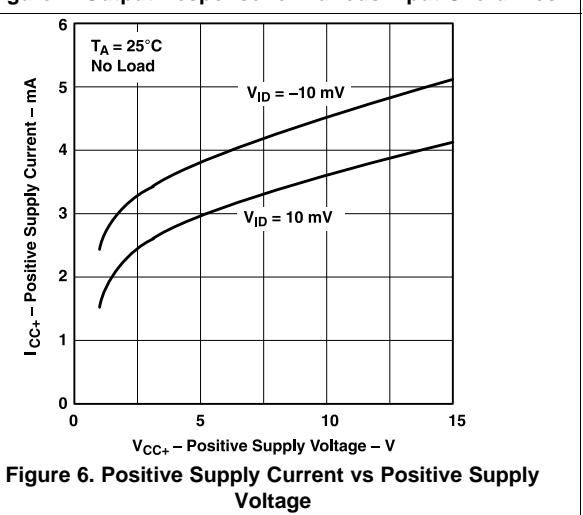
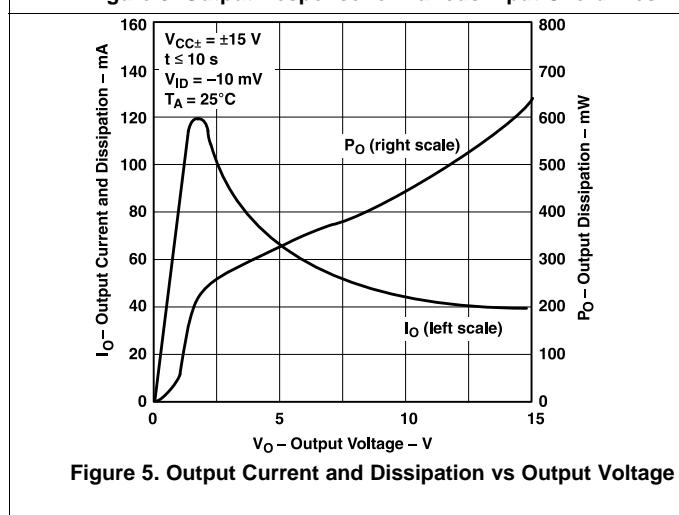
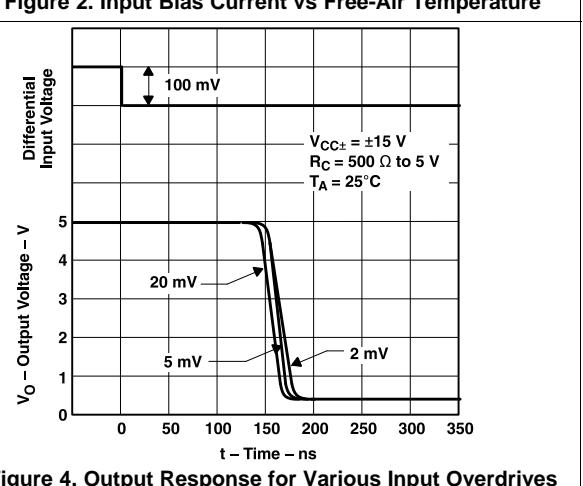
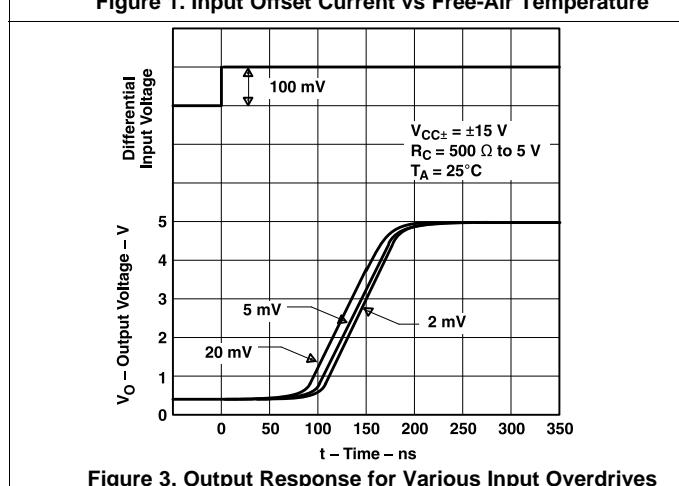
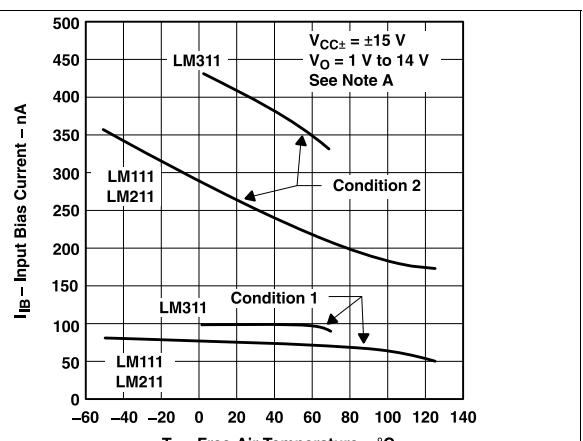
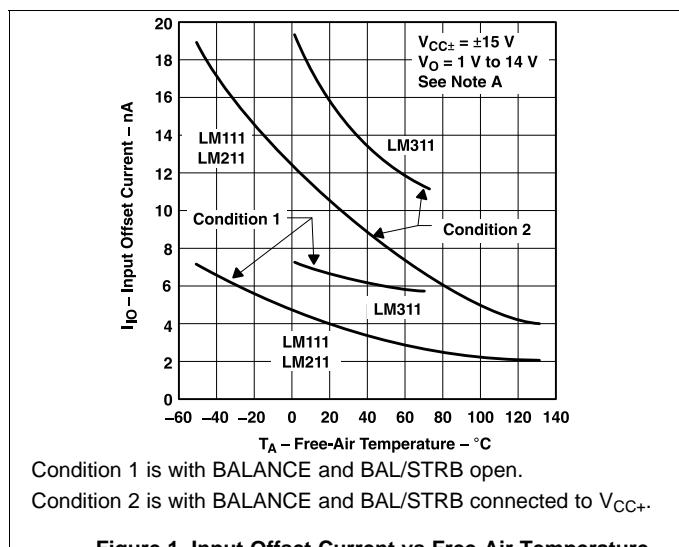
$V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LM111 LM211 LM211Q LM311		UNIT
		TYP		
Response time, low-to-high-level outputSee ⁽¹⁾	$R_C = 500$ Ω to 5 V, $C_L = 5$ pF, see ⁽²⁾	115		ns
Response time, high-to-low-level outputSee ⁽¹⁾		165		ns

(1) The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

(2) The package thermal impedance is calculated in accordance with MIL-STD-883.

6.8 Typical Characteristics



Typical Characteristics (continued)

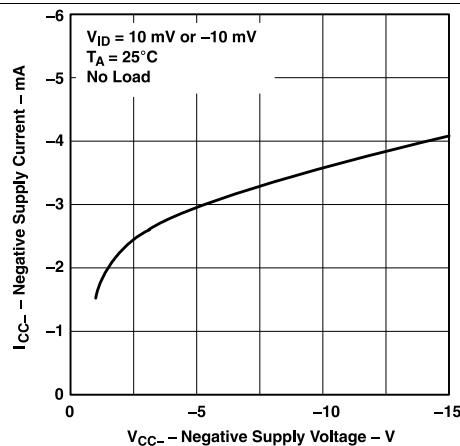


Figure 7. Negative Supply Current vs Negative Supply Voltage

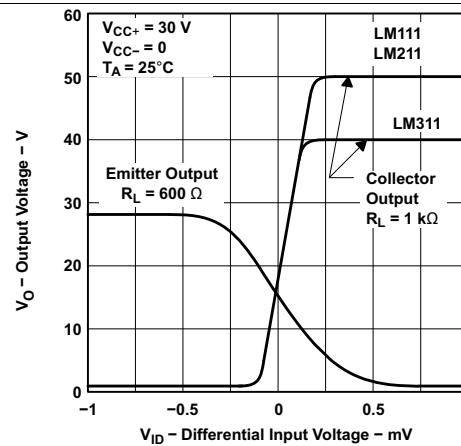
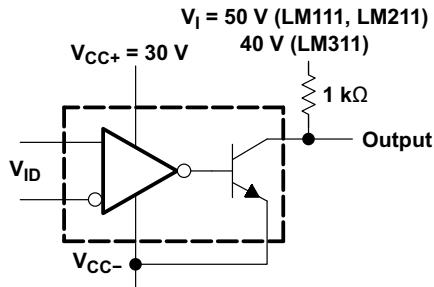


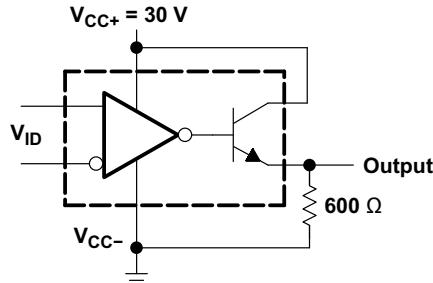
Figure 8. Voltage Transfer Characteristics and Test Circuits

7 Parameter Measurement Information



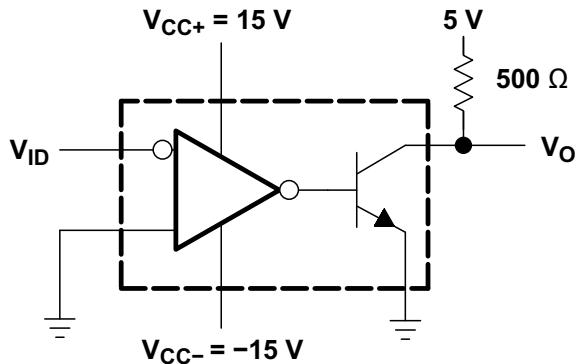
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Figure 9. Collector Output Transfer Characteristic Test Circuit



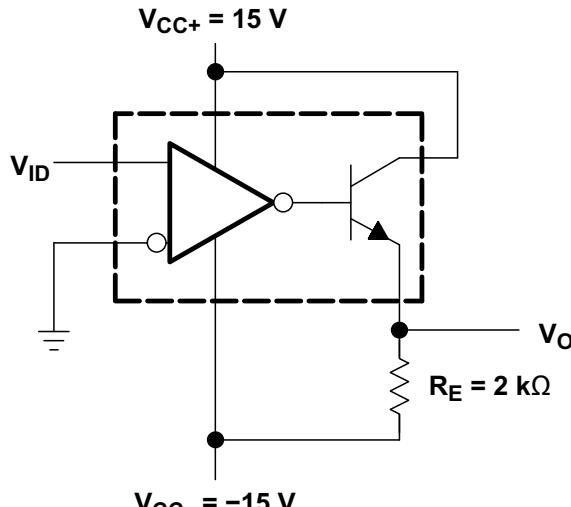
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Figure 10. Emitter Output Transfer Characteristic Test Circuit



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Figure 11. Test Circuit for Figure 3 and Figure 4



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Figure 12. Test Circuit for Figure 14 and Figure 15

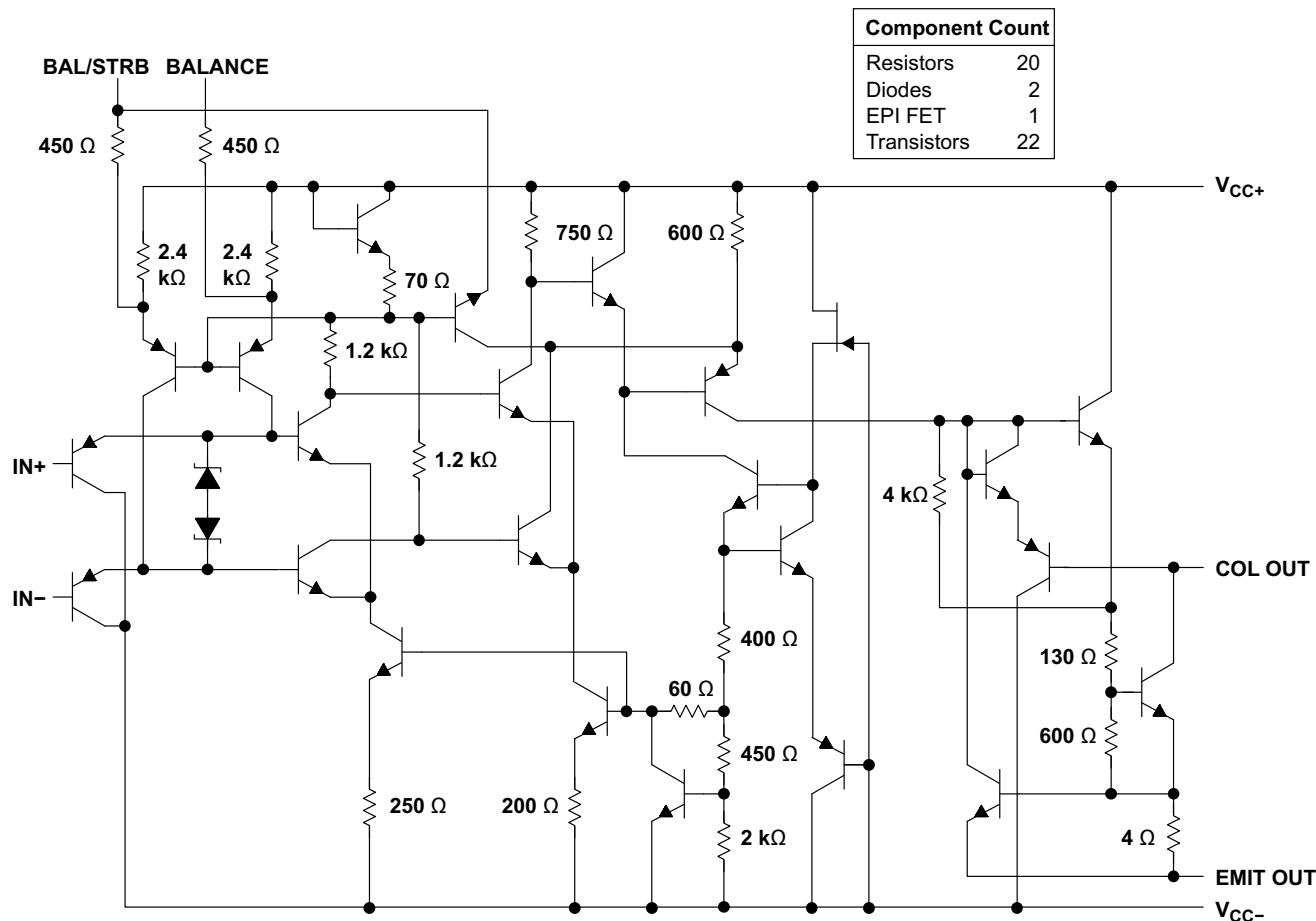
8 Detailed Description

8.1 Overview

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than legacy standard devices. They are also designed to operate over a wider range of supply voltages: from standard $\pm 15\text{V}$ op amp supplies down to the single 5-V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50 V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire ORed. The LM211 is identical to the LM111, except that its performance is specified over a -40°C to $+85^\circ\text{C}$ temperature range instead of -55°C to $+125^\circ\text{C}$. The LM311 has a temperature range of 0°C to $+70^\circ\text{C}$. The LM211Q has a temperature range of -40°C to $+125^\circ\text{C}$.

8.2 Functional Block Diagram



8.3 Feature Description

LMx11 consists of a PNP input stage to sense voltages near V_{CC-} . It also contains balance and strobe pins for external offset adjustment or trimming.

The input stage is followed by a very high gain stage for very fast response after a voltage difference on the input pins have been sensed.

This is then followed by the output stage that consists of an open collector NPN (pulldown or low-side) transistor. Unlike most open drain comparators, this NPN output stage has an isolated emitter from V_{CC-} , allowing this device to set the V_{OL} output value for collector output.

8.4 Device Functional Modes

8.4.1 Voltage Comparison

The LMx11 operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

9 Application and Implementation

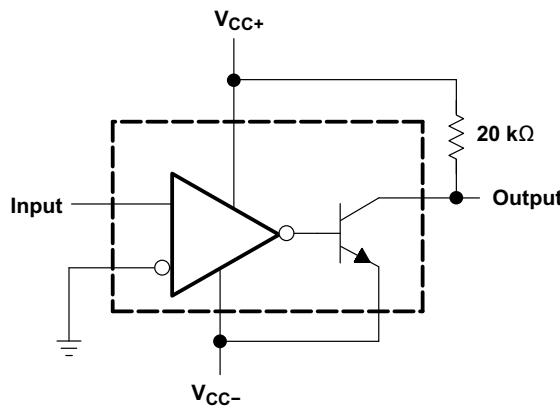
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

9.1 Application Information

A typical LMX11 application compares a single signal to a reference or two signals against each other. Many users take advantage of the open-drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LMX11 optimal for level shifting to a higher or lower voltage.

9.2 Typical Application



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Figure 13. Zero-Crossing Detector

9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	-15	13	V
V_{CC+}	Positive supply voltage		15	V
V_{CC-}	Negative supply voltage	-15		
I_{OUT}	Output current		20	mA

9.2.2 Detailed Design Procedure

When using LMX11 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

9.2.2.1 Input Voltage Range

When choosing the input voltage range, consider the input common mode voltage range (V_{ICR}). Operation outside of this range can yield incorrect comparisons.

The following list describes the outcomes of some input voltage situations.

- When both IN– and IN+ are both within the common-mode range:
 - If IN– is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - If IN– is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
- When IN– is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
- When IN+ is higher than common mode and IN– is within common mode, the output is high impedance and the output transistor is not conducting
- When IN– and IN+ are both higher than common mode, the output is undefined

9.2.2.2 Minimum Overdrive Voltage

Overdrive voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the Overdrive voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. [Figure 14](#) and [Figure 15](#) show positive and negative response times with respect to overdrive voltage.

9.2.2.3 Output and Drive Current

Output current is determined by the pullup resistance and pullup voltage. The output current produces a output low voltage (V_{OL}) from the comparator, in which V_{OL} is proportional to the output current. Use [Figure 5](#) to determine V_{OL} based on the output current.

The output current can also effect the transient response.

9.2.2.4 Response Time

The load capacitance (C_L), pullup resistance (R_{PULLUP}), and equivalent collector-emitter resistance (R_{CE}) levels determine the transient response. [Equation 1](#) approximates the positive response time. [Equation 2](#) approximates the negative response time. R_{CE} can be determine by taking the slope of [Figure 5](#) in the linear region at the desired temperature, or by [Equation 3](#).

$$\tau_P \approx R_{PULLUP} \times C_L \quad (1)$$

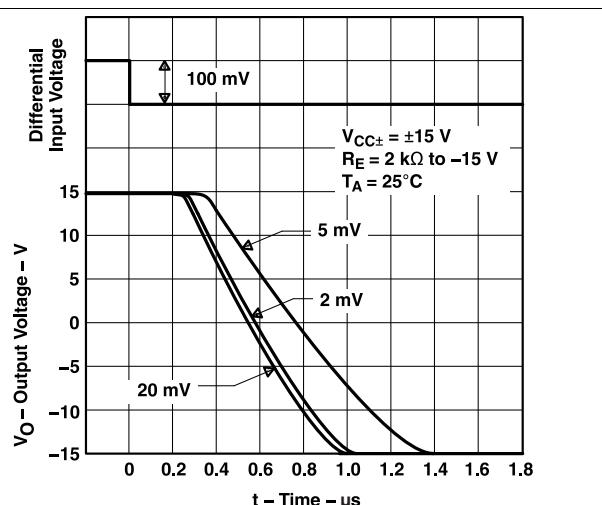
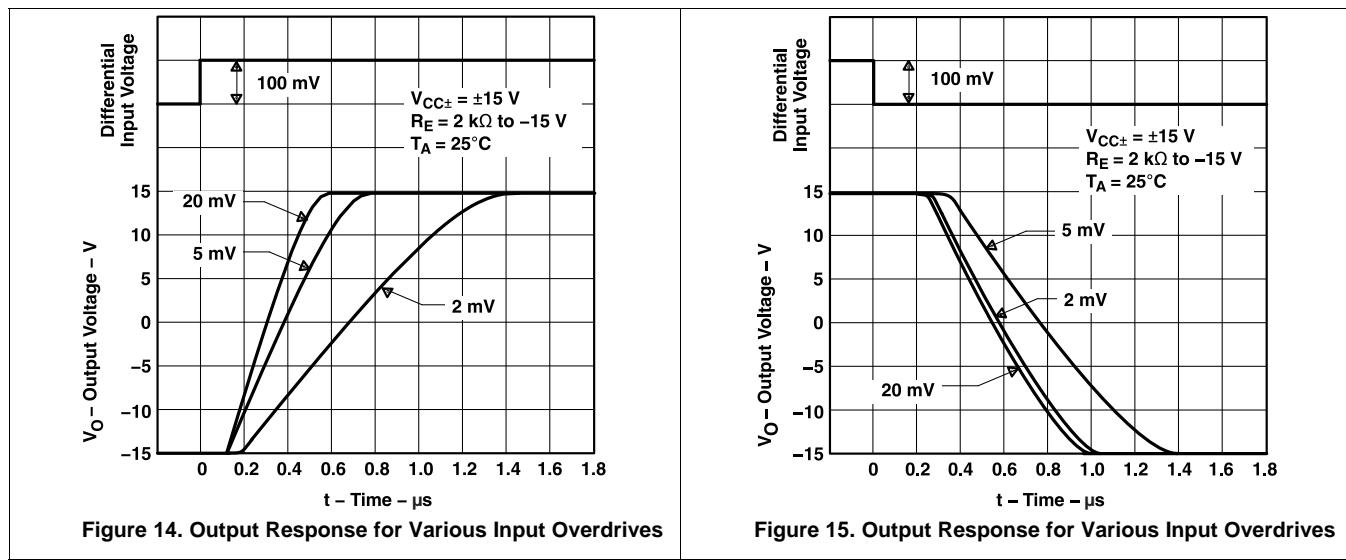
$$\tau_N \approx R_{CE} \times C_L \quad (2)$$

$$R_{CE} = \frac{V_{OL}}{I_{OUT}}$$

where

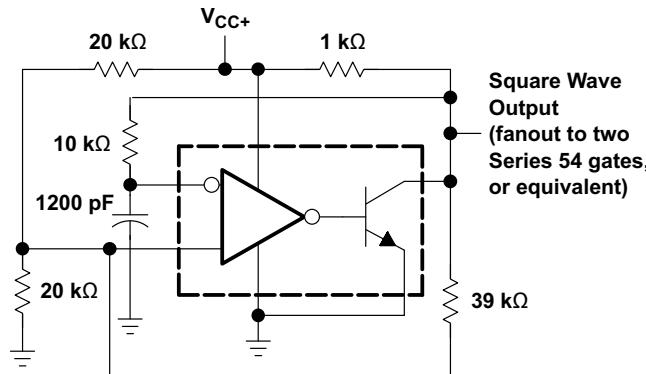
- V_{OL} is the low-level output voltage
 - I_{OUT} is the output current
- (3)

9.2.3 Application Curves



9.3 System Examples

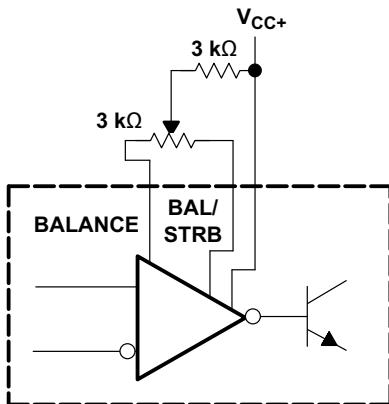
Figure 16 through Figure 33 show various applications for the LM111, LM211, and LM311 comparators.



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Figure 16. 100-kHz Free-Running Multivibrator

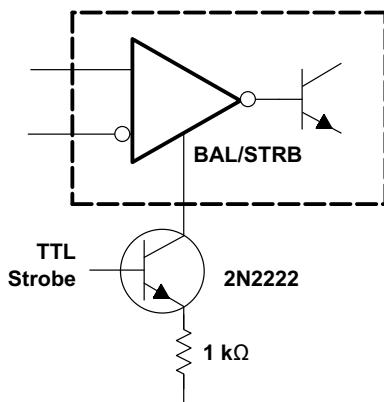
System Examples (continued)



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If offset balancing is not used, the BALANCE and BAL/STRB pins must be unconnected. It is also acceptable to short pins together.

Figure 17. Offset Balancing

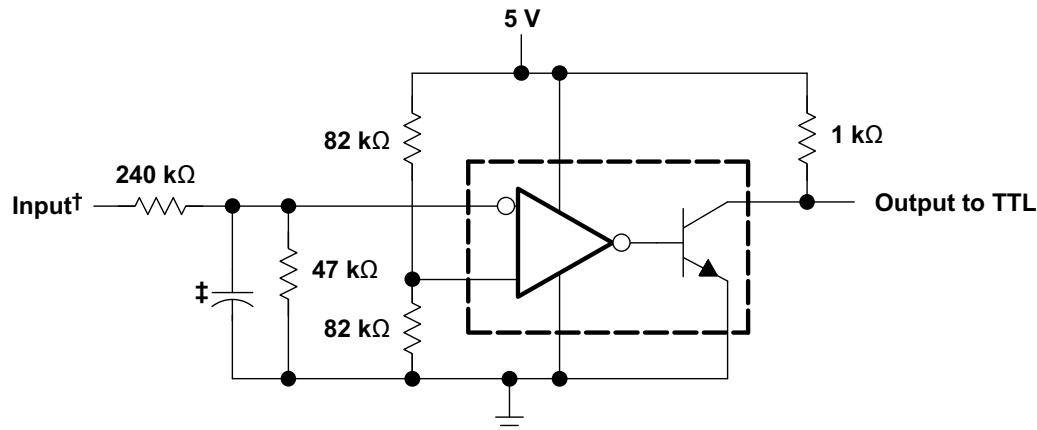


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Do not connect strobe pin directly to ground, because the output is turned off whenever current is pulled from the strobe pin.

Figure 18. Strobing

System Examples (continued)

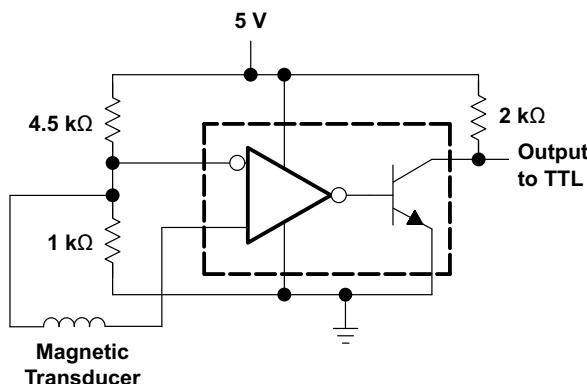


[†] Resistor values shown are for a 0- to 30-V logic swing and a 15-V threshold.

[‡] May be added to control speed and reduce susceptibility to noise spikes

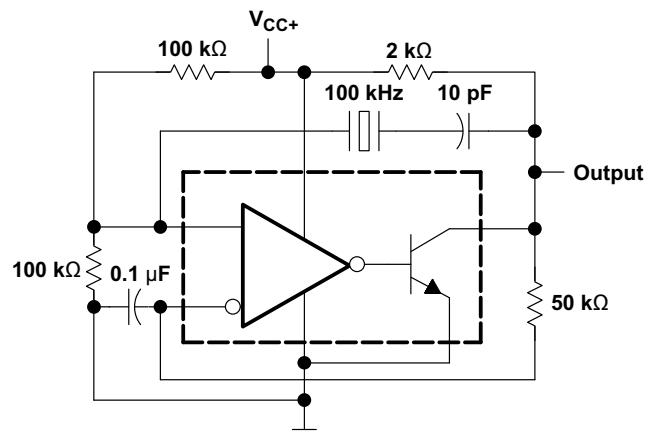
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Figure 19. TTL Interface With High-Level Logic



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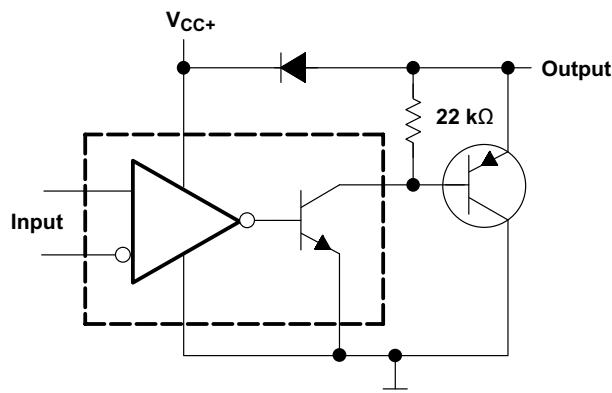
Figure 20. Detector for Magnetic Transducer



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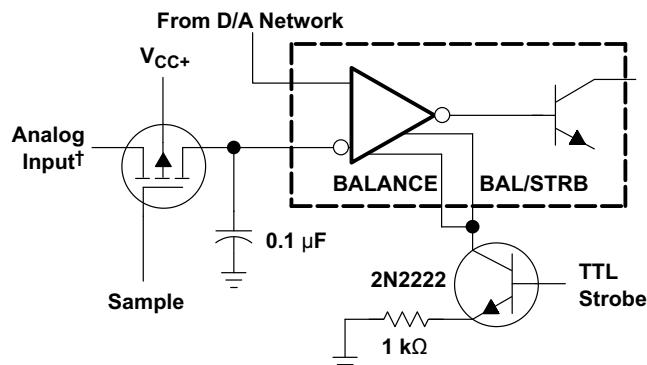
Figure 21. 100-kHz Crystal Oscillator

System Examples (continued)



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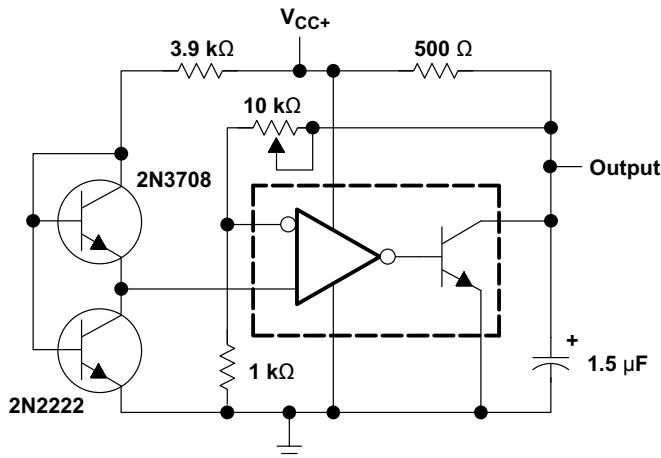
Figure 22. Comparator and Solenoid Driver



† Typical input current is 50 pA with inputs strobed off.

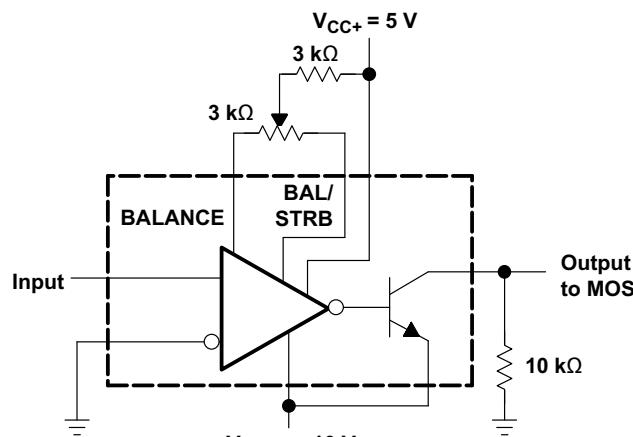
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Figure 23. Strobing Both Input and Output Stages Simultaneously



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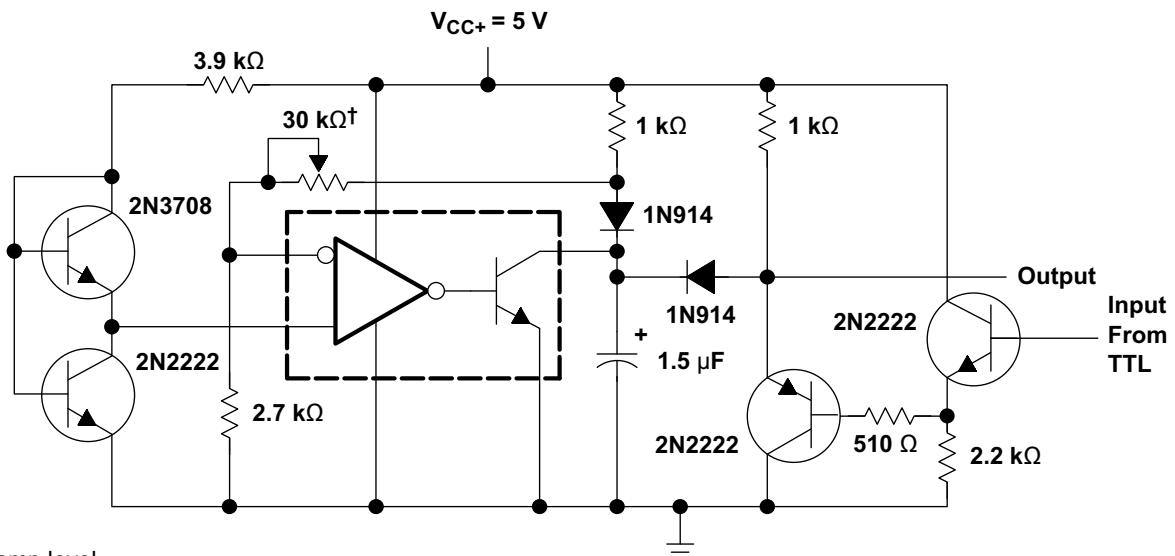
Figure 24. Low-Voltage Adjustable Reference Supply



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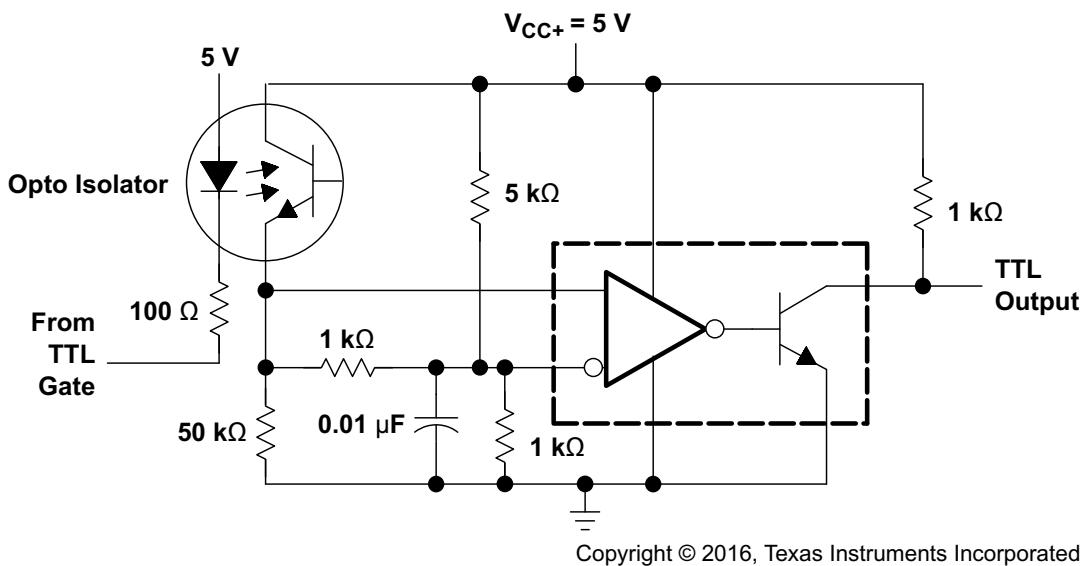
Figure 25. Zero-Crossing Detector Driving MOS Logic

System Examples (continued)



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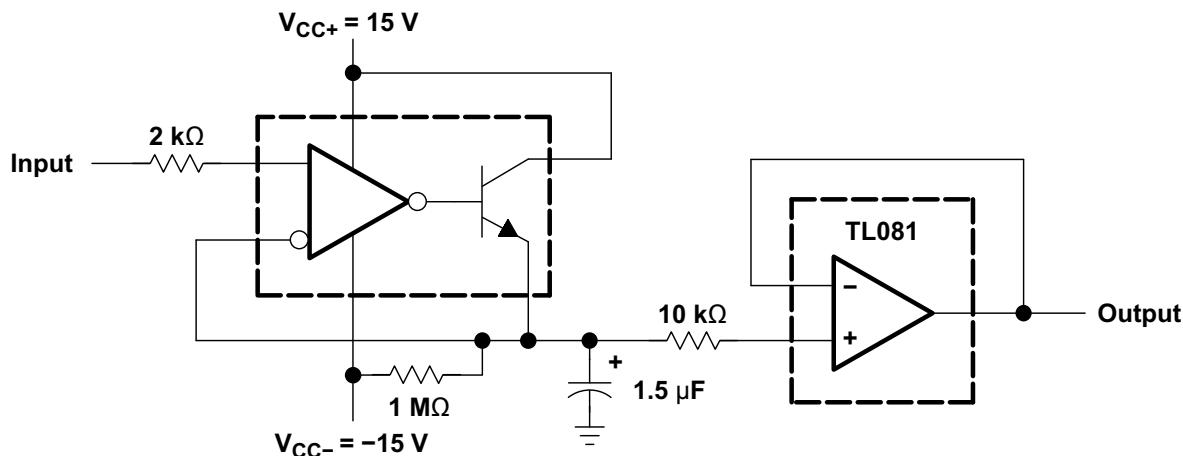
Figure 26. Precision Squarer



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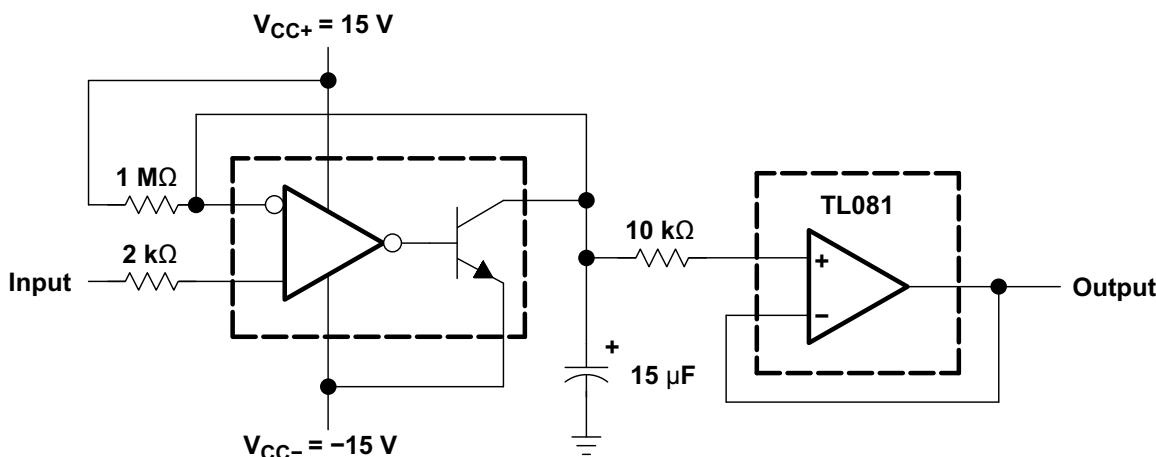
Figure 27. Digital Transmission Isolator

System Examples (continued)



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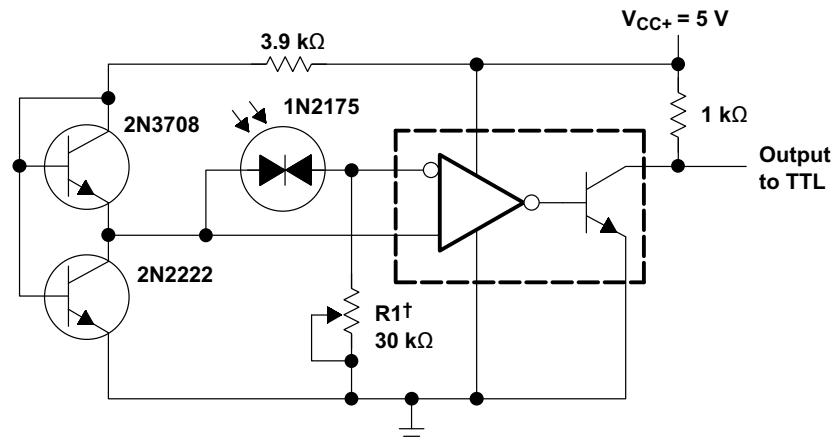
Figure 28. Positive-Peak Detector



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Figure 29. Negative-Peak Detector

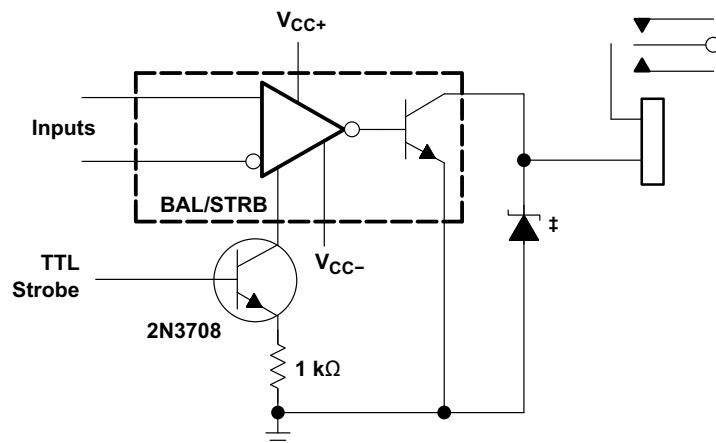
System Examples (continued)



† R1 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing dark current by an order of magnitude.

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Figure 30. Precision Photodiode Comparator

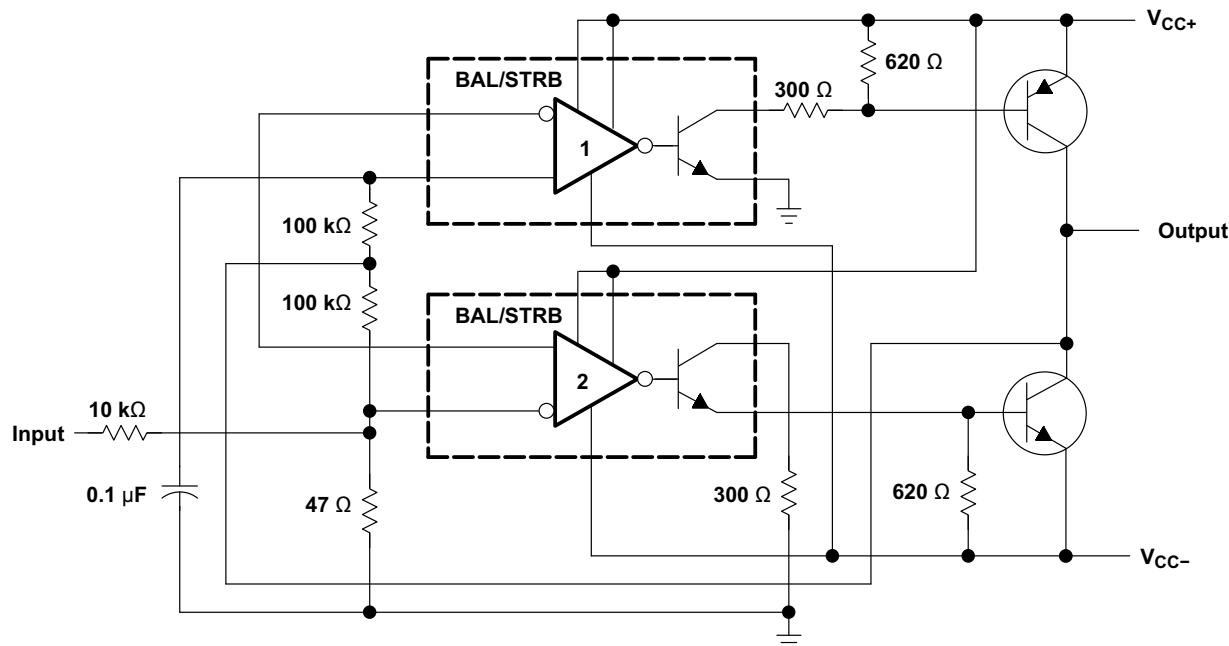


‡ Transient voltage and inductive kickback protection

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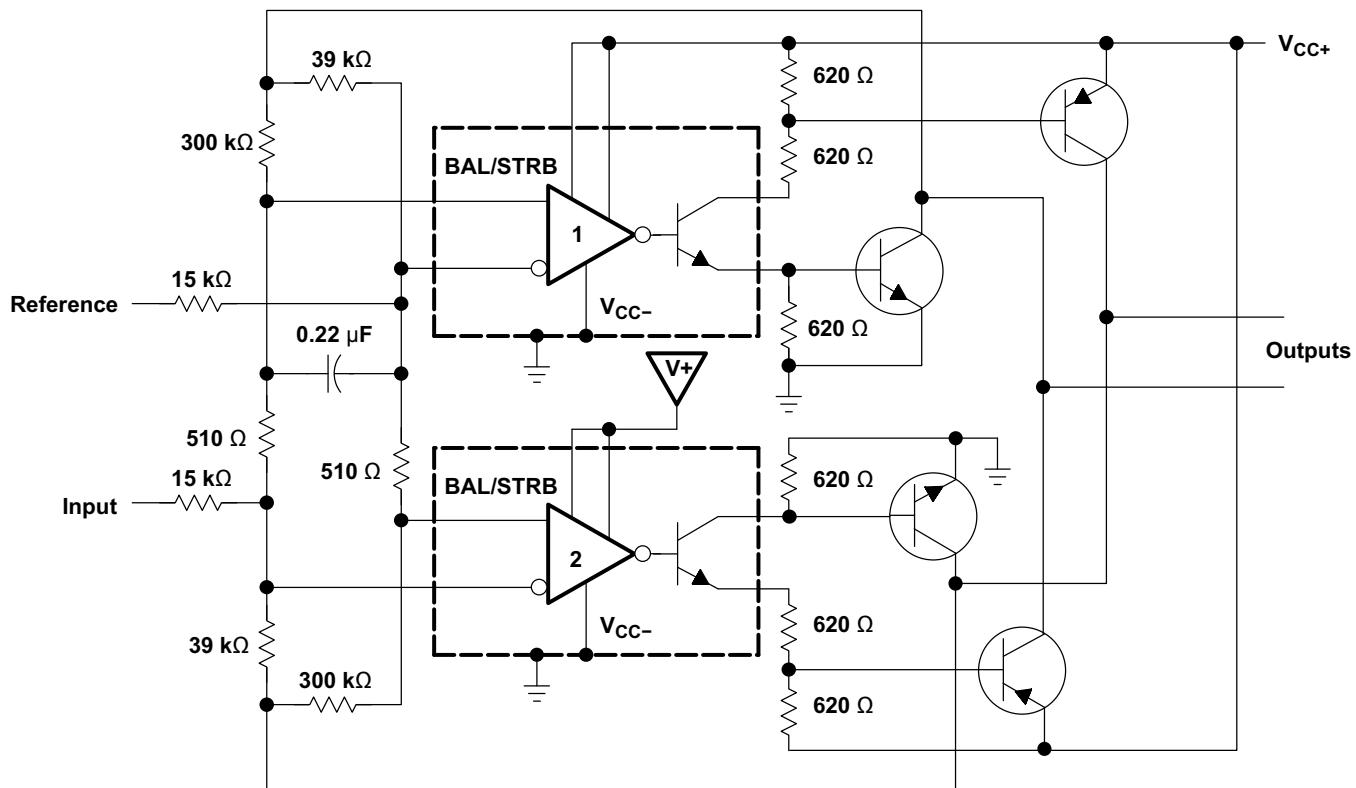
Figure 31. Relay Driver With Strobe

System Examples (continued)



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Figure 32. Switching Power Amplifier



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Figure 33. Switching Power Amplifiers

10 Power Supply Recommendations

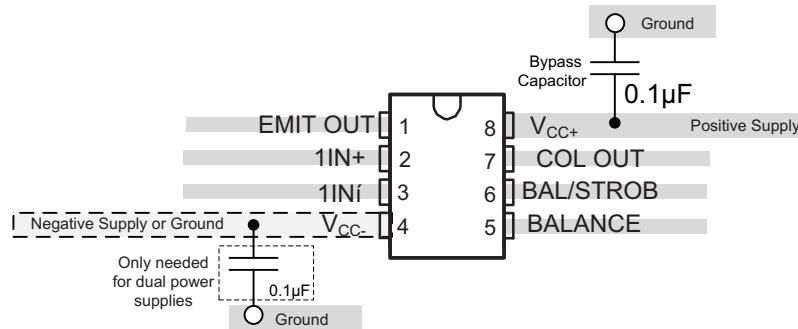
For fast response and comparison applications with noisy or AC inputs, use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can affect the common-mode range of the comparator input and create an inaccurate comparison.

11 Layout

11.1 Layout Guidelines

To create an accurate comparator application without hysteresis, maintain a stable power supply with minimized noise and glitches, which can affect the high level input common-mode voltage range. To achieve this accuracy, add a bypass capacitor between the supply voltage and ground. Place a bypass capacitor on the positive power supply and negative supply (if available).

11.2 Layout Example



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Figure 34. LMx11 Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM111	Click here				
LM211	Click here				
LM311	Click here				

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community **TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support **TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

 These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — **TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.



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PACKAGE OPTION ADDENDUM

9-Mar-2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/10304BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /10304BPA	Samples
LM111FKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM111FKB	Samples
LM111JG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM111JG	Samples
LM111JGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM111JGB	Samples
LM211D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM211	Samples
LM211DE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM211	Samples
LM211DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM211	Samples
LM211DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM211	Samples
LM211DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM211	Samples
LM211P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	LM211P	Samples
LM211PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	LM211P	Samples
LM211PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L211	Samples
LM211PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L211	Samples
LM211PWRE4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L211	Samples
LM211QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	Samples
LM211QDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	Samples
LM211QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	Samples
LM211QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	Samples
LM311D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	Samples



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PACKAGE OPTION ADDENDUM

9-Mar-2021

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM311DE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	Samples
LM311DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	Samples
LM311DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM311	Samples
LM311DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	Samples
LM311DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	Samples
LM311P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM311P	Samples
LM311PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM311P	Samples
LM311PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
LM311PSRE4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
LM311PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
LM311PWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
LM311PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
LM311PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
M38510/10304BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /10304BPA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.



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PACKAGE OPTION ADDENDUM

9-Mar-2021

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM211 :

• Automotive: [LM211-Q1](#)

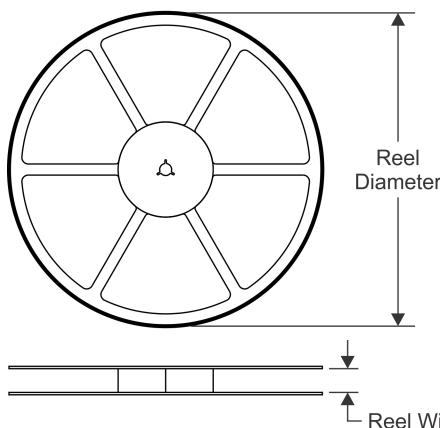
• Enhanced Product: [LM211-EP](#)

NOTE: Qualified Version Definitions:

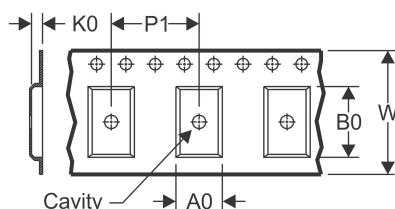
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

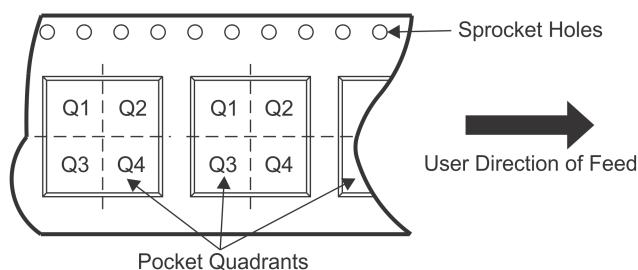


TAPE DIMENSIONS



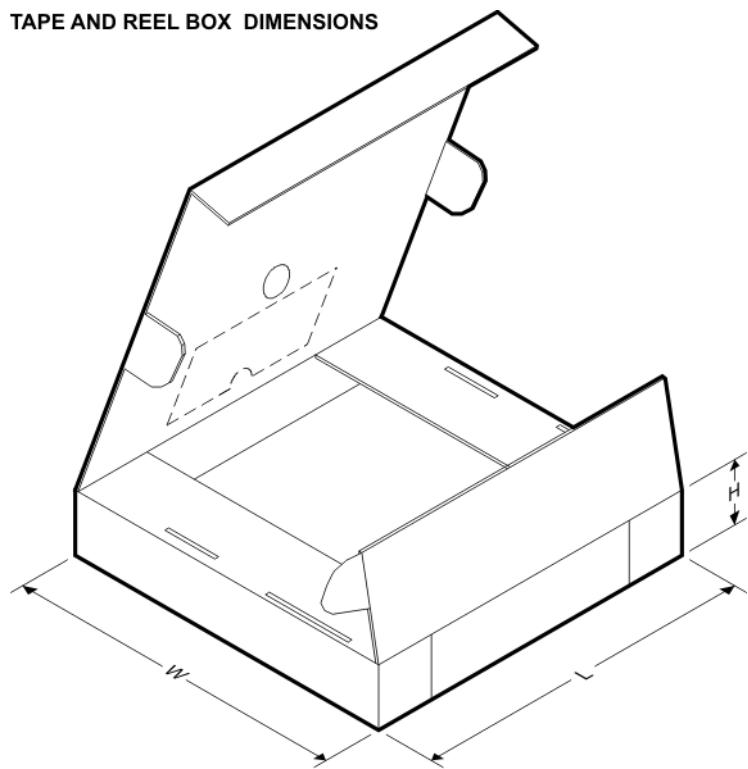
A_0	Dimension designed to accommodate the component width
B_0	Dimension designed to accommodate the component length
K_0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P_1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A_0 (mm)	B_0 (mm)	K_0 (mm)	P_1 (mm)	W (mm)	Pin1 Quadrant
LM211DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM211DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM211DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM211DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM211PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM211QDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM311DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM311DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM311DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM311DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM311DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM311PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


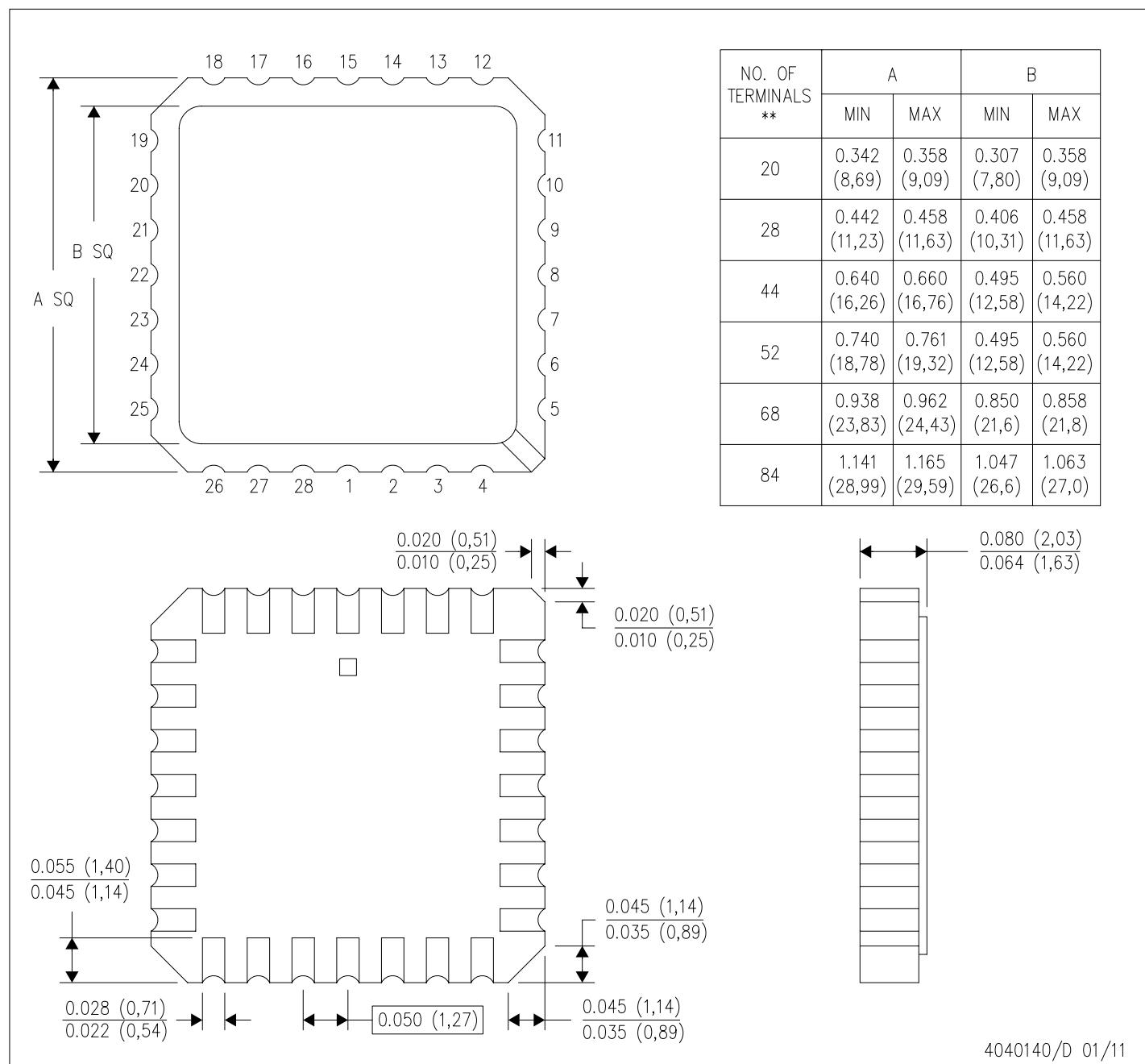
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM211DR	SOIC	D	8	2500	340.5	338.1	20.6
LM211DR	SOIC	D	8	2500	853.0	449.0	35.0
LM211DRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM211DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM211PWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM211QDR	SOIC	D	8	2500	340.5	338.1	20.6
LM311DR	SOIC	D	8	2500	364.0	364.0	27.0
LM311DR	SOIC	D	8	2500	340.5	338.1	20.6
LM311DR	SOIC	D	8	2500	853.0	449.0	35.0
LM311DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM311DRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM311PWR	TSSOP	PW	8	2000	853.0	449.0	35.0

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

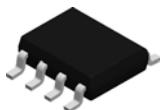
C. This package can be hermetically sealed with a metal lid.

D. Falls within JEDEC MS-004

4040140/D 01/11

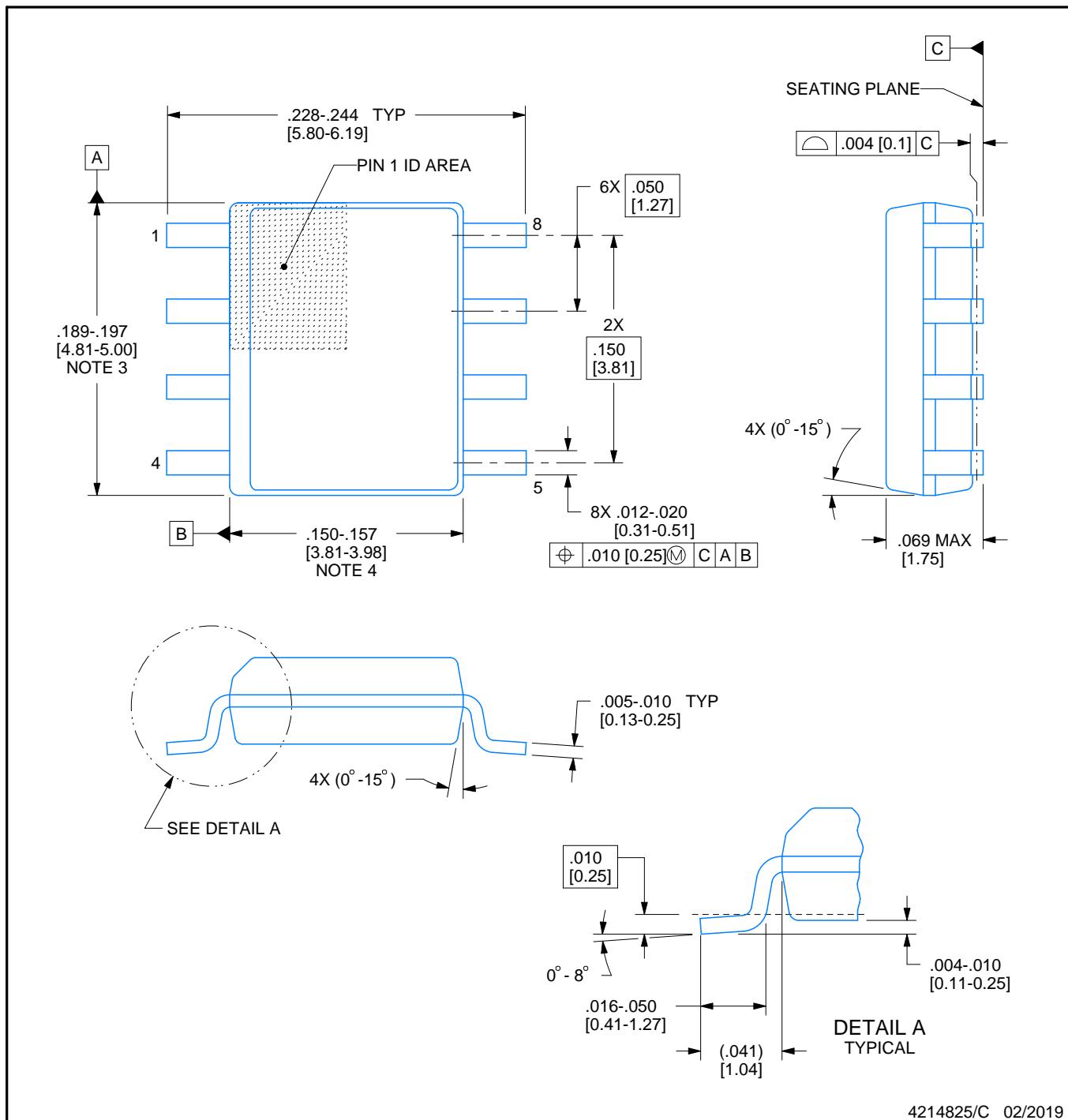
D0008A

PACKAGE OUTLINE



SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

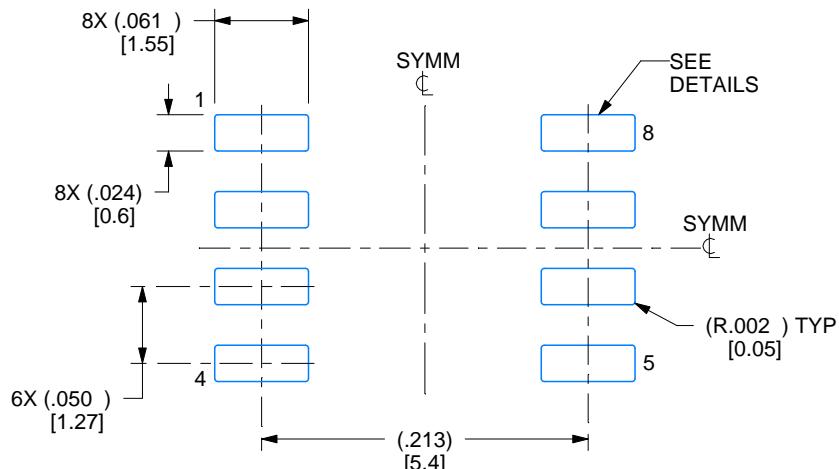
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

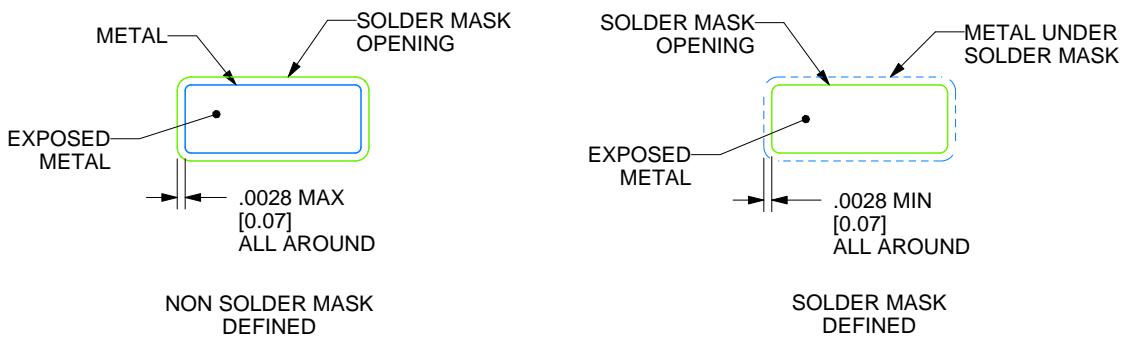
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

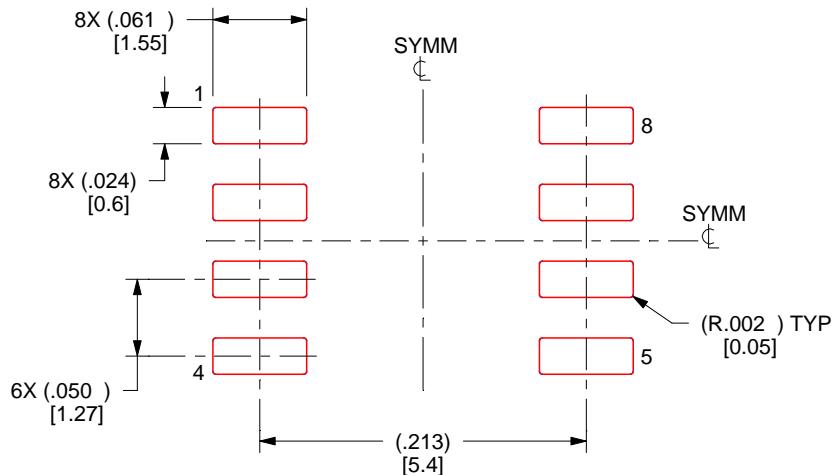
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

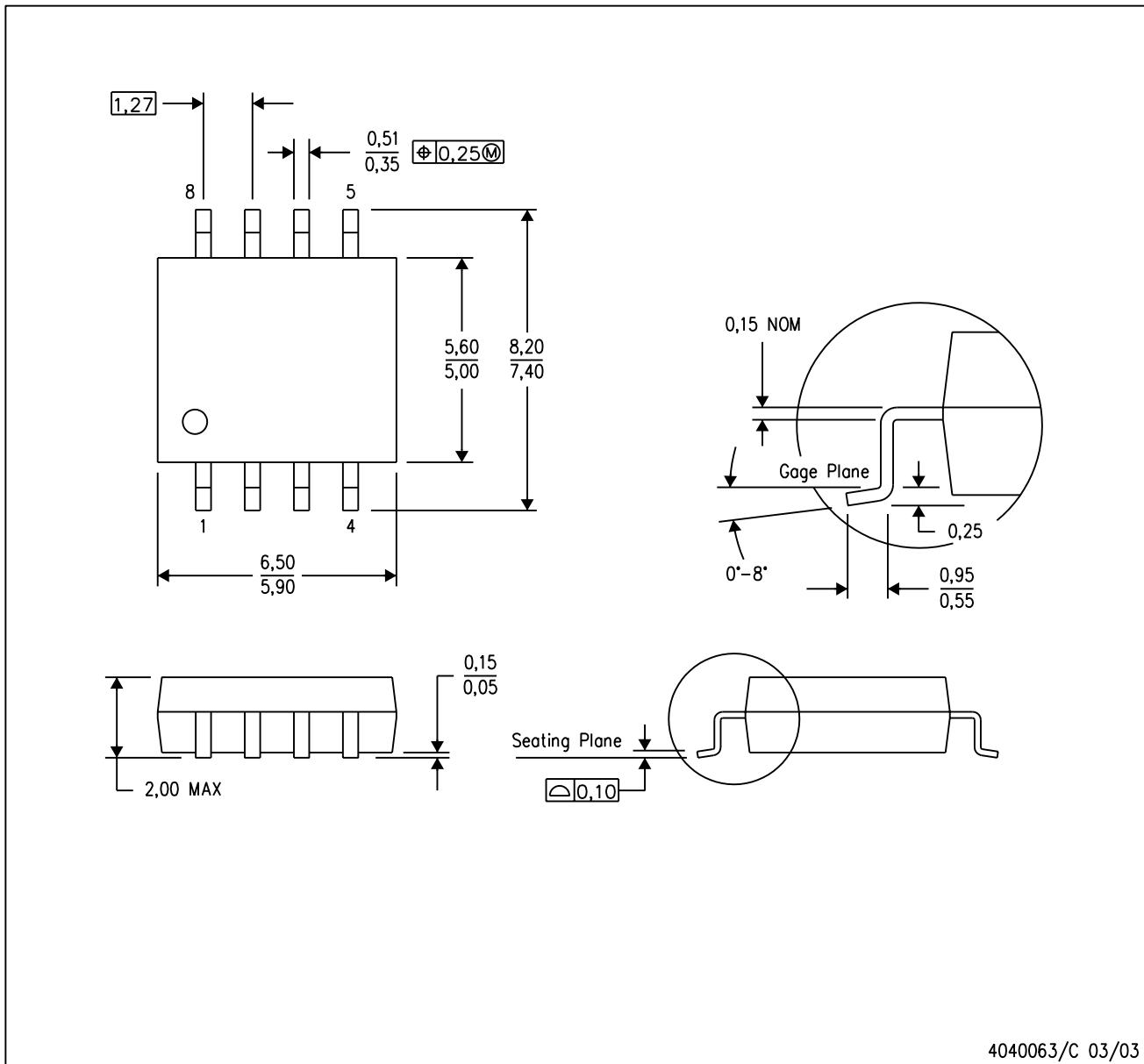
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

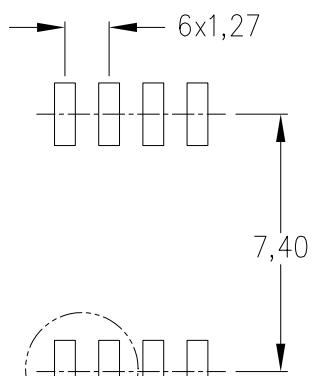
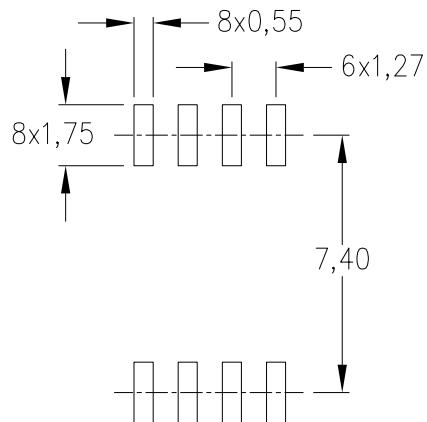
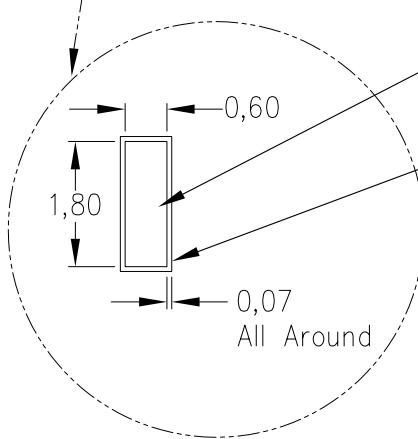


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE

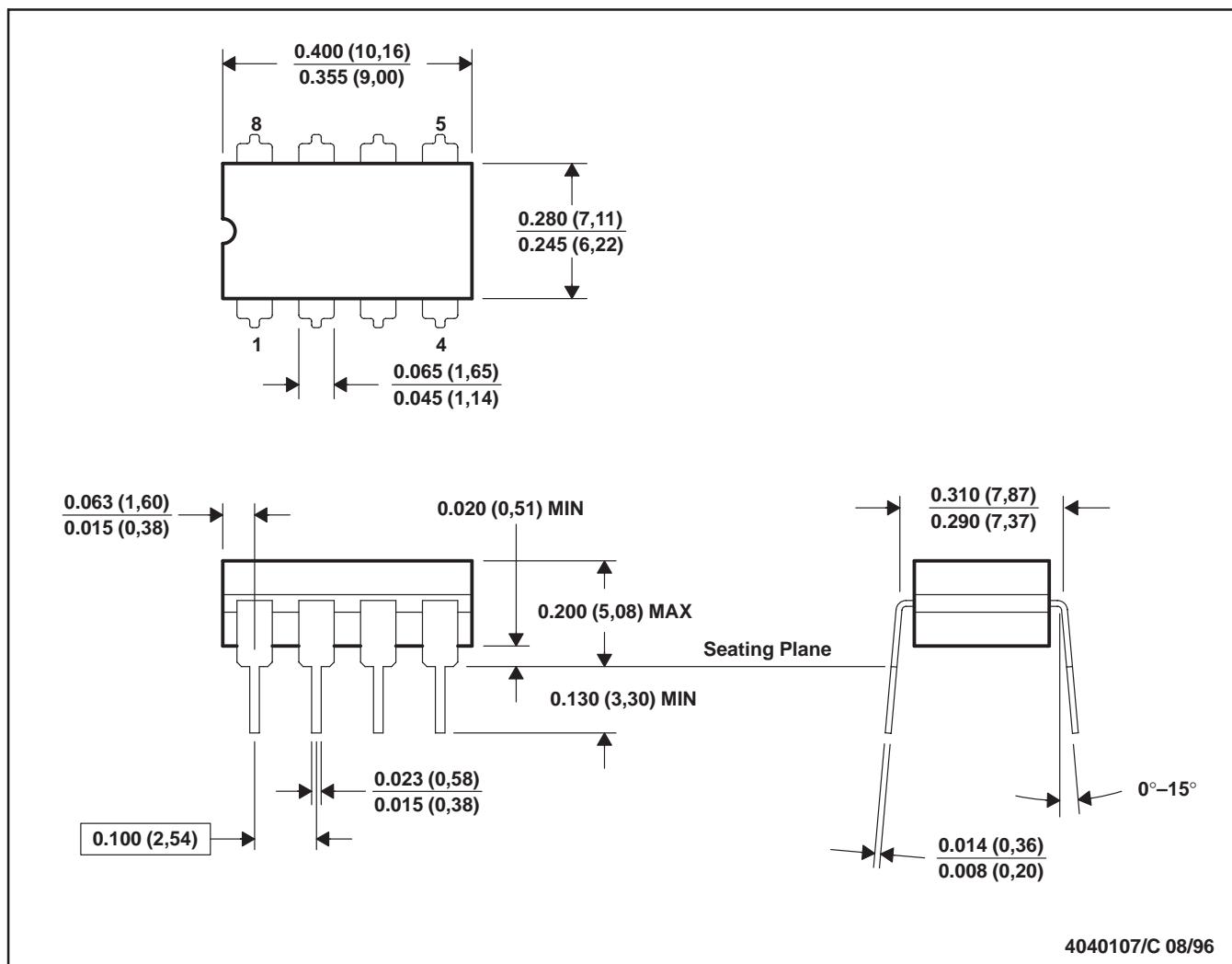
Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Non-Solder Mask Opening
(See Note E)

4212188/A 09/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

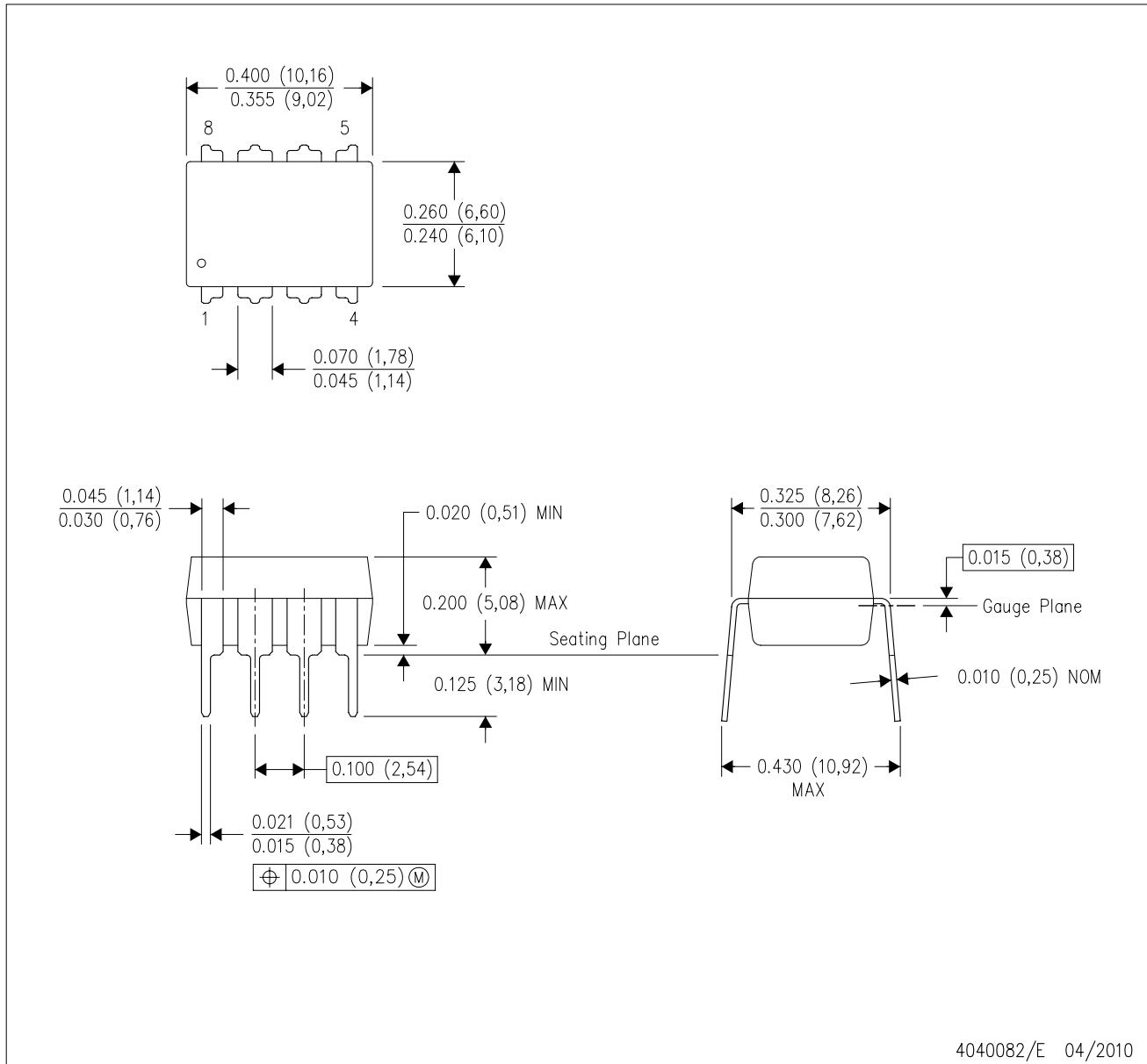


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

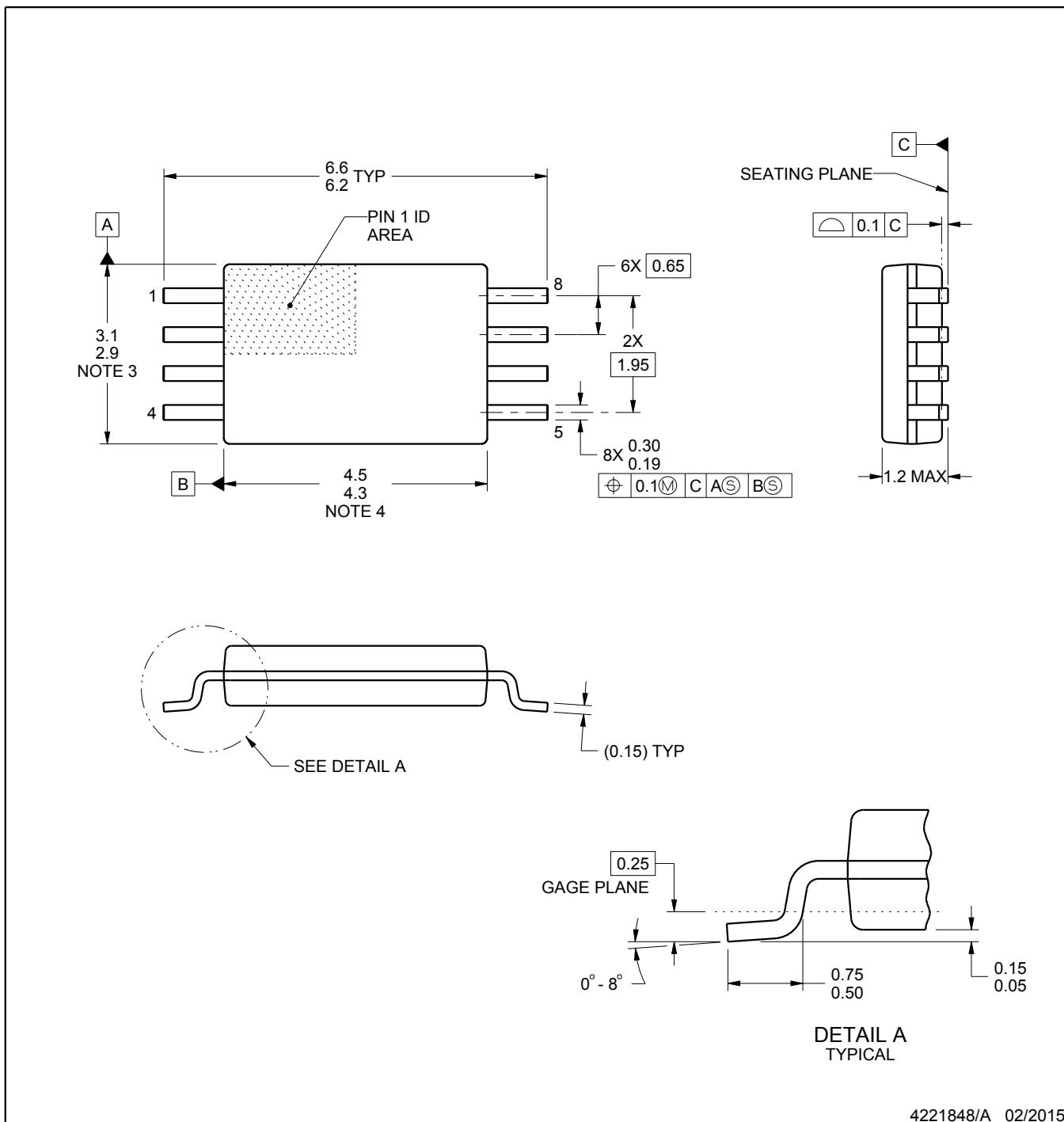
PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

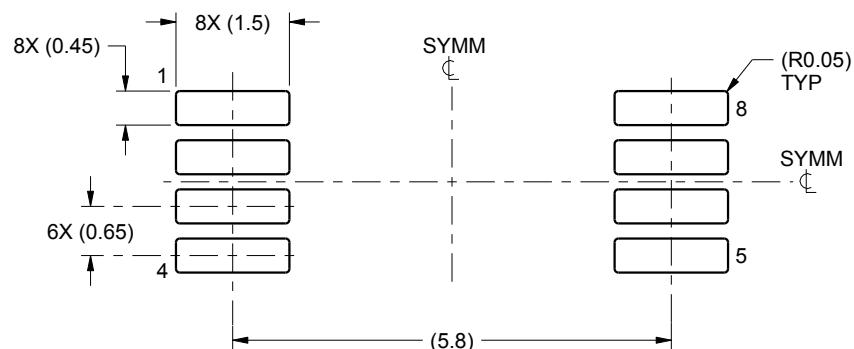
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

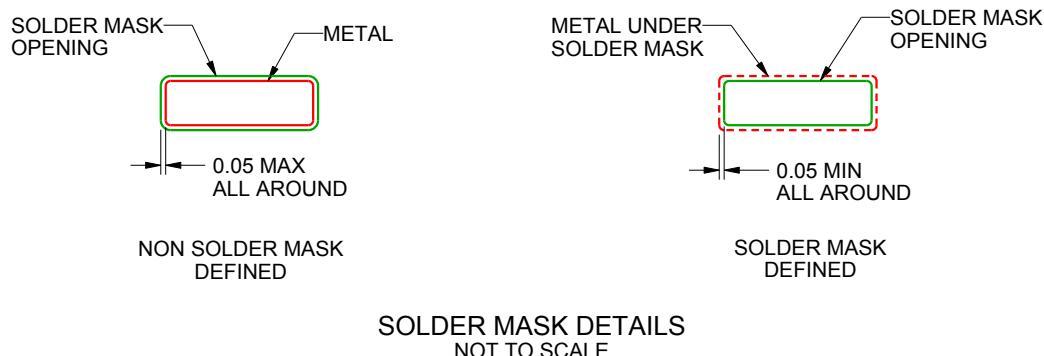
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

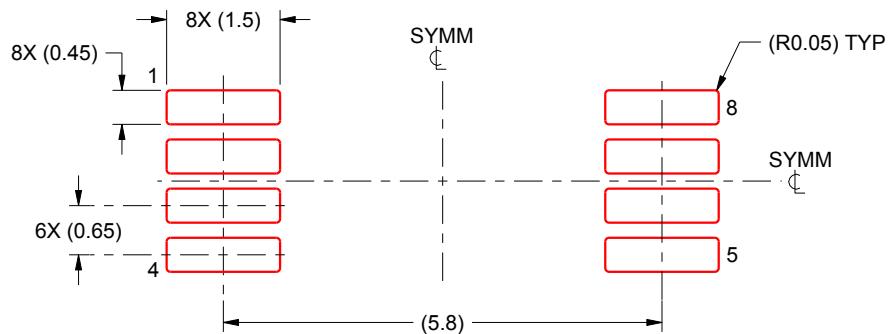
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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