Universidade Federal do Rio Grande do Sul

INF01058 - Circuitos Digitais

Documentação Hardware Unidade Lógica Aritmética

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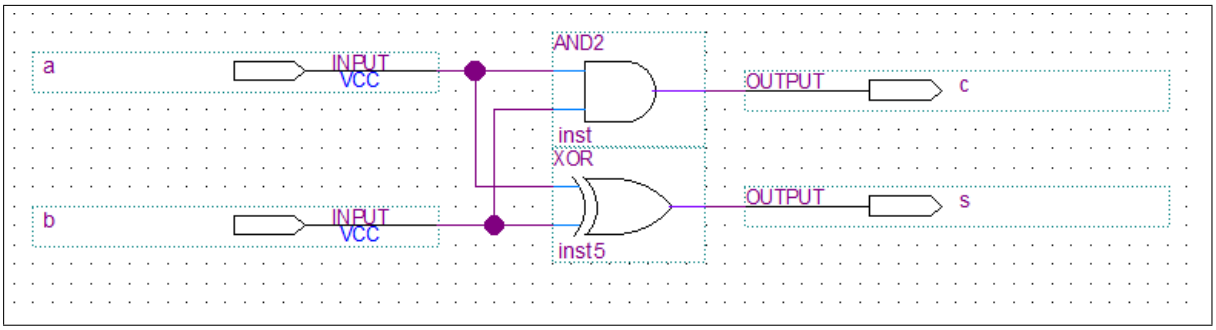
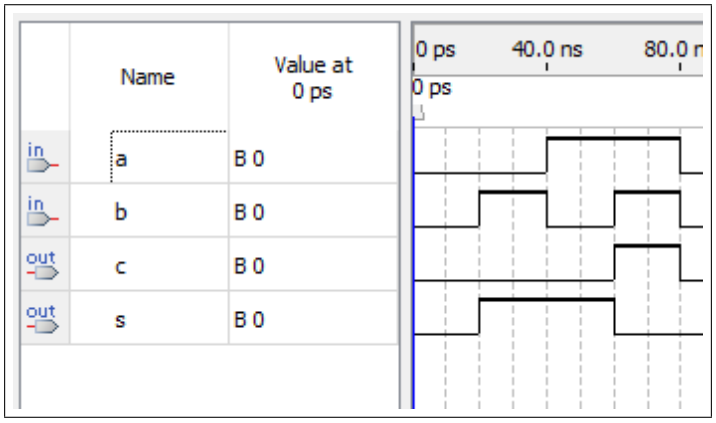
Sumário

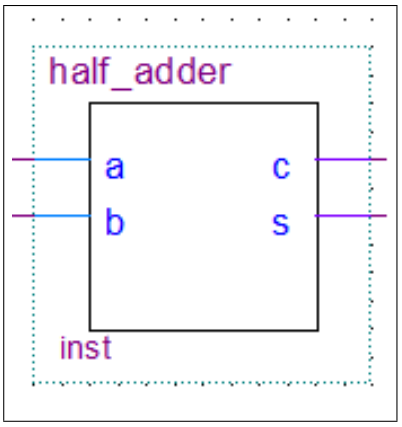
1 Operadores Aritméticos

1.1 Meio somador

Realiza a soma de 2 dígitos binários, devolvendo o valor do primeiro bit da soma em s e o segundo bit em c (carry).

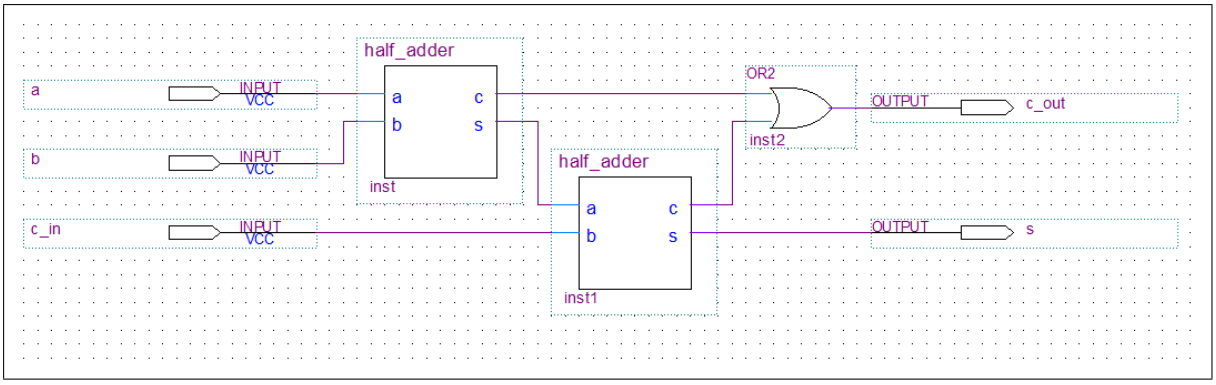


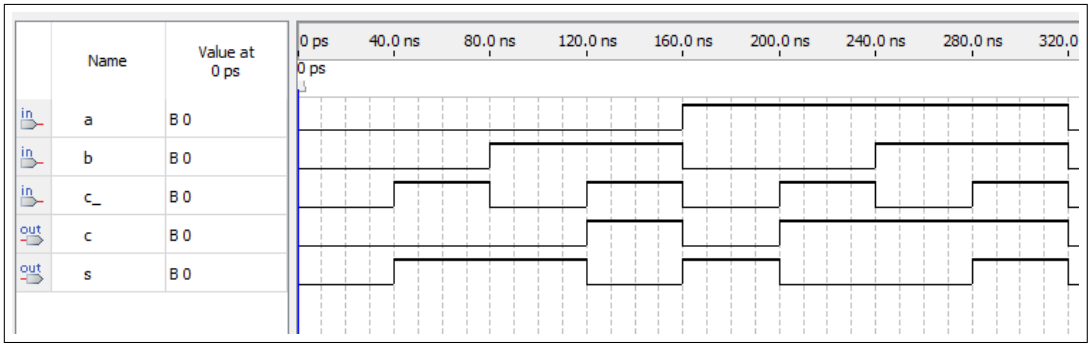


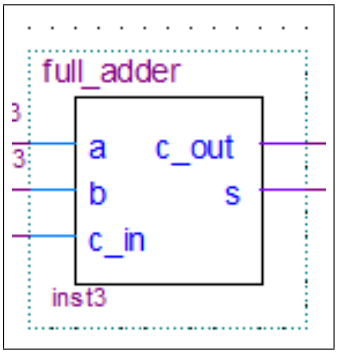


1.2 Somador completo

Realiza a soma de 3 dígitos binários, devolvendo o valor do primeiro bit da soma em s e o segundo bit em c (carry).

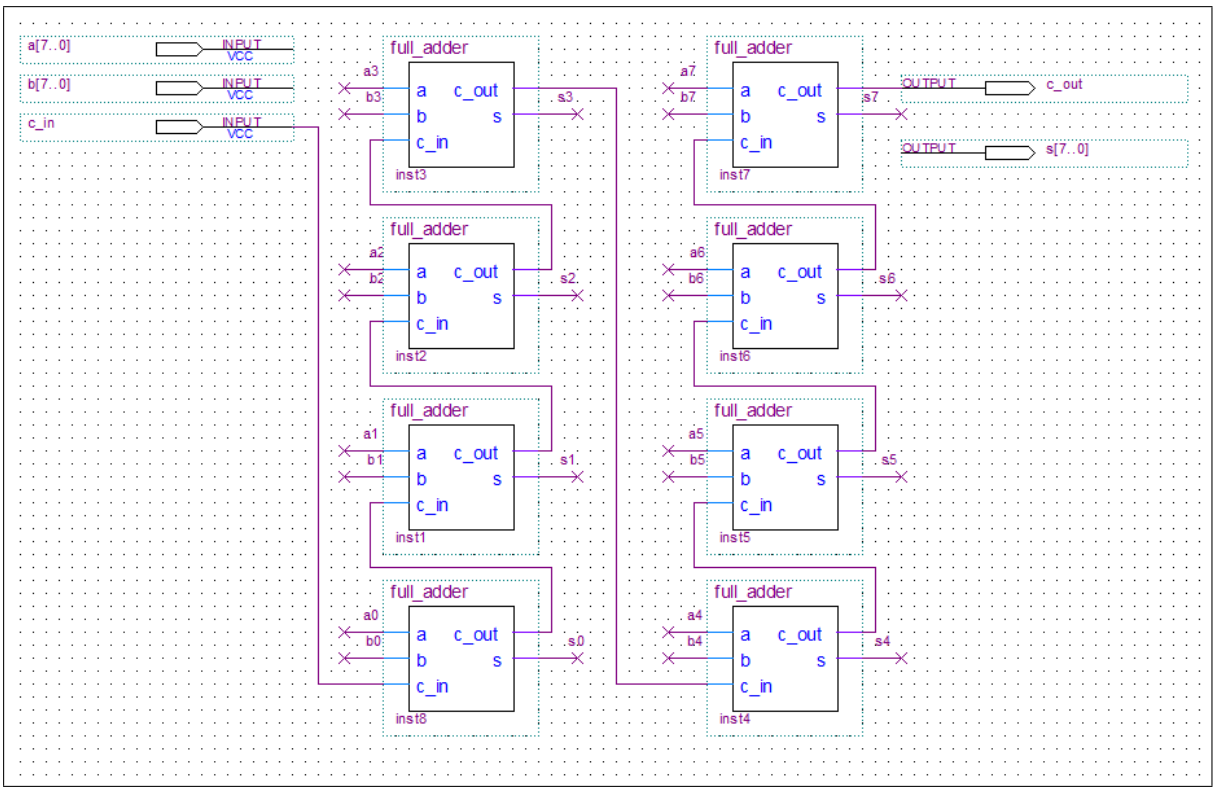


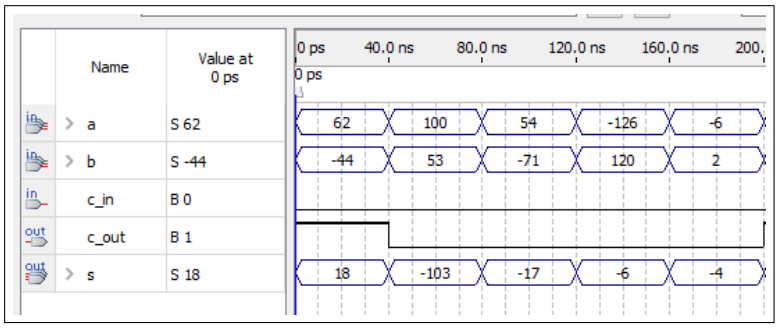


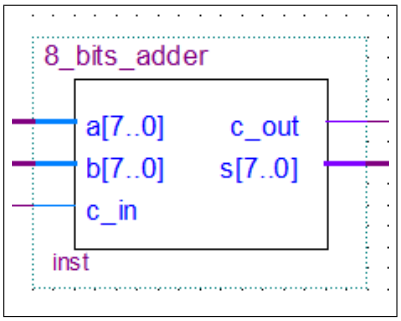


1.3 Somador 8 bits

Realiza a soma de 2 sinais binários de 8 bits. Caso seja inserido 1 na entrada c_in, o resultado será acrescido de 1, o que possibilita a utilização da mesma porta aritmética para realização de subtração, negando b, ou de inversão de sinal, colocando a entrada cujo sinal deve ser trocado em b, c_in em 1 e a em 0.



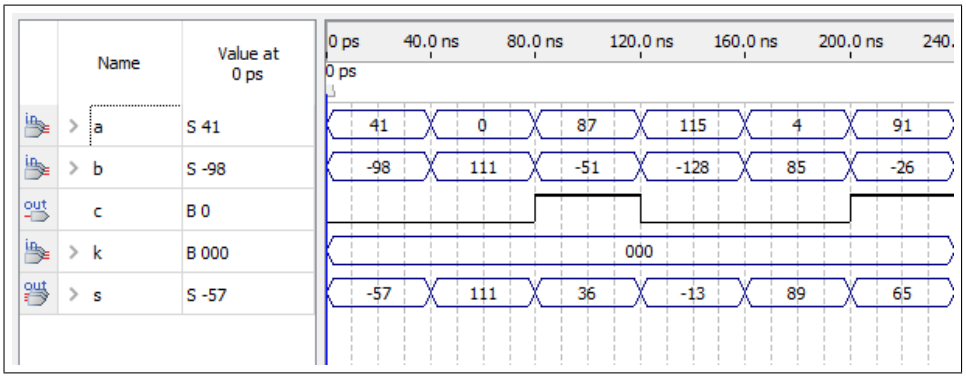


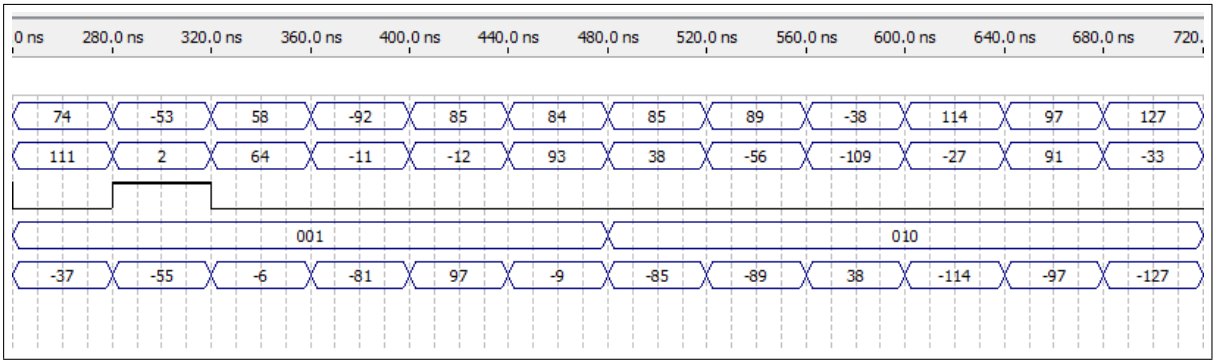


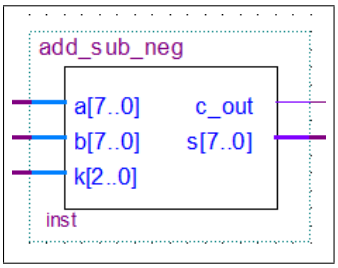
1.4 Somador, subtrator e inversor de sinal

Realiza as operações de soma, subtração e inversão de sinal de acordo com os valores para o controle k.

código	mnemônico	operação
000	ADD	Adição
001	SUB	Subtração
010	NEG	Inversão



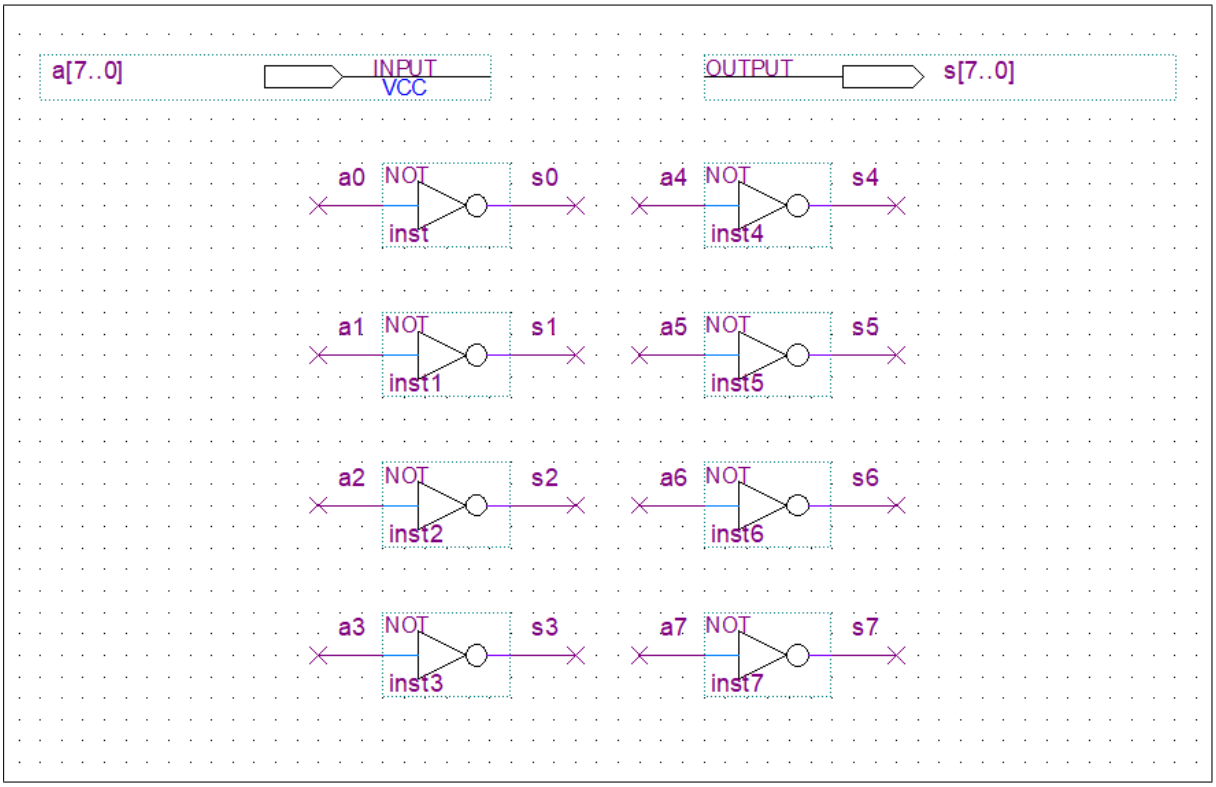


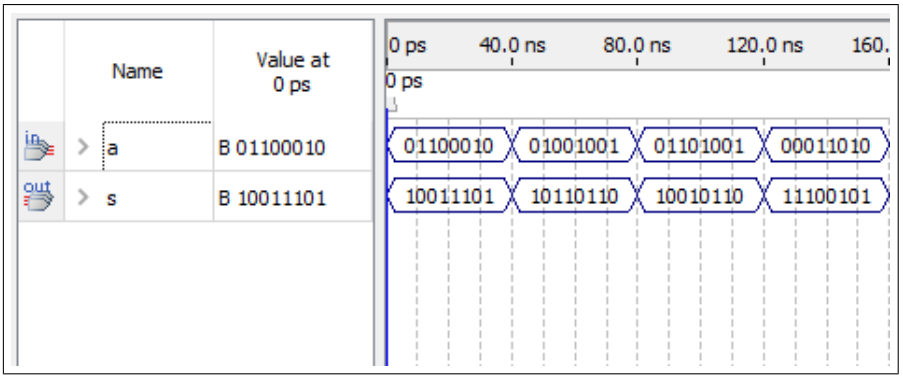


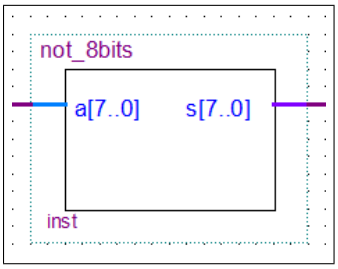
2 Operadores Lógicos

2.1 Not 8 bits

Realiza a operação not em cada um dos bits de um barramento de 8 bits.

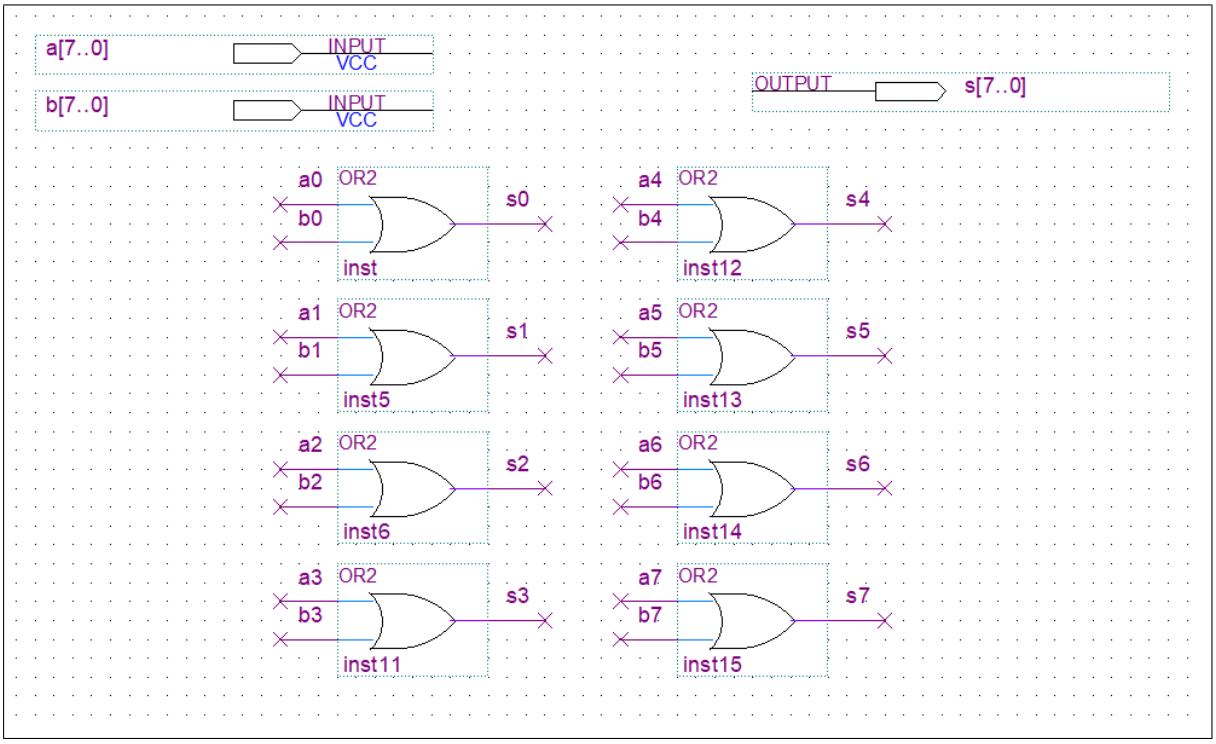


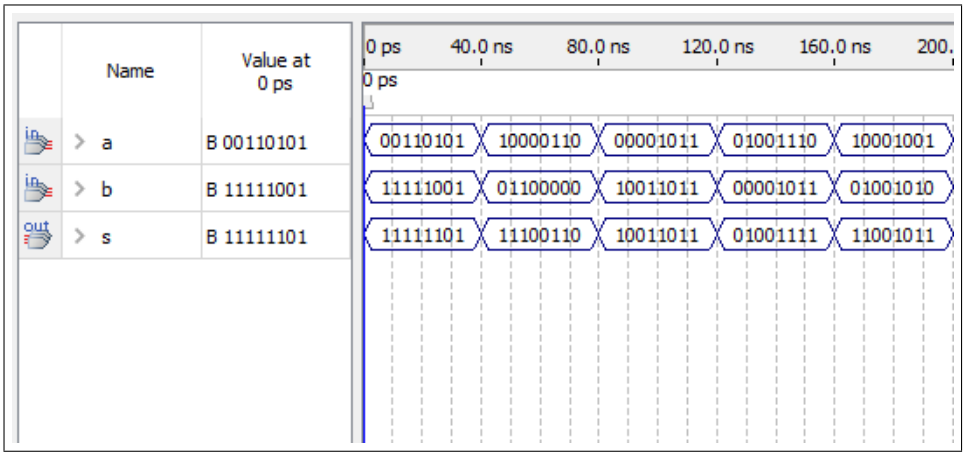


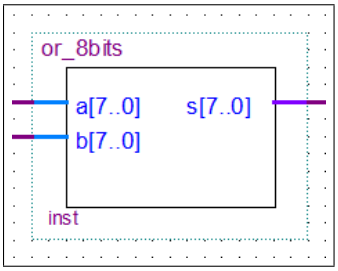


2.2 Or 8 bits

Realiza a operação or em cada um dos bits de um barramento de 8 bits.

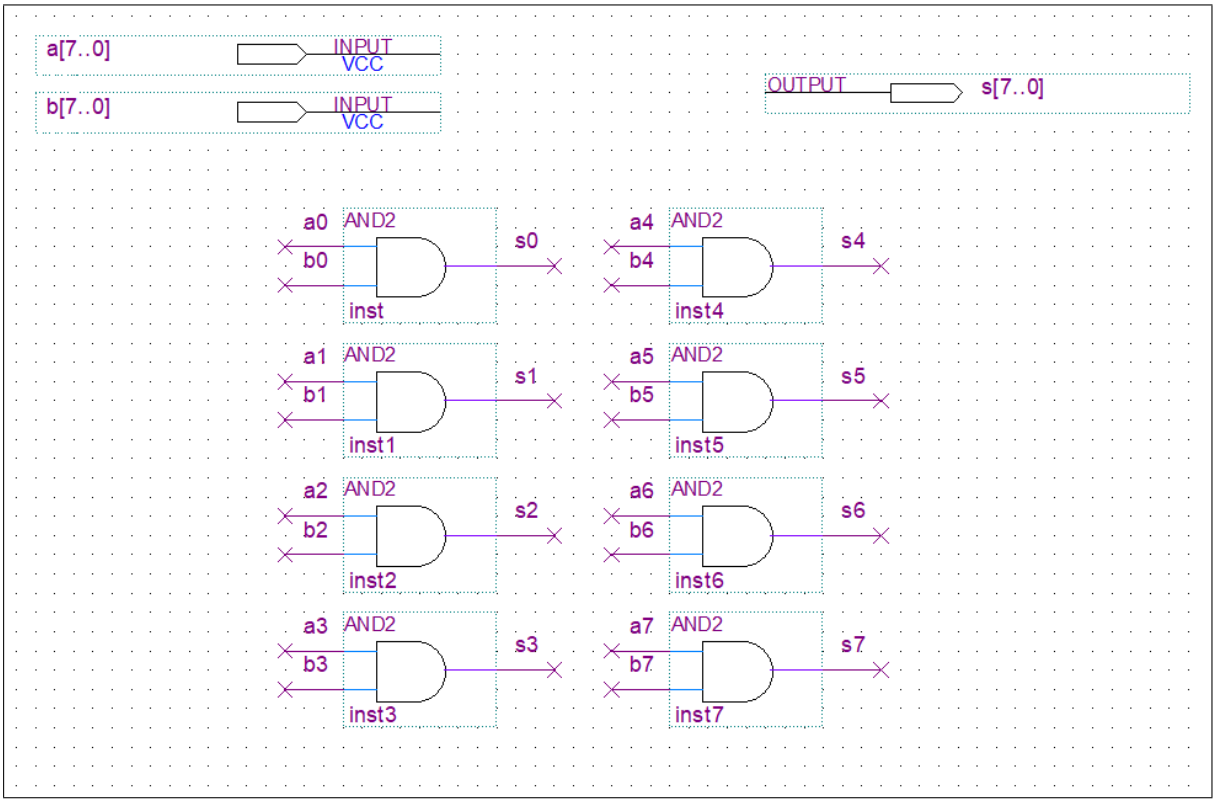


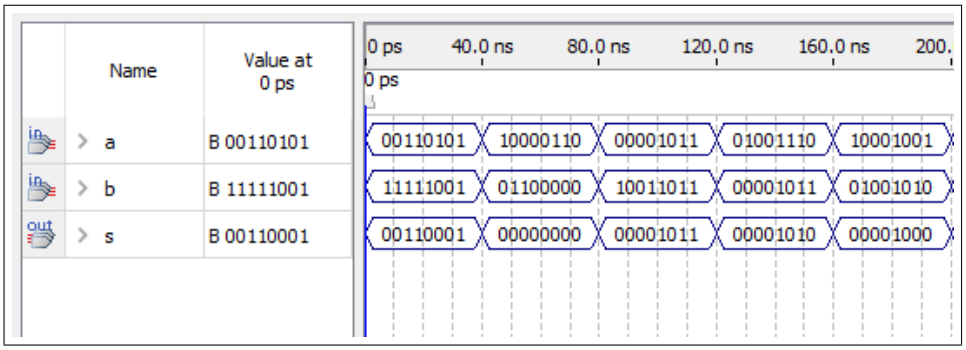


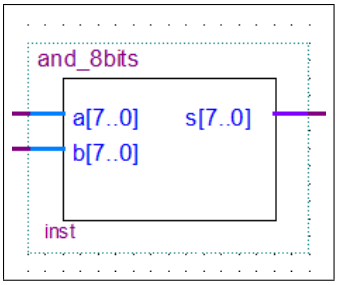


2.3 And 8 bits

Realiza a operação and em cada um dos bits de um barramento de 8 bits.

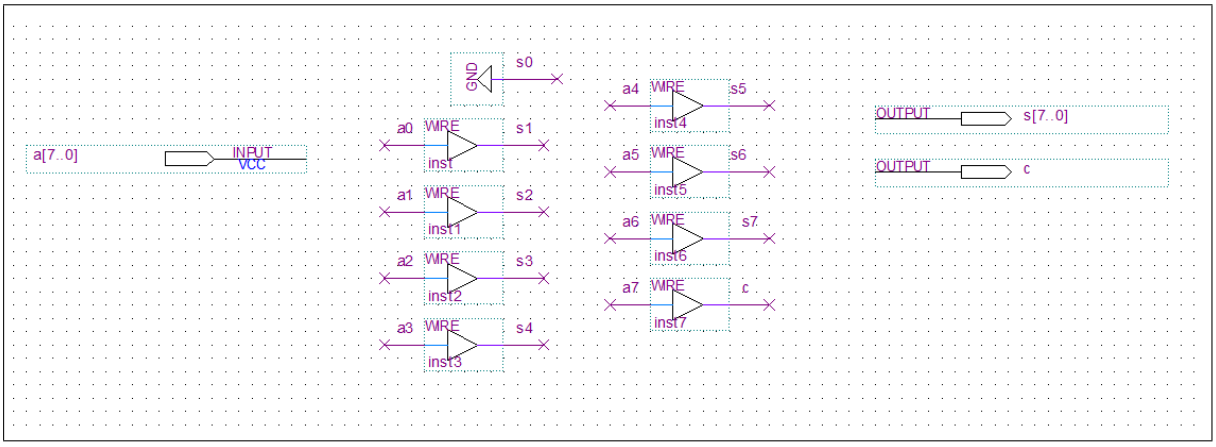


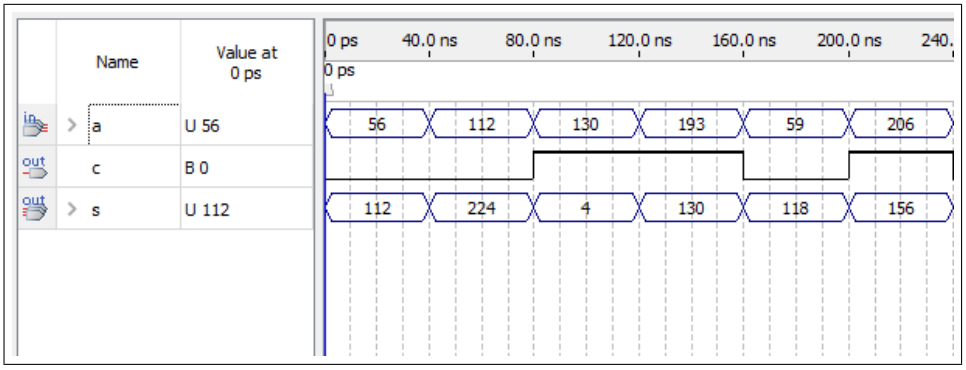


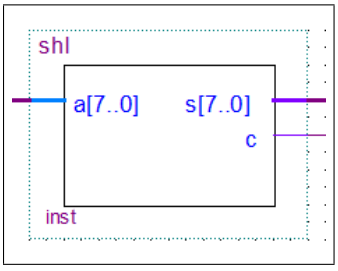


2.4 Shift Left 8 bits

Move cada um dos bits de um barramento de 8 bits para uma posição à esquerda. O bit mais significativo é enviado para a saída *c*. Equivale aritmeticamente a uma multiplicação por 2.



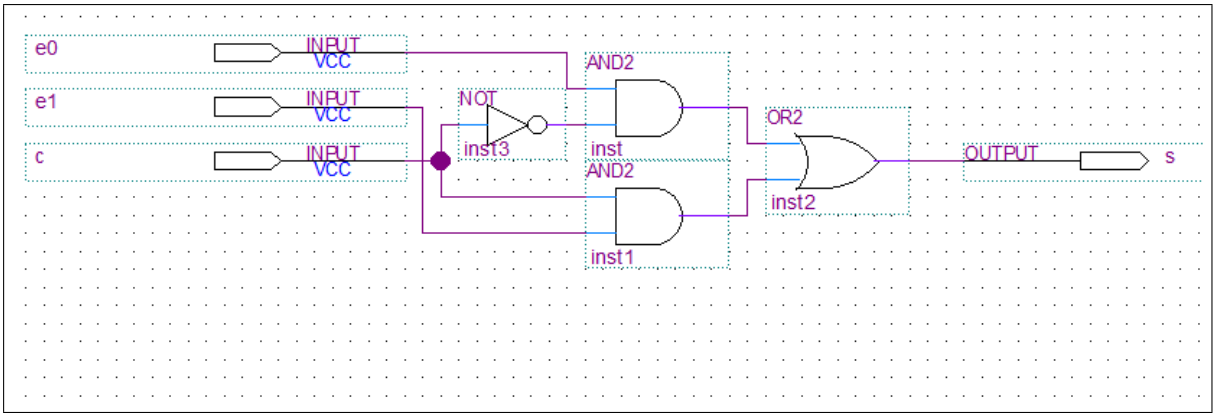


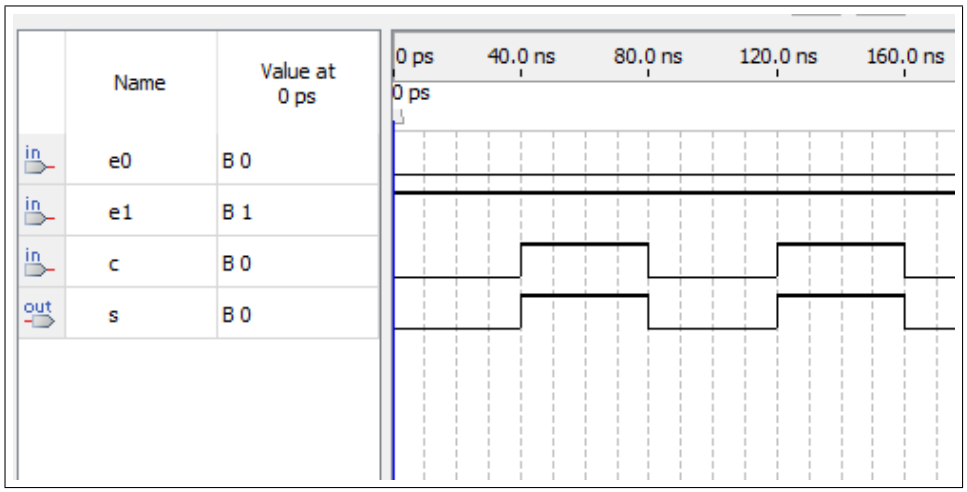


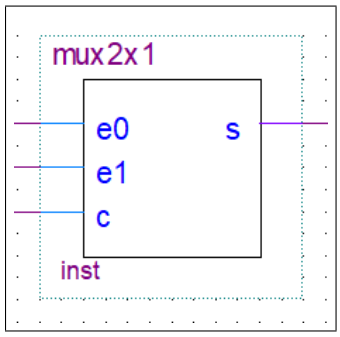
3 Circuitos de seleção

3.1 Mux 2x1

Seleciona uma de 2 entradas de acordo com o sinal de controle k.

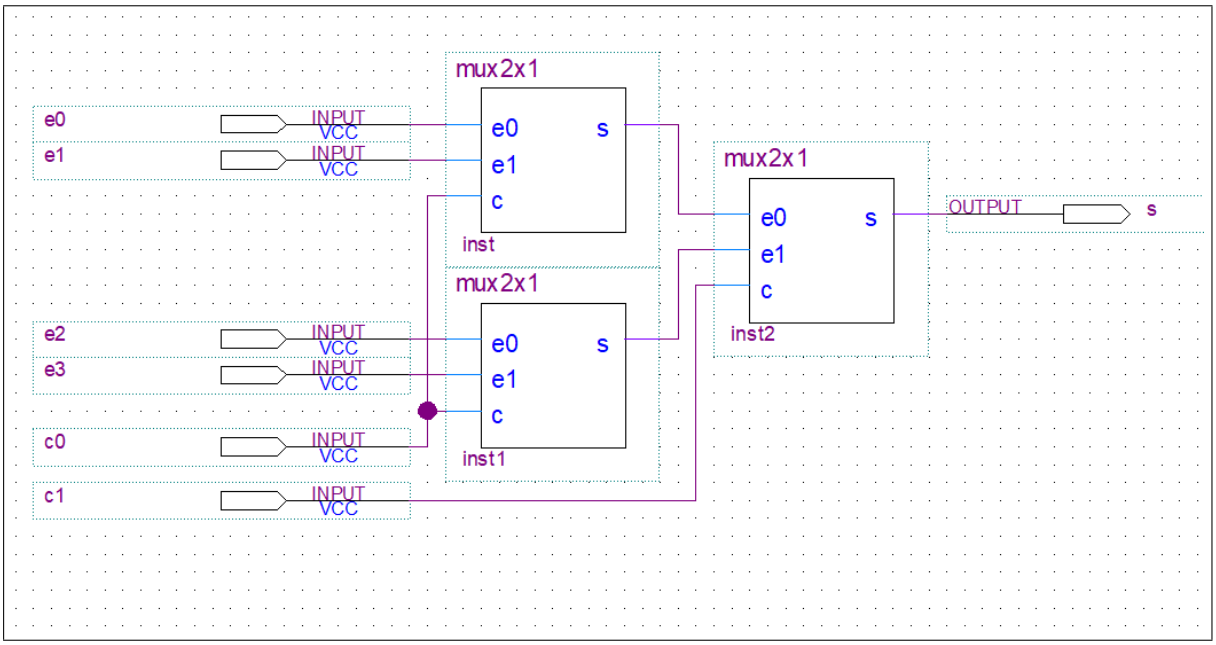


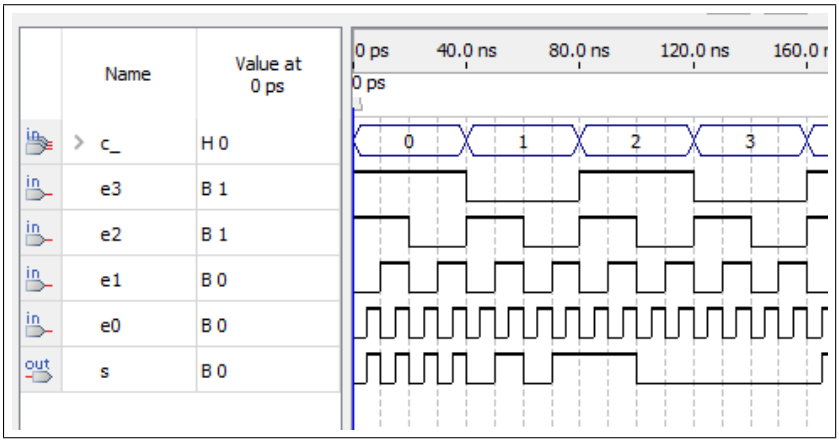


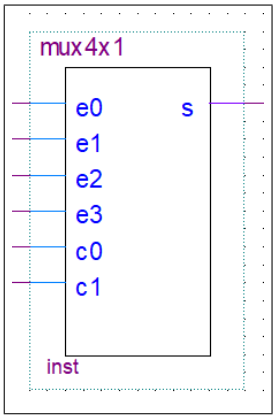


3.2 Mux 4x1

Seleciona uma de 4 entradas de acordo com o sinal de controle k de 2 bits.

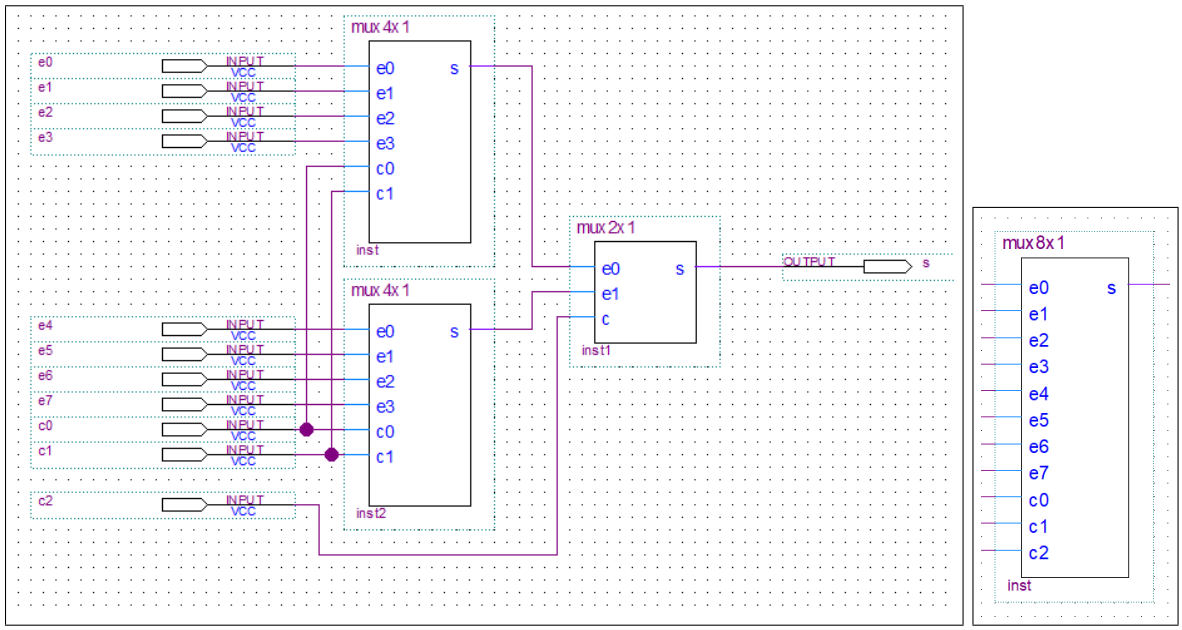


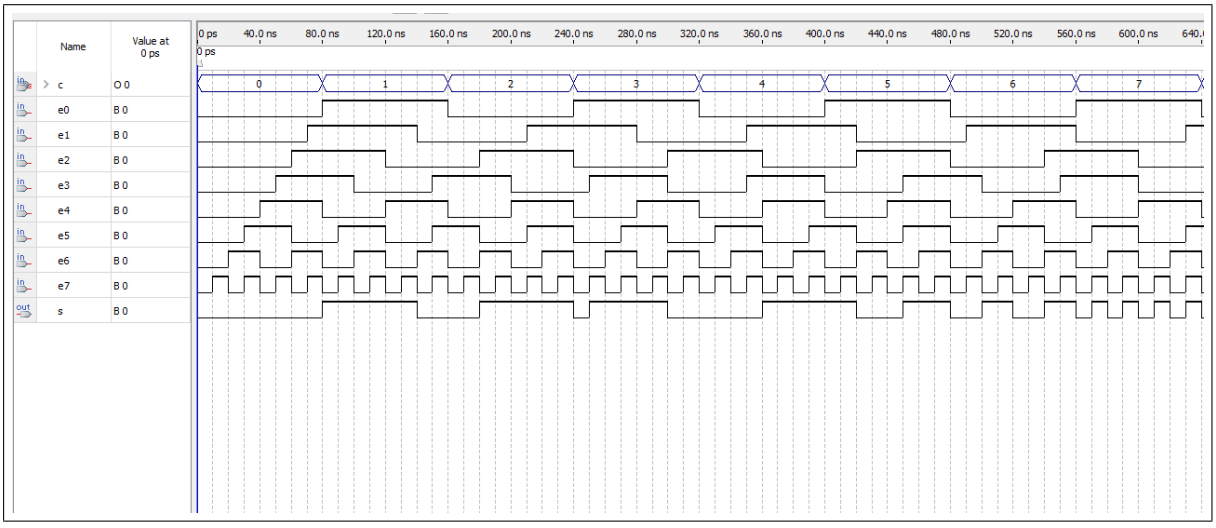




3.3 Mux 8x1

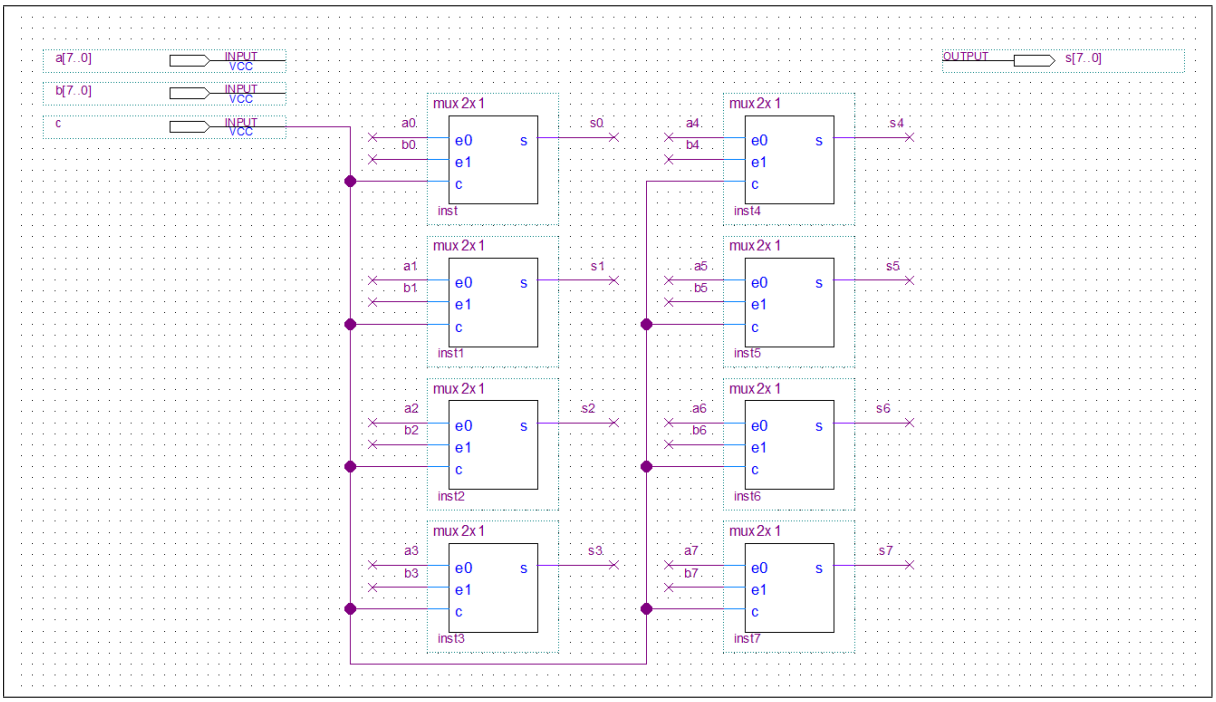
Seleciona uma de 8 entradas de acordo com o sinal de controle k.

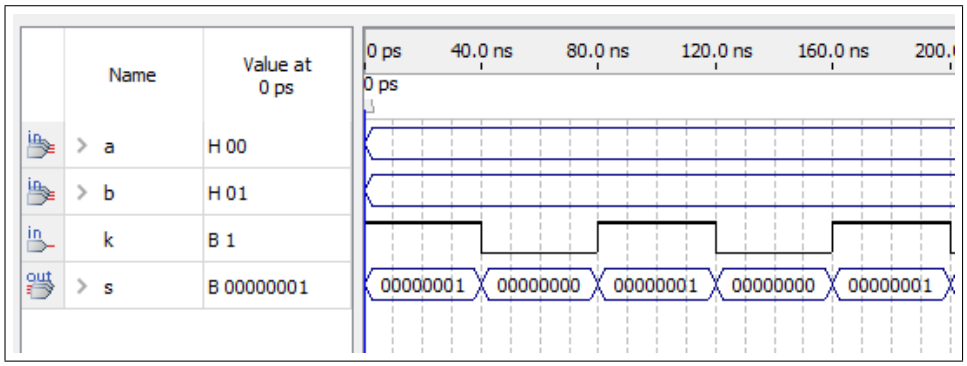


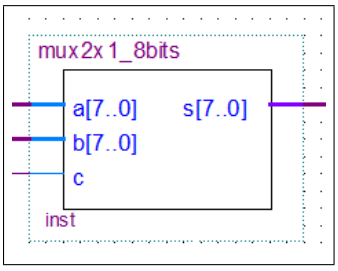


3.4 Mux 2x1 de 8 bits

Seleciona uma de 2 entradas de 8 bits cada de acordo com o sinal de controle k.

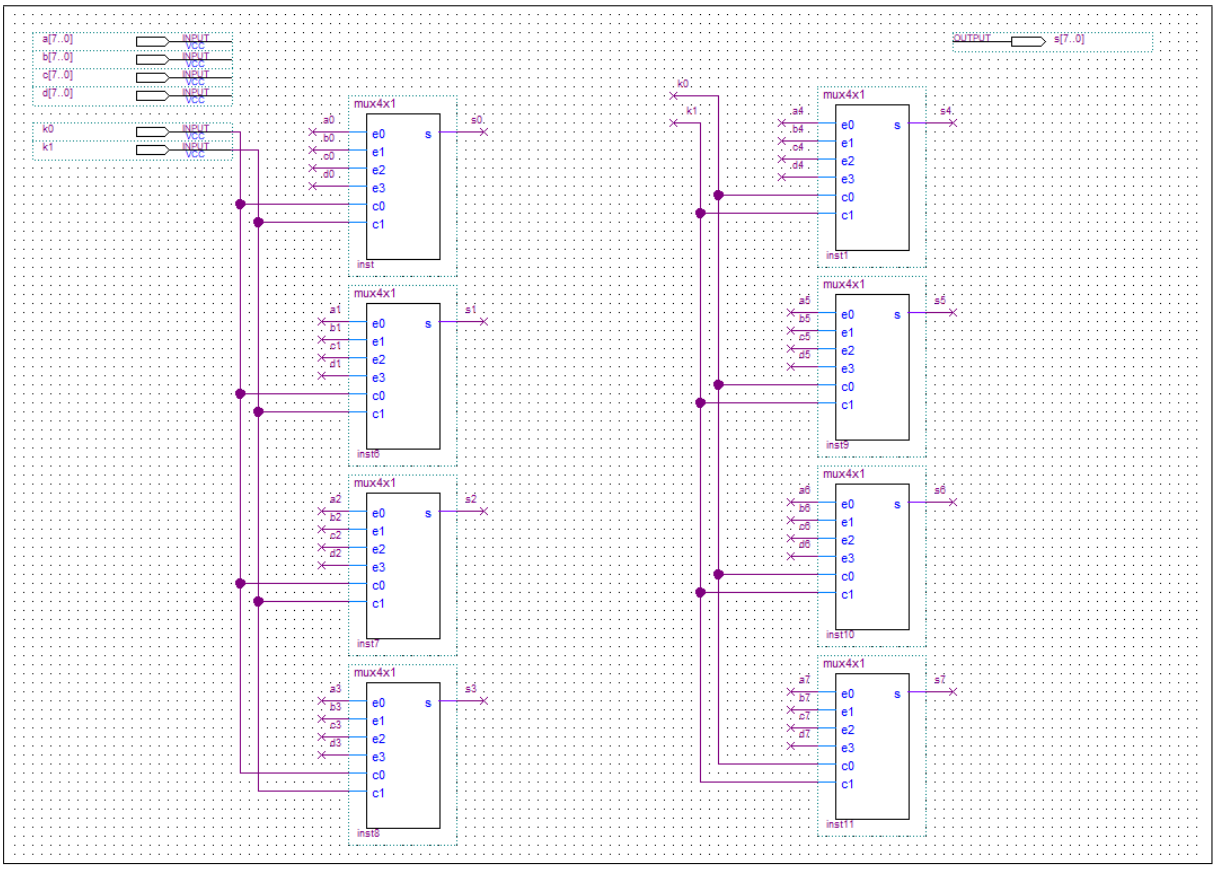


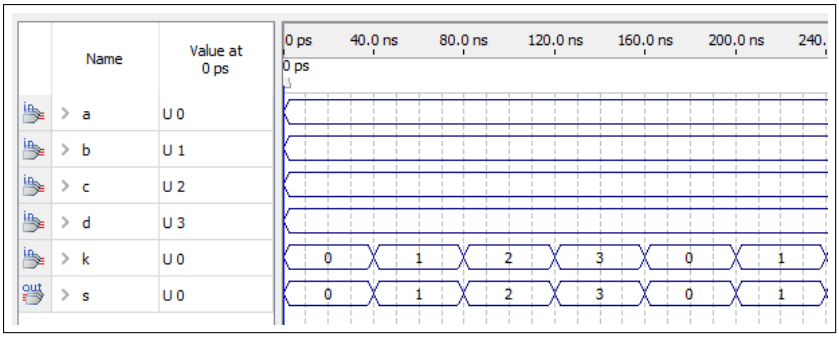


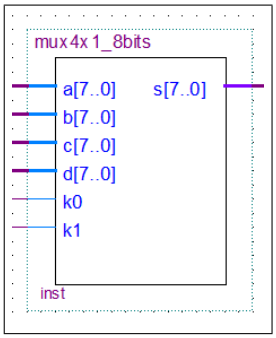


3.5 Mux 4x1 de 8 bits

Seleciona uma de 4 entradas de acordo com o sinal de controle k de 2 bits.

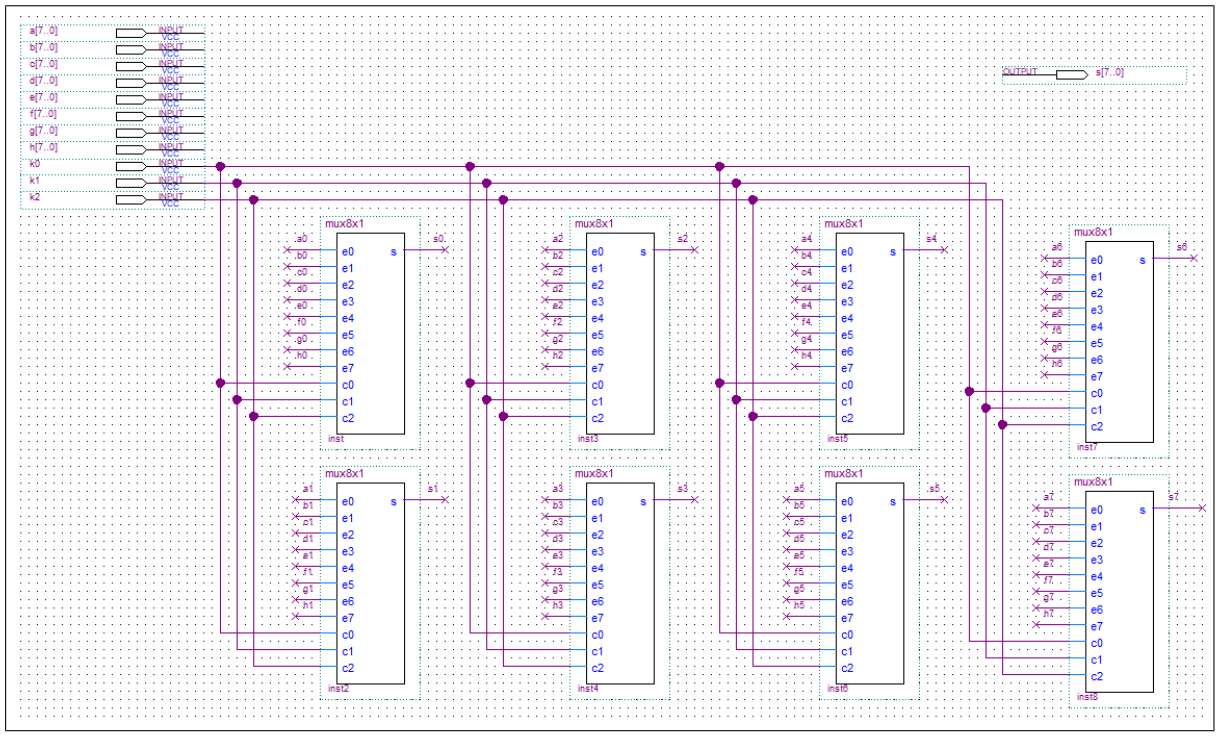


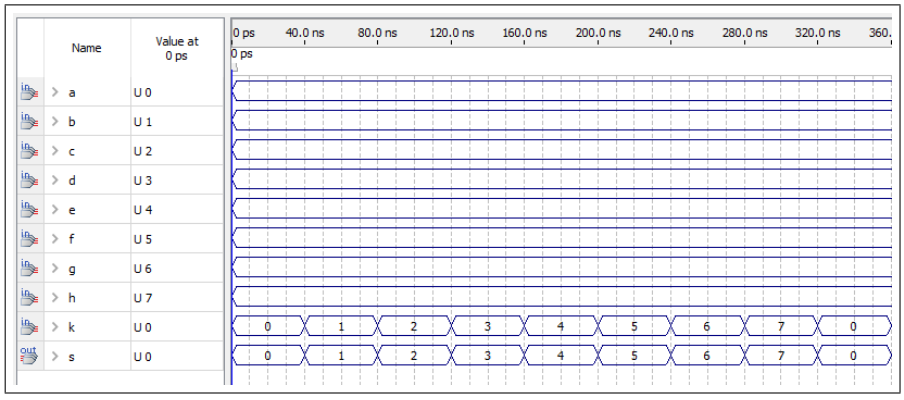


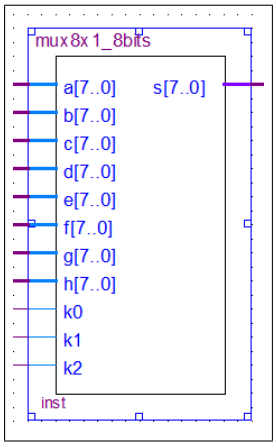


3.6 Mux 8x1 de 8 bits

Seleciona uma de 8 entradas de acordo com o sinal de controle k.



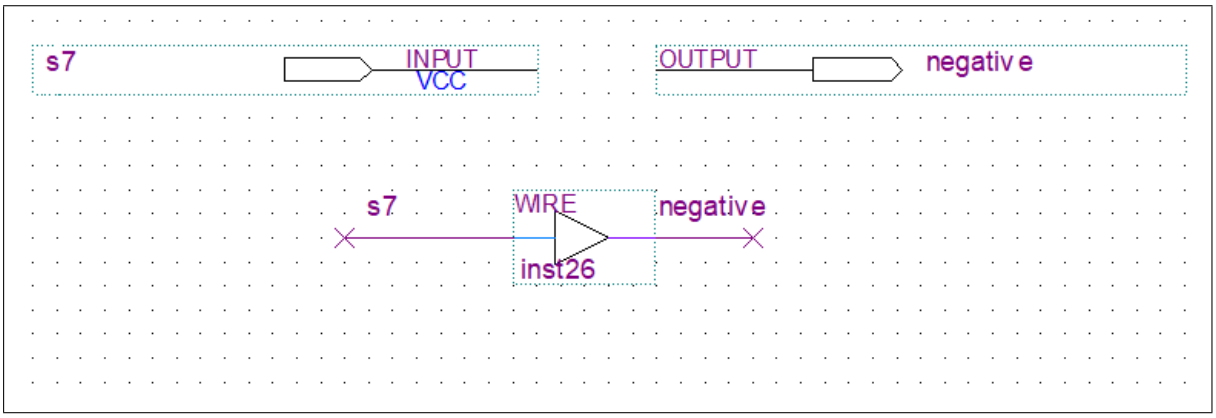


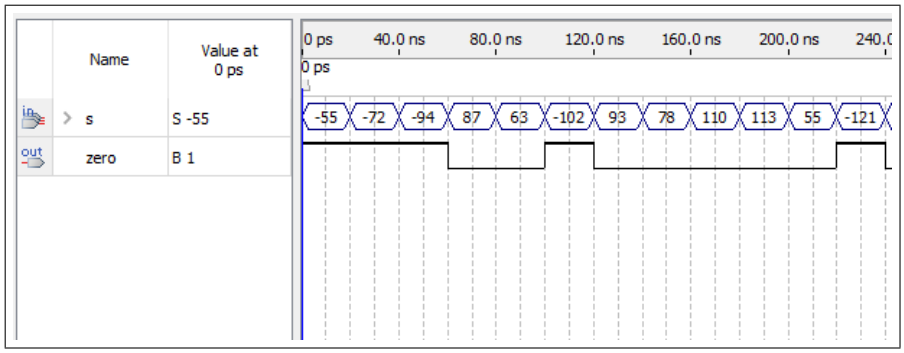


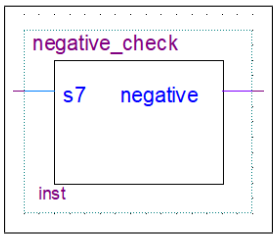
4 Verificadores de flags

4.1 Verificador Negativo

Retorna 1 se a entrada for negativa em complemento de 2

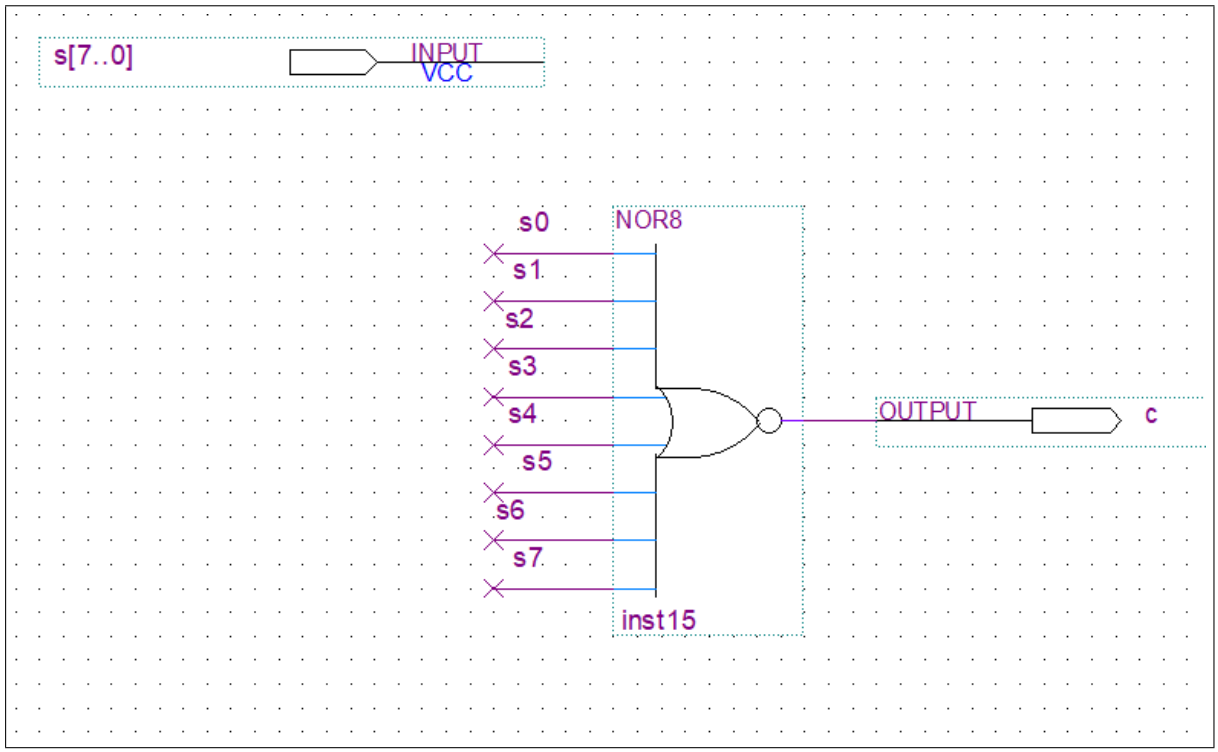


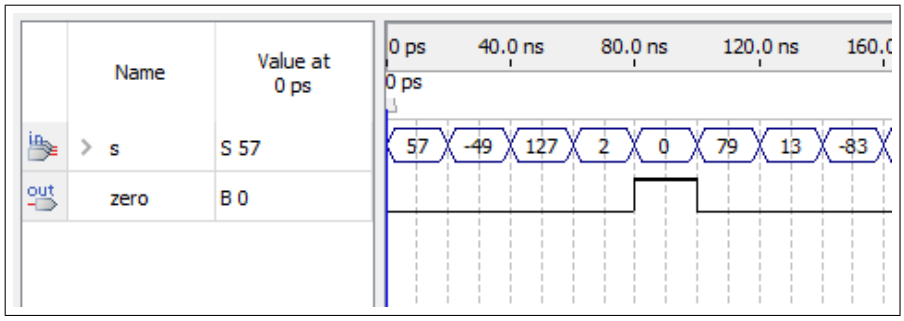


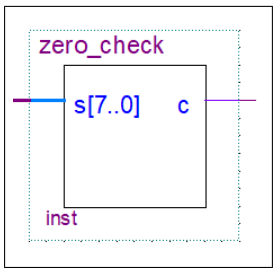


4.2 Verificador Zero

Retorna 1 se o valor de entrada é zero

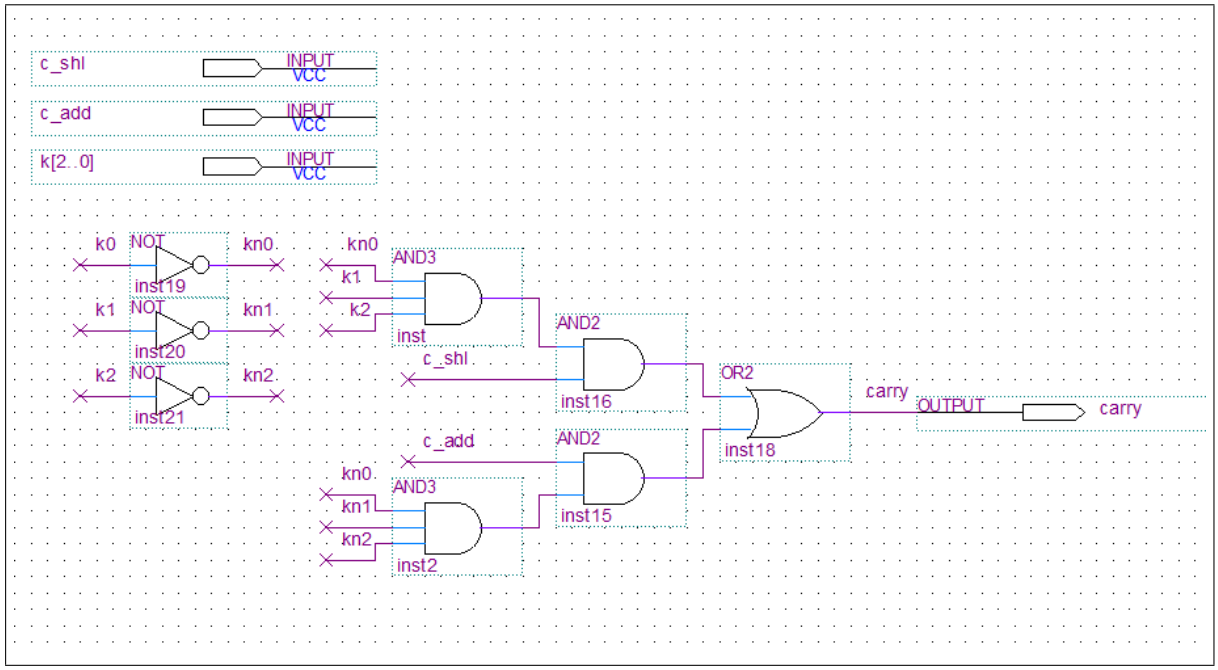


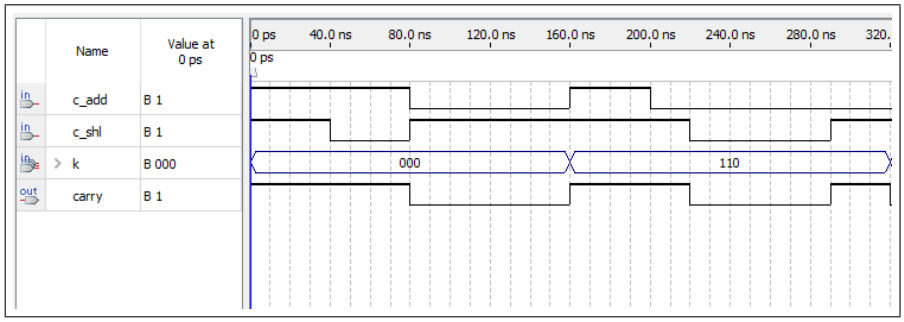


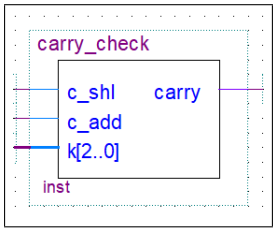


4.3 Verificador Carry

Retorna 1 se houve um carry na realização de uma soma ou um shift left. Caso não seja nenhuma dessas operações que esteja sendo realizada, o retorno da função é descartado.

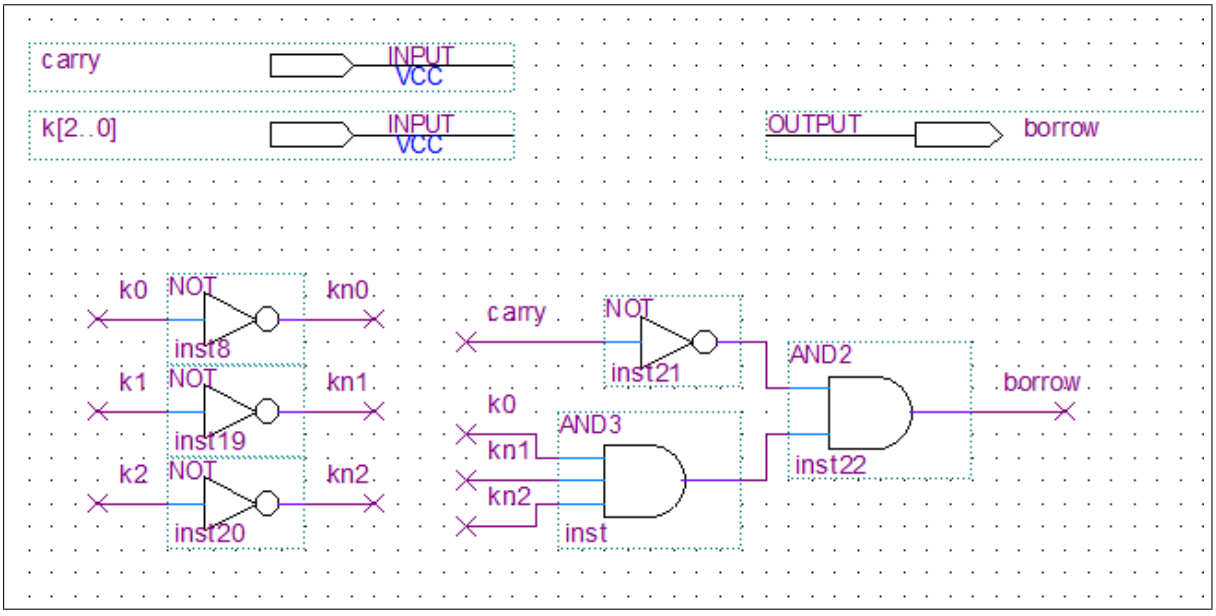


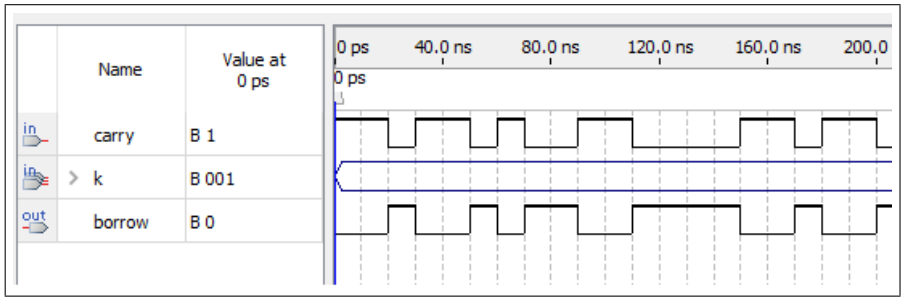


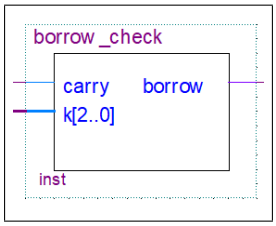


4.4 Verificador Borrow

Verifica se houve um borrow durante a execução de uma subtração. Caso a operação executada não seja uma subtração o valor deve ser desprezado.

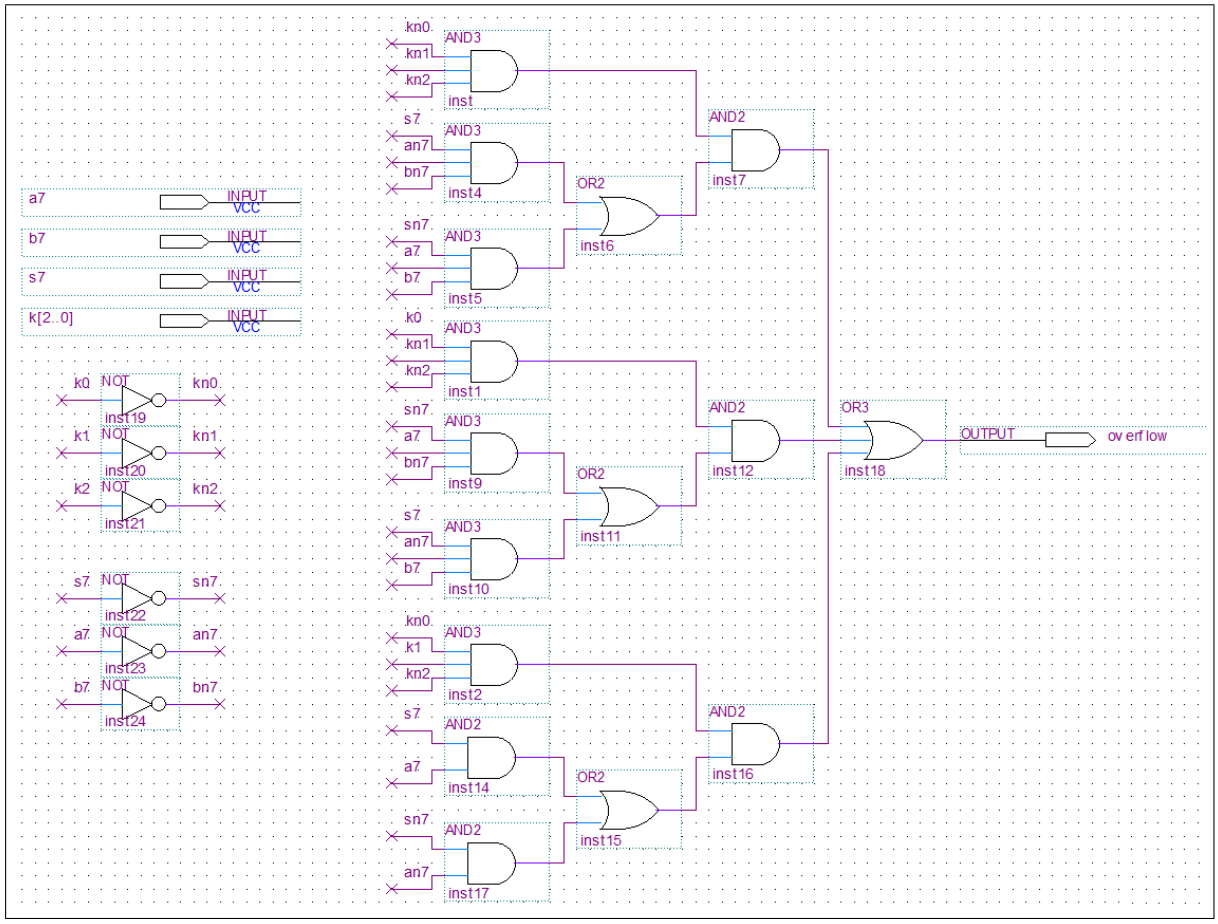


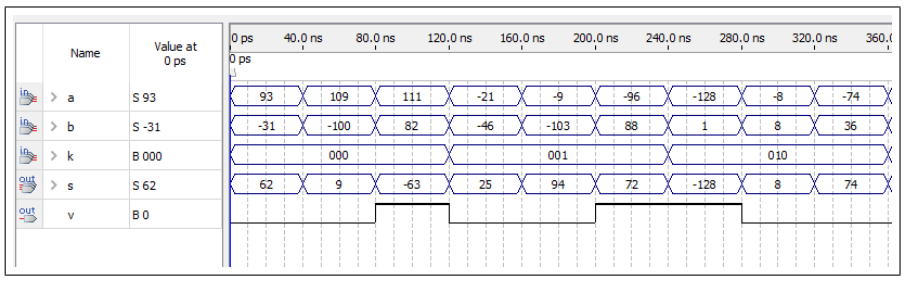


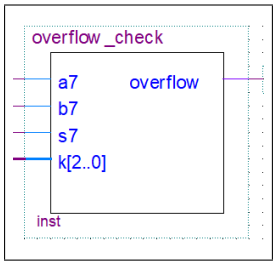


4.5 Verificador Overflow

Verifica se houve um estouro de representação durante a execução de uma soma, subtração ou negação. Caso a operação executada não seja uma dessas, o valor deve ser desprezado.



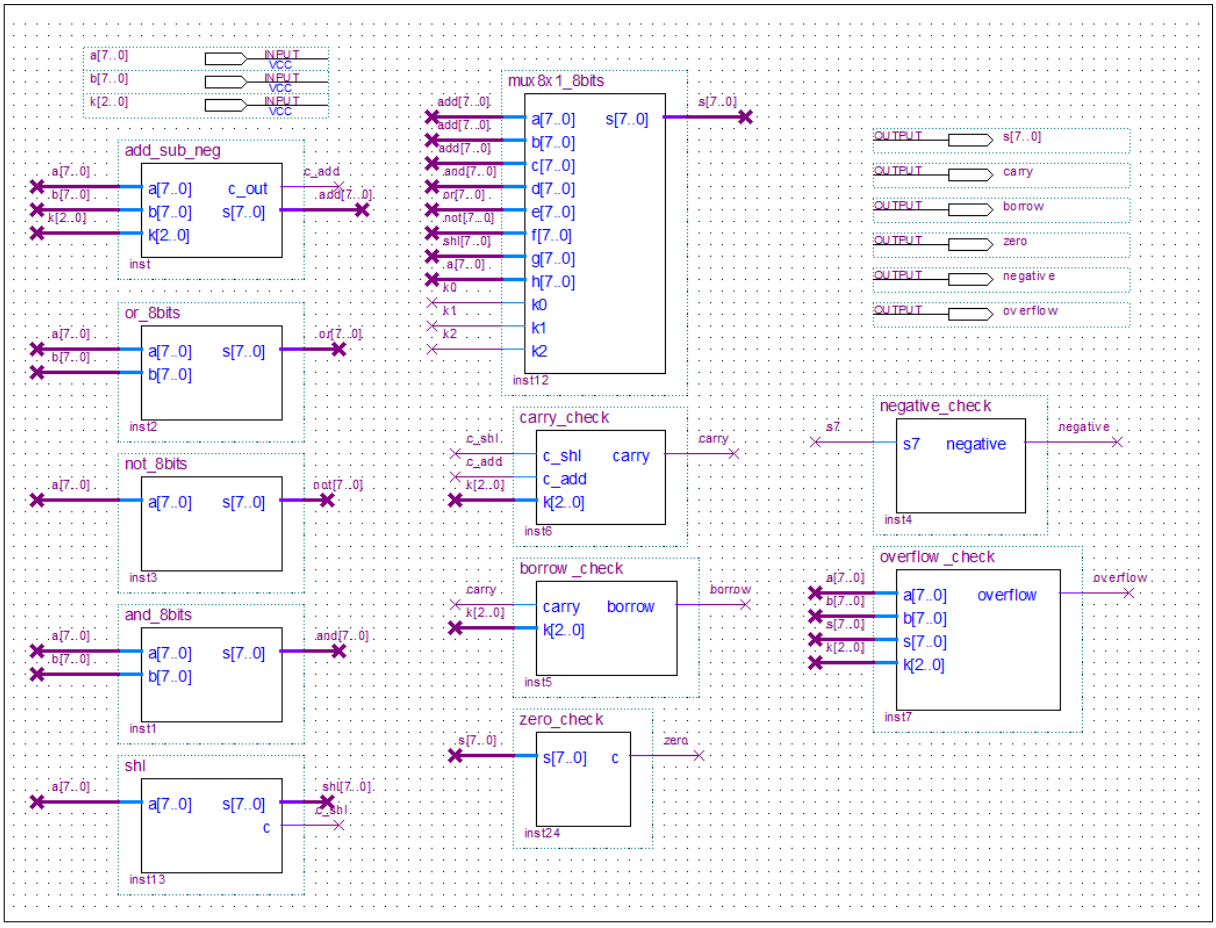




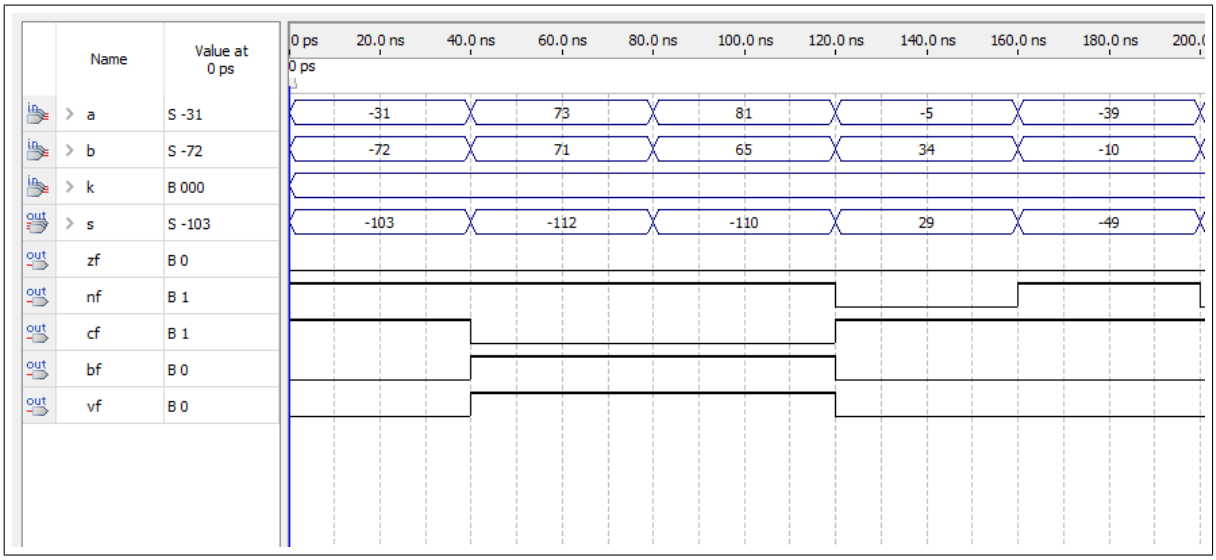
5 Unidade Lógica Aritmética

Ajusta os flags e executa a operação indicada pelo barramento de 3 bits $k[2..0]$, de acordo com a seguinte tabela.

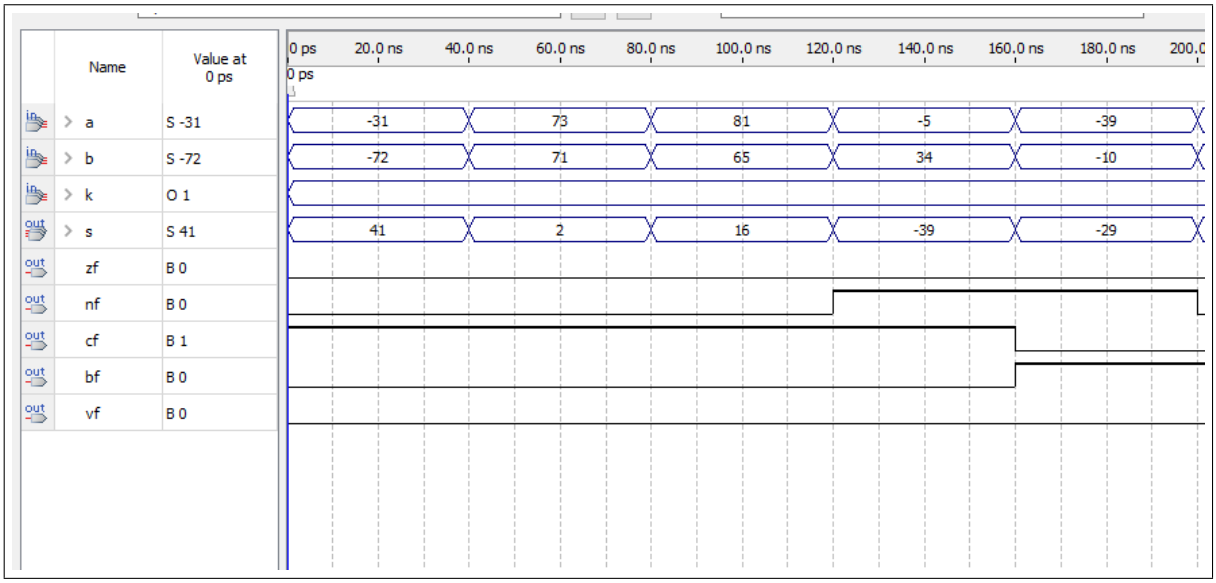
código	Hexadecimal	mnemônico	operação	flags
000	H0	ADD	Adição	N, Z, C, V
001	H1	SUB	Subtração	N, Z, B, V
010	H2	NEG	Inversão	N, Z, V
011	H3	AND	Ou lógico	N, Z
100	H4	OR	E lógico	N, Z
101	H5	NOT	Não lógico	N, Z
110	H6	SHL	Shift Left	N, Z, C
111	H7	NOP	Não altera	N, Z



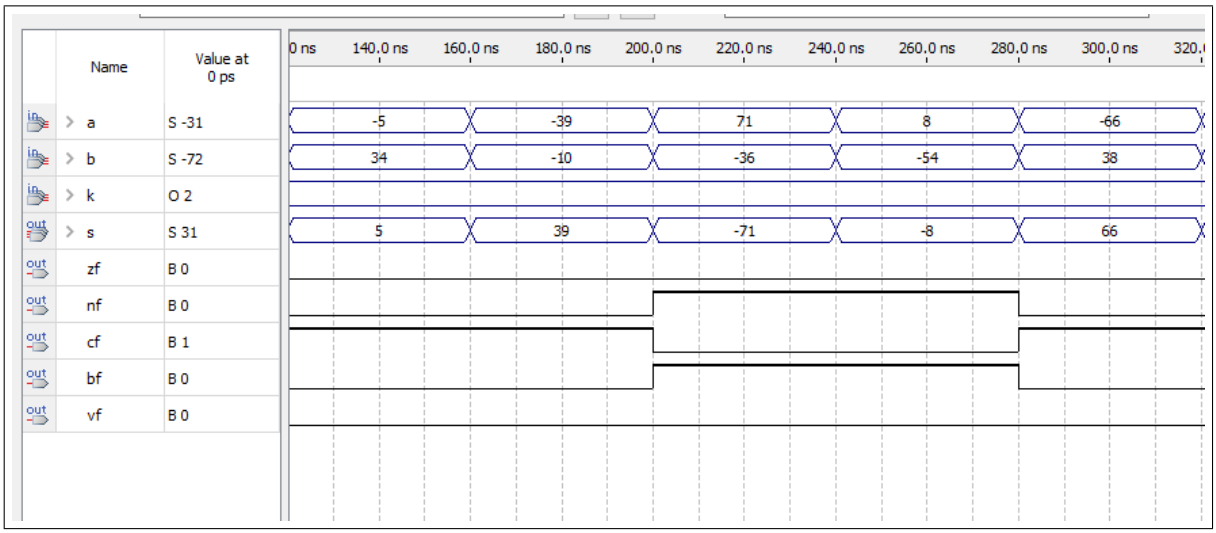
5.1 Adição



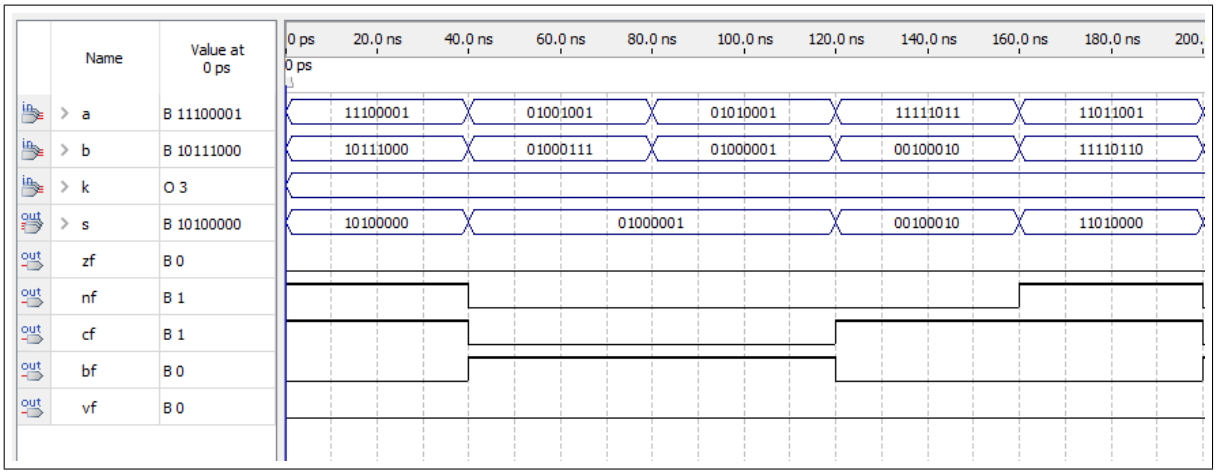
5.2 Subtração



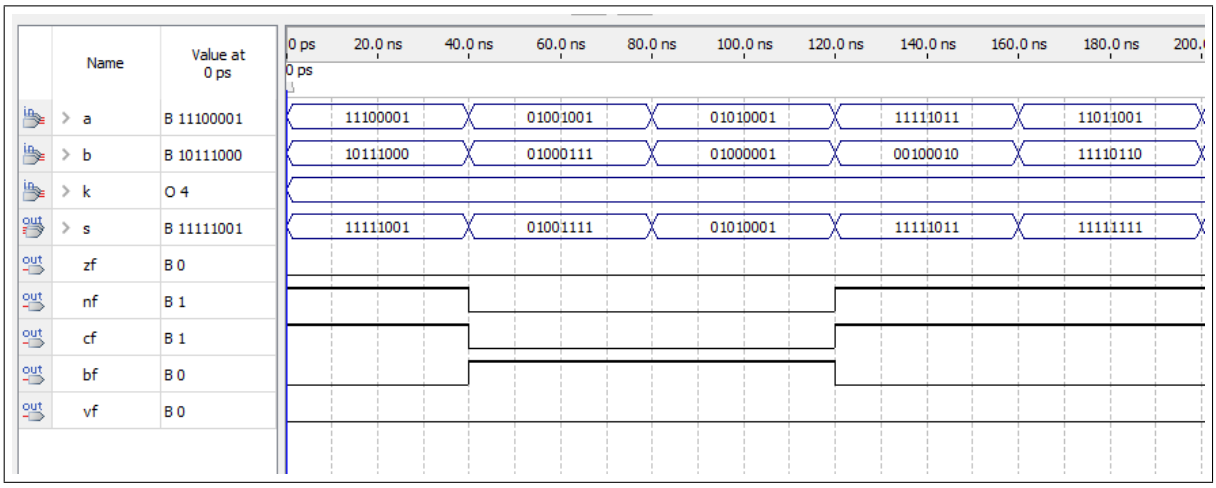
5.3 Negação



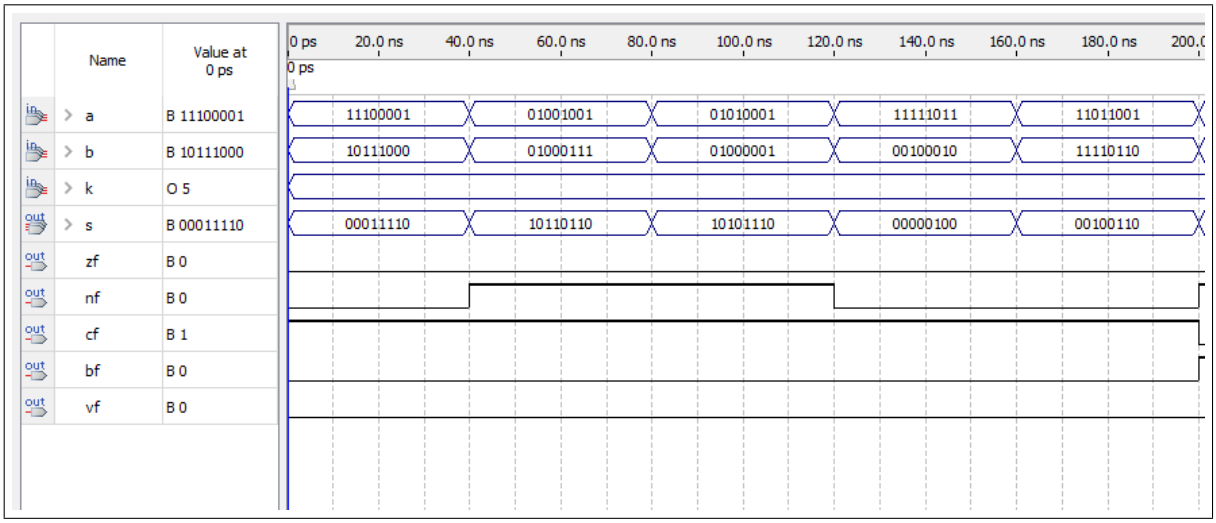
5.4 And lógico



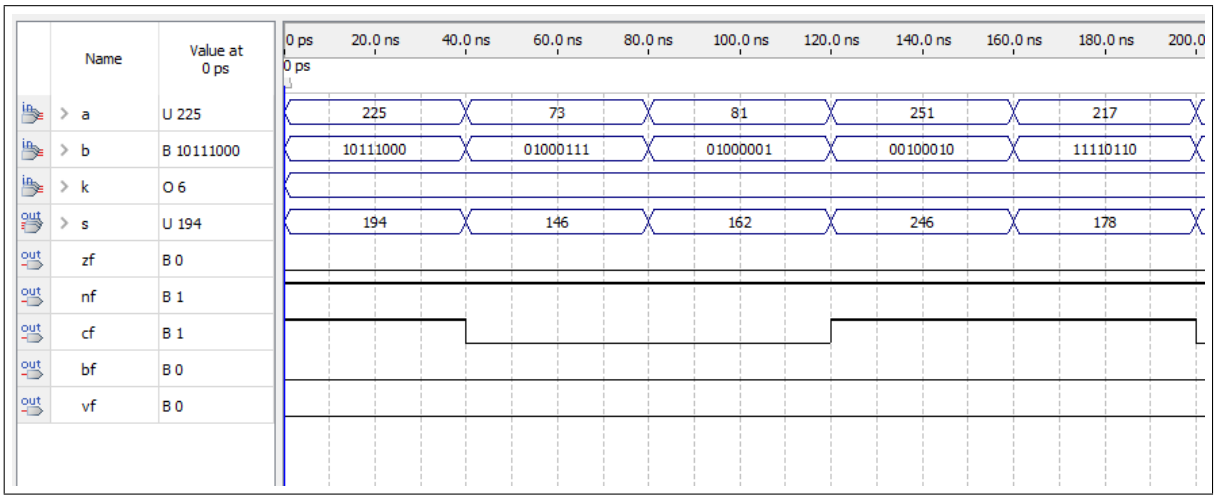
5.5 Or lógico



5.6 Not lógico



5.7 Shift Left



5.8 No Operation