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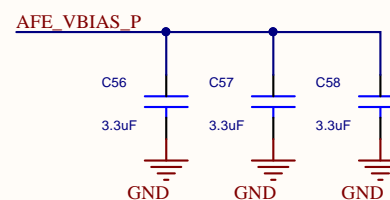
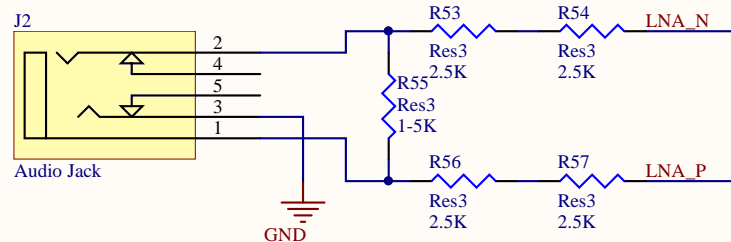
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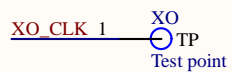
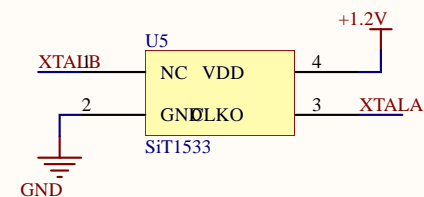
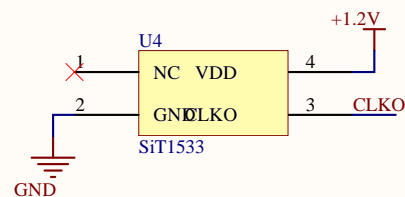
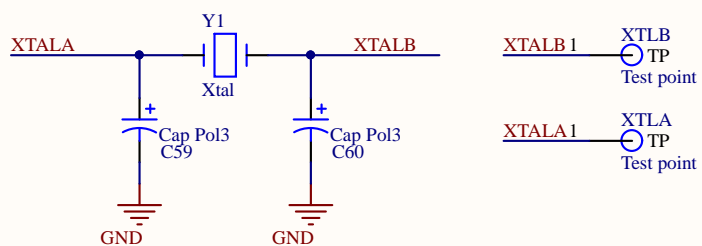
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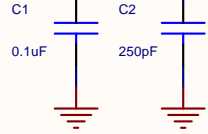
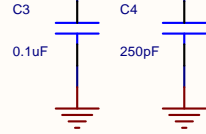
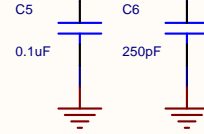
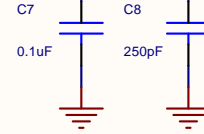
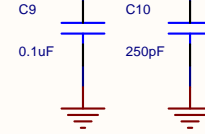
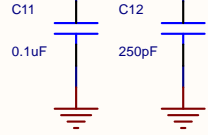
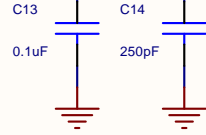
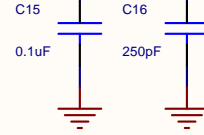
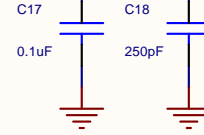
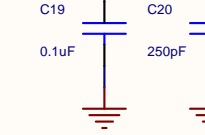
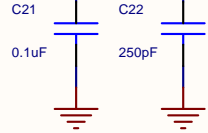
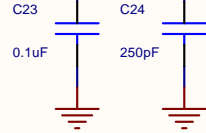
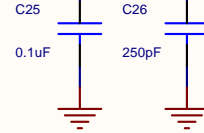
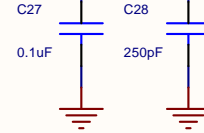


Clock Generation



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Decoupling Capacitors

VDD_2T_UNTRIMVDDVDD_BINVDD_AFEVDD_JTAGVDD_18VDD_10VDD_05VDD_CTRLVDD_PERVDD_SPI_HIVDD_SPI_LOVDDLIOVDDHIO

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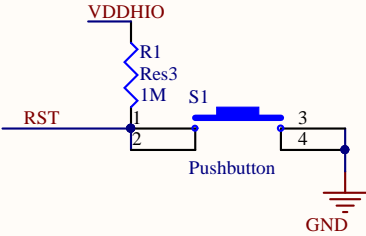
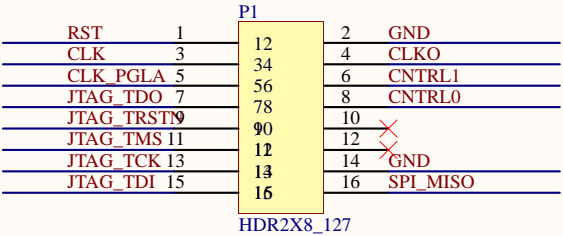
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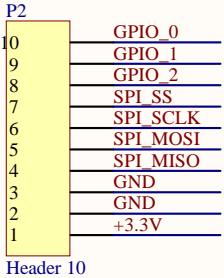
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Programming

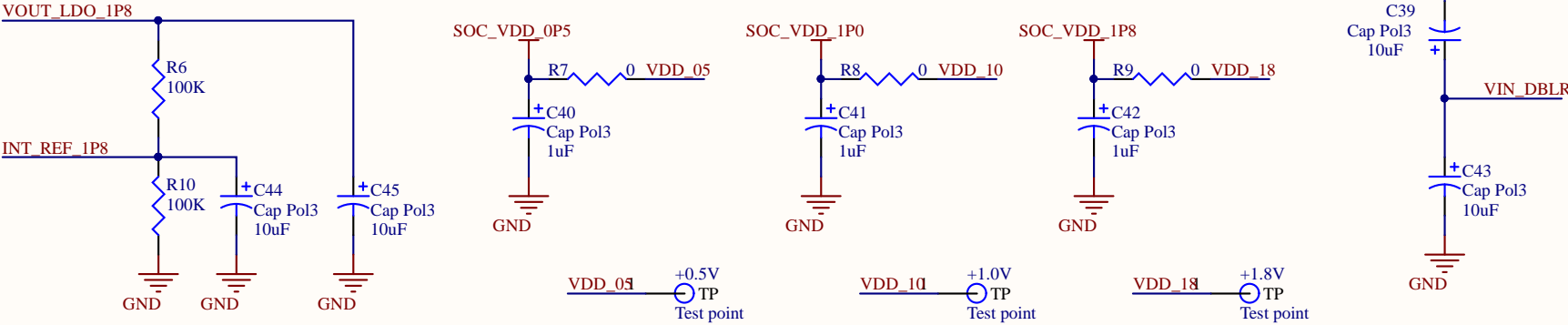
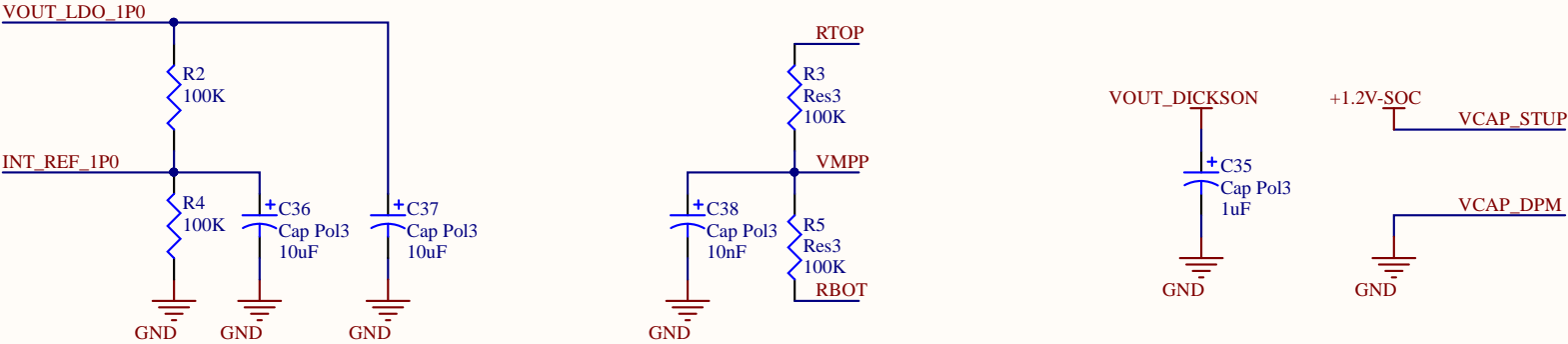


UMich Interface



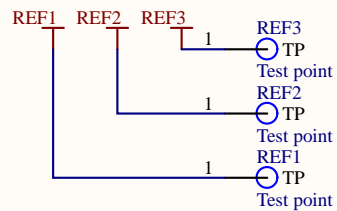
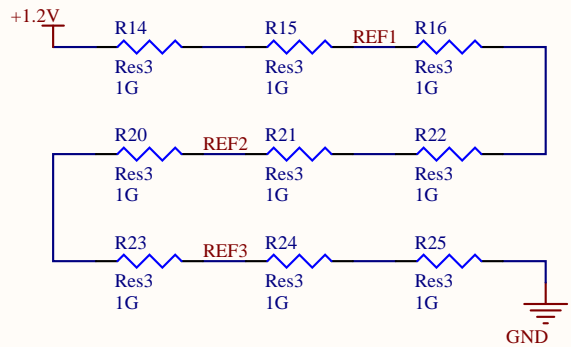
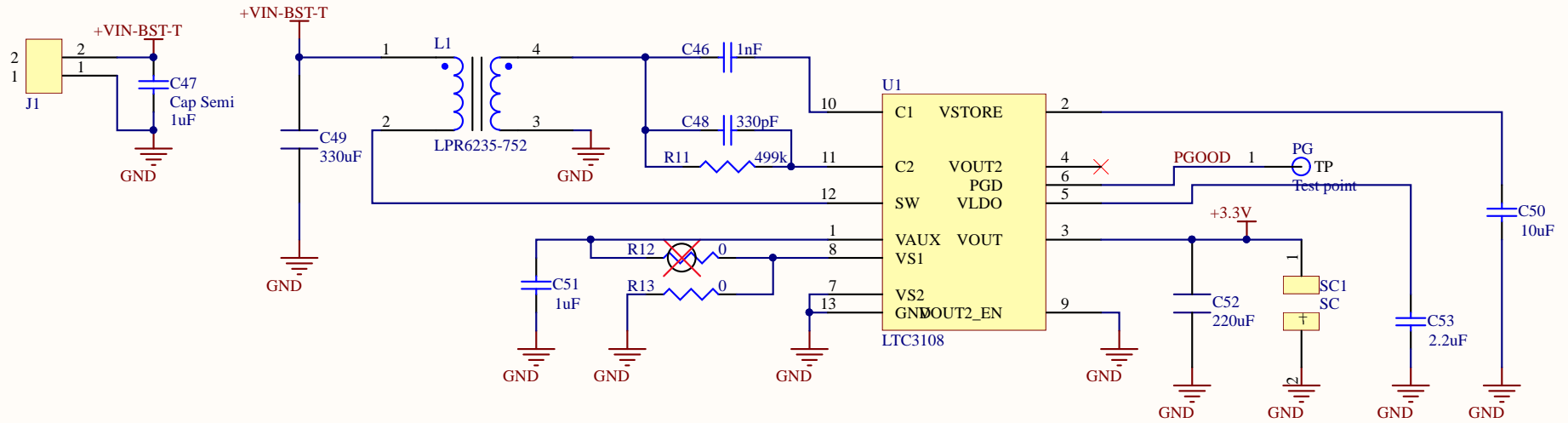
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PMU Setup

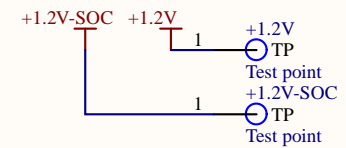
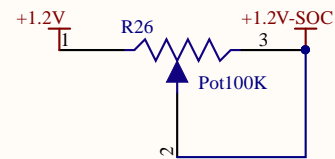
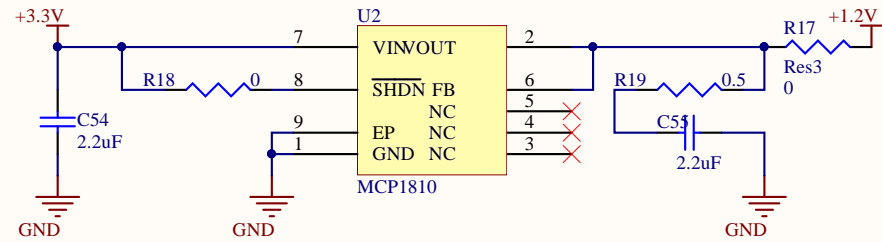


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Power Conversion and Regulation

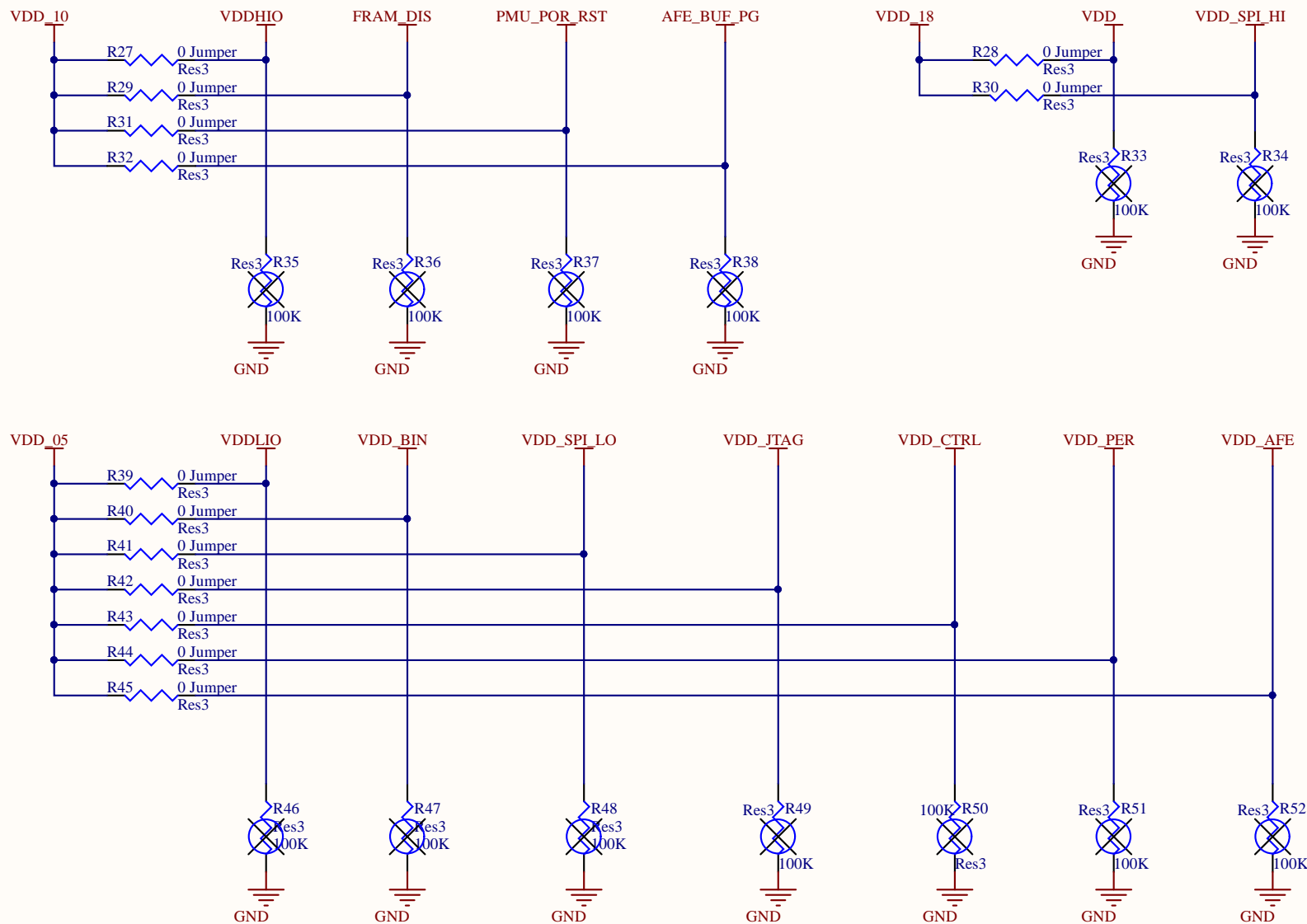


REF1 = 1.0V - 0.5V
REF2 = 0.5V - 0.4V
REF3 = 0.4V - 0.2V



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Power Selection



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UVA SoC 18

U3A

VOUT_DICKSON	1	VOUT_DICKSON		25	REF2
REF2	2	VREF_SW_CAP	EXT_REF_LDO_1P8	24	VDD_2T_UNTRIM
GND	3	VREF_0P5	VDD_2T_REF_UNTRIM	23	VMPP
VOUT_SW_CAP	4	VOUT_SW_CAP	VMPP	22	VREF_2T_UNTRIM
AFE_OUT	5	AFE_OUT	VREF_2T_REF_UNTRIM	21	
XO_CLK	6	XO_CLK	NC	20	
XTALB	7	XTALB	NC	19	
XTALA	8	XTALA	NC	18	VX_BOOST
VIN_BOOST	9	VIN_BOOST	VX_BOOST	17	VOUT_LDO_1P0
RTOP	10	RTOP	VOU_LDO_1P0	16	VOUT_LDO_1P8
RST_BOOST	11	RST_BOOST	VOU_LDO_1P8	15	INT_REF_1P0
GND	12	REF_SEL	INT_REF_1P0	14	INT_REF_1P8
RBOT	13	RBOT	INT_REF_1P8		

SoC18

U3B

REF3	26	EXT_REF_LDO_1P0		50	
VIN_DBLR	27	VIN_DBLR	FRAM_SPI_SCLK	49	
VCAP_DPM	28	VCAP_DPM	FRAM_SPI_MOSI	48	
VCAP_STUP	29	VCAP_STUP	NC	47	BLE_PWR_GATE
VCAP_DBLR	30	VCAP_DBLR	BLE_PWR_GATE	46	GND
VCAP_BOOST	31	VCAP_BOOST	BLE_FIFO_FULL	45	BLE_SPI_RST
VOUT_DBLR	32	VOUT_DBLR	BLE_SPI_RST	44	BLE_TX_RST
VCAP_SW_CAP	33	VCAP_SW_CAP	BLE_TX_RST	43	PMU_VDD_1P0
REF3	34	VBN	PMU_VDD_1P0	42	GND
REF1	35	VBP_BOOST	BLE_MISO	41	BLE_MOSI
FRAM_DIS	36	FRAM_DISABLE	BLE_MOSI	40	BLE_SCLK
GND	37	DPM_DEBUG_CTRL2	BLE_SCLK	39	GND
GND	38	DPM_DEBUG_CTRL0	DPM_DEBUG_CTRL0		

SoC18

U3C

GND	51	GND		75	JTAG_TDI
GND	52	GND	JTAG_TDI_PAD	74	PMU_POR_RST
GND	53	GND	PMU_POR_RST	73	VDD
VDD_BIN	54	VDDBIN	VDD	72	GPIO_0
CNTRL0	55	CHIP_CTRL_0	GPIO_0	71	GPIO_1
CNTRL1	56	CHIP_CTRL_1	GPIO_1	70	GPIO_2
	57	FRAM_RST	GPIO_2	69	GPIO_3
	58	FRAM_CLK_OUT	GPIO_3	68	GPIO_4
VDD_SPI_LO	59	VDD_SPI_LO	GPIO_4	67	GPIO_5
SPI_MISO	60	SPI_MISO	GPIO_5	66	GPIO_6
SPI_MOSI	61	SPI_MOSI	GPIO_6	65	GPIO_7
SPI_SCLK	62	SPI_SCLK	GPIO_7	64	VDD_SPI_HI
SPI_SS	63	SPI_SS_B	VDD_SPI_HI		

SoC18

U3D

JTAG_TCK	76	JTAG_TCK_PAD		100	AFE_VBIAS_P
JTAG_TMS	77	JTAG_TMS_PAD	AFE_VBIAS_P	99	VDDHIO
JTAG_TRSTN	78	JTAG_TRSTN_PAD	VDDHIO	98	VDDLIO
JTAG_TDO	79	JTAG_TDO_PAD	VDDLIO	97	VDD_CTRL
CLK	80	CHIP_CLK	VDD_CTRL	96	VDD_PER
RST	81	CHIP_RST	VDD_PERIPHERAL	95	SOC_VDD_0P5
AFE_BUF_PG	82	PAD_SRAM_DIN_TST	SOC_VDD_0P5	94	VDD_AFE
	83	COTS_VDD_1P8	VDD_AFE	93	LNA_N
	84	COTS_VDD_1P0	LNA_IN_N	92	LNA_P
	85	COTS_VDD_0P5	LNA_IN_P	91	SOC_VDD_1P0
VDD_JTAG	86	VDD_JTAG	SOC_VDD_1P0	90	SOC_VDD_1P8
POR_RST	87	POR_RST	SOC_VDD_1P8	89	POR_RST_1P8
POR_1P8	88	POR_1P8	POR_RST_1P8		

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