DEEC
DEPARTAMENTO DE ENGENHARIA ELETROTÉCNICA E DE COMPUTADORES
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Lab. Proj. 2

Computing Determinants

Scheduling and Resource Sharing

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Consider the problem of computing a set of determinants (Det_i) of a 2×2 matrix (M) whose values are obtained from the inputs A to F using the following algorithm:

```
for (i = 0; i < N; i++) {
    M11 = Ai * Bi ;
    M12 = Ai + Ei * Fi ;
    M21 = (Ci + Di) * Bi ;
    M22 = Ci + Di + (Ei * Fi)/4 ; // integer division
    Deti = M11 * M22 - M12 * M21 ;
}
```

1. **Data Flow Graph**
   Draw the data flow graph corresponding to one loop iteration of the algorithm.

2. **Priority List**
   Define a priority list using a critical path as metric.
   Assumes that the division operation by 4, requires no operator and takes no time (i.e., it is done when product value is written in the register). Therefore, should not be considered for the critical path metric.

3. **List Scheduling**
   Get a list scheduling using the priority list defined in 2. Consider that each operation requires a clock cycle and the only resources available (for arithmetic operations) are: 2 multipliers and 1 ALU (addition and subtraction).

4. **Circuit Design**
   Design a circuit to implement the algorithm to compute each Det_i, according to the constraints and schedule defined in 3. Choose the resource binding that provides the best performance (given the constraints indicated).

   Use an FSMD architecture and specify the datapath and control units in separated VHDL entities. For your project consider also the following design requirements/constraints:

   - The N value is fixed as $N = 16$. All the input values are integers of 16 bits in two's complement representation. All the computations should be done using the two's complements representations and all datapath buses can not exceed 32 bits.

- Each set of inputs values $(A_i, B_i, \cdots, F_i)$ are stored in the synchronous input memories with 16 bits output ports (using a RAMBs block memories). The output determinant (Det_i) will be store on consecutive positions in the synchronous output memory with one input port of 32 bits. See the VHDL examples of the memories **`memIN`** and **`memOUT`** given on the course web page.
- The circuit must have synchronous **`reset`** and **`done`** signals. The **`reset`** is active high and when become low the circuit should start the computation. The **`done`** signal should become high only after the last computed value of Det_i has been written in the output memory.
- The top circuit must have the following output signals: the **`done`** signal, write enable (**`we`**), the address bus (**`addr`**) and the data bus (**`dataOUT`**) of the output memory.
- All circuit registers must be positive edge-triggered and synchronous with an unique global clock signal (**`clk`**)

Draw the block diagram of the overall architecture of your circuit.
Also, draw a detailed block diagram of your datapath and indicate the number of registers and multiplexers required to implement it.
Describe your control FSM using a state diagram and indicate the total number of states.
Quantify the resource consumption of your circuit, in terms of the basic primitives of the FPGA technology.
Select the clock period most appropriate to execute the algorithm in your architecture.
Quantify the performance of your circuit and identify its latency.
Indicate which is the critical path of your circuit.
Justify by **a post-implementation timing simulation**.

Note: this project will be **demonstrated only by simulation**. Therefore, you also must **develop the appropriate testbench** to verify the correct operation of the circuit and evaluate its performance.

5. **Pipelining**
   Could you improve the circuit performance by pipelining the architecture? Do you need (or not) additional resources?
   Indicate the minimum number of multipliers, ALUs (adders or subtractors) needed to get the maximum throughput on result (Det_i), considering the clock period and schedule defined for circuit architecture designed in 4.
   Explicitly indicate the value of this maximum throughput.
   Justify you answer.
   Sketch a draft block diagram of the datapath of the pipelined architecture.

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