

AFE4950 Ultra-Small, Integrated AFE for Wearable Optical Heart-Rate Monitoring, SpO₂ and Electrical Bio-sensing

1 Features

- Supports simultaneous and synchronized acquisition of up to 24 PPG and a single-lead ECG signal.
- Flexible allocation of 8 LED, 4 PD in each phase
- ECG signal chain:
 - 1-lead ECG signal acquisition up to 2 kHz
 - RLD output to drive a third electrode
 - Input noise : 0.7 μ V-rms
 - Supports up to ± 0.65 V differential DC offset and +/-0.55 V common mode range
 - Programmable INA gain: 11, 21
 - High-pass filter with quick saturation recovery
 - Integrated 300 Hz anti-aliasing low pass filter
 - AC, DC lead-off detect: 2.9 nA to 92.5 nA
 - Low power continuous lead-on detection
- Impedance signal chain
 - Continuous low-power monitoring of impedance between 2 electrodes
 - 7 M Ω range
 - 300 Ω noise on 620 k Ω
- PPG Transmitter:
 - 8-Bit Programmable LED Current with range adjustable from 25 mA to 250 mA
 - Mode to fire two LEDs in parallel
 - Support of 8 LEDs in Common Anode configuration for SpO₂, Multi-Wavelength HRM
- PPG Receiver:
 - 2 parallel receivers (two sets of TIA/ filter)
 - Supports 4 Time-Multiplexed Photodiode Inputs to each Receiver
 - 8-bit Ambient Offset subtraction at each TIA input with 256 μ A range
 - 8-bit LED Offset Subtraction DAC with 64 μ A range
 - Automatic ambient cancellation and dynamic LED DC cancellation at TIA input
 - Ambient rejection close to 100 dB up to 10 Hz
 - Noise filtering with programmable bandwidth
 - Trans-impedance Gain: 3.7 k Ω to 1 M Ω
- Accurate, Continuous Heart-Rate Monitoring:
 - System SNR up to 109-dB at 16 μ A PD current
 - Low Current for Continuous Operation on a Wearable Device with a Typical Value: 15- μ A for an LED, 20- μ A for the Receiver
- External clock and internal oscillator modes
- Acquire data synchronized with system master clock
- FIFO with 256-sample Depth

- SPI, I²C interfaces: Selectable by pin
- 2.6-mm \times 2.5-mm DSBGA, 0.4-mm Pitch
- Supplies: Rx:1.7-1.9V (LDO Bypass); 1.9-3.6V (LDO Enabled), Tx:3-5.5V, IO:1.7-RX_SUP

2 Applications

- Optical Heart-Rate Monitoring (HRM) for Wearables, Hearables
- High performance ECG signal acquisition
- Synchronized PPG, ECG for BP estimation
- Heart-rate variability (HRV)
- Pulse oximetry (SpO₂) measurements

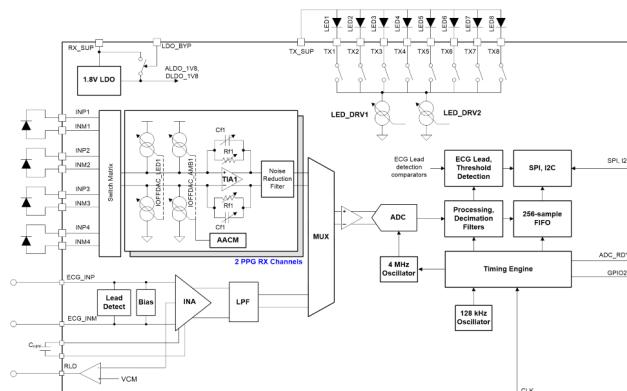
3 Description

The AFE4950 device is an analog front-end (AFE) for synchronized signal acquisition of PPG and ECG signals. The device can also be used for optical bio-sensing applications, such as heart-rate monitoring (HRM) and saturation of peripheral capillary oxygen (SpO₂). The ECG signal chain supports 2- and 3-electrode configurations and has an integrated Right leg drive (RLD) buffer. The ECG signal chain can also be used to do a continuous, low-power monitoring of the impedance between pair of electrodes.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
AFE4950	DSBGA (36)	2.60 mm \times 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2021) to Revision D (December 2022)	Page
• Deleted the text (5 LSBs) from the <i>Full MCU Control</i> summary in: <i>Input DC Cancellation</i> section	74
• Deleted the 8-bit and 5-bit <i>Control</i> details from <i>Full MCU Control</i> section	77
• Deleted the 5-bit <i>control</i> details from <i>Automatic Ambient Cancellation Using Analog AACM</i> section	79
• Deleted the 5-bit <i>control</i> details from <i>Automatic LED DC Cancellation</i> section	85

Changes from Revision B (January 2021) to Revision C (July 2021)	Page
• Changed the <i>Features</i> list AC, DC lead-off detect value From: 2.6-nA to 85-nA To: 2.9 nA to 92.5 nA	1
• Added the description of TX_SUP pin in <i>Pin Configuration and Functions</i> Table.....	5
• Changed the table note in <i>Recommended Operating Conditions</i> section.....	8
• Deleted the parameter <i>DC lead-off current</i>	10
• Deleted the parameter <i>AC lead-off current</i>	10
• Added the parameter <i>DC and AC lead off current</i>	10
• Changed the Table 7-1 in <i>Clocking modes</i> section.....	24
• Added note in <i>Internal Oscillator and External Clock Modes</i> section.....	27
• Changed table <i>Timing parameters associated with the signals of a phase in Signal Generation in PPG Phase Windows</i> section.....	55
• Changed table <i>Programming the amplitude of the Lead detect current sources in Active DC Lead Detect</i> section.....	113
• Changed the paragraph starting with <i>To support a wide range of electrode contact...</i> in <i>Active DC Lead Detect</i> section.....	113
• Changed the Table <i>Programming the amplitude of the Lead detect current sources in Active DC lead detect</i> section.....	113
• Added note in <i>AC Lead Detection</i> section.....	115
• Added a table note about the <i>Enabling method</i> attribute in table <i>Comparison of the lead detect modes</i> in <i>Comparison of Lead Detect Modes</i> section.....	118
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• Changed Selection of Interrupts Output on the ADC_RDY Pin Table and Selection of Input/ Output on GPIO2P Table in <i>Interrupt Modes</i> section.....	131
• Changed the paragraph starting with <i>The SPI is enabled by setting the...</i> in <i>Serial Programming Interface</i> section.....	135
• Added Bit CLKBUF_TRISTATE to CONTROL10 Register in <i>Page 0 Registers</i> section.....	142
• Added Bit AC_LEAD_DET_CLK_PHASE to CONTROL19 Register in <i>Page 0 Registers</i> section.....	142
• Added register address AC_LEAD_DEMOD_CFG in <i>Page 0 Registers</i> section.....	142
• Changed reset value and added table note for DESIGN_ID bit in <i>Register 28h (address = 28h)</i> table.....	166
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• Changed paragraph starting with <i>When used in environments where the electrodes....</i> in <i>Detailed Design Procedure - ECG</i> section.....	235

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• Changed From: <i>MASK_AFE_FREEZE_INT</i> To: 1 in <i>Page 0 Registers</i> section.....	142
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• Changed Bits D21, D20, D[15-11] of Register Address <i>INTR_SOFT</i> , From: 0 To: x in <i>Page 0 Registers</i> section.....	142
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• Changed the data sheet From: <i>Advanced Information</i> To: <i>Production</i> data.....	1

5 Pin Configuration and Functions

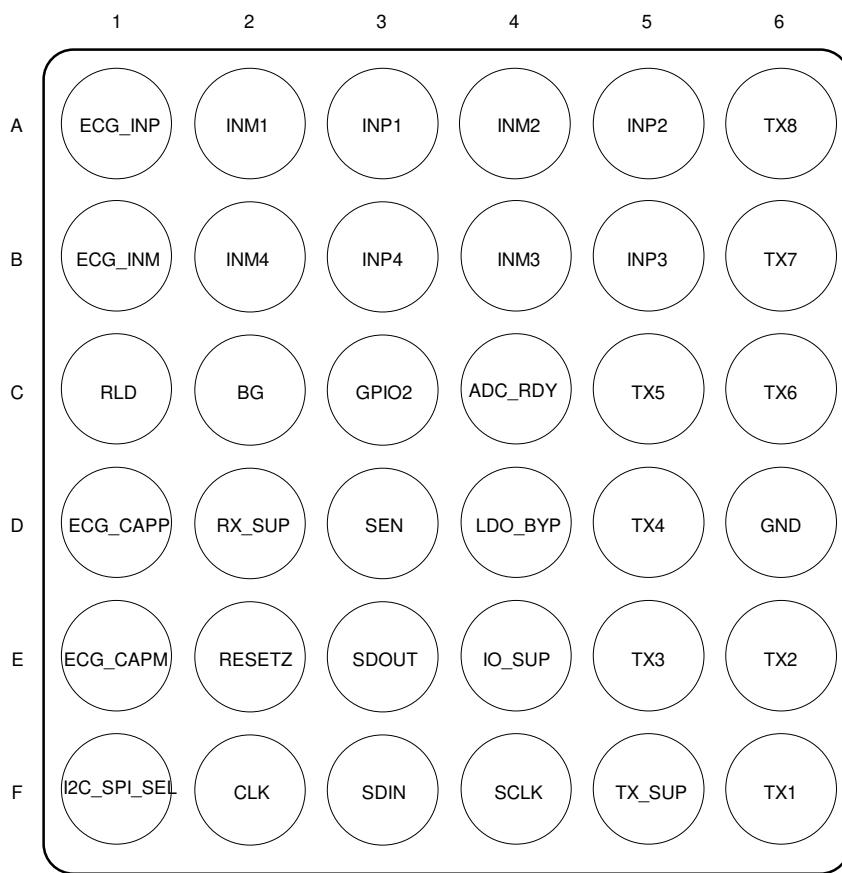


Figure 5-1. YBG package, 36-Ball (DSBGA), Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADC_RDY	C4	Digital	Programmable interrupt (output). Levels = 0 V to IO_SUP.
BG	C2	Analog	Band-gap voltage output. Use a 1- μ F decoupling capacitor. (1)
CLK	F2	Digital	Clock input pin. Levels = 0 V to IO_SUP.
GND	D6	Ground	Ground. Level = 0 V.
GPIO2	C3	Digital	Programmable I/O pin
INM1	A2	Analog	PPG negative input 1, Connect to photodiode anode
INP1	A3	Analog	PPG positive input 1, Connect to photodiode cathode
INM2	A4	Analog	PPG negative input 2, Connect to photodiode anode
INP2	A5	Analog	PPG positive input 2, Connect to photodiode cathode
INM3	B4	Analog	PPG negative input 3, Connect to photodiode anode
INP3	B5	Analog	PPG positive input 3, Connect to photodiode cathode
INM4	B2	Analog	PPG negative input 4, Connect to photodiode anode
INP4	B3	Analog	PPG positive input 4, Connect to photodiode cathode
ECG_INM	B1	Analog	ECG negative input
ECG_INP	A1	Analog	ECG positive input
ECG_CAPM	E1	Analog	ECG high pass filter cap. Connect capacitor between ECG_CAPP and ECG_CAPM
ECG_CAPP	D1	Analog	

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
I2C_SPI_SEL	F1	Digital	This pin enables selection between the I ² C and SPI interfaces. 0 = SPI interface, 1 = I ² C interface. Levels = 0 V to RX_SUP. Do not leave floating.
IO_SUP	E4	Supply	This pin provides a separate supply for the digital I/O. Levels = 1.7 V to RX_SUP.
LDO_BYP	D4	Digital	Digital control pin to bypass internal LDOs. LDO_BYP = 0V : Operate with internal LDO enabled. LDO_BYP = RX_SUP : Operate with internal LDO bypassed.
RESETZ	E2	Digital	This pin is either RESETZ or PWDN. Functionality is based on the (active low) duration of RESETZ. A 25-μs to 50-μs duration resets the device. A > 200-μs duration causes the device to enter the hardware powerdown (PWDN) mode. Use hardware powerdown only in LDO Enable mode. Do not use in LDO Bypass mode. Levels = 0 V to IO_SUP. Do not leave floating.
RLD	C1	Analog	Output common-mode bias voltage for ECG input pins. Connect a 100-pF decoupling capacitor to ground.
RX_SUP	D2	Supply	Receiver supply; 1-μF decapacitor to GND. With internal LDO enabled: 1.9 V to 3.6 V With internal LDO bypassed: 1.7 V to 1.9 V
SCLK	F4	Digital	In I ² C mode, this pin is an I ² C clock pin. An external pullup resistor (for example, 10 kΩ) to IO_SUP is required. In SPI mode, this pin is a serial clock input. Levels = 0 V to IO_SUP.
SDIN	F3	Digital	In I ² C mode, this pin is an I ² C data pin. An external pullup resistor (for example, 10 kΩ) to IO_SUP is required. In SPI mode, this pin is a serial data input. Levels = 0 V to IO_SUP.
SEN	D3	Digital	In I ² C mode, this pin inverts the LSB of the I ² C slave address. In SPI mode, this pin is the chip-select pin for the SPI (active low). Levels = 0 V to IO_SUP.
SDOUT	E3	Digital	In I ² C mode, this pin is a programmable interrupt (output). In SPI mode, this pin is a serial data output for the SPI. Levels = 0 V to IO_SUP.
TX1	F6	Analog	Transmit output 1, connect to LED1
TX2	E6	Analog	Transmit output 2, connect to LED2
TX3	E5	Analog	Transmit output 3, connect to LED3
TX4	D5	Analog	Transmit output 4, connect to LED4
TX5	C5	Analog	Transmit output 5, connect to LED5
TX6	C6	Analog	Transmit output 6, connect to LED6
TX7	B6	Analog	Transmit output 7, connect to LED7
TX8	A6	Analog	Transmit output 8, connect to LED8
TX_SUP	F5	Analog	Transmitter supply; 1-μF to 10-μF decap to GND. Levels = 3.0 V to 5.5 V

- (1) Using a 1-μF capacitor on BG improves the AFE noise but results in a higher recovery time from a software and hardware power-down.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT	
Supply voltage range	RX_SUP to GND LDO bypassed	-0.3	2.1	V	
	RX_SUP to GND LDO enabled ⁽³⁾	-0.3	4		
	IO_SUP to GND	-0.3	Min (4, [RX_SUP + 0.3])		
	TX_SUP to GND	-0.3	6		
Voltage applied to digital inputs		Max [-0.3, (GND - 0.3)]	Min (4.0, [IO_SUP + 0.3])	V	
Duty cycle (cumulative): sum of all LED phase durations as function of total period	25-mA LED current	22.4%			
	50-mA LED current	11.2%			
	100-mA LED current	5.6%			
	200-mA LED current	2.8%			
	250-mA LED current	2.2%			
Storage temperature, T _{stg}		-60	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If subjected to additional processing steps (for example during PCB assembly or product manufacturing), avoid exposure of the device to UV radiation and exposure to high temperatures (350°C and higher).
- (3) Voltages higher than 2.1V can be applied on RX_SUP only when LDO_BYP pin is at '0'.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	ECG_INP, ECG_INM, RLD pins	V
			8000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	All other pins	
			500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
RX_SUP	Receiver supply	1.7	1.9	V
	LDO bypass mode	1.9	Min (3.6, TX_SUP)	V
IO_SUP	I/O supply	1.7	Min(3.6,(RX_SUP+0.2))	V
TX_SUP	Transmitter supply	3 ⁽¹⁾	5.5	V
	Digital inputs (Except LDO_BYP, I2C_SPI_SEL)	0	IO_SUP	V
Digital input LDO_BYP, I2C_SPI_SEL		0	RX_SUP	V
PPG Analog inputs		0	Min (1.8, RX_SUP)	V
ECG Analog Inputs		0	RX_SUP	V
Recommended operating temperature		-20	85	°C

(1) For additional considerations to determine the minimum TX_SUP voltage, see [Table 7-30](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	WCSP (DSBGA)	UNIT
	36 BALLS	
R _{θJA}	Junction-to-ambient thermal resistance	55.0
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.2
R _{θJB}	Junction-to-board thermal resistance	12.0
Ψ _{JT}	Junction-to-top characterization parameter	0.1
Ψ _{JB}	Junction-to-board characterization parameter	11.9
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A

(1) For more information about traditional and new thermal metrics, refer to the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics - PPG Signal Chain

$T_A = 25^\circ\text{C}$; $\text{TX_SUP} = 5 \text{ V}$, LDO Bypass mode ($\text{RX_SUP} = \text{IO_SUP} = 1.8 \text{ V}$), Mixed clock mode with 32.768 kHz input clock, $R_f = 250 \text{ k}\Omega$, $C_f = 20 \text{ pF}$, 25-Hz PRF, LED ON width (and SAMP width) of $12 \times t_{TE}$ (approximately $94 \mu\text{s}$), Filter pre-charge width of $4 \times t_{TE}$ (approximately $31 \mu\text{s}$), Filter pre-charge bandwidth of 25 kHz , Filter fine settling bandwidth of 5 kHz , NUMAV = 2, $1 \mu\text{F}$ decap on BG pin, $C_{IN} = 50 \text{ pF}$ (capacitor across input pins to model the zero bias differential capacitance of the PD)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pulse Repetition Frequency					
f_{PRF} Pulse repetition frequency		5		1000 ⁽¹⁾	SPS
Receiver					
Ambient Offset DAC current range	1x range (default) 2x range 4x range 8x range 16x range	-15.9375 to +15.9375 -31.875 to +31.875 -63.75 to +63.75 -127.5 to +127.5 -255 to +255			μA
Ambient Offset DAC current resolution	All ranges (not including polarity bit)		8		bit
Ambient Offset DAC current step	Default (1X) range		0.0625		μA
Ambient Offset DAC accuracy	1x range, full scale current		± 25		%
LED Offset DAC current range	1X range (default) 2X range	-31.875 to +31.875 -63.75 to +63.75			μA
LED Offset DAC current resolution	Both ranges (not including polarity bit)		8		bit
LED Offset DAC current step	1X range		0.125		μA
LED Offset DAC accuracy	1x range, full scale current		± 25		%
TIA gain setting			3.7 k to 1 M		Ω
TIA gain accuracy	Gain setting of 500 K		± 10		%
CF setting			2.5 to 25		pF
Switched RC filter bandwidth			2.5 to 77.5		kHz
ADC averages		1		16	
Detector capacitance	Differential capacitance between the INP*, INM* pins introduced by the connection to the detector (including routing capacitances)	10		200	pF
Transmitter					
LED current range per driver ⁽²⁾	0.5x mode 1x mode (default) 2x mode 2.5x mode	0 to 25 ⁽²⁾ 0 to 50 ⁽²⁾ 0 to 100 ⁽²⁾ 0 to 125 ⁽²⁾			mA
LED current resolution			8		Bits
LED current accuracy	1x range, full scale current		± 20		%
Performance					
Input referred current noise	Receiver only ⁽⁴⁾ Transmitter and Receiver ⁽⁵⁾	35			pArms ⁽³⁾
70					
Current Consumption in PPG-only mode					
RX_SUP current ⁽⁷⁾	Normal operation ⁽⁶⁾ Software power-down mode ^{(7) (9)}	21			μA
IO_SUP current	Normal operation ⁽⁶⁾ Software power-down mode ^{(7) (9)}	1			μA
TX_SUP current	Normal operation ^{(6) (8)} Software power-down mode ^{(7) (8)}	1.5			μA
1					

- (1) Using a high number of phases can impose further constraints on the maximum PRF setting.
- (2) By programming current from both drivers to flow into a single LED, the current through an LED can be set to twice this number.
- (3) RMS noise over Nyquist bandwidth calculated from standard deviation of output code and converted to input referred current noise.
- (4) With open receiver inputs ($R_f = 500 \text{ k}\Omega$, $C_f = 10 \text{ pF}$)
- (5) 50 mA LED current is electrically looped back to the receiver inputs through an external op-amp to create a 0.5-V DC at the receiver output. ($R_f = 500 \text{ k}\Omega$, $C_f = 10 \text{ pF}$)
- (6) Operation in external clock mode at 25 Hz PRF with the device in an active state for 4% of the time during a PRF cycle.
- (7) This indicates the external clock switched off.
- (8) The LED currents are set to 0 mA.
- (9) In LDO bypass mode, the PDN_BG_IN_DEEP_SLEEP bit set to 1 along with PDNAFE. Also, to minimize the power consumption, set the acquisition mode to PPG mode before going into Software power-down mode.

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6.6 Electrical Characteristics - ECG Signal Chain

$T_A = 25^\circ\text{C}$; TX_SUP = 5 V, RX_SUP = 1.8V (LDO bypass mode), IO_SUP = 1.8 V, Synchronous mixed clock mode with 32.768 kHz input clock ECG: 1-kHz sampling rate, INA gain of 21.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PRF_ECG PRF in ECG-only mode (no PPG phases) ⁽¹⁾			2000		SPS
ECG PERFORMANCE					
INA gain	Gain = 11		11.2		
	Gain = 21		21.4		
INA gain error	Across units, over a ± 300 mV offset range		± 5		%
Differential DC Offset	2.8 V < RX_SUP < 3.6 V		± 0.65		V
	1.7 V < RX_SUP < 1.9 V		± 0.45		V
Common Mode Range	2.8 V < RX_SUP < 3.6 V		$V_{CM} \pm 0.55$		V
	1.7 V < RX_SUP < 1.9 V		$V_{CM} \pm 0.1$		V
Differential AC Signal	Gain = 21		35		mV
	Gain = 11		65		mV
DC Input impedance	Differential between ECG_INP and ECG_INM		10		G Ω
AC Input impedance	Estimated with a 10-mVpp, 60-Hz sine-wave AFE through a series 620 k Ω 4.7 nF		2		G Ω
Differential input capacitance	between ECG_INP and ECG_INM		2		pF
Common-mode input capacitance	from each ECG input pin to ground		4		pF
Noise ⁽²⁾	PRF_ECG = 1 kHz, lead-off detect disabled ⁽³⁾		0.7		μVRms
	PRF_ECG = 1 kHz, lead-off detect enabled with 12.5-nA current, 51 k Ω 47 nF ⁽³⁾		0.8		
CMRR - Common-mode rejection ratio ⁽²⁾	3-electrode configuration, 51 k Ω 47 nF balanced electrode-contact impedance		130		dB
	3-electrode configuration, Unbalanced contact impedance, 51 k Ω 47 nF on only 1 electrode		120		
	2-electrode configuration, 51 k Ω 47 nF balanced electrode-contact impedance		95		
	2-electrode configuration, Unbalanced contact impedance, 51 k Ω 47 nF on only 1 electrode		80		
RX_SUP current in ECG-only mode	ECG sampling rate = 1 kHz		310		μA
RLD OUTPUT					
Output voltage ⁽⁴⁾	2.6 V < RX_SUP < 3.6 V		1.4		V
	2.1 V < RX_SUP < 2.6 V		1.2		
	1.7 V < RX_SUP < 2.1 V		0.9		
Output impedance			25		k Ω
LEAD BIASING FOR LEAD-ON DETECTION AND LEAD IMPEDANCE MEASUREMENT					
Lead Bias Impedance ⁽⁵⁾	2-electrode configuration		12.5M – 200M		Ω
Lead impedance detection range			7		M Ω
Lead impedance detection noise	620 k Ω impedance		300		Ω
LOW PASS FILTER					
3-dB bandwidth	3 dB roll-off		300 ⁽⁶⁾		Hz
HIGH PASS FILTER					
High-pass corner frequency	$C_{HPF} = 10 \mu\text{F}$		0.4 ⁽⁷⁾		Hz
Saturation recovery time			100		ms
ECG LEAD OFF					
DC lead-off current	Programmable		2.6 – 85		nA
DC and AC lead off current	Lowest setting		2.9		nA
	Highest setting		92.5 ⁽⁸⁾		nA
AC lead-off frequency			4		kHz
Lead-off current accuracy	85 nA current setting		± 30		%

(1) PRF_ECG, the effective ECG sampling rate, is calculated as (PRF setting) \times (Number of active ECG time slots per PRF cycle).

(2) 50 Hz common mode tone.

(3) Measured by shorting ECG_INP and ECG_INM to RLD.

(4) Program the indicated output voltage for each supply range using the PROG_VCM_RLD register control.

(5) Used to bias ECG input pins when RLD electrode is not available, or when ECG electrodes are capacitively coupled to input pins.

(6) LPF bandwidth can vary from unit to unit up to $\pm 20\%$.

(7) Can vary from the nominal value from $\pm 20\%$ variation in the internal resistor. There can be additional variations from the tolerance and voltage derating of C_{HPF} . With all these variations, it may be required to add an extra capacitor (For example 4.7 μF) in parallel with 10 μF to keep the HPF corner below 0.5 Hz.

(8) Can vary by $\pm 25\%$ across units.

6.7 Electrical Characteristics - Clocking and Interface

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, LDO Bypass mode (with RX_SUP = IO_SUP = 1.8 V), Mixed clock mode with 32.768 kHz input clock

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Oscillator Mode					
Frequency of internal oscillator	Internal oscillator mode		128		kHz
Accuracy	Room temperature		$\pm 1\%$		
	With calibration using RTC clock		$\pm 0.2\%$		
Frequency drift with temperature	Full temperature range		$\pm 1\%$		
Jitter (RMS)			12		ns
Clock Input					
Input clock high level			IO_SUP		V
Input clock low level			0		V
Input capacitance of CLK pin	Capacitance to ground		< 4		pF
External Clock Mode					
Frequency on CLK pin ⁽¹⁾	PPG acquisition mode	31.2	128	524.8	kHz
	ECG and Mixed acquisition modes			128	
Duty cycle on CLK pin			50%		
Single-shot Clocking Mode					
Periodicity of pulse train on CLK pin			f_{PRF}		Hz
High-time of pulse			30–100		μs
Mixed Clock Mode					
Frequency on CLK pin		31.2	128	524.8	kHz
Duty cycle on CLK pin			50		%
Synchronous Mixed Clock Mode					
Frequency on CLK pin			32.768		kHz
Duty cycle on CLK pin			50		%
FIFO					
FIFO depth			256		samples
SPI Interface					
Maximum serial clock speed			8		MHz
I²C Interface					
Maximum data rate			400		kHz
I ² C slave address	SEN = 0		5B		Hex
	SEN = 1		5A		Hex
Digital Inputs					
V_{IH}	High-level input voltage	0.9 \times IO_SUP	IO_SUP		V
V_{IL}	Low-level input voltage		0	0.1 \times IO_SUP	V
Digital Outputs					
V_{OH}	High-level output voltage		IO_SUP		V
V_{OL}	Low-level output voltage		0		V

(1) The clock frequency should be kept between the ranges mentioned in [Table 7-2](#) and [Table 7-3](#)

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6.8 Timing Requirements: Interrupts

		MIN	NOM	MAX	UNIT
$t_{ADC_RDY_RISE}$	ADC_RDY rise time (10% to 90%) with a 15-pF capacitive load to ground ⁽¹⁾		12		ns
$t_{ADC_RDY_FALL}$	ADC_RDY fall time (90% to 10%) with a 15-pF capacitive load to ground ⁽¹⁾		12		ns

(1) The same timing applies to the interrupts on other output pins.

6.9 Timing Requirements: I²C Interface

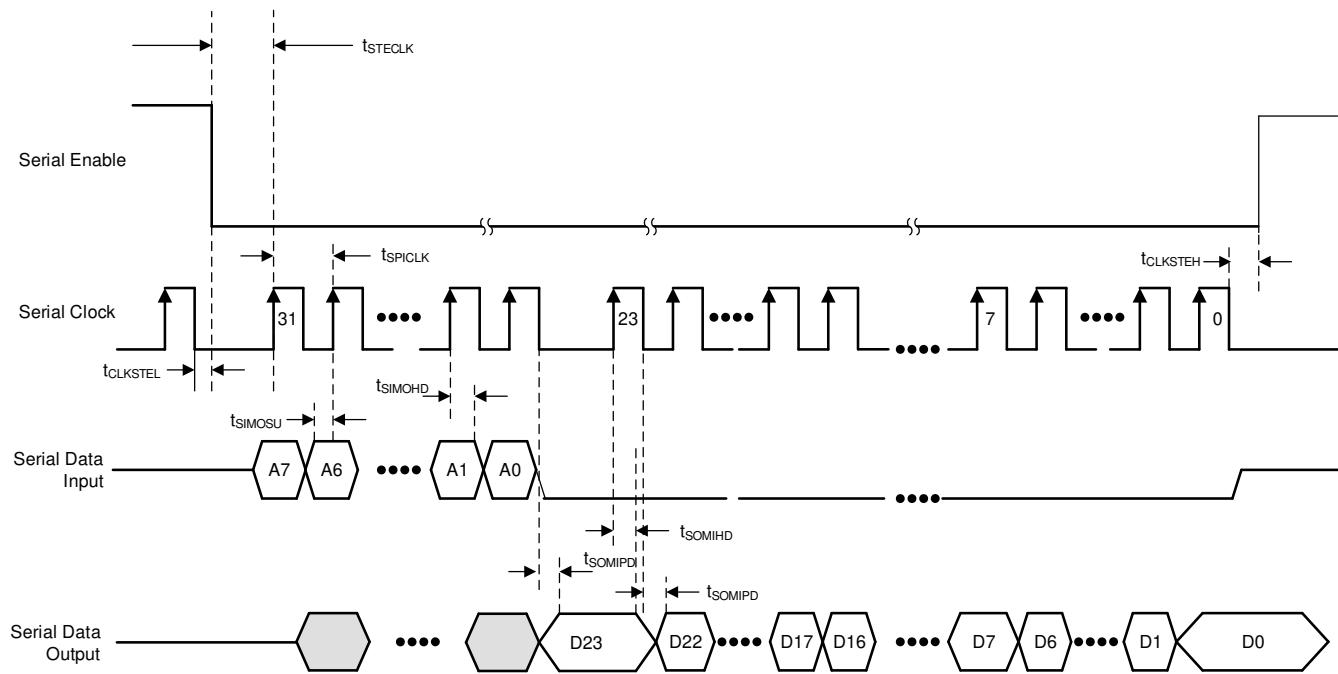
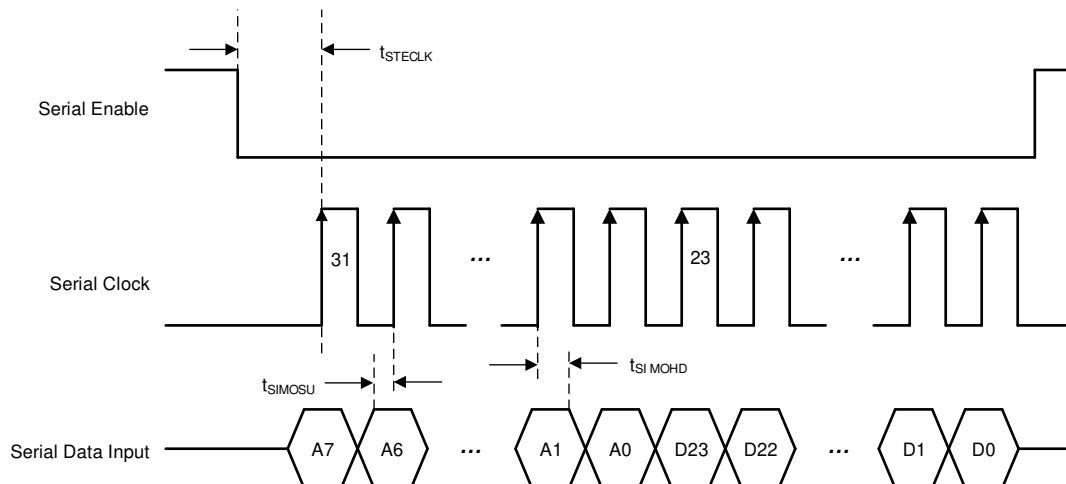
		MIN	NOM	MAX	UNIT
$t_{I^2C_RISE}^{(1)}$	I ² C data rise time with a 10-kΩ pullup resistor with a 20-pF load from I ² C data to GND		1200		ns
$t_{I^2C_RISE}$	I ² C data fall time (when the data line is pulled down by the AFE) with a 20-pF load from I ² C data to GND		28		ns

(1) Maximum achievable speed of the I²C interface could be limited by this parameter if the load on the I²C lines are high.

6.10 Timing Requirements: SPI Interface

see note ⁽¹⁾		MIN	NOM	MAX	UNIT
t_{SPICLK}	Serial shift clock period	125			ns
t_{STECLK}	Serial data enable low to serial clock rising edge, setup time	15			ns
$t_{CLKSTEH,L}$	Serial clock transition to serial data enable high or low	15			ns
t_{SIMOSU}	Serial data input to serial clock rising edge, setup time	15			ns
t_{SIMOHD}	Valid serial data input after SCLK rising edge, hold time	15			ns
t_{SOMIPD}	Serial clock falling edge to valid serial data output			15	ns
t_{SOMIHD}	Serial clock rising edge to invalid serial data output		0.5 × t_{SPICLK}		ns

(1) The values in this table refer to the timings of the logic signals that are internal to the AFE. Based on the external delays and the rise and fall times of these signals, additional timing margins may need to be accounted for.

**Figure 6-1. Serial Interface Timing Diagram, Read Operation****Figure 6-2. Serial Interface Timing Diagram, Write Operation**

6.11 Typical Characteristics

6.11.1 Typical Characteristics - PPG Signal Chain

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, LDO Bypass mode (with RX_SUP = IO_SUP = 1.8 V), Mixed clock mode with 32.768 kHz input clock, TIA $R_f = 250 \text{ k}\Omega$, TIA $C_f = 20 \text{ pF}$, 25-Hz PRF, LED ON width (and SAMP width) of $12 \times t_{TE}$ (approximately 94 μs), Filter pre-charge width of $4 \times t_{TE}$ (approximately 31 μs), Filter pre-charge bandwidth of 25 kHz, Filter fine settling bandwidth of 5 kHz, NUMAV = 2 (2 ADC averages), 1 μF decap on the BG pin, $C_{IN} = 50 \text{ pF}$ (capacitor across the input pins to model the zero bias differential capacitance of the PD)

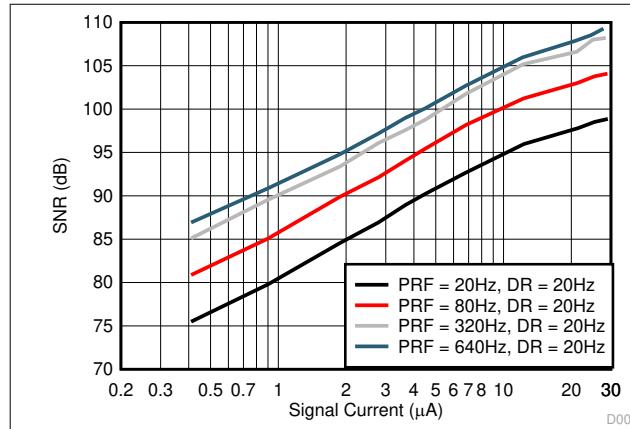


Figure 6-3. Full-System SNR in dB Measured over a 0.5-10 Hz Bandwidth vs. Input Current Level Across PRF

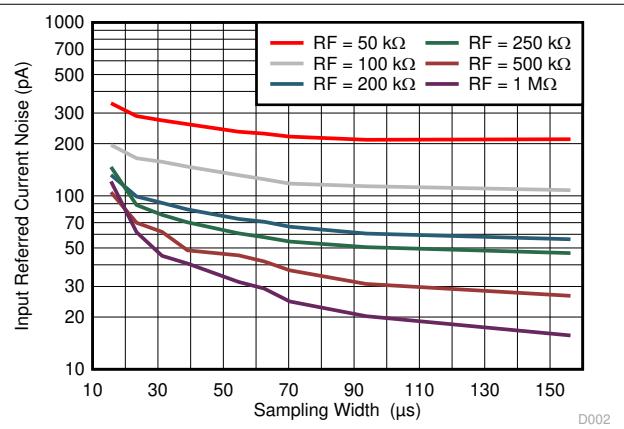


Figure 6-4. Input Referred Current Noise of the Receiver vs. SAMP Width Across RF Settings

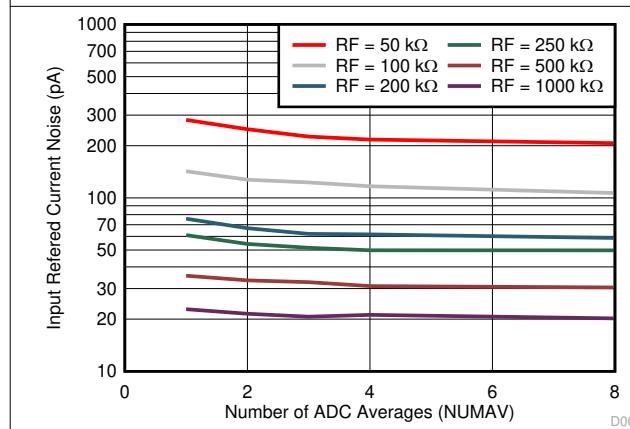


Figure 6-5. Input Referred Current Noise in pArms vs. Number of ADC Averages Across RF Settings

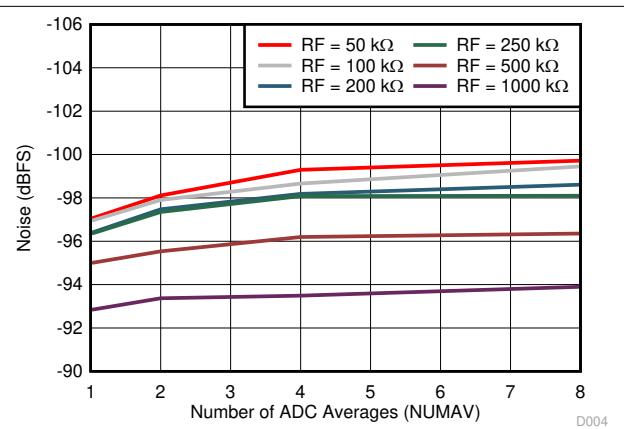


Figure 6-6. SNR in dBFS vs. Number of ADC Averages Across RF Settings

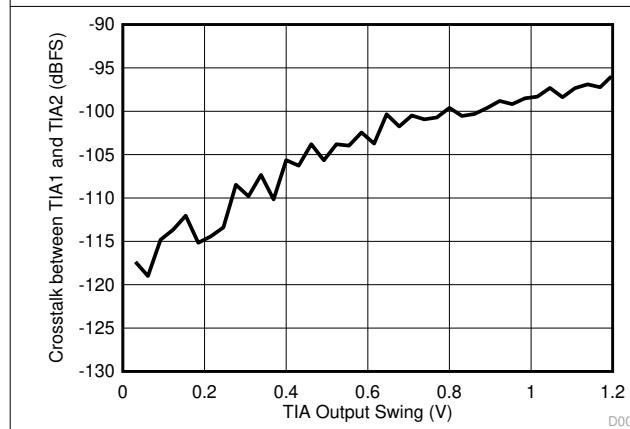


Figure 6-7. Crosstalk in Dual Receive Phase from TIA1 to TIA2 Across Output Swing of TIA1

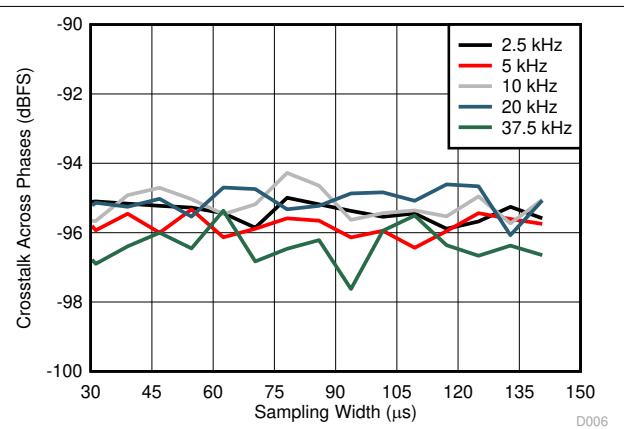


Figure 6-8. Crosstalk Between Neighboring Phases vs. SAMP Width Across Different Filter Bandwidth Settings for a Non-Staggered Timing (STAGGER_LED=0)

6.11.1 Typical Characteristics - PPG Signal Chain (continued)

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, LDO Bypass mode (with RX_SUP = IO_SUP = 1.8 V), Mixed clock mode with 32.768 kHz input clock, TIA $R_f = 250 \text{ k}\Omega$, TIA $C_f = 20 \text{ pF}$, 25-Hz PRF, LED ON width (and SAMP width) of $12 \times t_{TE}$ (approximately 94 μs), Filter pre-charge width of $4 \times t_{TE}$ (approximately 31 μs), Filter pre-charge bandwidth of 25 kHz, Filter fine settling bandwidth of 5 kHz, NUMAV = 2 (2 ADC averages), 1 μF decap on the BG pin, $C_{IN} = 50 \text{ pF}$ (capacitor across the input pins to model the zero bias differential capacitance of the PD)

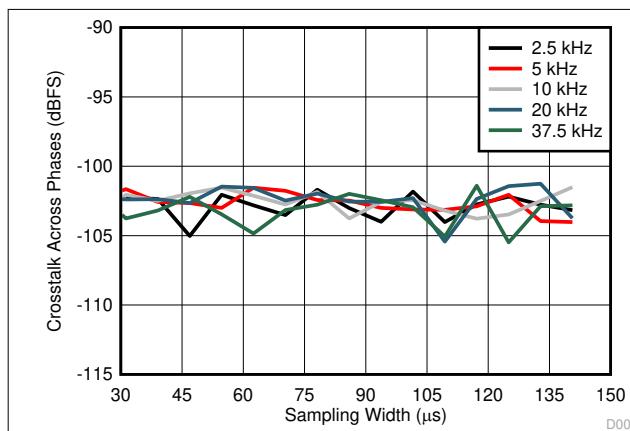


Figure 6-9. Crosstalk Between Neighboring Phases vs. SAMP Width Across Different Filter Bandwidth Settings for a Staggered Timing (STAGGER_LED=1)

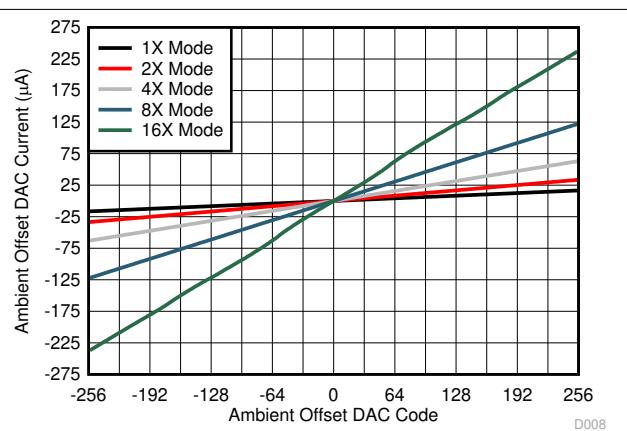


Figure 6-10. Ambient Offset DAC Current vs. Offset DAC Code Across Different Full-Scale Modes

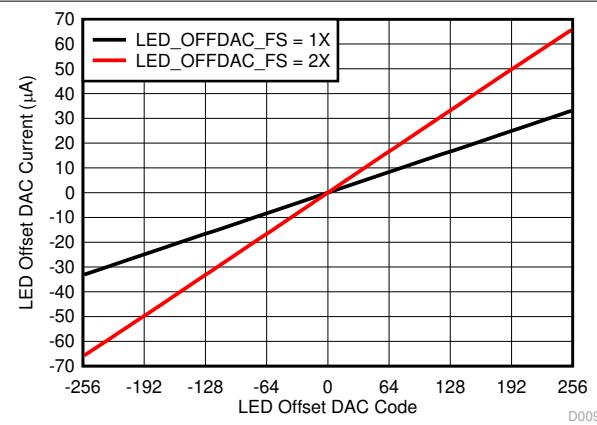


Figure 6-11. LED Offset DAC Current vs. Offset DAC Code

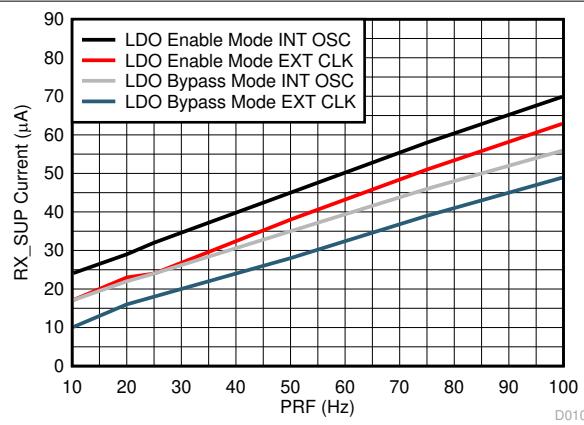


Figure 6-12. Average Current in RX_SUP vs. PRF Across LDO and Clocking Options When in PPG Mode

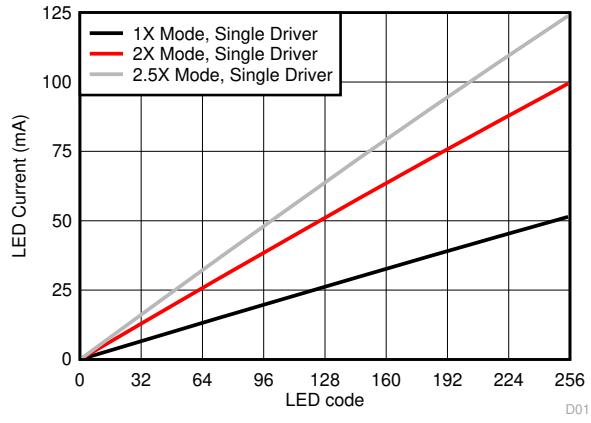


Figure 6-13. LED Current vs. LED Code Across Modes for a Single Driver

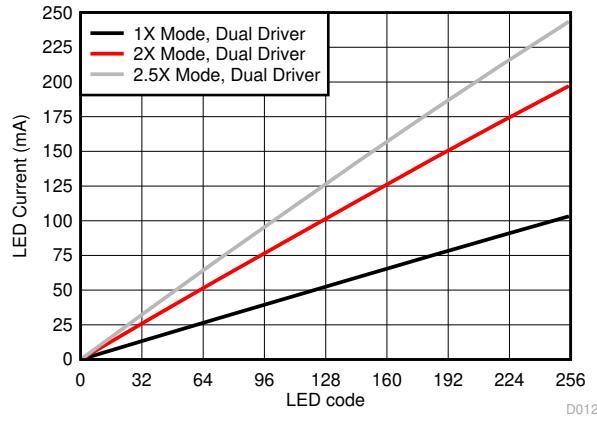


Figure 6-14. LED Current vs. LED Code Across Modes for a Dual Driver

6.11.1 Typical Characteristics - PPG Signal Chain (continued)

Typical specifications are at $T_A = 25^\circ\text{C}$; $\text{TX_SUP} = 5\text{ V}$, LDO Bypass mode (with $\text{RX_SUP} = \text{IO_SUP} = 1.8\text{ V}$), Mixed clock mode with 32.768 kHz input clock, $\text{TIA } R_f = 250\text{ k}\Omega$, $\text{TIA } C_f = 20\text{ pF}$, 25-Hz PRF, LED ON width (and SAMP width) of $12 \times t_{TE}$ (approximately 94 μs), Filter pre-charge width of $4 \times t_{TE}$ (approximately 31 μs), Filter pre-charge bandwidth of 25 kHz, Filter fine settling bandwidth of 5 kHz, NUMAV = 2 (2 ADC averages), 1 μF decap on the BG pin, $C_{IN} = 50\text{ pF}$ (capacitor across the input pins to model the zero bias differential capacitance of the PD)

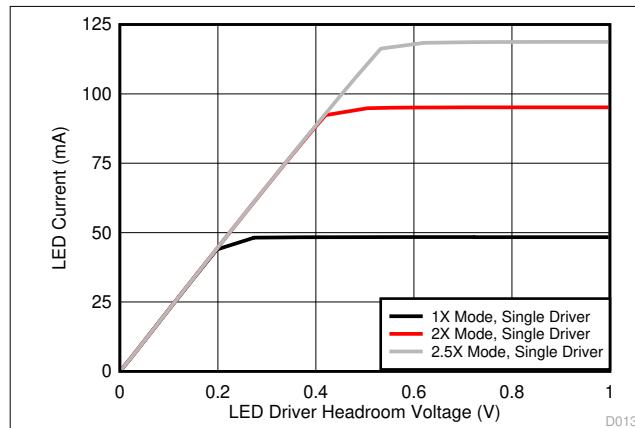


Figure 6-15. LED Driver Current vs. LED Driver Headroom Voltage for Single Driver Operation

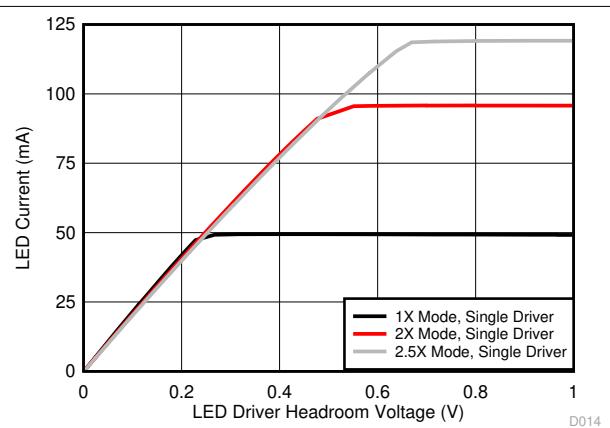


Figure 6-16. LED Driver Current vs. LED Driver Headroom Voltage for Single Driver Operation

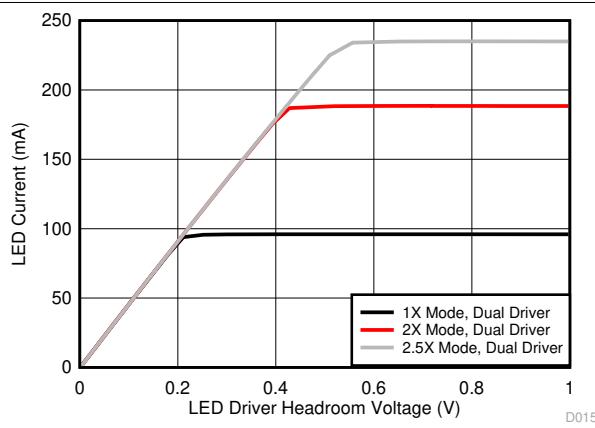


Figure 6-17. LED Driver Current vs. LED Driver Headroom Voltage for Dual Driver Operation

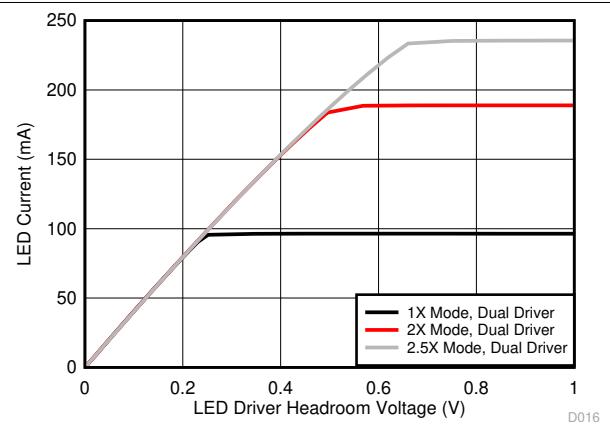


Figure 6-18. LED Driver Current vs. LED Driver Headroom Voltage for Dual Driver Operation

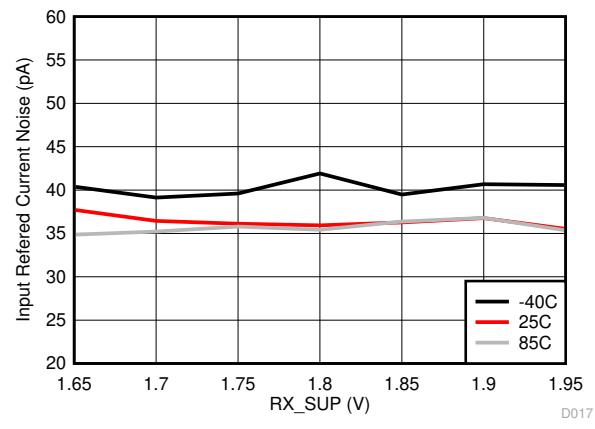


Figure 6-19. Input Referred Noise Current in pArms vs. RX_SUP Voltage Across Operating Temperature with Internal LDO Bypassed

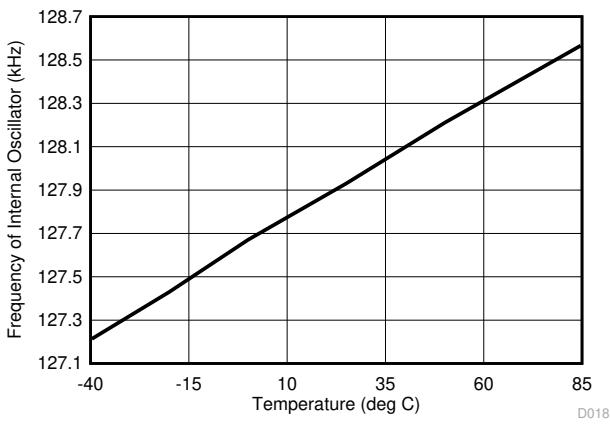


Figure 6-20. Frequency of Internal Oscillator vs. Temperature on a Sample Unit

6.11.1 Typical Characteristics - PPG Signal Chain (continued)

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, LDO Bypass mode (with RX_SUP = IO_SUP = 1.8 V), Mixed clock mode with 32.768 kHz input clock, TIA $R_f = 250 \text{ k}\Omega$, TIA $C_f = 20 \text{ pF}$, 25-Hz PRF, LED ON width (and SAMP width) of $12 \times t_{TE}$ (approximately 94 μs), Filter pre-charge width of $4 \times t_{TE}$ (approximately 31 μs), Filter pre-charge bandwidth of 25 kHz, Filter fine settling bandwidth of 5 kHz, NUMAV = 2 (2 ADC averages), 1 μF decap on the BG pin, $C_{IN} = 50 \text{ pF}$ (capacitor across the input pins to model the zero bias differential capacitance of the PD)

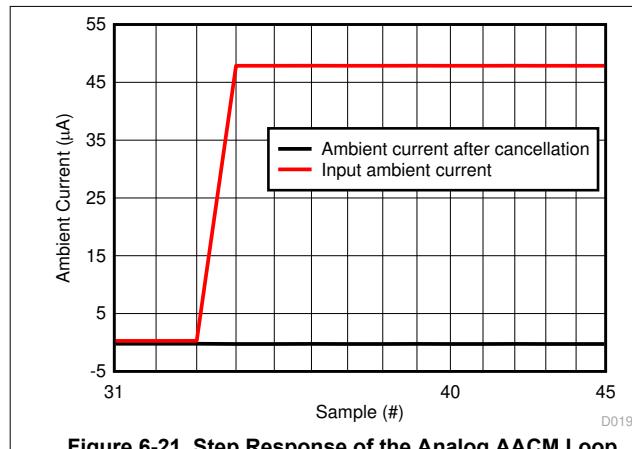


Figure 6-21. Step Response of the Analog AACM Loop

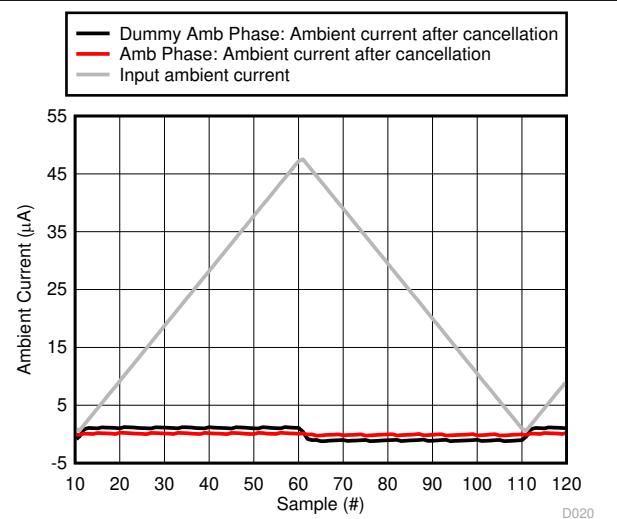


Figure 6-22. Transient Response of the Digital AACM Loop

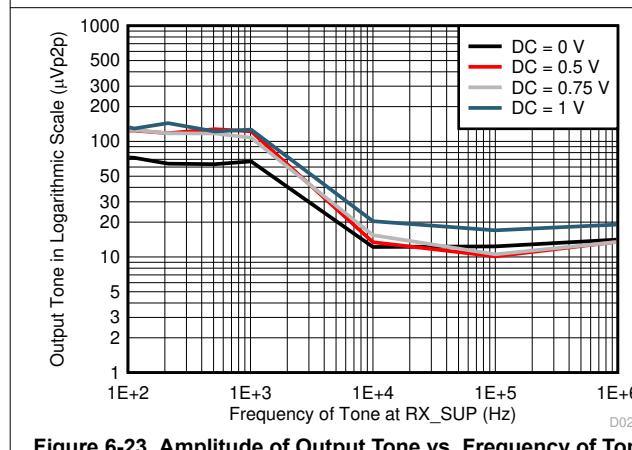


Figure 6-23. Amplitude of Output Tone vs. Frequency of Tone on RX_SUP Across Different Output DC Level in LDO Bypass Mode

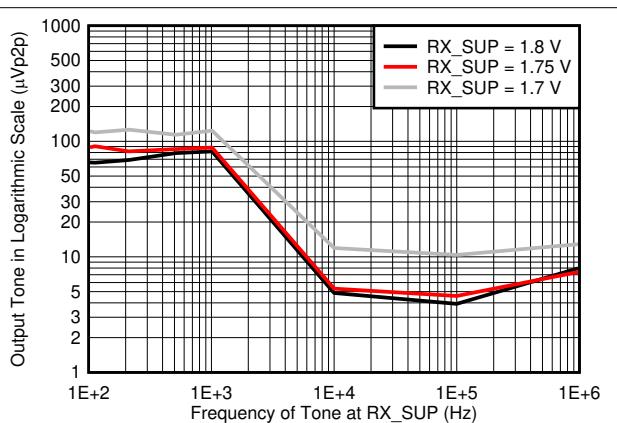


Figure 6-24. Amplitude of Output Tone vs. Frequency of Tone on RX_SUP Across Different RX_SUP Voltages in LDO Bypass Mode

6.11.1 Typical Characteristics - PPG Signal Chain (continued)

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, LDO Bypass mode (with RX_SUP = IO_SUP = 1.8 V), Mixed clock mode with 32.768 kHz input clock, TIA $R_f = 250 \text{ k}\Omega$, TIA $C_f = 20 \text{ pF}$, 25-Hz PRF, LED ON width (and SAMP width) of $12 \times t_{TE}$ (approximately 94 μs), Filter pre-charge width of $4 \times t_{TE}$ (approximately 31 μs), Filter pre-charge bandwidth of 25 kHz, Filter fine settling bandwidth of 5 kHz, NUMAV = 2 (2 ADC averages), 1 μF decap on the BG pin, $C_{IN} = 50 \text{ pF}$ (capacitor across the input pins to model the zero bias differential capacitance of the PD)

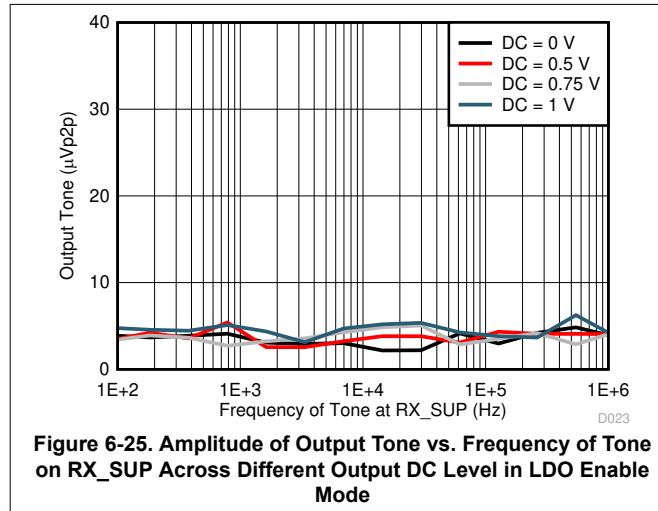


Figure 6-25. Amplitude of Output Tone vs. Frequency of Tone on RX_SUP Across Different Output DC Level in LDO Enable Mode

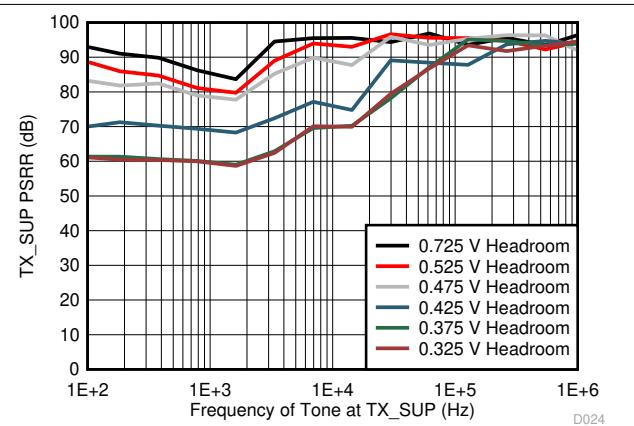
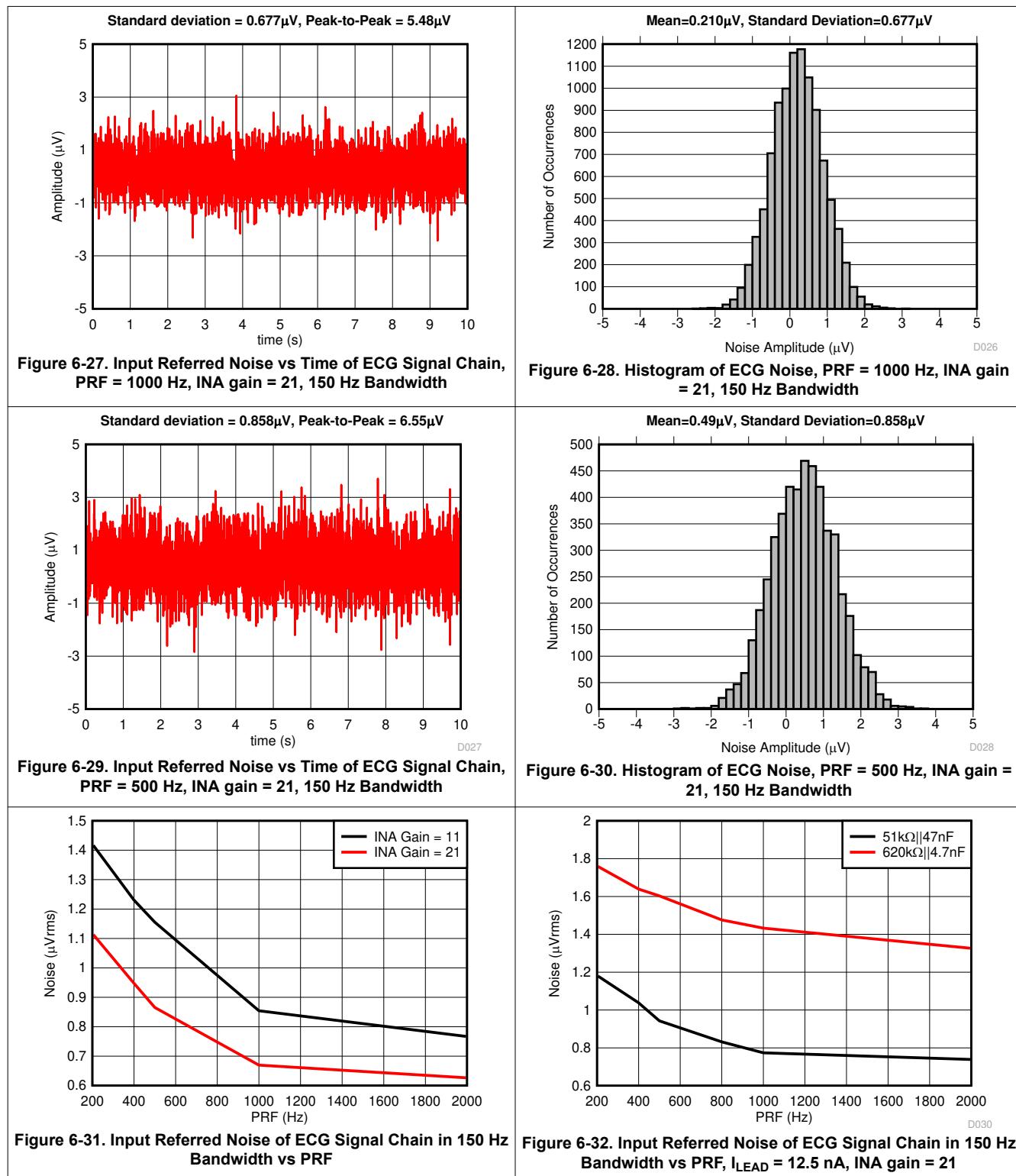


Figure 6-26. PSRR of TX_SUP Across Frequency of Tone on TX_SUP for Different LED Driver Headroom Voltages

6.11.2 Typical Characteristics - ECG Signal Chain

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, RX_SUP = 1.8V (LDO bypass mode), IO_SUP = 1.8 V, Synchronous mixed clock mode with 32.768 kHz input clock ECG: 1-kHz sampling rate, INA gain of 21, Chopper mode enabled, LPF enabled



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6.11.2 Typical Characteristics - ECG Signal Chain (continued)

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, RX_SUP = 1.8V (LDO bypass mode), IO_SUP = 1.8 V, Synchronous mixed clock mode with 32.768 kHz input clock ECG: 1-kHz sampling rate, INA gain of 21, Chopper mode enabled, LPF enabled

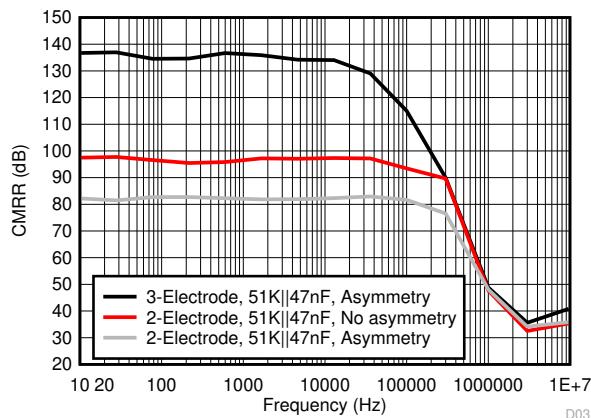


Figure 6-33. CMRR of the ECG Signal Chain as Function of Frequency with 2-Electrode and 3-Electrode Operation

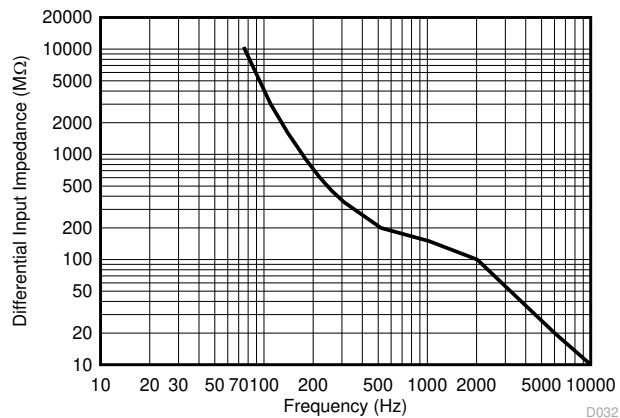


Figure 6-34. Differential Input Impedance of the ECG Inputs as a Function of Signal Frequency

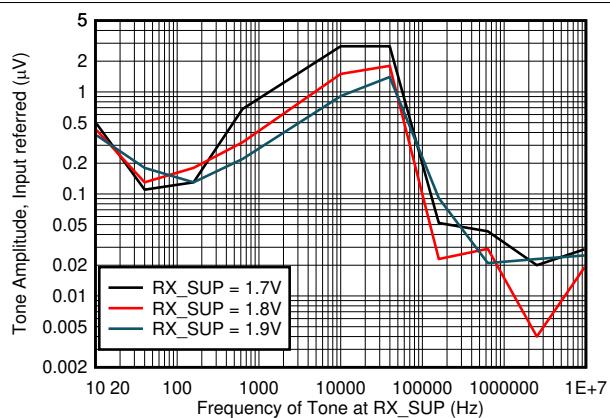


Figure 6-35. Amplitude of the Tone at the ECG Output for 50 mVpp Tone on RX_SUP as a Function of Frequency (LDO Bypass Mode, Across RX_SUP Voltage)

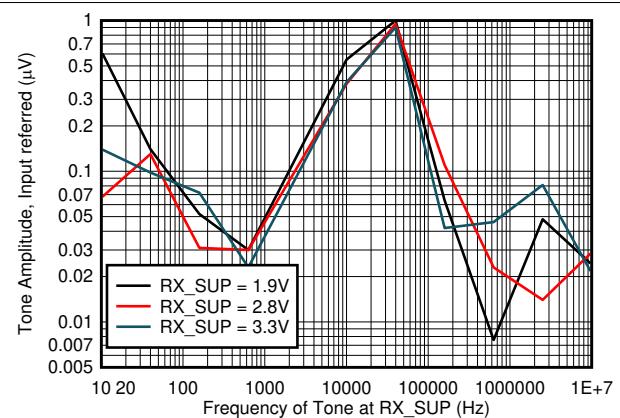


Figure 6-36. Amplitude of the Tone at the ECG Output for 50 mVpp Tone on RX_SUP as a Function of Frequency (LDO Enable Mode, Across RX_SUP Voltage)

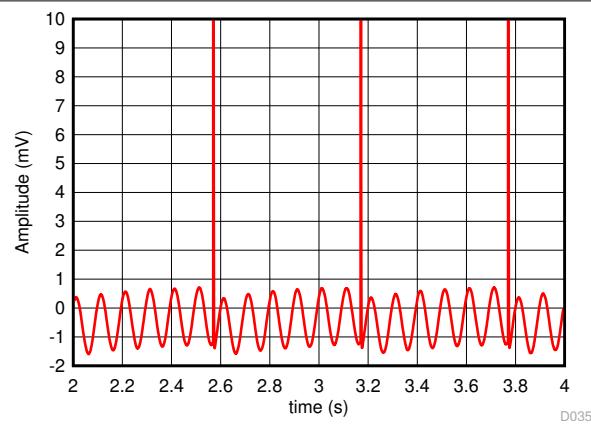


Figure 6-37. ECG Signal Chain Response to 2 mVpp, 10 Hz Sinusoidal Signal in the Presence of Pacemaker Signal of 200 mV Amplitude, 1 ms Pulse Duration

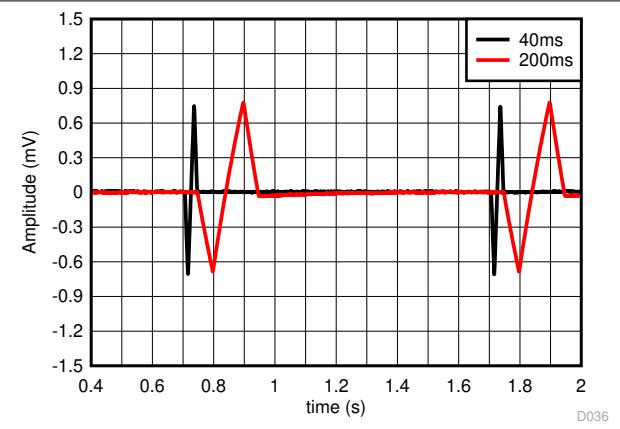


Figure 6-38. ECG Signal Chain Response to 40 ms and 200 ms Triangular Pulse Train of 1.5 mVpp Amplitude

6.11.2 Typical Characteristics - ECG Signal Chain (continued)

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, RX_SUP = 1.8V (LDO bypass mode), IO_SUP = 1.8 V, Synchronous mixed clock mode with 32.768 kHz input clock ECG: 1-kHz sampling rate, INA gain of 21, Chopper mode enabled, LPF enabled

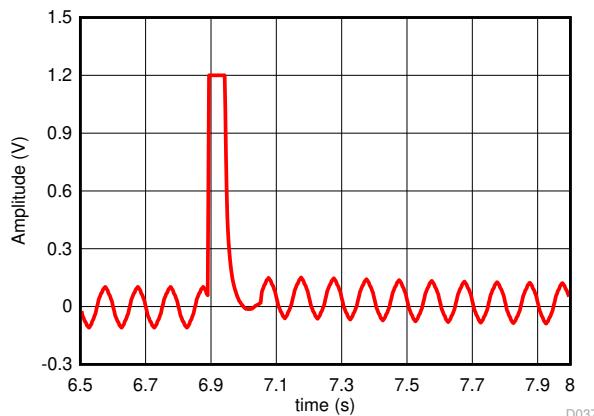


Figure 6-39. Fast Recovery of ECG Signal Chain High Pass Filter to a Differential Input Offset Step of 200 mV, ECG $f_{\text{HPPF}} = 0.4$ Hz

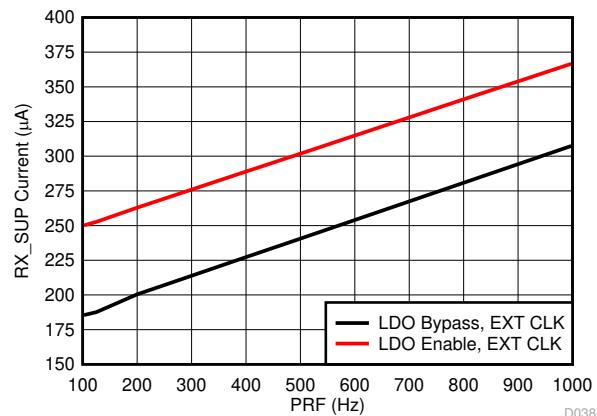


Figure 6-40. RX_SUP Current vs. PRF Across LDO and Clocking Modes for ECG Mode

7 Detailed Description

7.1 Overview

The AFE has signal chains for PPG and ECG which share the same ADC. Simultaneous acquisition of up to 24 PPG signals involving up to 8 LEDs and up to 4 PDs are supported, thereby enabling simultaneous applications like optical heart rate monitoring (OHRM) and pulse oximetry. The Ambient in the PPG signal is dealt with in two ways. The DC from the ambient signal can be cancelled by current subtraction at the receiver inputs using low noise Offset Cancellation DACs. Such cancellation may be programmed by the Host or controlled automatically by the Analog Ambient cancellation loop inside the AFE. Additionally, the tones in the LED data due to tones in the ambient can be suppressed using digital subtraction of the Ambient phase data from the LED phase data. The additional DC signal in the LED phase can be cancelled at the input using an LED Offset Cancellation DAC which can be either controlled by the MCU or automatically through one of 4 loops.

The ECG signal acquired from a pair of electrodes can be used for a standalone ECG application or can be combined with the information from the PPG signal for generating other useful metrics. Automatic detection of lead on/off at the ECG input pins allows for easy switch between operating modes (for example, from acquiring only PPG to acquiring PPG and ECG). Output from a RLD amplifier can be used to set the bias for the body.

A first in, first out (FIFO) is used to store samples from each PPG and ECG signal phase across multiple periods. When the FIFO is enabled, an output pin can be configured to serve as a FIFO_RDY interrupt which indicates when the FIFO has been filled up to a programmed watermark level. Several other useful interrupts can also be configured to come out on the output pins. The programming of the AFE registers and the readout of the FIFO can be done using either an SPI interface or an I2C interface (selectable using the I2C_SPI_SEL pin).

The AFE has several clocking options which allow it to be clocked using an internal oscillator or using an external clock or a combination of both. The clocking also allows for easy data synchronization to a system master clock.

The AFE can operate with either the internal LDOs enabled or bypassed. When LDO_BYP is connected to RX_SUP, the LDOs are powered down with their output tristate, and the internal nodes ALDO_1V8 and DLDO_1V8 are connected through switches to RX_SUP. When LDO_BYP is 0V, the two Internal LDOs are enabled and they drive ALDO_1V8 and DLDO_1V8 to 1.8V.

7.2 Functional Block Diagram

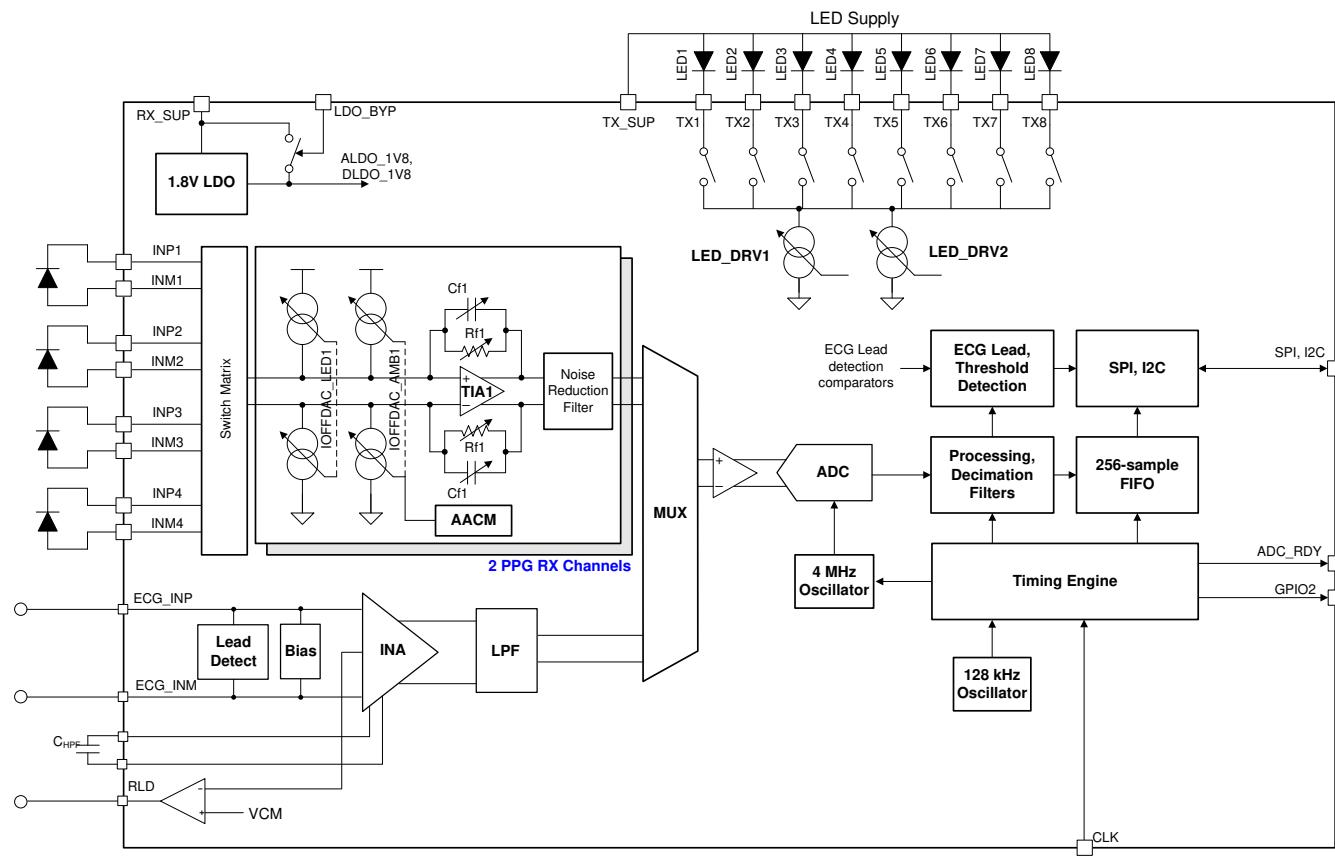


Figure 7-1. AFE4950 Block Diagram

7.3 Feature Description

7.3.1 Clocking and Signal acquisition

7.3.1.1 Overview

The AFE supports a PPG acquisition mode in which up to 24 PPG signals can be simultaneously acquired, an ECG acquisition mode in which a single-lead ECG signal can be acquired, as well as a Mixed acquisition mode in which both a set of PPG signals (up to 24) and the ECG signal can be acquired in a synchronized manner.

The PPG signal acquisition involves firing pulses of current into one or more LEDs while simultaneously acquiring the signal current from one or more Photodiodes and converting it into a digital output word. The rate of firing the pulses is referred to as the Pulse repetition frequency (PRF), a parameter that can be set using a programmable count register.

The AFE supports several clocking modes. In the internal oscillator mode, the AFE runs completely on an internally generated 128 kHz clock without requiring any external clocking. The AFE can also run on an external clock (usually 128 kHz) with the internal oscillator shut down. The AFE also has clocking modes in which an external clock (usually derived from a 32.768 kHz RTC clock) is used to set the PRF whereas the internal oscillator is used to generate all the timing signals within a PRF period. These clocking modes allow for a synchronization of the data rate with a system-level master clock, while using the internal oscillator for generating the timing of the internal operations within a PRF cycle.

Different PPG phase signals can be acquired at the PRF rate or can be programmed to a rate which is a binary fraction of the PRF rate. Depending on the number of ECG acquisition time slots defined within each PRF cycle, the ECG signal can be acquired at either the PRF or at a multiple of the PRF rate. By using a moving average filter, the output data stream from both the PPG and ECG signals can be optionally decimated to a lower rate while retaining good in-band SNR.

The AFE has hooks to allow a quick and seamless transition from one signal acquisition mode to another with minimal reconfiguration. Interrupts from the AFE can be configured to automatically prompt the Host when such a mode switch may be warranted – for example, when the ECG leads are detected and ECG signal acquisition needs to start. Some of the configuration registers are duplicated across acquisition modes, thereby allowing the signal chain to be independently configured for each mode on power up, and for the switch from one mode to another to require minimal register re-configuration. The PPG phase configurations used in the PPG acquisition mode occupy 24 sets of registers (one set for each of the 24 phases) and these registers are not duplicated for the PPG phase configuration in the Mixed acquisition mode. The same set of PPG phase configuration registers are referenced in the Mixed acquisition mode also. However, the PPG phases in the PPG acquisition mode and Mixed acquisition mode can reference either same or different portions of the Phase configuration register map, thereby achieving either same or mutually exclusive phase configuration between the two acquisition modes (this exclusivity is of course possible in totality only if the sum of the number of phases used in the two acquisition modes is less than or equal to 24).

7.3.1.2 Clocking Modes

The AFE has five clocking modes:

1. Internal oscillator mode
2. External clock mode
3. Single-shot acquisition mode
4. Mixed clock mode
5. Synchronous Mixed clock mode

The internal oscillator mode can be used when there is no clock signal of appropriate frequency available to clock the AFE. The Single-shot clocking mode is useful to synchronize the AFE data acquisition with data acquisition from another chip (for eg. an accelerometer). The Single shot clocking mode, when clocked with a periodic pulse train at the PRF rate achieves signal acquisition at the PRF rate. The Mixed clock mode is useful if the PRF needs to be derived using an accurate clock like a 32.768 kHz RTC clock, but the timing engine needs to continue to run at higher resolution off the 128 kHz internal oscillator. The Synchronous Mixed clock mode works similar to the Mixed clock mode but with an additional mechanism to synchronize the average

frequency of the internal oscillator to the RTC clock. Such synchronization is essential while operating with the ECG signal acquisition enabled.

The AFE timing operation involves a periodic generation of various timing control signals using a timing engine. The periodicity of the signal generation is referred to as the PRF, or Pulse repetition frequency. The AFE has two state machines that determine the periodicity of the timing signals as well as the generation of the signals:

1. A PRF state machine that gets reset either by a PRF counter reaching a programmed count or by a pulse on the external CLK pin. The PRF counter is enabled by setting the PRF_COUNTER_ENABLE register bit to '1'.
2. A timing engine state machine that generates the various timing control signals (for example, the LED ON and ADC Conversion signals of each phase) at the periodicity determined by the PRF state machine. The timing engine is enabled by setting the TIMER_ENABLE register bit to '1'. Setting the TM_COUNT_RST optionally keeps the timing engine in a reset state.

[Table 7-1](#) shows a comparison of the different timing modes. CLK_INT corresponds to the internally generated 128 kHz oscillator (f_{CLK_INT} approximately 128 kHz) which is trimmed to an accuracy of +/-1%. CLK_EXT corresponds to a signal provided on the external CLK pin. CLK_TE refers to the clock on which the timing engine operates. The time period of CLK_TE ($t_{TE} = 1/f_{CLK_TE}$) determines the time resolution to which the timing signals can be programmed. CLK_PRF refers to the clock on which the PRF counter counts. f_{CLK_PRF} refers to the frequency.

Table 7-1. Clocking Modes Available in the AFE

MODE	REGISTER SETTINGS FOR DIFFERENT SIGNAL ACQUISITION MODES		WAVEFORM APPLIED ON CLK PIN	PRF SET BY	f_{CLK_TE}	f_{CLK_PRF}
	PPG	ECG, Mixed				
Internal oscillator mode	CLKBUF_TRISTATE = 1	CLKBUF_TRISTATE = 1	–	PRF Counter running on f_{CLK_INT}	f_{CLK_INT} ⁽²⁾	f_{CLK_INT} ⁽²⁾
External clock mode	OSC_DIS_128K_PPG = 1	OSC_DIS_128K_NOTPPG=1	Free-running periodic waveform of frequency f_{CLK_EXT}	PRF Counter running on f_{CLK_EXT}	f_{CLK_EXT}	f_{CLK_EXT}
Single-shot acquisition mode	SINGLE_SHOT_MODE_PPG = 1 PDN_OSC_IN_DEEP_SLEEP_PPG = 1	Not Supported	Pulse train with periodicity equal to PRF period	High-going pulse from a pulse train determines start of new PRF cycle	f_{CLK_INT} ⁽²⁾	N/A
Mixed clock mode	SINGLE_SHOT_MODE_PPG = 1 EN_MIXED_CLK_MODE_PPG =1 PDN_OSC_IN_DEEP_SLEEP_PPG = 1	Not Supported	Free-running periodic waveform f_{CLK_EXT}	PRF Counter running on f_{CLK_EXT}	f_{CLK_INT} ⁽²⁾	f_{CLK_EXT}
Synchronous Mixed clock mode	EN_SYNC_INT_OSC = 1 SINGLE_SHOT_MODE_PPG = 1 EN_MIXED_CLK_MODE_PPG = 1 PDN_OSC_IN_DEEP_SLEEP_PPG = 1	EN_SYNC_INT_OSC=1	Free-running periodic waveform f_{CLK_EXT} ⁽¹⁾	PRF Counter running on f_{CLK_EXT} in PPG mode and on $4 \times f_{CLK_EXT}$ in ECG or Mixed Mode.	$f_{CLK_INT} = 4 \times f_{CLK_EXT}$ ⁽³⁾	$f_{CLK_INT} = 4 \times f_{CLK_EXT}$ ⁽³⁾

(1) f_{CLK_EXT} is to be set to 32.768 kHz.

(2) Internal oscillator frequency is approximately 128 kHz.

(3) Use only in ECG, or Mixed Mode. Internal oscillator frequency (f_{CLK_INT}) is made pseudo-synchronous to CLK_EXT and is equal to $4 \times f_{CLK_EXT}$.

In the Internal oscillator mode and the external clock mode, the frequency of the clock used for the PRF counter and the internal oscillator is the same. However, in the single-shot mode and the mixed clock mode, the signal that controls the timing engine gets decoupled from the signal that determines the PRF setting. For example, in the Mixed clock mode, a 32.768 kHz RTC clock can be used to run the PRF counter whereas a higher frequency (better time resolution) 128 kHz internal oscillator clock is used to control the timing engine. In the Synchronous mixed clock mode, the 128 kHz internal oscillator is made pseudo-synchronous with the 32.768 kHz RTC clock. As a result, f_{CLK_INT} becomes equal to $4 \times f_{CLK_EXT}$ on an average.

7.3.1.2.1 Internal Oscillator and External Clock Modes

The default clocking mode is the internal oscillator mode. In this mode, the timing engine that generates the timing for the signal phases within the PRF cycle as well as the counter that keeps count of the PRF runs off an internal 128 kHz oscillator. The internal oscillator needs to be always active while operating in this mode.

Note

If the CLK pin is left floating while operating in the Internal oscillator mode, the clock input buffer can draw current. To prevent this, set the CLKBUF_TRISTATE bit to '1' to tri-state the clock input buffer.

The External clock mode can be enabled by setting the OSC_DIS_128K register bit to '1'. In this mode, the internal oscillator is shut down and the timing engine and PRF counter runs off an external clock applied on the CLK pin. The default frequency expected on the CLK pin in the external clock mode is 128 kHz. However, other allowed clock frequencies are 32 kHz and 64 kHz with an allowed variation of up to +/-2.5% around each of these frequencies. The frequency being used on the CLK pin must be programmed into the register word EXT_CLK_FREQ in the manner shown in [Table 7-2](#).

Table 7-2. Clock Frequency Ranges in External Clock Mode

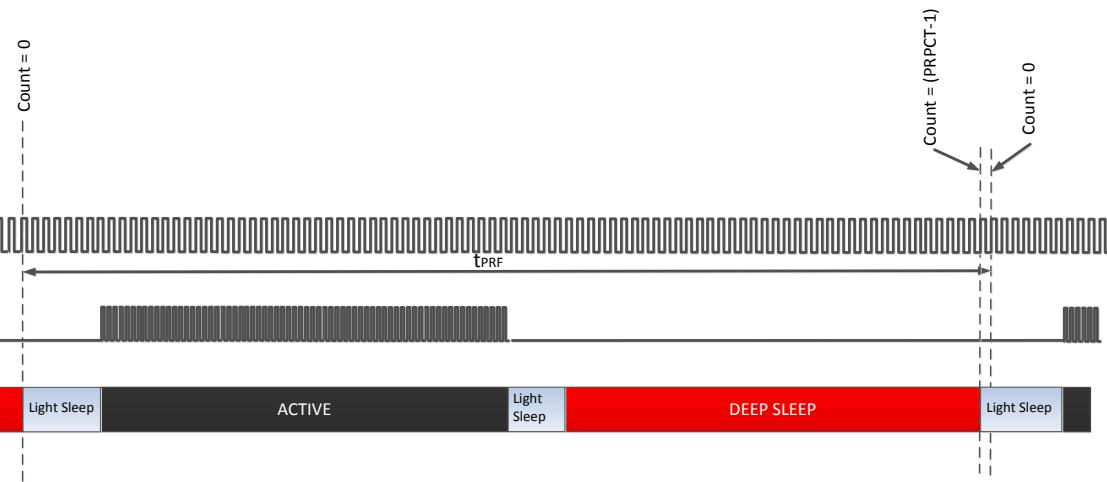
CLK FREQUENCY RANGE	DECIMAL VALUE TO BE WRITTEN INTO EXT_CLK_FREQ REGISTER WORD	Timing resolution (t_{TE})
128 kHz ± 2.5%	0	approximately 8 μ s
64 kHz ± 2.5%	5	approximately 16 μ s
32 kHz ± 2.5%	6	approximately 32 μ s

External clock frequencies of 256 kHz (±2.5%) and 512 kHz (±2.5%) can be supported by setting the EXT_CLK_FREQ word to '0' and using the CLK_DIV_CLK register control to enable a clock divider as shown in [Table 7-3](#).

Table 7-3. Using the Clock Divider in External Clock Mode

CLK frequency range	Decimal value to be written into EXT_CLK_FREQ register word	Decimal value to be written into CLK_DIV_CLK register word	Division factor for external clock	Timing resolution (t_{TE})
128 kHz ± 2.5%	0	0	1	approximately 8 us
256 kHz ± 2.5%	0	1	2	
512 kHz ± 2.5%	0	3	4	

The timing scheme for the External clock mode and Internal oscillator modes are shown in [Figure 7-2](#). The PRF counter counts from 0 to a count equal to (PRPCT-1). The duration of this count defines a PRF cycle. The Active and Deep sleep windows within the PRF cycle are automatically generated by the timing engine. Within the active phase, up to 24 signal phases can be defined and automatically generated by the phase timing engine.

**Figure 7-2. Overview of Timing in the External Clock Mode and Internal Oscillator Mode**

The PRPCT parameter is set through separate registers in the three signal acquisition modes as in [Table 7-4](#)

Table 7-4. Registers for setting PRPCT across signal acquisition modes

Mode	Register	PRPCT set as
PPG acquisition mode	REG_PRPCT_PPG	REG_PRPCT_PPG
Mixed acquisition mode	REG_PRPCT_MIX	REG_PRPCT_MIX
ECG acquisition mode	REG_PRPCT_ECG	REG_PRPCT_ECG

Calibration of the Internal Oscillator:

By default, the internal oscillator is trimmed to an accuracy of $\pm 1\%$. An optional calibration routine can be used to calibrate the internal oscillator to a much higher accuracy ($\pm 0.2\%$) using a high-accuracy external clock like a 32.768 kHz RTC clock. The calibration works by counting the number of clock periods of the external reference clock (reference clock count) over 6400 clock periods (observation window) of the internal oscillator (approximately 128 kHz) clock, and by adjusting the internal oscillator frequency accordingly.

To run the calibration, follow the below steps:

- Apply the high-accuracy external clock (For example, 32.768 kHz RTC clock) on the CLK pin
- Set the EN_128K_CLK_CALIB_1, EN_128K_CLK_CALIB_2 register bits to enable the Clock calibration routine
- Set CLK_128K_CALIB_RANGE = 2
- Input the frequency of the external clock using the EXT_CLK_CNT_CALIB register control as:
 - $\text{EXT_CLK_CNT_CALIB} = 6400 * (\text{f}_{\text{EXT}} / 128)$ where f_{EXT} is external clock frequency in kHz For example, if $\text{f}_{\text{EXT}} = 32.768$ kHz, then set EXT_CLK_CNT_CALIB to 1638.

The frequency of the internal oscillator gets adjusted with improved accuracy during the calibration routine. The calibration routine can be run either as a one-time calibration routine at start or can be run continuously in the background during normal operation. Two factors need to be considered if running the calibration routine continuously:

- Make sure the external clock (being asynchronous to the internal oscillator) does not cause any tones at the output
- Set a hysteresis count using CLK_128K_CALIB_RECONV_THR such that the internal oscillator frequency is changed only if the reference clock count error over the observation period exceeds this threshold. This helps avoid a switching of the 128 kHz oscillator if the reference clock count keeps toggling between closely spaced counts.

7.3.1.2.2 Single-shot Clocking Mode

In the Single-shot clocking mode, a high-going pulse (of width between 30 and 100 μ s) input on the CLK pin resets the timing engine and the PRF counter and triggers the start of a new cycle of signal acquisition. In this mode, the timing engine and the PRF counter run off the internal oscillator. While enabling the single-shot acquisition mode, the following register controls need to be set:

- Set SINGLE_SHOT_MODE_PPG to '1' to enable the Single-shot clocking mode
- Set OSC_DIS_128K to '0' to keep the 128 kHz oscillator active
- Set the PDN_OSC_IN_DEEP_SLEEP_PPG bit to '1' – setting this bit automatically shuts down the 128 kHz oscillator and freezes the timing engine as soon as the timing engine enters the Deep sleep window (after all the active phases are completed). As a result, the timing engine stays in a frozen state until the next high-going pulse on the CLK pin which once again wakes up the 128 kHz oscillator, resets the timing engine and results in a fresh cycle of signal acquisition. Additionally, set the PRPCT to a count to greater than the count where the Deep sleep window starts. This ensures that the PRF counter does not get reset because of the count reaching (PRPCT-1) – such an occurrence would cause a fresh set of signal acquisition.
- Set the EN_INT_IN_SINGLE_SHOT register bit additionally if needed to enable the generation of the INT_OUT2 interrupt on the GPIO2 pin. The start and end counts for these interrupts are based on the 128 kHz oscillator and the interrupt needs to be positioned to start and finish before the Deep sleep window starts.

The Single shot clocking mode, when clocked with a periodic pulse train behaves similar to the other clocking modes. The periodicity of the pulse train determines the PRF and should be compliant with the range of supported PRF. The Single shot clocking mode could also be used for acquisition of data samples placed non-uniformly in time to enable 'on-demand' signal acquisition. While the Single-shot clocking mode enables 'on-demand' signal acquisition merely by issuing a trigger pulse on CLK pin, there could be loss of signal accuracy if the trigger pulses are spaced very far apart. Such a loss of signal accuracy could occur due to slow leakages of internal nodes of the receiver signal chain. One way to overcome such a loss of signal accuracy is to follow the first trigger pulse with a second one after the first set of signal acquisitions are completed. The signal accuracy of the second set of signal acquisition is expected to be better than the first set.

Providing a periodic pulse train on the CLK pin with a periodicity of f_{PRF} in the Single-shot clocking mode results in a uniform sampling signal acquisition at a rate equal to f_{PRF} . The Single-shot clocking mode is also useful when it is required to synchronize the data acquisition from the AFE to a common time reference for the entire system.

The timing scheme of the Single-shot clocking mode is shown in [Figure 7-3](#).

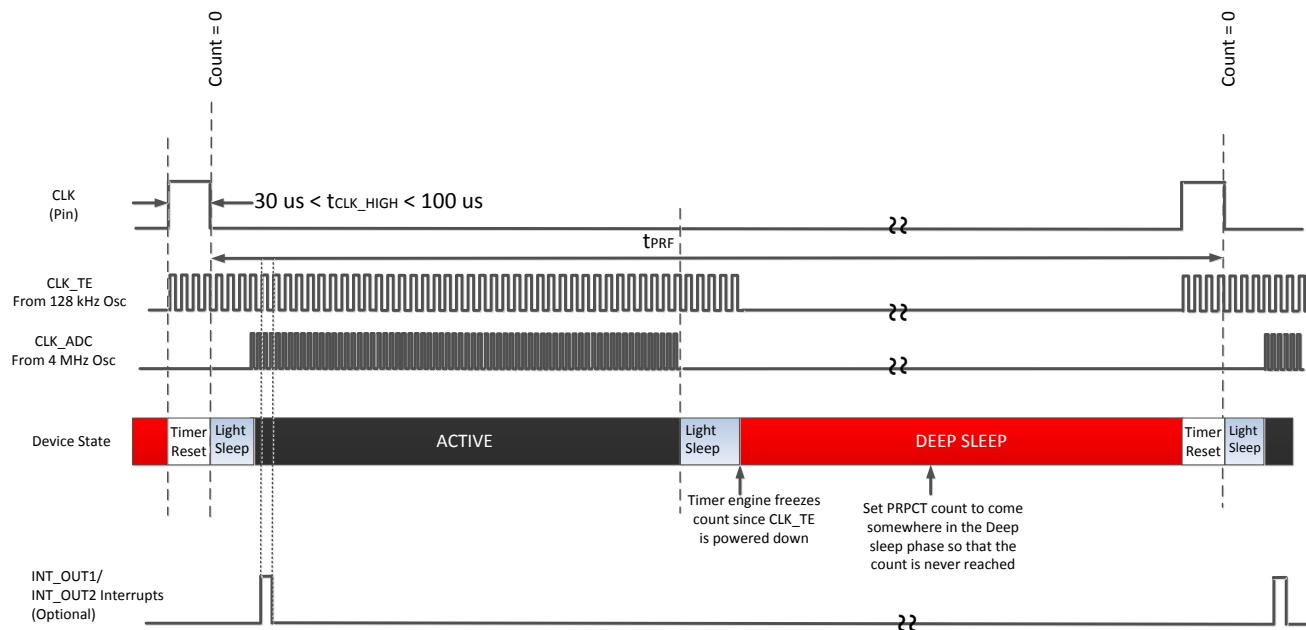


Figure 7-3. Timing Scheme in the Single Shot Acquisition Mode

7.3.1.2.3 Mixed Clocking Mode

In the Mixed clock mode, a free-running clock on the CLK pin is used to generate the PRF count as shown in [Figure 7-4](#). The REG_PRPCT* register control sets PRPCT, the count for the PRF counter, with the PRF counter counting on the CLK from 0 (PRPCT-1). In this mode, the timing engine continues to run off the 128 kHz internal oscillator. However the CLK pin could be driven by a lower frequency clock like the 32.768 kHz RTC clock.

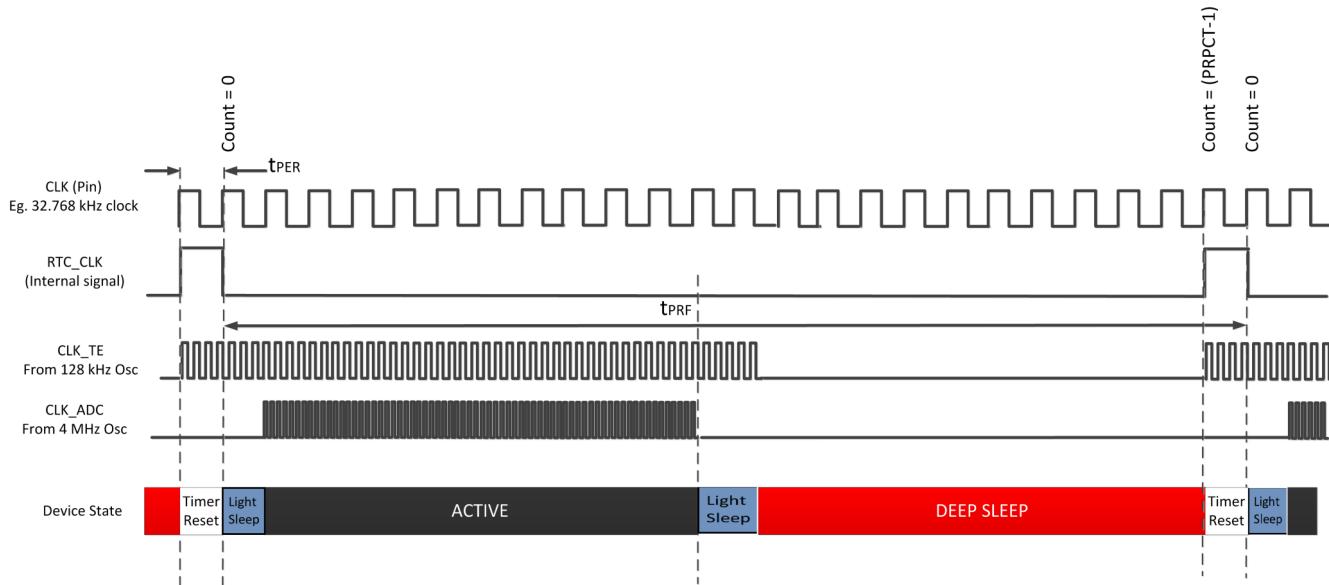


Figure 7-4. Overview of timing in the Mixed clock mode

While enabling the Mixed clock mode, the following register controls need to be set:

- Set bits SINGLE_SHOT_MODE_PPG and EN_MIXED_CLK_MODE_PPG to '1' to enable the Mixed clock mode
- Set OSC_DISABLE_128K to '0' to keep the 128 kHz oscillator active
- Set the PDN_OSC_IN_DEEP_SLEEP_PPG bit to '1' – setting this bit automatically shuts down the 128 kHz oscillator and freezes the timing engine as soon as the timing engine enters the Deep sleep window (after all the active phases are completed). As a result, the timing engine stays in a frozen state until the start of the next PRF cycle which once again wakes up the 128 kHz oscillator, resets the timing engine and results in a fresh cycle of signal acquisition.

By default, the PRF counter counts from 0 to (PRPCT-1) in increments of 1 while operating in the Mixed clock mode. The increment of the PRF counter can be set to a parameter STEP_COUNT programmable between 1 and 128. The parameter STEP_COUNT is derived from the register REG_STEP_COUNT as (REG_STEP_COUNT + 1).

The STEP_COUNT parameter can be used to achieve precise PRF on an average. For example, while running off a 32.768 kHz RTC clock, setting the STEP_COUNT to 25 results in an PRF (averaged over time) of precisely 25 Hz when the PRPCT parameter is set to 32768.

7.3.1.2.4 Synchronous mixed clock mode

The Synchronous Mixed clock mode works in a manner similar to the Mixed clock mode but with an additional mechanism for the synchronization of the internal oscillator with respect to the external clock. This synchronization mechanism is built in to ensure that a PRF cycle (set by an integer number of counts of the external RTC clock periods) also spans an integer number of clock periods of the internal oscillator. For example, while operating in the Synchronous mixed clock mode with an external clock of 32.768 kHz, the average rate of the internal oscillator over four consecutive periods becomes exactly equal to 131.072 kHz (four times the external clock frequency). Such synchronization is essential while operating in the Mixed acquisition mode and ECG acquisition modes wherein the PRF cycle is partitioned into fixed-width time slots and the signal acquisition happens within these time slots.

7.3.1.3 Signal Acquisition Modes

The AFE supports three signal acquisition modes:

1. PPG acquisition mode – acquire only PPG signals (up to 24 signal phases)
2. Mixed acquisition mode – acquire both PPG (up to 24 signal phases) and ECG signals
3. ECG acquisition mode – acquire only ECG signal from a single lead

The different signal acquisition modes can be set using the MODE_SEL register as shown in [Table 7-5](#)

Table 7-5. Signal Acquisition Modes

MODE_SEL Register	Mode	Comments
001 (default)	PPG acquisition	Only PPG signal acquired.
011	Mixed acquisition (ECG+PPG)	PPG and ECG signals acquired synchronously.
010	ECG acquisition	Only ECG signal acquired. This mode is a subset of Mixed acquisition mode.

The device is required to operate in different signal acquisition modes at different times. For example, when the ECG leads are not connected, the device can operate in the PPG acquisition mode continuously but can be required to switch to the Mixed acquisition mode when the ECG leads get connected. Also, different acquisition modes can require different signal chain settings. For example, the PPG acquisition mode can operate at a low PRF (For example, 25 Hz) but the device can require to switch to a higher PRF while acquiring ECG signals. Separate configuration registers are provided for each mode and on power up, all the register configurations for each mode can be loaded into the appropriate registers. Some of these registers are duplicated across modes so that the registers can be set to independent values for the different modes, thereby enabling the switch from one mode to another with the minimum set of register changes.

To enable quick and smooth switching between different signal acquisition modes (for example from Mode 1 to Mode 2) without requiring device reset, the AFE has a *Freeze State* control which can be enabled by writing a register interrupt bit REG_INTR_TO_AFE, programming the bit first to '1' and then to '0'. If the device is operating in Mode 1, and the register interrupt bit gets programmed during the Active window of the PRF cycle, the device completes the current active window, reach the Deep sleep window, and go into the Freeze state. If the REG_INTR_TO_AFE gets programmed during the Deep sleep window of the PRF cycle, then the device immediately goes into the Freeze State. With the AFE in the Freeze State, the host can configure the device to operate in Mode 2 (typically requiring a change to only the MODE_SEL register) and then writing a *Release State* register bit (REL_AFE_FREEZE), programming the device first to '1' and then to '0'. In the Freeze state, all the remaining (unread) data in the FIFO corresponding to Mode 1 can be read completely, or the FIFO pointers can be reset such that the subsequent readout of the FIFO after the release of the freeze state corresponds to data from Mode 2.

The transition from one mode to another can be initiated by the MCU as a response to an AFE interrupt. A possible scenario is the following – the AFE is operating in PPG acquisition mode (Mode 1) with the ECG lead-on detect interrupt enabled. On detection of the ECG leads, the AFE issues an interrupt to the MCU, and the MCU switches the mode to Mixed acquisition mode. The sequence of operations is summarized below:

- AFE is operating in PPG acquisition mode with the ECG lead-on detect interrupt enabled.
- AFE generates a Lead-on detect interrupt indicating ECG lead status change.
- Host reads the status registers and decides if the AFE needs to switched to Mixed acquisition mode.
- Host sets the interrupt register bit REG_INTR_TO_AFE first to '1', waits for at least $10 \times \text{CLK_TE}$ periods (approximately 78 μs) and writes REG_INTR_TO_AFE to '0'.
- The Host waits for a delay equal to 1 PRF cycle for the AFE to enter freeze state.
- The Host reads all the FIFO data (or resets the FIFO read pointer) and then writes the MODE_SEL register to change the mode to Mixed acquisition mode.
- The Host writes the *Release Freeze* register bit REL_AFE_FREEZE to '1', waits for at least $10 \times \text{CLK_TE}$ periods (approximately 78 μs) and writes REL_AFE_FREEZE to '0'.
- A new PRF cycle starts with the configuration pre-set for the Mixed acquisition mode.

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Figure 7-5 and Figure 7-6 show the timing diagram for scenarios where the REG_INTR_TO_AFE is written during the Active window and during the Deep-sleep window respectively.

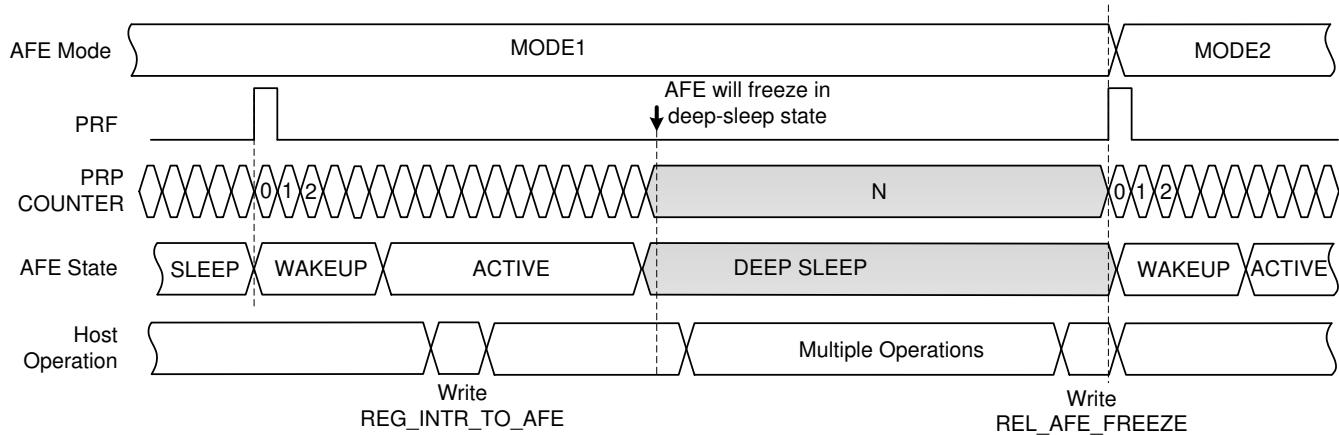


Figure 7-5. Switching Between Different AFE Modes with REG_INTR_TO_AFE Written During Active State

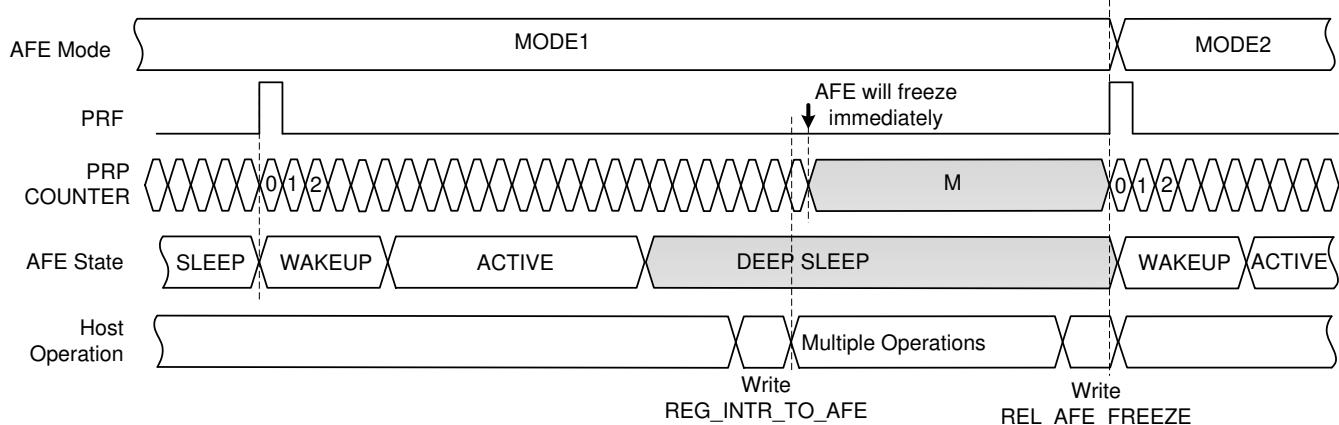


Figure 7-6. Switching Between Different AFE Modes with REG_INTR_TO_AFE Written During Deep-Sleep State

Table 7-6 shows the signal acquisition modes supported by each of the 5 clocking modes.

Table 7-6. Signal Acquisition Modes Supported by Each Clocking Mode

Clocking Mode	Signal Acquisition Modes Supported		
	PPG	ECG	Mixed
Internal oscillator mode	X	X	X
External clock mode	X	X ⁽¹⁾	X ⁽¹⁾
Single-shot clocking mode	X	-	-
Mixed clock mode	X	-	-
Synchronous Mixed clock mode		X ⁽²⁾	X ⁽²⁾

(1) Set to approximately 128 kHz

(2) Set to 32.768 kHz

Table 7-7 lists the supported use cases for the different acquisition modes.

Table 7-7. Summary Of Operating Modes And Key Features

Acquisition Mode	Use case mode	Comments
PPG	Watch-on detection	Detect if user has worn the watch based on sensing electrode contact to the wrist electrode. Can be used to switch to active PPG acquisition
	PPG + Watch-on detection	-
	PPG + Low power lead-on detection	PPG + Check if 2 or 3 ECG electrodes have been contacted and trigger acquisition of either 2-electrode or 3-electrode ECG mode using either the ECG or Mixed acquisition modes
	PPG + Impedance measurement	PPG + Continuous low-power measurement of impedance between chosen leads using AC excitation at low frequency
ECG	ECG with AC/DC lead detection	-
Mixed	PPG + ECG with AC/DC lead detection	-

7.3.1.3.1 Configuration of the AFE to seamlessly switch across signal acquisition modes:

To switch across the signal acquisition modes with minimal number of register writes, keep the following points in mind:

1. On power up, write the appropriate configuration registers for all intended modes of operation. The registers are named as per the following convention:
 - Register names ending with *_PPG* specify configuration for the parameter applicable only in PPG acquisition mode
 - Register names ending with *_ECG* specify configuration for the parameter applicable only in ECG acquisition mode
 - Register names ending with *_MIX* specify configuration for the parameter applicable only in Mixed acquisition mode
 - Register names ending with *_NOTPPG* specify configuration for the parameter applicable both in ECG and Mixed acquisition mode
 - Register names without any of the above endings are not acquisition mode specific. They are applicable to the parameter in all acquisition modes (provided of course the signal chain block controlled by the parameter is active in that mode)
2. Follow the procedure mentioned in [Section 7.3.1.3](#) to seamlessly switch from one mode to another.
3. In addition, follow the guidelines mention in [Section 7.3.1.3.7](#) to program any additional register bits which might be needed to control the power cycling differently between the PPG mode and the ECG/Mixed acquisition modes.

7.3.1.3.2 Analog-to-Digital Converter (ADC)

The AFE has separate signal chains for ECG and PPG that share the common ADC as shown in [Figure 7-7](#).

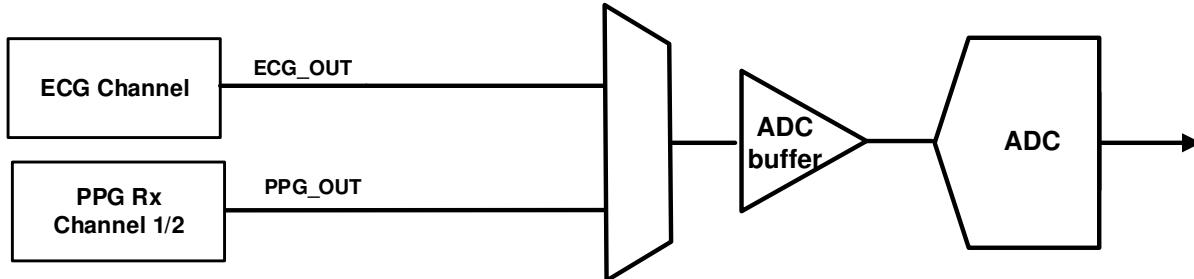


Figure 7-7. Interface of the Three Signal Chains to the Common ADC

The ADC provides a 22-bit representation of the voltage input to the device in the ECG time slot, or in the conversion phases of a PPG phase window. The ADC code can be read out from 24-bit registers in two's complement format. The ADC full-scale input range ($\pm FS$) is nominally ± 1.2 V and spans bits 21 to 0. The mapping of the ADC input voltage to the ADC code is shown in [Table 7-8](#).

Table 7-8. Mapping the ADC Input Voltage to the ADC Code

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT	24-BIT ADC OUTPUT CODE
$-FS$	11100000000000000000000000000000
$(-FS / 2^{21})$	11111111111111111111111111111111
0	00000000000000000000000000000000
$(FS / 2^{21})$	00000000000000000000000000000001
FS	00011111111111111111111111111111

When the input exceeds the full-scale levels, the output code saturates. For the ADC conversion of the PPG signal, the exact saturation value depends on the NUMAV setting. For different NUMAV settings, the saturation value on the positive side is between 1FFF19h and 1FFFFFh and the saturation value on the negative side is between E080E7h and E00000h. This kind of saturation behavior is applicable to the data corresponding to an individual conversion phase (for example, the LED or the Ambient data). The behavior of the (LED—Ambient) data are different from the one outlined above.

For the (LED—Ambient) data, the two MSBs of the 24-bit word serve as sign-extension bits to the 22-bit ADC code, and are equal to the MSB of the 22-bit ADC code when the input to the ADC is within the full-scale range, as shown in [Table 7-9](#).

Table 7-9. Using Sign-Extension bits to Determine the Input Operating Voltage

Bits 23-21 ⁽¹⁾	INPUT STATUS
000	Positive and lower than positive full-scale (within full-scale range)
111	Negative and higher than negative full-scale (within full-scale range)
001	Positive and higher than positive full-scale (outside full-scale range)
110	Negative and lower than negative full-scale (outside full-scale range)

(1) Note that D23 gets replaced by the Frame sync indicator bit when MODE_EN_FRAME_SYNC mode is set.

While the full scale range of the ADC is $\pm 1.2V$, the usable (operating) range of the ADC is limited as shown in [Table 7-10](#). The front-end gains in the signal chains can be adjusted to make sure that the ADC output code (coming out of the FIFO) stays within the indicated usable range.

Table 7-10. Usable (operating) Range of the ADC for Different Signal Acquisitions

Signal being converted by the ADC	Usable range of the ADC
PPG	$\pm 1V$
ECG	$\pm 1V$

7.3.1.3.3 Signal acquisition in PPG acquisition mode

The acquisition of PPG signals happens in well-defined PPG phase windows. The *PPG phase windows* are arranged in a contiguous manner and their entire time span of all the PPG phase windows is referred to as the *PPG signal acquisition window (PSAW)* as shown in [Figure 7-8](#). In the PPG acquisition mode, there is only one PPG signal acquisition window that contains all the PPG phase windows in each PRF cycle. Each PPG phase window can be configured to acquire either one or two PPG signal samples (a *signal* is defined by a combination of LEDs and PDs) based on whether the PPG phase is configured as a Single Receive phase or a Dual Receive phase.

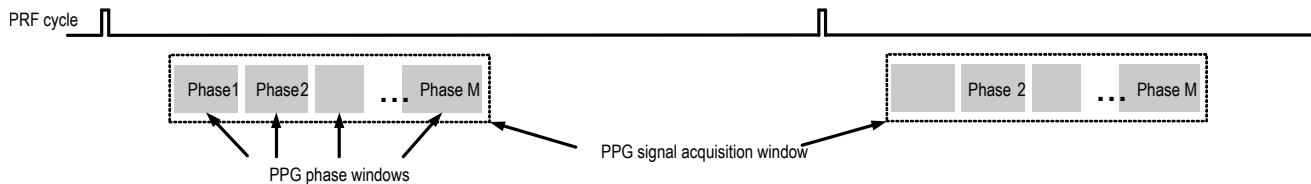


Figure 7-8. PPG Signal acquisition window in PPG acquisition mode

The number of active phases is set by a parameter called *NUMPHASE*. The register control `REG_NUMPHASE_PPG` (programmable from 0 to 23) determines *NUMPHASE* as $(\text{REG_NUMPHASE_PPG} + 1)$. There is a separate set of phase configuration registers associated with each phase# (total of 24 such sets). The phase configuration registers can be programmed to indicate the signal chain configuration and parameters corresponding to each phase

When operating in the PPG acquisition mode, the AFE goes through an automatic power cycling every PRF cycle, enabling extremely low power operation. The PRF cycle is split into three portions corresponding to Active state, Deep Sleep state and an in-between state termed as a Wake-up/Light sleep state. The positioning of the PPG phase windows within the active window of the PRF cycle as well as the timing of the Active and Deep sleep windows is shown in [Figure 7-9](#). The Phase timing engine automatically generates all the signals required for the transmit and receive operations within the PPG phase windows. Window #M contains within it the CONV signal(s) corresponding to Phase M and the LED ON signal corresponding to Phase (M+1). A programmable parameter t_{SEP} can be set to delay the start of each window.

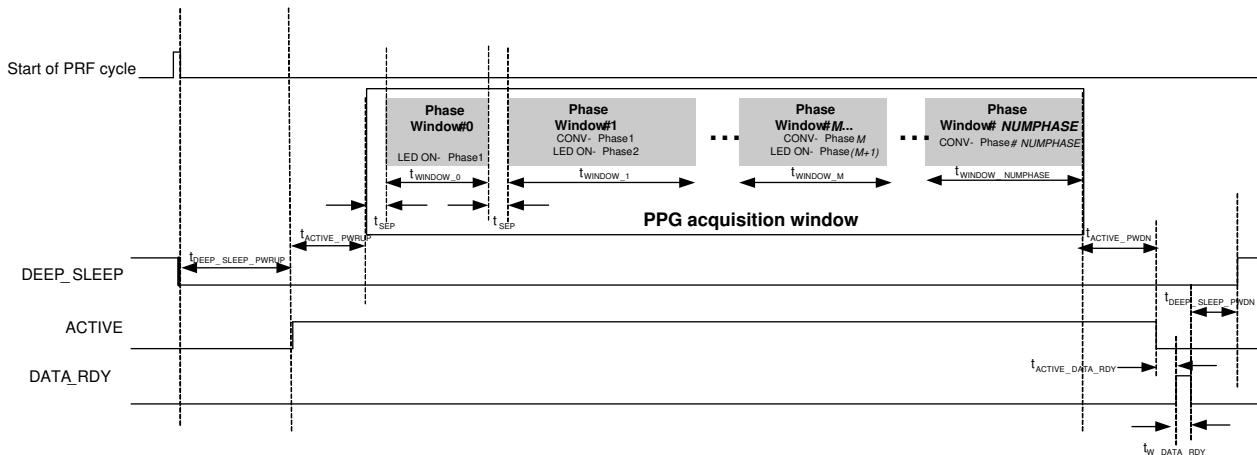


Figure 7-9. Definition of active, deep sleep and PPG signal acquisition phase and PPG phase windows within a PRF cycle while operating in PPG acquisition mode

The register control for setting the timing parameters shown in Figure 7-9 are listed in [Table 7-11](#).

Table 7-11. Timing Parameters Associated With The Various Timing Windows

Parameter ⁽¹⁾	Description	Set using register	Min	Default	Unit
$t_{DEEP_SLEEP_PWRUP}$	Start of PRF cycle to the start of Active phase	$(REG_TDEEP_SLEEP_PWRUP^{(2)} + 4) \times t_{TE}$	200	$26 \times t_{TE}$	μs
t_{ACTIVE_PWRUP}	Start of Active phase to the start of t_{SEP} window of Window #0	$(REG_TACTIVE_PWRUP^{(2)} + 1) \times t_{TE}$	300	$39 \times t_{TE}$	μs
t_{SEP}	Separation between successive windows	$REG_TSEP^{(2)} \times t_{TE}$	0	0	μs
t_{ACTIVE_PWDN}	End of Window #NUMPHASE to end of Active phase	$(REG_TACTIVE_PWDN^{(2)} + 2) \times t_{TE}$	Max (3 $\times t_{TE}$, 23.4375)	$3 \times t_{TE}$	μs
$t_{ACTIVE_DATA_RDY}$	End of Active phase to start of DATA_RDY pulse	$(REG_TACTIVE_DATA_RDY^{(2)} + 1) \times t_{TE}$	Max (4 $\times t_{TE}$, 31.25)	$4 \times t_{TE}$	μs
$t_{W_DATA_RDY}$	Width of DATA_RDY pulse	$(REG_TW_DATA_RDY^{(2)} + 1) \times t_{TE}$	$1 \times t_{TE}$	$1 \times t_{TE}$	μs
$t_{DEEP_SLEEP_PWDN}$	DATA_RDY fall to start of Deep Sleep window	$(REG_TDEEP_SLEEP_PWDN^{(2)} + 1) \times t_{TE}$	$6 \times t_{TE}$	$6 \times t_{TE}$	μs

(1) Throughout this table, t_{TE} refers to one clock period of the 128 kHz clock

(2) Global control

7.3.1.3.4 Power cycling in the PPG acquisition modes

When operating in the PPG acquisition mode at low PRF or low NUMPHASE, the active window duration is a small fraction of the PRF period. With default values for all the parameters listed in [Table 7-11](#), there is enough time for the device to cycle between the Deep sleep, Light sleep and Active states of the PRF cycle, thereby saving power. This is depicted in [Figure 7-10](#).



Figure 7-10. Power Cycling Scheme For PPG Signal Acquisition Mode At Low PRF

When operating in the PPG acquisition mode at high PRF or high NUMPHASE, there may be insufficient time for the device to transition in and out of the Deep sleep state. The power cycling can be disabled using the following register controls:

- Set register bit DIS_DEEP_SLEEP to '1' to disable the Deep sleep state

- Set registers REG_TDEEP_SLEEP_PWRUP, REG_TACTIVE_PWRUP, REG_TACTIVE_PWDN, REG_TDEEP_SLEEP_PWDN to 0 so as to minimize the time spent in the Wake-up state
- Change the REG_ACTIVE_CONTROLS register from its default value of 024880h to 0E48DBh

The above configuration results in a Power cycling scheme as shown in [Figure 7-11](#).



Figure 7-11. Power cycling scheme for PPG signal acquisition mode at high PRF

7.3.1.3.5 Signal Acquisition In Mixed Acquisition Mode

In the Mixed acquisition mode, the entire PRF is partitioned into acquisition windows for PPG and ECG. One or more *ECG Signal Acquisition Window (ESAW)* and one or more *PPG signal acquisition window (PSAW)* can be defined in a PRF cycle. Each PSAW can have one or more PPG phase windows. The total number of PPG phase windows across the multiple PPG signal acquisition windows is limited to a maximum value of 24 similar to the PPG acquisition mode. Each ESAW results in one ECG signal sample. The PSAWs and ESAWs can be arranged in an arbitrary manner within the PRF cycle. A couple of use cases are listed below:

- Case (i): ECG and PPG sampling rates are both equal to the PRF rate
- Case (ii): ECG sampling rate is a multiple (for example, 2X) of the PRF rate, PPG sampling rate is equal to the PRF rate

Case (i) is shown in [Figure 7-12](#). Only 1 ESAW is defined per PRF cycle. Also all PPG phase windows are contained within a single PSAW.

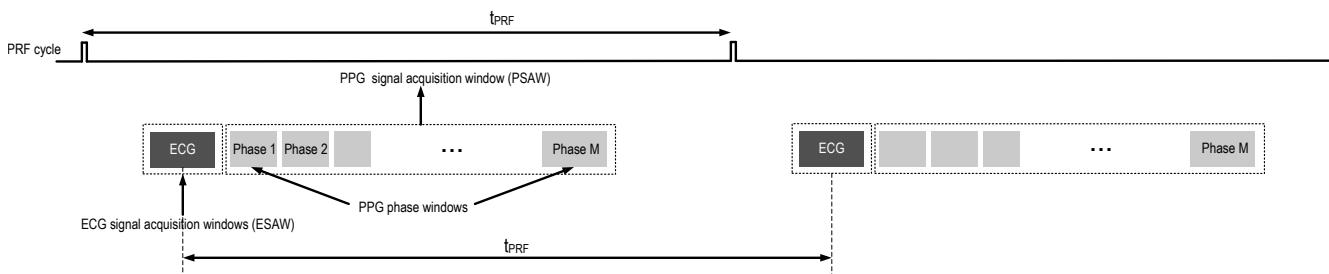


Figure 7-12. Mixed acquisition mode with ECG sampling rate equal to PRF rate

Case (ii) is shown in [Figure 7-13](#). In this case, two ECG signal acquisition windows are defined per PRF cycle and spaced $t_{PRF}/2$ apart. Two PPG signal acquisition windows are defined per PRF cycle. PPG phase windows #1 to #L are accommodated within the first PSAW, and PPG phase windows #(L+1) to #M are accommodated within the second PSAW.

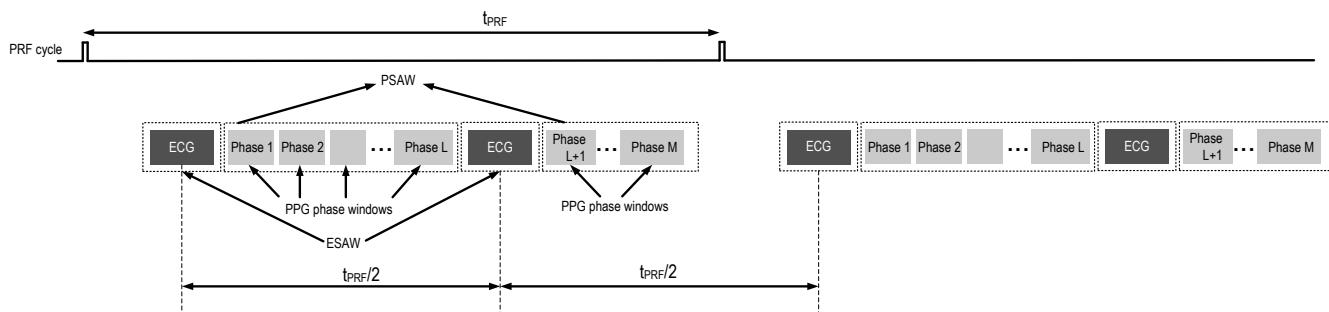


Figure 7-13. Mixed acquisition mode with ECG sampling rate equal to 2X of PRF rate

Case (ii) could also be extended to a case where the ECG sampling rate is even higher (eg. 4X of the PRF rate). Note that in the Mixed acquisition mode, just as in the PPG mode, the programmed PRF rate corresponds to the acquisition rate of the PPG signal(s).

The PRF cycle in the Mixed acquisition mode is partitioned into well-defined acquisition time slots. Each acquisition time slot is generated through 32 counts of the timing engine clock. For illustration, let us assume that the clock frequency used by the timing engine is exactly 128 kHz. A time slot is therefore $\sim 250 \mu\text{s}$ wide corresponding to 32 counts of the 128 kHz clock. While operating in the Mixed acquisition mode, it is essential to use a timing engine clock close to 128 kHz so as to maintain the width of the acquisition time slots close to 250 μs . It is also essential to set a PRF count such that the PRF period spans an integer number of acquisition time slots. These constraints rule out operation in the Single shot clocking and Mixed clock mode as these modes involve mutually independent mechanisms for setting the PRF period and clocking the timing engine. However, the Synchronous Mixed clock mode has a mechanism for the synchronization of these two clocks – specifically, a mechanism to make the internal oscillator's frequency to be equal to four times the external clock frequency. For example, when operating in the Synchronous mixed clock mode with a 32.768 kHz external clock, the timing engine clock is made equal to 131.072 kHz resulting in a time slot width of $\sim 244 \mu\text{s}$.

The ECG and PPG acquisition windows can be imprinted on to a repeating pattern of 8 time slots by setting the Time slot specification bit, CONFIG_TSM_MIX register bits (where M denotes the time slot #0 to #7). For example, CONFIG_TS0_MIX specifies the configuration in Time slot TS0. Each of these time slots can be configured to be a PPG time slot, an ECG time slot or a Blank time slot (where no signal acquisition takes place) as shown in [Table 7-12](#).

Table 7-12. PRF Time Slot Configuration In The Mixed Acquisition Mode

CONFIG_TSM_MIX M = 0,1..7	Description
000	Blank. This time slot is not used for any sensor.
001	ECG
010	PPG

The last time slot in the PRF period is forced to be a *Reserved Blank (RES_BLANK)* time slot. The 32 counts corresponding to the RES_BLANK time slot are split as 24 counts (187.5 μs) at the end of the PRF cycle and 8 counts (62.5 μs) at the beginning of the next PRF cycle

[Figure 7-14](#) shows the pattern of the 8 time slots and Reserved Blank time slot for the case where the PRF period is set to 2.25 ms (equal to exactly 9 time slots). The black cells at the start and end correspond to the two parts of the RES_BLANK time slot.

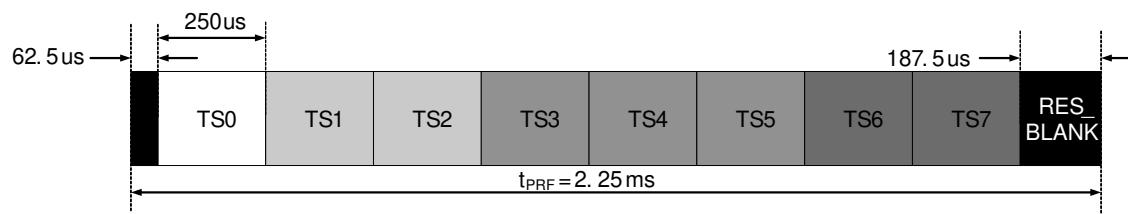


Figure 7-14. Time slots for a case where the PRF period is 2.25 ms

The PPG signal chain transitions into the Active start at the start of the PRF cycle and the segment of the RES_BLANK at the start of the PRF cycle serves as settling time for the PPG active state to stabilize.

Note

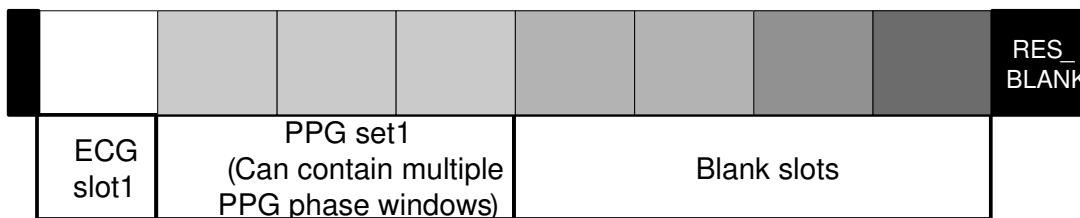
The device enters a low power state towards the end of the PRF cycle and recovers from this state to get into an active state at the beginning of the new PRF cycle. As a result, there might be slight performance loss for the signal acquisition during the TS0 time slot. To prevent such a performance loss, set the DIS_BUF_PDN_ON_ADC bit to 1. This bit disables the powering down of the ADC buffer after the active time slots of the PRF cycle.

[Table 7-13](#) shows an example definition of time slots as ECG, PPG and Blank slots

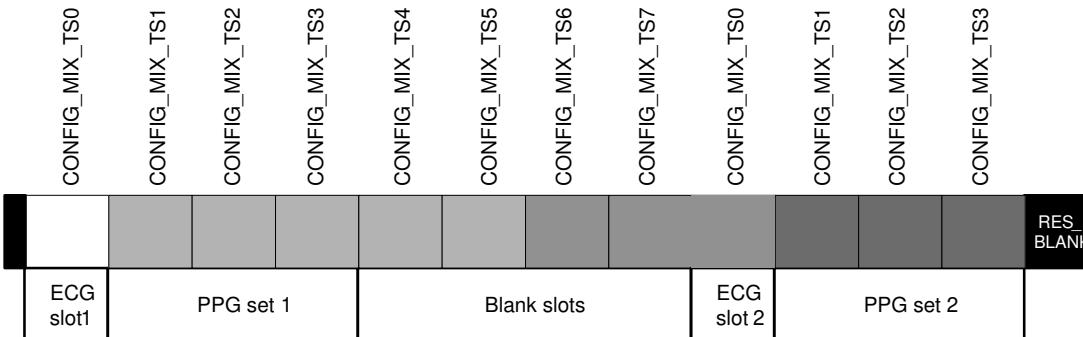
Table 7-13. An Example Definition Of Time Slots

Time slot specification register bit	Time slot type	Comment
CONFIG_TS0_MIX	ECG	-
CONFIG_TS1_MIX	PPG	
CONFIG_TS2_MIX	PPG	Time slots #1,2,3 comprises a PPG window1
CONFIG_TS3_MIX	PPG	
CONFIG_TS4_MIX	Blank	-
CONFIG_TS5_MIX	Blank	-
CONFIG_TS6_MIX	Blank	-
CONFIG_TS7_MIX	Blank	-

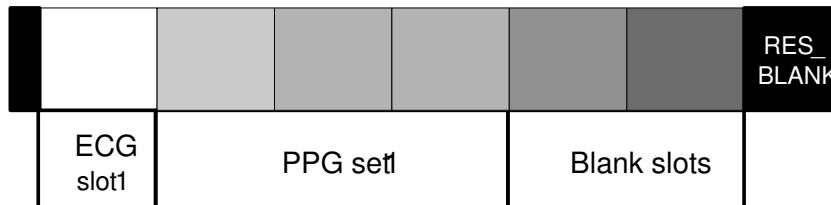
Figure 7-15 shows the ECG and PPG slots corresponding to the case in Figure 15 for the time slots as allocated in Table 7-13

**Figure 7-15. ECG and PPG windows when PRF period is 2.25 ms**

When the PRF period is set higher than 2.25 ms (but still a multiple of 250 µs), the time slots definitions repeat. Figure 7-16 shows the ECG and PPG windows corresponding to the time slot definition in Table 10 but with the PRF period set to 3.25 ms. The repeating pattern of grey shaded cells corresponds to the pattern of the 8 configurations set by CONFIG_TS0_MIX..CONFIG_TS7_MIX.

**Figure 7-16. ECG and PPG windows when PRF period is 3.25 ms**

When the PRF period is set lower than 2.25 ms (but still a multiple of 250 µs), the time slots definition pattern gets truncated. Figure 7-17 shows the ECG and PPG windows corresponding to the time slot definition in Table 10 but with the PRF set to 1.75 ms. As can be seen, only time slots TS0..TS5 are generated apart from the RES_BLANK time slot.

**Figure 7-17. ECG and PPG windows when PRF period is 1.75 ms**

Another set of time slot allocations is shown in [Table 7-14](#). Here, the PRF period is set to 2 m, which accommodates 7 time slots apart from the RES_BLANK time slot.

Table 7-14. Another example definition of time slots

Time slot specification bit	Time slot type	Comment
CONFIG_TS0_MIX	ECG	ECG window 1
CONFIG_TS1_MIX	PPG	Time slots #1,2,3 comprises PPG window 1
CONFIG_TS2_MIX	PPG	
CONFIG_TS3_MIX	PPG	
CONFIG_TS4_MIX	ECG	ECG window 2
CONFIG_TS5_MIX	PPG	Time slots #5,6 comprises PPG window 2
CONFIG_TS6_MIX	PPG	
CONFIG_TS7_MIX	PPG	Set as a PPG time slot but TS7 is not used for 2 ms PRF period

[Figure 7-18](#) shows the ECG and PPG windows for this case. TS7 does not appear in the sequence.

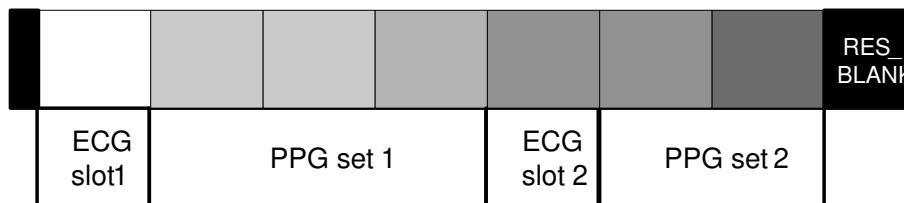


Figure 7-18. ECG and PPG windows for Table 7-14, PRF period is 2 ms

As shown, there are two ECG windows per PRF cycle (each spaced by half the PRF period). Also there are two PPG windows. Each PPG window can have a different set of phases windows.

Consider a case ([Figure 7-19](#)) where the time slot allocation is as shown in Table 12 but the PRF period is set to 6 ms.

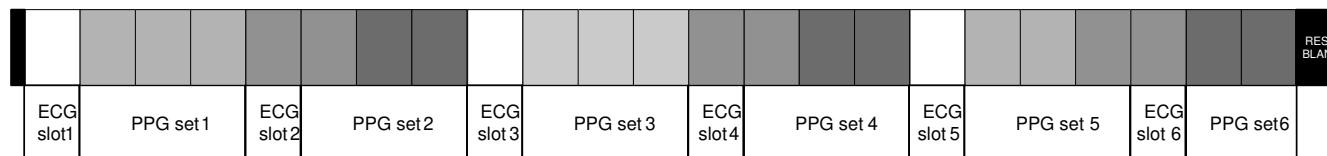


Figure 7-19. ECG and PPG signal acquisition windows for Table 12, PRF period is 6 ms

For this case, there are 6 ECG slots (all equally spaced) per PRF cycle. Also there are 6 sets of PPG slots per PRF cycle – each set occupying 4 slots except Set6 which is truncated to 3 slots. This example is used to illustrate the full level of configurability of ECG and PPG signal acquisition possible in the device. Out of all the available ECG slots in the PRF cycle, the number of active ECG signal acquisition windows(ESAW) in the PRF cycle can be specified by a parameter NUM_ESAW_MIX, which can take values from 1 to 64. NUM_ESAW_MIX is set through a register REG_NUM_ESAW_MIX as (REG_NUM_ESAW_MIX+1). For example, setting REG_NUM_ESAW_MIX to 5 causes the ECG signal to get acquired in all the 6 ECG slots of [Figure 7-19](#). On the other hand, setting REG_NUM_ESAW_MIX to 1 causes the ECG signal to get acquired only in the first two ECG slots.

The number of active PPG signal acquisition windows in the PRF cycle can be specified by a parameter NUM_PSAW_MIX which can take values from 1 to 4. NUM_PSAW_MIX is set through a register REG_NUM_PSAW_MIX as (REG_NUM_PSAW_MIX+1). For example, setting REG_NUM_PSAW_MIX to 3 results in the PPG sets 1 to 4 of [Figure 7-19](#) to all have PPG phases contained in them. On the other hand, setting REG_NUM_PSAW_MIX to 1 results in only PPG sets 1 to 2 to have PPG phases contained in them. Note that the number of PSAWs in a PRF cycle is limited to 4. Therefore, even for the case where

REG_NUM_PSAW_MIX is set to its maximum value of 3, the PPG set#5 and #6 are unusable and become blank slots.

The total number of PPG phases spread over the multiple(up to 4) PSAWs is limited to 24. The starting phase # and the number of phases for each of the 4 PSAWs can be programmed as shown in [Table 7-15](#). The starting phase# in PSAWx (x = 1 to 4) is a parameter START_PH_PSAWx which is set as (REG_START_PH_PSWAx), and the Number of phases in the PSAWx is a parameter NUM_PH_PSAWx which is set as (REG_NUM_PH_PSAWx). The flexibility in specifying the starting phase# provides in the Mixed acquisition mode a flexibility to reference a set of PPG phase numbers different from those used in the PPG acquisition mode (thereby allowing for independent PPG phase definitions between the two acquisition modes). For example, if the PPG acquisition mode uses 10 phases (NUMPHASE = 9), then the Mixed acquisition mode can either reference the same set of 10 phases or can reference a different set of phases starting from Phase #11 (the case shown in [Table 7-15](#)).

Table 7-15. Specification Of Phase Windows Within The 4 PPG Signal Acquisition Windows

PPG Signal acquisition window#	Register for Start phase #			Register for Number of phases	
	Register setting	Example setting	Register setting	Example setting	
PSAW1	REG_START_PH_PSAW1	10	REG_NUM_PH_PSAW1	2	
PSAW2	REG_START_PH_PSAW2	12	REG_NUM_PH_PSAW2	2	
PSAW3	REG_START_PH_PSAW3	14	REG_NUM_PH_PSAW3	3	
PSAW4	REG_START_PH_PSAW4	17	REG_NUM_PH_PSAW4	1	

[Figure 7-20](#) shows the signal acquisition scheme for the case corresponding to [Figure 7-19](#), with NUM_ESAW_MIX set to 2 and NUM_PSAW_MIX set to 4, and the phase windows as specified in [Table 7-14](#), [Table 7-15](#). The blue boxes correspond to the different PPG phases windows with the number denoting the phase number. The signal chain settings used for a phase are derived from the per-phase register set corresponding to that phase #.

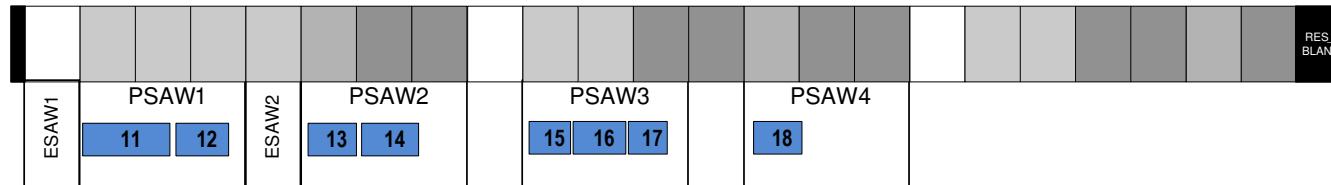


Figure 7-20. ECG and PPG signal acquisition scheme corresponding to Figure 7-19, with NUM_ESAW_MIX set to 2 and NUM_PSAW_MIX set to 4, and the phase windows as specified in Table 7-15

The PSAW and ESAW definitions for a few different use cases are shown in [Figure 7-21](#) and [Figure 7-22](#). [Figure 7-21](#) corresponds to a case where the timing engine clock is exactly 128 kHz and both the ECG and PPG signal acquisition rates are 500 Hz (note that when operating in the Synchronous mixed clock mode with a 32.768 kHz clock, the corresponding PRF would be equal to 512 Hz).

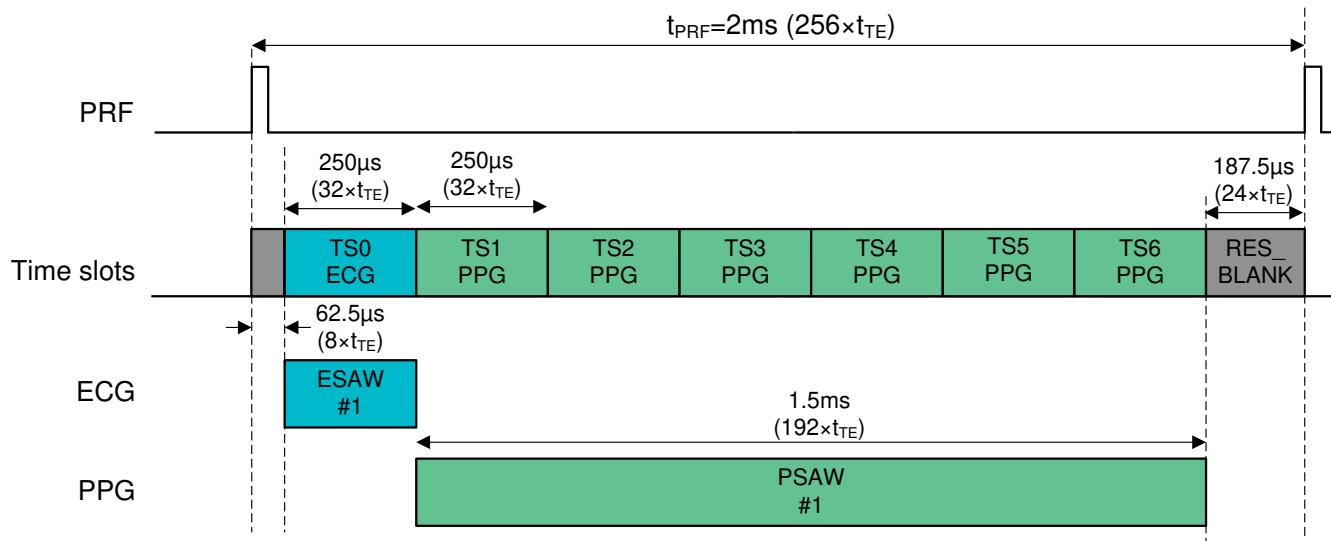


Figure 7-21. Multi-sensor mode PRF timing diagram. In this example PRF = 500 Hz

Figure 7-22 corresponds to a case where the PPG signal acquisition rate is 250 Hz and the ECG signal acquisition rate is 1 kHz. The PRF is set to 250Hz. Time Slots TS0, TS4 are defined as ECG slots and TS1, TS2, TS3, TS5, TS6, and TS7 are defined as PPG slots. Up to 4 PSAWs can be defined in this case, each containing a different set of PPG phase windows.

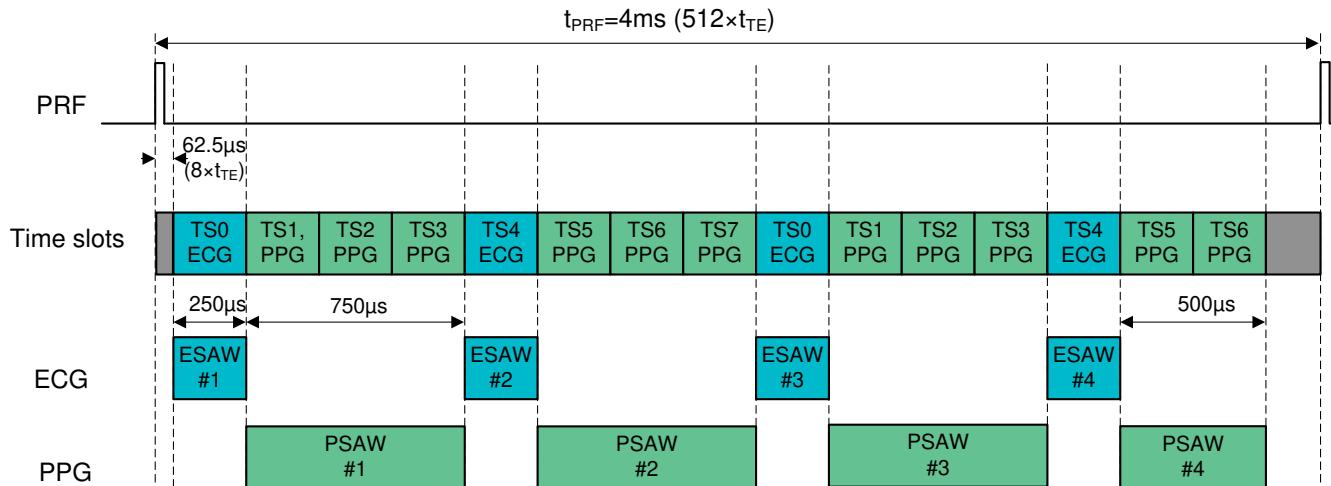


Figure 7-22. Multi-sensor mode PRF timing diagram. In this example PRF = 250 Hz

At the beginning of the PRF cycle, the ADC and TIA are powered up (internal signals ACTIVE_ADC and ACTIVE_TIA1 go high). After the active time slots in a PRF cycle are completed, the ADC and TIA are powered down, and the AFE enters a deep sleep state (internal signal DEEPSLEEP goes high). Figure 7-23 shows a timing diagram with these signals for a case corresponding to 500 Hz PRF. The RES_BLANK time slot section at the end of the PRF cycle is shown elongated to illustrate the details of the timing better.

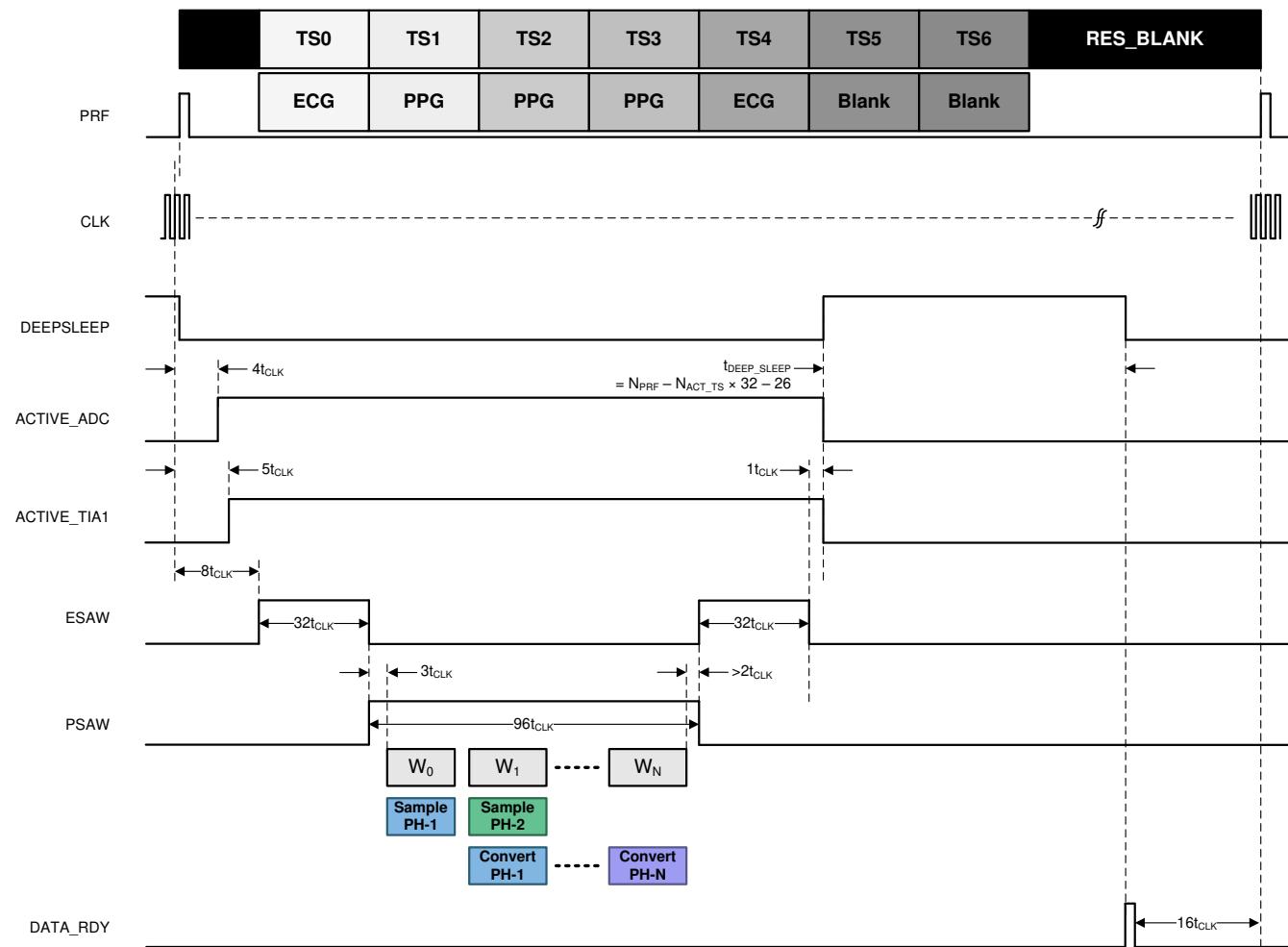


Figure 7-23. Timing of the Dynamic Active and Power-down Signals in Mixed Acquisition Mode

7.3.1.3.6 Signal Acquisition in ECG Acquisition Mode

The ECG acquisition mode works similar to the Mixed acquisition mode in terms of ECG signal acquisition but with the difference being that PPG is not supported. Each of 8 time slots can be defined as either a blank time slot or an ECG time slot using the CONFIG_TSM_ECG register control as shown in [Table 7-16](#). For example, CONFIG_TS0_ECG specifies the configuration in Time slot TS0. The number of ECG windows in the PRF cycle (NUM_ESAW_ECG) can be set using the register control REG_NUM_ESAW_ECG as (REG_NUM_ESAW_ECG+1).

Note

When operating in ECG acquisition mode, set the PDN_TIA1_STATIC bit to '1' to power down the TIA and save power.

Table 7-16. PRF Time Slot Configuration In ECG Acquisition Mode

CONFIG_TSM_ECG M = 0,1..7	Description
000	Blank. This time slot is not used for any sensor
001	ECG

[Figure 7-24](#) shows an example with PRF = 500 Hz and ECG sample rate = 2 kHz. Time slots TS0, TS2, TS4, TS6 are defined as ECG slots by setting CONFIG_TS0_ECG, CONFIG_TS2_ECG, CONFIG_TS4_ECG and CONFIG_TS6_ECG to '001'. In this example, REG_NUM_ESAW_ECG is set to 3 (thereby setting the number of ESAW in a PRF cycle to 4).

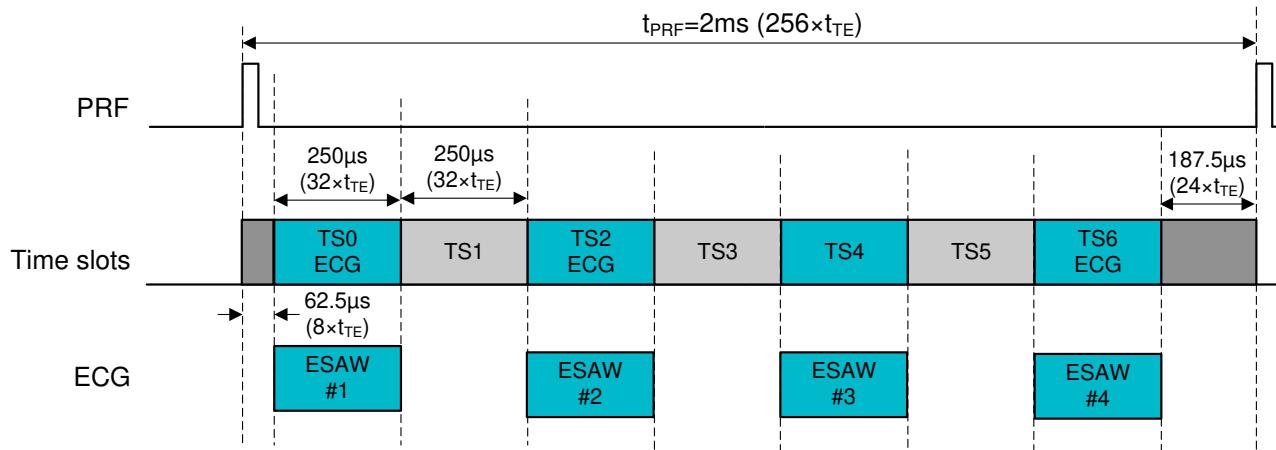


Figure 7-24. ECG Mode PRF Timing Diagram - PRF = 500 Hz

Table 7-17 shows a summary of the register controls for the three acquisition modes.

Table 7-17. Register Controls For Different Acquisition Modes

Register	PPG Acquisition mode	Mixed Acquisition mode	ECG Acquisition mode
PRF frequency	REG_PRPCT_PPG	REG_PRPCT_MIX	REG_PRPCT_ECG
Configuration of time slot (TS) #M M = 0 to 7	N/A	CONFIG_TSM_MIX	CONFIG_TSM_ECG
Number of PSAW in a PRF cycle	1	NUM_PSAW_MIX	N/A
# PPG phases in PSAW1	REG_NUMPHASE_PPG	REG_NUM_PH_PSAW1	N/A
Starting PPG phase # in PSAW1	1	REG_START_PH_PSAW1	N/A
# PPG phases in PSAW2	N/A	REG_NUM_PH_PSAW2	N/A
Starting PPG phase # in PSAW2	N/A	REG_START_PH_PSAW2	N/A
# PPG phases in PSAW3	N/A	REG_NUM_PH_PSAW3	N/A
Starting PPG phase # in PSAW3	N/A	REG_START_PH_PSAW3	N/A
# PPG phases in PSAW4	N/A	REG_NUM_PH_PSAW4	N/A
Starting PPG phase # in PSAW4	N/A	REG_START_PH_PSAW4	N/A
Number of ESAW in a PRF cycle	N/A	REG_NUM_ESAW_MIX	REG_NUM_ESAW_ECG

7.3.1.3.7 Power cycling in the Mixed Acquisition and ECG Acquisition Modes

The different power cycling controls are listed in [Table 7-18](#). The power cycling controls for the various blocks are controlled by a register word REG_ACTIVE_CONTROLS as listed in [Table 7-19](#).

Table 7-18. Power Cycling Controls for the PPG, ECG and Mixed Acquisition Modes

Register control	PPG acquisition mode		Mixed acquisition mode		ECG acquisition mode
	PPG at Low PRF	PPG at High PRF	PPG at Low PRF	PPG at High PRF	
Set DIS_DEEP_SLEEP to '1'	No	Yes	Don't care	Don't care	Don't care
Set REG_TDEEP_SLEEP_PWRUP, REG_TACTIVE_PWRUP, REG_TACTIVE_PWDN to 0	No	Yes	Don't care	Don't care	Don't care
Program REG_ACTIVE_CONTROLS to 0E48DBh	No	Yes	No	Yes	Don't care
CONNECT_BG_TO_PIN	Set same as DIS_DEEP_SLEEP		1	1	1

Table 7-19. Constituents of REG_ACTIVE_CONTROLS Register Word

Bits	Name	Function	REG_ACTIVE_CONTROLS Setting		
			024880h (Default)	0E48DBh	026C80h
D23..D21	FIXED_CTRL1	Always write '000'	000	000	000
D20..D18	TX_ACT_CTRL	-	000	011	000
D17..D15	FIXED_CTRL2	Always write '100'	100	100	100
D14..D9	INA_ACT_CTRL	INA dynamic power down control in PPG mode: 100100: Powered down in PPG mode 110110: Powered down in Deep sleep Other settings: Do not use	100100	100100	110110
D8..D6	ADC_ACT_CTRL	ADC dynamic power down control: 010: Powered down in Deep sleep 011: No power cycling Other settings: Do not use	010	011	010
D5..D3	TIA2_ACT_CTRL	TIA2 dynamic power down control: 000: Powered down in Deep sleep 011: No power cycling Other settings: Do not use	000	011	000
D2..D0	TIA1_ACT_CTRL	TIA1 dynamic power down control: 000: Powered down in Deep sleep 011: No power cycling Other settings: Do not use	000	011	000

7.3.1.4 Data Rate Controls for PPG and ECG Signals

The system may require acquisition of PPG and ECG signals at different acquisition rates and/or different output data rates. Additionally, PPG signals acquired from different sensors may require to be at different rates. The mechanisms and their controls to set different rates for different signals are summarized in [Table 7-20](#)

Table 7-20. Mechanisms for setting different data rates

Mechanism	Register control	Acquisition Mode			Rate	
		PPG	MIXED	ECG	Sampling rate	Output data
Defining multiple ESAW in a PRF cycle	REG_NUM_ESAW_W_MIX		X		ECG rate = PRF*NUM_ESAW_MIX (NUM_ESAW_MIX=REG_NUM_ESAW_MIX+1)	
	REG_NUM_ESAW_W_ECG				ECG rate = PRF*NUM_ESAW_ECG (NUM_ESAW_ECG=REG_NUM_ESAW_ECG+1)	
Global PPG masking (of all PPG phases)	Global mask factor REG_PPG_GBL_MASK_FACTOR		X		PPG phases rate = PRF/PPG_GBL_MASK_FACTOR (PPG_GBL_MASK_FATOR=REG_PPG_GBL_MASK_FATOR+1) REG_PPG_GBL_MASK_FATOR should be set to '0' in PPG acquisition mode	
Per-phase PPG Masking – mask each PPG phase selectively	Per-phase PPG mask factor REG_PH_MASK_FACTOR	X			Phase-specific PPG rate = PRF/PH_MASK_FACTOR (PH_MASK_FACTOR = $2^{REG_PH_MASK_FACTOR}$)	
PPG phase Decimation	PPG Decimation factor REG_PPG_DECx_FACTOR (x = 1..8 for the eight decimation filters)	X	X	PRF	Decimated PPG phase rate = PRF/PPG_DECx_FACTOR (PPG_DECx_FACTOR = $2^{REG_PPG_DECx_FACTOR+1}$)	
ECG phase Decimation	REG_ECG_DEC_FACTOR_MIX		X		PRF	ECG rate = PRF/MIX_ECG_DEC_FACTOR (MIX_ECG_DEC_FACTOR = $2^{REG_MIX_ECG_DEC_FACTOR+1}$)
	REG_ECG_DEC_FACTOR_ECG			PRF		ECG rate = PRF/ECG_DEC_FACTOR (ECG_DEC_FACTOR = $2^{REG_ECG_DEC_FACTOR_ECG+1}$)

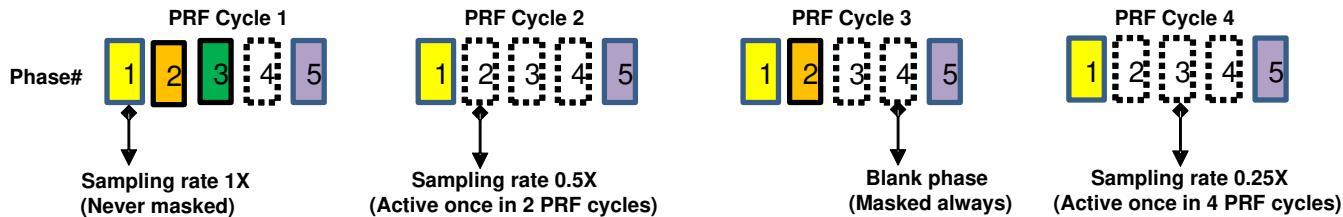
7.3.1.4.1 PPG Phase Masking

By default, each defined PPG phase in a PRF cycle results in a signal acquisition and generation of a data word. The data rate of each PPG signal is equal to the PRF rate. While operating in the PPG acquisition mode, a Per-phase PPG masking mode can be programmed individually for each PPG phase to control the signal acquisition (and output data) rate for that phase relative to the PRF. [Table 7-21](#) lists the Per-phase PPG masking modes that can be programmed through per-phase register control REG_PH_MASK_FACTOR. When a PPG phase is masked, signals for that phase continue to occupy the designated timeslots but do not perform any associated operations (operations like the LEDs turning on or the ADC converting). Also, a masked phase does not result in a FIFO sample in the PRF cycle where it is masked.

Table 7-21. Masking controls for a PPG phase

REG_PH_MASK_FACTOR	MASKING MODE	MASKING FACTOR PH_MASK_FACTOR	COMMENTS
0	Never mask	1	Never mask the phase
1	2X	2	Mask phase the last cycle of every 2 PRF cycles
2	4X	4	Mask phase the last 3 cycles of every 4 PRF cycles
...			
M	$2^M X$	2^M	Mask phase the last (2^M-1) cycles of every 2^M PRF cycles
...			
10	1024X	1024	Mask phase the last 1023 cycles of every 1024 PRF cycles
11-15	Always mask		Always mask the phase

Figure 7-25 shows an example where Phase 1 and Phase 5 are never masked), Phase 2 is set to 2X masking, Phase 3 is set to 4X masking and Phase 4 is always masked.

**Figure 7-25. Illustration of masking modes**

By default, the first PRF cycle of the repeating sequence contains the unmasked PPG phase. By setting the global bit MASK_REVERSE bit to '1', the last PRF cycle of the repeating sequence can be set as the unmasked (active) phase and the initial (M-1) phases become masked phases.

The masking mode can be applied in certain use cases that include:

1. Setting acquisition rate of different PPG sensors to different values
2. Setting rate of Dummy LED phase lower than actual LED phase to limit the update rate of the LED DC cancellation loop

When using different masking factors for different phases, it is inevitable that the number of FIFO samples changes across PRF cycles. To simplify the software handling of the FIFO data, it is recommended that the watermark level be chosen such that the data from an integer number of PRF cycles fills the FIFO up to the watermark level, and the arrangement of signals up to the watermark level constitutes a repetitive pattern. Such a repetitive pattern can be used as a reference template for how a block of FIFO data needs to get split into its constituent data streams and to identify the cycles where a phase is masked. While choosing very large masking factors, it may not be always possible to meet this constraint. In such cases, the MCU should handle the additional software complexity of mapping the read block of FIFO data to the constituent data streams.

When operating in the Mixed Acquisition mode, the per-phase masking factor is ignored. A *Global PPG masking mode* can be programmed by setting a global masking factor PPG_GBL_MASK_FACTOR common for all PPG phases, which can be any integer from 1 to 64 set through register REG_PPG_GBL_MASK_FACTOR as (REG_PPG_GBL_MASK_FACTOR+1). REG_PPG_GBL_MASK_FACTOR should be set to '0' in PPG only mode

7.3.1.4.2 PPG Phase Decimation

The signal bandwidth of interest for a PPG signal is usually 20 Hz or lower. Operating at a higher data rate helps lower the noise in the bandwidth of interest and results in improved SNR. However, operating at a higher data rate also fills up the FIFO faster and results in higher FIFO readout rates which increases the system level power

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consumption. To reduce the output data rate while still achieving the in-band SNR benefits from operating at a higher acquisition rate, the AFE has a decimation feature. The decimation filter is a moving average filter which averages the successive samples from the signal and generates a data stream at a lower rate.

The device has 8 PPG decimation filters that can be enabled using the EN_PPG_DEC1..EN_PPG_DEC8 register bits. Each filter can be assigned to the data from a PPG Phase number NUMPHASE_DECx set as (REG_NUMPH_PPG_DECx +1) (register takes values from 0..23) where x refers to the filter number (x can take values from 1 to 8; example: REG_NUMPH_PPG_DEC1 specifies the phase number to associate with Decimation filter 1). The data used for decimation is same as the FIFO data specified through the FIFO_DATA_CTRL_1, FIFO_DATA_CTRL_2 for that phase. The decimation filter performs a moving average of the output code from that PPG phase across PRF cycles. By default, the decimation filter works on the data stream corresponding to the output from TIA1 from the selected phase for that filter. To select TIA2 output to decimate, set the PPG_DECx_TIA_SEL bit to 1. For example, setting NUMPHASE_DEC=1, NUMPHASE_DEC2=1, PPG_DEC1_TIA_SEL=0, PPG_DEC2_TIA_SEL=1 associates Decimation filter #1 with TIA1 data of Phase 1, and associates Decimation filter #2 with TIA2 data of Phase 1.

The averaging operation of the decimation filter is done over multiple successive PRF cycles. The number of PRF cycles over which the averaging is done is a parameter called PPG_DECx_FACTOR which can be programmed through the REG_PPG_DECx_FACTOR register control (x refers to filter number from 1..8), as shown in [Table 7-22](#).

Table 7-22. Number of Averaging Cycles (Decimation Factor) as a Function of REG_PPG_DECx_FACTOR

REG_PPG_DECx_FACTOR (x = 1..8)	NUMBER OF SAMPLES AVERAGED (Decimation Factor) PPG_DECx_FACTOR (x = 1..8)
REG_PPG_DEC1_FACTOR, REG_PPG_DEC2_FACTOR	2
REG_PPG_DEC3_FACTOR, REG_PPG_DEC4_FACTOR	4
REG_PPG_DEC5_FACTOR, REG_PPG_DEC6_FACTOR	8
REG_PPG_DEC7_FACTOR, REG_PPG_DEC8_FACTOR	16
0	32
1	Do not use
2	
3	
4	
Other settings	

When PPG decimation mode is enabled, the periodicity of the data from that PPG phase entering the FIFO automatically scales down by a factor equal to the decimation factor. For example, when the decimation factor is set to 4, the periodicity of the data from that phase becomes PRF / 4. The data enters the FIFO only every 4th PRF cycle in a manner similar to the PPG phase masking mode.

The PPG decimation controls work in the same manner for both the PPG acquisition mode as well as the Mixed acquisition mode.

Note

PPG decimation cannot be used on a PPG phase for which PPG phase masking is programmed.

7.3.1.4.3 ECG phase Decimation

The signal bandwidth of interest for a ECG signal is usually 150 Hz or lower. A decimation filter can be enabled in the data path of the ECG data stream in both the Mixed acquisition mode and the ECG acquisition mode. The decimation filter performs the moving average on the samples of ECG datastream flowing out from the ADC across the multiple ECG phases during a PRF cycle as well as across PRF cycles. To enable decimation of the ECG data-stream, associate the decimation operation with the relevant time slots (that contain ECG samples). This can be done by setting the register bits SEL_DEC_FILT_TSx_MIX (SEL_DEC_FILT_TS0_MIX.. SEL_DEC_FILT_TS7_MIX) in the case of Mixed acquisition mode or SEL_DEC_FILT_TSx_ECG (SEL_DEC_FILT_TS0_ECG.. SEL_DEC_FILT_TS7_ECG) in the case of ECG acquisition mode to '1' – here x refers to the time slot # and can take values from 0 to 7. Set the decimation factor ECG_DEC_FACTOR using the register REG_ECG_DEC_FACTOR_MIX (in the case of Mixed

acquisition mode) or REG_ECG_DEC_FACTOR_ECG (in the case of ECG acquisition mode) as shown in [Table 7-23](#).

**Table 7-23. Number of Averaging Cycles (Decimation Factor) as a Function of
REG_ECG_DEC_FACTOR_ECG**

REG_ECG_DEC_FACTOR_ECG ⁽¹⁾	ECG_DEC_FACTOR
0	2
1	4
2	8
3	16
4	32
Other settings	Do not use

- (1) In the Mixed acquisition mode, the ECG decimation factor is termed as MIX_ECG_DEC_FACTOR and controlled by REG_ECG_DEC_FACTOR_MIX

7.3.2 PPG Signal Chain

7.3.2.1 Overview

The PPG signal chain involves a synchronized operation of a transmitter (LED driver) and a receiver (an analog front end followed by an ADC). In every cycle of a PRF, up to 24 signal phases can be defined and the signal acquired. A signal phase is associated with a combination of one or more LEDs (or none) turning on, and the current signal from a PD (or the sum of currents from more than one PD) getting sampled and converted. A first in, first out (FIFO) is used to store samples from each signal phase across multiple periods. When the FIFO is enabled, the ADC_RDY pin can be configured to serve as a FIFO_RDY interrupt which indicates when the FIFO has been filled up to a programmed watermark level.

The receiver input pins (INP*, INM*) are meant to be connected differentially to a photodiode. The signal current from the photodiode is converted to a differential voltage using a trans-impedance amplifier (TIA). The AFE has 2 TIAs. By default, only 1 TIA is enabled and any combination of 4 PDs can be connected to TIA1 in each phase. A Dual TIA mode, when enabled, powers up TIA2 as well. In this mode, each phase can be configured either as a Single Receive phase (where the TIA can be selected to be either TIA1 or TIA2) or as a Dual Receive phase (where both TIAs are used). In each phase, any combination of PDs can be connected to TIA1 (and/or any combination to TIA2). The gain of each TIA is set by its feedback resistor (R_F) and can be programmed from $3.7\text{k}\Omega$ to $1\text{ M}\Omega$ (independent per-phase control for TIA1 and for TIA2). The trans-impedance gain between the input current and output differential voltage of the TIA is equal to $2 \times R_F$. At the output of the TIAs is a programmable switched RC filter which serves as a Noise Bandwidth reduction filter and helps to limit the bandwidth of the optical noise from the sensor. There are two parallel RC filters that are each connected to the TIA1 output signal during every alternate sampling phases when the phases are configured to operate as a Single Receive phase, or concurrently to the output of TIA1 and TIA2 for a Dual Receive phase. With the number of sampling phases exceeding 2 (as is usually the case), the filters get reused across multiple signal phases with a reset between phases to erase memory. The output of each filter at the end of the sampling phase is stored on a capacitor, buffered and converted by an ADC. In a Dual Receive phase, the ADC converts the output of the two filters one after the other and produces two data words, one corresponding to each TIA. The ADC output in each phase can be stored in the FIFO and read out using the SPI or I2C interface.

The AFE has an Analog Ambient Cancellation Mode loop (Analog AACM) which can be used to suppress the input ambient in a set of phases which have a common ambient. In addition, the AFE also has 4 Digital AACM loops which can be configured to optionally cancel the DC from up to 4 LED phases. Canceling the DC from the LED phase dynamically can introduce glitches in the data and so this feature needs to be used with due consideration to the effect of these glitches on the heart rate extraction. Additionally, if using the LED Offset DAC to cancel the input DC in applications like SpO₂ where an accurate DC value is also required, the cancelled DC can be accurately reconstructed by disconnecting the PD from the receiver and estimating the Offset DAC accurately.

Two 8-bit Offset Cancellation DACs at the input of each TIA can be individually programmed in each signal phase to subtract two DC currents from the incident current signal from the Photodiode. One of these DACs (IOFFDAC_AMB) is used to remove the DC current from the Ambient, and can optionally be controlled by an Automatic Ambient Cancellation loop (independent control for the Offset DAC at TIA1 and TIA2). The other Offset DAC (IOFFDAC_LED) is meant to cancel the DC current due to the LED, and can be set either by a per-phase register control or can be controlled using a LED DC Cancellation loop. By removing some or all of the DC current, a higher TIA gain can be applied to maximize the Signal to Noise ratio at the output of the AFE. The signal chain is kept fully differential throughout the receiver channel in order to enable excellent rejection of common-mode noise as well as noise on the power supplies.

The transmitter comprises of an LED current driver (realized as a pair of parallel drivers) which can be routed in a flexible manner to any combination of 8 LEDs in each phase. The current setting of both the LED drivers can be independently set for each phase. The operation of the LEDs turning on is fully synchronized with the sampling of the signal from the photodiode by the receiver.

7.3.2.2 Signal Generation in PPG Phase Windows

The timing engine inside the AFE generates all the timing signals required to turn on the LEDs, sample the PDs and do the ADC conversions. The timing engine is enabled by setting the TIMER_ENABLE register bit. Additionally program the PRF_COUNTER_ENABLE register bit to '1' to enable the PRF counter. Setting the TM_COUNT_RST optionally keeps the timing engine in a reset state.

Up to 24 phases can be defined within a PRF cycle, and each phase can be associated with a unique signal definition. The number of active phases is set by a parameter called NUMPHASE. The register control REG_NUMPHASE (programmable from 0 to 23) determines NUMPHASE as (REG_NUMPHASE+1). The Phase timing engine automatically generates all the signals required for the transmit and receive operations within well-determined windows. The positioning of the phase windows within the active phase of the PRF cycle as well as the timing of the active and deep sleep window is shown in [Figure 7-26](#). By default, each phase operates as a Single receive phase. However, with the second TIA also enabled, a phase can be configured to be either a Single Receive phase or a Dual Receive phase. When operating as a Single Receive phase, Window #M contains the CONV signal corresponding to Phase M and the LED ON signal corresponding to Phase (M+1). A programmable parameter t_{SEP} can be set to delay the start of each window.

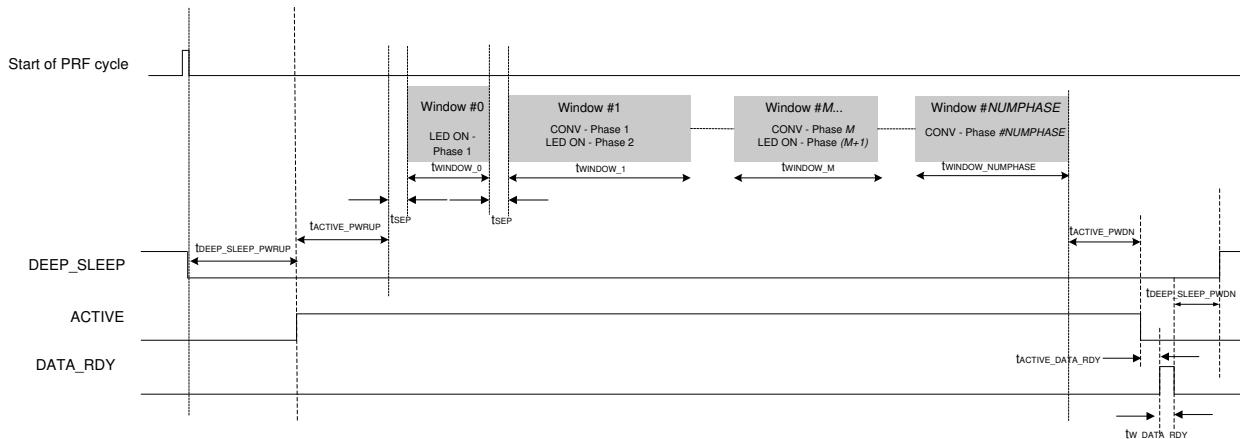


Figure 7-26. Definition of Active, Deep Sleep, and Phase Windows Within a PRF Cycle

The register control for setting the timing parameters shown in [Figure 7-26](#) are listed in [Table 7-24](#).

Table 7-24. Timing Parameters Associated With the Various Timing Windows

PARAMETER ^{(1) (3)}	DESCRIPTION	SET USING REGISTER	MIN	DEFAULT	UNIT
$t_{DEEP_SLEEP_PWRUP}$	Start of PRF cycle to the start of Active phase	$(REG_TDEEP_SLEEP_PWRUP^{(2)} + 4) \times t_{TE}$	200	$26 \times t_{TE}$	μs
t_{ACTIVE_PWRUP}	Start of Active phase to the start of t_{SEP} window of Window #0	$(REG_TACTIVE_PWRUP^{(2)} + 1) \times t_{TE}$	300	$39 \times t_{TE}$	μs
t_{SEP}	Separation between successive windows	$REG_TSEP^{(2)} \times t_{TE}$	0	0	μs
t_{ACTIVE_PWDN}	End of Window #NUMPHASE to end of Active phase	$(REG_TACTIVE_PWDN^{(2)} + 2) \times t_{TE}$	Max (3xt _{TE} ,23.4375)	$3 \times t_{TE}$	μs
$t_{ACTIVE_DATA_RDY}$	End of Active phase to start of DATA_RDY pulse	$(REG_TACTIVE_DATA_RDY^{(2)} + 1) \times t_{TE}$	Max (4xt _{TE} ,31.25)	$4 \times t_{TE}$	μs
$t_{W_DATA_RDY}$	Width of DATA_RDY pulse	$(REG_TW_DATA_RDY^{(2)} + 1) \times t_{TE}$	$1 \times t_{TE}$	$1 \times t_{TE}$	μs
$t_{DEEP_SLEEP_PWDN}$	DATA_RDY fall to start of Deep Sleep phase	$(REG_TDEEP_SLEEP_PWDN^{(2)} + 1) \times t_{TE}$	$6 \times t_{TE}$	$6 \times t_{TE}$	μs

(1) Throughout this table, t_{TE} refers to one clock period of the 128 kHz clock.

(2) Global controls.

(3) At low PRF rates, the device can be set to power cycle through the Deep sleep phase to reduce the average power, and all registers listed in this table can be kept at their default values on reset. At high PRF rates, there is not be sufficient time to power cycle the AFE through the Deep sleep state. In that case, the AFE can be kept in Active state throughout the PRF cycle using the EN_ALWAYS_ACTIVE and DIS_DEEP_SLEEP register bit. Additionally, the registers REG_TDEEP_SLEEP_PWRUP, REG_TACTIVE_PWRUP, REG_TACTIVE_PWDN, REG_TDEEP_SLEEP_PWDN can be set to 0.

Each phase is associated with LED_ON, SAMP and CONV signals. The LED_ON signal can either trigger one or more LEDs to turn on (or for all LEDs to be off for an Ambient phase). When operating as a ‘Single receive’ phase, the signal from one or more PDs can be input to TIA1, sampled across a filter during the SAMP signal, and converted by the ADC during the CONV signal. When operating as a ‘Dual receive phase’, one or more PDs can be switched to each TIA, the output of each TIA gets sampled on to a different filter during the common SAMP signal, and the sampled output on the two filters then gets converted sequentially by the ADC in two successive CONV phases.

The generation of the LED ON, SAMP and CONV signals within each timing window is automatically achieved by the Phase timing engine. The timing signals within Window #0 is shown in [Figure 7-27](#) for a case where Phase 1 is a ‘Single receive phase’ case (only a single TIA#T, T is 1 or 2, is enabled). The separation between the start of the LED_ON signal and the SAMP signal is determined by a global parameter called t_{LED_SAMP} . A filter reset window of duration equal to $t_{W_FILT_RST}$ is allocated prior to the LED ON phase. If the filter reset mode is enabled (default mode), the filter is automatically reset during the filter reset window. TI recommends to keep t_{LED_SAMP} at 0 so as to maximize the time for the filter to sample the TIA output (which tracks the LEDs turning on). By default, the SAMP signal ends at the same time as the LED_ON signal. By programming a register bit called EARLY_SAMP_FALL, the fall of SAMP can be advanced by 1 CLK_TE cycle relative to the LED_ON signal.

The EARLY_SAMP_FALL setting results in less than adequate use of the LED power but can be essential to set in case a synchronized parallel operation of two AFEs is required, with one AFE sampling an LED driven from the other AFE.

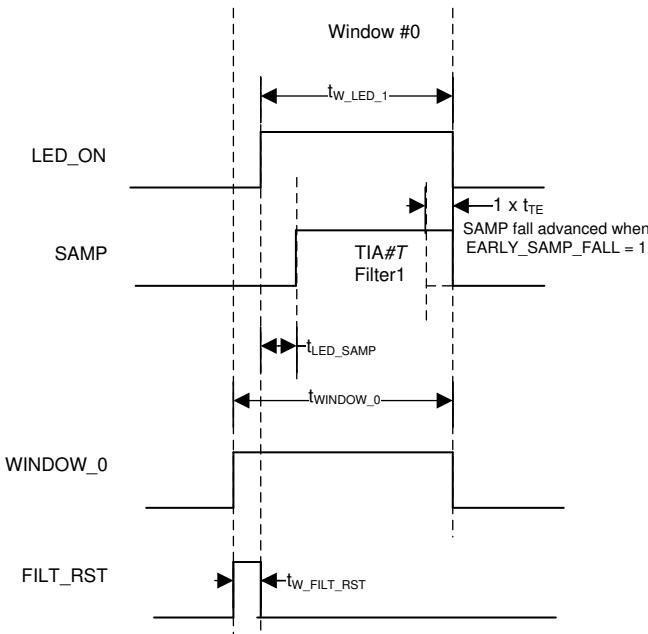


Figure 7-27. Timing Signals Within Window #0, single TIA #T ($T = 1$ or 2) enabled in Phase 1

The timing shown in [Figure 7-27](#) is applicable both if the phase is an LED phase or an Ambient phase. The Ambient phase is merely differentiated by setting all the LED driver switch control bits to '0' so that no LED turns on during the LED_ON signal.

[Figure 7-28](#) shows the timing signals in Window #0 for a case where Phase 1 is a 'Dual receive phase' (both TIAs enabled). Both the filters are reset prior to the LED_ON phase.

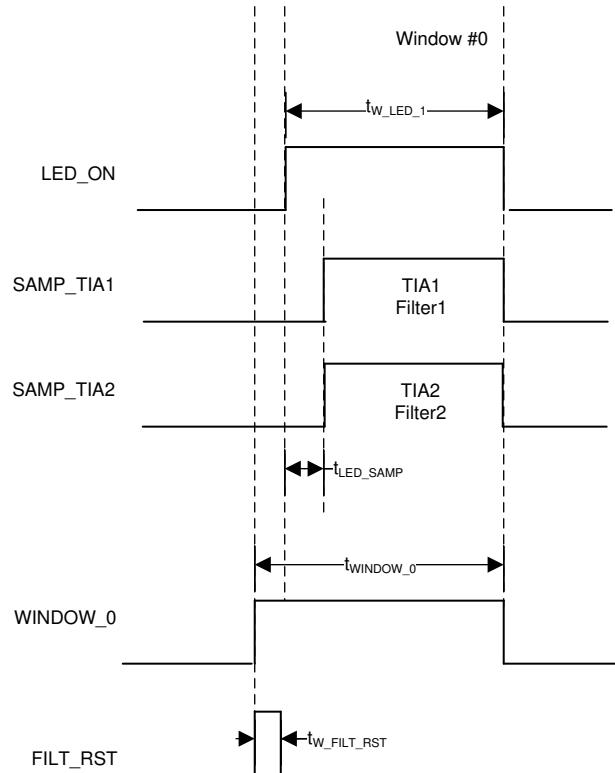
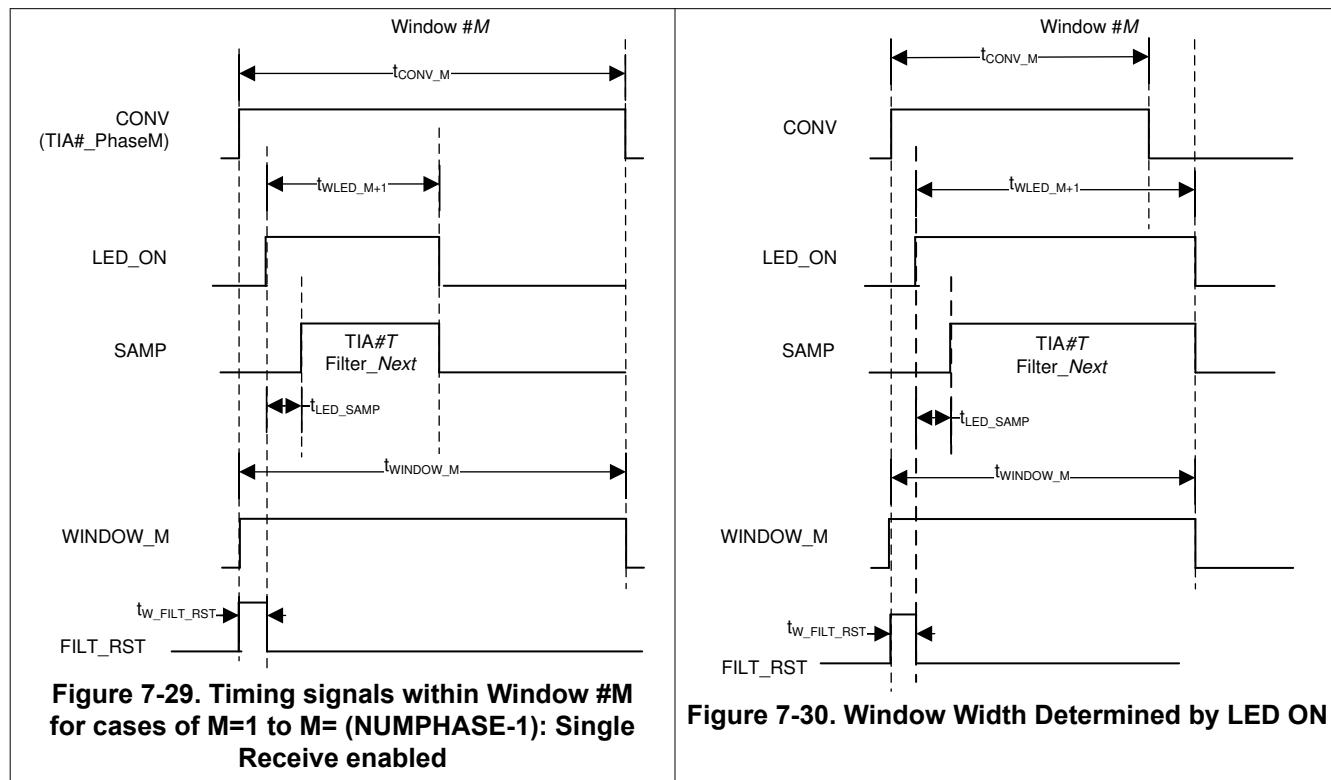


Figure 7-28. Timing Signals Within Window #0 both TIAs enabled in Phase 1

The generation of the LED ON, SAMP and CONV signals for Window #M for cases of M=1 to M=(NUMPHASE-1) is shown in [Figure 7-29](#), and [Figure 7-30](#). The CONV signal in Window #M corresponds to the CONV signal corresponding to Phase M and is automatically generated with the appropriate width (t_{CONV_M}) depending on the NUMAV setting for that phase.

While operating in the single receiver mode, an optional 'Stagger mode' control can be exercised to trade off between power consumption and cross-talk between phases. By default (Stagger mode set to '0'), the CONV signal of one phase overlaps with the LED ON signal of the next phase. Such overlap can result in some signal cross-talk between phases, especially if the supply/ground routings to the AFE are weak. If such a cross-talk is prominent, then the Stagger mode can be set so as to cause the LED ON signal of the next phase to come after completion of the CONV of the current phase. The Stagger mode results in a higher active time (higher power consumption) and a larger separation between the LED and Ambient sampling instants. For this reason, if the single receiver is used, then the single receiver can be preferable to not use the Stagger mode. While operating in Dual Receiver mode (both TIAs active), operating in a Staggered manner is mandatory.

[Figure 7-29](#), and [Figure 7-30](#) correspond to a case where the STAGGER_LED control for Phase #(M+1) is set to '0' so that the LED_ON signal of Phase #(M+1) overlaps with the CONV signal of Phase #M. Such overlapping of LED_ON and CONV signals is supported only if both Phase #M and Phase #(M+1) are operated as a 'Single Receive phase'. For such a case, one filter is available to sample the TIA output during the LED_ON signal of Phase #(M+1) while the signal of Phase #M sampled on the other filter is getting converted by the ADC. The width of the window is governed by whichever signal ends later – CONV of Phase #M or LED_ON of Phase #(M+1).



Note

Timing signals within Window #M for cases of M = 1 to M = (NUMPHASE-1): Single Receive enabled in Phase #M and Phase #(M+1) and STAGGER_LED set to '0' in Phase #(M+1)

If the Phase #(M+1) operates as a Single Receive phase with STAGGER_LED control for Phase #(M+1) is set to '1'. [Figure 7-31](#) and [Figure 7-32](#) correspond to Phase #M configured as Single Receive phase and Dual Receive phase respectively.

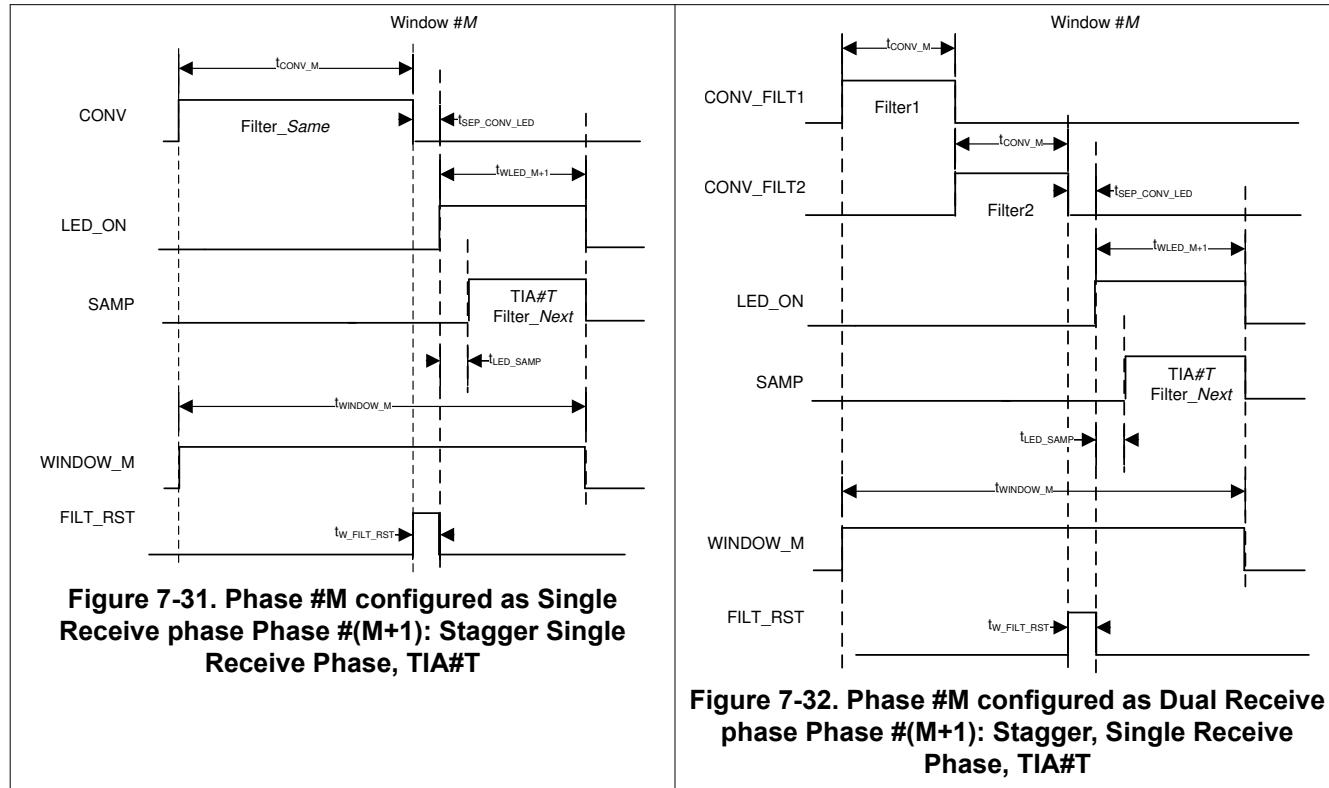


Figure 7-31. Phase #M configured as Single Receive phase Phase #(M+1): Stagger Single Receive Phase, TIA#T

Figure 7-32. Phase #M configured as Dual Receive phase Phase #(M+1): Stagger, Single Receive Phase, TIA#T

Note

Timing signals within Window #M for cases of M=1 to M= (NUMPHASE-1): Phase #(M+1) set to operate as Single Receive phase with STAGGER_LED of Phase #(M+1) set to '1'

[Figure 7-33](#) and [Figure 7-34](#) corresponds to a case where the Phase #(M+1) operates as a Dual Receive phase. For this case, the STAGGER_LED bit of Phase #(M+1) is a Don't care, and Window #M is made to operate in a staggered mode with the LED ON signals of Phase #(M+1) starting after the end of the CONV signals of Phase #M. (a) and (b) correspond to Phase #M configured as Single Receive phase and Dual Receive phase respectively.

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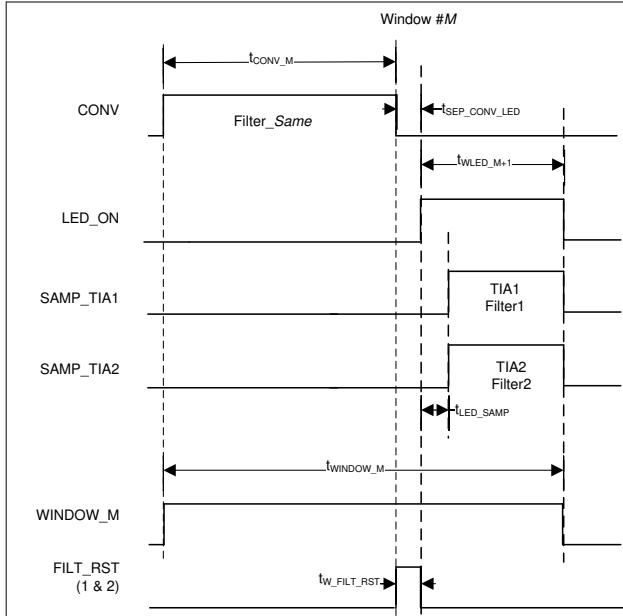


Figure 7-33. Phase #M configured as Single Receive phase. Phase #(M+1): Dual Receive Phase

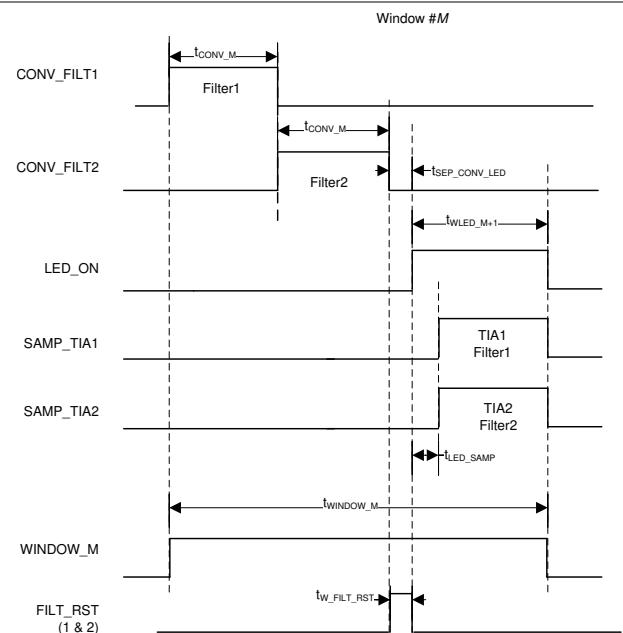


Figure 7-34. Phase #M configured as Dual Receive phase. Phase #(M+1): Dual Receive Phase

Note

Timing signals within Window #M for cases of M=1 to M= (NUMPHASE-1): Phase #(M+1) is a Dual Receive phase

The timing in the last window (Window #NUMPHASE) is shown in [Figure 7-35](#) and [Figure 7-36](#), and correspond to Phase #NUMPHASE operating either as Single Receive phase or Dual Receive phase .

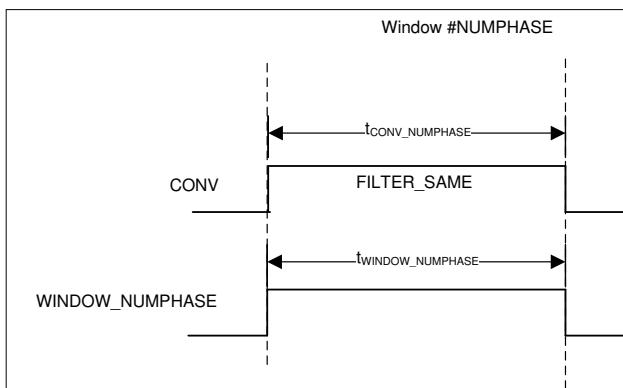


Figure 7-35. Phase #NUMPHASE : Single Receive phase

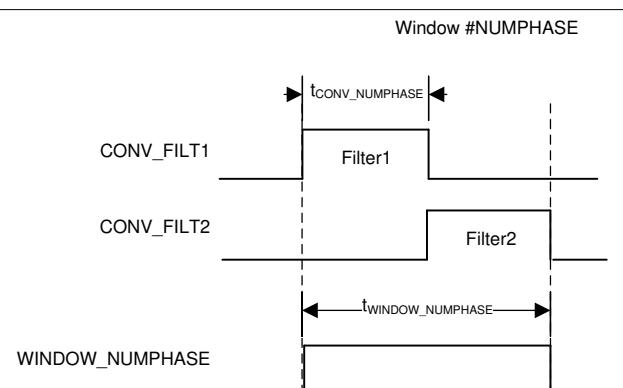


Figure 7-36. Phase #NUMPHASE : Dual Receive phase

Note

Timing signals within Window #NUMPHASE

The register control that determine the settings of the timing parameters are listed in [Table 7-25](#)

Table 7-25. Timing parameters associated with the signals of a phase

Parameter	Description	Set as	Default	Unit
t_{WLED_M}	Width of LED ON signal of Phase M	$(REG_TWLED^{(1)} + 1) \times t_{TE}$		μs
t_{LED_SAMP}	Start of LED ON to start of SAMP	$REG_TLED_SAMP^{(2)} \times t_{TE}$	0	μs
t_{CONV_M}	Width of the CONV signal of Phase M	$\{(REG_NUMAV^{(1)} + 1) \times 55 + 17.25\}^{(3)}$		μs
$t_{SEP_CONV_LED}$	Separation between end of CONV and start of LED_ON signal for the phase where the Staggered LED mode is set	$REG_TSEP_CONV_LED^{(2)} \times t_{TE}$	$1 \times t_{TE}$	μs
$t_{W_FILT_RST}$	Filter reset window	$1 \times t_{TE}$	$1 \times t_{TE}$	μs
t_{WINDOW_0}	Width of Window #0	$t_{W_FILT_RST} + t_{WLED_1}$		μs
t_{WINDOW_M}	Width of Window #M {M=1 to M=(NUMPHASE-1)} Phase M: Single Receive Phase M+1: Single Receive, STAGGER_LED='0'	$\text{Max}[t_{CONV_M}, (t_{W_FILT_RST} + t_{WLED_M+1})]$		μs
	Width of Window #M {M=1 to M=(NUMPHASE-1)} Phase M: Single Receive Phase M+1: Single Receive, STAGGER_LED='1'	$t_{CONV_M} + t_{SEP_CONV_LED} + t_{WLED_M+1}^{(4)}$		μs
	Width of Window #M {M=1 to M=(NUMPHASE-1)} Phase M: Dual Receive Phase M+1: Single Receive, STAGGER_LED='1'	$2 \times t_{CONV_M} + t_{SEP_CONV_LED} + t_{WLED_M+1}^{(4)}$		μs
	Width of Window #M {M=1 to M=(NUMPHASE-1)} Phase M: Single Receive Phase M+1: Dual Receive , STAGGER_LED='1'	$t_{CONV_M} + t_{SEP_CONV_LED} + t_{WLED_M+1}^{(4)}$		μs
	Width of Window #M {M=1 to M=(NUMPHASE-1)} Phase M: Dual Receive Phase M+1: Dual Receive , STAGGER_LED='1'	$2 \times t_{CONV_M} + t_{SEP_CONV_LED} + t_{WLED_M+1}^{(4)}$		μs
$t_{WINDOW_NUMPHASE}$	Width of Window #NUMPHASE Phase NUMPHASE: Single Receive	$t_{CONV_NUMPHASE}$		μs
	Width of Window #NUMPHASE Phase NUMPHASE: Dual Receive	$2 \times t_{CONV_NUMPHASE}$		μs

(1) Per-phase control.

(2) Global control.

(3) Rounded off to the nearest integer number of timing engine clocks that is \geq the value indicated by the formula.(4) Make sure that $t_{SEP_CONV_LED} \geq t_{W_FILT_RST}$.

7.3.2.3 Signal definition for a phase

The signal to be acquired in a phase is defined using per-phase register controls to associate one or more PDs and one or more LEDs to be active during that phase.

7.3.2.3.1 Single/Dual Receive phase selection

By default, the AFE operates as a single receiver and only TIA1 is used. TIA2 is powered down. By setting the EN_DUAL_TIA_GBL bit, TIA2 is powered up during the Active phase of the PRF cycle. Each individual phase can be specified to use either TIA1 or TIA2 or both using per-phase TIA_SEL bit as shown in [Table 7-26](#)

Table 7-26. Timing parameters associated with TIA selection in the Single and Dual receive modes

TIA_SEL	Active TIA for that phase	Phase Description
00	Only TIA1	Single Receive phase with TIA1
01	Only TIA1	Single Receive phase with TIA1
10	Only TIA2	Single Receive phase with TIA2
11	TIA1 and TIA2	Dual Receive phase with TIA1 & TIA2

7.3.2.3.1.1 PD Association for a Phase

The switch matrix that connects the input pins to TIA1 and TIA2 is shown in [Figure 7-37](#). Signals marked INP_TIA1<4:1> and INM_TIA1<4:1> are derived from the per-phase (of Phase M) register bits IN_TIA1<4:1> and correspond to the connection of the input pins to TIA1 for Phase M. Similarly the signals marked as INP_TIA2<4:1> and INM_TIA2<4:1> are derived from the per-phase (of Phase M) register bits IN_TIA2<4:1> and correspond to the connection of the input pins to TIA2 for Phase M. Each of the 24 signal phases has two sets of 4 bits (INP_TIA1<4:1> for TIA1 and INP_TIA2<4:1> for TIA2) which denote whether the corresponding input pin(s) are to be connected to TIA1 (or TIA2) during that particular phase or not. The switch controls bits for Phase M are used in Window (M-1) since the Window (M-1) contains the LED_ON signal of Phase M, hence the gating of the static control bits with the WINDOW(M-1) in [Figure 7-37](#)

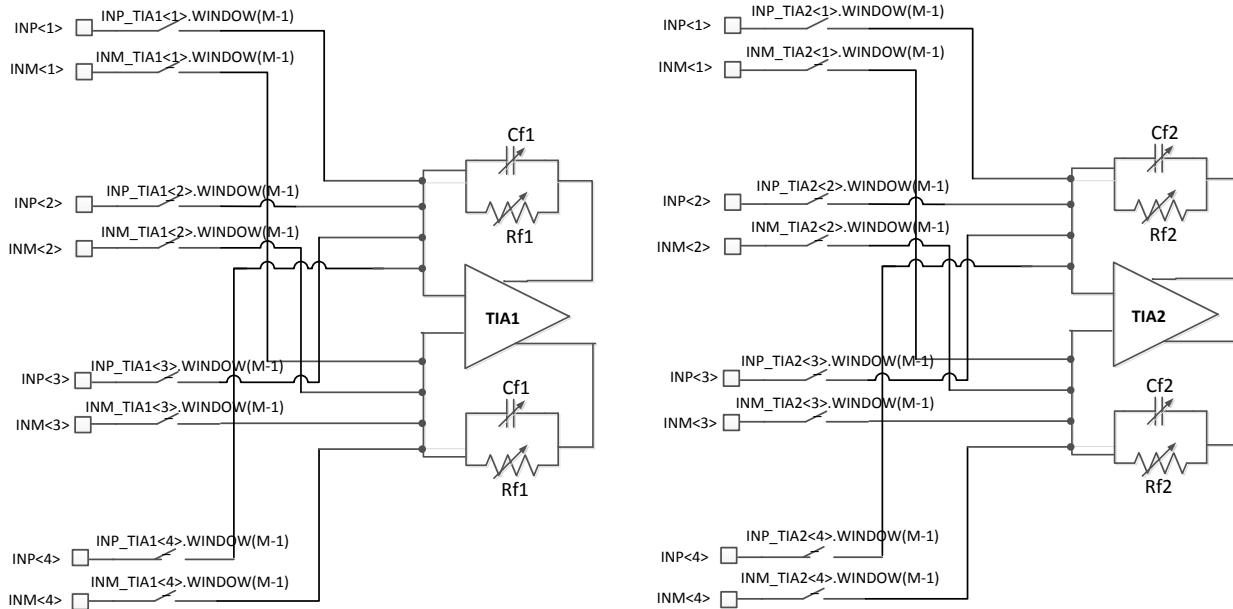


Figure 7-37. Switch matrix showing connectivity of the input pins to TIA1 and TIA2 in Phase M

The PDs are connected differentially to the TIAs. So INP_TIAx<y> and INM_TIAx<y> are the same as IN_TIAx<y> the per-phase register control bits (x:TIA# = 1,2; y:IN#=1,2,3,4).

In addition to the per-phase controls for connecting or disconnecting the PDs to the TIA, global controls PD_DISCONNECT_TIA1(PD_DISCONNECT_TIA2) causes all the PDs (both P and M side switches) to be disconnected from TIA1 (/TIA2) even if any of the PD_ON bits have been set to '1'. When in the PD_DISCONNECT* mode, the input current to the TIA during a phase is equal to the Offset Cancellation DAC set for that phase. The PD_DISCONNECT mode is useful to calibrate the Offset DAC.

When a particular PD is connected to the TIA, the TIA maintains the proper bias on the PD through its negative feedback mechanism. When a PD is disconnected from the TIA, a mechanism to automatically short the input pins to an internal node VCM is used to maintain the PD bias.

7.3.2.3.1.2 LED Association for a Phase

The LED association for each phase is set by the 'per-phase' register controls LED_DRV1_TX<8:1> and LED_DRV2_TX<8:1> as shown in [Figure 7-38](#). These static signals defined for each phase combine with the dynamically switching LED_ON signal during that phase window to generate the appropriate switch controls to route the driver currents to the desired TX pin(s).

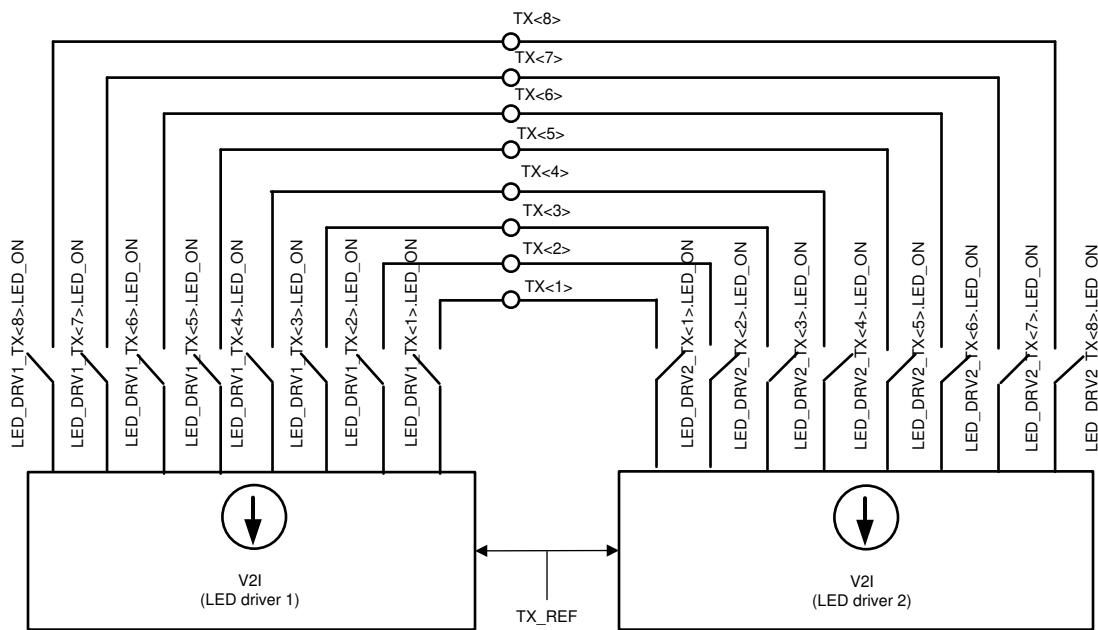


Figure 7-38. Scheme for LED Association in a Phase

Setting the LED_DRVx_TX <y> bit for a phase turns on the switch between LED Driver x (where x=1,2) and the TX <y> pin (where y= 1,2,3,4,5,6,7,8). Any combination of the control bits can be set for each phase, resulting in a complete flexibility in which LEDs are turned on in a phase.

For an Ambient phase, set all the LED driver switch control bits (LED_DRVx_TX<y>) to '0'. The LED_ON signal is generated even for the Ambient phase but no current is generated since all the 8 switches are off.

7.3.2.4 Setting Receiver Signal Chain Parameters for a Phase

The register controls for setting the signal chain parameters for a given phase are summarized in [Table 7-27](#).

Table 7-27. Register Controls for Setting the Signal Chain Parameters of a Phase

Parameter	Register control	# bits	Range of control	Classification	Comments	
Ambient Offset DAC range	IFS_AMB_OFFSETDAC_TIA1	3	1X to 16X	Global control for TIA1, TIA2	Ambient Offset DAC full scale range	
	IFS_AMB_OFFSETDAC_TIA2	3				
LED Offset DAC range	IFS_LED_OFFSETDAC_TIA1	1	1X, 2X	Global control for TIA1, TIA2	LED Offset DAC full scale range	
	IFS_LED_OFFSETDAC_TIA2	1				
Enable LED Offset DAC	EN_LED_OFFSETDAC_TIA1	1	0 or 1	Global control	Enables LED Offset DAC (LED Offset DAC is disabled by default)	
	EN_LED_OFFSETDAC_TIA2	1				
Enable Ambient DAC LSB control	EN_AMB_DAC_LSB	1	0 or 1	Global control	Set to '1' to enable the LSB control of the Ambient DAC	
Ambient/ LED Offset DAC current setting	IOFFDAC_PH_TIA1	8	255 steps between 0 and full scale value	Per-phase control for TIA1 & TIA2	Depends on IFS_AMB_OFFSETDAC for Ambient DAC, IFS_LED_OFFSETDAC for LED DAC	
	IOFFDAC_PH_TIA2	8				
Offset DAC polarity	POL_IOFFDAC_AMB	1	Add or Subtract	Global control for Ambient, LED DACs	1 = Subtract 0 = Add,	
	POL_IOFFDAC_LED	1				
TIA gain	RF_TIA1	4	3.7 kΩ - 1 MΩ	Per-phase for TIA1		
	RF_TIA2	4		Per-phase for TIA2		
TIA feedback cap	CF_TIA1	3	2.5 pF – 25 pF	Per-phase for TIA1		
	CF_TIA2	3		Per-phase for TIA2		
Filter Controls	FILTER_SET_SEL	1	0 or 1	Per-phase control Global control common for both receivers	Choose between Set 1, Set 2	
	REG_TW_FILTER_PRE	8	0 to 127		Pre-charge time window	
	OVERRIDE_BW_PRE	1	0 or 1		Override bit to enabled register control of Pre-charge filter bandwidth (Set 1 & Set 2)	
	FILTER_BW_PRE_SET1	5	2.5 kHz to 77.5kHz		Filter BW Set 1	
	FILTER_BW_FINE_SET1					
	FILTER_BW_PRE_SET2				Filter BW Set 2	
	FILTER_BW_FINE_SET2					
# of ADC averages	REG_NUMAV	4	1 to 16 ADC averages	Per-phase – common for TIA1, TIA2	# of ADC averages = REG_NUMAV+1	
LED full scale current	ILED_FS	3	50mA (default 1X 0.5X to 2.5X)	Global control		
LED current setting	ILED_DRV1	8	0 to full scale setting – 256 steps	Per-phase control	LED Driver 1	
	ILED_DRV2				LED Driver 2	

7.3.2.5 LED Driver

By default, the full scale current range of each of the two parallel drivers is 50 mA. The register control ILED_FS can be used to change the full-scale range as shown in [Table 7-28](#).

Table 7-28. Register Controls for Setting the LED Full-Scale Current

ILED_FS	Mode	LED full scale current – one driver	LED full scale current – two drivers
000	1X mode	50 mA	100 mA
010	2X mode	100 mA	200 mA
110	2.5X mode	125 mA	250 mA
001	0.5X mode	25 mA	50 mA
Other settings		Do not use	

The current setting of each of the two drivers with respect to the full-scale current is set using per-phase 8-bit controls ILED_DRV1 for driver 1 and ILED_DRV2 for driver 2 as shown in [Table 7-29](#).

Table 7-29. Register Controls for Setting the LED Current

DECIMAL EQUIVALENT OF 8-BIT ILED_DRV1 AND ILED_DRV2 CURRENT CONTROL	LED CURRENT (mA) for different modes – Typical value			
	1X mode ILED_FS='000'	2X mode ILED_FS = '010'	2.5X mode ILED_FS='110'	0.5X mode ILED_FS='001'
0	0	0	0	0
1	0.196	0.392	0.49	0.098
2	0.392	0.784	0.98	0.196
..				
255	50 ⁽¹⁾	100 ⁽¹⁾	125 ⁽¹⁾	25 ⁽¹⁾

(1) Due to saturation effects in the driver, the full scale current can be lower than these values.

The full-scale current range of both drivers ‘LED driver 1’ and ‘LED driver 2’ is controlled by an internally generated bias voltage called TX_REF. By programming TX_REF using the register controls ILED_FS, the full-scale current range of both drivers can be programmed as shown in [Table 7-30](#)

Table 7-30. Full-Scale LED Current and Headroom Voltage

LED full-scale Mode	TX_REF voltage	1 LED driver ON		2 LED drivers ON through same LED		2 LED drivers ON, 2 LEDs	
		Full scale current ⁽¹⁾	VHR ⁽²⁾	Full scale current ⁽¹⁾	VHR ⁽²⁾	Full scale current ⁽¹⁾	VHR ⁽²⁾
1X	150 mV	50 mA	320 mV	100 mA	370 mV	50 mA	345 mV
2X	300 mV	100 mA	600 mV	200 mA	650 mV	100 mA	625 mV
2.5X	375 mV	125 mA	800 mV	250 mA	850 mV	125 mA	825 mV
0.5X	75 mV	25 mA	220 mV	50 mA	250 mV	25 mA	240 mV

(1) Full scale current through LED .

(2) Typical voltage headroom needed for the LED driver. To determine the minimum TX_SUP voltage required to drive the LEDs, add VHR, VLED_MAX (the highest forward voltage of the LED), and an additional margin of approximately 300 mV.

For the same LED current setting, the mode with the higher TX_REF voltage (higher VHR) results in a better (lower) noise operation of the LED driver.

If none of the switches to a driver are set to be on, the driver is switched off in that phase (for example, both drivers are off in the Ambient phase by setting all the switches of both drivers to be OFF).

7.3.2.6 Offset Cancellation DAC

There are two Offset DACs at the input of each TIA – these are denoted as *Ambient Offset DAC* and *LED Offset DAC* and their respective currents are denoted as IOFFDAC_AMB_TIA1, IOFFDAC_AMB_TIA2 and IOFFDAC_LED_TIA1, IOFFAC_LED_TIA2 respectively. The Ambient Offset DAC is enabled by default whereas the LED Offset DAC is disabled by default.

There are two 8-bit per-phase Offset DAC controls, one associated with each TIA – IOFFDAC_PH_TIA1 for TIA1 and IOFFDAC_PH_TIA2 for TIA2. Based on the Ambient cancellation scheme (Manual or Automatic), the IOFFDAC_PH_TIA* register controls may sometimes control IOFFDAC_LED_TIA* and sometimes control IOFFDAC_AMB_TIA*. The Offset DAC circuit scheme is shown in [Figure 7-39](#).

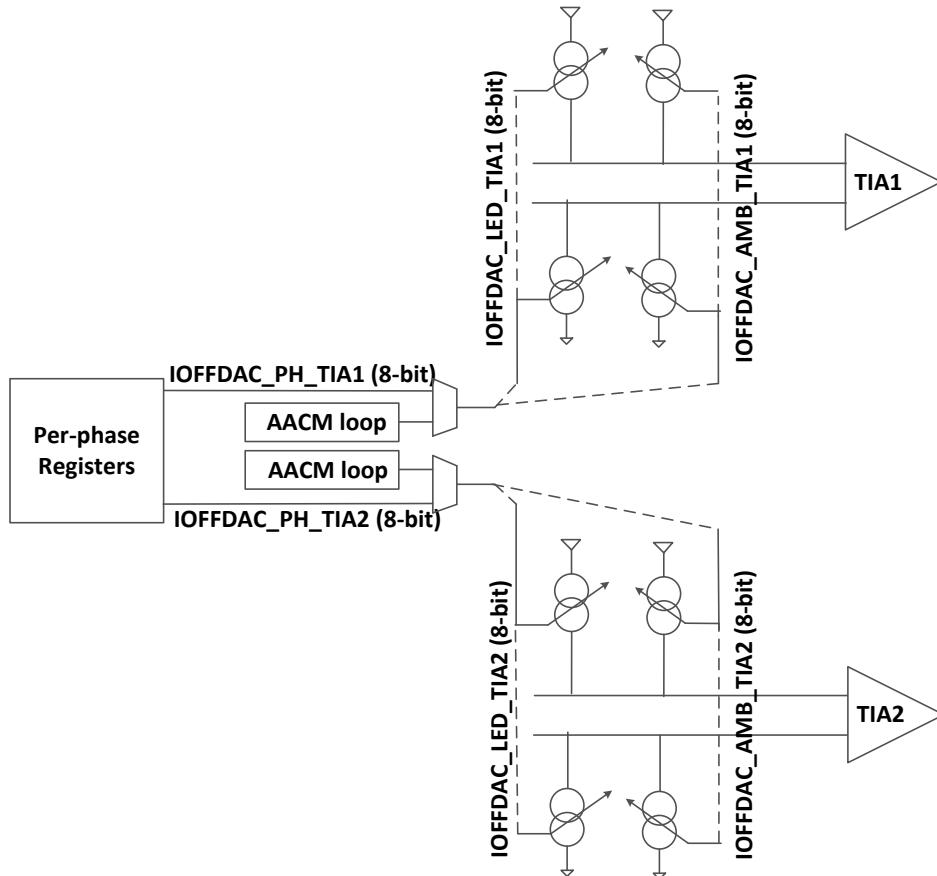


Figure 7-39. Offset DAC scheme showing the Ambient and LED Offset DACs

The Offset DAC full scale current control of the Ambient Offset DAC is set through global registers IFS_AMB_OFFSETDAC_TIA1 and IFS_AMB_OFFSETDAC_TIA2 (for TIA1 and TIA2 respectively) as shown in [Table 7-31](#). The full-scale current setting is common to the IOFFDAC_AMB_TIA* across all the phases.

Table 7-31. Full-scale current control of Ambient Offset DAC using IFS_OFFDAC controls (applicable to IOFFDAC_AMB_TIA* in all the phases)

Register controls to set the mode		
Mode notation	IFS_AMB_OFFDAC_TIA1, IFS_AMB_OFFDAC_TIA2 (binary)	Full scale current
1X mode	000	$\pm 15.9375 \mu A$
2X mode	001	$\pm 31.875 \mu A$
4X mode	011	$\pm 63.75 \mu A$
8X mode	101	$\pm 127.5 \mu A$
16X mode	111	$\pm 255 \mu A$
	Other settings	Do not use

Note

For the same offset DAC current setting, the mode with the lower full scale current operates with the lowest noise. Therefore, it is recommended that at low levels of ambient current, the 1X mode be used.

Also, in the phases where IOFFDAC_PH_TIA* controls the IOFFDAC_AMB_TIA*, the IOFFDAC_AMB_TIA* current for that phase is set through bits D7..D0 of IOFFDAC_PH_TIA* as shown in [Table 7-32](#). Note that by default, only D7 to D1 of IOFFDAC_PH_TIA* control the Ambient Offset DAC, and to enable the D0 control, the EN_AMB_DAC_LSB needs to be programmed.

Table 7-32. Mapping of the Ambient Offset DAC Setting to D7..D1 of I_OFFDAC_TIA Register^{(1) (2)}

DECIMAL EQUIVALENT IOFFDAC_PH_TIA1<7:0> IOFFDAC_PH_TIA2<7:0>	AMBIENT OFFSET DAC CURRENT (μA) FOR DIFFERENT MODES				
	1X MODE	2X MODE	4X MODE	8X MODE	16X MODE
0	0	0	0	0	0
1	0.0625	0.125	0.25	0.5	1
2	0.125	0.25	0.5	1	2
..
255	15.9375	31.875	63.75	127.5	255

(1) Above table corresponds to POL_IOFFDAC_AMB=0. With POL_IOFFDAC_AMB=1, the above currents become negative

(2) Set EN_AMB_DAC_LSB to '1' to enable the LSB control of IOFFDAC_PH_TIA*

The full scale current of the LED Offset DAC has a default value of $31.875 \mu A$ (1X mode) and can be increased to $63.75 \mu A$ (2X mode) by setting the IFS_LED_OFFDAC_TIA1 (/ IFS_LED_OFFDAC_TIA2) bit to 1. In the phases where IOFFDAC_PH_TIA* controls the IOFFDAC_LED_TIA*, the IOFFDAC_LED_TIA* current for that phase is set using the per-phase control IOFFDAC_PH_TIA* as shown in [Table 7-33](#)

Table 7-33. Mapping of the LED Offset DAC Setting to the I_OFFDAC* Register⁽¹⁾

DECIMAL EQUIVALENT IOFFDAC_PH_TIA1<7:0> IOFFDAC_PH_TIA2<7:0>	LED OFFSET DAC CURRENT (μA)	
	1X Mode	2X Mode
0	0	0
1	0.125	0.25
2	0.25	0.5
..
255	31.875	63.75

(1) Above table corresponds to POL_IOFFDAC_LED=0. With POL_IOFFDAC_LED = 1, the above currents become negative.

The Ambient Offset DAC is enabled by default whereas the LED Offset DAC is disabled by default.

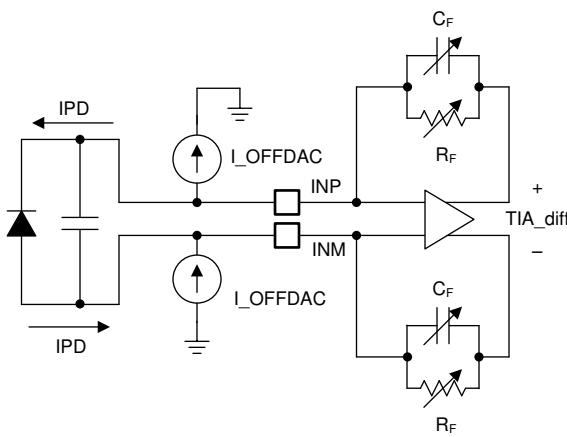
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To enable the LED Offset DAC, set the global bits EN_LED_OFFSETDAC_TIA1 (to enable the LED Offset DAC for TIA1) and EN_LED_OFFSETDAC_TIA2 (to enable the LED Offset DAC for TIA2).

The polarity of the Ambient offset DAC is controlled by a global register bit POL_IOFFDAC_AMB, and the polarity of the LED Offset DAC is controlled by a global register bit POL_IOFFDAC_LED.

With zero input current and zero current in the offset cancellation DAC, the output of the AFE is close to zero. Based on the channel offset, the output voltage for zero input current can be a small positive or negative value, usually in the range of several millivolts. With the photodiode connected as shown in [Figure 7-40](#) and a signal current coming from the photodiode, the output code of the device is expected to be positive with the offset cancellation DAC set to zero ($\text{IOFFSET}^* = 0$). With IOFFSET^* set as a negative ($\text{POL_OFFFAC}^* = 1$), a dc offset can be subtracted from the signal. This is the case for both the Ambient DAC and the LED DAC. If the polarity of the PD connection to the input pins is reversed with respect to what is shown in [Figure 7-40](#), then setting POL_OFFDAC^* to 0 results in a subtraction of the Offset DAC current from the input current of the PD. [Figure 7-40](#) shows the polarity of only one Offset DAC. However, the same polarity applies to both the Ambient and LED Offset DACs.



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Figure 7-40. Offset Cancellation Current Polarity Diagram (applicable to both Ambient and LED Offset DAC)

7.3.2.7 Trans-impedance amplifier (TIA Controls)

The gain of TIA1 and TIA2 can be programmed using the per-phase controls RF_TIA1 and RF_TIA2 respectively. The mapping of the TIA gain settings to the RF control is shown in [Table 7-34](#).

Table 7-34. Mapping of the TIA Gain to the RF Register Control

RF_TIA* Register Value	TIA GAIN (R _F)
0	3.7 kΩ
1	5 kΩ
2	10 kΩ
3	25 kΩ
4	33.3 kΩ
5	50 kΩ
6	71.5 kΩ
7	100 kΩ
8	142 kΩ
9	166 kΩ
10	200 kΩ
11	250 kΩ
12	500 kΩ
13	1 MΩ

The feedback capacitance (C_f) of TIA1 and TIA2 can be programmed using the per-phase controls CF_TIA1 and CF_TIA2 respectively. The mapping of the TIA feedback capacitor settings to the CF control is shown in [Table 7-35](#).

Table 7-35. Mapping of the TIA feedback cap to the CF register control

CF_TIA* register value	TIA FEEDBACK CAPACITOR (C _F)
0	2.5 pF
1	5 pF
2	7.5 pF
3	10 pF
4	17.5 pF
5	20 pF
6	22.5 pF
7	25 pF

The product of R_F and C_F determines time constant of the TIA and determines the TIA transient settling during the LED_ON phase. Refer [Table 7-39](#) for choice of the TIA time constant based on the LED ON time.

7.3.2.8 PPG Noise Reduction Filter

The signal from the PD contains optical noise which needs to be band-limited before the ADC converts the signal. The Noise reduction filter at the output of the TIA helps limit the bandwidth of the optical noise and improve the system SNR. The output of the TIA is sampled by the Noise reduction filter during the SAMP phase. The filter's RC bandwidth can be programmed. There are 2 such filters. When used as a Single Receiver, the two filters get connected to the same TIA during the SAMP of alternate phase windows. When used as a Dual receiver, each filter connects to the output of one of the two TIAs during the same SAMP. The voltage sampled across a filter in SAMP is converted by the ADC in the associated CONV. Before a filter enters SAMP, the filter is reset to erase any signal memory from use in a prior phase. As a result, the filter needs to be able to settle from zero to the signal level during SAMP, while also providing noise filtering. To address the conflicting requirements of settling and noise filtering, SAMP is partitioned into two portions – a Pre-charge window during which the filter bandwidth can be set higher to speed up settling, followed by a Fine Settling window where a lower filter bandwidth can be used for noise filtering.

The width of the Pre-charge window (programmed in terms of CLK_TE) is controlled using a global control REG_TW_FILTER_PRE. The default setting of the pre-charge window width is 4 clocks, and the MSB of this word serves as an over-ride bit to change the default setting as shown in [Table 7-36](#). The rest of SAMP after completion of the Pre-charge window automatically gets assigned for the Fine settling window.

Table 7-36. Programming the Filter Pre-Charge Phase Width

REG_TW_FILTER_PRE								Filter Pre-charge window width ($t_{W_FILTER_PRE}$)
D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	4 × CLK_TE (Default)
1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1 × CLK_TE
1	0	0	0	0	0	1	0	2 × CLK_TE
1					...			
1	1	1	1	1	1	1	1	127 × CLK_TE

The timing scheme showing the transition of the filter bandwidth from the pre-charge phase to the fine settling phase is shown in [Figure 7-41](#).

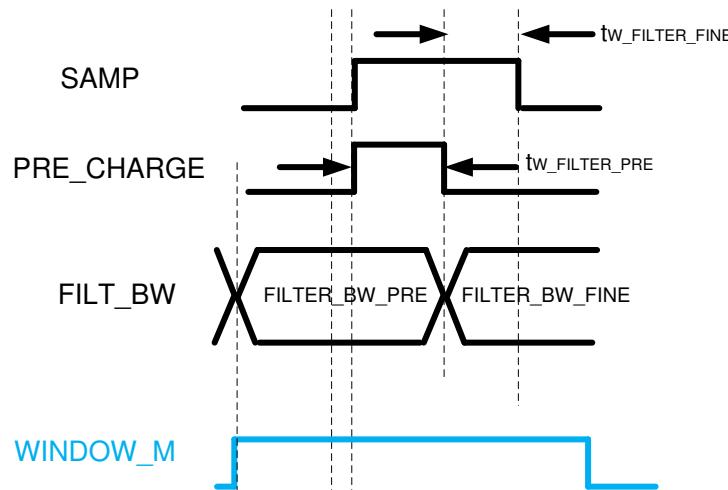


Figure 7-41. Filter Bandwidth Transition Scheme

Two sets of filter bandwidth controls can be programmed – Set 1 and Set 2. For each of the 24 signal phases within a PRF cycle, either set can be selected using the per-phase register bit FILTER_SET_SEL. Each set comprises the register controls for the filter bandwidth in the Pre-charge window as well as the filter bandwidth in the Fine settling window. By default, FILTER_BW_PRE of both Set 1 and Set 2 is set to 50 KHz. By setting the OVERRIDE_BW_PRE register bit to '1', FILTER_BW_PRE can be set using the global register control FILTER_BW_PRE_SET1 (when using Set 1 for the phase) and using FILTER_BW_PRE_SET2 (when using Set 2 for the phase). The bandwidth controls are specified in [Table 7-37](#).

Table 7-37. Filter Bandwidth Selection

Filter BW setting	Set 1 - Used for phase where FILTER_SET_SEL=0		Set 2 - Used for phase where FILTER_SET_SEL=1	
	OVERRIDE_BW_PRE = 0	OVERRIDE_BW_PRE = 1	OVERRIDE_BW_PRE = 0	OVERRIDE_BW_PRE = 1
In Pre-charge phase	50 kHz	FILTER_BW_PRE_SET1	50 kHz	FILTER_BW_PRE_SET2
In Fine settling phase	FILTER_BW_FINE_SET1			FILTER_BW_FINE_SET2

Each filter bandwidth register control listed in [Table 7-37](#) is a 5-bit register word of the form FILTER_BW<4:0>

Filter bandwidth in kHz = FILTER_BW<0> × 2.5 + FILTER_BW<1> × 5 + FILTER_BWZ<2> × 10 + FILTER_BW<3> × 20 + FILTER_BW<4> × 40 where FILTER_BWZ<2> corresponds to the invert of the FILTER_BW<2> register bit.

With the 5-bit control, filter bandwidth settings from 2.5 Hz to 77.5 kHz can be achieved in steps of 2.5 kHz.

A few example settings of the filter bandwidth are shown in [Table 7-38](#). Using a low filter bandwidth provides more noise filtering to the noise from the sensor and the TIA.

Table 7-38. Filter Bandwidth Set by FILTER_BW Control

FILTER_BW<4>	FILTER_BW<3>	FILTER_BW<2>	FILTER_BW<1>	FILTER_BW<0>	Typical f _{RC} (kHz)
0	0	0	0	0	10
0	0	0	0	1	12.5
0	0	0	1	0	15
0	0	0	1	1	17.5
0	0	1	0	0	Do not use
0	0	1	0	1	2.5 (Lowest)
0	0	1	1	0	5
0	0	1	1	1	7.5
0	1	0	0	0	30
0	1	0	0	1	32.5
...					
1	0	0	0	0	50
1	0	0	0	1	52.5
...					
1	1	0	1	1	77.5 (Highest)
...					
1	1	1	1	1	67.5

To support shorter SAMP widths (and thereby shorter LED ON times), the transient settling of the TIA and the filter needs to be fast in the Pre-charge window. The suggested settings for the TIA time constant (maximum value), filter pre-charge window width and filter bandwidth settings in the pre-charge and fine settling phases are listed in [Table 7-39](#) across SAMP widths (t_{TE} in this table corresponds to the time period of a 128 kHz clock).

Table 7-39. Filter and TIA settings across SAMP widths

SAMP width (t_{W_SAMP}) ⁽¹⁾	Max TIA time constant ($\tau_{TIA} = R_f \times C_f$)	Pre-charge width ($t_{W_FILTER_PRE}$)	Pre-charge BW ($FILTER_BW_PRE$)	Fine settling BW($FILTER_BW_FINE$)
2 × t_{TE} approximately 16 µs	3 µs	0	50 kHz	50 kHz
3 × t_{TE} approximately 24 µs	4.6 µs	0	30 kHz	30 kHz
4 × t_{TE} approximately 31 µs	6 µs	0	25 kHz	25 kHz
5 × t_{TE} approximately 39 µs	7.5 µs	0	20 kHz	20 kHz
6 × t_{TE} approximately 47 µs	3 µs	2 × t_{TE} approximately 16 µs	50 kHz	10 kHz
8 × t_{TE} approximately 63 µs	6 µs	4 × t_{TE} approximately 31 µs	25 kHz	10 kHz
9 × t_{TE} approximately 70 µs	6 µs	4 × t_{TE} approximately 31 µs	25 kHz	7.5 kHz
10 × t_{TE} approximately 78 µs	6 µs	4 × t_{TE} approximately 31 µs	25 kHz	5 kHz
12 × t_{TE} approximately 94 µs	6 µs	4 × t_{TE} approximately 31 µs	25 kHz	5 kHz
15 × t_{TE} approximately 117 µs	6 µs	4 × t_{TE} approximately 31 µs	25 kHz	2.5 kHz

(1) t_{TE} in this table corresponds to a 128 kHz internal clock. If using a different t_{TE} , then follow the same guidelines as in the table based on the SAMP width in µs.

7.3.2.9 ADC Averaging

To reduce the noise in the PPG phase output, the input to the ADC (sampled on the filter's capacitor) can be converted by the ADC multiple times and averaged. The per-phase register control REG_NUMAV determines the number of ADC averages for that phase (NUMAV).

The number of averages is set using the REG_NUMAV register control as NUMAV = (REG_NUMAV + 1)

As an example, when NUMAV is programmed to 4 (REG_NUMAV = 3), the ADC converts its input four times in each phase, averages the four conversions, and stores the averaged value in the FIFO. The width of the CONV signal for a phase is automatically changed based on the NUMAV setting for that phase.

Averaging only helps in reducing ADC noise and not the front-end noise because the input to the ADC is the same sampled voltage across all ADC conversions used to generate the average (this voltage corresponds to the voltage sampled on the sampling capacitor of the filter). The number of samples that can be averaged ranges from 1 to 16 (when REG_NUMAV is programmed from 0 to 15). A higher number of averages results in larger conversion times leading to higher active time and larger power consumption. A high value of NUMAV also increases the separation between the sampling instants of LED and Ambient signals, which is undesirable from perspective of Ambient rejection. Therefore, for high gain settings (250 KΩ and beyond), set NUMAV to 1. For gains in the range of 100 KΩ, a NUMAV of 2 provides adequate SNR improvement. Settings of NUMAV higher than 2 only help at very low TIA gain settings.

Averaging is implemented in the following manner:

The number of ADC samples corresponding to the number of averages (NUMAV + 1) are accumulated, as shown in [Equation 1](#):

$$\text{SUMADC} = \sum_{i=1}^{(\text{NUMAV}+1)} (\text{ADC}_i) \quad (1)$$

where

- ADC_i = the i^{th} sample converted by the ADC

The accumulator output (SUMADC) is then divided by a factor D that is obtained by $D = 128 / X$, with X being an integer.

The averaged output is calculated as shown in [Equation 2](#):

$$\text{ADCOUT} = \text{SUMADC} / D \quad (2)$$

where

- $D = 128 / X$, with X being an integer

This implementation gives an averaging function that is exact when the number of averages is a power of 2 but deviates from ideal values for other settings, as shown in [Table 7-40](#).

Table 7-40. ADC Averaging Mode Settings

REG_NUMAV	NUMBER OF AVERAGES (NUMAV)	INTEGER (X)	DIVISION FACTOR (D)
0	1	128	1.0
1	2	64	2.0
2	3	43	2.97
3	4	32	4.0
4	5	26	4.92
5	6	21	6.10
6	7	18	7.11
7	8	16	8.0
8	9	14	9.14
9	10	13	9.85
10	11	12	10.67
11	12	11	11.64
12	13	10	12.8
13	14	9	14.22
14	15	9	14.22
15	16	8	16.0

7.3.2.10 Input DC Cancellation

The Ambient signal incident on the sensor can be modeled as the sum of a DC (or slow varying) component and an AC (fast-varying) component. The AC component can show up as tones in the LED phase data, and can interfere with the detection of the heart rate from the PPG signal. The tones from the AC component of the ambient can be largely suppressed by defining LED and Ambient phases, and by subtracting the Ambient phase data from the LED phase data.

From a theoretical calculation, the ambient rejection from digital subtraction of the ambient phase data from the LED phase data is given by:

$$\text{Ambient rejection through } (\text{LED} - \text{Ambient}) = \sqrt{2 \times (1 - \cos(2\pi f_{AMB} \cdot t_{SEP}))} \quad (3)$$

where

- f_{AMB} is the frequency of the ambient light and t_{SEP} is the time separation between the SAMP end of the LED and Ambient phases

An even higher level of ambient rejection can be achieved by combining the Ambient signal from more than one phase and subtracting the combined Ambient signal from the LED phase. The Digital subtraction of Ambient (or a combination of multiple Ambients) can help suppress tones.

However, the other undesirable effect of the ambient signal is that the DC component of the ambient signal can fill a portion of the dynamic range of the receiver in both the LED and ambient phases. A high ambient signal level can limit the maximum TIA gain setting and limit the achievable SNR. The Ambient Offset DACs at the input of the TIA can be configured (either automatically or by the MCU) to cancel out all or a portion of the DC signal from the Ambient. Similarly, the DC component of the signal in the LED phase also can be cancelled out using either the Ambient or the LED Offset DACs.

The AFE offers multiple schemes for controlling the LED and Ambient Offset DAC to cancel out the DC of the signal in the LED and Ambient phases. The Ambient DC cancellation can be controlled either by the MCU, or by enabling Analog AACM control loops to estimate and cancel the Ambient DC. The LED Offset DAC can be controlled by the MCU. Alternatively, when using the Analog AACM loop to cancel the Ambient DC, the Digital AACM control loop can be used to estimate and cancel the additional DC in the LED phase. An overview of control schemes are depicted in [Figure 7-42](#) and listed in [Table 7-41](#). The Digital AACM gets the name by virtue of the control loop being realized through digital logic – the ADC output code in the LED phase serves as the input to this logic. The Analog AACM loop, on the other hand uses the Analog output of the TIA to determine the Offset DAC setting required to cancel the Ambient.

Note that while both the Analog and Digital loops are named as AACM (Automatic Ambient Cancellation Mode) loops, the Analog AACM loop is meant for cancellation of Ambient DC, the Digital AACM loop is meant for cancelling the DC from the LED.

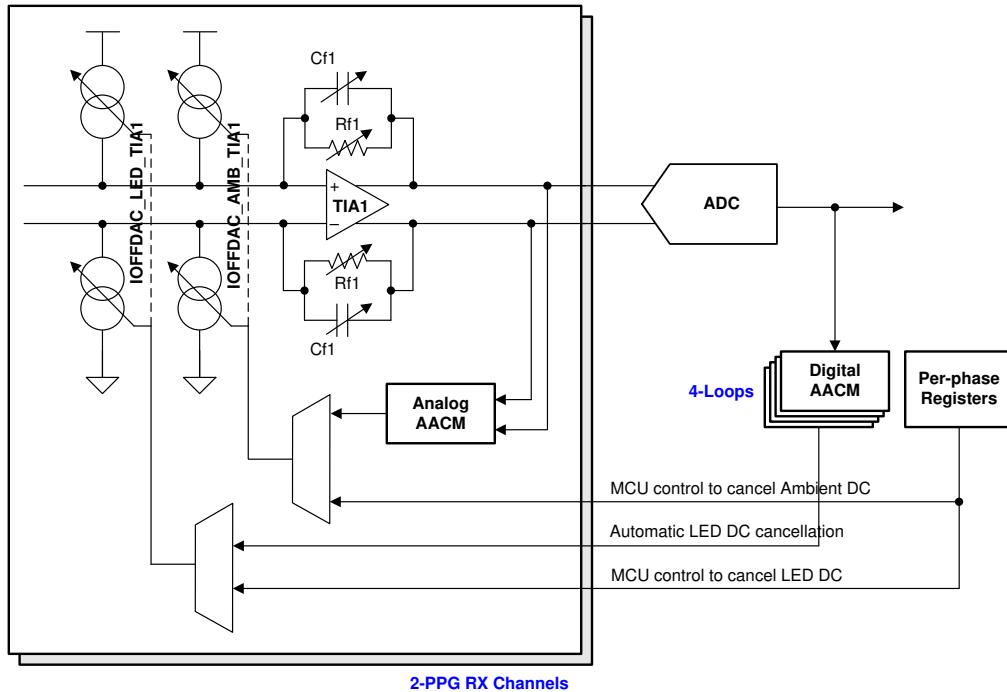


Figure 7-42. Control Schemes for Ambient and LED DC Cancellation

Table 7-41. Control Schemes for Ambient and LED DC Cancellation⁽⁶⁾

Scheme Name	Scheme Description	DC subtraction in LED phase done using ⁽¹⁾	Ambient DC DAC Control		LED Offset DAC control In LED Phase ⁽²⁾
			In baseline Ambient Phase	In LED Phase	
Full MCU control	MCU controls cancellation of Ambient, LED DC	Ambient Offset DAC ⁽³⁾	Set by IOFFDAC_PH_TIA* register	Increment using IOFFDAC_PH_TIA* register	–
		LED Offset DAC ⁽⁴⁾	Set by IOFFDAC_PH_TIA* register	Retains value set in baseline Ambient phase	Set by IOFFDAC_PH_TIA* register
Automatic Ambient cancellation using Analog AACM	Ambient DC cancelled using Analog AACM / MCU controls LED DC cancellation	Ambient Offset DAC ⁽³⁾	Controlled by Analog AACM loop	Increment using IOFFDAC_PH_TIA* register	–
		LED Offset DAC ⁽⁴⁾	Controlled by Analog AACM loop	Retains value set in baseline Ambient phase	Set by IOFFDAC_PH_TIA* register
Automatic LED DC cancellation ⁽⁵⁾	Ambient DC cancelled using Analog AACM / LED DC cancelled using Digital AACM	Controlled by Digital AACM loop ⁽⁴⁾	Controlled by Analog AACM loop	Retains value set in baseline Ambient phase	Controlled by Digital AACM loop

(1) DC subtraction in Ambient phase is always done using the Ambient Offset DAC

(2) LED Offset DAC is meant to be set to zero in Ambient phase

(3) Set USE_AMB_DAC_FOR_LED to '1'. Using the Ambient DAC for cancelling the LED DC is not recommended because glitches can occur in the (LED-AMB) data whenever there is an update of the Ambient DC by the Analog AACM loop.

(4) Set USE_AMB_DAC_FOR_LED to '0'. Also make sure that the LED Offset DAC is enabled using the register bits EN_LED_OFFDAC*.

(5) Updating the LED Offset DAC to cancel the DC in the LED phase causes a sudden change in the (LED-AMB) data and needs to be handled by the heart rate extraction algorithm.

(6) Make sure that the IFS_OFFDAC is chosen so that the Ambient Offset DAC has enough range to cancel the Ambient signal range.

The schemes are summarized below:

- **Full MCU control:**

The MCU writes an 8-bit code in the per-phase IOFFDAC_PH* register word to set the value of the Offset DAC in a baseline Ambient phase (the ambient phase which is the first phase in a sequence of phases that are expected to have the same ambient). This value serves as the baseline value for a set of subsequent phases for which the ambient can be considered to be the same (an assumption that can be the case if the same PD or set of PDs were used as in the Ambient phase where the Offset DAC baseline was programmed). The additional DC in the LED phases can be cancelled by the MCU in two ways:

1. With USE_AMB_DAC_FOR_LED bit set to '1': Specifying a code to the IOFFDAC_PH* (8-bit control) for the LED phase which represents the incremental DC level due to the LED turning on. This increment gets added to the Baseline value and applied to the Ambient Offset DAC in the LED phase. The LED Offset DAC is not used. If an increment in the Ambient Offset DAC is set to cancel the LED DC, then an update to the Ambient Offset DAC in the Ambient phase also updates with Ambient Offset DAC in the LED phase by a similar amount. This common update mostly cancels out by a subtraction of the Ambient from the LED. However, a small residual glitch can occur due to the nonlinearity of the Ambient Offset DAC
2. With USE_AMB_DAC_FOR_LED bit set to '0': Setting the LED Offset DAC to cancel the DC due to the LED turning on, by specifying the IOFFDAC_PH* in the LED phase. The Ambient Offset DAC continues to be at the Baseline value. To avoid the glitching effect due to the nonlinearity of the Ambient Offset DAC described above. TI prefers to use the LED Offset DAC to cancel the DC from the LED if the range of the LED DC is within the range supported by the LED Offset DAC (15.5 µA).

- **Analog AACM:**

The Analog AACM loop can be used to cancel the DC in the Ambient phases. In the Analog AACM scheme, a set of consecutive phases having the same Ambient signal (phases corresponding to the same PD or to the same combination of PDs) are grouped together. The first of this set of phases is defined as an Ambient phase and a convergence of the Analog AACM loop is defined at the start of this phase to acquire the baseline ambient and to update the Ambient Offset DAC. The Analog AACM loop acquires the information of the Ambient level through a convergence of the loop at the start of this phase, updates the Ambient Offset

DAC and applies the same value for the cancellation of ambient in all phases in the set. Any number of such sets of phases can be defined and the Analog AACM loop can be set to acquire the ambient freshly at the start of each set. The additional DC in the LED phase can be cancelled out through MCU control using either an increment to the Ambient Offset DAC, or by controlling the LED Offset DAC in the manner outlined in the ‘Full MCU control’ scheme. Alternatively, the LED Offset DAC can be set to be automatically cancelled by associating one of four Digital AACM loops with the LED phase. While using the scheme where the Ambient DAC is incremented in the LED phase to cancel the additional DC in the LED phase, glitches can result whenever there is an update of the Ambient DAC by the AACM loop. The frequency of such updates (and resulting glitches) depend on how close the ambient level is to the re-convergence threshold of the Analog AACM loop. The glitches are caused by the non linearity in the transfer function of the Ambient DAC current versus IOFFDAC code. Therefore, TI recommends that the additional DC in the LED phase be canceled using the LED DAC rather than through an additional increment of the Ambient DAC in the LED phase.

- **Automatic LED DC cancellation by the Digital AACM loop:**

While using the Analog AACM scheme to cancel the Ambient signal, using the Digital AACM loops to automatically cancel the additional DC in LED phases is possible. Since there are 4 Digital AACM loops, this scheme can be used to cancel the DC in up to 4 LED phases. The Automatic LED DC cancellation involves an automatic update by a Digital AACM loop to the LED Offset DAC when the signal from the PD in the LED phase changes by a value more than a threshold. This update results in a glitch in the data. Fast changing DC (for example during motion) can cause frequent glitching which can interfere with the heart rate extraction. In such a scenario, the Automatic LED DC cancellation feature can be enabled for a one-time setting of the LED Offset DAC at start of signal acquisition and then frozen to avoid further updates during signal acquisition. Alternatively, a Dummy LED phase can be defined and set to come once at the start of a time window, and the Digital AACM loop updates the LED Offset DAC only during the PRF cycle where the Dummy LED phase is active (not masked).

7.3.2.10.1 Full MCU Control

The Ambient and LED Offset DACs can be manually controlled by the MCU using the per-phase IOFFDAC_PH_TIA* register controls (separate for TIA1 and TIA2). To use the manual control of the Offset DAC use the following method:

1. Set the first phase of a group of phases as a baseline Ambient phase by setting the UPDATE_BASELINE* bit – use UPDATE_BASELINE_TIA1 for TIA1 and the UPDATE_BASELINE_TIA2 for TIA2. If both TIAs are used in the set of phases and the Ambient Offset DAC of both have to be manually controlled, then set both the UPDATE_BASELINE_TIA* bits to ‘1’.
2. Set the IOFFDAC_PH_TIA* register control to the desired 8-bit word to control the Ambient Offset DAC. This setting is used for the Ambient Offset DAC for the baseline Ambient phase and for the subsequent set of phases until the next phase where the UPDATE_BASELINE bit is set to ‘1’ again.
3. When USE_AMB_DAC_FOR_LED=0: For the subsequent phases whose Ambient Offset DAC is to be set to the same value as in the baseline Ambient phase, set the UPDATE_BASELINE_TIA* bits to ‘0’. Set the D4..D0 bits of IOFFDAC_PH_TIA* to set the control for the LED Offset DAC (make sure the LED Offset DAC is enabled).. The Ambient Offset DAC for these phases continue to be set by the setting in the most recent baseline ambient phase, and the LED Offset DAC for these phases is set by the IOFFDAC_PH_TIA* control corresponding to the phase.
4. When USE_AMB_DAC_FOR_LED=1: For the subsequent phases whose Ambient Offset DAC is to be set to the same value as the baseline Ambient phase, set the UPDATE_BASELINE_TIA* bits to ‘0’. Set the IOFFDAC_PH to set the incremental Offset DAC code corresponding to the DC from the LED turning on. The baseline value is incremented by this code and applied to the Ambient Offset DAC to cancel the DC from both the Ambient and the LED. The LED Offset DAC remains at 0. This manner of cancelling the additional DC in the LED phase using an incremental update to the Ambient Offset DAC can cause a small glitching when the Ambient DAC baseline is updated. However, using the Ambient Offset DAC to additionally cancel the LED DC offers a potentially larger range and better resolution than using the LED Offset DAC to cancel the LED DC.

The timing of the manual control scheme is shown in [Figure 7-43](#)

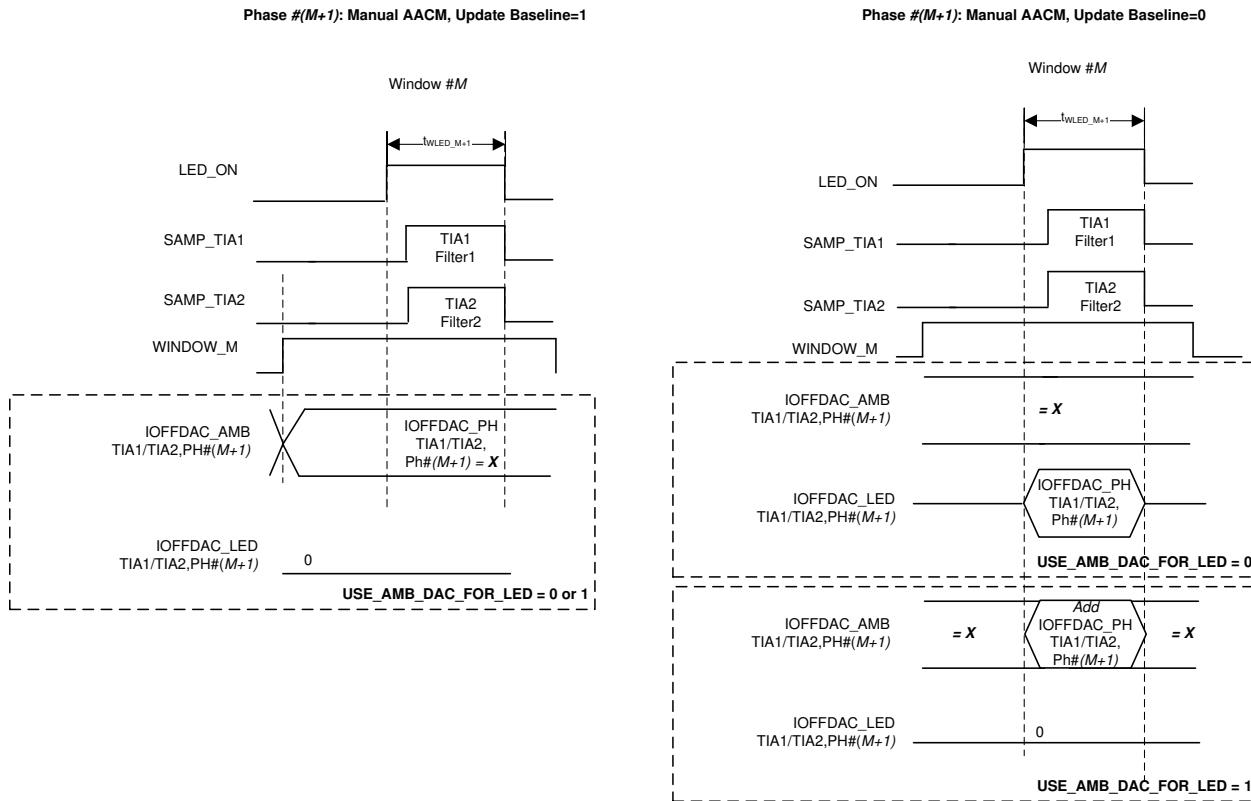


Figure 7-43. Timing of the Manual Control Scheme for the Ambient and LED Offset DACs

The above section described the setting of the Ambient and LED Offset DACs in a likely operating scenario involving a set of Ambient and LED phases - a Baseline Ambient phase followed by a set of LED and/or Ambient phases with the same ambient signal as the Baseline ambient phase. However, there can be scenarios where the LED Offset DAC in a phase needs to be forced by the IOFFDAC_PH register without consideration of the phases preceding. As an example, a calibration of the LED Offset DAC related to the functioning of the Automatic LED Cancellation loop requires setting a value for the LED Offset DAC with the Ambient Offset DAC set to 0. To set the LED Offset DAC in a phase to the value specified by the IOFFDAC_PH register (with the Ambient Offset DAC set to 0), set the UPDATE_BASELINE bit for that phase to '0' while making sure that the last previous phase that had the UPDATE_BASELINE bit as '1' had an IOFFDAC_PH setting for the Ambient Offset DAC as '0'. Also set the USE_AMB_DAC_FOR_LED to '0'.

7.3.2.10.2 Automatic Ambient Cancellation Using Analog AACM

An Analog Automatic Cancellation Mode (Analog AACM) scheme can be used to control the Ambient Offset DAC for a set of phases having the same ambient (referred to as a Common Ambient set). The Analog AACM scheme uses a short ambient acquisition window during the first phase (defined to be the baseline Ambient phase) of the Common Ambient set. The TIA output during the Ambient Acquisition window is used to estimate the Baseline Ambient level and update the Ambient Offset DAC across all phases belonging to the Common Ambient set. Set the USE_ANA_AACM_TIA1 (for TIA1) and/or USE_ANA_AACM_TIA2 (for TIA2) to '1' to associate all the phases of a Common Ambient set with the Analog AACM control. The first phase in the Common Ambient set is marked to be the Ambient Baseline phase by setting the UPDATE_BASELINE_TIA* bit to '1', and a short Ambient acquisition window (ANA_ACQ*) is automatically generated (commonly for each active TIA in that phase) prior to the start of the LED_ON signal for the phase. The setting of the Ambient Offset DAC needed to cancel the ambient is automatically determined during the ANA_ACQ* window and is used for all the phases associated with the set. In a similar manner, a new Common ambient set can be defined by setting the UPDATE_BASELINE_TIA* to '1' in the first of those set of phases and setting USE_ANA_AACM bit to '1' for all of them, and. In any of the phases, the LED Offset DAC can be additionally set using the IOFFDAC_PH register control for that phase. The registers relevant to Analog AACM operation are listed in [Table 7-42](#).

Table 7-42. Analog AACM Register Controls

Parameter	Register Control	Number of Bits	Classification	Comments
Enable LSB control of Offset DAC control	EN_AMB_DAC_LSB	1	Global control	Always set to '1'
Per-phase Analog AACM loop activation bit	USE_ANA_AACM_TIA1	1	Per-phase control (TIA specific)	Set to '1' if the phase is associated with the Analog AACM loop
	USE_ANA_AACM_TIA2	1		
Ambient Baseline Acquisition specification bit	UPDATE_BASELINE_TIA1	1	Per-phase control (TIA specific)	Set to '1' to acquire ambient baseline in that phase (for use across the Common Ambient set)
	UPDATE_BASELINE_TIA2	1		

[Figure 7-44](#) shows a generic case of how the Analog AACM loop can be used to acquire the ambient and update the Ambient Offset DAC for a set of phases with common ambient. [Figure 7-44](#) shows the phases in one PRF cycle. The cell marked in grey corresponds to the Ambient baseline phase for the Analog AACM loop. At the start of the baseline phase, a short Analog ambient acquisition window (shaded in black) is automatically generated during which the Analog AACM loop converges and acquires the ambient.

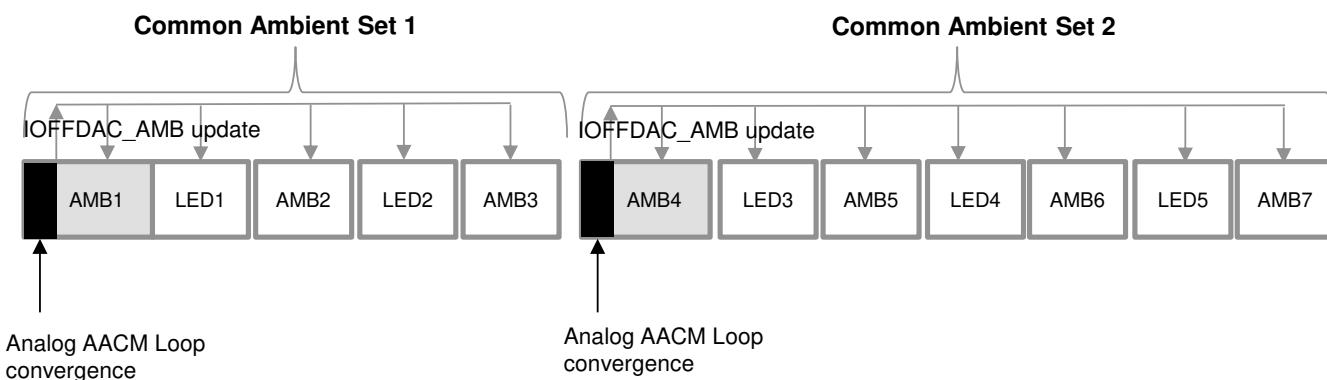


Figure 7-44. Placement of LED and AMB Phases Within One PRF Cycle Illustrating the Positioning of the Ambient Baseline Phases for the Analog AACM Loop

To illustrate the manner of setting the Analog AACM register controls, a particular case is described in [Table 7-43](#). Some of the phases are configured as Single receive phases (using only TIA1) whereas some others are configured as Dual receive phases (using both TIA1 and TIA2). The example shows a fresh convergence of the Analog AACM loop of TIA2 for Phase 3 and 4. Alternatively, since the Ambient for PD2 was already acquired in Phase 1, a Common Ambient set involving Phases 1-4 can have been defined.

Table 7-43. Example case for Illustrating Analog AACM Register Settings

Phase # ⁽¹⁾	Type of phase	PD connected to TIA1	PD connected to TIA2	Phase description
1	Dual Receive	PD1	PD2	Ambient phase for PD1 and PD2
2	Dual Receive	PD1	PD2	LED phase for PD1 and PD2
3	Single Receive		PD2	A second ambient phase for PD2
4	Single Receive		PD2	A second LED phase for PD2
5	Single Receive	PD3		Ambient phase for PD3
6	Single Receive	PD3		LED phase for PD3
7	Single Receive	PD4		Ambient phase for PD4
8	Single Receive	PD4		LED phase for PD4

(1) Like color cells correspond to a Common Ambient set.

Table 7-44 shows the register settings for the use case shown in Table 7-43.

Table 7-44. Register Settings for Case shown in Table 7-43

Phase #	TIA1 controls ^{(1) (2)}		TIA2 controls	
	USE_ANA_AACM_TIA1	UPDATE_BASELINE_TIA1	USE_ANA_AACM_TIA2	UPDATE_BASELINE_TIA2
1	1	1	1	1
2	1		1	
3			1	1
4			1	
5	1	1		
6	1			
7	1	1		
8	1			

(1) Like color cells correspond to a Common Ambient set.

(2) Empty cells imply value of '0'.

The transition of the Ambient Offset DAC and LED Offset DAC is shown in Figure 7-45 for a case where Phase 1 is used to acquire the ambient (USE_ANA_AACM*='1' and UPDATE_BASELINE_TIA*=1 for Phase 1). As a general case, Figure 7-45 shows an additional application of the Offset DAC to cancel out DC from the LED. This application is not required since the phase is an Ambient phase.

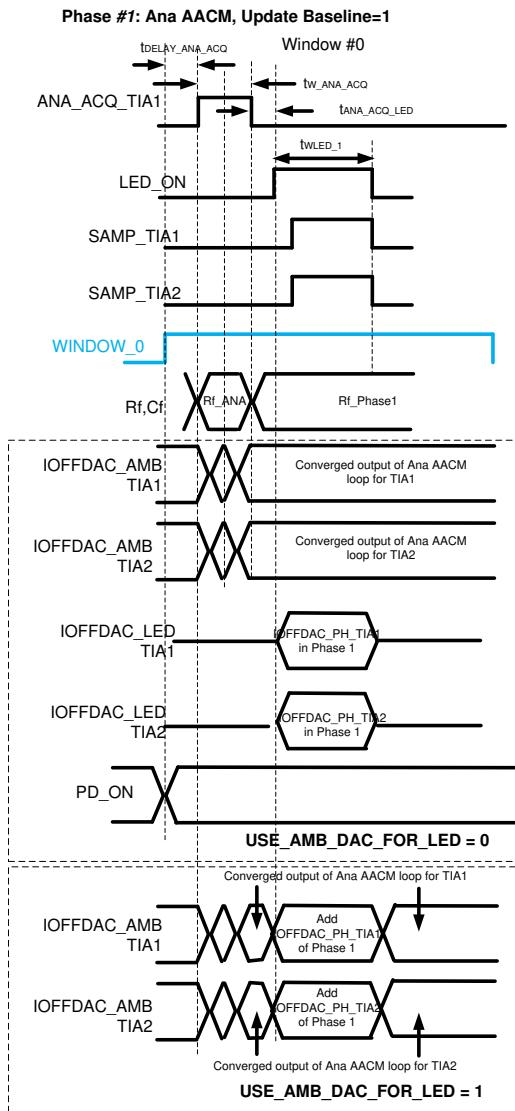


Figure 7-45. Transition of the Ambient and LED Offset DAC for a Case Where Phase 1 is Used by the Analog AACM Control Loop to Acquire the Ambient

The default width of the ANA_ACQ phase is approximately 30 us (set as 1 count for 32 kHz, 2 counts for 64 kHz and 4 counts for 128 kHz).

The parameters $t_{\text{DELAY_ANA_ACQ}}$, $t_{\text{W_ANA_ACQ}}$ and $t_{\text{SEP_ANA_ACQ_LED}}$ are calculated automatically but can be an over-ride option is available using register controls as shown in [Table 7-45](#)

Table 7-45. Timing Parameters for the Analog AACM Loop and Register Controls

Parameter	Description	Default ⁽¹⁾	To Override	Unit
$t_{DELAY_ANA_ACQ}$	Separation between start of phase window and ANA_ACQ_TIA signal	0	$REG_DELAY_ANA_ACQ \times t_{TE}$	μs
$t_W_ANA_ACQ$	Width of ANA_ACQ_TIA signal	31.25 ⁽²⁾	Set $TW_ANA_ACQ_ OVERRIDE = 1$ and program desired value as $(REG_TW_ANA_ACQ + 1) \times t_{TE}$	μs
$t_{SEP_ANA_ACQ_LED}$	Separation between ANA_ACQ_TIA signal and LED ON signal for that phase	$1 \times t_{TE}$	Set $TSEP_ANA_ACQ_LED_ OVERRIDE = 1$ and program desired value as $(REG_TSEP_ANA_ACQ_LED) \times t_{TE}$	μs

(1) Also the minimum value.

(2) For default value, number of timing engine clocks adjusted automatically (for example to $4 \times t_{TE}$ at 128 kHz) based on EXT_CLK_FREQ setting.

The R_f and C_f controls during the ANA_ACQ phase are derived from global registers RF_ANA_AACM_START_TIA1 / RF_ANA_AACM_START_TIA2 (separate controls for TIA1 and TIA2) and RF_ANA_AACM_END (common control for TIA1 and TIA2). Depending on the IFS_OFFDAC mode, set these registers to the values shown in [Table 7-46](#). Note that the code mapping the register values to the R_f settings are different from the per-phase R_f code shown in [Table 7-34](#).

Table 7-46. R_f and C_f controls during ANA_ACQ phase of the Analog AACM

IFS_OFFDAC mode	RF_ANA_AACM_START_TIA1/ RF_ANA_AACM_START_TIA2 word (in Decimal)	RF_ANA_AACM_END word (in Decimal)
1X, 2X	6	10
4X, 8X, 16X	0	5

[Figure 7-46](#) shows a case where the ambient is acquired in Phase M ($M \neq 1$). The CONV phase of Phase #(M-1) shown in dotted line can either be a single CONV signal if Phase #(M-1) is a Single receive phase or two CONV signals if Phase #(M-1) is a Dual receive phase.

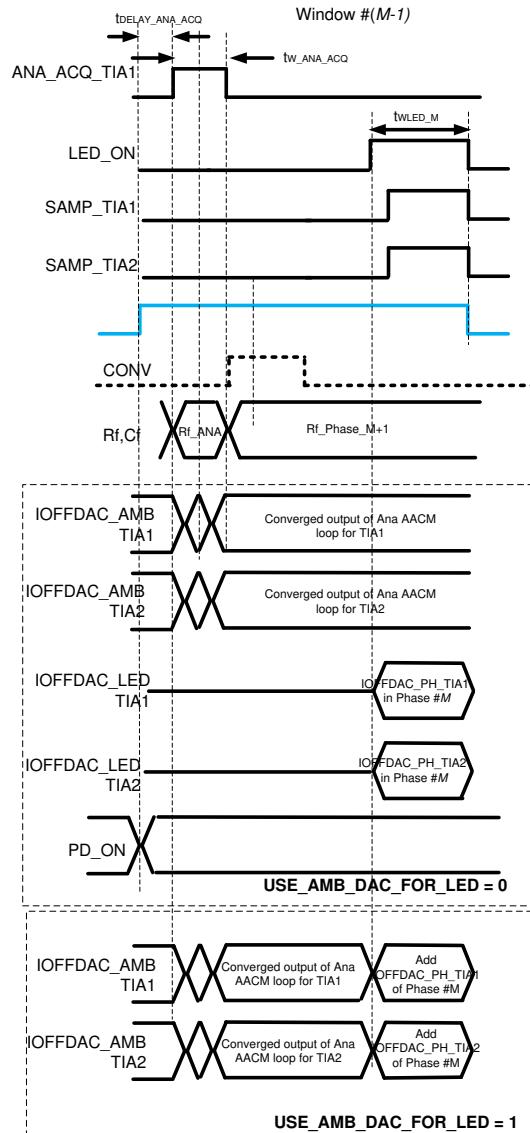


Figure 7-46. Transition of the Ambient and LED Offset DAC for a Case Where Phase M ($M \neq 1$) is Used by the Analog AACM Control Loop to Acquire the Ambient

The **IOFFDAC_AMB** code determined by the AACM loop in an Analog AACM phase marked with **UPDATE_BASELINE='1'** can be embedded into the 9 LSB of the FIFO word corresponding to that phase using the register bit **EMBED_ANA_AACM_IN_FIFO**. This mode can be used as a diagnostic mode to occasionally check the level of the ambient signal being canceled and to determine whether to switch to a different **IFS_OFFSETDAC** mode.

[Figure 7-47](#) shows the Offset DAC control in a phase that is associated with a set of Analog AACM phases, but is not the Baseline ambient phase.

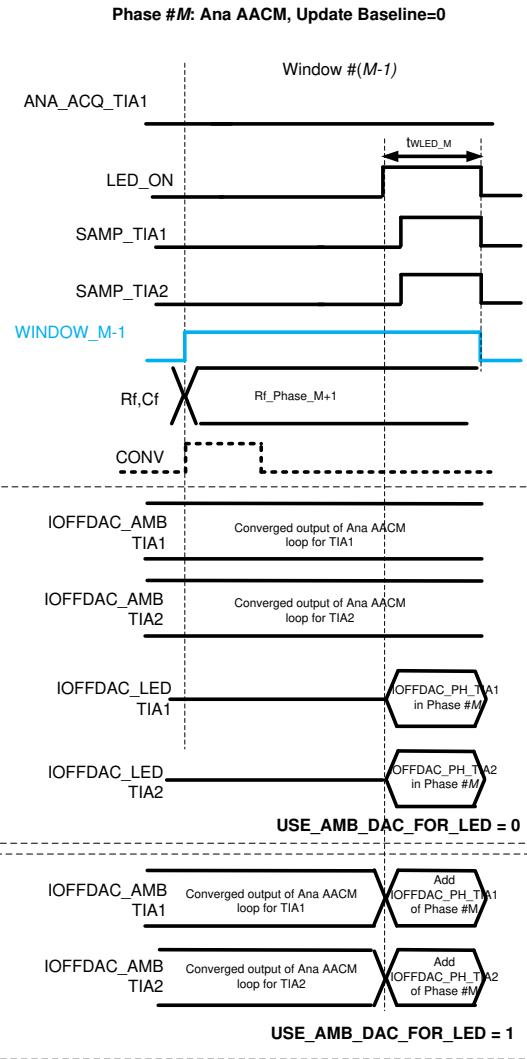


Figure 7-47. Control of the Ambient and LED Offset DAC for a Case Where the Phase is Associated with a Set of Analog AACM Phases but is not the Phase Used to Acquire the Ambient

7.3.2.10.3 Automatic LED DC Cancellation

While using the Analog AACM to control the Ambient Offset DAC and cancel the Ambient level in Common Ambient set of phases (that can typically include Ambient and LED phases), the Digital AACM loops (four in number) can be used to control the LED Offset DAC to cancel the additional DC in up to 4 LED phases. Unlike canceling Ambient using an update to the Ambient Offset DAC in both the Ambient and LED phases, cancelling additionally the DC in only the LED phase using an automatic update to the LED Offset DAC leads to glitches in the data. Whenever the PD current in the LED phase changes by more than a threshold level, the Automatic LED DC cancellation loop updates the LED Offset DAC. Therefore, this feature can be useful only in scenarios where the drift in the signal is small and/or slow.

Table 7-47 lists the register controls for Automatic LED DC cancellation using the Digital AACM loop.

Table 7-47. Automatic LED DC Cancellation Using Digital AACM - Register Controls

Parameter	Register control	Number of bits	Classification	Comments
Calibration words	CHANNEL_OFFSET_AACM_TIA1	13	Calibration word used by each loop	Channel offsets of TIA1 and TIA2
	CHANNEL_OFFSET_AACM_TIA2	13		
	CALIB_AACM_LOOP1	12		Transfer function between LED Offset DAC code and ADC output code – generated using same R_f and same TIA as associated with loop operation
	CALIB_AACM_LOOP2	12		
	CALIB_AACM_LOOP3	12		
	CALIB_AACM_LOOP4	12		
Per-phase Digital AACM Loop# association	REG_LOOP_NUM_TIA1	2	Per-phase control (TIA specific)	Set to 0,1,2 or 3 to associate Digital AACM Loops #1,2,3 or 4 with that phase
	REG_LOOP_NUM_TIA2	2		
Re-convergence threshold (ADC code at which loop re-converges)	RECONV_THRESH_AACM_LOOP1	3	Loop specific control	
	RECONV_THRESH_AACM_LOOP2	3		
	RECONV_THRESH_AACM_LOOP3	3		
	RECONV_THRESH_AACM_LOOP4	3		
Digital AACM loop output readout	IOFFDAC_AACM_READ_LOOP1	8	Loop specific output	Registers containing the current converged value (LED Offset DAC) of each of the Digital AACM loops
	IOFFDAC_AACM_READ_LOOP2			
	IOFFDAC_AACM_READ_LOOP3			
	IOFFDAC_AACM_READ_LOOP4			
Digital AACM loop output readout (polarity)	POL_OFFDAC_AACM_READ_LOOP1	1	Loop specific output	Registers containing the polarity of the LED Offset DAC for each of the LED Digital AACM loops
	POL_OFFDAC_AACM_READ_LOOP2			
	POL_OFFDAC_AACM_READ_LOOP3			
	POL_OFFDAC_AACM_READ_LOOP4			
Freeze Digital AACM loop	FREEZE_AACM_LOOP1	1	Loop specific control	Freeze the Digital AACM loop and retain the last converged value of the Offset DAC
	FREEZE_AACM_LOOP2			
	FREEZE_AACM_LOOP3			
	FREEZE_AACM_LOOP4			

Table 7-48 lists the per-phase controls associated with the Automatic LED DC Cancellation function. To do LED DC cancellation on a signal acquired using TIA1, set the per-phase bits DIG_AACM_LED_TIA1 and USE_DIG_AACM_TIA1 as shown in Table 7-48 (separate controls for TIA2). Additionally set REG_LOOP_NUM_TIA1 (and/or REG_LOOP_NUM_TIA2) to associate one of the four Digital AACM loops number (#1,#2,#3 or #4) with the cancellation of the LED DC for the signal. The associated Digital AACM loop cancels the DC from the LED by updating the LED Offset DAC. The Ambient Offset DAC can be made to retain the baseline value from the previous Ambient phase (for example, the converged value from the Analog AACM loop operating in a prior baseline Ambient phase). Set the USE_ANA_AACM_TIA1 bit to 0 for the LED DC cancellation phase. Configured in this manner, the associated Digital AACM loop uses the DC level from the

ADC output code in the LED phase to determine if the LED Offset DAC needs to be incremented/ decremented. Since the Ambient level is already cancelled through applying the Ambient Offset DAC to the latest value, the Digital AACM loop has left to cancel is the LED DC is expected.

Table 7-48. Register Controls Associated with Automatic LED DC Cancellation

Register bit controls				DC Cancellation	
USE_ANA_AACM_TIA1	USE_DIG_AACM_TIA1	DIG_AACM_LED_TIA1	UPDATE_BASELINE_TIA1	Ambient DC	LED DC
1	0	0	1	Acquire ambient baseline	N/A
1	0	0	0	Retain from previous baseline	N/A
0	1	1	1	Retain from previous baseline	Acquire and Update LED DC
0	1	1	0	Retain from previous baseline	Retain from previous phase

Figure 7-48 shows an illustration of how the Automatic LED DC cancellation functions across PRF cycles. The IOFFDAC_AMB can get updated at the end of the LED phase if the residual input current (input current minus the current value of IOFFDAC_LED) exceeds the re-convergence threshold of $\pm 0.5 \mu\text{A}$.

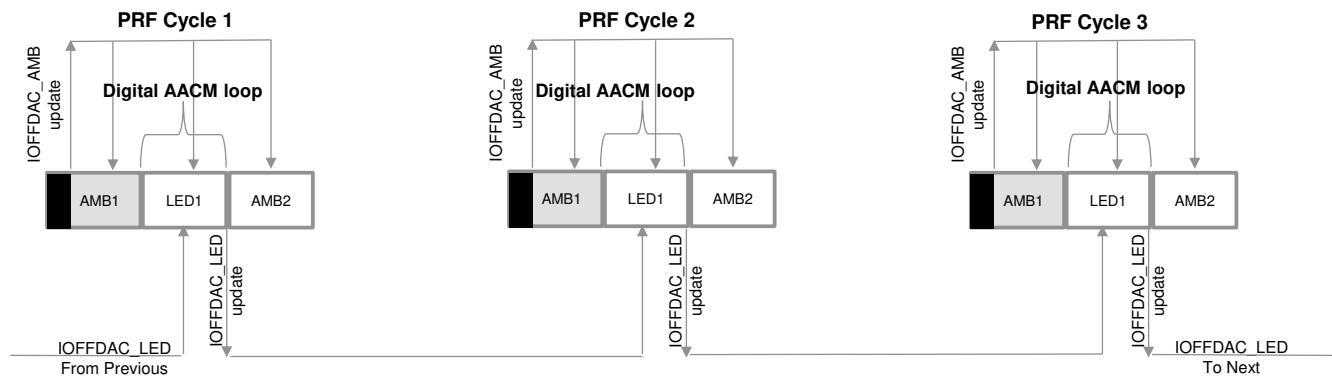


Figure 7-48. Functioning of the Automatic LED DC Cancellation Across PRF Cycles

To illustrate the manner of setting the register controls for Automatic LED DC Cancellation, a particular case is described in [Table 7-49](#). One loop is associated for each of the LED signals.

Table 7-49. Example case for illustrating LED DC Cancellation⁽¹⁾

Phase #	Type of phase	PD connected to TIA1	PD connected to TIA2	Digital AACM loop for LED DC cancellation		Phase description
				TIA1	TIA2	
1	Dual Receive	PD1	PD2			Ambient phase for PD1 and PD2
2	Dual Receive	PD1	PD2	Loop1	Loop2	LED phase for PD1 and PD2 – Use Digital AACM loops 1 and 2 to cancel LED DC
3	Single Receive		PD2			A second ambient phase for PD2
4	Single Receive		PD2		Loop3	A second LED phase for PD2 – Use Digital AACM loop 3 to cancel LED DC
5	Single Receive	PD3				Ambient phase for PD3
6	Single Receive	PD3		Loop4		LED phase for PD3 – Use Digital AACM loop 4 to cancel LED DC
7	Single Receive	PD4				Ambient phase for PD4
8	Single Receive	PD4				LED phase for PD4 – No automatic LED DC cancellation

- (1) Like color cells correspond to a set of phases with the same ambient (with the ambient signal cancelled using the same AACM loop output)

Table 7-50 shows the register settings for the case shown in Table 7-49.

Table 7-50. Register settings for example case⁽¹⁾⁽²⁾

Phase #	TIA1 controls					TIA2 controls				
	USE_ANA_AACM_TIA_1	USE_DIG_AACM_TIA_1	DIG_AACM_LED_TIA1	REG_LOOP_NUM_TIA1	UPDATE_BASELINE_TIA1	USE_ANA_AACM_TIA_2	USE_DIG_AACM_TIA_2	DIG_AACM_LED_TIA2	REG_LOOP_NUM_TIA2	UPDATE_BASELINE_TIA2
1	1				1	1				1
2		1	1	0	1		1	1	1	1
3						1				1
4							1	1	2	1
5	1				1					
6		1	1	3	1					
7	1				1					
8	1									

- (1) Like color cells correspond to a set of phases with the same ambient (with the ambient signal cancelled using the same AACM loop output)

- (2) Empty cells imply value of '0'.

While Phases 1, 3, 5 and 7 acquire the Baseline Ambient DC, Phases 2, 4 and 6 acquire the LED DC.

Note that the Ambient DC level is common between the LED and Ambient phases, and therefore a change in the Ambient Offset DAC is transparent when the Ambient phase output is digitally subtracted from the LED phase output. However, a change in the LED Offset DAC happens only in the LED phase. Therefore, an update to the LED Offset DAC can cause a step change in the (LED-Ambient) data as shown in Figure 7-49.

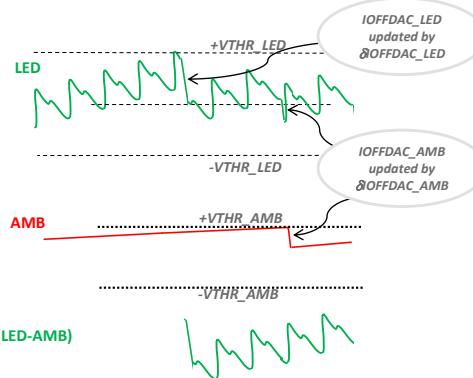
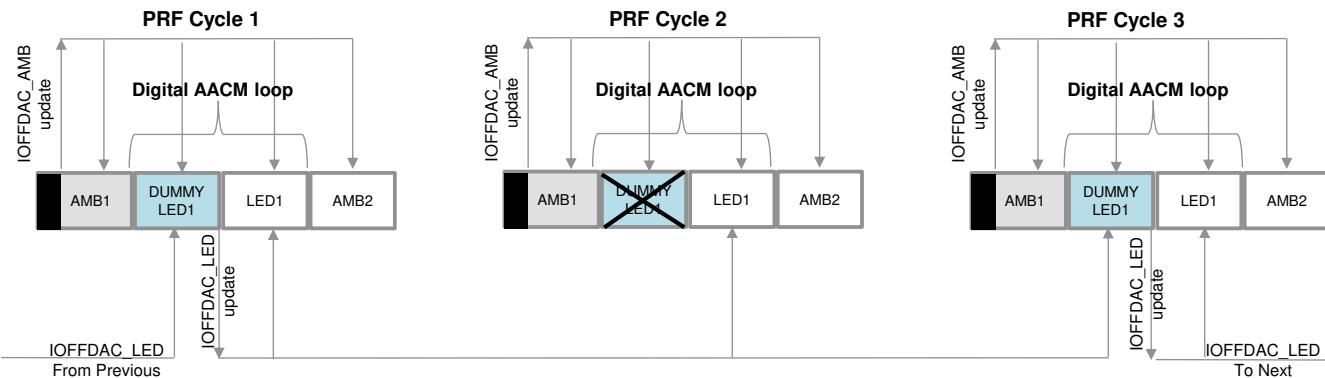


Figure 7-49. Glitch in (LED-AMB) Data When LED Offset DAC is Updated

By introducing a *Dummy LED* phase preceding the actual LED phase, and by setting the masking factor of the Dummy LED phase to a high enough value, a time window can be defined wherein the Digital AACM loop controlling the LED DC ceases to update the LED Offset DAC, thereby avoiding sudden jumps in the LED's DC within this window. By setting an appropriate masking for the Dummy LED phases using the REG_MASK_FACTOR, the update of the LED Offset DAC can be constrained to happen at the start of a time window corresponding to a set of REG_MASK_FACTOR PRF cycles. The heart rate estimation algorithm can do appropriate adjustment to the signal processing to deal with the potential steps in the LED data caused due to update in the LED Offset DAC at the start of this time window. Setting a high REG_MASK_FACTOR in the Dummy LED phase reduces the occurrence of the steps in the data, and also reduces the power overhead from having to fire the LED in the Dummy LED phase. However, the channel gain needs to be set to a low enough value that the drift in the LED phase DC over the time window does not cause the channel to saturate. Note that the LED current setting needs to be same between the Dummy LED phase and the actual LED phase. Figure 7-50 shows an illustration of how the Automatic LED DC cancellation using the Dummy LED phase functions across PRF cycles. The Dummy LED phase is shown to have a masking factor of 2 so that the Dummy LED phase is masked every alternate PRF cycle. A fresh update of the LED Offset DAC can happen during an active Dummy LED phase and the update gets applied to the succeeding LED phase until the next occurrence of the Dummy LED phase.



- A. In this example, the Dummy LED phase is set to have a masking factor of 2.

Figure 7-50. Functioning of the Automatic LED DC Cancellation Using the Dummy LED Phase Across PRF Cycles

Note that while operating in this manner with the Dummy phase also defined, the phases must be operated in a staggered manner so that the CONV signal of the Dummy LED phase completes before the start of the LED ON signal of the following LED phase.

The use case shown in Table 7-49 is repeated in Table 7-51 but with the Dummy LED phases now included. The Digital AACM loop convergence and LED Offset DAC update happens in Phases 2, 5, and 8 and the LED Offset DAC update is applied for Phases 3, 6, and 9 respectively.

Table 7-51. LED DC Cancellation with Dummy LED Phases Inserted⁽¹⁾

Phase #	Type of phase	PD connected to TIA1	PD connected to TIA2	Digital AACM loop for LED DC cancellation		Phase description
				TIA1	TIA2	
1	Dual Receive	PD1	PD2			Ambient phase for PD1 and PD2
2	Dual Receive	PD1	PD2	Loop1	Loop2	Dummy LED phase - Use Digital AACM loops 1 and 2 to cancel LED DC in Phase 2 and Phase 3
3	Dual Receive	PD1	PD2	Loop1	Loop2	LED phase for PD1 and PD2
4	Single Receive		PD2			A second ambient phase for PD2
5	Single Receive		PD2		Loop3	Dummy LED phase - Use Digital AACM loop 3 to cancel LED DC in Phase 5 and Phase 6
6	Single Receive		PD2		Loop3	LED phase for PD2
7	Single Receive	PD3				Ambient phase for PD3
8	Single Receive	PD3		Loop4		Dummy LED phase - Use Digital AACM loop 4 to cancel LED DC in Phase 8 and Phase 9
9	Single Receive	PD3		Loop4		LED phase for PD3
10	Single Receive	PD4				Ambient phase for PD4
11	Single Receive	PD4				LED phase for PD4 – No automatic LED DC cancellation

(1) Like color cells correspond to a set of phases with the same ambient (with the ambient signal cancelled using the same AACM loop output)

Table 7-52 shows the register settings for the case shown in Table 7-51 .

Table 7-52. Register Settings for Example Case⁽¹⁾

Phase #	TIA1 controls					TIA2 controls				
	USE_ANA_AACM_TI_A1	USE_DIG_AACM_TI_A1	DIG_AAC_M_LED_TI_A1	REG_LOO_P_NUM_TI_A1	UPDATE_BASELINE_TIA1	USE_ANA_AACM_TI_A2	USE_DIG_AACM_TI_A2	DIG_AAC_M_LED_TI_A2	REG_LOO_P_NUM_TI_A2	UPDATE_BASELINE_TIA2
1	1				1	1				1
2		1	1	0	1		1	1	1	1
3		1	1	0			1	1	1	
4						1				1
5							1	1	2	1
6							1	1	2	
7	1				1					
8		1	1	3	1					
9		1	1	3						
10	1				1					
11	1									

(1) Like color cells correspond to a set of phases with the same ambient (with the ambient signal cancelled using the same AACM loop output)

By setting an appropriate masking for the Dummy LED phases using the REG_PH_MASK_FACTOR, the update of the LED Offset DAC can be constrained to happen at the start of a time window corresponding to a set of PH_MASK_FACTOR PRF cycles. The heart rate estimation algorithm can do appropriate adjustment to the signal processing to deal with the potential steps in the LED data caused due to update in the LED Offset DAC at the start of this time window. Setting a high PH_MASK_FACTOR in the Dummy LED phase reduces the

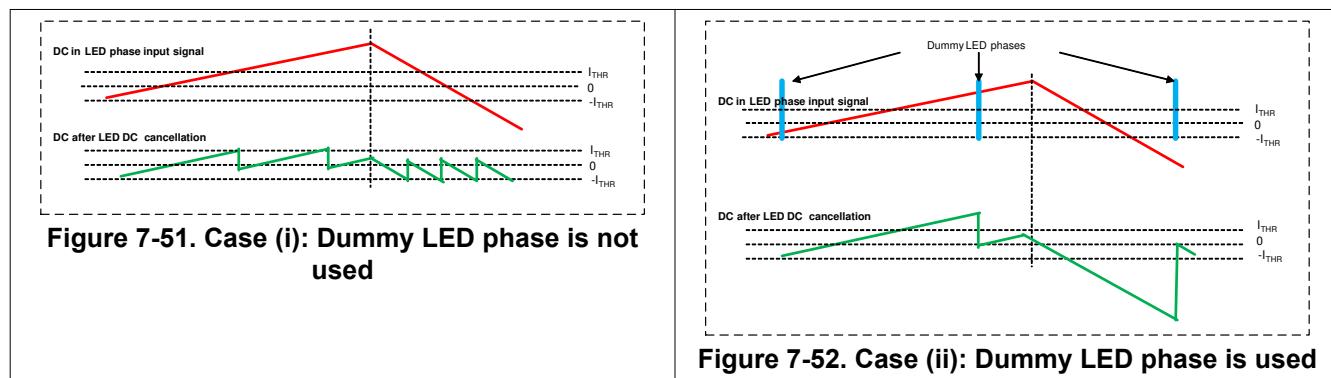
occurrence of the steps in the data, and also reduces the power overhead from having to fire the LED in the Dummy LED phase. However, the channel gain needs to be set to a low enough value that the drift in the LED phase DC over the time window does not cause the channel to saturate. Note that the LED current setting needs to be same between the Dummy LED phase and the actual LED phase.

Re-convergence Threshold setting for LED DC Cancellation

With the Automatic LED DC cancellation enabled, the effective input current to the TIA is the residual value of the PD current after subtraction of the converged value of the LED Offset DAC. The LED DC cancellation updates the LED Offset DAC based on the residual input current in terms of number of LSBs of the LED Offset DAC ($I_{LSB_LED_DAC} \sim 125 \text{ nA}$) exceeding a programmed threshold value set by register RECONV_THRESH_AACM_LOOP1 (for Loop1). There are separate controls for each of the 4 loops. The residual current corresponding to the re-convergence threshold is given by: $\pm I_{THR} = \pm(2^{RECONV_THRESH_AACM_LOOP1}) \times I_{LSB_LED_DAC}$

For example, if the RECONV_THRESH_AACM_LOOP1 is set to 3, then I_{THR} is equal to $1 \mu\text{A}$. So every time the residual current reaches $1 \mu\text{A}$ or $-1 \mu\text{A}$, re-convergence of the loop is triggered and the LED Offset DAC is updated.

An illustration of LED DC Cancellation is shown for the two cases – (i) Dummy LED phase is not used (ii) Dummy LED phase is used in conjunction with a masking factor is shown in [Figure 7-51](#) and [Figure 7-52](#) respectively. In (i), the LED Offset DAC gets updated every time I_{THR} (the threshold input current level) is crossed, whereas in Case (ii), the LED Offset DAC updates happen only if I_{THR} is crossed during the PRF cycle during which the Dummy LED phase is unmasked.



Calibration for the Automatic LED DC Cancellation

The detection of the ambient current reaching the re-convergence threshold and the subsequent cancellation is achieved by the Digital AACM loop through monitoring the ADC output code in the LED (or Dummy LED) phase and incrementing or decrementing the LED Offset DAC code. Since the transfer function between the LED Offset DAC code and the ADC output code is affected by part-to-part variations in gain (Rf) and Offset DAC, as well as channel offset, TI recommends that the MCU run a calibration routine after device power up, and writes the calibration words into designated registers. These calibration words serve as reference for the one or more Digital AACM loops to accurately translate the ADC output code to an appropriate increment or decrement to the LED Offset DAC to cancel the DC from the LED. The calibration words can be written one-time as part of the device initialization and left unchanged subsequently. Note that the registers get erased every time the device is power cycled or when the device comes out of the hardware power-down mode; therefore, the registers need to be re-written.

There are 2 sets of calibration words:

1. Gain calibration word for each Digital AACM loop that is used (for example CALIB_AACM_LOOP1 if Digital AACM loop 1 is used). This word is a representation of the ADC output code change caused by 1 LSB change to the LED Offset DAC, and must be generated using the same TIA with the same Rf as what is used in the LED phase corresponding to that loop.

2. Offset calibration word for each TIA that is used (CHANNEL_OFFSET_AACM_TIA1 for TIA1 and CHANNEL_OFFSET_AACM_TIA2 for TIA2). These calibration words are representations of the ADC output code corresponding to the channel offsets when the particular TIA is used.

A coarse functioning of the Digital AACM loop can be achieved by setting the Offset calibration words to '0' and by setting the gain calibration words to the value indicated in [Table 7-53](#). Note that in this table, 'TIA gain' corresponds to the R_f setting in the LED phase. TI requires to limit the setting of R_f to a maximum setting of 250 KΩ while using the Automatic LED DC cancellation feature.

Table 7-53. Approximate Decimal Equivalent Code of the CALIB_AACM_LOOP Word for LED DC Cancellation

IFS_LED_OF_FDAC	CALIB_AACM_LOOP based on setting of TIA gain (R_f)							
	25 KΩ	50 KΩ	100 KΩ	166 KΩ	200 KΩ	250 KΩ	500 KΩ	1000 KΩ
31.875 μA	21	43	85	142	171	213	427	853
63.75 μA	43	85	171	283	341	427	853	Do not Use⁽¹⁾

(1) Do not use these combinations of TIA gain and Offset DAC full scale mode.

For a more accurate functioning of the AACM, TI strongly recommends to run a calibration routine on start-up to accurately determine the calibration words. The calibration routine is described below:

1. Set the PD_DISCONNECT mode to disconnect all the PDs from the TIA.
2. Regardless of the polarity of the Photodiode connection to the AFE input pins, set POL_OFFSETDAC_LED to '0' while performing calibration. Also make sure that the LED Offset DAC is enabled (EN_LED_OFFSETDAC_TIA1, EN_LED_OFFSETDAC_TIA2).
3. To generate the calibration words corresponding to a specific R_f (the same R_f as is intended for the LED phase whose DC is being cancelled), program the AFE to operate with two phases (REG_NUMPHASE=1) both with the same R_f setting. Using the Manual MCU control mode, set the LED Offset DAC to 0 LSB and 1 LSB in the two phases respectively. The Ambient Offset DAC must be set to 0 μA during this calibration. Program the LED Offset DAC currents as shown in [Table 7-54](#).

Table 7-54. Configuration of Phase Settings in the Calibration Routine for Automatic LED DC Cancellation

Phase #	1	2
IOFFDAC_PH (set) ⁽¹⁾	00000000	00000001 ⁽²⁾
UPDATE_BASELINE_TIA1/ TIA2	1	0
Measured Output code (22 bit)	CODE1	CODE2

(1) Set POL_OFFDAC_LED to 0.

(2) Set USE_AMB_DAC_FOR_LED bit to '0' to set the LED Offset DAC to 1 LSB in this phase.

4. Derive the CALIB_AACM_LOOP word using CODE1 and CODE2 as shown in [Figure 7-53](#). Here, CODE1 and CODE2 are the 22-bit output word from the AFE.

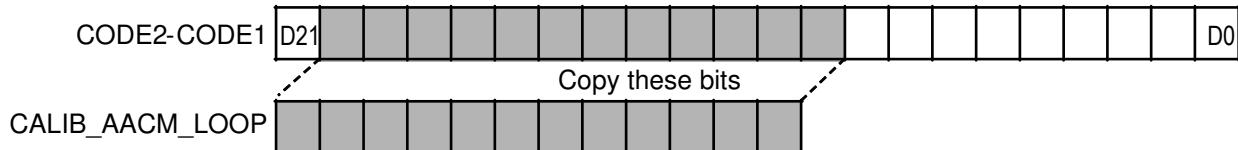


Figure 7-53. Derivation of the CALIB_AACM_LOOP Word

5. Derive the CHANNEL_OFFSET_AACM calibration word as shown in [Figure 7-54](#).

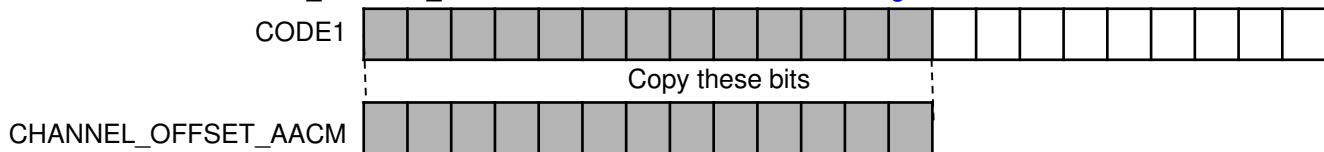


Figure 7-54. Derivation of the CHANNEL_OFFSET Word

6. Write the above derived codes for CALIB_AACM_LOOP* and CHANNEL_OFFSET_AACM* to the corresponding registers

7.3.2.10.4 Dynamic Range Extension Mode

The Automatic LED DC cancellation mode introduces a step in the LED phase data every time the LED Offset DAC is updated. By enabling the Dynamic Range Extension (DRE) mode, the steps can be removed and the dynamic range of the AFE can be significantly increased for a smooth, step-free operation over a dynamic range which is several times higher than the dynamic range of the ADC. What this achieves in effect is an ability to operate at a high TIA gain setting (which results in low noise operation) while extending the dynamic range to a value corresponding to a low TIA gain setting. The dynamic range can be extended up to a factor of 64, which means that a dynamic range of up to 32 μ A can be achieved for a TIA gain setting of 1 M Ω which otherwise supports an input dynamic range of only 0.5 μ A.

The DRE scheme is illustrated in [Figure 7-55](#)

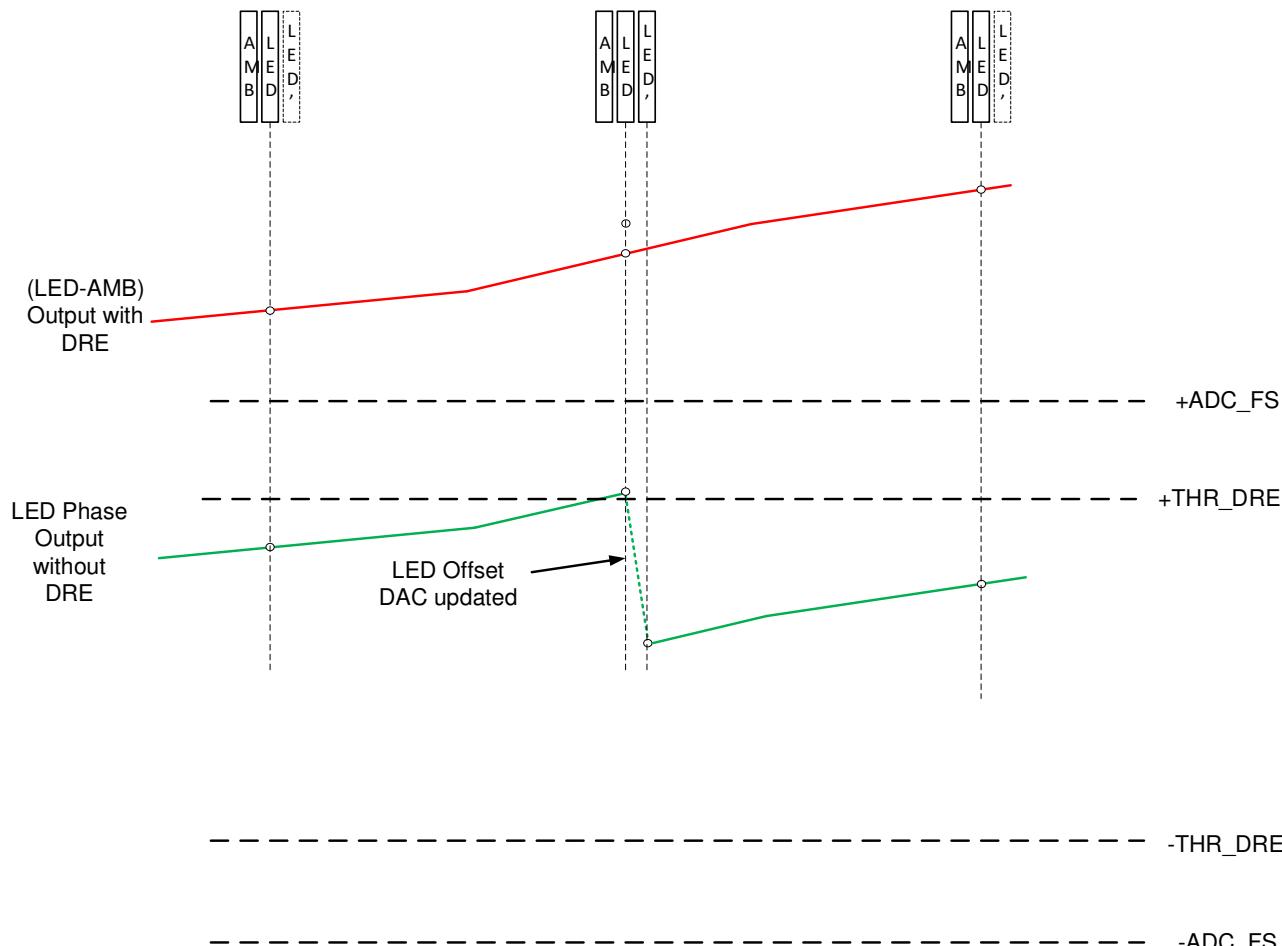


Figure 7-55. Illustration of the Dynamic Range Extension (DRE) Mode

The DRE mode is enabled through the following means:

1. Define two LED phases for every one LED phase data. This is done similar to the sequence of Dummy LED followed by actual LED phase in the Automatic LED DC Cancellation mode. However, in the DRE mode, the first LED phase in the sequence is the actual LED phase (LED) where signal is acquired, and the second LED phase (LED') in the sequence is an On-demand LED phase. Set the LED current in both phases to the same value. While the first LED phase is fired in every PRF cycle, the On-demand LED phase is fired only on-demand whenever there is an update of the Offset DAC as determined based on the ADC output of the first LED phase.
2. Associate a Digital AACM loop with the pair of the (first) LED & (second) On-demand LED phase, setting the loop to be updated based on the output of the (first) LED phase.

3. Set the ENABLE_DRE register word (3-bit) to '111'. The ENABLE_DRE setting is common to all the 4 Digital AACM loops.
4. Program the THR_DRE register word (6-bit) as the upper 6 bits (D20..D15) of the ADC code threshold at which the DRE loop updates the LED Offset DAC. The THR_DRE setting is common to all the 4 Digital AACM loops.
5. Set REG_SCALE_DRE_LOOPx register word (3-bit word, one for each Loop number, x: 1..4) to represent the factor by which the Dynamic range is to be extended. The dynamic range gets extended by a factor SCALE_DRE equal to $2^{\text{REG_SCALE_DRE_LOOP}x}$. REG_SCALE_DRE_LOOPx takes values from 0 to 5, resulting in SCALE_DRE taking values from 1 to 32. The ADC range is extended to represent the extension of the AFE dynamic range by right-shifting the bits by a number of bits equal to SCALE_DRE. The 22-bit output of the AFE is now a representation of the extended dynamic range. Figure 2 shows the right-shifting of the bits to accommodate the dynamic range extension for a case where SCALE_DRE is programmed to 8.
6. Set the FIFO_DATA_CTRL setting in the LED phase to '2' so that it outputs the (LED-AMB) data with the dynamic range extension automatically implemented by the DRE logic.

Note

While using the DRE mode, the recommended setting of NUMAV is 1 (REG_NUMAV = 0). This helps minimize the time for the CONV of the LED phase to complete before the start of LED' phase. While using the DRE mode, do not use REG_NUMAV settings of 2, 4, 9, 10, 11, 12 or 14 (corresponding to NUMAV of 3, 5, 10, 11, 12, 13, or 15)

Note

When operating in the DRE mode, the phase where LED DC cancellation is enabled has to be set as a Single TIA phase with only TIA1 enabled. If TIA2 is also enabled for a DRE phase, then the DRE logic applies a faulty offset DAC update to TIA2 even if LED DC cancellation is not enabled on TIA2.

Figure 7-56 shows the right-shifting of the bits to accommodate the dynamic range extension for a case where SCALE_DRE is programmed to 2^3 .

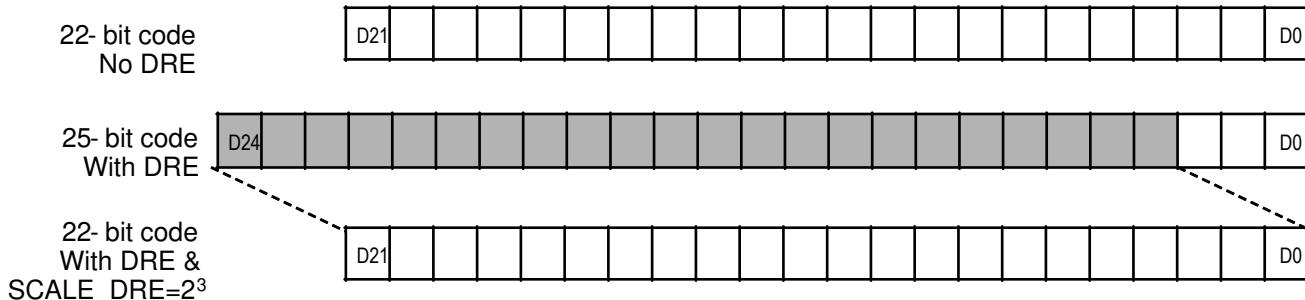


Figure 7-56. Right-Shifting of Bits with DRE Enabled and SCALE_DRE set to 2^3

Table 7-55 shows the DRE settings associated with Figure 7-56.

Table 7-55. DRE Settings Associated with Figure 7-56 (1)

Phase #	USE_ANA_AACM_TIA1	USE_DIG_AACM_TIA1	DIG_AACM_LED_TIA1	REG_LOOP_NUMBER_TIA1	UPDATE_BASELINE_TIA1	FIFO_DATA_CTRL
AMB	1(2)				1(2)	1
LED		1(3)	1(3)	0(4)	1(5)	2(6)
LED		1(3)	1(3)	0(4)		1

(1) Additionally program registers ENABLE_DRE, THR_DRE, REG_SCALE_DRE_LOOP1

(2) Analog AACM loop acquires the Ambient and updates the baseline in the AMB phase

(3) Digital AACM loop associated with LED and LED' phases

(4) Digital AACM Loop number 1 associated with the LED and LED' phases

(5) LED Offset DAC baseline updated based on the output of the LED phase

(6) LED phase output is the (LED-AMB) data after dynamic range extension

Figure 7-57 shows the PPG raw data for a few cases:

1. (a) $R_f = 25 \text{ k}\Omega$, No DRE: The PPG signal is seen to be within the ADC full scale range but the AC signal is small and noise is high.
2. (b) and (c) $R_f=500 \text{ k}\Omega$, With Automatic LED DC cancellation, DRE disabled and re-convergence threshold (RECONV_THR_AACM_LOOP) set to '1': The AC signal has gotten amplified but the steps because of the LED offset DAC updates cause the PPG signal to become distorted.
3. (d), (e) & (f) $R_f = 500 \text{ k}\Omega$, With Automatic LED DC cancellation, DRE enabled: The amplified AC signal is restored and the steps are removed by enabling the DRE.

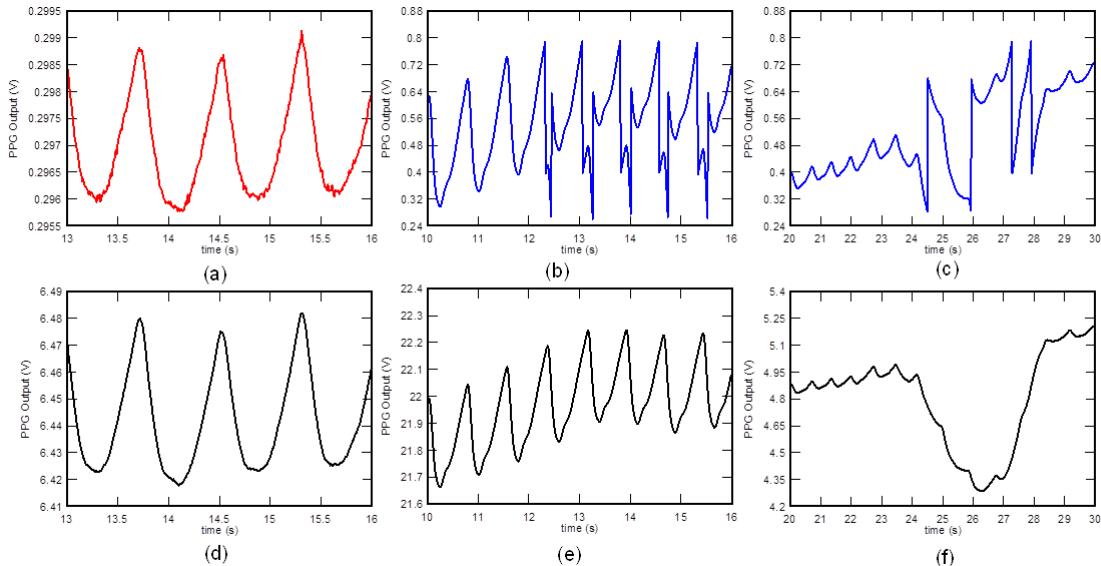


Figure 7-57. PPG raw data without (waveforms on top) and with (waveforms at the bottom) DRE enabled

7.3.3 ECG Signal Chain

7.3.3.1 Overview

The ECG signal chain is shown in [Figure 7-58](#). It consists of a DC-coupled instrumentation amplifier (INA) with an integrated high-pass filter (HPF), the corner frequency of which is set using external capacitor. The HPF enables higher INA gain while supporting large DC/low frequency differential offset. To reduce the transient time for the HPF to recover from an input transient, mechanisms of saturation detection and HPF reset are built into the ECG signal chain.

The INA gain is programmable between 11 and 21. The output of the INA is filtered with a 300Hz integrated low pass filter (LPF) and then converted by the on-chip ADC. The LPF filters the noise from the INA and external protection resistors before sampled by the ADC and serves as an anti-aliasing filter. At the input of INA, there are low-power AC/DC lead detection blocks. Lead on/off interrupts can be generated and output on the GPIO pins to alert the host to changes in the lead status

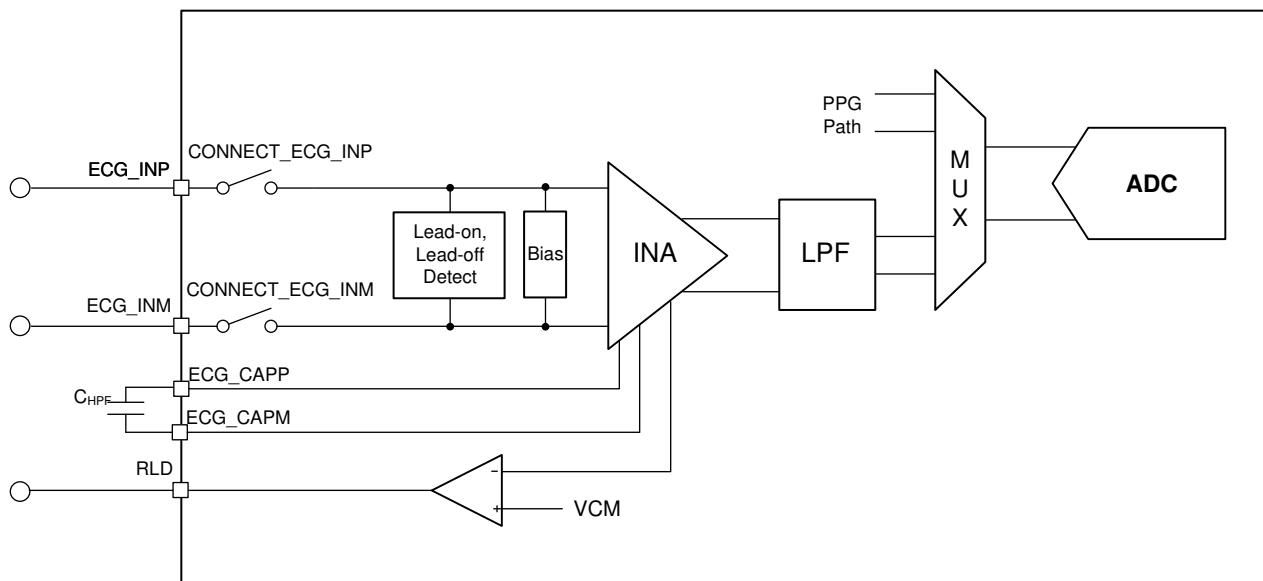


Figure 7-58. ECG Signal Chain

The ECG signal chain is inactive (powered down) when operating in the PPG acquisition mode and gets enabled in the Mixed acquisition and ECG acquisition modes. To configure the ECG signal chain in a manner that it starts acquiring ECG signals as soon as the mode is switched to the ECG or Mixed acquisition modes, the following register bits need to be set on powerup after the device reset:

- Set EN_ECG_SIG_CHAIN to make the ECG signal chain active as soon as mode is switched from PPG acquisition mode
- Set bits CONNECT_ECG_INP and CONNECT_ECG_INM to connect the ECG input pins ECG_INP and ECG_INM respectively to the INA inputs

Figure 7-59 and Figure 7-60 shows the typical frequency response of the ECG receiver arising out of the HPF and LPF.

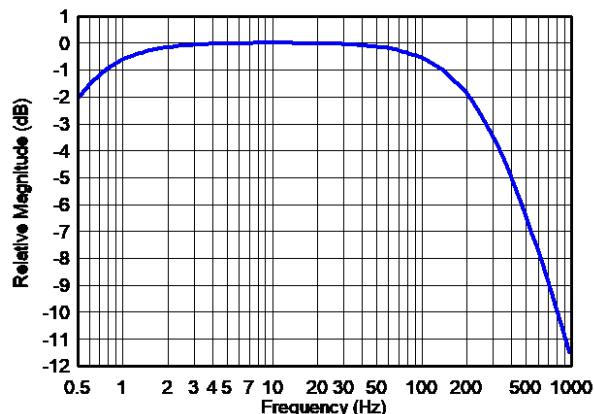


Figure 7-59. Normalized Typical Amplitude Response

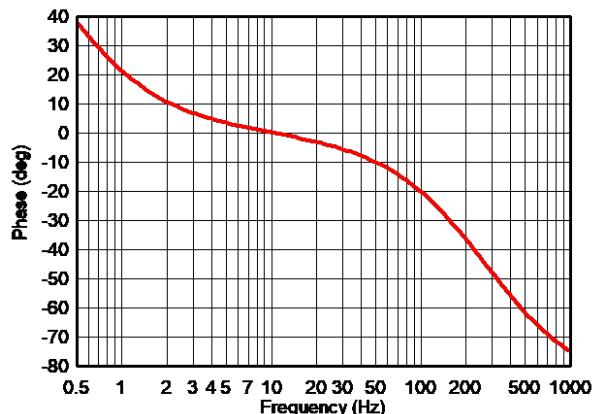


Figure 7-60. Typical Phase Response

7.3.3.2 Instrumentation Amplifier (INA)

The front end of the ECG signal chain is an INA with a programmable gain which can be programmed between values 11 and 21 (closest approximate integer) using the register control ECG_INA_GAIN as shown in [Table 7-56](#)

Table 7-56. ECG Gain Programming Register

ECG_INA_GAIN register	INA gain (closest approximate integer)
000	21
001	11

The INA has low frequency noise that can affect the ECG signal acquisition. A chopping circuit in the INA shifts the low frequency noise from the ECG signal chain to a higher frequency and gets filtered.

Note

A portion of the INA circuit runs off a boosted supply (charge pump). While operating in the LDO enable mode, set TM_BOOST_SEL = 1 for RX_SUP < 2.3 V.

7.3.3.3 Low pass filter (LPF)

The ECG signal chain has a LPF at a 3-dB corner of ~300 Hz (untrimmed) at the INA output. The LPF can help filter the high frequency noise from the INA as well as noise from external sources before signal conversion by the ADC. The LPF is enabled by default and can be bypassed by setting the DIS_LPF_ECG bit to '1'.

7.3.3.4 Right-leg drive (RLD) Amplifier

To utilize the full output range of the INA, the ECG input pins are meant to operate with an internally generated optimal common mode voltage referred to as VCM. A feedback circuit using an RLD amplifier can be used to generate a bias voltage called RLD which tracks the VCM voltage. The RLD pin can be connected to a third electrode driving the body such that the body, and thereby the input pins are biased at the optimal value. The scheme of generation of RLD output is shown in [Figure 7-61](#). Use an external 100 pF capacitor on RLD pin.

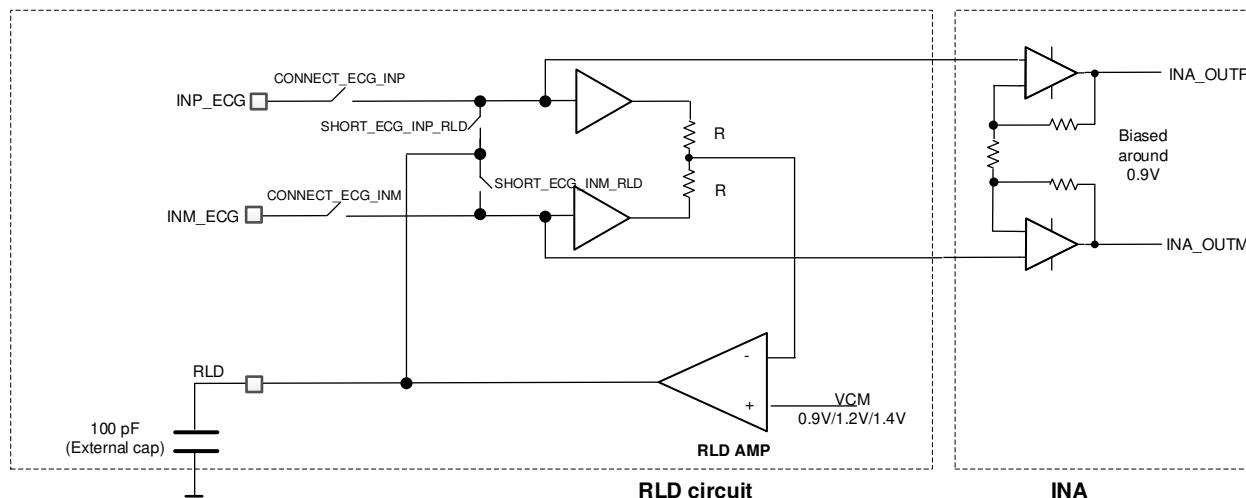


Figure 7-61. RLD Circuit Scheme

The ECG input pins (ECG_INP, ECG_INM) can be internally shorted to RLD through switches using the register bits SHORT_ECG_INP_RLD and SHORT_ECG_INM_RLD. This mode is a diagnostic mode (for example to measure the noise of the ECG signal chain) and is not meant to be used in normal operation.

The VCM voltage sets the target voltage for the RLD amplifier. Depending on the operating range of RX_SUP, the VCM voltage needs to be adjusted between 0.9V, 1.2V and 1.4V using the PROG_VCM_RLD register as shown in [Table 7-57](#). Note that the output common mode of the INA is decoupled from its input common mode, and stays at 0.9V irrespective of the programmed VCM.

Table 7-57. Programmability of the RLD reference voltage using the PROG_VCM_RLD register

PROG_VCM_RLD register	In LDO Bypass mode	In LDO Enable mode
0	0.9 ⁽¹⁾	1.4 ⁽²⁾
1	0.85	1.35
2	0.95	N/A
3	N/A	0.9 ⁽³⁾
4	N/A	0.85
5	N/A	0.95
6	0.65	1.2 ⁽⁴⁾
7	1.15	N/A

(1) Recommended setting while operating in the LDO bypass mode.

(2) Recommended setting while operating in the LDO enable mode with $2.6 \text{ V} \leq \text{RX_SUP} \leq 3.6 \text{ V}$.

(3) Recommended setting while operating in the LDO enable mode with $1.9 \text{ V} \leq \text{RX_SUP} \leq 2.1 \text{ V}$.

(4) Recommended setting while operating in the LDO enable mode with $2.1 \text{ V} \leq \text{RX_SUP} \leq 2.6 \text{ V}$.

The RLD amplifier normally operates in feedback, suppressing any common mode tone picked up by the body by applying an appropriate out-of-phase signal on the RLD electrode. The RLD amplifier can be optionally configured using the CONFIG_RLD_AS_UGB register bit as a unity gain buffer that drives a fixed output voltage on the RLD pin. Such a configuration is useful when biasing the ECG input pins to RLD using the internal bias resistors when operating in a two electrode configuration.

7.3.3.5 High Pass Filter (HPF)

The ECG signal chain has an integrated high pass filter (HPF) that rejects the DC and low frequency differential offset at the ECG inputs and allows setting a high INA gain. The corner of the HPF is set by the external capacitor (C_{HPF}) connected between CAP_P and CAP_M pins as:

$$f_{\text{HPF}} = 1 / 2\pi R_{\text{HPF}} C_{\text{HPF}} \quad (4)$$

where

- $R_{\text{HPF}} = 40 \text{ k}\Omega$

For example, a C_{HPF} of $10\mu\text{F}$ results in a corner frequency, $f_{\text{HPF}} = 0.4\text{Hz}$. A sudden change in the input differential DC voltage can cause the INA output to saturate. The HPF has an associated settling time to track the change in the differential voltage. For a filter time constant of $\sim 400\text{ms}$ (corresponding to the corner frequency of 0.4Hz), the HPF takes about ~ 2 seconds (5 time constants) to recover from the sudden change in the differential voltage. Such a high settling time is not desirable. The AFE has an in-built mechanism for Saturation detection and HPF reset to achieve fast recovery. By detecting saturation and resetting the HPF, recovery times as small as 100 ms can be achieved for a C_{HPF} of $10\mu\text{F}$. Resetting the HPF involves reducing the time constant of the HPF by reducing the value of R_{HPF} when the HPF Reset pulse is active. The ECG samples acquired during the HPF reset can be tagged to distinguish them. The 2-bit tag replaces the two LSBs of the data word. The data tagging is enabled by setting EN_DATA_MARKER to '1'.

While a value of $10 \mu\text{F}$ results in a typical HPF corner frequency of 0.4 Hz , variations in R_{HPF} from unit to unit, and tolerance and voltage de-rating of C_{HPF} may cause a deviation of f_{HPF} from its typical value. To keep f_{HPF} within 0.5 Hz , it is therefore recommended to use a value of C_{HPF} higher than $10 \mu\text{F}$ - for example, C_{HPF} may be realized as a parallel combination of three $4.7 \mu\text{F}$ capacitors or a $4.7 \mu\text{F}$ capacitor in parallel with a $10 \mu\text{F}$ capacitor.

7.3.3.5.1 Saturation Detection

There are two ECG saturation detection methods:

1. *Analog saturation detection* done based on the INA output
2. *Digital saturation detection* done based on the ADC output.

Analog saturation detection is done using four comparators at the INA output as shown in [Figure 7-62](#). The comparators are disabled by default and can be enabled by setting the register bit EN_INA_OUT_COMP.

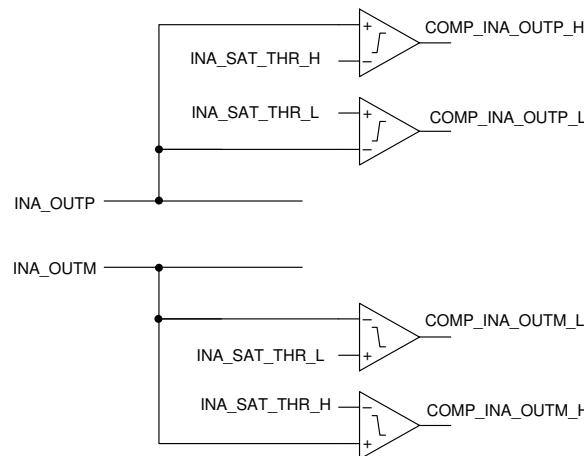


Figure 7-62. INA Output Comparators for Analog Saturation Detection

The comparator threshold voltages INA_SAT_THR_H and INA_SAT_THR_L are programmable using register controls PROG_INA_SAT_THR_H and PROG_INA_SAT_THR_L respectively as shown in [Table 7-58](#) and [Table 7-59](#).

Table 7-58. Programming the Analog Saturation Detection Comparator Threshold High Voltages

PROG_INA_SAT_THR_H Register Value	INA_SAT_THR_H voltage
0	1.3 V
1	1.35 V
2	1.4 V
3	1.45 V

Table 7-59. Programming the Analog Saturation Detection Comparator Threshold Low Voltages

PROG_INA_SAT_THR_L Register Value	INA_SAT_THR_L voltage
0	0.5 V
1	0.45 V
2	0.4 V
3	0.35 V

When the INA output is within the programmed thresholds, all the comparator outputs are ‘0’. When the INA output exceeds the thresholds, at least one of the four comparator outputs becomes ‘1’. The individual outputs of the 4 comparators can be read out from the register bits ECG_INA_OUTP_COMP_H, ECG_INA_OUTP_COMP_L, ECG_INA_OUTM_COMP_H, ECG_INA_OUTM_COMP_L.

To enable reliable saturation detection, a digital filter at the output of the saturation detection block can be configured such that the saturation status changes only when the resulting comparators change state for a duration higher than a programmed time $t_{SAT_DET_WIDTH}$ set using a 7-bit register ECG_SAT_DET_WIDTH as:

$$t_{ECG_SAT_DET_WIDTH} = t_{CLK_PRF} \times 128 \times (4 + ECG_SAT_DET_WIDTH)$$

where t_{CLK_PRF} is the period of the clock for the PRF counter.

The range of programmability of $t_{ECG_SAT_DET_WIDTH}$ is 4 ms to 131 ms and the default value is 50 ms.

Digital Saturation Detection:

Instead of Analog Saturation detection, a Digital Saturation detection mode can be chosen by:

- Disabling the Analog Saturation detection by setting DIS_ECG_INA_SAT_DET register bit to '1'.
- Enabling the Digital Saturation detection by setting EN_ECG_DIG_SAT_DET register bit to '1'.

Digital saturation detection is done by comparing the magnitude of the ECG digital output from the ADC with programmed threshold codes DIG_SAT_THR_H and DIG_SAT_THR_L. These codes are derived from 4-bit registers REG_DIG_SAT_THR_H and REG_DIG_SAT_THR_L.

$$DIG_SAT_THR_H = 2^{17} \times (REG_DIG_SAT_THR_H + 1)$$

$$DIG_SAT_THR_L = 2^{17} \times REG_DIG_SAT_THR_L.$$

When Digital saturation detection is enabled, the internal ECG saturation flag (ECG_SAT) goes to '1' when the magnitude of the ECG output word exceeds the threshold DIG_SAT_THR_H and returns back to '0' when the ECG output becomes lower than DIG_SAT_THR_L, thereby providing a hysteresis mechanism for the saturation detection as shown in [Figure 7-63](#). The digital filtering mechanism described in Analog Saturation detection is also applicable to the Digital Saturation detection mode.

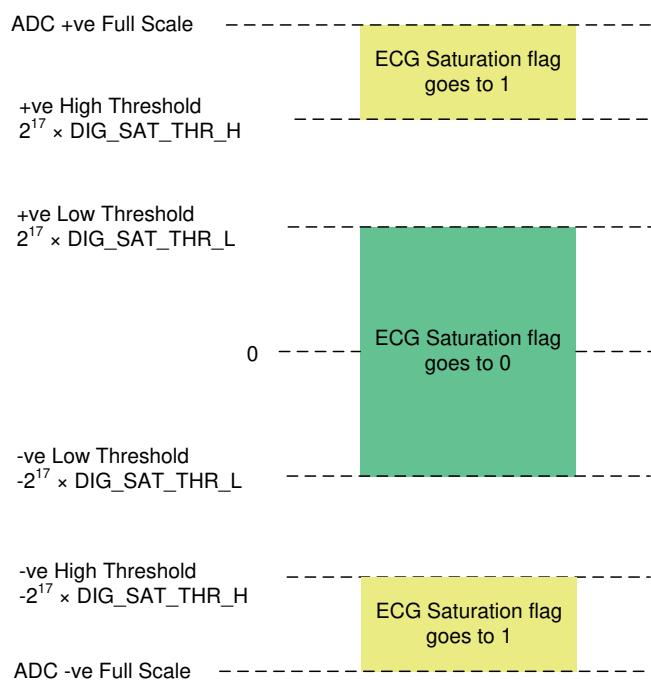


Figure 7-63. ECG Saturation Flags in Digital Saturation Detection

7.3.3.5.2 HPF Reset

On detection of saturation, a HPF reset pulse can be generated. During HPF reset, the HPF is configured to operate with a reduced time constant of approximately $T_{HPF}/20$. This reduced time constant is referred to as the recovery time constant (T_{HPF_REC}) and has a value of approximately 20 ms for a case where $C_{HPF} = 10 \mu F$. This is achieved by reducing R_{HPF} . After the HPF reset pulse has gone low, R_{HPF} (and thereby T_{HPF}) reverts back to the normal operating value. The different mechanisms of generating the HPF reset pulse are listed below:

1. Automatic Recovery with Fixed HPF reset pulse width
2. Automatic Recovery with Dynamic HPF reset pulse width
3. Manual HPF reset
4. HPF reset based on the AFE switching modes

Automatic Recovery with Fixed HPF reset pulse width:

As soon as Analog (or Digital) saturation is detected for a Saturation duration width greater than the programmed threshold value ($t_{ECG_SAT_DET_WIDTH}$), a HPF reset pulse becomes active and stays active for a fixed width equal to $t_{HPF_RST_PW}$. The timing of saturation detection and HPF reset pulse generation is shown in [Figure 7-64](#)

The width of the HPF reset pulse is programmed using a 10-bit register control HPF_RST_PW as:

$$t_{HPF_RST_PW} = t_{CLK_PRF} \times 128 \times (1+HPF_RST_PW) \text{ where } t_{CLK_PRF} \text{ refers to the period of the clock for the PRF counter.}$$

The range of programmability of $t_{HPF_RST_PW}$ is 1 ms to 1024 ms and the default value is 100 ms.

A HPF reset pulse width corresponding to about 5 recovery time constants (approximately 100 ms for a case where $C_{HPF} = 10 \mu F$) is recommended for the HPF to settle after a saturation event.

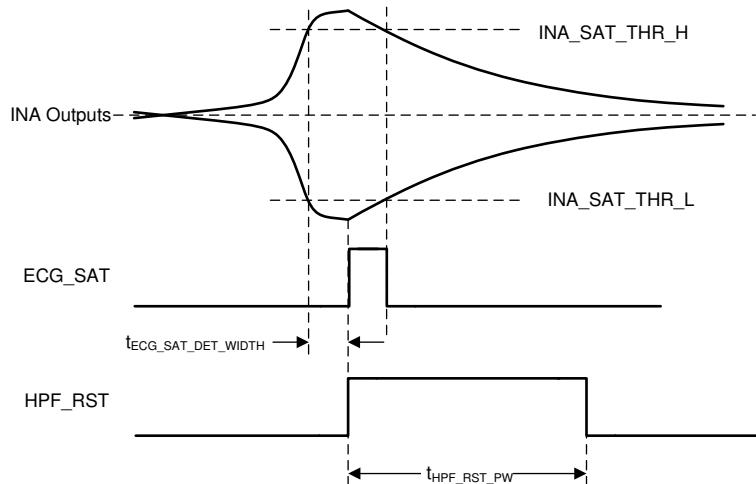


Figure 7-64. Timing Diagram of Automatic Recovery with Analog Saturation Detection and Fixed HPF Reset Pulse Width

Automatic Recovery with Dynamic HPF reset pulse width:

To switch from Fixed HPF reset pulse width mode to Dynamic HPF reset pulse width mode, set $EN_DYN_HPF_RST_PW$ to '1'. In this mode, as soon as Analog (or Digital) saturation is detected for a Saturation duration width larger than the programmed threshold value ($t_{ECG_SAT_DET_WIDTH}$), a HPF reset pulse becomes active. The HPF reset pulse stays active for the entire remaining duration of saturation and remains active for an additional time equal to $t_{HPF_RST_PW}$ after saturation ceases.

The timing of saturation detection and HPF reset pulse generation is shown in [Figure 7-65](#) for a case where Digital saturation detection is used. The hysteresis controls in the Digital saturation detection scheme can be utilized to stretch the HPF reset pulse such that the HPF reset stays high until saturation has ceased. While

using the Dynamic HPF reset pulse width mode in conjunction with Digital Saturation Detection, set $t_{\text{HPF_RST_PW}} = 10 \text{ ms}$.

If using the dynamic HPF reset with analog saturation detection mode (which does not have a hysteresis mechanism), set $t_{\text{HPF_RST_PW}}$ to about 5 recovery time constants.

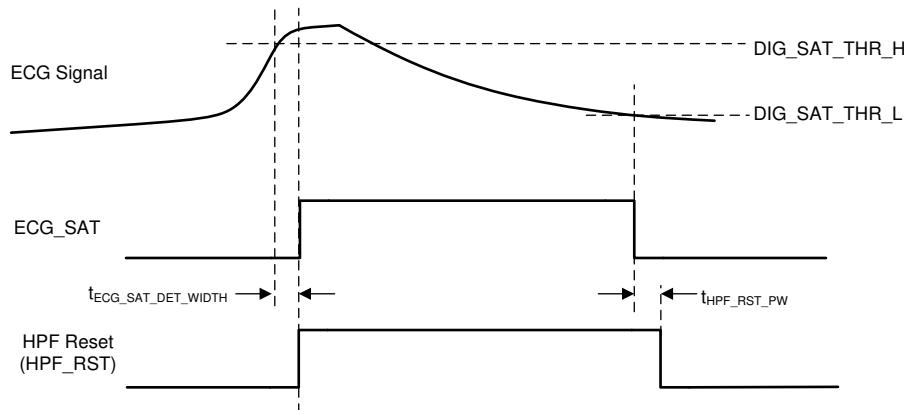


Figure 7-65. Timing Diagram of Automatic Recovery with Digital Saturation Detection and Dynamic HPF Reset Pulse Width

Manual HPF Reset:

The AFE also has an option to disable the automatic HPF reset (either Fixed or Dynamic HPF reset pulse width modes) by setting **DIS_AUTO_HPF_RST** to '1' and to control the HPF reset window using the register bit **FORCE_HPF_RST**. In this scheme, the Host detects saturation from analyzing the ECG data. The Host can then force the HPF reset by setting **FORCE_HPF_RST** register bit to '1'. The Host then sets the **FORCE_HPF_RST** bit to '0' once the ECG signal chain has come out of saturation.

HPF reset based on the AFE switching modes:

When the AFE switches from PPG mode to ECG or Mixed acquisition mode, the HPF reset filter with a fixed pulse width determined by **HPF_RST_PW** (value equal to $t_{\text{HPF_RST_PW}}$) is generated. By default, such a reset operation is enabled. Set **DIS_HPF_RST_ON_MODE_SWITCH** to '1' to disable automatic HPF reset generation on mode switching.

Automatic HPF Reset for AC coupled system:

In systems with AC coupling, the external capacitor in series with the ECG inputs can be reset automatically using the HPF reset signal. To enable the automatic reset set **EN_AUTO_HPF_RST_AC_COUPLING** = 1, **SHORT_ECG_INP_RLD** = 1 and **SHORT_ECG_INM_RLD** = 1 along with the settings required for the dynamic reset described above.

7.3.3.6 Bias resistor network for ECG pins

The AFE has resistors (value controlled by parameter R_{BIAS}) which can be used to connect the ECG input and RLD pins to reference voltages in a variety of ways. The value of R_{BIAS} can be programmed from 200 MΩ (default) down to 6.25 MΩ using the register control SEL_ECG_BIAS_RES_PPG (in PPG acquisition mode) and SEL_ECG_BIAS_RES_NOTPPG (in ECG/ Mixed acquisition modes) as shown in [Table 7-60](#)

Table 7-60. R_{BIAS} values as selected by SEL_ECG_BIAS_RES* bits

SEL_ECG_BIAS_RES_PPG/ SEL_ECG_BIAS_RES_NOTPPG	R _{BIAS} Resistor value
0	200 MΩ
1	100 MΩ
2	50 MΩ
3	25 MΩ
4	12.5 MΩ
5	6.25 MΩ

The connection of the resistors to the ECG input pins and to RLD pin can be controlled by the register controls CFG_RES_ECG_INM_PPG, CFG_RES_ECG_INP_PPG in PPG acquisition mode and register controls CFG_RES_ECG_INM_NOTPPG, CFG_RES_ECG_INP_NOTPPG in ECG/ Mixed acquisition mode. The register controls for CFG_RES_ECG_INM* and CFG_RES_ECG_INP* are shown in [Table 7-61](#) and [Table 7-62](#) respectively.

Table 7-61. Register control CFG_RES_ECG_INM*

CFG_RES_ECG_INM_PPG CFG_RES_ECG_INM_NOTPPG	Resistor connection
0	No connection
1	Connect INM to RX_SUP through resistor R _{BIAS}
2	Connect INM to ground (0 V) through resistor R _{BIAS}
3	Connect INM to RLD through resistor R _{BIAS}
4	Connect INM to ALDO_1V8 through resistor R _{BIAS}
5	Impedance measurement mode – Refer Table 7-63
6	Low power lead detect mode - Refer Table 7-65
7	Do not use

Table 7-62. Register control CFG_RES_ECG_INP*

CFG_RES_ECG_INP_PPG CFG_RES_ECG_INP_NOTPPG	Resistor connection
0	No connection
1	Connect INP to RX_SUP through resistor R _{BIAS}
2	Connect INP to ground (0V) through resistor R _{BIAS}
3	Connect INP to RLD through resistor R _{BIAS}
4	Connect INP to ALDO_1V8 through resistor R _{BIAS}
5	Impedance measurement mode – Refer Table 7-63
6	Low power lead detect mode - Refer Table 7-65
7	Do not use

For a 3 electrode measurement using DC coupled electrodes, the RLD amplifier sets the bias on the ECG input pins through a feedback mechanism as shown in [Figure 7-66](#). The RLD amplifier senses the common mode voltage at the ECG input pins and drives the body through the 3rd electrode so the ECG input common mode voltage is close to the programmed value of VCM.

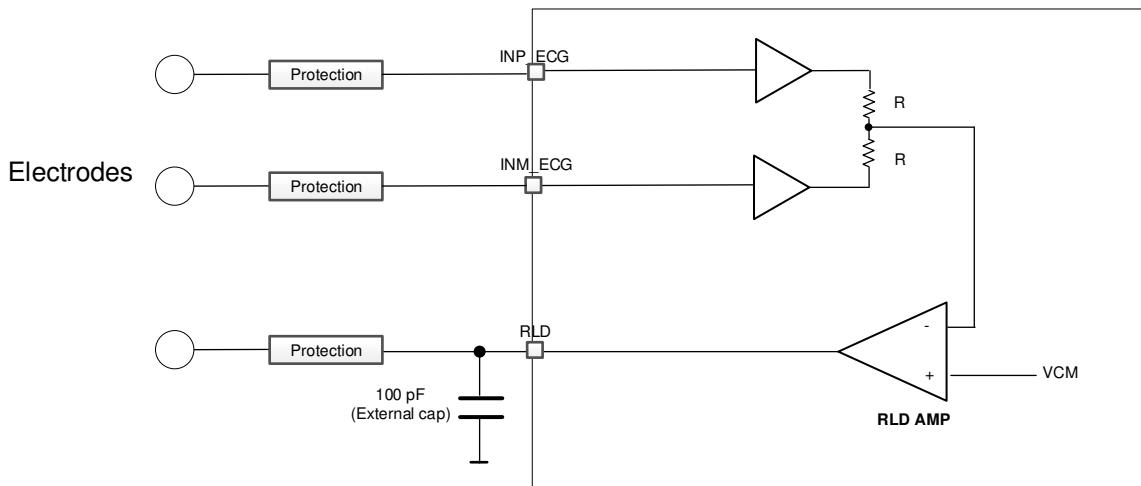


Figure 7-66. ECG input biasing using RLD feedback loop

Configurations where the RLD feedback loop cannot be used to set the ECG input bias include:

- Electrodes are AC coupled to the ECG input pins
- No 3rd electrode that can be driven by the RLD feedback loop

In these cases, the ECG input bias can be set by introducing bias resistors between each ECG input pin and RLD output. Using the internal bias resistor network, bias resistors as high as $200\text{ M}\Omega$ can be added (refer [Table 7-60](#), [Table 7-61](#) and [Table 7-62](#)). Additionally, configure the RLD amplifier as a Unity gain buffer using `CONFIG_RLD_AS_UGB`. The internal input biasing configuration is shown in [Figure 7-67](#).

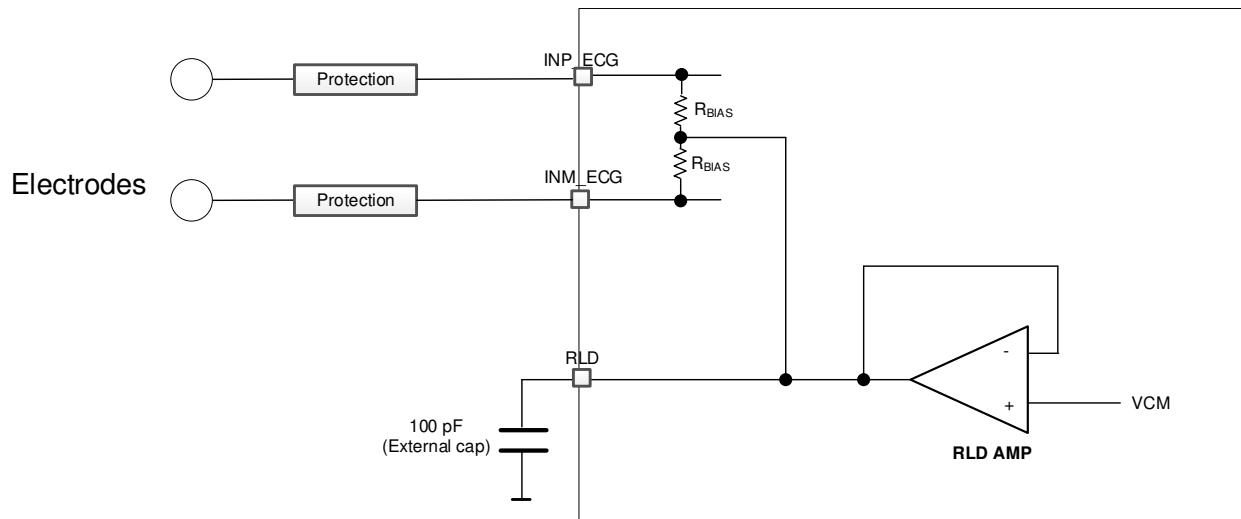


Figure 7-67. ECG input biasing using internal bias resistor network

7.3.3.7 Impedance Measurement Using the ECG Signal Chain

When operating in the PPG acquisition mode, the ECG signal chain can be used to measure the total impedance between a pair of input pins. This total impedance includes the contact impedances on either electrode and the actual skin/body impedance between the two electrodes. An example application can be to measure the Galvanic Skin Response (GSR) using the electrodes ECG_INM and RLD or ECG_INP and RLD. The power cycling scheme of the PPG acquisition mode can be used effectively to do a low-power continuous impedance measurement at low PRF rate.

To enable such a measurement, configure the device as follows:

1. Based on whether the impedance needs to be measured between ECG_INM & RLD or ECG_INP & RLD, configure the input resistor network and the input pins as shown in [Table 7-63](#).
2. Set register bit EN_ECG_SIG_CHAIN to '1' to enable the ECG signal chain.
3. Set the gain of the INA in the ECG signal chain to a value of 11 (ECG_INA_GAIN='001')
4. Set bits DIS_CHOP_INA, DIS_LPF_ECG, DIS_CHOP_LPF_ECG and BYP_LPF_INA to '1' to configure the ECG signal chain appropriately for measuring the GSR.
5. Choose a PPG phase where the measured impedance is required to be output on, and set the per-phase bit CONFIG_PHASE_AS_IMP to '1'. The REG_NUMAV for that phase determines the number of measurements that are taken and averaged to generate one sample in that PRF cycle.
6. Set appropriate power cycling controls as: REG_ACTIVE_CONTROLS = 026C80h

Table 7-63. Register control for configuring the input pins in the Impedance measurement mode

Mode	Register controls for Connection of ECG pins to the INA input	Register controls for input bias resistor			Input resistor configuration
		CFG_RES_ECG_INM_PPG	CFG_RES_ECG_INP_PPG	SWAP_CFG_RE_S	
Impedance measurement between ECG_INM and RLD	CONNECT_ECG_INM=1 SHORT_ECG_INP_RLD=1	5	5	0	Switches INM and RLD between ALDO, ground through RBIAS; Connects INP to 0 V through RBIAS
Impedance measurement between ECG_INP and RLD	CONNECT_ECG_INP=1 SHORT_ECG_INM_RLD=1	5	5	1	Switches INP and RLD between ALDO, ground through RBIAS; Connects INM to 0 V through RBIAS
Impedance measurement between ECG_INP and ECG_INM	CONNECT_ECG_INP=1, CONNECT_ECG_INM=1, SHORT_ECG_INP_RLD=1	5	0	0	Switches INM and INP between ALDO, ground through RBIAS

The Impedance is measured using the ECG signal chain as illustrated in [Figure 7-68](#).

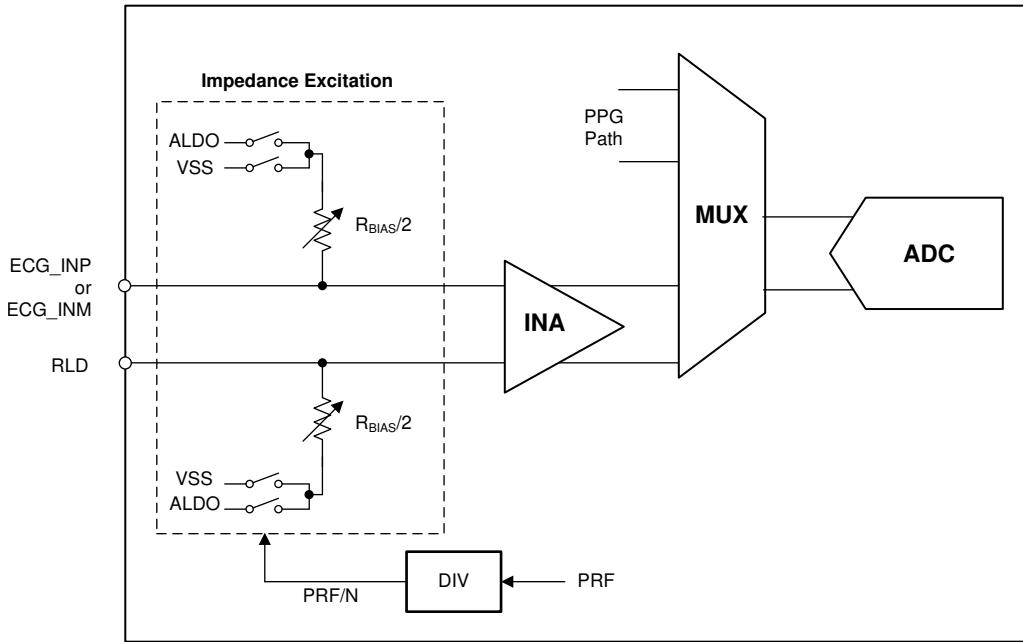


Figure 7-68. ECG Signal chain Configured for Measuring Impedance

The input bias resistors (3.125 MΩ to 100 MΩ) as chosen by the SEL_ECG_BIAS_RES_PPG register, switch a pair of ECG pins between ALDO (output of the 1.8 V LDO when LDO is enabled, or RX_SUP when LDO is bypassed) and 0 V. The pair of pins are set to be either ECG_INM & RLD or ECG_INP & RLD based on the SWAP_CFG_RES register bit.

The default rate of switching is PRF/2 and can be programmed as shown in [Table 7-64](#) using the REG_FSWITCH_IMP.

Table 7-64. Register Control for Rate of Switching the Excitation for Impedance Measurement

REG_FSWITCH_IMP	Rate of Switching the Input Resistors
0	PRF/2
1	PRF/4
2	PRF/8
3	PRF/16

This switching results in an AC excitation getting applied on the impedance between the chosen pair of pins as shown in [Figure 7-69](#). R_{CONT1} , R_{CONT2} represent the two electrode contact impedances and R_{IMP} represents the impedance between the two electrodes (for example, the skin impedance being measured).

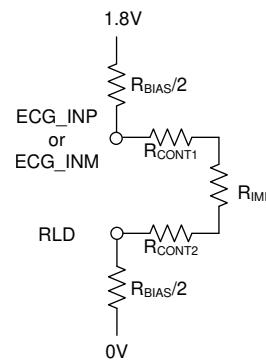


Figure 7-69. Impedance Network Created During Impedance Measurement

The differential voltage developed on the input pins is equal to:

$$V_{\text{DIFF}} = 1.8V \times R_{\text{TOTAL}} / (R_{\text{TOTAL}} + R_{\text{BIAS}}) \text{ where } R_{\text{TOTAL}} = R_{\text{CONT1}} + R_{\text{IMP}} + R_{\text{CONT2}} \quad (5)$$

Based on the range of R_{TOTAL} being measured, R_{BIAS} has to be chosen such that V_{DIFF} is limited to 90 mV (or lower) so that V_{DIFF} is compliant with the full scale input range corresponding to an INA gain of 11,

For example, when R_{BIAS} is set to 200 MΩ, the maximum value of R_{TOTAL} that can be measured is approximately 7 MΩ.

The ADC output in the designated impedance measurement phase is equal to:

$$V_{\text{OUT}} = V_{\text{DIFF}} \times G_{\text{INA}} \text{ where } G_{\text{INA}} = 11 \quad (6)$$

From [Equation 5](#) and [Equation 6](#), the value of R_{TOTAL} can be estimated from the ADC output.

The FIFO data across 2 PRF cycles is shown in [Figure 7-70](#) for a case where Phase 2 is set as an Impedance measurement phase (CONFIG_PHASE_AS_IMP=1) and REG_FSWITCH_IMP is set to 0 (switching at PRF/2). Note the alternating polarity of the impedance values because of the resistors switching at the input between 0 and 1.8V. The two alternating samples can be subtracted to get an estimate of the impedance magnitude.

P1	+IMP	P2	P3	P1	-IMP	P2	P3	P1	+IMP	P2	P3	P1	-IMP	P2	P3
----	------	----	----	----	------	----	----	----	------	----	----	----	------	----	----

Figure 7-70. FIFO Data for a Case where Resistors are Switched at PRF/2 (P1, P2, P3 are PPG phases)

7.3.4 Lead Detection

A typical ECG measurement on a wearable device involves 3 electrodes – two input electrodes which contain the differential ECG signal, and a third RLD electrode which is used by the AFE to drive the body to a potential. A proper ECG signal requires all three electrodes to make proper contact with the body. Lead detection works on the principle that when the input electrodes make contact to the body, a low impedance path is created between them through the impedance of the body. However, when one or both of the electrodes are disconnected from the body, the impedance between the electrodes is very large. There are three Lead detection mechanisms:

1. Low power DC lead detect using Bias Resistors
2. Active DC lead detect using DC current sources
3. AC lead detect using AC current sources

While enabling any type of lead detection, set bit LEAD_DET_MODULE_CLK_EN to '1' to enable clocking functions associated with the lead detection. [Figure 7-71](#) illustrates the block diagram for the three schemes.

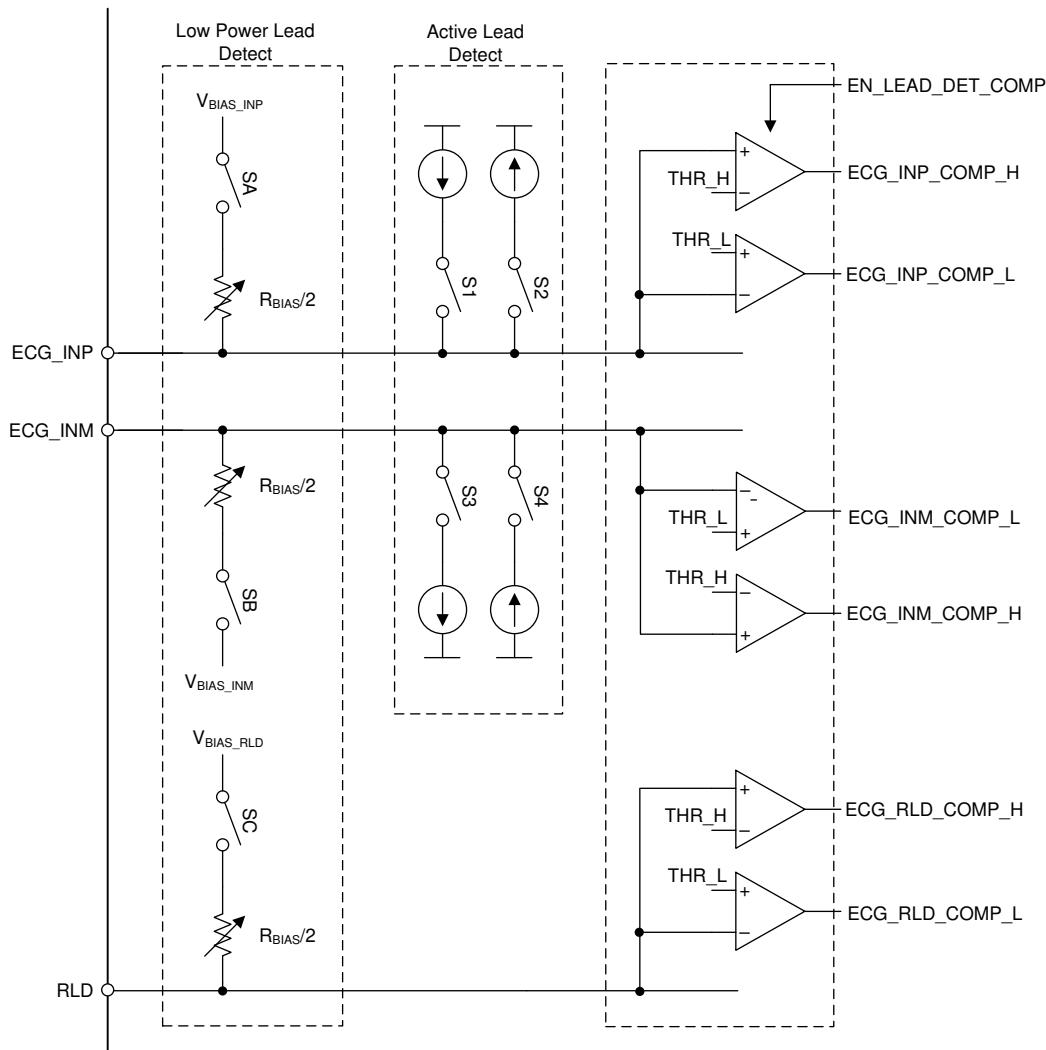


Figure 7-71. Lead detection schemes

The Low power lead detect mode consumes very less power and is meant to be used while waiting for the body to make a contact to the leads. The Active DC Lead detect mode and AC lead detect mode are meant to be used while actively acquiring the ECG signal to monitor if the leads have gotten disconnected. In that sense, the Low Power DC lead detect mode is a 'Leads on' detect mode whereas the other two modes are 'Leads off' detect modes.

7.3.4.1 Low Power DC Lead Detect

The Low power DC lead detect mode is shown in [Figure 7-72](#). Low power DC lead detect mode is meant to be used when the AFE is awaiting the detection of leads contacting to the body and the AFE needs to do lead detection at a very small incremental power. The Low power DC lead detect mode can be used for leads-on detection while operating in the PPG acquisition mode or when the AFE is idle (not acquiring any signal). However, this mode is not be a good choice for use during ECG signal acquisition as this mode continuously loads the ECG inputs with resistors. The Low Power DC lead detect block detects when the body makes contact to any two out of three electrodes (ECG_INM & RLD, ECG_INP & ECG_INM) or to all the three electrodes, and operates with very low power consumption. The Low Power DC lead detect can be kept active independent of the other AFE blocks as long as the supplies and the PRF counter clock are active. Also set bit LEAD_DET_MODULE_CLK_EN to '1'.

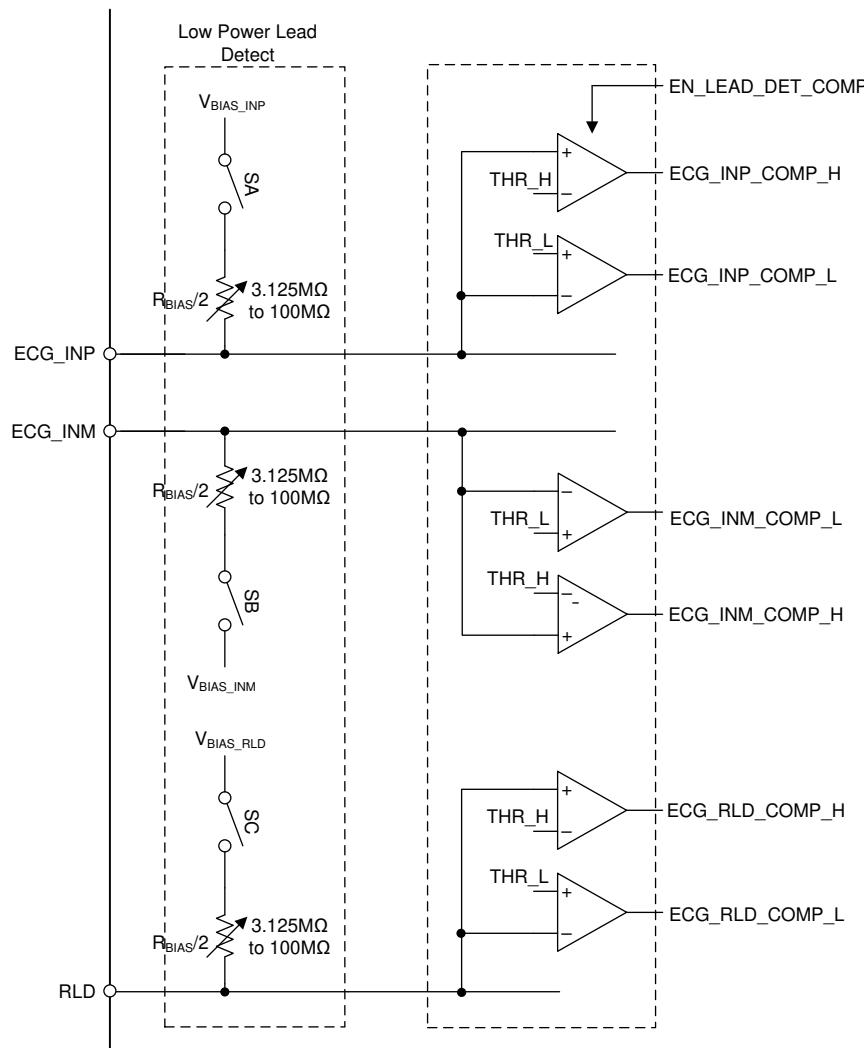


Figure 7-72. Low Power DC Lead Detect Mode

The Low power DC lead detect mode uses bias resistors to connect the ECG input pins and RLD pin to either 0 V or to rail. By programming the CFG_RES_ECG_INM* and CFG_RES_ECG_INP* registers, the pins can be connected to 0 V and 1.8 V as shown in [Figure 7-72](#).

Table 7-65. Register Control for Low Power DC Lead Detect Mode

Special Mode	CFG_RES_ECG_INM_PPG	CFG_RES_ECG_INP_PPG	Resistor connection	
			SWAP_CFG_RES = 0	SWAP_CFG_RES = 1
Low power DC lead detect	6	6	Connect INM to RX_SUP through $R_{BIAS}/2$; Connect INP and RLD to 0 V through $R_{BIAS}/2$	Connect INP to RX_SUP through $R_{BIAS}/2$; Connect INM and RLD to 0 V through $R_{BIAS}/2$

For a configuration where the ECG_INM and RLD are contacted by the same hand and ECG_INP is contacted by the other hand, set the SWAP_CFG_RES bit to 0 to connect the ECG_INP and RLD pins to 0 V and the ECG_INM pin to 1.8 V (set SWAP_CFG_RES to 1 if ECG_INP and RLD are contacted by the same hand and ECG_INM is contacted by the other hand). With the electrodes not making contact to the body, the pin voltages are set by the bias resistor connections. When all 3 electrodes make contact to the body, the voltages on all 3 pins come well within the operating range – a condition that can be discerned from the output of the comparators

Six comparators check for the input pin voltages against high and low threshold voltages (THR_H and THR_L). The threshold voltages can be programmed using the register controls LEAD_DET_THR_H_PPG, LEAD_DET_THR_L_PPG (in PPG acquisition mode) and LEAD_DET_THR_H_NOTPPG, LEAD_DET_THR_L_NOTPPG (in ECG/ Mixed acquisition modes). The comparators are disabled by default and can be enabled by setting the EN_LEAD_DET_COMP_PPG in PPG acquisition mode and by setting EN_LEAD_DET_COMP_NOTPPG in ECG/Mixed acquisition modes.

The thresholds are related to the register settings as follows (N corresponds to the value of the corresponding register setting):

$$\text{THR_L} = [\text{RX_SUP} * (250 + 50.N) / 3600] \text{ for } N \leq 7$$

$$\text{THR_L} = [\text{RX_SUP} * (100.N - 100) / 3600] \text{ for } N \geq 8$$

$$\text{THR_H} = [\text{RX_SUP} - \text{RX_SUP} * (250 + 50.N) / 3600] \text{ for } N \leq 7$$

$$\text{THR_H} = [\text{RX_SUP} - \text{RX_SUP} * (100.N - 100) / 3600] \text{ for } N \geq 8$$

Maximum value of threshold voltage supported is 2.3V. Do not use a register setting which results in a threshold voltage greater than 2.3V. [Table 7-66](#) and [Table 7-67](#) lists the values of THR_L and THR_H for a case where RX_SUP = 1.8 V.

Table 7-66. Values of THR_L for a Case Where RX_SUP = 1.8 V

LEAD_DET_THR_L_PPG/ LEAD_DET_THR_L_NOTPPG	THR_L (Comparator Low Threshold voltage)
0	0.13
1	0.15
2	0.17
3	0.20
4	0.23
5	0.25
6	0.28
7	0.30
8	0.35
9	0.40
10	0.45
11	0.50
12	0.55
13	0.60
14	0.65
15	0.70

Table 7-67. Values of THR_H for a case where RX_SUP = 1.8 V

LEAD_DET_THR_H_PPG/ LEAD_DET_THR_H_NOTPPG	THR_H (Comparator High Threshold voltage)
0	1.67
1	1.65
2	1.63
3	1.60
4	1.58
5	1.55
6	1.52
7	1.50
8	1.45
9	1.40
10	1.35
11	1.30
12	1.25
13	1.20
14	1.15
15	1.10

The output of the 6 comparators are consolidated into three Lead status flags (which are available for read out through register bits) that indicate whether each of the leads are connected or not. These 3 flags are referred to as ECG_RLD_LEAD_STATUS, ECG_INM_LEAD_STATUS and ECG_INP_LEAD_STATUS, and go high when the output of both the comparators on the pin become 0. [Table 7-68](#) indicates the expected values of the Lead status flags for different lead on/off conditions. This table corresponds to a case where ECG_INM and RLD make contact to the wrist of the same hand and ECG_INP makes contact to the finger of the other hand, and SWAP_CFG_RES bit is set to 0.

Table 7-68. Expected Values for the Lead Status Flags

ECG_INP_LEAD_STAT_US	ECG_INM_LEAD_STATUS	ECG_RLD_LEAD_STATUS	Lead status
0	0	0	All Leads-off
0	1	1	Watch-on-wrist detected
1	1	0	ECG_INP, ECG_INM connected to body, RLD not connected. ECG can be acquired using 2-electrodes ECG_INP, ECG_INM. Resistors of value RBIAS (eg. 200MΩ) can be introduced between ECG_INP & RLD and ECG_INM & RLD and the RLD amp can be configured to drive a fixed bias voltage.
1 ⁽¹⁾	0 ⁽¹⁾	1 ⁽¹⁾	This case corresponds to ECG_INP, RLD connected to the body but ECG_INM is not connected and is treated as leads-off. However this condition cannot be determined by the Low power Lead detect circuit if SWAP_CFG_RES = 0.
1	1	1	ECG_INP, ECG_INM and RLD are all connected to the body. ECG can be acquired using 3-electrode configuration.

(1) This condition can be detected only if SWAP_CFG_RES bit is set to '1'.

By reading the 3 Lead status flags, the Host can determine which all leads are connected to the body and can initiate an acquisition mode change. Additionally, based on a change in Lead status flags, an interrupt DC LEAD DET can be generated.

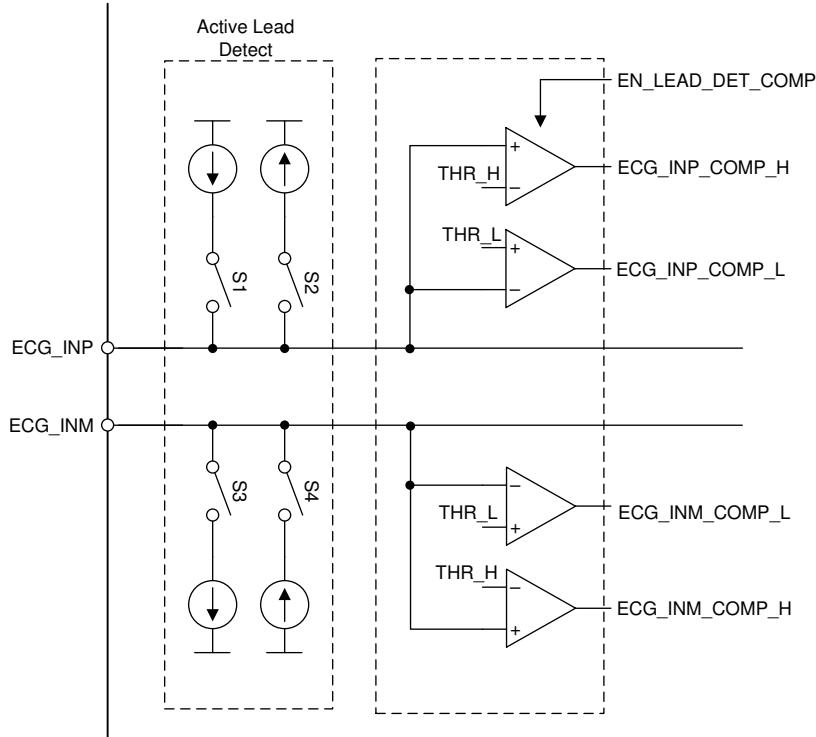
To enable reliable lead status change detection, a digital filter at the output of the lead detect block can be configured such that the DC LEAD DET gets generated only when the resulting comparators change state for a duration higher than a programmed time $t_{LEAD_DET_WIDTH}$ which is set using a register control LEAD_DET_WIDTH as:

$t_{LEAD_DET_WIDTH} = t_{CLK_PRF} \times 128 \times LEAD_DET_WIDTH$ where t_{CLK_PRF} is the period of the clock for the PRF counter. When operating in the PPG acquisition mode, an additional parameter SCALE LEAD DET WIDTH_PPG can be used to scale the $t_{LEAD_DET_WIDTH}$ as:

$$t_{LEAD_DET_WIDTH} = t_{CLK_PRF} \times 128 \times LEAD_DET_WIDTH / 2^{SCALE_LEAD_DET_WIDTH_PPG}$$

7.3.4.2 Active DC Lead Detect

The Active DC Lead Detect mode can be used during ECG signal acquisition as the Active DC Lead Detect mode presents very high impedance and does not significantly reduce the input impedance of the INA. Each of ECG_INP and ECG_INM pins have a source and sink current sources as shown in Figure 7-73, which can be enabled using EN LEAD DET CURR PPG (when in the PPG acquisition mode) and using EN LEAD DET CURR NOTPPG (when in the ECG acquisition mode or Mixed acquisition mode). Also set bit LEAD DET MODULE CLK EN to '1'.

**Figure 7-73. Active DC Lead Detect Mode**

The connection of the 4 current sources to the pins can be set using the SEL_ECG_INM_CURR_POL and SEL_ECG_INP_CURR_POL as shown in [Table 7-69](#) and [Table 7-70](#)

Table 7-69. Choosing source/sink Lead detect current sources for INM

SEL_ECG_INM_CURR_POL	Active Current source
0	No active current source
1	Sink current on INM is active
2	Source current on INM is active
3	Both sink and source currents on INM are active (Net current is approximately 0)

Table 7-70. Choosing source/ sink Lead detect current sources for INP

SEL_ECG_INP_CURR_POL	Active Current source
0	No active current source
1	Sink current on INP is active
2	Source current on INP is active
3	Both sink and source currents on INP are active (Net current is approximately 0)

For example, by programming SEL_ECG_INP_CURR_POL to 2, and SEL_ECG_INM_CURR_POL to 1, the current sources can be configured to source current into the ECG_INP pin and to sink current from the ECG_INM pin, thereby realizing a differential current source between ECG_INP and ECG_INM.

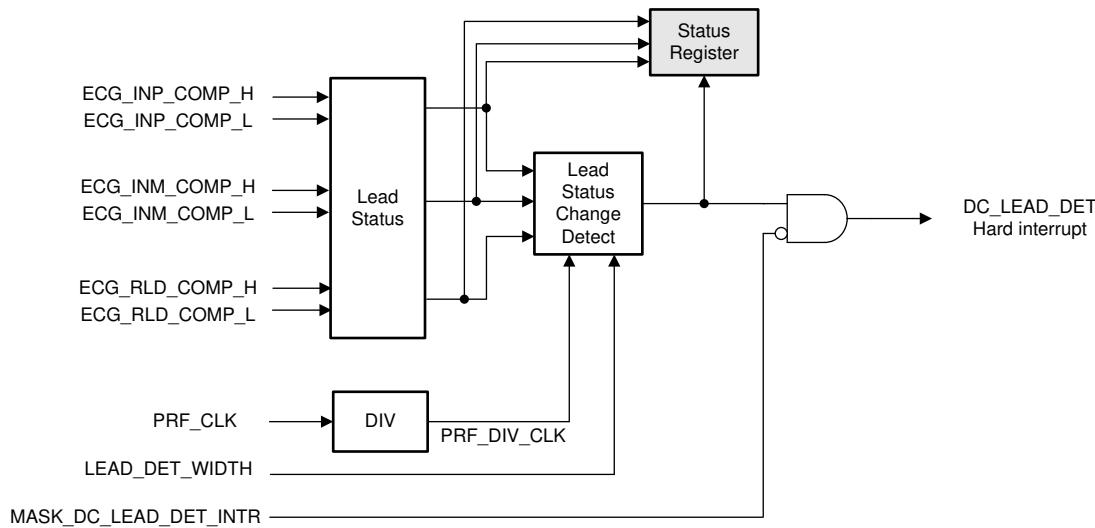
To support a wide range of electrode contact impedance, the value of the currents (common for all the 4 sources) can be programmed using register control ILEAD_AMP as shown in [Table 7-71](#). Additionally, program the ILEAD_BIAS_AMP register as indicated so that the bias current to the lead detect block is also appropriately programmed

Table 7-71. Programming the Amplitude of the Lead Detect Current Sources

I _{LEAD_AMP}	Amplitude of Lead detect current source	Decimal value to be programmed in I _{LEAD_BIAS_AMP} register
1	2.9 nA	0
2	5.8 nA	0
3	11.6 nA	3
4	23.2 nA	5
5	46.3 nA	9
6	92.5 nA	25

The enabling of the lead detect comparators and their threshold programming are same as in the Low power detect mode. Also set bit LEAD_DET_MODULE_CLK_EN to '1'. While using the Active DC Lead detect mode, make sure that the bias resistors are all disconnected from the input pins and the RLD pin.

Figure 7-74 shows the scheme of the low power and DC lead detection and generation of the interrupt DC_LEAD_DET while operating in this mode

**Figure 7-74. Low Power and DC Lead Detect Mode**

7.3.4.3 AC Lead Detection

By setting the EN_AC_LEAD_DET bit to '1', an AC lead detection feature can be enabled. With the AC lead detection enabled and with the SEL_ECG_INM_CURR_POL and SEL_ECG_INP_CURR_POL bits both set to 0, the source/sink lead detect current sources at the ECG_INP and ECG_INM pins get configured to switch at 4 kHz frequency to generate an AC lead signal that goes from $+I_{LEAD}$ to $-I_{LEAD}$. The strength of the AC lead signal can be extracted from the ECG output data stream through digital demodulation followed by a 16-sample averaging which generates the AC lead signal used for comparison with thresholds. The AC lead signal after averaging and decimation-by-16 is compared with a high AC lead threshold code and a leads-off interrupt AC_LEAD_OFF is generated if the AC lead signal amplitude exceeds the high threshold. The high threshold code is derived from a 11-bit register AC_LEAD_DET_THR_H as:

$$\text{High AC lead Threshold in ADC codes} = 2^{10} \times (\text{AC_LEAD_DET_THR_H} + 1)$$

Similarly a leads-on interrupt AC_LEAD_ON can be generated if the AC lead signal amplitude is less than a programmed low AC lead threshold code and greater than a code 0x000040. 0x000040 is kept as a lower limit for lead-on detection so the INA saturation does not result in a false leads-on signal.

The low threshold code is derived from a 8-bit register AC_LEAD_DET_THR_L as:

$$\text{Low AC lead Threshold in ADC codes} = 2^{10} \times \text{AC_LEAD_DET_THR_L}$$

Figure 7-75 shows the AC lead threshold and leads-on/off ranges. In some scenarios, when the leads are off, the INA can saturate. In this scenario, the AFE does not generate a leads-off signal. The accumulator output in every PRF cycle can also be read out from a 24-bit AC_LEAD_AMPL register.

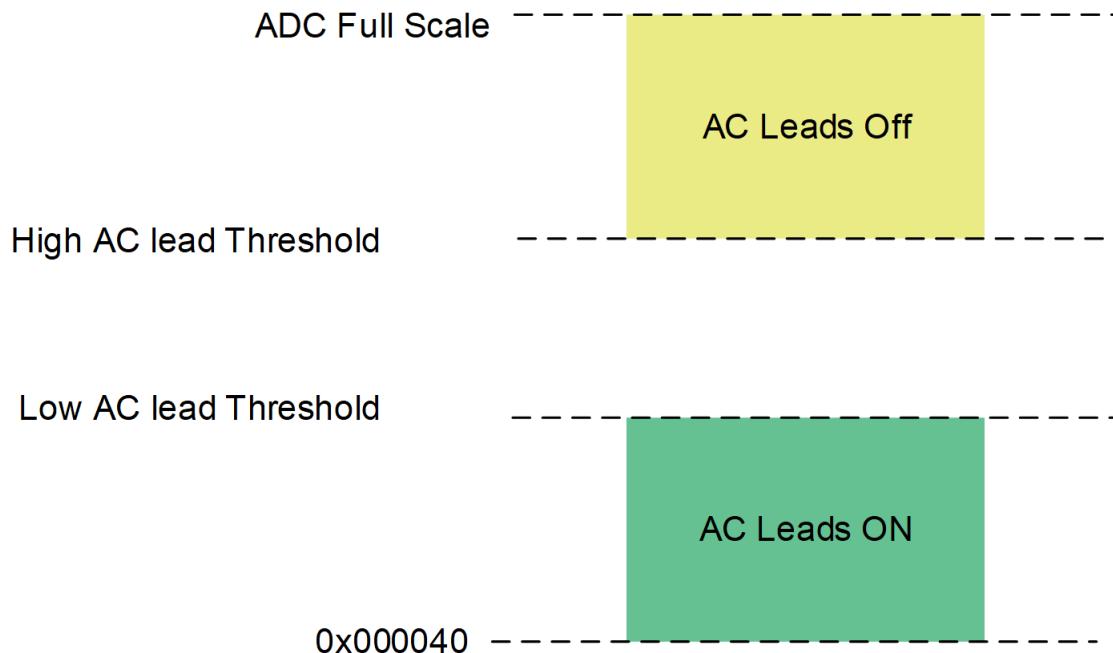


Figure 7-75. AC Lead On/Off Ranges with Respect to the AC Lead Threshold Levels

Figure 7-76 shows the scheme of AC lead detection. PRF_ECG refers to the effective ECG sampling rate (and not the ECG output data rate, which is governed by the ECG decimation factor).

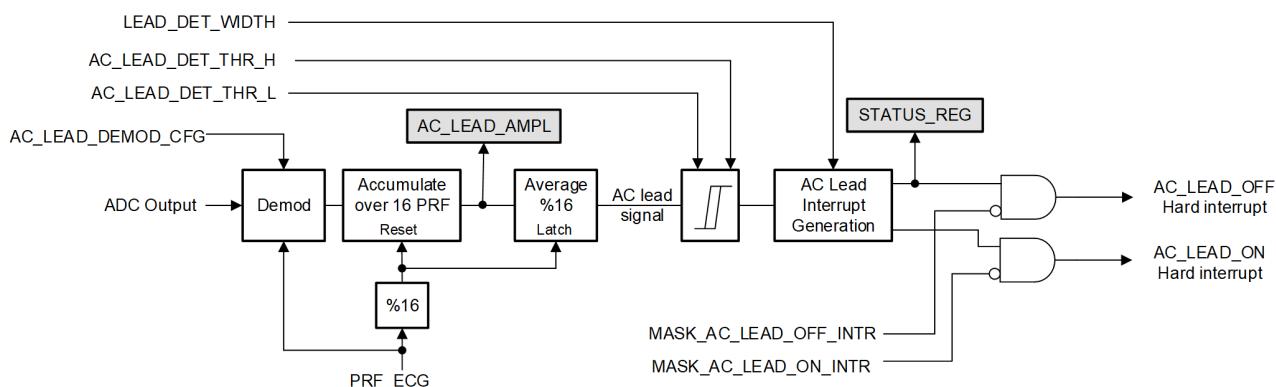


Figure 7-76. AC Lead Detection Scheme

Requirements for reliable AC lead detection:

1. The decimal value of the LEAD_DET_WIDTH register represents the time window (in ms) over which the AC lead interrupt generation updates the output. For the AC lead detection to work properly, the LEAD_DET_WIDTH must be set to a value equivalent to $10 \times t_{\text{PRF_ECG}}$ where $t_{\text{PRF_ECG}}$ refers to the time period of ECG sampling equal to $1/f_{\text{PRF_ECG}}$. For example, at a PRF_ECG of 500 Hz, set the LEAD_DET_WIDTH to a value of 20 or lower so that the AC lead interrupt generation updates the outputs at intervals of 20 ms or lower. This guideline is not affected by the ECG decimation factor setting.

2. At a transition of the leads from lead-on to lead-off or lead-off to lead-on, there can be transients in the signal. These transients can result in spurious lead on/ lead off interrupt generation. TI recommends to follow a sequence of operations as shown in [Figure 7-77](#) to determine the steady state of the leads:
- On receiving an AC_LEAD_ON or AC_LEAD_OFF interrupt, initiate a "Wait and Observe" window of 200 ms
 - During the "Wait and Observe" window, ignore any interrupts that indicate AC lead on/ lead off
 - At the end of the "Wait and Observe" window, read the 2-bit AC_LEAD_SEQ register. A value of '01' indicates that the current lead condition is "Lead on" whereas a value of '10' indicates that the current lead condition is "Lead off"

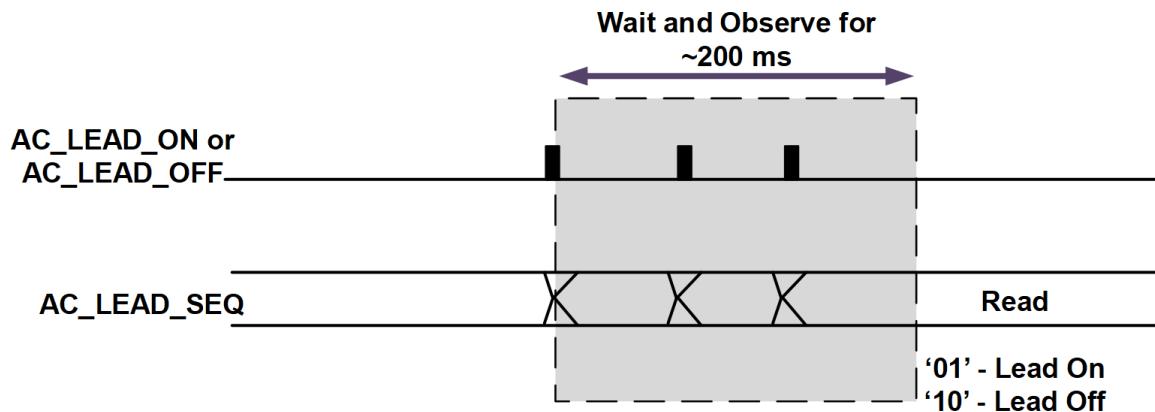


Figure 7-77. Sequence of operations to determine the lead status on receipt of an interrupt

3. The AC_LEAD_AMPL register contains the information of the AC lead signal, which is a measure of the strength of the lead connection. However, a direct readout of the AC_LEAD_AMPL register is not a true indicator of the AC lead signal. The reason is as follows. The accumulator is reset to zero after every 16 ECG samples (prior to decimation) and starts a fresh operation over the next set of 16 ECG samples. The AC lead signal, which is the value used for comparison with the high and low thresholds, corresponds to the accumulator output after 16 ECG samples (prior to decimation). However, the readout of AC_LEAD_AMPL corresponds to the instantaneous value of the accumulator output. When the number of ECG samples (number of active ESAW) in a PRF cycle is 1, then the readout of the AC_LEAD_AMPL register over 16 consecutive PRF cycles can be used to determine the AC lead signal. The largest value over the 16 PRF cycles gives an estimation of the AC lead signal as shown in [Figure 7-78](#)

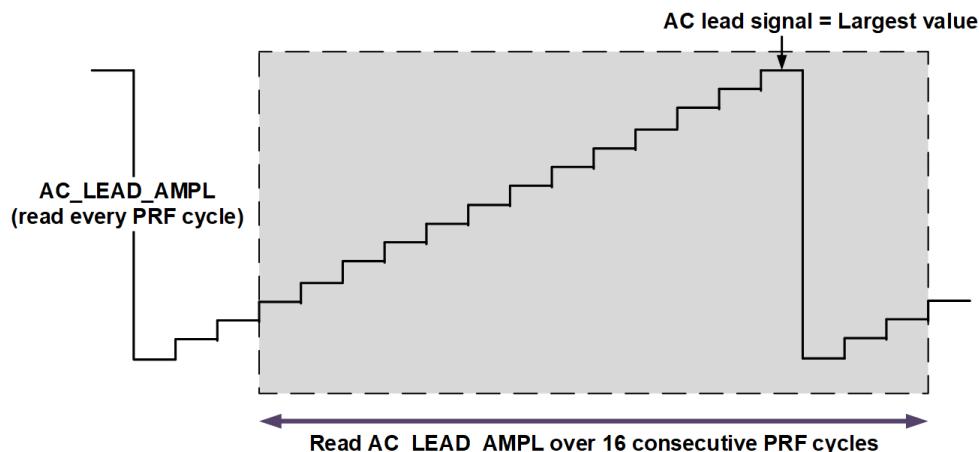


Figure 7-78. Method of Determining the AC Lead Signal from Readout of AC LEAD_AMPL (NUM_ESAW=1)

Note

The accuracy in the AC lead strength extraction can be affected by any DC drift in the ECG signal. In Rev2 Silicon, this effect can be reduced by setting the AC_LEAD_DET_CLK_PHASE bit to '1', and programming the AC_LEAD_DEMOD_CFG register to a value of 33h. In Rev1 Silicon, do not program these bits.

7.3.4.4 Comparison of Lead Detect Modes

Table 7-72 shows a comparison of the three lead detect modes.

Table 7-72. Comparison of the lead detect modes

Attribute	Lead detect mode		
	Low power	Active DC	AC
Usable in PPG acquisition mode or idle mode (when ECG acquisition is not active)	X (Recommended)	X	
Recommended for use in Mixed acquisition or ECG acquisition mode		X	X
Enabling method	Select resistor value using SEL_ECG_BIAS_RES_NOTPPG in ECG/ Mixed acquisition mode and using SEL_ECG_BIAS_RES_PPG in PPG acquisition mode Configure resistors using CFG_RES_ECG_INP_NOTPPG, CFG_RES_ECG_INM_NOTPPG in ECG/ Mixed acquisition mode and using CFG_RES_ECG_INP_PPG, CFG_RES_ECG_INM_PPG in PPG acquisition mode	Configure lead detect current sources and comparators	Configure lead detect current sources and comparators and set EN_AC_LEAD_DET to '1' ⁽²⁾
Input comparators enabled by	EN LEAD DET COMP NOTPPG in ECG/Mixed acquisition modes EN LEAD DET COMP PPG in PPG acquisition mode	N/A	
Clocking functions in lead detection enabled by	LEAD_DET_MODULE_CLK_EN		
High threshold programmed by	LEAD_DET_THR_H_NOTPPG in ECG/Mixed acquisition mode LEAD_DET_THR_H_PPG in PPG acquisition mode	AC LEAD DET THR_H	
Low threshold programmed by	LEAD_DET_THR_L_NOTPPG in ECG/Mixed acquisition mode LEAD_DET_THR_L_PPG in PPG acquisition mode	AC LEAD DET THR_L	
Lead detect current sources enabled by	N/A	EN LEAD DET Curr NOTPPG in ECG/ Mixed acquisition mode EN LEAD DET Curr PPG in PPG acquisition mode	
Polarity of lead detect current sources enabled by	N/A	SEL_ECG_INP_Curr_POL SEL_ECG_INM_Curr_POL	N/A ⁽¹⁾
Magnitude of lead detect current sources	N/A	ILEAD_AMP	
Lead status flags	ECG_RLD_LEAD_STATUS ECG_INM_LEAD_STATUS ECG_INP_LEAD_STATUS	N/A	
Interrupt corresponding to Lead-on detect	DC LEAD DET	AC LEAD ON	
Interrupt corresponding to Lead-off detect	DC LEAD DET	AC LEAD OFF	

(1) Set bits SEL_ECG_INP_CURR_POL and SEL_ECG_INM_CURR_POL to '0'.

(2) In Rev2 Silicon, if setting AC_LEAD_DET_CLK_PHASE to '1', then set AC_LEAD_DEMOD_CFG to 33h.

7.3.5 First-In, First-Out (FIFO) Block

7.3.5.1 FIFO pointers and Watermark level

The AFE has a 256-sample FIFO that can be used to store data from the phases. Each sample corresponds to a 3-byte ADC word. The FIFO read and write pointers are reset to 0 whenever a hardware or software reset is applied. When the FIFO is enabled by setting the FIFO_EN bit to 1, the write pointer starts to progress whenever a data word streams into the FIFO. The read pointers progress when a data word is read out from the FIFO.

The FIFO_RDY interrupt is an indicator to the MCU to read out the data from the FIFO and can be made to be output on one of the output pins (refer section on Interrupts). Note that the AFE can also output interrupts other than FIFO_RDY depending on the state of the interrupt selection mux. For example, by default, the ADC_RDY pin outputs a DATA_RDY interrupt once in every PRF cycle. The MCU should take care so as to not treat such interrupts as FIFO_RDY interrupts, and avoid reading data from the FIFO. This inadvertent readout of data from the FIFO based on an interrupt that is not the FIFO_RDY interrupt can result in a mismatch in the FIFO phase ordering. This situation can be avoided by configuring the interrupt mux to output the FIFO_RDY interrupt on the desired pin before the FIFO is enabled.

The FIFO_RDY gets generated when the difference between the Write and Read pointers exceeds a programmed Watermark (WM) level referred to as WM_FIFO. The REG_WM_FIFO register control sets the Watermark level (WM_FIFO) to be equal to (REG_WM_FIFO+1). With WM_FIFO thus set, the FIFO_RDY interrupt is now an indication to the MCU that a number of samples equal to WM_FIFO are ready to be read out. The position of the FIFO_RDY within the PRF cycle is fixed to come after the last defined phase and before the start of the Deep sleep window. If the MCU fails to start reading before the completion of the active window of the next PRF cycle, the FIFO_RDY interrupt repeats and keeps repeating in every subsequent PRF cycle until sufficient samples have been read out and the pointer difference has dropped below the watermark level. WM_FIFO should be chosen such that the FIFO fills to the Watermark level on completion of an integer number of PRF cycles.

The instantaneous difference between the write and read pointers can be read out through an 8-bit register REG_POINTER_DIFF. The difference between the write and read pointers (POINTER_DIFF) is equal to (REG_POINTER_DIFF+1). On receiving a FIFO_RDY, the MCU can read out this register (prior to reading out the FIFO) to confirm that POINTER_DIFF is indeed equal to WM_FIFO. [Figure 7-79](#) illustrates the case of how the FIFO_RDY interrupt gets generated in the Watermark FIFO mode for a case where WM_FIFO is set to 32. In this example, the MCU is shown as reading only 8 samples after receipt of the first FIFO_RDY. Note that, in this example, only 1 data sample is stored in the FIFO in every PRF cycle and so the write pointer advances by 1 in every PRF cycle.

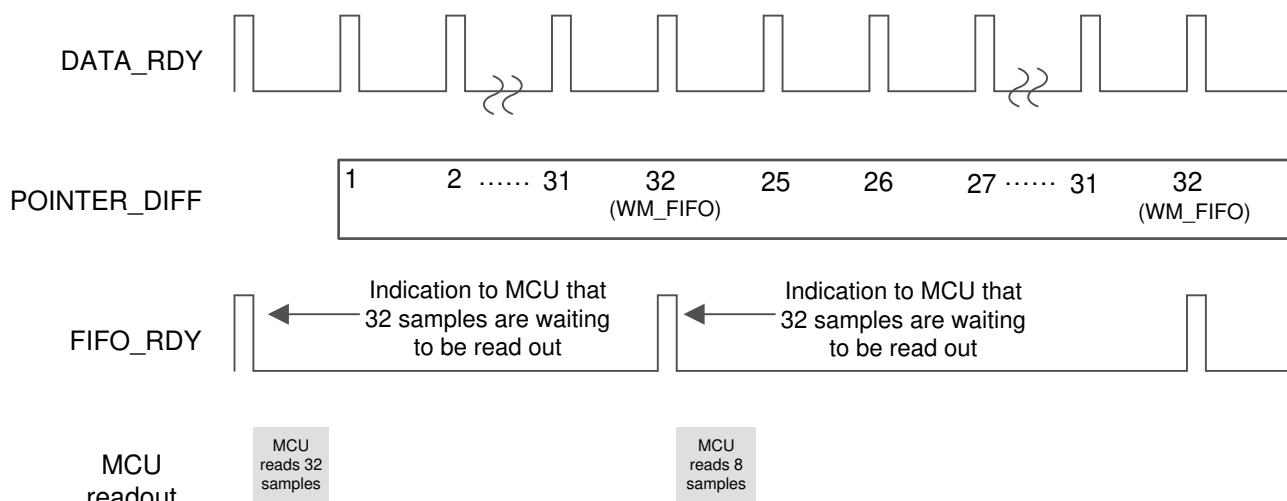


Figure 7-79. FIFO Mode Based on Programmable Watermark Level

The generation of FIFO_RDY interrupt can be masked using the MASK_FIFO_RDY register control. Such masking may be useful in cases where the MCU is not interested in reading data from the AFE for a period

of time but wants to retrieve prior data stored in the FIFO when it starts reading again. To achieve this, the Read pointer can be forced relative to Write pointer by setting the FORCE_FIFO_OFFSET to '1', and then programming FIFO_OFFSET_TO_FORCE to force the location of the Read pointer relative to current location of Write pointer.

The recommended method of achieving this is illustrated in [Figure 7-80](#). In this illustration, the AFE has been configured to output a THR_DET_RDY interrupt which could be an indication to the MCU that the signal level in a particular phase has crossed a certain threshold and the MCU needs to wake up and read the FIFO data. Since the THR_DET_RDY interrupt is also positioned at the start of the Deep sleep window, it is an indication to the MCU that the FIFO has been most recently updated with a full PRF cycle of data. The MCU should complete all the indicated register write and FIFO read before the end of the Deep sleep window before unmasking the FIFO_RDY interrupt.

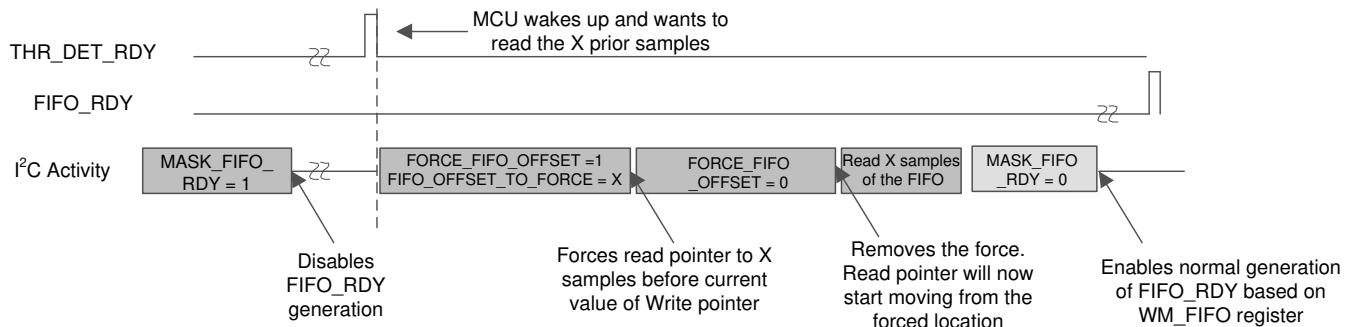


Figure 7-80. Method of Resuming FIFO Read Following a FIFO_RDY Masking Phase

When the MCU desires to continue accessing the FIFO but cannot start reading out data before the start of the next PRF cycle, repetitive interrupts may be undesirable. To prevent the occurrence of repetitive interrupts, an AUTO_MASK_FIFO_RDY bit can be set, to '1' – when set, only the first FIFO_RDY interrupt is given out. Subsequent interrupts are masked. To unmask the FIFO_RDY interrupt generation, the MCU needs to set this bit to '0' for a duration of at least 1 full PRF cycle and then to '1' after it services the interrupt by reading FIFO data.

7.3.5.2 FIFO Data Generation Controls

By default, the ADC words generated in each Phase N streams into the FIFO and gets stored in the FIFO. [Table 7-73](#) lists the different ways in which the FIFO data corresponding to Phase N can be derived from the ADC words from Phase N and the adjoining phases through the per-phase register control FIFO_DATA_CTRL.

Table 7-73. Register Control for Defining the FIFO Data Generated by a Phase

FIFO_DATA_CTRL_2	FIFO_DATA_CTRL_1	FIFO data generated in Phase N	
		Phases N-2, N-1, N configured as Single receive phases	Phases N-2, N-1, N configured as Dual receive phases
0	0	Phase N output	Phase N output of TIA1 Phase N output of TIA2 ⁽²⁾
0	1	No data written to the FIFO	No data written to the FIFO
0	2	Phase N – Phase N-1 ⁽¹⁾	(Phase N – Phase N-1) ⁽¹⁾ for TIA1 (Phase N – Phase N-1) ⁽¹⁾ for TIA2 ⁽²⁾
0	3	Phase N-1 – Average (Phase N, Phase N-2) ⁽¹⁾	[Phase N-1 – Average (Phase N, Phase N-2)] ⁽¹⁾ for TIA1 [Phase N-1 – Average (Phase N, Phase N-2)] ⁽¹⁾ for TIA2 ⁽²⁾
1	x	Phase N – Phase N-2 ^{(1) (3)}	(Phase N – Phase N-2) ⁽¹⁾ for TIA1 (Phase N – Phase N-2) ⁽¹⁾ for TIA2 ^{(2) (3)}

(1) Set only if all relevant phases # (eg. N, N-1 and N-2) exist and are not masked.

(2) The two data samples go into the FIFO one after the other (TIA1 sample followed by TIA2 sample).

(3) When decimation of Phases N and Phase N-2 is enabled, then the FIFO data is generated as Phase N – Phase N-2. When decimation of Phase N and Phase N-2 is not enabled, then the FIFO data is generated as Phase N-2 – Phase N

The first word in a PRF cycle that goes into the FIFO can be distinguished from the other words in that cycle by setting the register bit MODE_EN_FRAME_SYNC. When this mode is enabled, the MSB bit (D23) is replaced by the Frame sync indicator bit, which is set to '1' for the first FIFO word in a PRF cycle, and set to '0' for other words in that cycle as shown in [Figure 7-81](#)

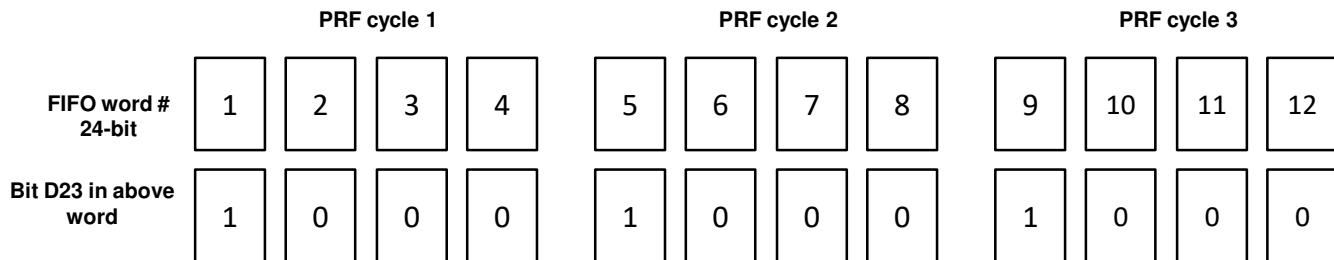


Figure 7-81. Scheme for Frame synchronization

7.3.5.3 FIFO Data Tags

To distinguish ECG and PPG data from the FIFO, a two bit LSB tag can be embedded in the FIFO data. The two bit LSB tag replaces bits D1,D0 of the ADC word. By default LSB tagging is disabled. LSB tagging in the FIFO output can be enabled by setting register bit EN_DATA_MARKER to '1'.

A MSB tag to indicate the first FIFO sample from a PRF cycle can be enabled by setting the MODE_EN_FRAME_SYNC bit to '1'. The MSB tag replaces D23 of the FIFO output word. The MSB and LSB tags are listed in [Table 7-74](#)

Table 7-74. FIFO data tagging

Enable bit	MSB Tag	LSB Tag	Description
EN_DATA_MARKER		00	Data is a PPG sample
		01	Data is an ECG sample
		11	Data is an ECG data taken during the HPF reset
MODE_EN_FRAME_SYNC	0		Not the first FIFO sample in PRF cycle
	1		First FIFO sample in PRF cycle

7.4 Device Functional Modes

7.4.1 Power Modes

The AFE has the following power modes:

1. Normal mode
2. Software power-down mode (PDNAFE). This mode is enabled by using a register bit. When operating in the LDO bypass mode, additionally set the PDN_BG_IN_DEEP_SLEEP to '1' to get to the lowest power. Also, to minimize the power consumption, before going into Software powerdown mode, set the acquisition mode to PPG mode.

7.4.2 RESET Modes

The AFE has internal registers that must be reset before valid operation. There are two ways to reset the device.

1. Hardware reset - A reset signal can be issued by pulsing the RESETZ pin low for a duration of 25 to 50 μ s.
2. Software reset: A software reset via a self-clearing SW_RESET register bit.

7.4.3 LDO Modes

The AFE has the following LDO modes:

1. **LDO Bypass mode:** Set by connecting EN_LDO_BYP to RX_SUP. While operating in the LDO Bypass mode, the register bit PD_BG_IN_DEEP_SLEEP can be set to '1' to power-down the bandgap circuitry during Deep sleep phase, and save power.
2. **LDO Enable mode:** Set by EN_LDO_BYP to 0V. The internal LDOs are enabled in this mode and provide improved PSRR for any tones on the RX_SUP rail. The PDN_BG_IN_DEEP_SLEEP bit should be set to '0' when operating in the LDO Enable mode

The logic level on the EN_LDO_BYP pin can be read out through a register bit FLAG_LDO_STATE (1=Bypass).

7.4.4 Clocking Modes

The AFE has the following Clocking modes:

1. **Internal oscillator mode:** Default mode. The internal 128 kHz oscillator is made active and the timing engine runs on this oscillator. The PRF setting by PRPCT is also based on the 128 kHz oscillator.
2. **External clock mode:** A free running clock on the CLK pin is used for the timing engine and the PRF counter. Timing counts and PRF setting are based on the external clock. Set by programming OSC_DIS_128K to '1'. Program EXT_CLK_FREQ based on the operating frequency range.
3. **Single-shot acquisition mode:** A high pulse on CLK pin triggers a fresh set of signal acquisition. The 128 kHz oscillator is kept active until start of the Deep sleep window. Timing counts are based on the 128 kHz oscillator. Periodicity of signal acquisition is determined by the separation of the pulses on CLK pin. Set register bits SINGLE_SHOT_MODE_PPG and PDN_OSC_IN_DEEP_SLEEP_PPG to '1', and set the PRPCT register (counts of the 128 kHz clock) to start beyond the start of the Deep sleep window. Additionally, if the programmable interrupt INT_OUT2 needs to be generated, program the EN_INT_IN_SINGLE_SHOT register bit to '1' and position the interrupt to start and end before the start of the Deep sleep window. The start and end counts for the programmable interrupt are based on the internal (128 kHz) clock.
4. **Mixed Clock mode:** A free running clock on the CLK pin is used by the PRF counter to set the PRF. The timing engine runs on the internal 128 kHz oscillator. Set the SINGLE_SHOT_MODE_PPG and EN_MIXED_CLK_MODE_PPG and PDN_OSC_IN_DEEP_SLEEP_PPG bits to '1'. The start and end counts for programmable interrupts are based on the free running input clock on the CLK pin.
5. **Synchronous Mixed clock mode:** This mode is similar to the Mixed clock mode but in this mode, the internal oscillator's clock is synchronized to the external clock and equal to 4 times the external clock frequency. In addition to the settings for the Mixed clock mode, set EN_SYNC_INT_OSC to 1.

7.4.5 Sleep phase modes

The AFE has three signal acquisition modes that can be chosen through the MODE_SEL register:

1. **PPG acquisition mode:** In this mode, up to 24 PPG phases can be acquired
2. **Mixed acquisition mode:** In this mode, one ECG signal and up to 24 PPG phases can be acquired.
3. **ECG acquisition mode:** In this mode, one ECG signal can be acquired.

7.4.6 Threshold Detect Modes

7.4.6.1 Normal Threshold Detect Mode

The device has a threshold detect mode that can be enabled by setting the THR_DET_EN register bit. In this mode, the device compares the output code of the selected phase with respect to a programmed set of lower and upper limits. Based on the comparison, a THR_DET_RDY interrupt goes high during the corresponding window of the DATA_RDY pulse of that PRF cycle. The number of the phase, the data from which is to be used for the Threshold detect comparison is as (REG_THR_DET_PHASE+1) where the register takes values from 0 to 23. Threshold detection is done only on the output from TIA1 in the specified phase. The appropriate data associated with the phase selected for threshold detection (designated as Phase N in [Table 7-75](#)) is set by the per-phase control THR_SEL_DATA_CTRL.

Table 7-75. Manner in which the Data from Phase Selected for Threshold Detection is used for Comparison

THR_SEL_DATA_CTRL	Which data is used for comparison in Phase N
0	Not used
1	Phase N output
2	Phase N – Phase N-1 ⁽¹⁾
3	Phase N-1 – Average (Phase N, Phase N-2) ⁽¹⁾

(1) Set only if all relevant phases # (example. N, N-1 and N-2) exist and are not masked.

The data as selected from [Table 7-75](#) for the chosen phase can be compared against a set of signed 12-bit codes called HIGH_THRESHOLD_CODE and LOW_THRESHOLD_CODE. The THR_DET_RDY is generated if the output word (signed) constructed using the 12 MSBs of the 22-bit output code of the threshold detection phase falls within the programmed High and low thresholds. By programming the THR_SEL_LOGIC bit to '01', the THR_DET_RDY can be made to get generated if the output word falls outside the High and Low thresholds. The THR_DET_RDY interrupt has roughly the same timing as the DATA_RDY interrupt.

7.4.6.2 Combinational Threshold Detect Mode

The device has a combinational threshold detect mode that can be enabled by setting the THR_DET_EN and COMB_THR_DET_EN register bits. In this mode, the device compares the output code of a selected combination of phases with respect to a programmed set of lower and upper limits. Based on the combination of comparisons, a THR_DET_RDY interrupt goes high during the corresponding window of the DATA_RDY pulse of that PRF cycle.

A per-phase register control (2-bit) THR_SEL_DATA_CTRL determines the manner in which the data from a phase should be used for the comparison against the thresholds as shown in [Table 7-76](#)

Table 7-76. Manner in which a data from a phase is used for comparison against the thresholds

THR_SEL_DATA_CTRL	Which data is used for comparison/combination in Phase N
0	Not used
1	Phase N output
2	Phase N – Phase N-1 ⁽¹⁾
3	Phase N-1 – Average (Phase N, Phase N-2) ⁽¹⁾

(1) Set only if all relevant phases # (eg. N, N-1 and N-2) exist and are not masked.

The data resulting from each phase (defined as in Table) can be compared against either of two sets of 12-bit codes. The selection of which set to use is based on the per-phase register bit THR_SEL as shown in [Table 7-77](#)

Table 7-77. Selection of high and low thresholds for a phase

THR_SEL	12-bit High Code used for comparison	12-bit Low code used for comparison
0	HIGH_THRESHOLD_CODE1	LOW_THRESHOLD_CODE1
1	HIGH_THRESHOLD_CODE2	LOW_THRESHOLD_CODE2

By default, the THR_DET_RDY interrupt is generated if all of the selected phases are within the range as set by the respective low and high threshold codes. The manner of combining the different checks to generate the THR_DET_RDY can be altered by using the register control THR_SEL_LOGIC as shown in [Table 7-78](#)

Table 7-78. Register control for setting the combination logic for the Combinational Threshold detect

THR_SEL_LOGIC Register setting (in binary)	CONDITION USED FOR THR_DET_RDY generation
00	ALL of the chosen checks IN range
01	ANY of the chosen checks OUT of range
10	ANY of the chosen checks IN range
11	ALL of the chosen checks OUT of range

The THR_DET_RDY interrupt has the same timing as the DATA_RDY interrupt.

The result from the comparison of Phase N is stored in a register flag THR_PPG_FLAGN (N from 1..24) which can be read out through the I2C/SPI interface. For example, the result of comparison of Phase 1 is stored in the register flag THR_PPG_FLAG1.

Note

The flags are reset to '0' at the beginning of every PRF cycle and are updated to the proper value at the end of the Active phase of the PRF cycle. Therefore, the flags should be read out during the Deep sleep portion of the PRF cycle. Also, the THR_SEL_LOGIC control does not alter the generation of the flags. A flag is generated if the chosen phase data is within the range of the programmed thresholds irrespective of the THR_SEL_LOGIC setting.

7.4.7 LED Under-Current Detection

The AFE has an LED Under current detect (UCD) circuit that when enabled helps monitor a likelihood of under-current of any of the 8 LEDs. The mechanism of under-current detection is indirect and is based on a monitoring of the voltage across the LED current driver when the corresponding LED* turns on.

The LED under-current detection can be turned on by enabling the EN_LED_UCD register control. When enabled, the voltage across the LED current driver in each LED phase is compared with a programmable threshold voltage (V_{THR}) during each LED ON phase. The register control PROG_VTHR_UCD for programming this threshold voltage is shown in [Table 7-79](#).

Table 7-79. Register control for programming V_{THR}

PROG_VTHR_UCD Register value	Threshold voltage used for LED under-current detection (V_{THR}) in Volts
0	0.2
1	0.225
2	0.25
3	0.275
4	0.3
5	0.325
6	0.35
7	0.375

The result of the eight comparison are stored in the register bits FLAG_UCD_LED1..FLAG_UCD_LED8 for LED1..LED8 respectively. The detailed circuit scheme of the UCD circuit is shown in [Figure 7-82](#).

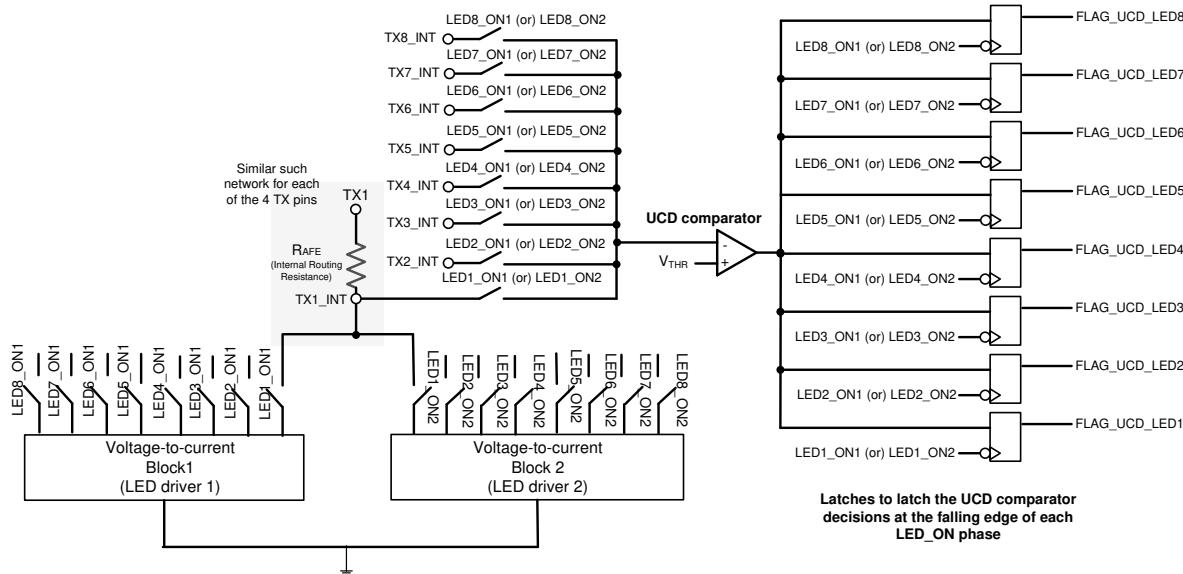


Figure 7-82. Circuit scheme of the LED Under-current detect (UCD) circuit

The following points need to be noted while using the UCD circuit:

1. The UCD circuit should be enabled only for use cases where the LED_ON signal associated with the eight LEDs are all non-overlapping. Enabling the UCD circuit for a case where the LED_ON signals associated with two or more LEDs are overlapping will cause the corresponding TX pins to get shorted through the switches connecting the TX_INT nodes to the input of the UCD comparator, and may result in faulty current settings for the associated LEDs.
2. The UCD flags have valid information only if the corresponding TX pin has an LED connected to it.

Application information for the UCD circuit:

Figure 7-83 shows the LED connection to the TX pin and the voltage drops from the LED supply to ground. For simplicity, connection of only one of the LEDs is shown.

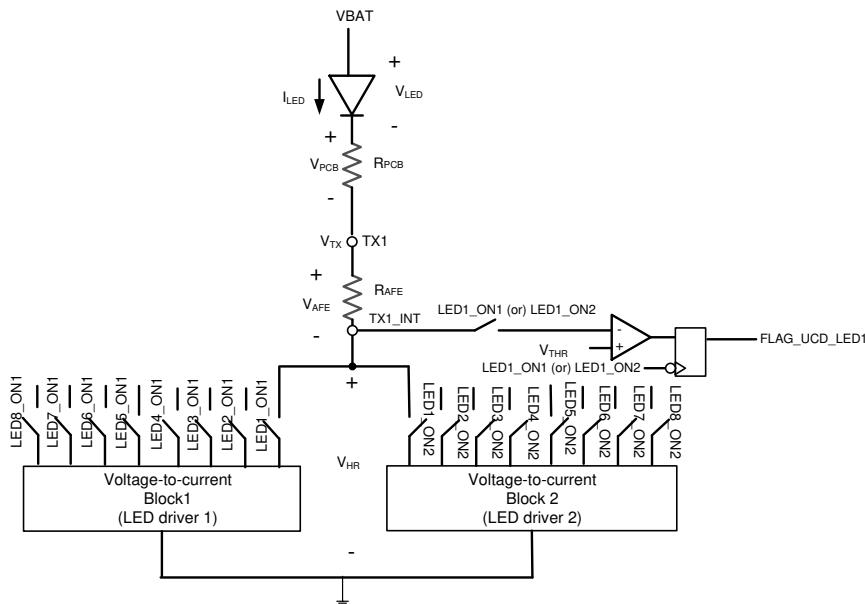


Figure 7-83. Connection of the LED to the TX pin and associated voltage drops

Assuming that LED_SUP is directly connected to the battery, the intent of the UCD circuit is to be able to estimate when the battery falls below a threshold voltage that could likely cause the LEDs to become

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significantly less brighter than the desired setting. There are multiple voltage drops in the path between LED_SUP and ground as shown in [Figure 7-83](#). These parameters are described below:

V_{BAT} = Battery voltage (connected to the anode of the LED)

V_{LED} = Forward voltage of the LED, a function of the current through the LED

R_{PCB} = Routing resistance of the trace on the PCB in series with the LED

V_{PCB} = Voltage drop across R_{PCB} = $I_{LED} \times R_{PCB}$

V_{TX} = Voltage at the TX pin

R_{AFE} = Routing resistance between LED current driver (internal node TX1_INT) and TX pin = $1\text{-}2\Omega$

V_{AFE} = Voltage drop across R_{AFE} = $I_{LED} \times R_{AFE}$

V_{HR} = Headroom voltage available for the LED current driver

$$V_{TX} = \text{Voltage at the TX pin} = V_{HR} + V_{AFE} \quad (7)$$

$$V_{BAT} = V_{LED} + V_{PCB} + V_{TX} \quad (8)$$

Let us first analyze a case where V_{BAT} is high enough such that V_{HR} is much higher than the minimum voltage needed for the LED current driver to operate in a constant current mode. Let us refer to the LED current corresponding to this case as I_{LED_FINAL} . This current corresponds to the ILED register current setting but could deviate from the nominal value because of part to part variations. As V_{BAT} is lowered, the LED current remains relatively flat (and close to I_{LED_FINAL}) because of the high DC PSRR of the LED current driver. However, at some low enough V_{BAT} , V_{HR} starts to go below the threshold required for the LED current driver's current to stay flat, and I_{LED} starts to fall relative to I_{LED_FINAL} . The intent of the UCD circuit is to flag the advent of the LED driver into this under-current region

The principle of operation of the UCD is as follows: the UCD senses V_{HR} during the ON time of each LED and compares it against the programmed voltage threshold (V_{THR}). The result of the comparison is stored in the FLAG_UCD* register bit (one for each LED phase). If the FLAG_UCD* register bit reads '1', then it indicates the likelihood that V_{HR} could have fallen low enough so as to cause the actual LED driver current to be much lower than the set current

The UCD circuit works by estimating the headroom voltage rather than actually measuring the LED current. As a result, the FLAG_UCD is an indirect indicator of an under-current situation. [Table 7-80](#) shows the recommended settings of the UCD thresholds (V_{THR}) for the two LED full-scale current modes (25 mA and 50 mA). With these recommended threshold settings, a case of the FLAG_UCD* flag reading '0' can be used to determine that the LED current setting has not fallen lower than 90% of I_{LED_FINAL}

Table 7-80. Recommended UCD threshold settings

LED full-scale current mode	Recommended UCD threshold setting (V_{THR})
25 mA	0.275 V
50 mA	0.375 V

The depiction of the FLAG_UCD* state relative to the LED current vs. headroom plot is shown in [Figure 7-84](#). The zone shown in Yellow depicts the bounds of where the FLAG_UCD transitions relative to the LED driver's current versus headroom plot across units for the VTHR settings shown in [Table 7-80](#)

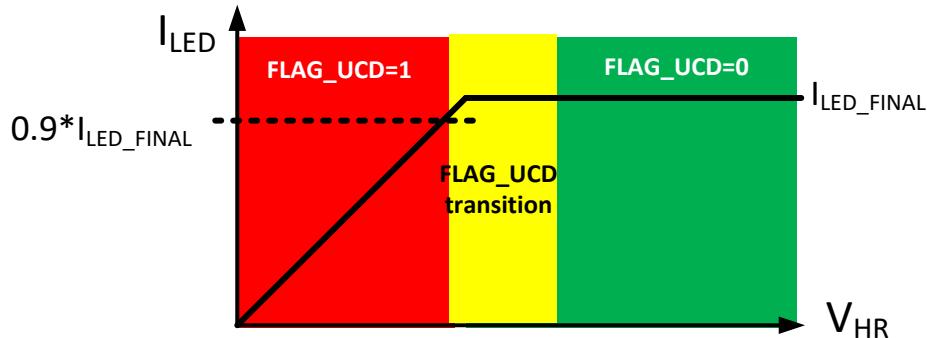


Figure 7-84. Depiction of the FLAG_UCD* relative to the LED current vs. headroom plot

Based on the FLAG_UCD transition point, the voltage at VBAT can be estimated as follows for the 25 mA current mode and 25 mA current setting:

$$V_{THR} = \text{Recommended threshold voltage setting for the UCD (Typical value from Table 7-80)} = 275 \text{ mV}$$

$$\delta V_{THR} = \text{Part-to-part variation in } V_{THR} \text{ including the UCD comparator offset} = +/- 50 \text{ mV}$$

$$V_{HR} (\text{FLAG_UCD from 0->1}) = 225-325 \text{ mV}$$

$$V_{AFE} = 25-50 \text{ mV} \text{ (Based on } R_{AFE} = 1-2\Omega \text{ and } I_{LED} = 25 \text{ mA)}$$

Therefore, from [Equation 7](#), voltage at the TX pin at the FLAG_UCD transition point is calculated as:

$$V_{TX} (\text{FLAG_UCD from 0->1}) = 250-375 \text{ mV}$$

V_{BAT} can be then calculated using [Equation 8](#).

On reading the FLAG_UCD to be '1', the resultant action taken by the MCU could either be to reduce of the LED current setting (which would result in a reduction of V_{LED} , an associated increase in V_{HR} , and a possible release of the FLAG_UCD*) or to prompt to the user about the battery requiring charging

7.4.8 Parallel AFE operation modes

The device provides a synchronized way to operate two AFEs in either sequential or concurrent mode.

1. Parallel AFEs with sequential operation
2. Parallel AFEs with concurrent operation

7.4.8.1 Parallel AFEs with sequential operation

Figure 7-85 shows two AFEs connected to operate with sequential active phases. AFE1 is operated in the Synchronous Mixed clock mode with 32.768 kHz RTC clock on CLK pin. The 128 kHz clock of AFE1 (synchronized to 4x the frequency of the RTC clock) is output on GPIO2 by setting the register control EN_128K_CLKOUT to '1' (set register bit EN_GPIO2_OUT to '1' to enable the output on the GPIO2 pin, and set INT_MUX_GPIO2_1 to '00'). The GPIO2 pin of AFE1 is connected to the CLK pin of AFE2. AFE2 is operated in external clock mode. Programmable interrupt INT_OUT2 from AFE1 is positioned to come after the active phases of AFE1, and is routed from the ADC_RDY pin of AFE1 to the GPIO2 pin of AFE2. Set EN_GPIO2_IN to '1' for AFE2 to configure GPIO2 as an input pin. Set INPUT_PRF_RST_ON_GPIO2 to '11' for AFE2 to cause the interrupt on GPIO2 to serve as a PRF reset pulse for AFE2. Set INPUT_PRF_RST_ON_GPIO2 to '00' for AFE1. Figure 7-86 shows the timing scheme.

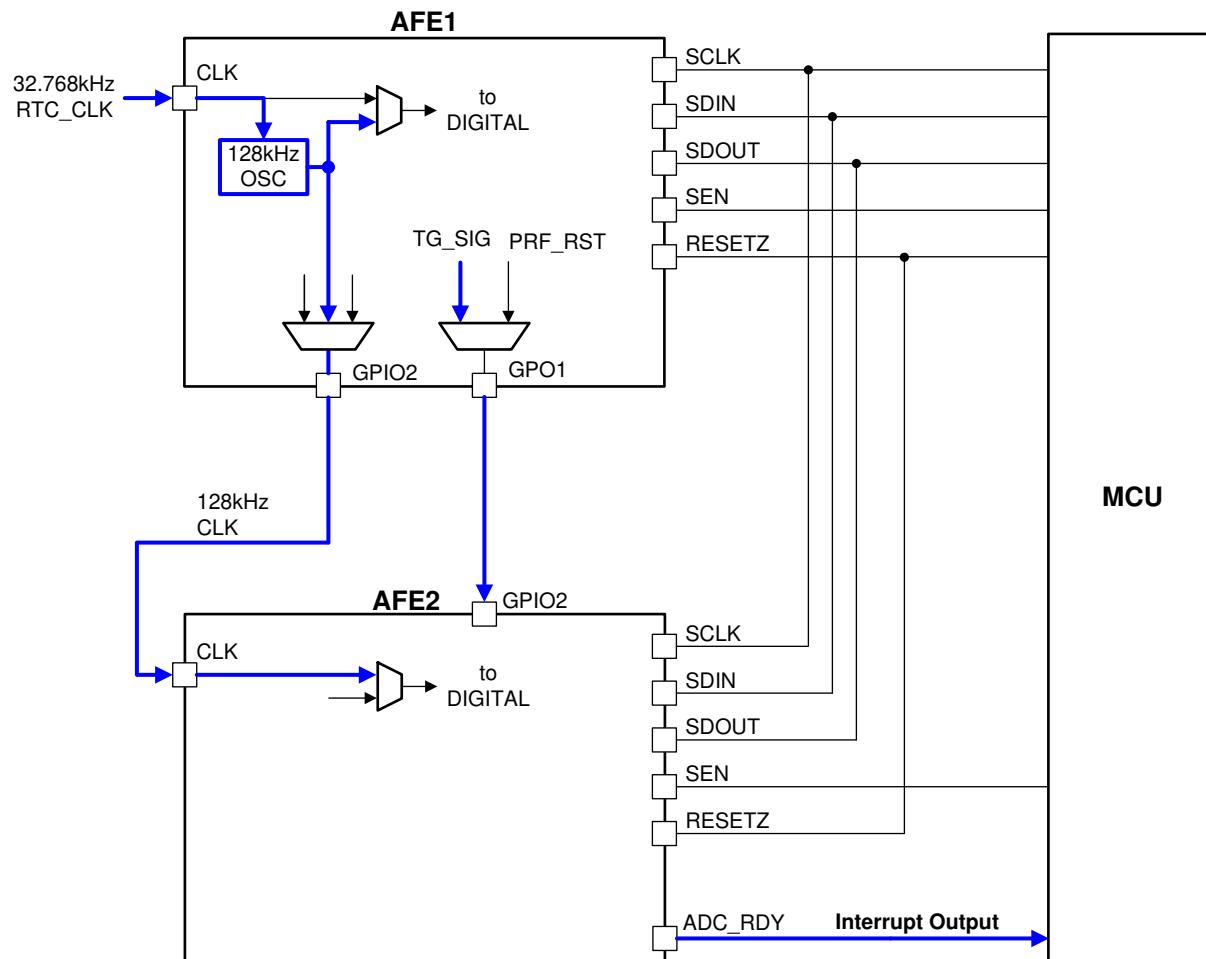


Figure 7-85. Two AFEs connected to operate with sequential active phases

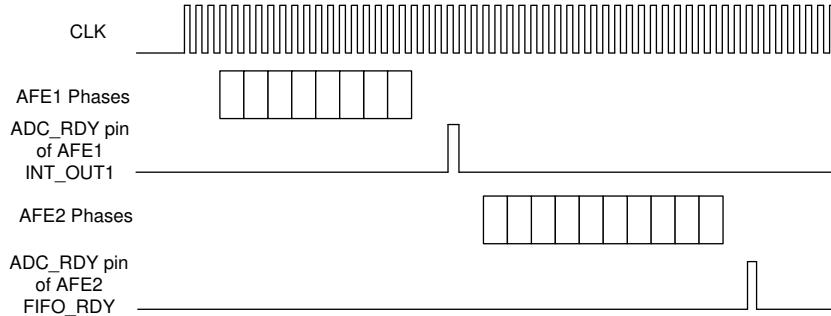


Figure 7-86. Timing for two AFEs connected to operate with sequential active phases

7.4.8.2 Parallel AFEs with concurrent operation

Figure 7-87 shows two AFEs connected to operate with concurrent active phases. AFE1 is operated in the Synchronous Mixed clock mode with 32.768 kHz RTC clock on CLK pin. The 128 kHz clock of AFE1 (synchronized to 4x the frequency of the RTC clock) is output on GPIO2 by setting the register control EN_128K_CLKOUT to '1' (set register bit EN_GPIO2_OUT to '1' to enable the output on the GPIO2 pin, and set INT_MUX_GPIO2_1 to '00'). The GPIO2 pin of AFE1 is connected to the CLK pin of AFE2. AFE2 is operated in external clock mode. An interrupt PRF_RST (timed at the reset point of the PRF counter of AFE1) is output on the ADC_RDY pin of AFE1. This PRF_RST is connected to the GPIO2 pin of AFE2. Set EN_GPIO2_IN to '1' for AFE2 to configure GPIO2 as an input pin. Set INPUT_PRF_RST_ON_GPIO2 to '11' for AFE2 to cause the interrupt on GPIO2 to serve as a PRF reset pulse for AFE2. Set INPUT_PRF_RST_ON_GPIO2 to '01' for AFE1. Figure 7-88 shows the timing scheme.

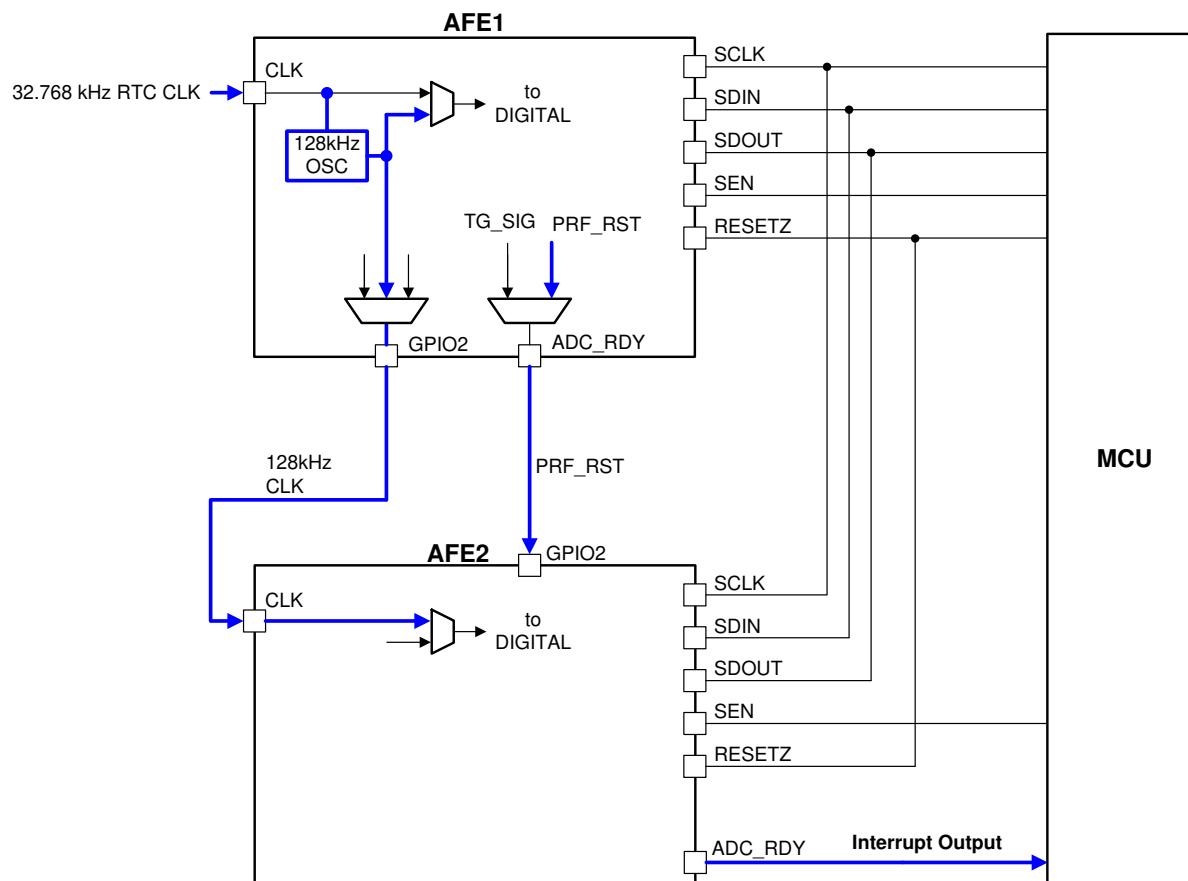


Figure 7-87. Two AFEs connected for concurrent operation with simultaneous active phases

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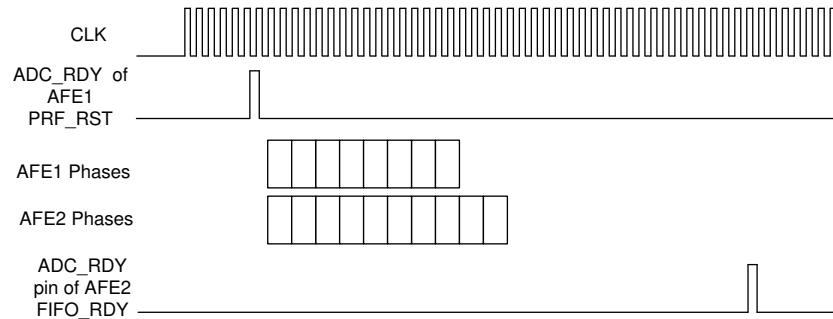


Figure 7-88. Timing for two AFEs connected for concurrent operation with simultaneous active phases

7.4.9 Interrupt Modes

The AFE performs several signal processing operations and checks. A soft interrupt is associated with each of these events as listed in [Table 7-81](#). The soft interrupts can be combined to produce a hard interrupt on either the ADC_RDY pin or the GPIO2 pin. By default, an event on any of the soft interrupts results in the firing of the hard interrupt. By setting the appropriate Mask bit to 1, a particular soft interrupt event can be masked such that the soft interrupt event does not result in the hard interrupt generation.

The interrupts are listed in [Table 7-81](#).

Table 7-81. Soft and Hard Interrupts

Soft interrupt	Register that indicates event status	Description of the associated event	Mask bit for generation of Hard interrupt
DC_LEAD_DET	ECG_RLD_LEAD_STATUS, ECG_INP_LEAD_STATUS, ECG_INM_LEAD_STATUS	DC lead status change flag. generated when there is a change in the connection of ECG leads (ECG_INP, ECG_INM and RLD)	MASK_DC_LEAD_DET
AC LEAD ON	AC LEAD SEQ: Indicates the most recent AC lead status. 01 – Most recent lead status is AC LEAD ON 10 – Most recent lead status is AC LEAD OFF	AC lead-on flag. Works only in the ECG mode. Indicates that the ECG leads (ECG_INP, ECG_INM) are connected.	MASK_AC LEAD ON
AC LEAD OFF	AC LEAD SEQ: Indicates the most recent AC lead status. 01 – Most recent lead status is AC LEAD ON 10 – Most recent lead status is AC LEAD OFF	AC lead-off flag. Works only in the ECG mode. Indicates that the ECG leads (ECG_INP, ECG_INM) are disconnected..	MASK_AC LEAD OFF
FIFO_RDY	REG_POINTER_DIFF	FIFO ready flag. Indicates that FIFO reached the Watermark level in that PRF cycle	MASK_ADC_FIFO_RDY

If during the active state of the PRF cycle, any of the unmasked soft interrupts became high, the AFE makes the hard interrupt active in that PRF cycle by generating a single pulse after the active phases are completed. The timing diagram showing the generation of the hard interrupt is shown in [Figure 7-89](#). In cases where the soft interrupt goes high during the Deep-sleep state of the PRF cycle (for example, the DC lead interrupt), the hard interrupt pulse is generated immediately.

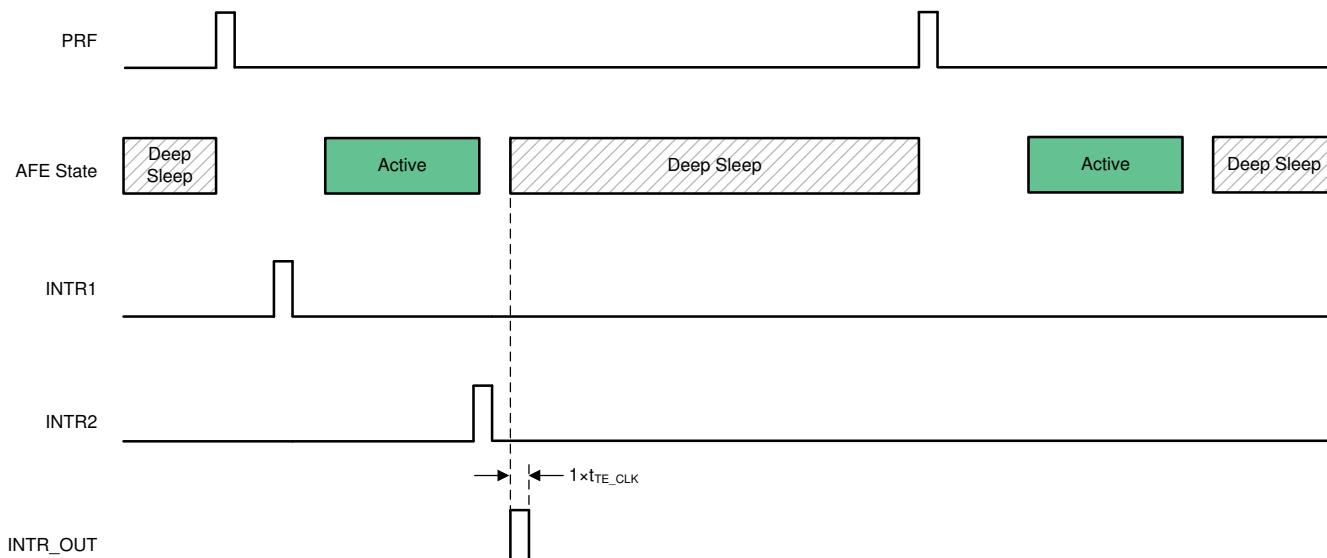


Figure 7-89. Hard Interrupt (INTR_OUT) Generation Timing When Multiple Unmasked Soft Interrupts (INTR1, INTR2) Go High Before the Deep Sleep State of the PRF Cycle

Figure 7-90 shows the timing where one unmasked soft interrupt goes high before entering the Deep-sleep state and another soft interrupt goes high after entering the Deep-sleep state.

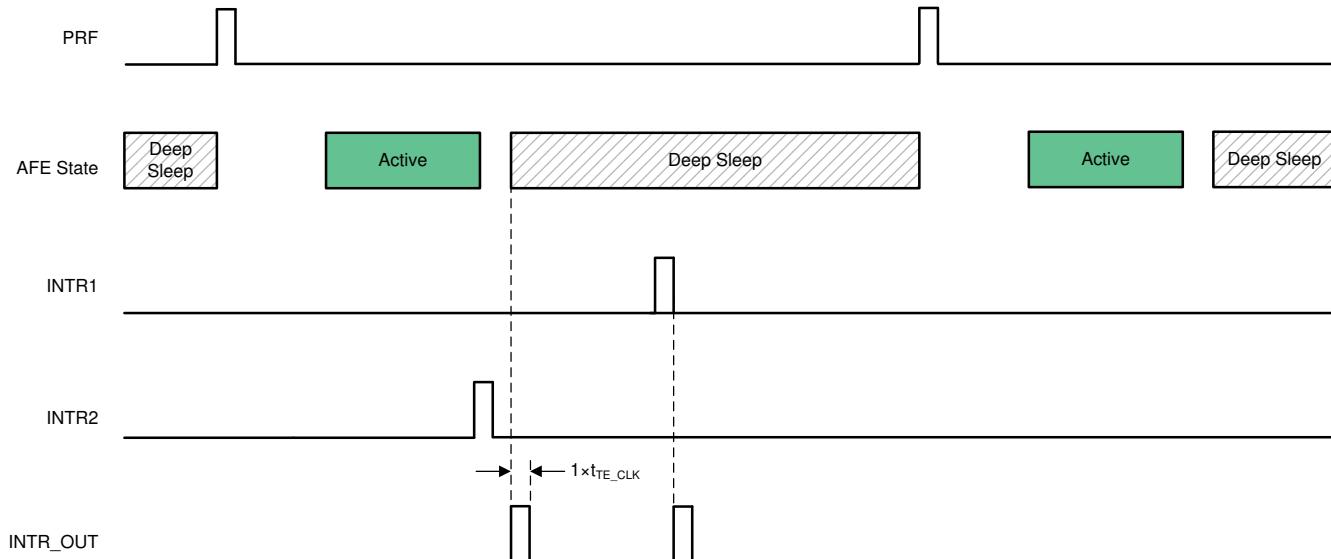


Figure 7-90. Hard Interrupt (INTR_OUT) Generation Timing When One Unmasked Soft Interrupt (INTR1) Goes High Before the Deep Sleep State and a Second Interrupt (INTR2) Goes High After Entering the Deep-Sleep State

Figure 7-91 shows the generation of the hard interrupt when the device does not enter a Deep sleep state during the PRF cycle, a likely case when operating at high PRF.

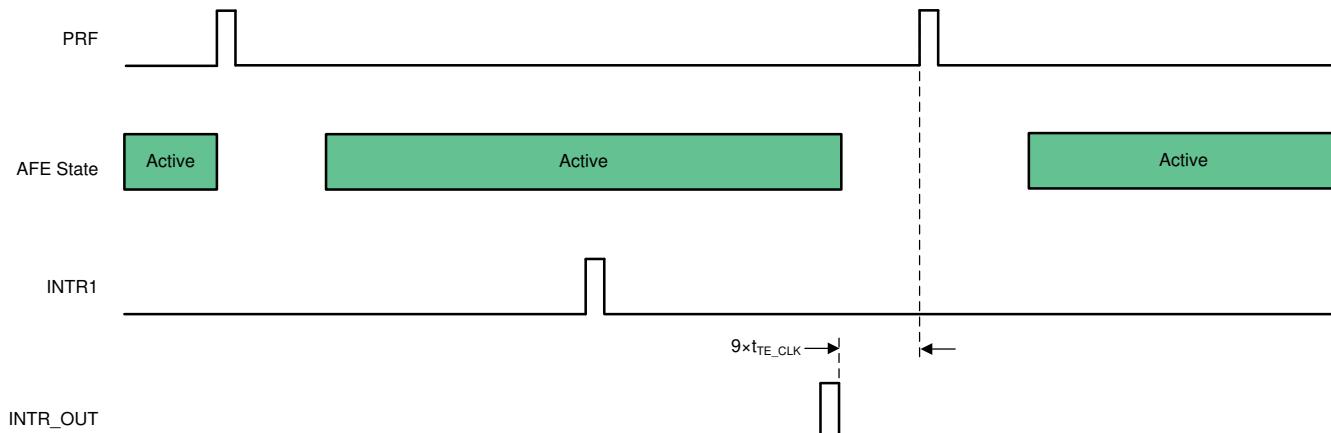


Figure 7-91. Hard Interrupt (INTR_OUT) Generation Timing When There is no Deep-Sleep State During the PRF Cycle

In addition to the Hard interrupt, other interrupts can also be made to output on the ADC_RDY and GPIO2 pins. These interrupts are listed in Table 7-82.

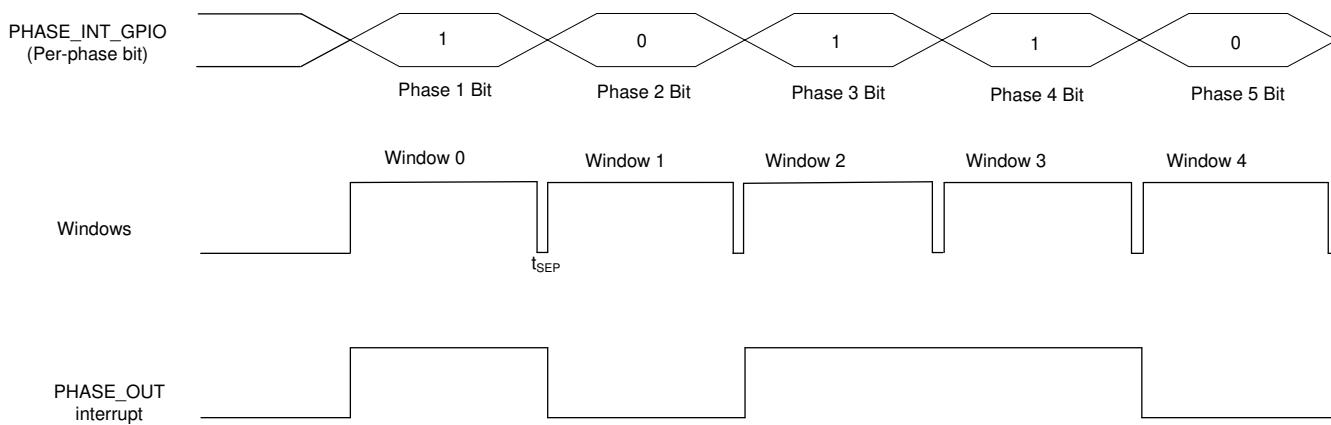
Table 7-82. Description of Various Interrupts

INTERRUPT	DESCRIPTION	Position
DATA_RDY	Interrupt that comes out at the same rate as the output data rate. Rate is equal to the PRF.	DATA_RDY pulse
FIFO_RDY	Interrupt issued when the Watermark level is reached	Same as DATA_RDY pulse (delayed by 1 count)

Table 7-82. Description of Various Interrupts (continued)

INTERRUPT	DESCRIPTION	Position
THR_DET_RDY	Threshold detect interrupt applicable when the device is in threshold detect mode; goes high during the corresponding DATA_RDY window in the periods where the threshold comparisons result in a TRUE	Same as DATA_RDY pulse (delayed by 1 count)
INT_OUT2	Interrupt 2 that is generated as a pulse every period.	Set through timing counts of PRF counter as PROG_INT2_STC to PROG_INT2_ENDC + 1
PHASE_OUT	Phase-based interrupt that is generated on a per-phase control bit PHASE_INT_GPIO	Goes high in all the phase windows where the PHASE_INT_GPIO bit is high

The PHASE_OUT interrupt can be made to go high during any signal phase by setting the per-phase control bits PHASE_INT_GPIO. An illustration of the PHASE_OUT interrupt is shown in [Figure 7-92](#)

**Figure 7-92. Generation of PHASE_OUT Interrupt Based on the Per-Phase Bits**

The register controls for the selection of interrupts on the various output pins is shown in [Table 7-83](#) and [Table 7-84](#).

Table 7-83. Selection of Interrupts Output on the ADC_RDY Pin

INT_MUX_ADC_RDY_2	INT_MUX_ADC_RDY_1	INTERRUPT OUTPUT ON ADC_RDY PIN ⁽¹⁾	ADDITIONAL CONTROLS REQUIRED
0	00	DATA_RDY	—
0	01	THR_DET_RDY	Set THR_DET_EN = 1
0	10	FIFO_RDY	Set FIFO_EN = 1
1	00	Hard Interrupt	Set appropriate masking bits
1	01	INT_OUT2	
1	11	PRF_RST ⁽²⁾	INPUT_PRF_RST_ON_GPIO2 = 01
Other settings		Do not use	

(1) When the EN_GPIO2_INT_ON_ADC_RDY bit is set to '1', the interrupt on ADC_RDY is determined by [Table 7-84](#).

(2) PRF_RST corresponds to a pulse that is synchronized to the start of the PRF cycle. AFE is PRF_RST Master in a parallel AFE configuration.

Table 7-84. Selection of Input/Output on GPIO2 Pin

EN_GPIO2_IN	EN_GPIO2_OUT	INT_MUX_GPIO2_2	INT_MUX_GPIO2_1	EN_PHASE_INT_GPIO	EN_128K_CLKOUT	GPIO2 – INPUT OR OUTPUT	OUTPUT ON GPIO2	INPUT ON GPIO2	ADDITIONAL CONTROLS REQUIRED ^{(1) (2)}
0	1	0	00	0	0	OUTPUT	INT_OUT2		
0	1	0	00	1	0	OUTPUT	PHASE_OUT		
0	1	0	00	0	1	OUTPUT	CLK_128KHz		
0	1	0	01	0	0	OUTPUT	DATA_RDY		
0	1	0	10	0	0	OUTPUT	THR_DET_RDY		THR_DET_EN = 1
0	1	0	11	0	0	OUTPUT	FIFO_RDY		FIFO_EN = 1
0	1	1	00	0	0	OUTPUT	Hard interrupt		Set appropriate masking bits
1	0	0	00	0	0	INPUT		PRF_RST ⁽³⁾	INPUT_PRF_RST_ON_GPIO2 = '11'

- (1) While operating in the Single-shot clocking mode, additionally set EN_INT_IN_SINGLE_SHOT register bit to '1' and position the interrupt before the start of the Deep sleep window. The start and end counts are based on the internal (128 kHz) clock.
- (2) Interrupts programmed to come out on the GPIO2 pin can be made to come out on ADC_RDY pin by setting the EN_GPIO2_INT_ON_ADC_RDY bit to '1'
- (3) PRF_RST corresponds to a pulse that is synchronized to the start of the PRF cycle. AFE is PRF_RST Slave in a parallel AFE configuration.

7.5 Programming

The AFE has both a SPI and an I2C interface which can be selected using the I2C_SPI_SEL pin.

7.5.1 SPI

7.5.1.1 Serial Programming Interface

The SPI consists of four signals: SCLK (serial clock), SDOUT (serial interface data output), SDIN (serial interface data input), and SEN (serial interface enable).

The SPI is enabled by setting the I2C_SPI_SEL pin low. The I2C interface is enabled by setting the I2C_SPI_SEL pin high. Note that the logic high level of I2C_SPI_SEL corresponds to the RX_SUP voltage level. When operating in SPI mode, the pins are reconfigured as shown in [Table 7-85](#).

Table 7-85. Pin Functions in SPI Mode

PIN		PIN FUNCTION IN SPI MODE
NAME	NUMBER	
SCLK	F3	SCLK: serial clock input
SDIN	F2	SDIN: serial clock data
SEN	E3	SEN: chip select (active low)
SDOUT	E2	SDOUT: serial data output

The serial clock (SCLK) is the serial peripheral interface (SPI) serial clock. SCLK shifts in commands and shifts out data from the device. SCLK features a Schmitt-triggered input and clocks data out on SDOUT. Data are clocked in on SDIN. Even though the input has hysteresis, SCLK is recommended to be kept as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low. The serial interface enable (SEN) enables the serial interface to clock data from SDIN into the device.

7.5.1.2 Writing Data

The SPI_REG_READ register bit must be set to 0 before writing to a register. When SEN is low:

- Serially shifting bits into the device is enabled.
- Serial data (on SDIN) are latched at every SCLK rising edge.
- The serial data are loaded into the register at every 32nd SCLK rising edge.

The first eight bits form the register address and the remaining 24 bits form the register data. [Figure 7-93](#) shows an SPI timing diagram for a single write operation.

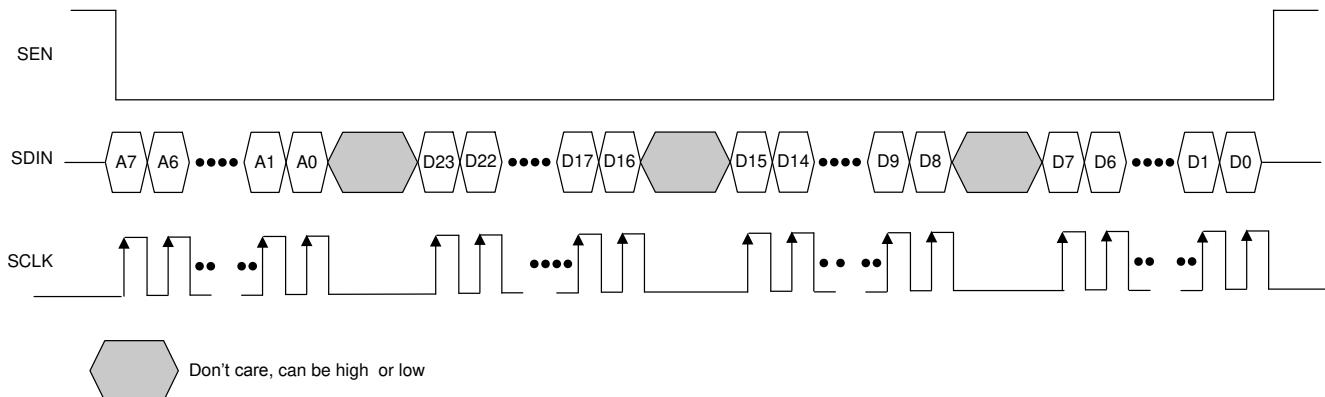


Figure 7-93. AFE SPI Write Timing Diagram

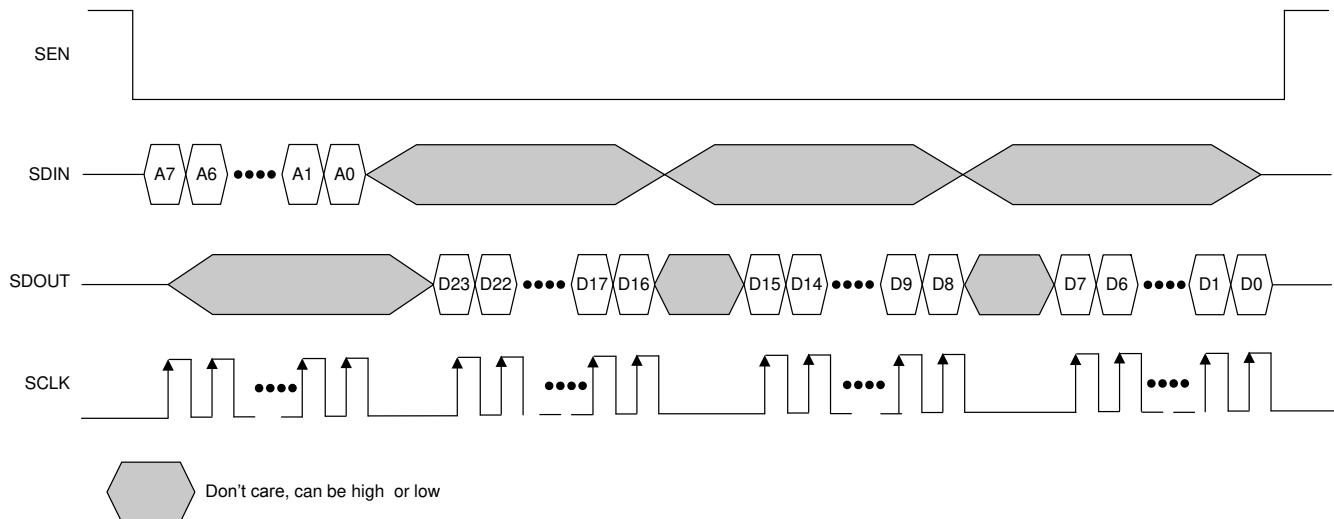
7.5.1.3 Reading Data

The AFE includes a mode where the contents of the internal registers can be read back on SDOUT. This mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the AFE. To enable this mode, first set the SPI_REG_READ register bit using the SPI write command.

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In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the AFE outputs the contents of the specified register on the SDOUT pin. [Figure 7-94](#) shows an SPI timing diagram for a single read operation. The SDOUT is in tri-state whenever SEN is high (inactive) and is active when SEN is low. The SDOUT buffer can be permanently tri-stated by using the SDOUT_TRISTATE register bit.



- The SPI_REG_READ register bit must be enabled before attempting a serial readout from the AFE.
- Specify the register address of the content that must be read back on bits A[7:0].
- The AFE outputs the contents of the specified register on the SDOUT pin

Figure 7-94. AFE SPI Read Timing Diagram

7.5.1.4 Continuous Read/Write Mode in the SPI

The SPI can be operated in a continuous read or write mode by writing 1 to the RW_CONT bit. In this mode, the address is specified at the start of the read or write cycle. Subsequently, the address of the register being read or written auto-increments until SEN is pulled high. The continuous write and read modes are illustrated in [Figure 7-95](#) and [Figure 7-96](#), respectively.

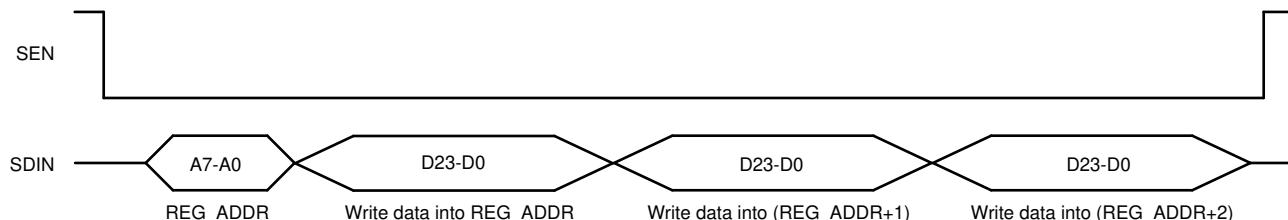


Figure 7-95. Continuous SPI Write (RW_CONT = 1)

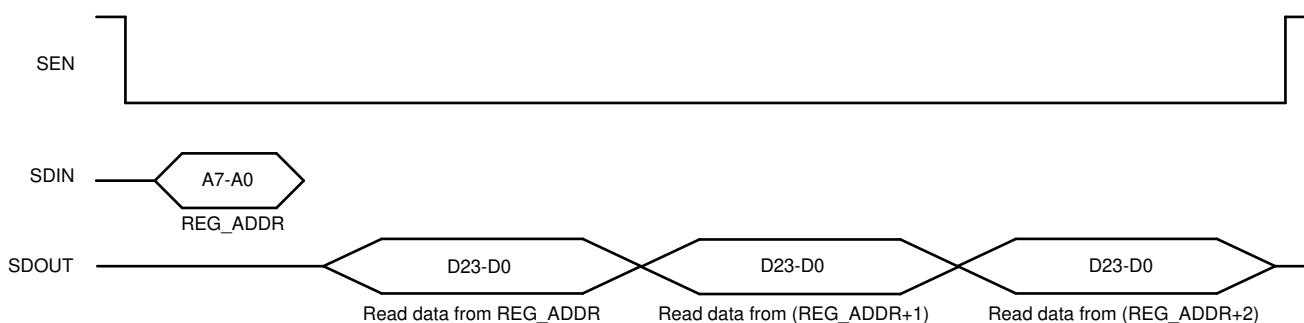


Figure 7-96. Continuous SPI Read (RW_CONT = 1, SPI_REG_READ = 1)

7.5.1.5 FIFO Readout Through the SPI Over a Single Continuous Read Operation

The contents of the FIFO can be readout in a continuous manner using the SPI. The RW_CONT bit is not required to be set to 1 to continuously read out the FIFO. The SPI_REG_READ bit is also not required to be set to 1 when reading out the FIFO. The REG_ADDR used for reading out the FIFO must be set to FFh. The readout method is shown in [Figure 7-97](#).

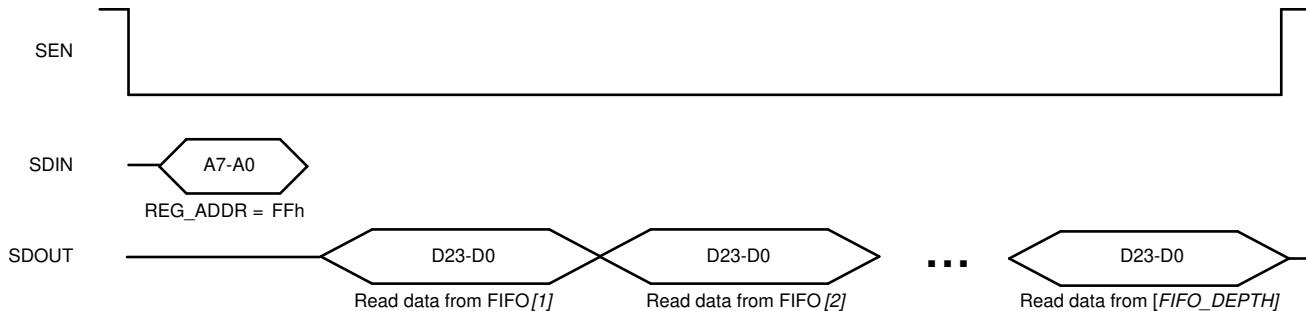


Figure 7-97. Continuous FIFO Readout Through the SPI

7.5.1.6 FIFO Readout Through the SPI Over Multiple Read Operations

The FIFO can also be read out over multiple read operations. [Figure 7-98](#) shows the FIFO being read out over two read operations.

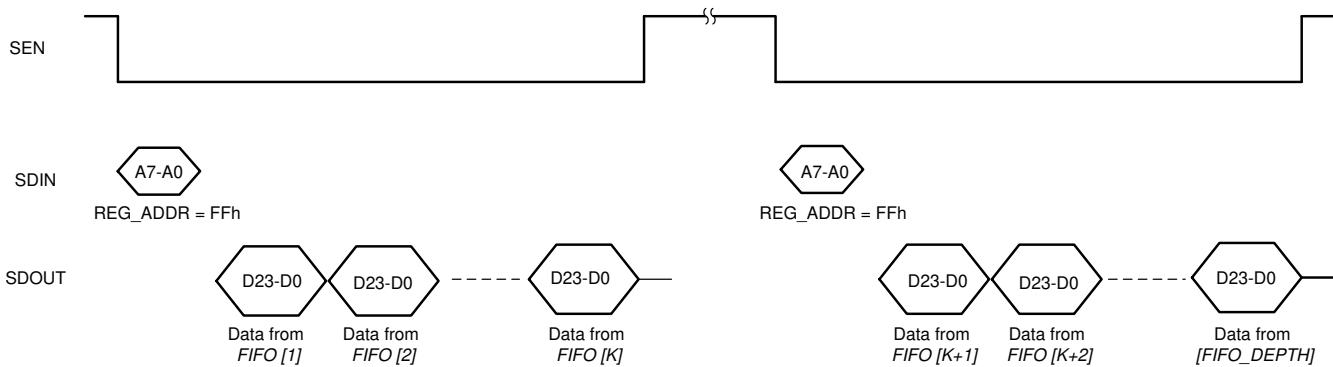


Figure 7-98. FIFO Readout Over Two Read Operations

7.5.2 I²C Interface

7.5.2.1 I²C Protocol

The AFE has an I²C interface for communication. The I2C_CLK and I2C_DAT lines require external pullup resistors to IO_SUP. See the I²C protocol standards documents for details of the I²C interface. This section only describes certain key features of the interface. The data on I2C_DAT must be stable during the high level of I2C_CLK and can transition during the low level of I2C_CLK, as shown in [Figure 7-99](#).

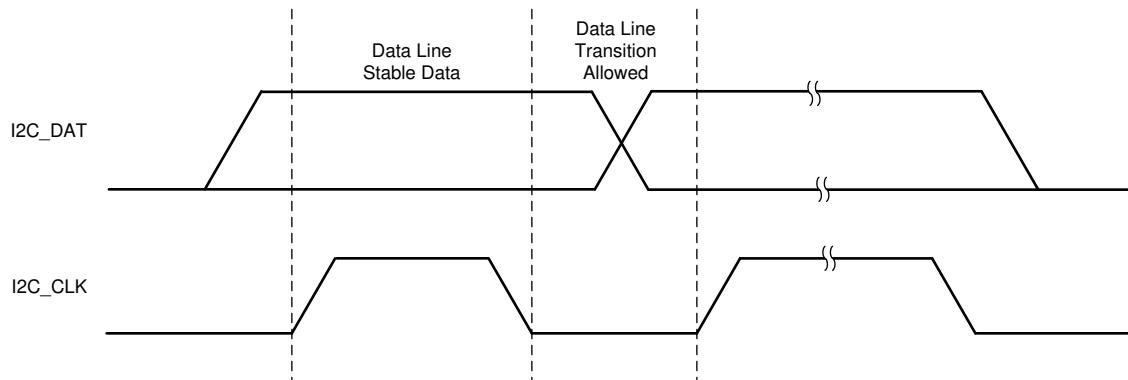


Figure 7-99. Allowed Transition of I2C_DAT During Data Bit Transmission

The start condition is indicated by a high-to-low transition of the I2C_DAT line when the I2C_CLK is high. A stop condition is indicated by a low-to-high transition of the I2C_DAT line when the I2C_CLK is high. [Figure 7-100](#) shows the start and stop conditions.

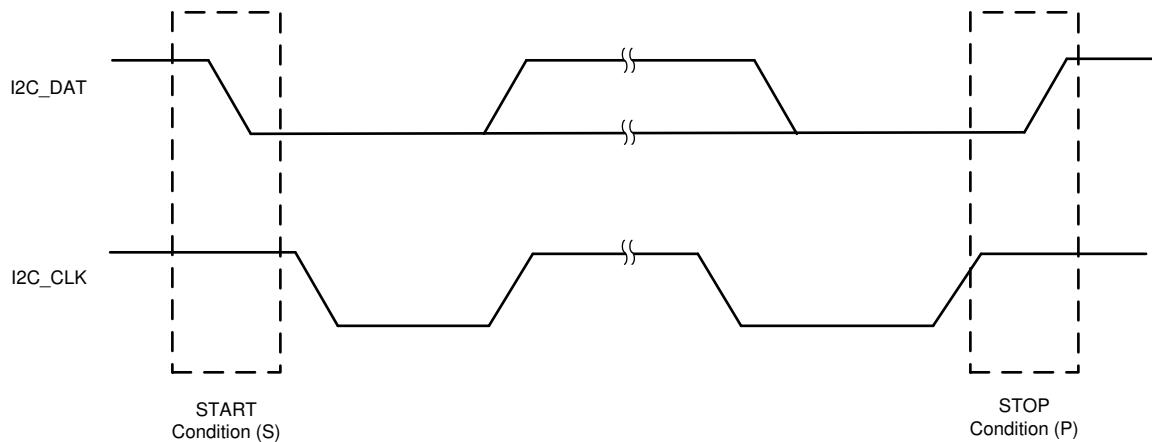
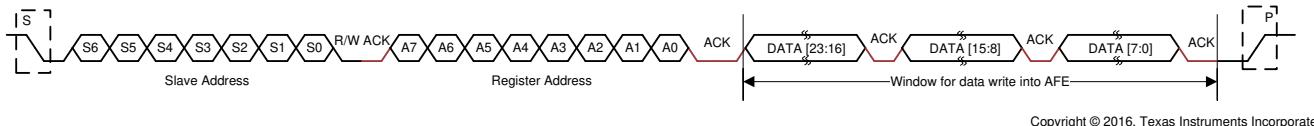


Figure 7-100. Transition of I2C_DAT During Start and Stop Conditions

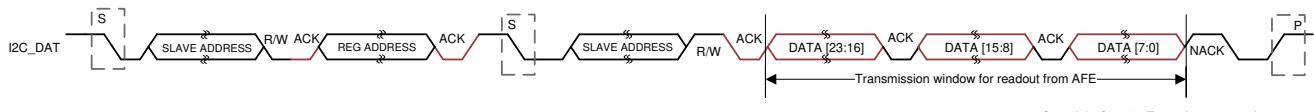
7.5.2.2 I²C Write and Read Operations

With the previously mentioned protocols for data, start, and stop conditions, the write and read operations are as shown in [Figure 7-101](#) and [Figure 7-102](#), respectively. The slave address for the AFE (indicated as SA6 to SA0) is a 7-bit representation of either address 5Bh (when the SEN pin is low) or 5Ah (when the SEN pin is high). The R/W bit is the read/write bit and is set to 1 for reads and 0 for writes. In [Figure 7-101](#) and [Figure 7-102](#), the activity performed by the host is shown in black whereas the activity from the AFE is shown in red. Thus, after the host sends the slave address during a write operation, the AFE pulls the I2C_DAT line low (shown as ACK) if the slave address matches 5Bh (when SEN is low) or 5Ah (when SEN is high). Similarly, the host pulls the I2C_DAT line high (shown as NACK) as an acknowledgment of a successfully completed read operation involving three bytes of data.



A. Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 7-101. I²C Write Option Timing Diagram

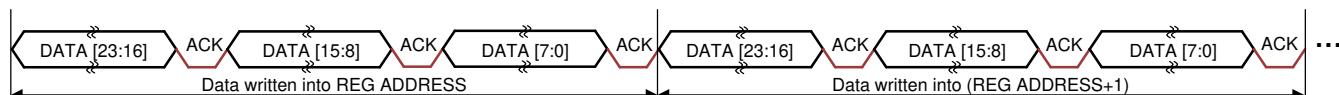


A. Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 7-102. I²C Read Option Timing Diagram

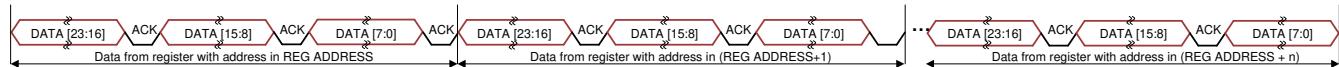
7.5.2.3 Continuous I²C Read/Write Mode

Continuous read/write mode is supported by enabling the RW_CONT bit. The FIFO, however, can be read out continuously without setting this bit. The protocol for the continuous write and read modes are shown in [Figure 7-103](#) and [Figure 7-104](#), respectively.



A. Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 7-103. Window for Data Writes Into the AFE in Continuous I²C Write Mode (RW_CONT = 1)

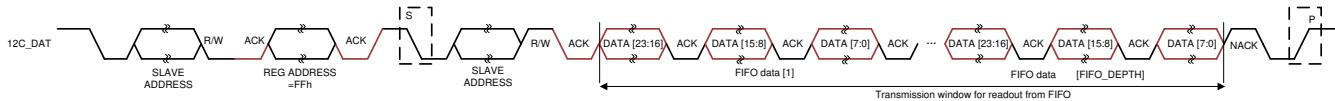


A. Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 7-104. Transmission Window for Readout From the AFE in Continuous I²C Read Mode (RW_CONT = 1)

7.5.2.4 Data Readout From the FIFO Using a Single Continuous Read Operation

When the MCU receives the FIFO_RDY interrupt, the FIFO can be read out through the I²C interface in continuous readout mode, as shown in [Figure 7-105](#). The REG ADDRESS for reading out the FIFO is FFh. The parameter [FIFO_DEPTH] refers to the utilized depth of the FIFO as set by the Watermark level. Additional restrictions on the FIFO readout timing are mentioned in the *FIFO Readout Timing Constraints* section.

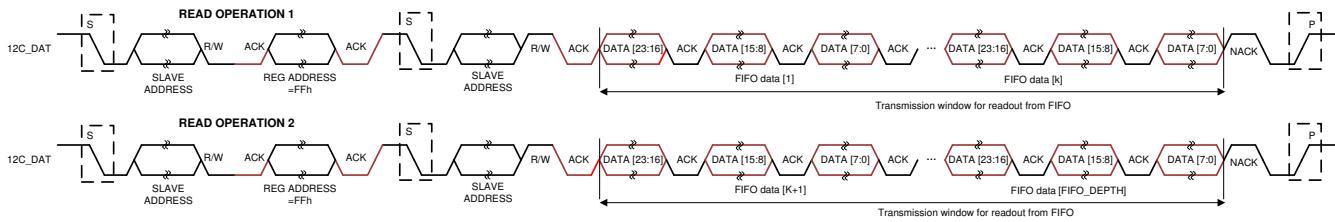


- A. Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 7-105. I²C Readout From the FIFO

7.5.2.5 Data Readout From the FIFO Over Multiple Read Operations

The data from the FIFO can also be read out over multiple read operations with a break in between the operations. A readout over two such read operations is shown in [Figure 7-106](#).



- A. Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 7-106. I²C Readout From the FIFO Over Two Read Operations

7.6 Register Map

7.6.1 Page selection

The register map has two pages as shown in [Figure 7-107](#). The per-phase registers are located in Page 1 (PAGE_SEL = '1') starting from address 20h to 97h. Set the PAGE_SEL register bit to the appropriate value to read and write from the desired page.

Registers with address from 00h to 1Fh and A7h to FFh can be written to and read from any page irrespective of the setting of the PAGE_SEL. The SPI_REG_READ bit in register 0h serves as the register read enable bit for registers in both Page 0 as well as in Page 1.

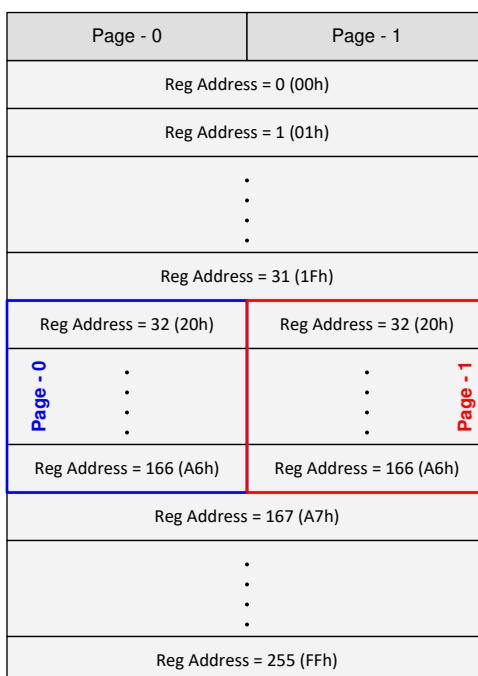


Figure 7-107. Register Map Organization

7.6.2 Page 0 Registers

Table 7-86. Page 0 registers

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RW_CONT	SW_RESET	0	TM_COUNT_RST	PAGE_SEL SPI_REG_READ
CONTROL1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CONTROL2	2	0		POL_IOFFDAC_AMB		POL_IOFFDAC_LED		USE_AMB_DAC_FOR_LED		EN_DUAL_TIA_GBL															INT_MUX_GPIO2_1
GPIO2_INT_ST	3	0	0	0	0	0	0	0	0																PROG_INT2_STC
GPIO2_INT_END	4	0	0	0	0	0	0	0	0																PROG_INT2_ENDC
PRF_CONTROL	1D	TIMER_ENABLE	PRF_COUNTER_ENABLE	LEAD_DET_MODULE_CLK_EN	0	0	0	0	0																REG_PRPCT_PPG

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL3	1E	0	0	0	0	0	0	0	0	EN_MIXED_CLK_MODE_PPG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
CONTROL4	23									EN_AMB_DAC_LSB	0													PDN AFE	
CONTROL5	24	0	0	0	0	0	0	0	0	EN_LED_OFFDAC_TIA2	0														
CONTROL6	25	0	0	0	0	0	0	0	0	EN_LED_OFFDAC_TIA1	P	0	0	0	0	0	0	0	0	0	0	0	0	0	
READ_DESIGNID	28	x	x	x	x					DESIGN_ID							x	x	x	x	x	x	x	x	
CONTROL7	29									SDOUT_TRISTATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ_FLAG1	30	x	x	x	x	INT_MUX_GPIO2_2	CONNECT_BG_TO_PIN	FLAG_LDO_STATE	0	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0	0
CONTROL8	31	0	0	0	0	0	0	0	0	0	0	0	EN_GPIO2_IN	0	0	0	0	0	0	0	0	0	0	0	0
CONTROL9	42	0	0	0	0	0	0	0	0	0	0	0	REG_WM_FIFO	0	0	0	0	0	0	0	0	0	0	0	0
CONTROL10	4B	0	EN_128K_CLKOUT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CONTROL11	4E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL12	50	0	0	0	0	ECG_INA_GAIN	0	SINGLE_SHOT_MODE_PPG	0	PDN_OSC_IN_DEEP_SLEEP_PPG	EN_LED_UCD	0	PROG_VTHR_UCD	0	0	0	0	0	0	0	0	0	CONFIG_RLD_AS_UGB	0	0
CONTROL13	51	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FIFO_OFFSET_TO_FORCE	
CONTROL14	62	0	0	0	0	PROG_VCM_RLD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CONTROL15	6C	0	0	0	0	0	0	DIS_CHOP_INA	PROG_INA_SAT_THR_H	PROG_INA_SAT_THR_L	0	EN_INA_OUT_COMP	0	0	0	AUTO_MASK_FIFO_RDY	MASK_FIFO_RDY	FORCE_FIFO_OFFSET	0	0	0	0	0	0	0
READ_POINTER	6D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	REG_POINTER_DIFF	
CONTROL16	72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IFS_AMB_OFFDAC_TIA2	

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CONTROL17	73	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
CONTROL18	74	0																								
			EN_SYNC_INT_OSC																							
CONTROL19	75		OVERRIDE_BW_PRE	AC_LEAD_DET_CLK_PHASE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FILT_BW_SET1	78				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FILT_BW_SET2	79	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CONFIG_DRE1	7C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
CONFIG_DRE2	7D	0	0	0	0	0	0	0	0	0	REG_SCALE_DRE_LOOP4		0	REG_SCALE_DRE_LOOP3		0	REG_SCALE_DRE_LOOP2	0	REG_SCALE_DRE_LOOP1								
THR_CODE1	80	HIGH_THRESHOLD_CODE1												LOW_THRESHOLD_CODE1													
THR_CODE2	81	HIGH_THRESHOLD_CODE2												LOW_THRESHOLD_CODE2													
CONTROL20	88	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EN_PHASE_INT_GPIO	0	MODE_EN_FRAME_SYNC	0	REG_NUMPHASE_PPG						
TIMING1	8A	0	0	0	REG_TACTIVE_PWRUP								0	0	0	REG_TDEEP_SLEEP_PWRUP											
TIMING2	8B	0	0	0	0	0	0	0	0	0	0	0	0	REG_TSEP_CONV_LED		0	0	0	0	0	0	0	0	0	0		
TIMING3	8C	0	0	REG_TSEP	0	0	REG_TLED_SAMP								0	0	0	0	0	0	0	0	0	0	0	0	
TIMING4	8D	0	0	0	0	REG_TW_DATA_RDY		0	0	0	0	0	0	0	0	0	REG_TACTIVE_DATA_RDY										
TIMING5	8E	0	0	0	REG_TDEEP_SLEEP_PWDN								0	0	0	REG_TACTIVE_PWDN											
TIMING6	8F	0	MASK_REVERSE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EXT_CLK_FREQ		
CONTROL21	92	0	0	0	0	0	REG_STEP_COUNT												EN_INT_IN_SINGLE_SHOT	0	0	0	0	0	0	0	0
CONTROL22	93	0	0	0	CHANNEL_OFFSET_AACM_TIA1												0	0	0	0	0	0	0	0	0	0	
CONTROL23	94	0	0	0	CHANNEL_OFFSET_AACM_TIA2												REG_TW_FILTER_PRE										

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Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CONTROL24	95			EMBED_ANA_AACM_IN_FIFO																						
DEC1TO4_1	96	0	0		TSEP_ANA_ACQ_LED_OVERRIDE																					
DEC1TO4_2	97	EN_PPG_DEC4		REG_NUMPH_PPG_DEC4	EN_PPG_DEC3	PPG_DEC2_TIA_SEL																				
LOOP1_AACM1	98	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOOP1_AACM2	99	0																							CALIB_AACM_LOOP1
LOOP1_AACM3	9A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IOFFDAC_AACM_READ_LOOP1
LOOP2_AACM1	9C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOOP2_AACM2	9D	0	RECONV_THRES_H_AACM_LOOP2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALIB_AACM_LOOP2

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOOP2_AACM3	9E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	POL_OFFSET_AACM_READ_LOOP2									
LOOP3_AACM1	A0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FREEZE_AACM_LOOP3	0	0	0	0	0	0	0	0	0
LOOP3_AACM2	A1	0	RECONV_THRESH_AACM_LOOP3		0	0	0	0	0	0	0	0	0	0	0	CALIB_AACM_LOOP3									
LOOP3_AACM3	A2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	POL_OFFSET_AACM_READ_LOOP3									

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOOP4_AACM1	A4	0	0	0	0	0	0	0	0	0	0	0	0	0	FREEZE_AACM_LOOP4	0	0	0	0	0	0	0	0	0	
LOOP4_AACM2	A5	0					0	0	0	0	0	0	0	0									CALIB_AACM_LOOP4		
LOOP4_AACM3	A6	0	0	0	0	0	0	0	0	0	0	0	0	0	POL_OFFDAC_AACM_READ_LOOP4										
DEC5TO8_1	A9	0	0	0	0	0	PPG_DEC8_TIA_SEL	PPG_DEC7_TIA_SEL	PPG_DEC6_TIA_SEL	PPG_DEC5_TIA_SEL	0	REG_PPG_DEC8_FACTOR	0	REG_PPG_DEC7_FACTOR	0	REG_PPG_DEC6_FACTOR	0	REG_PPG_DEC5_FACTOR							

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEC5TO8_2	AA	REG_NUMPH_PPG_DEC8						EN_PPG_DEC7						EN_PPG_DEC6					EN_PPG_DEC5						
OSC_CALIB	B0	EN_128K_CLK_CALIB_2																							
THR_GLOBAL	B4	COMB THR_DET_EN	0	CLK_128K_CALIB_RANGE	0	CLK_128K_CALIB_RECONV_THR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
READ_THR_FLAG	B5																								
READ_AC_LEAD	B6																								
THR_AC_LEAD	B7	0																							
AC LEAD DEMOD MOD	B8																								
HPF_REG1	B9	0																							

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
HPF_REG2	BA	0	0	0	0	0	0	SCALE_ LEAD_DET_WIDTH_PPG																LEAD_DET_WIDTH		
MASK_INT_REG	BB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INTR_SOFT	BC	AC_ LEAD_SEQ		x	x			ECG_INA_OUTP_COMP_H	ECG_INA_OUTP_COMP_L	ECG_INA_OUTML_COMP_H	ECG_INA_OUTML_COMP_L	ECG_INA_OUTM_COMP_H	ECG_INA_OUTM_COMP_L	x	x	x	x	x	x	ECG_INP_LEAD_STATUS	ECG_INM_LEAD_STATUS	ECG_RLD_LEAD_STATUS	x	x	x	x
CONTROL25	BE	0	EN_DATA_MARKER		0	0	0	DEEP_SLEEP_DEL																MODE_SEL		
																				REL_AFE_FREEZE	REG_INTR_TO_AFE	0				
																				MASK_ADC_FIFO_RDY	MASK_AC_LEAD_OFF	x				
																				MASK_AC_LEAD_ON	MASK_DC_LEAD_DET	x				

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
MIX_REG1	C0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
MIX_REG2	C1	CONFIG_TS7_MIX			CONFIG_TS6_MIX			CONFIG_TS5_MIX			CONFIG_TS4_MIX			CONFIG_TS3_MIX			CONFIG_TS2_MIX			CONFIG_TS1_MIX			CONFIG_TS0_MIX				
MIX_REG3	C2	0	0	REG_NUM_PSAW_MIX			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	REG_NUM_ESAW_MIX	
PSAW_REG1	C3	REG_NUM_PH_PSAW2			0	0	0	REG_START_PH_PSAW2						REG_NUM_PH_PSAW1			0	0	0	0	0	0	0	0	0	REG_START_PH_PSAW1	
PSAW_REG2	C4	REG_NUM_PH_PSAW4			0	0	0	REG_START_PH_PSAW4						REG_NUM_PH_PSAW3			0	0	0	0	0	0	0	0	0	REG_START_PH_PSAW3	
MIX_REG4	C5	0	0	SEL_DEC_FILT_TS7_MIX		0	0	SEL_DEC_FILT_TS6_MIX		0	0	SEL_DEC_FILT_TS5_MIX		0	0	SEL_DEC_FILT_TS4_MIX		0	0	SEL_DEC_FILT_TS3_MIX		0	0	SEL_DEC_FILT_TS2_MIX			
MIX_REG5	C7	0	0	REG_PPG_GBL_MASK_FACTOR						0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	REG_ECG_DEC_FACTOR_MIX		
CONTROL26	CA	REG_ACTIVE_CONTROLS																									
CONTROL27	CB	0	0	0	OSC_DIS_128K_NOTPPG		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	

Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL28	CF	0	0	0	0	0	0	0	0	EN_ECG_DIG_SAT_DET	0	0	0	REG_DIG_SAT_THR_H	0	0	0	0	0	0	0	0	0	REG_DIG_SAT_THR_L	
ECG_REG1	D0	0	0	0	0	0	0	0	0	0	0	0	0	REG_PRPCT_ECG											
ECG_REG2	D1	CONFIG_TS7_ECG		CONFIG_TS6_ECG		CONFIG_TS5_ECG		CONFIG_TS4_ECG		CONFIG_TS3_ECG		CONFIG_TS2_ECG		CONFIG_TS1_ECG		CONFIG_TS0_ECG									
ECG_REG3	D2	0	0	0	0	0	0	0	0	0	0	0	0	REG_NUM_ESAW_ECG											
ECG_REG4	D3	0	0	0	SEL_DEC_FILT_TS7_ECG	0	SEL_DEC_FILT_TS6_ECG	0	SEL_DEC_FILT_TS5_ECG	0	SEL_DEC_FILT_TS4_ECG	0	SEL_DEC_FILT_TS3_ECG	0	SEL_DEC_FILT_TS2_ECG	0	SEL_DEC_FILT_TS1_ECG	0	SEL_DEC_FILT_TS0_ECG						
ECG_REG5	D5	0	0	0	REG_FSWITCH_IMP	0	SWAP_BIAS_RES	0	LEAD_DET_THR_H_NOTPPG	0	LEAD_DET_THR_L_NOTPPG	0	EN_LEAD_DET_CURR_NOTPPG	0	EN_LEAD_DET_COMP_NOTPPG	0	SEL_ECG_BIAS_RES_NOTPPG	0	REG_ECG_DEC_FACTOR_ECG						
CONTROL29	D7	0												CFG_RES_ECG_INM_NOTPPG	0	CFG_RES_ECG_INP_NOTPPG	0	CFG_RES_ECG_INP_NOTPPG	0	CFG_RES_ECG_INP_NOTPPG					

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Table 7-86. Page 0 registers (continued)

Name	(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL30	D8	0	0	0	0																				
CONTROL31	D9	0	0	0	0	0	0																		

7.6.3 Page 1 Registers

The registers in Page 1 correspond to the Per-phase register controls for the PPG phases. These registers serve as the common setting across both the PPG acquisition mode as well as the Mixed acquisition mode. The set of 5 registers associated with each phase is listed in [Table 7-87](#). It is important to note that the per-phase registers in Page 1 do not have any default values on reset. Therefore, all 5 address of all the defined phases (#1 to #NUMPHASE) need to be written even if some of these registers contain features not intended for use.

Table 7-87. List of addresses (in Hex) associated with each phase

Phase	Register 1	Register 2	Register 3	Register 4	Register 5					
Phase	Name	Addr1	Name	Addr2	Name	Addr3	Name	Addr4	Name	Addr5
1	REG1_PH1	20	REG2_PH1	21	REG3_PH1	22	REG4_PH1	23	REG5_PH1	24
2	REG1_PH2	25	REG2_PH2	26	REG3_PH2	27	REG4_PH2	28	REG5_PH2	29
3	REG1_PH3	2A	REG2_PH3	2B	REG3_PH3	2C	REG4_PH3	2D	REG5_PH3	2E
4	REG1_PH4	2F	REG2_PH4	30	REG3_PH4	31	REG4_PH4	32	REG5_PH4	33
5	REG1_PH5	34	REG2_PH5	35	REG3_PH5	36	REG4_PH5	37	REG5_PH5	38
6	REG1_PH6	39	REG2_PH6	3A	REG3_PH6	3B	REG4_PH6	3C	REG5_PH6	3D
7	REG1_PH7	3E	REG2_PH7	3F	REG3_PH7	40	REG4_PH7	41	REG5_PH7	42
8	REG1_PH8	43	REG2_PH8	44	REG3_PH8	45	REG4_PH8	46	REG5_PH8	47
9	REG1_PH9	48	REG2_PH9	49	REG3_PH9	4A	REG4_PH9	4B	REG5_PH9	4C
10	REG1_PH10	4D	REG2_PH10	4E	REG3_PH10	4F	REG4_PH10	50	REG5_PH10	51
11	REG1_PH11	52	REG2_PH11	53	REG3_PH11	54	REG4_PH11	55	REG5_PH11	56
12	REG1_PH12	57	REG2_PH12	58	REG3_PH12	59	REG4_PH12	5A	REG5_PH12	5B
13	REG1_PH13	5C	REG2_PH13	5D	REG3_PH13	5E	REG4_PH13	5F	REG5_PH13	60
14	REG1_PH14	61	REG2_PH14	62	REG3_PH14	63	REG4_PH14	64	REG5_PH14	65
15	REG1_PH15	66	REG2_PH15	67	REG3_PH15	68	REG4_PH15	69	REG5_PH15	6A
16	REG1_PH16	6B	REG2_PH16	6C	REG3_PH16	6D	REG4_PH16	6E	REG5_PH16	6F
17	REG1_PH17	70	REG2_PH17	71	REG3_PH17	72	REG4_PH17	73	REG5_PH17	74
18	REG1_PH18	75	REG2_PH18	76	REG3_PH18	77	REG4_PH18	78	REG5_PH18	79
19	REG1_PH19	7A	REG2_PH19	7B	REG3_PH19	7C	REG4_PH19	7D	REG5_PH19	7E
20	REG1_PH20	7F	REG2_PH20	80	REG3_PH20	81	REG4_PH20	82	REG5_PH20	83
21	REG1_PH21	84	REG2_PH21	85	REG3_PH21	86	REG4_PH21	87	REG5_PH21	88
22	REG1_PH22	89	REG2_PH22	8A	REG3_PH22	8B	REG4_PH22	8C	REG5_PH22	8D
23	REG1_PH23	8E	REG2_PH23	8F	REG3_PH23	90	REG4_PH23	91	REG5_PH23	92
24	REG1_PH24	93	REG2_PH24	94	REG3_PH24	95	REG4_PH24	96	REG5_PH24	97

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The per-phase registers (for Phase 1 as an example) are listed in [Table 7-88](#).

Table 7-88. Per-phase registers (shown for Phase 1)

Name	Hex	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
REG1_PH1	20	IN_TIA2<4:1>				IN_TIA1<4:1>				LED_DRV2_TX<8:1>										LED_DRV1_TX<8:1>						
REG2_PH1	21	IOFFDAC_PH_TIA1										USE_DIG_AACM_TIA1	CF_TIA1		REG_LOOP_NUM_TIA1		RF_TIA1			REG_NUMAV						
REG3_PH1	22	TIA_SEL	PHASE_INT_GPIO	0	CONFIG_PHASE_AS_IMP	FIFO_DATA_CTRL_1	THR_SEL_DATA_CTRL	USE_ANA_AACM_TIA1	THR_SEL	USE_ANA_AACM_TIA1	UPDATE_BASELINE_TIA1	FIFO_DATA_CTRL_2	UPDATE_BASELINE_TIA2	STAGGER_LED	FILTER_SET_SEL	x	x	x	REG_TWLED							
REG4_PH1	23	IOFFDAC_PH_TIA2										USE_DIG_AACM_TIA2	CF_TIA2		REG_LOOP_NUM_TIA2		RF_TIA2			x	x	x	x	x		
REG5_PH1	24	DIG_AACM_LED_TIA1	DIG_AACM_LED_TIA2	x	x	REG_PH_MASK_FACTOR	ILED_DRV2										ILED_DRV1									

7.6.3.1 Page 0 Registers Description**7.6.3.1.1 CONTROL0: Register 00h (address = 00h)****Figure 7-108. Register 00h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	FIFO_EN	0	RW_CONT	SW_RESET	0	TM_COUNT_RST	SPI_REG_READ
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 7-89. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
23-7	0	W	0h	Must write 0
6	FIFO_EN	W	0h	0 = FIFO disabled 1 = FIFO enabled
5	0	W	0h	Must write 0
4	RW_CONT			0 = Read or write only one register at a time 1 = Read or write continuously
3	SW_RESET	W	0h	Self-clearing reset bit. For a software reset, write 1.
2	0	W	0h	Must write 0
1	TM_COUNT_RST	W	0h	This bit is used to suspend the count and keep the counter in a reset state.
0	SPI_REG_READ	W	0h	Register readout enable for SPI interface 0 = Register write mode 1 = Enables the readout of write registers Not required for readout of the FIFO data (address FFh).

7.6.3.1.2 CONTROL 1: Register 01h (address = 01h)**Figure 7-109. Register 01h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PAGE_SEL
W-0h							

Table 7-90. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
23-1	0	W	0h	Must write 0
0	PAGE_SEL	W	0h	Page select bit 0 = Subsequent read/ write accesses registers in Page 0 1 = Subsequent read/ write accesses registers in Page 1.

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7.6.3.1.3 CONTROL2: Register 02h (address = 02h)**Figure 7-110. Register 02h**

23	22	21	20	19	18	17	16
0	POL_IOFFDAC_AMB	POL_IOFFDAC_LED	0	USE_AMB_DAC_FOR_LED	EN_DUAL_TIA_GBL	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	INT_MUX_GPIO2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-91. Register 02h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22	POL_IOFFDAC_AMB	R/W	0h	Polarity of Ambient Offset DAC – if anode of PD connects to INM and cathode of PD connects to INP, set polarity to ‘1’ to subtract Ambient Offset DAC current from the PD current.
21	POL_IOFFDAC_LED	R/W	0h	Polarity of LED Offset DAC - if anode of PD connects to INM and cathode of PD connects to INP, set polarity to ‘1’ to subtract LED offset DAC current from the PD current.
20	0	R/W	0h	Must write 0
19	USE_AMB_DAC_FOR_LED	R/W	0h	Set to ‘0’ when LED Offset DAC is intended to be used to cancel additional DC in the LED phase. Set to ‘1’ when the Ambient Offset DAC is intended to be used to cancel additional DC in the LED phase.
18	EN_DUAL_TIA_GBL	R/W	0h	Set to ‘1’ when any of the phases involves use of TIA2. Setting this bit to ‘1’ keeps TIA2 also on during the active phase, resulting in an increase in the active phase current.
17-2	0	R/W	0h	Must write 0
1-0	INT_MUX_GPIO2_1	R/W	0h	Controls interrupt to be output on the GPIO2 pin. Additionally set EN_GPIO2_OUT register bit to ‘1’ to enable the interrupt.

7.6.3.1.4 GPIO2_INT_ST: Register 03h (address = 03h)**Figure 7-111. Register 03h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PROG_INT2_STC							
R/W-0h							
7	6	5	4	3	2	1	0
PROG_INT2_STC							
R/W-0h							

Table 7-92. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	R/W	0h	Must write 0
15-0	PROG_INT2_STC	R/W	0h	Start count for INT_OUT2 (programmable interrupt on GPIO2)

7.6.3.1.5 GPIO2_INT_END: Register 04h (address = 04h)**Figure 7-112. Register 04h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PROG_INT2_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
PROG_INT2_ENDC							
R/W-0h							

Table 7-93. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	R/W	0h	Must write 0
15-0	PROG_INT2_ENDC	R/W	0h	End count for INT_OUT2 (programmable interrupt on GPIO2)

7.6.3.1.6 PRF_CONTROL: Register 1Dh (address = 1Dh)**Figure 7-113. Register 1Dh**

23	22	21	20	19	18	17	16
TIMER_ENABLE	PRF_COUNTER_ENABLE	LEAD_DET_MODULE_CLK_EN	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
REG_PRPCT							
R/W-0h							
7	6	5	4	3	2	1	0
REG_PRPCT							
R/W-0h							

Table 7-94. Register 1Dh Field Descriptions

Bit	Field	Type	Reset	Description
23	TIMER_ENABLE	R/W	0h	This bit enables the timing engine. Set in conjunction with PRF_COUNTER_ENABLE. 0 = Timer module disabled 1 = Enables timer module.
22	PRF_COUNTER_ENABLE	R/W	0h	This bit enables the PRF counter that defines the PRF. Set in conjunction with TIMER_ENABLE. 0 = PRF counter disabled 1 = PRF counter enabled.
21	LEAD_DET_MODULE_CLK_EN	R/W	0h	Set to '1' when using any of the lead detection modes. This bit enables additional clocking associated with lead detection.
20-16	0	R/W	0h	Must write 0
15-0	REG_PRPCT	R/W	0h	The PRF timer count, PRPCT, is set as the decimal value of REG_PRPCT. The timing engine counts until (PRPCT-1) and then returns back to 0 to start the next count. REG_PRPCT thereby sets the PRF period.

7.6.3.1.7 CONTROL3: Register 1Eh (address = 1Eh)**Figure 7-114. Register 1Eh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
EN_MIXED_CLK_MODE_PPG	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-95. Register 1Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	R/W	0h	Must write 0
15	EN_MIXED_CLK_MODE_PPG	R/W	0h	Enables the Mixed clock mode in which an external free running clock (for eg. 32.768-kHz clock) is used to clock the PRF counter and set the PRF, and the internal 128-kHz oscillator is used by the timing engine to define the signal phases. While setting the mixed clock mode, also set the SINGLE_SHOT_MODE_PPG bit to '1'.
14-0	0	R/W	0h	Must write 0

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7.6.3.1.8 CONTROL4: Register 23h (address = 23h)**Figure 7-115. Register 23h**

23	22	21	20	19	18	17	16
PD_DISCONNECT_TIA1	0	0	0	0	ILED_FS		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8
EN_AMB_DAC_LSB	0	PD_DISCONNECT_TIA2		IFS_AMB_OFFSETDAC_TIA1	OSC_DIS_128K_PPG		0
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PDNAFE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-96. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
23	PD_DISCONNECT_TIA1	R/W	0h	Disconnect all PDs from the TIA1 inputs. When set to '1', input current to the TIA1 in a phase is equal to Offset DAC current setting for that phase.
22-19	0	R/W	0h	Must write 0
18-16	ILED_FS	R/W	0h	Full-scale current control for LED
15	EN_AMB_DAC_LSB	R/W	0h	Enables the LSB bit control of the Ambient DAC. Always set to '1'.
14	0	R/W	0h	Must write 0
13	PD_DISCONNECT_TIA2	R/W	0h	Disconnect all PDs from the TIA2 inputs. When set to '1', input current to the TIA2 in a phase is equal to Offset DAC current setting for that phase.
12-10	IFS_AMB_OFFSETDAC_TIA1	R/W	0h	Programs the full-scale current range of the Ambient Offset Cancellation DAC for TIA1
9	OSC_DIS_128K_PPG	R/W	0h	Disable 128-kHz oscillator when operating in the PPG mode 0 – Internal oscillator enabled 1 – Internal oscillator disabled
8-1	0	W	0h	Must write 0.
0	PDNAFE	R/W	0h	Software power-down mode. When operating in the LDO bypass mode, set the PDN_BG_IN_DEEP_SLEEP bit to '1' to get to the lowest power state in the Software power-down mode. Also, to minimize the power consumption, set the acquisition mode to PPG mode before going into Software powerdown mode.

7.6.3.1.9 CONTROL5: Register 24h (address = 24h)**Figure 7-116. Register 24h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	EN_LED_OFFSET_AC_TIA2	EN_LED_OFFSET_AC_TIA1	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-97. Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
23-15	0	R/W	0h	Must write 0
14	EN_LED_OFFSETDAC_TIA2	R/W	0h	Enables the LED Offset DAC corresponding to TIA2
13	EN_LED_OFFSETDAC_TIA1	R/W	0h	Enables the LED Offset DAC corresponding to TIA1
12-0	0	R/W	0h	Must write 0

7.6.3.1.10 CONTROL6: Register 25h (address = 25h)**Figure 7-117. Register 25h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	CLK_DIV_CLK	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-98. Register 25h Field Descriptions

Bit	Field	Type	Reset	Description
23-4	0	R/W	0h	Must write 0
3-2	CLK_DIV_CLK	R/W	0h	Programs division ratio of external clock in external clock mode. Useful if operating with external clocks of 256 kHz or 512 kHz.
1-0	0	R/W	0h	Must write 0

7.6.3.1.11 READ_DESIGNID: Register 28h (address = 28h)**Figure 7-118. Register 28h**

23	22	21	20	19	18	17	16
x	x	x	x				DESIGN_ID
R-x	R-x	R-x	R-x				R-1Eh
15	14	13	12	11	10	9	8
				DESIGN_ID			
					R-1Eh		
7	6	5	4	3	2	1	0
DESIGN_ID	x	x	x	x	x	x	x
R-1Eh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh

Table 7-99. Register 28h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	x	R	x	Read only register
19-7	DESIGN_ID	R	0Eh - Rev 1 Silicon	Design ID register ⁽¹⁾
			1Eh - Rev 2 Silicon	
6-0	x	R	x	Read only register

(1) Rev2 Silicon has additional register controls AC_LEAD_DEMOD_CFG and AC_LEAD_DET_CLK_PHASE.

7.6.3.1.12 CONTROL7: Register 29h (address = 29h)**Figure 7-119. Register 29h**

23	22	21	20	19	18	17	16
EN_GPIO2_INT_ON_ADC_RDY	0	0	0	EN_GPIO2_OUT	DIS_DEEP_SLEEP	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	SDOUT_TRISTATE	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-100. Register 29h Field Descriptions

Bit	Field	Type	Reset	Description
23	EN_GPIO2_INT_ON_ADC_RDY	R/W	0h	Set to '1' to make the interrupt programmed on GPIO2 pin to come out on ADC_RDY pin instead
22-20	0	R/W	0h	Must write 0
19	EN_GPIO2_OUT	R/W	0h	Enables interrupts on GPIO2
18	DIS_DEEP_SLEEP	R/W	0h	Disables blocks getting powered down in Deep Sleep phase
17-11	0	R/W	0h	Must write 0
10	SDOUT_TRISTATE	R/W	0h	Static SDOUT Tristate Mode. Set to '1' to make SDOUT tristated
9-0	0	R/W	0h	Must write 0

7.6.3.1.13 READ_FLAG1: Register 30h (address = 30h)**Figure 7-120. Register 30h**

23	22	21	20	19	18	17	16
x	x	x	x	FLAG_LDO_ST ATE	x	x	x
R-xh	R-xh	R-xh	R-xh	R-0h	R-xh	R-xh	R-xh
15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
7	6	5	4	3	2	1	0
FLAG_UCD_LE D8	FLAG_UCD_LE D7	FLAG_UCD_LE D6	FLAG_UCD_LE D5	FLAG_UCD_LE D4	FLAG_UCD_LE D3	FLAG_UCD_LE D2	FLAG_UCD_LE D1
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh

Table 7-101. Register 30h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R	xh	Read only register
19	FLAG_LDO_STATE	R	xh	Read out state of EN_LDO_BYP. 0 = LDO enabled 1 = LDO bypassed
18-8	0	R	xh	Read only register
7	FLAG_UCD_LED8	R	xh	Undercurrent detect flag for LED8
6	FLAG_UCD_LED7	R	xh	Undercurrent detect flag for LED7
5	FLAG_UCD_LED6	R	xh	Undercurrent detect flag for LED6
4	FLAG_UCD_LED5	R	xh	Undercurrent detect flag for LED5
3	FLAG_UCD_LED4	R	xh	Undercurrent detect flag for LED4
2	FLAG_UCD_LED3	R	xh	Undercurrent detect flag for LED3
1	FLAG_UCD_LED2	R	xh	Undercurrent detect flag for LED2
0	FLAG_UCD_LED1	R	xh	Undercurrent detect flag for LED1

7.6.3.1.14 CONTROL8: Register 31h (address = 31h)**Figure 7-121. Register 31h**

23	22	21	20	19	18	17	16
0	0	0	0	CONNECT_BG_TO_PIN	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	EN_GPIO2_IN	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-102. Register 31h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R/W	0h	Must write 0
19	CONNECT_BG_TO_PIN	R/W	0h	Set CONNECT_BG_TO_PIN = 1 in ECG or Mixed signal acquisition mode and set to same value as DIS_DEEP_SLEEP in PPG only mode.
18-15	0	R/W	0h	Must write 0
14	EN_GPIO2_IN	R/W	0h	Configures GPIO2 as an input pin
13-0	0	R/W	0h	Must write 0

7.6.3.1.15 CONTROL9: Register 42h (address = 42h)**Figure 7-122. Register 42h**

23	22	21	20	19	18	17	16
0	0	0	0	INT_MUX_GPI_O2_2	0	0	INT_MUX_ADC_RDY_2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0			REG_WM_FIFO			
R/W-0h	R/W-0h			R/W-0h			
7	6	5	4	3	2	1	0
REG_WM_FIFO		INT_MUX_ADC_RDY_1		0	0	0	0
R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-103. Register 42h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R/W	0h	Must write 0
19	INT_MUX_GPIO2_2	R/W	0h	Reserved function. Set to 0.
18-17	0	R/W	0h	Must write 0
16	INT_MUX_ADC_RDY_2	R/W	0h	Reserved function. Set to 0.
15-14	0	R/W	0h	Must write 0
13-6	REG_WM_FIFO	R/W	0h	Watermark level as set by (REG_WM_FIFO+1) determines difference between Write and Read pointer at which FIFO_RDY interrupt is generated.
5-4	INT_MUX_RDY_RDY_1	R/W	0h	Selection for interrupt multiplexing on the ADC_RDY pin.
3-0	0	R/W	0h	Must write 0

7.6.3.1.16 CONTROL10: Register 4Bh (address = 4Bh)**Figure 7-123. Register 4Bh**

23	22	21	20	19	18	17	16
0	EN_128K_CLK_OUT	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	DIS_BUF_PDN_ON_ADC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
ADC_RDY_OP_EN_DRAIN	0	0	0	CLKBUF_TRISTATE	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-104. Register 4Bh Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22	EN_128K_CLKOUT	R/W	0h	Enables the 128-kHz oscillator output clock to come out on GPIO2 pin.
21-9	0	R/W	0h	Must write 0
8	DIS_BUF_PDN_ON_ADC	R/W	0h	Disables powering down the ADC buffer after the active time slots of the PRF cycle. Set to '1' when operating in the Mixed acquisition and ECG modes to avoid performance degradation in the first time slot (TS0).
7	ADC_RDY_OPEN_DRAIN	R/W	0h	Setting this bit to '1' makes the ADC_RDY open drain output.
6-4	0	W	0h	Must write 0
3	CLKBUF_TRISTATE	R/W	0h	Tri-state clock input buffer. Set to '1' when using Internal Oscillator mode
2-0	0	W	0h	Must write 0

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7.6.3.1.17 CONTROL11: Register 4Eh (address = 4Eh)**Figure 7-124. Register 4Eh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CONNECT_ECG_INP	CONNECT_ECG_INM	SHORT_ECG_INP_RLD	SHORT_ECG_INM_RLD	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	EN_ECG_SIG_CHAIN	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-105. Register 4Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	AC_LEADOFF_FREQ	R/W	0h	Must write 0
15	CONNECT_ECG_INP	R/W	0h	Connect the ECG input pin ECG_INP to the ECG receiver chain
14	CONNECT_ECG_INM	R/W	0h	Connect the ECG input pin ECG_INM to the ECG receiver chain
13	SHORT_ECG_INP_RLD	R/W	0h	Short ECG input pin ECG_INP to RLD through a switch
12	SHORT_ECG_INM_RLD	R/W	0h	Short ECG input pin ECG_INM to RLD through a switch
11-3	0	R/W	0h	Must write 0
2	EN_ECG_SIG_CHAIN	R/W	0h	Enable ECG signal chain and power up the INA
1-0	0	R/W	0h	Must write 0

7.6.3.1.18 CONTROL12: Register 50h (address = 50h)**Figure 7-125. Register 50h**

23	22	21	20	19	18	17	16
0	0	0		ECG_INA_GAIN		0	SINGLE_SHOT_MODE_PPG
W-0h	W-0h	W-0h		R/W-0h		W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	PDN_OSC_IN_DEEP_SLEEP_PPG	EN_LED_UCD	0		PROG_VTHR_UCD		0
W-0h	R/W-0h	R/W-0h	W-0h		R/W-0h		W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	CONFIG_RLD_AS_UGB	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h

Table 7-106. Register 50h Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	W	0h	Must write 0
20-18	ECG_INA_GAIN	R/W	0h	INA gain control
17	0	R/W	0h	Must write 0
16	SINGLE_SHOT_MODE_PPG	R/W	0h	Set to '1' to enable single shot acquisition mode. When set to '1' along with the EN_MIXED_CLK_MODE_PPG bit, enables the Mixed clock mode.
15	0	R/W	0h	Must write 0
14	PDN_OSC_IN_DEEP_SLEEP_PPG	R/W	0h	Powers down the 128-kHz oscillator when the device enters the Deep sleep window. Use in conjunction with the Single shot acquisition mode and Mixed clock mode.
13	EN_LED_UCD	R/W	0h	Enable the LED Under-current detection (UCD) circuit
12	0	W	0h	Must write 0
11-9	PROG_VTHR_UCD	R/W	0h	Programs the threshold voltage against which the voltages on the TX pin(s) are compared during the LED ON phase by the LED Under-current detect circuit
8-3	0	W	0h	Must write 0
2	CONFIG_RLD_AS_UGB	R/W	0h	Configures RLD amplifier as a unity gain buffer that drives a fixed output voltage on the RLD pin
1-0	0	W	0h	Must write 0

7.6.3.1.19 CONTROL13: Register 51h (address = 51h)**Figure 7-126. Register 51h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	AUTO_MASK_FIFO_RDY	MASK_FIFO_RDY	FORCE_FIFO_OFFSET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
FIFO_OFFSET_TO_FORCE							
R/W-0h							

Table 7-107. Register 51h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Must write 0
10	AUTO_MASK_FIFO_RDY	R/W	0h	Set to '1' to prevent the occurrence of repetitive FIFO_RDY interrupts when the pointer difference has exceeded the watermark level.
9	MASK_FIFO_RDY	R/W	0h	Masks the FIFO_RDY interrupt generation when operating in the Watermark FIFO mode.
8	FORCE_FIFO_OFFSET	R/W	0h	Force the FIFO read pointer with respect to the write pointer. The offset to force is set by FIFO_OFFSET_TO_FORCE.
7-0	FIFO_OFFSET_TO_FORCE	R/W	0h	Offset of the read pointer relative to the write pointer. Use in conjunction with FORCE_FIFO_OFFSET set to 1.

7.6.3.1.20 CONTROL14: Register 62h (address = 62h)**Figure 7-127. Register 62h**

23	22	21	20	19	18	17	16
0	0	0		PROG_VCM_RLD		0	0
W-0h	W-0h	W-0h		R/W-0h		W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 7-108. Register 62h Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	W	0h	Must write 0
20-18	PROG_VCM_RLD	R/W	0h	Programs the output voltage of the RLD buffer
17-0	0	W	0h	Must write 0

7.6.3.1.21 CONTROL15: Register 6Ch (address = 6Ch)**Figure 7-128. Register 6Ch**

23	22	21	20	19	18	17	16
0	0	0	0	0	DIS_CHOP_INA	PROG_INA_SAT_THR_H	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PROG_INA_SAT_THR_L	0	EN_INA_OUT_COMP		0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-109. Register 6Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-19	0	W	0h	Must write 0
18	DIS_CHOP_INA	R/W	0h	Mode to disable chopping in the ECG INA – use while doing Impedance measurement using the ECG signal chain
17-16	PROG_INA_SAT_THR_H	R/W	0h	Program high threshold for Analog saturation detection at INA output
15-14	PROG_INA_SAT_THR_L	R/W	0h	Program low threshold for Analog saturation detection at INA output
13	0	W	0h	Must write 0
12	EN_INA_OUT_COMP	R/W	0h	Enable comparators for Analog saturation detection at INA output
11-0	0	W	0h	Must write 0

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7.6.3.1.22 READ_POINTER: Register 6Dh (address = 6Dh)**Figure 7-129. Register 6Dh**

23	22	21	20	19	18	17	16
x	x	x	x	x	x	x	x
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
7	6	5	4	3	2	1	0
REG_POINTER_DIFF							
R-xh							

Table 7-110. Register 6Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-8	x	R	xh	Read only (Do not care)
7-0	REG_POINTER_DIFF	R	xh	The instantaneous value of the (Write pointer minus Read pointer) minus 1 is stored in REG_POINTER_DIFF. When a FIFO_RDY interrupt is issued, the value stored in REG_POINTER_DIFF is expected to be equal to the value programmed in REG_WF_FIFO.

7.6.3.1.23 CONTROL16: Register 72h (address = 72h)**Figure 7-130. Register 72h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	IFS_AMB_OFFSETDAC_TIA2		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

Table 7-111. Register 72h Field Descriptions

Bit	Field	Type	Reset	Description
23-3	0	R/W	0h	Must write 0
2-0	IFS_AMB_OFFSETDAC_TIA2	R/W	0h	Full-scale current control for Ambient Offset DAC of TIA2

7.6.3.1.24 CONTROL17: Register 73h (address = 73h)**Figure 7-131. Register 73h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	RF_ANA_AACM_START_TIA2				PDN_TIA1_STA TIC	0
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	RF_ANA_AACM_START_TIA1				0	0
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h

Table 7-112. Register 73h Field Descriptions

Bit	Field	Type	Reset	Description
23-14	0	R/W	0h	Must write 0
13-10	RF_ANA_AACM_START_TIA2	R/W	0h	Rf control code during start of ANA_ACQ_TIA2
9	PDN_TIA1_STATIC	R/W	0h	When operating in ECG-only mode, set this bit to '1' to power down the TIA
8-6	0	R/W	0h	Must write 0
5-2	RF_ANA_AACM_START_TIA1	R/W	0h	Rf control code during start of ANA_ACQ_TIA1
1-0	0	R/W	0h	Must write 0

7.6.3.1.25 CONTROL18: Register 74h (address = 74h)**Figure 7-132. Register 74h**

23	22	21	20	19	18	17	16
0	EN_SYNC_INT_OSC	EN_128K_CLK_CALIB_1	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
IFS_LED_OFF_DAC_TIA2	IFS_LED_OFF_DAC_TIA1	0	0	0	0	PDN_BG_IN_D_EEP_SLEEP	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-113. Register 74h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22	EN_SYNC_INT_OSC	R/W	0h	Set to '1' as part of enabling Synchronous Mixed clock mode
21	EN_128K_CLK_CALIB_1	R/W	0h	Enable calibration routine for 128 kHz oscillator using external RTC clock
20-8	0	R/W	0h	Must write 0
7	IFS_LED_OFFDAC_TIA2	R/W	0h	Full scale current programmability for LED Offset DAC of TIA2
6	IFS_LED_OFFDAC_TIA1	R/W	0h	Full scale current programmability for LED Offset DAC of TIA1
5-2	0	R/W	0h	Must write 0
1	PDN_BG_IN_DEEP_SLEEP	R/W	0h	Powers down the Bandgap when device is in Deep Sleep phase as well as during Software power-down mode This bit should be set to '0' when operating with the LDOs enabled
0	0	R/W	0h	Must write 0

7.6.3.1.26 CONTROL19: Register 75h (address = 75h)**Figure 7-133. Register 75h**

23	22	21	20	19	18	17	16
AC_LEAD_DET_CLK_PHASE	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	DIS_LPF_ECG
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DIS_CHOP_LP_F_ECG	0	TM_BOOST_SEL	0	0	0	BYP_LPF_INA	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-114. Register 75h Field Descriptions

Bit	Field	Type	Reset	Description
23	AC_LEAD_DET_CLK_PHASE	R/W	0h	Change AC lead polarity for cancellation of DC drift in AC lead strength estimation. Not available in Rev1 Silicon
22-9	0	R/W	0h	Must write 0
8	DIS_LPF_ECG	R/W	0h	Disables LPF – set to 1 for Impedance measurement
7	DIS_CHOP_LPF_ECG	R/W	0h	Disables chopping associated with LPF – set to 1 for Impedance measurement
6	0	R/W	0h	Must write 0
5	TM_BOOST_SEL	R/W	0h	In LDO enable mode set TM_BOOST_SEL = 1 for RX_SUP < 2.3 V
4-2	0	R/W	0h	Must write 0
1	BYP_LPF_INA	R/W	0h	Bypasses LPF – set to 1 for Impedance measurement
0	FILTER_BW_FINE_SET1	R/W	0h	Bandwidth setting control for Filter bandwidth in Fine settling phase (Set 1)

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7.6.3.1.27 FILT_BW_SET1: Register 78h (address = 78h)**Figure 7-134. Register 78h**

23	22	21	20	19	18	17	16
OVERRIDE_B_W_PRE	0	0	0	0	0	0	FILTER_BW_PRE_SET1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
FILTER_BW_PRE_SET1				0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0		FILTER_BW_FINE_SET1			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

Table 7-115. Register 78h Field Descriptions

Bit	Field	Type	Reset	Description
23	OVERRIDE_BW_PRE	R/W	0h	Override bit – set to '1' to program pre-charge filter BW (Set 1) using FILTER_BW_PRE_SET1
22-17	0	R/W	0h	Must write 0
16-12	FILTER_BW_PRE_SET1	R/W	0h	Bandwidth setting control for Filter bandwidth in pre-charge phase (Set 1)
11-5	0	R/W	0h	Must write 0
4-0	FILTER_BW_FINE_SET1	R/W	0h	Bandwidth setting control for Filter bandwidth in Fine settling phase (Set 1)

7.6.3.1.28 FILT_BW_SET2: Register 79h (address = 79h)**Figure 7-135. Register 79h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	FILTER_BW_PRE_SET2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
FILTER_BW_PRE_SET2				0	0	0	0
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0		FILTER_BW_FINE_SET2			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

Table 7-116. Register 79h Field Descriptions

Bit	Field	Type	Reset	Description
23-17	0	R/W	0h	Must write 0
16-12	FILTER_BW_PRE_SET2	R/W	0h	Bandwidth setting control for Filter bandwidth in pre-charge phase (Set 2)
11-5	0	R/W	0h	Must write 0
4-0	FILTER_BW_FINE_SET2	R/W	0h	Bandwidth setting control for Filter bandwidth in Fine settling phase (Set 2)

7.6.3.1.29 Register 7Ch (address = 7Ch)**Figure 7-136. Register 7Ch**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	THR_DRE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
THR_DRE				0	ENABLE_DRE		
R/W-0h				R/W-0h	R/W-0h		

Table 7-117. Register 7Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-10	0	R/W	0h	Must write 0
9-4	THR_DRE	R/W	0h	DRE threshold
3	0	R/W	0h	Must write 0
2-0	ENABLE_DRE	R/W	0h	000 = DRE disabled 111 = Enable DRE

7.6.3.1.30 Register 7Dh (address = 7Dh)**Figure 7-137. Register 7Dh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	REG_SCALE_DRE_LOOP4			0	REG_SCALE_DRE_LOOP3		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
0	REG_SCALE_DRE_LOOP2			0	REG_SCALE_DRE_LOOP1		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 7-118. Register 7Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-15	0	R/W	0h	Must write 0
14-12	REG_SCALE_DRE_LOOP4	R/W	0h	DRE extension factor for Loop 4
11	0	R/W	0h	Must write 0
10-8	REG_SCALE_DRE_LOOP3	R/W	0h	DRE extension factor for Loop 3
7	0	R/W	0h	Must write 0
6-4	REG_SCALE_DRE_LOOP2	R/W	0h	DRE extension factor for Loop 2
3	0	R/W	0h	Must write 0
2-0	REG_SCALE_DRE_LOOP1	R/W	0h	DRE extension factor for Loop 1

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7.6.3.1.31 THR_CODE1: Register 80h (address = 80h)**Figure 7-138. Register 80h**

23	22	21	20	19	18	17	16
HIGH_THRESHOLD_CODE1							
R/W-0h							
15	14	13	12	11	10	9	8
HIGH_THRESHOLD_CODE1				LOW_THRESHOLD_CODE1			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
LOW_THRESHOLD_CODE1							
R/W-0h							

Table 7-119. Register 80h Field Descriptions

Bit	Field	Type	Reset	Description
23-12	HIGH_THRESHOLD_CODE1	R/W	0h	High threshold code used for comparison in Threshold detect mode
11-0	LOW_THRESHOLD_CODE1	R/W	0h	Low threshold code used for comparison in Threshold detect mode

7.6.3.1.32 THR_CODE2: Register 81h (address = 81h)**Figure 7-139. Register 81h**

23	22	21	20	19	18	17	16
HIGH_THRESHOLD_CODE2							
R/W-0h							
15	14	13	12	11	10	9	8
HIGH_THRESHOLD_CODE2				LOW_THRESHOLD_CODE2			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
LOW_THRESHOLD_CODE2							
R/W-0h							

Table 7-120. Register 81h Field Descriptions

Bit	Field	Type	Reset	Description
23-12	HIGH_THRESHOLD_CODE2	R/W	0h	High threshold code used for comparison in Threshold detect mode
11-0	LOW_THRESHOLD_CODE2	R/W	0h	Low threshold code used for comparison in Threshold detect mode

7.6.3.1.33 CONTROL20: Register 88h (address = 88h)**Figure 7-140. Register 88h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	EARLY_SAMP_FALL	0	0	0	EN_PHASE_IN_T_GPIO
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	MODE_EN_FR AME_SYNC	0					REG_NUMPHASE_PPG
R/W-0h	R/W-0h	R/W-0h					R/W-0h

Table 7-121. Register 88h Field Descriptions

Bit	Field	Type	Reset	Description
23-13	0	R/W	0h	Must write 0
12	EARLY_SAMP_FALL	R/W	0h	Advances fall of SAMP relative to fall of LED_ON by 1 CLK_TE cycle
11-9	0	R/W	0h	Must write 0
8	EN_PHASE_INT_GPIO	R/W	0h	Enable per-phase interrupt on GPIO2 pin
7	0	R/W	0h	Must write 0
6	MODE_EN_FRAME_SYNC	R/W	0h	Replaces MSB (D23) of each data going into the FIFO with a frame sync bit. Frame sync bit gets set to '1' for the first FIFO data of every PRF cycle.
5	0	R/W	0h	Must write 0
4-0	REG_NUMPHASE_PPG	R/W	0h	Sets the number of active signal phases as (REG_NUMPHASE_PPG + 1)

7.6.3.1.34 TIMING1: Register 8Ah (address = 8Ah)**Figure 7-141. Register 8Ah**

23	22	21	20	19	18	17	16
0	0	0		REG_TACTIVE_PWRUP			
R/W-0h	R/W-0h	R/W-0h		R/W-26h			
15	14	13	12	11	10	9	8
		REG_TACTIVE_PWRUP		0	0	0	REG_TDEEP_SLEEP_PWRUP_P
			R/W-26h	R/W-0h	R/W-0h	R/W-0h	R/W-16h
7	6	5	4	3	2	1	0
			REG_TDEEP_SLEEP_PWRUP				
				R/W-16h			

Table 7-122. Register 8Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	R/W	0h	Must write 0
20-12	REG_TACTIVE_PWRUP	R/W	26h	Count that determines start of Active phase to start of Window #0
11-9	0	R/W	0h	Must write 0
8-0	REG_TDEEP_SLEEP_PWRUP	R/W	16h	Count that determines start of PRF cycle to start of Active phase

7.6.3.1.35 TIMING2: Register 8Bh (address = 8Bh)**Figure 7-142. Register 8Bh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0		REG_TSEP_CONV_LED		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-1h		
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-123. Register 8Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-12	0	R/W	0h	Must write 0
11-8	REG_TSEP_CONV_LED	R/W	1h	Count that determines separation between end of CONV of previous phase and start of LED ON signal for the current phase when these signals are staggered (non-overlapping).
7-0	0	R/W	0h	Must write 0

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7.6.3.1.36 TIMING3: Register 8Ch (address = 8Ch)**Figure 7-143. Register 8Ch**

23	22	21	20	19	18	17	16
0	0	REG_TSEP		0	0	REG_TLED_SAMP	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
	REG_TLED_SAMP			0	0	0	0
	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-124. Register 8Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	Must write 0
21-20	REG_TSEP	R/W	0h	Count that determines separation between successive phase windows
19-18	0	R/W	0h	Must write 0
17-12	REG_TLED_SAMP	R/W	0h	Count that determines Start of LED ON to start of SAMP
11-0	0	R/W	0h	Must write 0

7.6.3.1.37 TIMING4: Register 8Dh (address = 8Dh)**Figure 7-144. Register 8Dh**

23	22	21	20	19	18	17	16
0	0	0	0		REG_TW_DATA_RDY		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
				REG_TACTIVE_DATA_RDY			
				R/W-3h			

Table 7-125. Register 8Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R/W	0h	Must write 0
19-16	REG_TW_DATA_RDY	R/W	0h	Count that determines width of the DATA_RDY pulse
15-8	0	R/W	0h	Must write 0
7-0	REG_TACTIVE_DATA_RDY	R/W	3h	Count that determines end of Active phase to start of DATA_RDY pulse

7.6.3.1.38 TIMING5: Register 8Eh (address = 8Eh)**Figure 7-145. Register 8Eh**

23	22	21	20	19	18	17	16
0	0	0		REG_TDEEP_SLEEP_PWDN			
R/W-0h	R/W-0h	R/W-0h		R/W-5h			
15	14	13	12	11	10	9	8
		REG_TDEEP_SLEEP_PWDN		0	0	0	REG_TACTIVE_PWDN
			R/W-5h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
			REG_TACTIVE_PWDN				
				R/W-1h			

Table 7-126. Register 8Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	R/W	0h	Must write 0
20-12	REG_TDEEP_SLEEP_PWDN	R/W	5h	Count that determines DATA_RDY fall to start of Deep sleep phase
11-9	0	R/W	0h	Must write 0
8-0	REG_TACTIVE_PWDN	R/W	1h	Count that determines end of the last phase window to end of Active phase

7.6.3.1.39 TIMING6: Register 8Fh (address = 8Fh)**Figure 7-146. Register 8Fh**

23	22	21	20	19	18	17	16
0	MASK_REVERSE	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0		EXT_CLK_FREQ	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

Table 7-127. Register 8Fh Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22	MASK_REVERSE	R/W	0h	'0': The first PRF cycle of the repeating masking sequence is the unmasked phase '1': The last PRF cycle of the repeating masking sequence is the unmasked phase
21-3	0	R/W	0h	Must write 0
2-0	EXT_CLK_FREQ	R/W	0h	Specify frequency of external clock while operating in external clock mode. Use in conjunction with CLK_DIV_CLK if operating at an external clock frequency of 256 kHz or 512 kHz.

7.6.3.1.40 CONTROL21: Register 92h (address = 03h)**Figure 7-147. Register 92h**

23	22	21	20	19	18	17	16
0	0	0	0	0		REG_STEP_COUNT	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
		REG_STEP_COUNT		0	0	0	EN_INT_IN_SINGLE_SHOT
			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-128. Register 92h Field Descriptions

Bit	Field	Type	Reset	Description
23-19	0	R/W	0h	Must write 0
18-12	REG_STEP_COUNT	R/W	0h	Step increment in PRF counter while operating in Mixed clock mode
11-9	0	R/W	0h	Must write 0
8	EN_INT_IN_SINGLE_SHOT	R/W	0h	Additional control needed for the generation of programmable interrupts when operating in the Single shot acquisition mode.
7-0	0	R/W	0h	Must write 0

7.6.3.1.41 CONTROL22: Register 93h (address = 93h)**Figure 7-148. Register 93h**

23	22	21	20	19	18	17	16
0	0	0		CHANNEL_OFFSET_AACM_TIA1			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
15	14	13	12	11	10	9	8
		CHANNEL_OFFSET_AACM_TIA1		R/W-0h			
				R/W-0h			
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-129. Register 93h Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	R/W	0h	Must write 0
20-8	CHANNEL_OFFSET_AACM_TIA1	R/W	R/W	Calibration word denoting channel offset to be written as part of AACM calibration – this word corresponds to the channel offset of TIA1
7-0	0	R/W	0h	Must write 0

7.6.3.1.42 CONTROL23: Register 94h (address = 94h)**Figure 7-149. Register 94h**

23	22	21	20	19	18	17	16
0	0	0		CHANNEL_OFFSET_AACM_TIA2			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
15	14	13	12	11	10	9	8
		CHANNEL_OFFSET_AACM_TIA2		R/W-0h			
				R/W-0h			
7	6	5	4	3	2	1	0
		REG_TW_FILTER_PRE		R/W-0h			
				R/W-0h			

Table 7-130. Register 94h Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	R/W	0h	Must write 0
20-8	CHANNEL_OFFSET_AACM_TIA2	R/W	R/W	Calibration word denoting channel offset to be written as part of AACM calibration – this word corresponds to the channel offset of TIA2
7-0	REG_TW_FILTER_PRE	R/W	0h	Register control to program Filter Pre-charge phase width

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7.6.3.1.43 CONTROL24: Register 95h (address = 95h)**Figure 7-150. Register 95h**

23	22	21	20	19	18	17	16
EMBED_ANA_AACM_IN_FIFO	0	TSEP_ANA_ACQ_LED_OVERRIDE	TW_ANA_ACQ_OVERRIDE	REG_TSEP_ANA_ACQ_LED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
15	14	13	12	11	10	9	8
		REG_TW_ANA_ACQ		REG_DELAY_ANA_ACQ			
		R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
		RF_ANA_AACM_END		0	0	0	0
		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-131. Register 95h Field Descriptions

Bit	Field	Type	Reset	Description
23	EMBED_ANA_AACM_IN_FIFO	R/W	0h	Using this diagnostic mode, the Ambient Offset DAC code determined by the AACM loop in an Analog AACM phase marked with UPDATE_BASELINE = '1' can be embedded into the 9 LSB of the corresponding FIFO word.
22	0	R/W	0h	Must write 0
21	TSEP_ANA_ACQ_LED_OVERRIDE	R/W	0h	Set to '1' to override $t_{\text{SEP_ANA_ACQ_LED}}$ using the register control REG_TSEP_ANA_ACQ_LED
20	TW_ANA_ACQ_OVERRIDE	R/W	0h	Set to '1' to override $t_{\text{W_ANA_ACQ}}$ using the register control REG_TW_ANA_ACQ.
19-16	REG_TSEP_ANA_ACQ_LED	R/W	0h	Register control for $t_{\text{SEP_ANA_ACQ_LED}}$. Used to override default value when TSEP_ANA_ACQ_LED_OVERRIDE is set to '1'.
15-12	REG_TW_ANA_ACQ	R/W	0h	Register control for $t_{\text{W_ANA_ACQ}}$. Used to override default value when TW_ANA_ACQ_OVERRIDE is set to '1'
11-8	REG_DELAY_ANA_ACQ	R/W	0h	Register control for $t_{\text{DELAY_ANA_ACQ}}$.
7-4	RF_ANA_AACM_END	R/W	5h	Rf control code during end of ANA_ACQ_TIA1 and ANA_ACQ_TIA2
3-0	0	R/W	0h	Must write 0

7.6.3.1.44 DEC1TO4_1: Register 96h (address = 96h)**Figure 7-151. Register 96h**

23	22	21	20	19	18	17	16
0	0	0	0	PPG_DEC4_TIA_SEL	PPG_DEC3_TIA_SEL	PPG_DEC2_TIA_SEL	PPG_DEC1_TIA_SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	REG_PPG_DEC4_FACTOR			0	REG_PPG_DEC3_FACTOR		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
0	REG_PPG_DEC2_FACTOR			0	REG_PPG_DEC1_FACTOR		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 7-132. Register 96h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R/W	0h	Must write 0
19	PPG_DEC4_TIA_SEL	R/W	0h	Select the decimation filter 4 association with TIA. 0 – TIA1, 1 – TIA2
18	PPG_DEC3_TIA_SEL	R/W	0h	Select the decimation filter 3 association with TIA. 0 – TIA1, 1 – TIA2
17	PPG_DEC2_TIA_SEL	R/W	0h	Select the decimation filter 2 association with TIA. 0 – TIA1, 1 – TIA2
16	PPG_DEC1_TIA_SEL	R/W	0h	Select the decimation filter 1 association with TIA. 0 – TIA1, 1 – TIA2
14-12	REG_PPG_DEC4_FACTOR	R/W	0h	Decimation factor control for PPG Decimation filter 4
11	0	R/W	0h	Must write 0
10-8	REG_PPG_DEC3_FACTOR	R/W	0h	Decimation factor control for PPG Decimation filter 3
7	0	R/W	0h	Must write 0
6-4	REG_PPG_DEC2_FACTOR	R/W	0h	Decimation factor control for PPG Decimation filter 2
3	0	R/W	0h	Must write 0
2-0	REG_PPG_DEC1_FACTOR	R/W	0h	Decimation factor control for PPG Decimation filter 1

7.6.3.1.45 DEC1TO4_2: Register 97h (address = 97h)**Figure 7-152. Register 97h**

23	22	21	20	19	18	17	16
EN_PPG_DEC4		REG_NUMPHASE_PPG_DEC4			EN_PPG_DEC3	REG_NUMPHASE_PPG_DEC3	
R/W-0h		R/W-0h			R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
		REG_NUMPHASE_PPG_DEC3		EN_PPG_DEC2		REG_NUMPHASE_PPG_DEC2	
		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
REG_NUMPHASE_PPG_DEC2	EN_PPG_DEC1			REG_NUMPHASE_PPG_DEC1			
R/W-0h		R/W-0h		R/W-0h			

Table 7-133. Register 97h Field Descriptions

Bit	Field	Type	Reset	Description
23	EN_PPG_DEC4	R/W	0h	Enable PPG Decimation filter 4
22-18	REG_NUMPHASE_PPG_DEC4	R/W	0h	PPG Phase number to which PPG Decimation filter #4 needs to be assigned is set as (REG_NUMPHASE_PPG_DEC4+1)
17	EN_PPG_DEC3	R/W	0h	Enable PPG Decimation filter 3
16-12	REG_NUMPHASE_PPG_DEC3	R/W	0h	PPG Phase number to which PPG Decimation filter #3 needs to be assigned is set as (REG_NUMPHASE_PPG_DEC3+1)
11	EN_PPG_DEC2	R/W	0h	Enable PPG Decimation filter 2
10-6	REG_NUMPHASE_PPG_DEC2	R/W	0h	PPG Phase number to which PPG Decimation filter #2 needs to be assigned is set as (REG_NUMPHASE_PPG_DEC2+1)
5	EN_PPG_DEC1	R/W	0h	Enable PPG Decimation filter 1
4-0	REG_NUMPHASE_PPG_DEC1	R/W	0h	PPG Phase number to which PPG Decimation filter #1 needs to be assigned is set as (REG_NUMPHASE_PPG_DEC1+1)

7.6.3.1.46 LOOP1_AACM1: Register 98h (address = 98h)**Figure 7-153. Register 98h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	FREEZE_AAC M_LOOP1	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-134. Register 98h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Must write 0
10	FREEZE_AACM_LOOP1	R/W	0h	Freeze AACM loop 1 and prevent further update of Offset DAC
9-0	0	R/W	0h	Must write 0

7.6.3.1.47 LOOP1_AACM2: Register 99h (address = 99h)**Figure 7-154. Register 99h**

23	22	21	20	19	18	17	16
0	RECONV_THRESH_AACM_LOOP1			0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0		CALIB_AACM_LOOP1		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
			CALIB_AACM_LOOP1				
			R/W-0h				

Table 7-135. Register 99h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22-20	RECONV_THRESH_AACM_LOOP1	R/W	0h	Re-convergence threshold for Digital AACM Loop 1
19-12	0	R/W	0h	Must write 0
11-0	CALIB_AACM_LOOP1	R/W	0h	Calibration word for Digital AACM Loop 1.

7.6.3.1.48 LOOP1_AACM3: Register 9Ah (address = 9Ah)**Figure 7-155. Register 9Ah**

23	22	21	20	19	18	17	16
x	x	x	x	x	x	x	x
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	POL_OFFDAC_AACM_READ_LOOP1
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
7	6	5	4	3	2	1	0
IOFFDAC_AACM_READ_LOOP1							
R-xh							

Table 7-136. Register 9Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-9	x	R	xh	
8	POL_OFFDAC_AACM_READ_LOOP1	R	xh	Readout of AACM output for Loop 1 (Polarity of Offset DAC controlled by the loop)
7-0	IOFFDAC_AACM_READ_LOOP1	R	xh	Readout of AACM output for Loop 1 (Amplitude of Offset DAC controlled by the loop)

7.6.3.1.49 LOOP2_AACM1: Register 9Ch (address = 9Ch)**Figure 7-156. Register 9Ch**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	FREEZE_AACM_LOOP2	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-137. Register 9Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Must write 0
10	FREEZE_AACM_LOOP2	R/W	0h	Freeze AACM loop 2 and prevent further update of Offset DAC
9-0	0	R/W	0h	Must write 0

7.6.3.1.50 LOOP2_AACM1: Register 9Dh (address = 9Dh)**Figure 7-157. Register 9Dh**

23	22	21	20	19	18	17	16
0		RECONV_THRESH_AACM_LOOP2		0	0	0	0
R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0		CALIB_AACM_LOOP2		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
				CALIB_AACM_LOOP2			
				R/W-0h			

Table 7-138. Register 9Dh Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22-20	RECONV_THRESH_AACM_LOOP2	R/W	0h	Re-convergence threshold for Digital AACM Loop 2
19-12	0	R/W	0h	Must write 0
11-0	CALIB_AACM_LOOP2	R/W	0h	Calibration word for Digital AACM Loop 2

7.6.3.1.51 LOOP2_AACM3: Register 9Eh (address = 9Eh)**Figure 7-158. Register 9Eh**

23	22	21	20	19	18	17	16
x	x	x	x	x	x	x	x
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	POL_OFFDAC_AACM_READ_LOOP2
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
7	6	5	4	3	2	1	0
				IOFFDAC_AACM_READ_LOOP2			
				R-xh			

Table 7-139. Register 9Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-9	x	R	xh	
8	POL_OFFDAC_AACM_READ_LOOP2	R	xh	Readout of AACM output for Loop 2 (Polarity of Offset DAC controlled by the loop)
7-0	IOFFDAC_AACM_READ_LOOP2	R	xh	Readout of AACM output for Loop 2 (Amplitude of Offset DAC controlled by the loop)

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7.6.3.1.52 LOOP3_AACM1: Register A0h (address = A0h)**Figure 7-159. Register A0h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	FREEZE_AAC M_LOOP3	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-140. Register A0h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Must write 0
10	FREEZE_AACM_LOOP3	R/W	0h	Freeze AACM loop 3 and prevent further update of Offset DAC
9-0	0	R/W	0h	Must write 0

7.6.3.1.53 LOOP3_AACM2: Register A1h (address = A1h)**Figure 7-160. Register A1h**

23	22	21	20	19	18	17	16
0	RECONV_THRESH_AACM_LOOP3			0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0		CALIB_AACM_LOOP3		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
			CALIB_AACM_LOOP3				
			R/W-0h				

Table 7-141. Register A1h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22-20	RECONV_THRESH_AACM_LOOP3	R/W	0h	Re-convergence threshold for Digital AACM Loop 3
19-12	0	R/W	0h	Must write 0
11-0	CALIB_AACM_LOOP3	R/W	0h	Calibration word for Digital AACM Loop 3

7.6.3.1.54 LOOP3_AACM3: Register A2h (address = A2h)**Figure 7-161. Register A2h**

23	22	21	20	19	18	17	16
x	x	x	x	x	x	x	x
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	POL_OFFDAC_AACM_READ_LOOP3
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
7	6	5	4	3	2	1	0
IOFFDAC_AACM_READ_LOOP3							
R-xh							

Table 7-142. Register A2h Field Descriptions

Bit	Field	Type	Reset	Description
23-9	0	R	xh	Must write 0
8	POL_OFFDAC_AACM_READ_LOOP3	R	xh	Readout of AACM output for Loop 3 (Polarity of Offset DAC controlled by the loop)
7-0	IOFFDAC_AACM_READ_LOOP3	R	xh	Readout of AACM output for Loop 3 (Amplitude of Offset DAC controlled by the loop)

7.6.3.1.55 LOOP4_AACM1: Register A4h (address = A4h)**Figure 7-162. Register A4h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	FREEZE_AACM_LOOP4	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-143. Register A4h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Must write 0
10	FREEZE_AACM_LOOP4	R/W	0h	Freeze AACM loop 4 and prevent further update of Offset DAC
9-0	0	R/W	0h	Must write 0

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7.6.3.1.56 LOOP4_AACM2: Register A5h (address = A5h)**Figure 7-163. Register A5h**

23	22	21	20	19	18	17	16
0		RECONV_THR_AACM_LOOP4		0	0	0	0
R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0		CALIB_AACM_LOOP4		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
			CALIB_AACM_LOOP4				
				R/W-0h			

Table 7-144. Register A5h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22-20	RECONV_THRESH_AACM_LOOP4	R/W	0h	Re-convergence threshold for Digital AACM Loop 4
19-12	0	R/W	0h	Must write 0
11-0	CALIB_AACM_LOOP4	R/W	0h	Calibration word for Digital AACM Loop 4.

7.6.3.1.57 LOOP4_AACM3: Register A6h (address = A6h)**Figure 7-164. Register A6h**

23	22	21	20	19	18	17	16
x	x	x	x	x	x	x	x
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	POL_OFFSETDAC_AACM_READ_LOOP4
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
7	6	5	4	3	2	1	0
			IOFFDAC_AACM_READ_LOOP4				
				R-xh			

Table 7-145. Register A6h Field Descriptions

Bit	Field	Type	Reset	Description
23-9	x	R	xh	
8	POL_OFFSETDAC_AACM_READ_LOOP4	R	xh	Readout of AACM output for Loop 4 (Polarity of Offset DAC controlled by the loop)
7-0	IOFFDAC_AACM_READ_LOOP4	R	xh	Readout of AACM output for Loop 4 (Amplitude of Offset DAC controlled by the loop)

7.6.3.1.58 DEC5TO8_1: Register A9h (address = A9h)**Figure 7-165. Register A9h**

23	22	21	20	19	18	17	16
0	0	0	0	PPG_DEC8_TIA_SEL	PPG_DEC7_TIA_SEL	PPG_DEC6_TIA_SEL	PPG_DEC5_TIA_SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	REG_PPG_DEC8_FACTOR			0	REG_PPG_DEC7_FACTOR		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
0	REG_PPG_DEC6_FACTOR			0	REG_PPG_DEC5_FACTOR		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 7-146. Register A9h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R/W	0h	Must write 0
19	PPG_DEC8_TIA_SEL	R/W	0h	Select the decimation filter 8 association with TIA 0 – TIA1, 1 – TIA2
18	PPG_DEC7_TIA_SEL	R/W	0h	Select the decimation filter 7 association with TIA. 0 – TIA1, 1 – TIA2
17	PPG_DEC6_TIA_SEL	R/W	0h	Select the decimation filter 6 association with TIA 0 – TIA1, 1 – TIA2
16	PPG_DEC5_TIA_SEL	R/W	0h	Select the decimation filter 5 association with TIA 0 – TIA1, 1 – TIA2
15	0	R/W	0h	Must write 0
14-12	REG_PPG_DEC8_FACTOR	R/W	0h	Decimation factor control for PPG Decimation filter 8
11	0	R/W	0h	Must write 0
10-8	REG_PPG_DEC7_FACTOR	R/W	0h	Decimation factor control for PPG Decimation filter 7
7	0	R/W	0h	Must write 0
6-4	REG_PPG_DEC6_FACTOR	R/W	0h	Decimation factor control for PPG Decimation filter 6
3	0	R/W	0h	Must write 0
2-0	REG_PPG_DEC5_FACTOR	R/W	0h	Decimation factor control for PPG Decimation filter 5

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7.6.3.1.59 DEC5TO8_2: Register AAh (address = AAh)**Figure 7-166. Register AAh**

23	22	21	20	19	18	17	16
EN_PPG_DEC8		REG_NUMPH_PPG_DEC8		EN_PPG_DEC7	REG_NUMPH_PPG_DEC7		
R/W-0h		R/W-0h		R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8
		REG_NUMPH_PPG_DEC7		EN_PPG_DEC6	REG_NUMPH_PPG_DEC6		
		R/W-0h		R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
REG_NUMPH_PPG_DEC6	EN_PPG_DEC5		REG_NUMPH_PPG_DEC5				
R/W-0h	R/W-0h		R/W-0h				

Table 7-147. Register AAh Field Descriptions

Bit	Field	Type	Reset	Description
23	EN_DEC8	R/W	0h	Enable PPG Decimation filter 8.
22-18	REG_NUMPH_PPG_DEC8	R/W	0h	PPG Phase number to which PPG Decimation filter #4 needs to be assigned is set as (REG_NUMPH_PPG_DEC8+1)
17	EN_PPG_DEC7	R/W	0h	Enable PPG Decimation filter 7
16-12	REG_NUMPH_PPG_DEC7	R/W	0h	PPG Phase number to which PPG Decimation filter #3 needs to be assigned is set as (REG_NUMPH_PPG_DEC7+1)
11	EN_PPG_DEC6	R/W	0h	Enable PPG Decimation filter 6
10-6	REG_NUMPH_PPG_DEC6	R/W	0h	PPG Phase number to which PPG Decimation filter #2 needs to be assigned is set as (REG_NUMPH_PPG_DEC6+1)
5	EN_PPG_DEC5	R/W	0h	Enable PPG Decimation filter 5
4-0	REG_NUMPH_PPG_DEC5	R/W	0h	PPG Phase number to which PPG Decimation filter #1 needs to be assigned is set as (REG_NUMPH_PPG_DEC5+1)

7.6.3.1.60 OSC_CALIB: Register B0h (address = B0h)**Figure 7-167. Register B0h**

23	22	21	20	19	18	17	16
EN_128K_CLK_CALIB_2	0	CLK_128K_CALIB_RANGE		0	CLK_128K_CALIB_RECONV_THR		
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8
0	0	0		EXT_CLK_CNT_CALIB			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
			EXT_CLK_CNT_CALIB				
				R/W-0h			

Table 7-148. Register B0h Field Descriptions

Bit	Field	Type	Reset	Description
23	EN_128K_CLK_CALIB_2	R/W	0h	Enable calibration routine for 128 kHz oscillator using external RTC clock
22	0	R/W	0h	Must write 0
21-20	CLK_128K_CALIB_RANGE	R/W	0h	Set CLK_128K_CALIB_RANGE = 2
19	0	R/W	0h	Must write 0
18-16	CLK_128K_CALIB_RECONV_THR	R/W	0h	Hysteresis control for re-convergence in Oscillator calibration routine
15-13	0	R/W	0h	Must write 0
12-0	EXT_CLK_CNT_CALIB	R/W	0h	Information of the frequency of the external (RTC) clock used for calibrating the internal oscillator

7.6.3.1.61 THR_GLOBAL: Register B4h (address = B4h)**Figure 7-168. Register B4h**

23	22	21	20	19	18	17	16
COMB_THR_D ET_EN	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	REG_THR_DE T_PHASE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
REG_THR_DET_PHASE				0	THR_SEL_LOGIC		THR_DET_EN
R/W-0h				R/W-0h		R/W-0h	

Table 7-149. Register B4h Field Descriptions

Bit	Field	Type	Reset	Description
23	COMB_THR_DET_EN	R/W	0h	Enables Combinational threshold detect mode
22-9	0	R/W	0h	Must write 0
8-4	REG_THR_DET_PHASE	R/W	0h	The phase number, the data from which is to be used for the Threshold detect comparison is programmed as (REG_THR_DET_PHASE+1).
3	0	R/W	0h	Must write 0
2-1	THR_SEL_LOGIC	R/W	0h	Determines whether generation of Threshold detect interrupt is based on the code being within range or out of range of the high and low threshold codes 00 = Generate interrupt if code is within range of thresholds 01 = Generate interrupt if code is outside range of thresholds Other settings = Do not use
0	THR_DET_EN	R/W	0h	Enables threshold detect mode

7.6.3.1.62 READ_THR_FLAG: Register B5h (address = B5h)**Figure 7-169. Register B5h**

23	22	21	20	19	18	17	16
THR_PPG_FLAG							
R-0h							
15	14	13	12	11	10	9	8
THR_PPG_FLAG							
R-0h							
7	6	5	4	3	2	1	0
THR_PPG_FLAG							
R-0h							

Table 7-150. Register B5h Field Descriptions

Bit	Field	Type	Reset	Description
23-0	THR_PPG_FLAG	R	0h	Flag register that indicates the result of threshold detect comparison. THR_PPG_FLAG[N] corresponds to the result of threshold detect comparison from PPG phase [N]

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7.6.3.1.63 READ_AC_LEAD: Register B6h (address = B6h)**Figure 7-170. Register B6h**

23	22	21	20	19	18	17	16
AC LEAD AMPL							
R-0h							
15	14	13	12	11	10	9	8
AC LEAD AMPL							
R-0h							
7	6	5	4	3	2	1	0
AC LEAD AMPL							
R-0h							

Table 7-151. Register B6h Field Descriptions

Bit	Field	Type	Reset	Description
23-0	AC LEAD AMPL	R	0h	Amplitude of the accumulator output (average of which over 16 samples is the AC lead signal)

7.6.3.1.64 THR_AC_LEAD: Register B7h (address = B7h)**Figure 7-171. Register B7h**

23	22	21	20	19	18	17	16
0				AC LEAD DET THR H			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
		AC LEAD DET THR H		0	0	0	0
			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
			AC LEAD DET THR L				
			R/W-0h				

Table 7-152. Register B7h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22-12	AC LEAD DET THR H	R/W	0h	AC lead detect high threshold $2^{10} \times$ AC LEAD DET THR H is compared with magnitude of ADC output
11-8	0	R/W	0h	Must write 0
7-0	AC LEAD DET THR L	R/W	0h	AC lead detect low threshold $2^{10} \times$ AC LEAD DET THR L is compared with magnitude of ADC output

7.6.3.1.65 AC_LEAD_DEMOD_CFG: Register B8h (address = B8h)**Figure 7-172. Register B8h**

23	22	21	20	19	18	17	16
AC_LEAD_DEMOD_CFG							
R/W-66h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-153. Register B8h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	AC_LEAD_DEMOD_CFG	R/W	66h	Demodulation scheme for AC lead strength detection. Use only in Rev2 Silicon.
15-0	0	R/W	0h	Must write 0

7.6.3.1.66 HPF_REG1: Register B9h (address = B9h)**Figure 7-173. Register B9h**

23	22	21	20	19	18	17	16
0				ECG_SAT_DET_WIDTH			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
DIS_ECG_INA_SAT_DET	DIS_AUTO_HPF_RST	EN_DYN_HPF_RST_PW	FORCE_HPF_RST	DIS_HPF_RST_ON_MODE_SWITCH	0		HPF_RST_PW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
				HPF_RST_PW			
				R/W-0h			

Table 7-154. Register B9h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22-16	ECG_SAT_DET_WIDTH	R/W	2Eh	Saturation detect window width for saturation detection
15	DIS_ECG_INA_SAT_DET	R/W	0h	Set to '1' to switch to ECG saturation detection using Digital detection method
14	DIS_AUTO_HPF_RST	R/W	0h	Disable automatic reset of HPF on detection of ECG saturation
13	EN_DYN_HPF_RST_PW	R/W	0h	Set to '1' to switch from Fixed HPF reset pulse width mode to Dynamic HPF reset pulse width mode
12	FORCE_HPF_RST	R/W	0h	Manually reset the HPF for the duration this bit is set to '1'
11	DIS_HPF_RST_ON_MODE_SWITCH	R/W	0h	Set this bit to '1' to disable automatic HPF reset generation on mode switching
10	0	R/W	0h	Must write 0
9-0	HPF_RST_PW	R/W	63h	Program the pulse width of the HPF reset pulse

7.6.3.1.67 HPF_REG2: Register BAh (address = BAh)**Figure 7-174. Register BAh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	SCALE_LEAD_DET_WIDTH_PPG	G
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
LEAD_DET_WIDTH							
R/W-0h							

Table 7-155. Register BAh Field Descriptions

Bit	Field	Type	Reset	Description
23-18	0	R/W	0h	Must write 0
17-16	SCALE_LEAD_DET_WIDTH_PPG	R/W	0h	Scale the lead detect time in PPG mode. $t_{LEAD_DET_WIDTH_PPG} = t_{CLK_PRF} \times 128 \times LEAD_DET_WIDTH / 2^{SCALE_LEAD_DET_WIDTH_PPG}$
15-8	0	R/W	0h	Must write 0
7-0	LEAD_DET_WIDTH	R/W	64h	Lead detect width $t_{LEAD_DET_WIDTH} = t_{CLK_PRF} \times 128 \times LEAD_DET_WIDTH$

7.6.3.1.68 MASK_INT_REG: Register BBh (address = BBh)**Figure 7-175. Register BBh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	1	1	MASK_ADC_FI FO_RDY	MASK_AC_LEA D_OFF	MASK_AC_LEA D_ON	MASK_DC_LE AD_DET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-156. Register BBh Field Descriptions

Bit	Field	Type	Reset	Description
23-6	0	R/W	0h	Must write 0
5-4	1	R/W	0h	Must write 1
3	MASK_ADC_FIFO_RDY	R/W	0h	Mask bit for masking FIFO_RDY soft interrupt from generating the hard interrupt
2	MASK_AC_LEAD_OFF	R/W	0h	Mask bit for masking AC_LEAD_OFF soft interrupt from generating the hard interrupt
1	MASK_AC_LEAD_ON	R/W	0h	Mask bit for masking AC_LEAD_ON soft interrupt from generating the hard interrupt
0	MASK_DC_LEAD_DET	R/W	0h	Mask bit for masking DC_LEAD_DET soft interrupt from generating the hard interrupt

7.6.3.1.69 INTR_SOFT: Register BCh (address = BCh)**Figure 7-176. Register BCh**

23	22	21	20	19	18	17	16
AC LEAD SEQ	x	x	ECG INA OUT P COMP H	ECG INA OUT P COMP L	ECG INA OUT M COMP H	ECG INA OUT M COMP L	
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
15	14	13	12	11	10	9	8
x	x	x	x	x	ECG INP LEA D STATUS	ECG INM LEA D STATUS	ECG RLD LEA D STATUS
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh

Table 7-157. Register BCh Field Descriptions

Bit	Field	Type	Reset	Description
23-22	AC LEAD SEQ	R	x	Indicates the most recent AC lead status, whether Lead On or Lead Off
21-20	x	R	x	Read only register
19	ECG INA OUTP COMP H	R	x	Output of the saturation detect comparators at the INA output.
18	ECG INA OUTP COMP L	R	x	
17	ECG INA OUTM COMP H	R	x	
16	ECG INA OUTM COMP L	R	x	
15-11	x	R	x	Read only register
10	ECG INP LEAD STATUS	R	x	Connect status of INP electrode
9	ECG INM LEAD STATUS	R	x	Connect status of INM electrode
8	ECG RLD LEAD STATUS	R	x	Connect status of RLD electrode
7-0	x	R	x	Read only register

7.6.3.1.70 CONTROL25: Register BEh (address = BEh)**Figure 7-177. Register BEh**

23	22	21	20	19	18	17	16
0	EN_DATA_MARKER	0	0	0	0	INPUT_PRF_RST_ON_GPIO2	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0			DEEP_SLEEP_DEL	
R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h	
7	6	5	4	3	2	1	0
0	0	REL_AFE_FREEZE	REG_INTR_TO_AFE	0		MODE_SEL	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

Table 7-158. Register BEh Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22	EN_DATA_MARKER	R/W	0h	Controls Tagging of 2 LSBs in data
21-18	0	R/W	0h	Must write 0
17-16	INPUT_PRF_RST_ON_GPIO2	R/W	0h	Configure two AFEs in master-slave mode for PRF reset
15-12	0	R/W	0h	Must write 0
11-8	DEEP_SLEEP_DEL	R/W	0h	Delay the deep sleep signal to the bandgap pin connect switch. Set DEEP_SLEEP_DEL register to 3h.
7-6	0	R/W	0h	Must write 0
5	REL_AFE_FREEZE	R/W	0h	Register bit associated with release of AFE freeze state associated with transition from one data acquisition mode to another
4	REG_INTR_TO_AFE	R/W	0h	Soft interrupt bit to AFE to initiate switch from one data acquisition mode to another
3	0	R/W	0h	Must write 0
2-0	MODE_SEL	R/W	1h	Selection of data acquisition mode

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7.6.3.1.71 MIX_REG1: Register C0h (address = C0h)**Figure 7-178. Register C0h**

23	22	21	20	19	18	17	16
1	0	1	0	1	0	1	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0		REG_PRPCT_MIX		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
				REG_PRPCT_MIX			
				R/W-0h			

Table 7-159. Register C0h Field Descriptions

Bit	Field	Type	Reset	Description
23-12	0	R/W	AA0h	Must write AAh
11-0	REG_PRPCT_MIX	R/W	0h	PRF control in Mixed acquisition mode

7.6.3.1.72 MIX_REG2: Register C1h (address = C1h)**Figure 7-179. Register C1h**

23	22	21	20	19	18	17	16
CONFIG_TS7_MIX			CONFIG_TS6_MIX			CONFIG_TS5_MIX	
R/W-0h			R/W-0h			R/W-0h	
15	14	13	12	11	10	9	8
CONFIG_TS5_MIX	CONFIG_TS4_MIX			CONFIG_TS3_MIX			CONFIG_TS2_MIX
R/W-0h	R/W-0h			R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
CONFIG_TS2_MIX	CONFIG_TS1_MIX			CONFIG_TS0_MIX			
R/W-0h	R/W-0h			R/W-0h			

Table 7-160. Register C1h Field Descriptions

Bit	Field	Type	Reset	Description
23-21	CONFIG_TS7_MIX	R/W	0h	Definition of Time slot 7 in Mixed acquisition mode
20-18	CONFIG_TS6_MIX	R/W	0h	Definition of Time slot 6 in Mixed acquisition mode
17-15	CONFIG_TS5_MIX	R/W	0h	Definition of Time slot 5 in Mixed acquisition mode
14-12	CONFIG_TS4_MIX	R/W	0h	Definition of Time slot 4 in Mixed acquisition mode
11-9	CONFIG_TS3_MIX	R/W	0h	Definition of Time slot 3 in Mixed acquisition mode
8-6	CONFIG_TS2_MIX	R/W	0h	Definition of Time slot 2 in Mixed acquisition mode
5-3	CONFIG_TS1_MIX	R/W	0h	Definition of Time slot 1 in Mixed acquisition mode
2-0	CONFIG_TS0_MIX	R/W	0h	Definition of Time slot 0 in Mixed acquisition mode

7.6.3.1.73 PSAW_REG2: Register C4h (address = C4h)**Figure 7-180. Register C4h**

23	22	21	20	19	18	17	16
REG_NUM_PH_PSAW4				0	0	0	REG_START_PH_PSAW4
R/W-0h			R/W-0h			R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
REG_START_PH_PSAW4				REG_NUM_PH_PSAW3			
R/W-0h							
7	6	5	4	3	2	1	0
REG_NUM_PH_PSAW3			REG_START_PH_PSAW3			R/W-0h	
R/W-0h							

Table 7-161. Register C4h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	REG_NUM_PH_PSAW4	R/W	0h	Sets number of PPG phases inside PSAW4 in Mixed acquisition mode.
19-17	0	R/W	0h	Must write 0
16-12	REG_START_PH_PSAW4	R/W	0h	Sets starting PPG phase number inside PSAW4 in Mixed acquisition mode
11-8	REG_NUM_PH_PSAW3	R/W	0h	Sets number of PPG phases inside PSAW3 in Mixed acquisition mode
7-5	0	R/W	0h	Must write 0
4-0	REG_START_PH_PSAW3	R/W	0h	Sets starting PPG phase number inside PSAW3 in Mixed acquisition mode

7.6.3.1.74 MIX_REG4: Register C5h (address = C5h)**Figure 7-181. Register C5h**

23	22	21	20	19	18	17	16
0	0	SEL_DEC_FILT_TS7_MIX	0	0	SEL_DEC_FILT_TS6_MIX	0	0
R/W-0h							
15	14	13	12	11	10	9	8
SEL_DEC_FILT_TS5_MIX	0	0	SEL_DEC_FILT_TS4_MIX	0	0	SEL_DEC_FILT_TS3_MIX	0
R/W-0h							
7	6	5	4	3	2	1	0
0	SEL_DEC_FILT_TS2_MIX	0	0	SEL_DEC_FILT_TS1_MIX	0	0	SEL_DEC_FILT_TS0_MIX
R/W-0h							

Table 7-162. Register C5h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	Must write 0
21	SEL_DEC_FILT_TS7_MIX	R/W	0h	While operating in the Mixed acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS7
20-19	0	R/W	0h	Must write 0
18	SEL_DEC_FILT_TS6_MIX	R/W	0h	While operating in the Mixed acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS6
17-16	0	R/W	0h	Must write 0
15	SEL_DEC_FILT_TS5_MIX	R/W	0h	While operating in the Mixed acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS5
14-13	0	R/W	0h	Must write 0
12	SEL_DEC_FILT_TS4_MIX	R/W	0h	While operating in the Mixed acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS4
11-10	0	R/W	0h	Must write 0
9	SEL_DEC_FILT_TS3_MIX			While operating in the Mixed acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS3
8-7		R/W	0h	Must write 0
6	SEL_DEC_FILT_TS2_MIX	R/W	0h	While operating in the Mixed acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS2
5-4	0	R/W	0h	Must write 0
3	SEL_DEC_FILT_TS1_MIX	R/W	0h	While operating in the Mixed acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS1
2-1	0	R/W	0h	Must write 0
0	SEL_DEC_FILT_TS0_MIX	R/W	0h	While operating in the Mixed acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS0

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7.6.3.1.75 MIX_REG5: Register C7h (address = C7h)**Figure 7-182. Register C7h**

23	22	21	20	19	18	17	16			
0	0			REG_PPG_GBL_MASK_FACTOR						
R/W-0h	R/W-0h			R/W-0h						
15	14	13	12	11	10	9	8			
0	0	0	0	0	0	0	0			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0			
0	0	0	0	0	REG_ECG_DEC_FACTOR_MIX					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h					

Table 7-163. Register C7h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	Must write 0
21-16	REG_PPG_GBL_MASK_FACTOR	R/W	0h	Sets global masking factor for PPG signals when operating in Mixed acquisition mode. It should be set to '0' in PPG only mode.
15-3	0	R/W	0h	Must write 0
2-0	REG_ECG_DEC_FACTOR_MIX	R/W	0h	Sets decimation factor for the ECG decimation filter when operating in Mixed acquisition mode

7.6.3.1.76 CONTROL26: Register CAh (address = CAh)**Figure 7-183. Register CAh**

23	22	21	20	19	18	17	16			
				REG_ACTIVE_CONTROLS						
				R/W-0h						
15	14	13	12	11	10	9	8			
				REG_ACTIVE_CONTROLS						
				R/W-0h						
7	6	5	4	3	2	1	0			
				REG_ACTIVE_CONTROLS						
				R/W-0h						

Table 7-164. Register CAh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	REG_ACTIVE_CONTROLS	R/W	024880h	Power cycling control register

7.6.3.1.77 CONTROL27: Register CBh (address = CBh)**Figure 7-184. Register CBh**

23	22	21	20	19	18	17	16
0	0	0	OSC_DIS_128K_NOTPPG	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-165. Register CBh Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	R/W	0h	Must write 0
20	OSC_DIS_128K_NOTPPG	R/W	0h	In ECG or Mixed acquisition mode this register bit is used instead of OSC_DIS_128K_PPG
19-8	0	R/W	0h	Must write 0
7-0	4Fh	R/W	4Fh	Must write 4Fh

7.6.3.1.78 CONTROL28: Register CFh (address = CFh)**Figure 7-185. Register CFh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
EN_ECG_DIG_SAT_DET	0	0	0		REG_DIG_SAT_THR_H		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
0	0	0	0		REG_DIG_SAT_THR_L		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		

Table 7-166. Register CFh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	R/W	0h	Must write 0
15	EN_ECG_DIG_SAT_DET	R/W	0h	Enables Digital Saturation detection mode for detection of ECG channel saturation – use in conjunction with DIS_ECG_INA_SAT_DET to switch from Analog saturation detection to Digital saturation detection
14-12	0	R/W	0h	Must write 0
11-8	REG_DIG_SAT_THR_H	R/W	Eh	High threshold control for Digital saturation detection
7-4	0	R/W	0h	Must write 0
3-0	REG_DIG_SAT_THR_L	R/W	8h	Low threshold control for Digital saturation detection

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7.6.3.1.79 ECG_REG1: Register D0h (address = D0h)**Figure 7-186. Register D0h**

23	22	21	20	19	18	17	16
1	0	1	0	1	0	1	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0		REG_PRPCT_ECG		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
				REG_PRPCT_ECG			
				R/W-0h			

Table 7-167. Register D0h Field Descriptions

Bit	Field	Type	Reset	Description
23-12	0	R/W	0h	Must write 0
11-0	REG_PRPCT_ECG	R/W	0h	PRF control in ECG acquisition mode

7.6.3.1.80 ECG_REG2: Register D1h (address = D1h)**Figure 7-187. Register D1h**

23	22	21	20	19	18	17	16
			CONFIG_TS7_ECG		CONFIG_TS6_ECG		CONFIG_TS5_ECG
			R/W-0h		R/W-0h		R/W-0h
15	14	13	12	11	10	9	8
CONFIG_TS5_ECG		CONFIG_TS4_ECG		CONFIG_TS3_ECG		CONFIG_TS2_ECG	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
CONFIG_TS2_ECG		CONFIG_TS1_ECG		CONFIG_TS0_ECG			
R/W-0h		R/W-0h		R/W-0h			

Table 7-168. Register D1h Field Descriptions

Bit	Field	Type	Reset	Description
23-21	CONFIG_TS7_ECG	R/W	0h	Definition of Time slot 7 in ECG acquisition mode
20-18	CONFIG_TS6_ECG	R/W	0h	Definition of Time slot 6 in ECG acquisition mode
17-15	CONFIG_TS5_ECG	R/W	0h	Definition of Time slot 5 in ECG acquisition mode
14-12	CONFIG_TS4_ECG	R/W	0h	Definition of Time slot 4 in ECG acquisition mode
11-9	CONFIG_TS3_ECG	R/W	0h	Definition of Time slot 3 in ECG acquisition mode
8-6	CONFIG_TS2_ECG	R/W	0h	Definition of Time slot 2 in ECG acquisition mode
5-3	CONFIG_TS1_ECG	R/W	0h	Definition of Time slot 1 in ECG acquisition mode
2-0	CONFIG_TS0_ECG	R/W	0h	Definition of Time slot 0 in ECG acquisition mode

7.6.3.1.81 ECG_REG3: Register D2h (address = D2h)**Figure 7-188. Register D2h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0			REG_NUM_ESAW_ECG			
R/W-0h	R/W-0h			R/W-0h			

Table 7-169. Register D2h Field Descriptions

Bit	Field	Type	Reset	Description
23-6	0	R/W	0h	Must write 0
5-0	REG_NUM_ESAW_ECG	R/W	0h	Number of ESAW while operating in ECG acquisition mode

7.6.3.1.82 ECG_REG4: Register D3h (address = D3h)**Figure 7-189. Register D3h**

23	22	21	20	19	18	17	16
0	0	SEL_DEC_FILT_TS7_ECG	0	0	SEL_DEC_FILT_TS6_ECG	0	0
R/W-0h							
15	14	13	12	11	10	9	8
SEL_DEC_FILT_TS5_ECG	0	0	SEL_DEC_FILT_TS4_ECG	0	0	SEL_DEC_FILT_TS3_ECG	0
R/W-0h							
7	6	5	4	3	2	1	0
0	SEL_DEC_FILT_TS2_ECG	0	0	SEL_DEC_FILT_TS1_ECG	0	0	SEL_DEC_FILT_TS0_ECG
R/W-0h							

Table 7-170. Register D3h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	Must write 0
21	SEL_DEC_FILT_TS7_ECG	R/W	0h	While operating in the ECG acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS7
20-19	0	R/W	0h	Must write 0
18	SEL_DEC_FILT_TS6_ECG	R/W	0h	While operating in the ECG acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS6
17-16	0	R/W	0h	Must write 0
15	SEL_DEC_FILT_TS5_ECG	R/W	0h	While operating in the ECG acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS5
14-13	0	R/W	0h	Must write 0
12	SEL_DEC_FILT_TS4_ECG	R/W	0h	While operating in the ECG acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS4
11-10	0	R/W	0h	Must write 0
9	SEL_DEC_FILT_TS3_ECG	R/W	0h	While operating in the ECG acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS3
8-7	0	R/W	0h	Must write 0
6	SEL_DEC_FILT_TS2_ECG	R/W	0h	While operating in the ECG acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS2
5-4	0	R/W	0h	Must write 0
3	SEL_DEC_FILT_TS1_ECG	R/W	0h	While operating in the ECG acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS1
2-1	0	R/W	0h	Must write 0
0	SEL_DEC_FILT_TS0_ECG	R/W	0h	While operating in the ECG acquisition mode, enable the ECG decimation filter for ECG data stream in time slot TS0

7.6.3.1.83 ECG_REG5: Register D5h (address = D5h)**Figure 7-190. Register D5h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	REG_ECG_DEC_FACTOR_ECG		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

Table 7-171. Register D5h Field Descriptions

Bit	Field	Type	Reset	Description
23-3	0	R/W	0h	Must write 0
2-0	REG_ECG_DEC_FACTOR_ECG	R/W	0h	Decimation factor for ECG decimation filter when operating in ECG acquisition mode

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7.6.3.1.84 CONTROL29: Register D7h (address = D7h)**Figure 7-191. Register D7h**

23	22	21	20	19	18	17	16
0	REG_FSWITCH_IMP	SWAP_CFG_RES		LEAD_DET_THR_H_NOTPPG			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
15	14	13	12	11	10	9	8
			LEAD_DET_THR_L_NOTPPG	0	EN LEAD DET _CURRE NOTPPG	EN LEAD DET _COMP NOTPPG	SEL ECG_BIAS RES NOTPPG
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEL_ECG_BIAS_RES_NOTPPG		CFG_RES_ECG_INM_NOTPPG		CFG_RES_ECG_INP_NOTPPG			
R/W-0h		R/W-0h		R/W-0h			

Table 7-172. Register D7h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22-21	REG_FSWITCH_IMP	R/W	0h	Switching rate of input excitation for Impedance measurement
20	SWAP_CFG_RES	R/W	0h	This bit controls the biasing combination for the ECG input and RLD pins
19-16	LEAD_DET_THR_H_NOTPPG	R/W	0h	While operating in ECG or Mixed acquisition mode, this register controls the high threshold voltage setting for the DC Lead detection
15-12	LEAD_DET_THR_L_NOTPPG	R/W	0h	While operating in ECG or Mixed acquisition mode, this register controls the low threshold voltage setting for the DC Lead detection (Active DC lead detection and Low power DC lead detection)
11	0	R/W	0h	Must write 0
10	EN LEAD DET _CURRE NOTPPG	R/W	0h	While operating in ECG or Mixed acquisition mode, this bit turns on the lead detect current sources used in the Active DC lead detection and AC lead detection
9	EN LEAD DET _COMP NOTPPG	R/W	0h	While operating in ECG or Mixed acquisition mode, this bit turns on the comparators in the Low power DC lead detect and Active DC lead detect modes
8-6	SEL_ECG_BIAS_RES_NOTPPG	R/W	0h	While operating in ECG or Mixed acquisition mode, this register controls the value of the input bias resistors that connect to the ECG input pins and RLD pin
5-3	CFG_RES_ECG_INM_NOTPPG	R/W	0h	While operating in ECG or Mixed acquisition mode, these registers control the connectivity of the input bias resistors that connect to the ECG input pins and RLD pin
2-0	CFG_RES_ECG_INP_NOTPPG	R/W	0h	

7.6.3.1.85 CONTROL30: Register D8h (address = D8h)**Figure 7-192. Register D8h**

23	22	21	20	19	18	17	16
0	0	0	0		LEAD_DET_THR_H_PPG		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
15	14	13	12	11	10	9	8
		LEAD_DET_THR_L_PPG		0	EN_LEAD_DET_CURR_PPG	EN_LEAD_DET_COMP_PPG	SEL_ECG_BIAS_RES_PPG
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEL_ECG_BIAS_RES_PPG		CFG_RES_ECG_INM_PPG			CFG_RES_ECG_INP_PPG		
R/W-0h		R/W-0h			R/W-0h		

Table 7-173. Register D8h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R/W	0h	Must write 0
19-16	LEAD_DET_THR_H_PPG	R/W	0h	While operating in PPG acquisition mode, this register controls the high threshold voltage setting for the DC Lead detection
15-12	LEAD_DET_THR_L_PPG	R/W	0h	While operating in PPG acquisition mode, this register controls the low threshold voltage setting for the DC Lead detection (Active DC lead detection and Low power DC lead detection)
11	0	R/W	0h	Must write 0
10	EN_LEAD_DET_CURR_PPG	R/W	0h	While operating in PPG acquisition mode, this bit turns on the lead detect current sources used in the Active DC lead detection and AC lead detection
9	EN_LEAD_DET_COMP_PPG	R/W	0h	While operating in PPG acquisition mode, this bit turns on the comparators in the Low power DC lead detect and Active DC lead detect modes
8-6	SEL_ECG_BIAS_RES_PPG	R/W	0h	While operating in PPG acquisition mode, this register controls the value of the input bias resistors that connect to the ECG input pins and RLD pin
5-3	CFG_RES_ECG_INM_PPG	R/W	0h	While operating in PPG acquisition mode, these registers control the connectivity of the input bias resistors that connect to the ECG input pins and RLD pin
2-0	CFG_RES_ECG_INP_PPG	R/W	0h	

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7.6.3.1.86 CONTROL31: Register D9h (address = D9h)**Figure 7-193. Register D9h**

23	22	21	20	19	18	17	16
0	0	0	0	0	EN_AUTO_HPF_RST_AC_COUPLING	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	EN_AC_LEAD_DET	SEL_ECG_INM_CURR_POL	SEL_ECG_INP_CURR_POL		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
		ILEAD_BIAS_AMP			ILEAD_AMP		
		R/W-0h			R/W-0h		

Table 7-174. Register D9h Field Descriptions

Bit	Field	Type	Reset	Description
23-19	0	R/W	0h	Must write 0
18	EN_AUTO_HPF_RST_AC_COUPLING	R/W	0h	Enable automatic reset of AC coupling capacitor to ECG inputs.
12	EN_AC_LEAD_DET	R/W	0h	Set this bit to '1' while enabling the AC lead detect block
11-10	SEL_ECG_INM_CURR_POL	R/W	0h	Activates the source/ sink lead detect current sources on INM when operating in the Active DC lead detect mode. Set to '00' when operating in the AC lead detect mode
9-8	SEL_ECG_INP_CURR_POL	R/W	0h	Activates the source/ sink lead detect current sources on INP when operating in the Active DC lead detect mode. Set to '00' when operating in the AC lead detect mode
7-3	ILEAD_BIAS_AMP	R/W	0h	Set this register according to the setting of ILEAD_AMP
2-0	ILEAD_AMP	R/W	0h	Programs the amplitude of the lead detect current sources when operating in the Active DC lead detect or AC lead detect modes

7.6.4 Per-phase registers

7.6.4.1 REG1_PH1: Phase start address + 0

Figure 7-194. Phase start address + 0

23	22	21	20	19	18	17	16
IN_TIA2<4:1>				IN_TIA1<4:1>			
R/W-x				R/W-x			
15	14	13	12	11	10	9	8
LED_DRV2_TX<8:1>				R/W-x			
LED_DRV1_TX<8:1>				R/W-x			
7	6	5	4	3	2	1	0

Table 7-175. Phase start address + 0 Field Descriptions

Bit	Field	Type	Reset	Description
23	IN_TIA2<4>	R/W	x	Connect input pin set IN4 to TIA2
22	IN_TIA2<3>	R/W	x	Connect input pin set IN3 to TIA2
21	IN_TIA2<2>	R/W	x	Connect input pin set IN2 to TIA2
20	IN_TIA2<1>	R/W	x	Connect input pin set IN1 to TIA2
19	IN_TIA1<4>	R/W	x	Connect input pin set IN4 to TIA1
18	IN_TIA1<3>	R/W	x	Connect input pin set IN3 to TIA1
17	IN_TIA1<2>	R/W	x	Connect input pin set IN2 to TIA1
16	IN_TIA1<1>	R/W	x	Connect input pin set IN1 to TIA1
15	LED_DRV2_TX<8>	R/W	x	Connect LED driver 2 to TX8 pin
14	LED_DRV2_TX<7>	R/W	x	Connect LED driver 2 to TX7 pin
13	LED_DRV2_TX<6>	R/W	x	Connect LED driver 2 to TX6 pin
12	LED_DRV2_TX<5>	R/W	x	Connect LED driver 2 to TX5 pin
11	LED_DRV2_TX<4>	R/W	x	Connect LED driver 2 to TX4 pin
10	LED_DRV2_TX<3>	R/W	x	Connect LED driver 2 to TX3 pin
9	LED_DRV2_TX<2>	R/W	x	Connect LED driver 2 to TX2 pin
8	LED_DRV2_TX<1>	R/W	x	Connect LED driver 2 to TX1 pin
7	LED_DRV1_TX<8>	R/W	x	Connect LED driver 1 to TX8 pin
8	LED_DRV1_TX<7>	R/W	x	Connect LED driver 1 to TX7 pin
5	LED_DRV1_TX<6>	R/W	x	Connect LED driver 1 to TX6 pin
4	LED_DRV1_TX<5>	R/W	x	Connect LED driver 1 to TX5 pin
3	LED_DRV1_TX<4>	R/W	x	Connect LED driver 1 to TX4 pin
2	LED_DRV1_TX<3>	R/W	x	Connect LED driver 1 to TX3 pin
1	LED_DRV1_TX<2>	R/W	x	Connect LED driver 1 to TX2 pin
0	LED_DRV1_TX<1>	R/W	x	Connect LED driver 1 to TX1 pin

7.6.4.2 REG2_PH1: Phase start address + 1**Figure 7-195. Phase start address + 1**

23	22	21	20	19	18	17	16
IOFFDAC_PH_TIA1							
R/W-x							
15	14	13	12	11	10	9	8
USE_DIG_AAC_M_TIA1	USE_ANA_AA_CM_TIA1	UPDATE_BASELINE_TIA1		CF_TIA1		REG_LOOP_NUM_TIA1	
R/W-x	R/W-x	R/W-x		R/W-x		R/W-x	
7	6	5	4	3	2	1	0
RF_TIA1				REG_NUMAV			
R/W-x							

Table 7-176. Phase start address + 1 Field Descriptions

Bit	Field	Type	Reset	Description
23-16	IOFFDAC_PH_TIA1	R/W	x	Determines current setting for that phase for the Ambient Offset DAC of TIA1 or for the LED Offset DAC of TIA1
15	USE_DIG_AACM_TIA1	R/W	x	Associate Digital AACM loop (Loop number as set by REG_LOOP_NUM_TIA1) to cancel input DC current of TIA1
14	USE_ANA_AACM_TIA1	R/W	x	Associate an Analog AACM loop operation with TIA1 signal of phase
13	UPDATE_BASELINE_TIA1	R/W	x	Setting this bit to '1' causes the Ambient Offset DAC of TIA1 to be updated to the set value of IOFFDAC_PH_TIA1 when the AACM loop is not enabled. When the AACM loop is enabled, setting this bit to '1' is an indication that this phase is meant to serve as the baseline ambient phase, and that the ambient needs to be acquired in this phase. Setting this bit to '0' uses the baseline value of the ambient from the previous baseline ambient phase.
12-10	CF_TIA1	R/W	x	TIA feedback capacitor (Cf) setting of TIA1 for the phase
9-8	REG_LOOP_NUM_TIA1	R/W	x	This word specifies the Digital AACM Loop number (set as REG_LOOP_NUM_TIA1+1) to be used for that phase for TIA1 (applicable when USE_DIG_AACM_TIA1 is set to '1').
7-4	RF_TIA1	R/W	x	TIA gain (Rf) setting of TIA1 for the phase
3-0	REG_NUMAV	R/W	x	Number of ADC averages for the phase is set as (REG_NUMAV+1)

7.6.4.3 REG3_PH1: Phase start address + 2**Figure 7-196. Phase start address + 2**

23	22	21	20	19	18	17	16
TIA_SEL	PHASE_INT_G PIO	0	CONFIG_PHASE_AS_IMP	FIFO_DATA_CTRL_1	THR_SEL_DATA_CTRL		
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		R/W-x
15	14	13	12	11	10	9	8
THR_SEL_DATA_CTRL	0	FIFO_DATA_CTL_2	STAGGER_LED	FILTER_SET_SEL	0	0	0
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
7	6	5	4	3	2	1	0
REG_TWLED							
R/W-x							

Table 7-177. Phase start address + 2 Field Descriptions

Bit	Field	Type	Reset	Description
23-22	TIA_SEL	R/W	x	Determines which TIA(s) need to be used for signal acquisition for that phase. If TIA2 needs to be involved in the signal acquisition, make sure EN_DUAL_TIA_GBL bit is set to '1'.
21	PHASE_INT_GPIO	R/W	x	Per-phase interrupt bit for generation of PHASE_OUT interrupt
20	0	R/W	x	Must write 0
19	CONFIG_PHASE_AS_IMP	R/W	x	Configures phase as an Impedance measurement phase
18-17	FIFO_DATA_CTRL_1	R/W	x	Determines data associated with the phase to be stored in the FIFO
16-15	THR_SEL_DATA_CTRL	R/W	x	Determines the data associated with the phase to be used for the Threshold detect check
14	0	R/W	x	Must write 0
13	FIFO_DATA_CTRL_2	R/W		Determines data associated with the phase to be stored in the FIFO
12	STAGGER_LED	R/W	x	Set to '1' to enable the Staggered LED mode for the phase wherein LED ON signal for the phase starts after the completion of the CONV signal for the previous phase
11	FILTER_SET_SEL	R/W	x	Selection of which filter bandwidth set (Set1 or Set 2) to use for the phase
10-8	0	R/W	x	Must write 0
7-0	REG_TWLED	R/W	x	Width of LED ON signal in the phase

7.6.4.4 REG4_PH1: Phase start address + 3**Figure 7-197. Phase start address + 3**

23	22	21	20	19	18	17	16
IOFFDAC_PH_TIA2							
R/W-x							
15	14	13	12	11	10	9	8
USE_DIG_AAC_M_TIA2	USE_ANA_AA_CM_TIA2	UPDATE_BASELINE_TIA2		CF_TIA2		REG_LOOP_NUM_TIA2	
R/W-x	R/W-x	R/W-x		R/W-x		R/W-x	
7	6	5	4	3	2	1	0
RF_TIA2				0		0	
R/W-x				R/W-x		R/W-x	

Table 7-178. Phase start address + 3 Field Descriptions

Bit	Field	Type	Reset	Description
23-16	IOFFDAC_PH_TIA2	R/W	x	Determines current setting for that phase for the Ambient Offset DAC of TIA2 or for the LED Offset DAC of TIA2
15	USE_DIG_AAC_M_TIA2	R/W	x	Associate Digital AACM loop (Loop number as set by LOOP_NUM_TIA2) to cancel input DC current of TIA2
14	USE_ANA_AAC_M_TIA2	R/W	x	Associate an Analog AACM loop operation with TIA2 signal of phase
13	UPDATE_BASELINE_TIA2	R/W	x	Setting this bit to '1' causes the Ambient Offset DAC of TIA2 to be updated to the set value of IOFFDAC_PH_TIA1 when the AACM loop is not enabled. When the AACM loop is enabled, setting this bit to '1' is an indication that this phase is meant to serve as the baseline ambient phase, and that the ambient needs to be acquired in this phase. Setting this bit to '0' uses the baseline value of the ambient from the previous baseline ambient phase.
12-10	CF_TIA2	R/W	x	TIA feedback capacitor (Cf) setting of TIA2 for the phase
9-8	REG_LOOP_NUM_TIA2	R/W	x	This word specifies the Digital AACM Loop number (set as REG_LOOP_NUM_TIA2+1) to be used for that phase for TIA2 (applicable when USE_DIG_AAC_M_TIA2 is set to '1').
7-4	RF_TIA2	R/W	x	TIA gain (Rf) setting of TIA2 for the phase

7.6.4.5 REG5_PH1: Phase start address + 4**Figure 7-198. Phase start address + 4**

23	22	21	20	19	18	17	16
DIG_AACM_LE_D_TIA1	DIG_AACM_LE_D_TIA2	0	0		REG_PH_MASK_FACTOR		
R/W-x	R/W-x	R/W-x	R/W-x		R/W-x		
15	14	13	12	11	10	9	8
			ILED_DRV2				
				R/W-x			
7	6	5	4	3	2	1	0
			ILED_DRV1				
				R/W-x			

Table 7-179. Phase start address + 4 Field Descriptions

Bit	Field	Type	Reset	Description
23	DIG_AACM_LED_TIA1	R/W	x	Automatic LED DC cancellation enable bit (for TIA1 signal)
22	DIG_AACM_LED_TIA2	R/W	x	Automatic LED DC cancellation enable bit (for TIA2 signal)
21-20	0	R/W	x	Must write 0
19-16	REG_PH_MASK_FACTOR	R/W	x	Masking factor setting for the phase – common for TIA1 and TIA2
15-8	ILED_DRV2	R/W	x	LED driver 2 current setting
7-0	ILED_DRV1	R/W	x	LED driver 1 current setting

8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Reference Schematic

Figure 8-1 shows typical device connections for the device operating in the below listed:

- LDO enable mode
- SPI
- External clock input for Mixed clock mode operation. External clock for PRF and internal clock for the timing generation
- 4 photodiodes and 8 LEDs for the PPG
- One lead ECG with 3-electrodes
- ECG high pass filter set to 0.4Hz using external capacitor connected between ECG_CAPP and ECG_CAPM

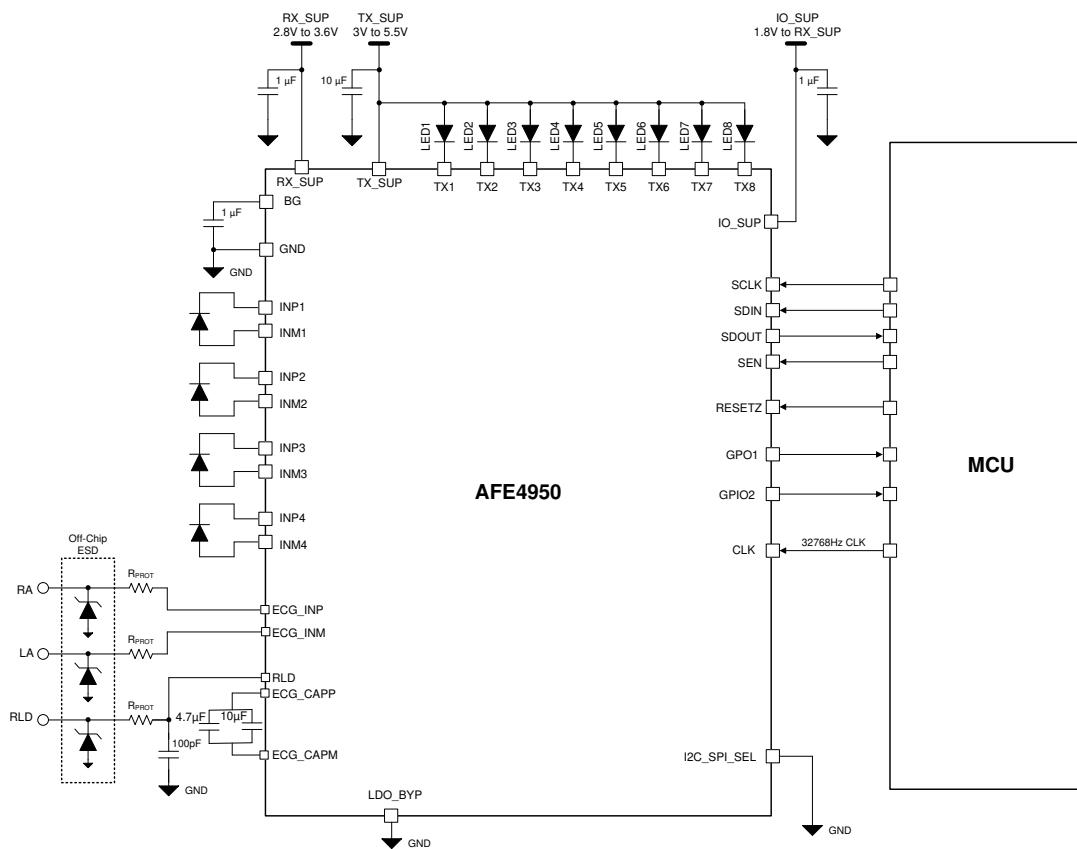


Figure 8-1. Typical Device Connections in SPI mode, LDO Enable Mode and With an External Clock for Mixed Clock Mode Operation

8.1.2 Typical Application - Optical Heart rate monitoring (OHRM)

A typical application of the device is optical heart rate monitoring (OHRM). [Figure 8-2](#) shows an overview of a heart rate monitoring signal chain using the device.

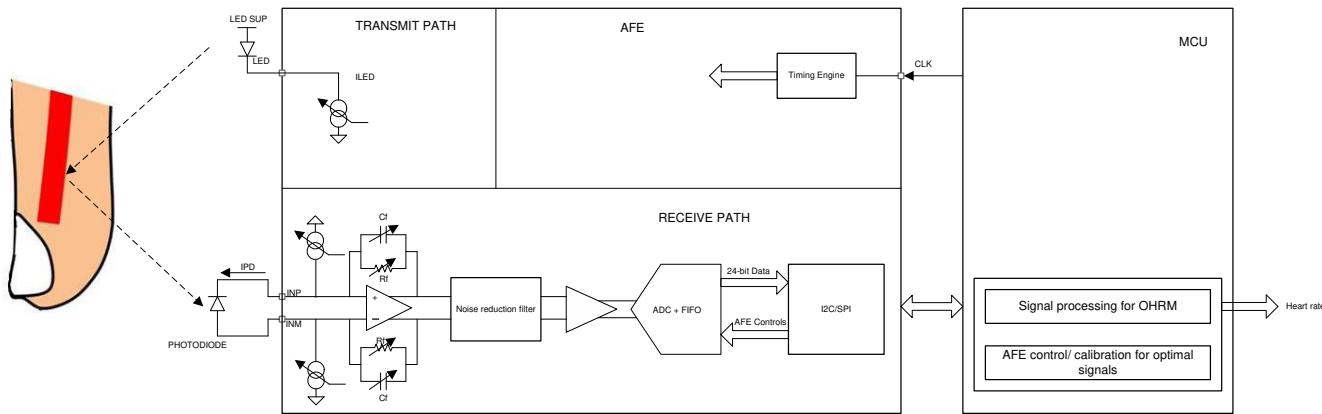


Figure 8-2. Overview of a Typical OHRM System

The OHRM system uses the LED to make a light incident on the human skin. The pulsatile signal reflection is converted to a current using a photodiode (PD) and processed by the Device. The digital equivalent of the PD current is output from the device on an SPI interface and processed by the MCU to extract the heart rate. The signal processing block in the MCU can also calibrate and optimize the device signal chain settings to maximize the signal strength output from the device.

8.1.2.1 Design Requirements - OHRM

[Table 8-1](#) shows the typical design requirements of an OHRM system using the device.

Table 8-1. Design requirements of OHRM system

PARAMETER	EXAMPLE VALUE	COMMENTS
RX_SUP	2 V in LDO enable mode. 1.8 V in LDO bypass mode.	Have enough margin for dc inaccuracy and ripple in the supply driver. The most power-optimal way to drive RX_SUP in a battery-powered application is to use a buck converter to derive a voltage 2 V or higher, and operate the device in LDO enable mode. The LDO internal to the device can be used to reject the tones generated by the buck converter. When operating in LDO bypass mode, an external LDO may be required to achieve the required PSRR and to eliminate output tones.
TX_SUP	Battery voltage	If directly driven from the battery, the LED driver is functional down to the lowest battery voltage where the headroom requirements are satisfied. If driven by the output of a boost converter, choose the boost converter output voltage based on the LED forward voltage and the voltage headroom requirements of the device current driver at the maximum current setting.
IO_SUP	1.8 V	Compatible with the I/O level of the MCU. Can be either the same as RX_SUP or lower than RX_SUP.
PRF	50 Hz	Based on the sampling rate required by the heart rate monitoring algorithm in the MCU. Set by the PRPCT setting.
Output heart rate	0.5 Hz to 4 Hz	Typical range of the human heart rate to be measured

8.1.2.2 Detailed Design Procedure - OHRM

The following important factors are key to extracting the full performance benefit from the device:

1. Good optics including bright LEDs, and high sensitivity photodiodes and their optimal construction and placement .
2. Good mechanical design to reduce the sensitivity to ambient light and motion artefacts
3. An automatic gain control (AGC) loop in the MCU that sets optimal device settings based on the signal conditions

The device has a high dynamic range. This high dynamic range can be very useful in enabling accurate heart rate monitoring even when the pulsatile signal is weak or in the presence of highly interfering ambient and motion artifacts. The control knobs include TIA gain (R_F), TIA bandwidth, LED current (I_{LED}), offset cancellation DAC (I_{OFFDAC}), and the bandwidth setting of the noise-reduction filter (f_{RC}).

The photoplethysmogram (PPG) signal as observed at the output of the AFE is one-sided (either always positive or always negative, depending on the polarity of the PD connection to the AFE inputs) and contains a high dc signal and a small ac signal (which is the signal of interest from which the heart rate frequency can be calculated). If such a signal is directly input to the TIA, then severe underutilization of the device dynamic range results. However, by subtracting a programmable current at the input of the TIA using the offset cancellation DAC, the signal going into the TIA can be centered around zero and a high gain can be applied so that the signal of interest fills a larger fraction of the dynamic range. Operating at higher TIA gains results in a lower input referred noise and better signal quality at the AFE output.. The DC signal in the ambient phase can be automatically cancelled by enabling the AACM loop. The MCU can set an additional Offset DAC increment to cancel out all or a portion of the DC signal in the LED phase or the Automatic LED DC cancellation feature can be used to do this same function.

The DC from the Ambient signal can be automatically cancelled using the Analog AACM loop. In this manner, the control of the Ambient Offset DAC can be automatically handled by the AFE without MCU intervention. In cases where the DC in the LED phase drifts slowly, the LED Offset DAC can be controlled by the AFE using the Automatic LED DC cancellation feature. In that case, the MCU may need to periodically update only the TIA gain and the LED current to achieve an optimum signal level. For example, if the AC signal is weak (as determined by the Heart rate extraction algorithm), the LED current may need to be increased. Also, if the signal level in the LED phase changes fast causing the output to approach saturation (or for the LED Offset DAC to constantly keep getting updated by the Automatic LED DC cancellation), the TIA gain may need to be reduced. Intelligent control involves periodic updating of these parameters to achieve optimum utilization of the full dynamic range of the AFE, while not causing disruption to the acquired signal so often that the heart rate extraction accuracy is compromised.

8.1.2.3 Application Curves - OHRM

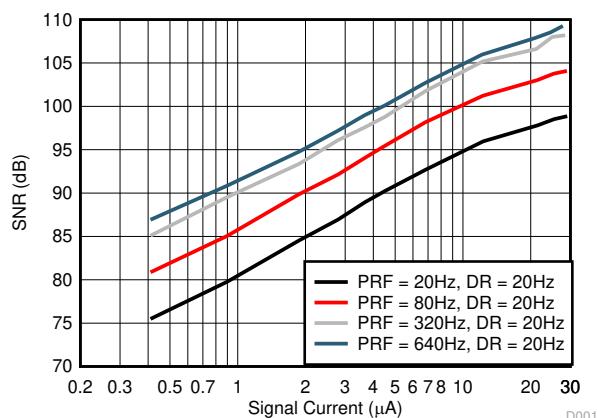


Figure 8-3. Full-system SNR in dB measured over a 0.5-10 Hz bandwidth vs. Input current level across PRF

The SNR required from the system depends on the quality of the PPG signal for a given use case. When the user is at rest, the signal quality is usually good and SNR may be traded off for reduced power consumption (lower LED current, lower PRF, etc.). When used under high motion conditions, the PPG signal quality may be poorer and may be affected by motion artefacts. Switching to signal chain settings that give higher SNR may be essential in such scenarios.

Figure 8-3 shows the Signal to Noise ratio (SNR) measured as a function of input signal current. The SNR is defined by the ratio of the input signal current and the input referred current noise. The AFE is hooked up to a LED and PD (indicative of the complete system). The light from the LED is made to reflect on to the PD, which generates the indicated level of input signal current. By adjusting the LED current up to 250 mA, the signal current from the PD is swept up to ~30 μA . The LED Offset DAC is set to cancel out the DC level of the input signal at each setting so that the AFE output is roughly zero. The TIA gain is set to 250 KOhm. The output noise from the AFE (in the LED minus Ambient data) is measured and converted to an input referred current noise. This noise current is inclusive of the noise from all the components in the system - the optical noise from the LED and PD as well as the electrical noise from the AFE transmit and receive paths, including the Offset DAC. The 4 curves correspond to PRF settings of 20 Hz, 80 Hz, 320 Hz and 640 Hz. In each case, the output data rate is lowered to 20 Hz by appropriate control of the decimation factor (no decimation, Decimation by 4, Decimation by 16 and Decimation by 32 respectively). The noise is computed in the frequency band of 0.5 Hz to 10 Hz from the FFT of the decimated data stream, and is referred to the AFE input as a current noise. The SNR is computed in dB by referring the rms value of the input-referred current noise to the input signal current from the PD set for the measurement. By operating at higher PRF, it can be seen that the noise in the 0.5 Hz to 10 Hz frequency band can be reduced. For this plot, an LED ON width (and SAMP width) of $15 \times t_{TE}$ (~117 μs) is used, A filter pre-charge width of $4 \times t_{TE}$ (~31 μs), filter pre-charge bandwidth of 25 kHz, and filter fine settling bandwidth of 2.5 kHz is used.

8.1.3 Typical Application - ECG

8.1.3.1 Design Requirements - ECG

An ECG signal acquisition involves interfacing 2 or 3 electrodes to the AFE. Figure 8-4 through Figure 8-6 shows a few configurations for interfacing 2 or 3 electrodes to the ECG pins.

Configurations for interfacing 2 or 3 electrodes to the ECG pins.

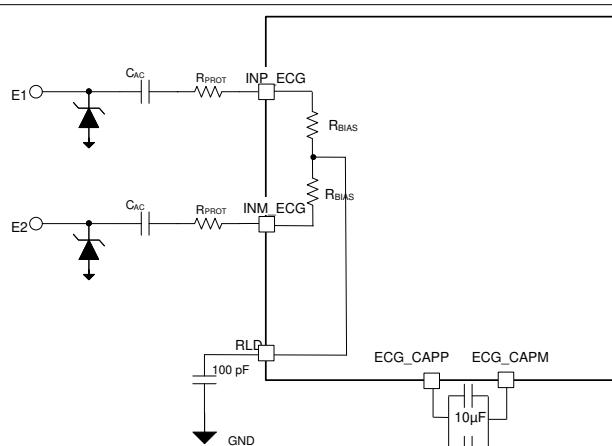


Figure 8-4. 2 Electrodes with AC Coupling

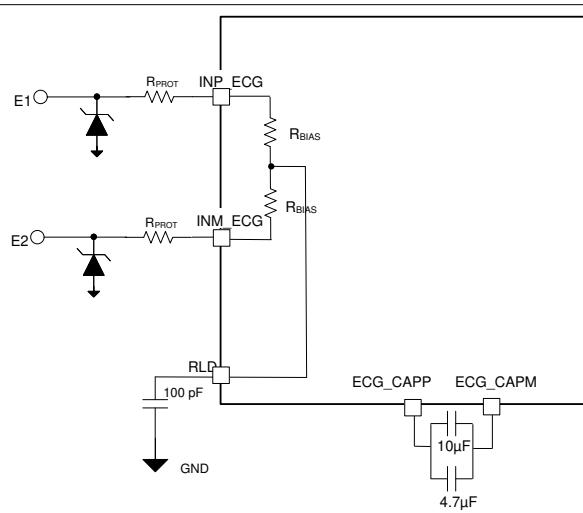


Figure 8-5. 2 Electrodes with DC Coupling

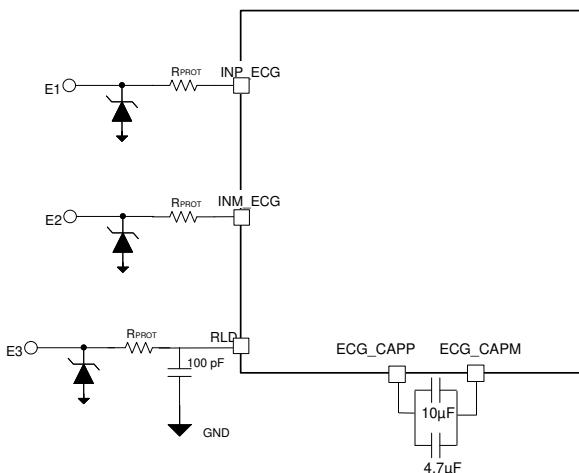


Figure 8-6. 3 Electrodes with DC Coupling

One of the important design requirements is to acquire good quality ECG signals in scenarios where there is a high contact impedance of the electrode-to-skin in the ECG signal band. For the choice of electrodes, a value of the worst-case electrode contact impedance needs to be determined.

Another important system parameter to establish is the AC and DC shunt impedance at the ECG input pins on account of the PCB components and routings. The electrodes, protection diodes, intentional capacitors and PCB routings all introduce shunt capacitances at the ECG input pins. The effect of these is to lower the input impedance of the ECG receiver which can lead to an attenuation of the ECG signal and a reduction in the CMRR. A large input capacitance is also undesirable as a large input capacitance reduces the sensitivity of AC lead on detection.

8.1.3.2 Detailed Design Procedure - ECG

This section describes some careabouts for the design of an ECG acquisition system. When using dry electrodes, the skin-electrode contact impedance plays a significant role in the quality of the ECG signals. Excessively high contact impedance can lead to attenuated signal, higher noise, and lower CMRR. DC coupling the electrodes to the ECG input pins, and using a separate 3rd RLD electrode to drive the body potential helps achieve the highest input impedance from the ECG front end and also helps improve the CMRR.

When used in environments where the electrodes can pick up strong high-frequency common mode interference, TI requires to place additional capacitors C_{IN_ECG} (approximately few 10 s of pF) at the ECG input pins (that is between INP_ECG and ground, and between INM_ECG and ground). The combination of R_{PROT} and C_{IN_ECG} forms a low-pass filter to filter out these interferences. Example values are $R_{PROT} = 100 \text{ k}\Omega$, and $C_{IN_ECG} = 20 \text{ pF}$.

Table 8-2 lists some careabouts for each configuration.

Table 8-2. Careabouts for ECG Electrode Configurations

CAREABOUT	2 electrodes with AC coupling	2 electrodes with DC coupling	3 electrodes with DC coupling
ECG input pin bias set by	R_{BIAS} resistors (Example 200 M Ω)		RLD electrode driving body
RLD amplifier configuration	Unit gain buffer driving fixed voltage		Feedback buffer
Input HPF scheme	Internal HPF at 0.5 Hz External HPF corner set by C_{AC}/R_{BIAS}		Internal HPF at 0.5 Hz
CMRR	Lower CMRR		Best CMRR

Operating at the higher INA gain helps improve the noise but limits the input differential swing that can be supported. Operating at a higher ECG sampling rate also lowers the noise floor and results in a lower integrated noise in the ECG signal band of interest. While operating at high sampling rates, the decimation filter can be enabled to lower the output data rate while still retaining the low noise in the signal band.

The lead on detect current must be chosen based on the worst case impedance that needs to be considered as valid leads on, and the detection thresholds need to be set appropriately.

8.1.3.3 Application Curves - ECG

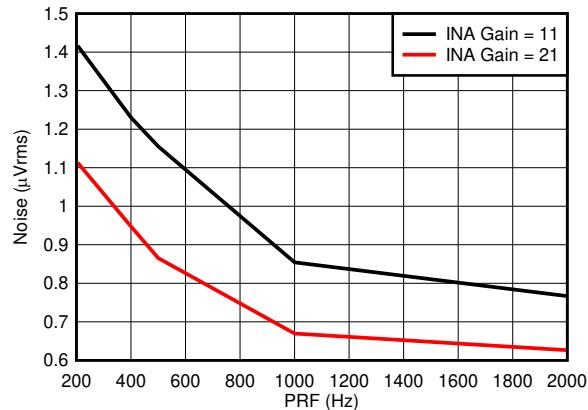


Figure 8-7. Input referred noise of ECG signal chain in 150 Hz bandwidth versus PRF

Figure 8-7 plots the input referred noise of the ECG signal chain in 150 Hz bandwidth versus PRF at different INA gains. The noise in the 150 Hz bandwidth gets lower as the PRF is increased since the noise gets spread over a wider Nyquist bandwidth. Also the noise reduces as the INA gain is increased. In addition to the noise from the AFE as shown in this plot, there could be additional sources of noise associated with the ECG signal acquisition. For example, in a system using dry electrodes, the large electrode-skin contact impedance could be a significant noise contributor.

8.1.4 Application Curves

[Figure 6-3](#) shows the Signal to Noise ratio (SNR) measured as a function of input signal current. The SNR is defined by the ratio of the input signal current and the input referred current noise. The AFE is hooked up to a LED and PD (indicative of the complete system). The light from the LED is made to reflect on to the PD, which generates the indicated level of input signal current. By adjusting the LED current up to 250 mA, the signal current from the PD is swept up to approximately 30 μ A. The LED Offset DAC is set to cancel out the DC level of the input signal at each setting so that the AFE output is roughly zero. The TIA gain is set to 250 KOhm. The output noise from the AFE (in the LED minus Ambient data) is measured and converted to an input referred current noise. This noise current is inclusive of the noise from all the components in the system - the optical noise from the LED and PD as well as the electrical noise from the AFE transmit and receive paths, including the Offset DAC. The 4 curves correspond to PRF settings of 20 Hz, 80 Hz, 320 Hz and 640 Hz. In each case, the output data rate is lowered to 20 Hz by appropriate control of the decimation factor (no decimation, Decimation by 4, Decimation by 16 and Decimation by 32 respectively). The noise is computed in the frequency band of 0.5 Hz to 10 Hz from the FFT of the decimated data stream, and is referred to the AFE input as a current noise. The SNR is computed in dB by referring the rms value of the input-referred current noise to the input signal current from the PD set for the measurement. By operating at higher PRF, the noise in the 0.5 Hz to 10 Hz frequency band can be reduced. For this plot, an LED ON width (and SAMP width) of $15 \times t_{TE}$ (approximately 117 μ s) is used, A filter pre-charge width of $4 \times t_{TE}$ (approximately 31 μ s), filter pre-charge bandwidth of 25 kHz, and filter fine settling bandwidth of 2.5 kHz is used.

[Figure 6-4](#) shows the input referred noise of the Receiver for different settings of the SAMP width across different TIA gains. For each SAMP width setting, the TIA time constant and Filter settings are chosen as per the guidelines in [Table 7-39](#). The measurement is done with zero input current signal. The output noise from the AFE is measured and converted to input referred noise current (the transfer function between the output voltage noise and input referred current noise is determined by the TIA gain used for the measurement). At higher TIA gains, the input referred current noise from the AFE receiver reduces. Similarly, at higher LED ON times, the filter can be operated at a lower bandwidth. This too results in a lowering of the input-referred noise. This plot illustrates the two differentiating features of the AFE architecture - the benefits of input DC cancellation which allow operating at high TIA gain, and the noise bandwidth reduction resulting from the filter.

[Figure 6-5](#) shows the input referred current noise of the receiver versus Number of ADC Averages (NUMAV). The multiple curves correspond to different TIA gain settings. The SNR improves with higher number of ADC averages but the improvement becomes marginal for the higher TIA gains. This is because the contribution of the ADC noise to the total noise becomes less significant at higher TIA gain settings.

[Figure 6-6](#) corresponds to the same measurement as [Figure 6-5](#). The SNR in dBFS is calculated as the input referred noise current referred to the full scale input current which is a function of the TIA gain. For example, at a TIA gain setting of 250 k Ω , the full scale input current is 2 μ A. The trend of the SNR reducing with increasing TIA gain is explained by the fact that the full-scale input current keeps inversely reducing as the TIA gain is increased. However, the input-referred noise current does not reduce at the same rate. This plot gives an estimate of the SNR that can result if the Offset Cancellation DAC was not used to extend the input current range for a given TIA gain setting.

[Figure 6-7](#) plots the crosstalk from the signal on TIA1 on to the signal on TIA2 in a Dual receive phase. A sine wave of 10 Hz frequency is made input to TIA1 and a zero input to TIA2. By computing the power of the 10 Hz tone at the TIA2 output, and referring to the input signal on TIA1, the crosstalk is computed.

[Figure 6-8](#) shows the effect of crosstalk between phases where the SAMP signal of a phase overlaps the CONV signal of the previous phase. Such an overlap results in a crosstalk of a phase to the previous phase. The plot is generated by presenting a sine wave signal on the second phase and looking at the level of coupling of that signal on the first phase (with zero input on the first phase). This can be achieved by connecting the TIA inputs to INP1,INM1 in the first phase with zero signal on INP1,INM1; and by connecting the TIA inputs to INP2, INM2 in the second phase with a full scale signal on INP2, INM2.

[Figure 6-9](#) is generated in a similar manner to [Figure 6-8](#), but with non-overlap between the SAMP signal and CONV signals of successive phases. Such a non-overlap can be achieved either by setting the STAGGER_LED

bit of the second phase to '1'. As can be seen, the level of crosstalk becomes extremely low with non-overlap between the SAMP and CONV phases.

[Figure 6-10](#) illustrates the Ambient Offset DAC current across the decimal equivalent of the code as set by the I_OFFSETDAC* register control.

[Figure 6-11](#) illustrates the LED Offset DAC current across the decimal equivalent of the code as set by the I_OFFSETDAC* register control.

[Figure 6-12](#) plots the RX_SUP current versus PRF for different settings (internal oscillator/ external clock modes and LDO enabled/ bypassed) when operating in the PPG mode. As the PRF is reduced, the device spends more time in the Deep sleep phase which results in a reduction in the RX_SUP current at the lower PRF settings.

[Figure 6-13](#) illustrates the LED current across the decimal equivalent of the LED code as set by ILED* register control. The currents are plotted for the 1X, 2X and 2.5X modes, with only one of the two drivers turned on.

[Figure 6-14](#) shows the LED current across the decimal equivalent ILED code for the Dual driver case.

[Figure 6-15](#) and [Figure 6-16](#) illustrates the LED current as a function of the voltage at the TX pin for the single driver case. The voltage at the TX pin is swept by connecting a load resistor from the TX pin to LED_SUP (a supply different from TX_SUP) and changing the voltage of LED_SUP to control the voltage on the TX pin. The voltage headroom required by the driver can be determined by the TX pin voltage beyond which the current curve becomes flat. While [Figure 6-15](#) corresponds to a TX_SUP voltage of 5 V, [Figure 6-16](#) corresponds to a TX_SUP voltage of 3 V.

[Figure 6-17](#) and [Figure 6-18](#) illustrates the full-scale LED current versus the voltage at the TX pin for the Dual driver case at TX_SUP voltage of 5 V and 3 V respectively.

[Figure 6-19](#) shows the input referred current noise across the RX_SUP voltage in the LDO bypass mode. The 3 curves correspond to different operating temperatures.

[Figure 6-20](#) shows the Frequency drift of the internal oscillator across temperature on a sample unit.

[Figure 6-21](#) shows the step response of the Analog AACM loop.

[Figure 6-22](#) shows the response of the Digital AACM loop to a transient waveform.

[Figure 6-23](#) illustrates the effect of a tone on the RX_SUP pin when operating in the LDO Bypass mode. The amplitude of the tone is set to 50 mVpp and the frequency is swept. The TIA gain is set to 500 Kohm and the input current for the four different curves is adjusted so as to result in output DC levels of 0.25 V, 0.5 V, 0.75 V and 1 V respectively. The output tone as a function of the frequency of the tone on RX_SUP is plotted.

[Figure 6-24](#) illustrates the output tone due to the 50 mVpp tone on RX_SUP around different levels of the RX_SUP voltage. The device is operated in LDO bypass mode.

[Figure 6-25](#) shows the output tone (with a 50 mVpp tone on RX_SUP) when the AFE is operated with the LDO enabled.

[Figure 6-26](#) illustrates the effect of a tone on the TX_SUP pin when the LED driver current is set to 50 mA (and a single driver is turned on). The amplitude of the tone on TX_SUP is set to 50 mVPP and the frequency is swept. The PSRR is defined as the equivalent tone on the LED driver current (deduced from the tone at the receiver output) referred to the current setting of 50 mA. The PSRR curve is plotted for different values of LED driver headroom, which is measured as the lowest voltage at the TX pin during the transient wave form resulting from the tone on TX_SUP.

[Figure 6-27](#) plots the ECG signal chain input referred noise versus time measured at PRF = 1000 Hz, INA gain = 21. The output of the AFE is filtered with 150 Hz off-chip low pass filter.

[Figure 6-28](#) plots the ECG signal chain input referred noise histogram at PRF = 1000 Hz, INA gain = 21. The output of the AFE is filtered with 150 Hz off-chip low pass filter.

[Figure 6-29](#) plots the ECG signal chain input referred noise versus time measured at PRF = 500 Hz, INA gain = 21. The output of the AFE is filtered with 150 Hz off-chip low pass filter.

[Figure 6-30](#) plots the ECG signal chain input referred noise histogram at PRF = 500 Hz, INA gain = 21. The output of the AFE is filtered with 150 Hz off-chip low pass filter.

[Figure 6-31](#) plots the input referred noise of the ECG signal chain in 150 Hz bandwidth versus PRF at different INA gains. The noise in the 150 Hz bandwidth gets lower as the PRF is increased since the noise gets spread over a wider Nyquist bandwidth. Also the noise reduces as the INA gain is increased.

[Figure 6-32](#) plots the input referred noise of the ECG signal chain in 150 Hz bandwidth versus PRF at different input source impedances $51 \text{ k}\Omega||47 \text{ nF}$ and $620 \text{ k}\Omega||4.7 \text{ nF}$ with a lead-on detection current of 12.5 nA enabled. The noise in the 150 Hz bandwidth gets lower as the PRF is increased since the noise gets spread over a wider Nyquist bandwidth.

[Figure 6-33](#) plots the Common mode rejection ratio (CMRR) of the ECG signal chain as a function of frequency with 2- and 3-electrode configurations. The CMRR is a measure of the extent to which a common mode tone applied equally on the ECG input pins appears as a differential output. The common mode tone is coupled through a 100 pF capacitor to the input pins. With the RLD loop enabled (3-electrode operation), the RLD buffer provides an additional suppression of the common mode signal. The input impedance in 3-electrode mode is much higher than the input impedance in 2-electrode which has a differential input impedance of $400 \text{ M}\Omega$ due to the bias resistor. 3-electrode configuration provides a very high CMRR due to common mode suppression by the RLD feedback loop and high input impedance.

[Figure 6-34](#) plots the differential input impedance of the ECG inputs as a function of the signal frequency. The reduction of the input impedance with increasing signal frequency is because of the capacitive component of the impedance.

[Figure 6-35](#) plots the amplitude of the tone at the ECG output (referred to the input of the AFE) for a 50 mVpp tone on RX_SUP as a function of frequency. The measurement is done with the LDO bypass mode, and the different curves correspond to different RX_SUP voltages.

[Figure 6-36](#) plots the amplitude of the tone at the ECG output (referred to the input of the AFE) for a 50 mVpp tone on RX_SUP as a function of frequency with the internal LDO enabled.

[Figure 6-37](#) shows the ECG signal chain response to a 2 mVpp, 10 Hz sinusoidal signal in the presence of a 1 ms pulse of amplitude 200 mV, akin to a pacemaker pulse. The ECG high pass filter corner was set to 0.4 Hz by an appropriate choice of C_{HPF} .

[Figure 6-38](#) shows the ECG signal chain response to 40 ms and 200 ms triangular pulse train of 1.5 mVpp amplitude. The ECG high pass filter corner was set to 0.4 Hz.

[Figure 6-39](#) show the fast recovery of ECG signal chain high pass filter to a differential input offset step of 200 mV. Note that the high pass filter recovers in less than 100 ms to a differential offset step.

[Figure 6-40](#) shows the RX_SUP current versus PRF in the ECG-only mode.

8.2 What to Do and What Not to Do

8.2.1 Important Guidelines

The following points are a collection of important considerations related to using the AFE4950 and are summarized as a handy reference:

1. Avoid extended operation of the device where some supplies are on and others are off. Such operation can result in spurious currents; see the [Section 8.3](#) for additional guidelines related to power supplies.
2. Always issue a hardware reset after the RX_SUP and IO_SUP supplies are stabilized and before writing into the registers. A reset is also required after the device comes out of the hardware power down mode. The reset causes all registers to get reset to their default values, and also reads and registers the values of internal OTPs which store device parameter trims.
3. If using a software reset to clear the registers, write register 00h first with the SW_RESET bit set to 1. Then, after a delay, again program the other bits in register 00h with the SW_RESET bit set to 0.
4. Use decoupling capacitors (1 μ F or higher) placed close to the device to filter noise on RX_SUP and IO_SUP. An even higher value (Example: 10 μ F) may be required in TX_SUP.
5. The voltage level used for IO_SUP must be the same as the I/O voltage level for the MCU. LDO_BYP and I2C_SPI_SEL must be referred to the RX_SUP rail.
6. When in power-down mode (PWDN), the external CLK can be shut off to avoid any switching current.
7. Ensure that LED_ON duty cycles do not exceed rated absolute maximum specifications
8. If system-level ESD requirements exceed the device-level ESD specifications, additional external protection diodes may be required.
9. The ECG circuitry may require additional components like protection resistors and ESD diodes.

Below are a set of guidelines for maximizing the performance from the AFE.

1. Use Ambient cancellation (either through MCU control or using the Analog AACM loop) to cancel the Ambient current right at the AFE input using the Ambient Offset DAC.
2. If there is a significant DC from LED, use the LED Offset DAC to remove the LED's DC. Such cancellation could be done either through MCU control or by enabling Automatic LED DC cancellation.
3. With both Ambient and LED DC suppressed, use a high gain setting (R_f) to reduce the AFE's input referred noise. A setting of 250 k Ω or lower might be sufficient to achieve the required SNR for most scenarios. Also use the highest value of C_f .
4. Use the lowest full-scale range of the Offset DAC (taking into account the +/-20% variation) that will be sufficient to cancel the Ambient current. For example, if the Ambient DC is less than 10 μ A, then set IFS_AMB_OFFSETDAC to operate in the 1X mode. The extra noise added by the Offset DAC is lowest in the 1X mode.
5. Operating the LED driver with the highest headroom (V_{HR}) reduces the noise contribution from the LED driver. So for the same current setting, operating in the 2.5X mode gives the lowest noise.
6. Defining an ambient phase and digitally subtracting the Ambient from the LED phase is highly recommended. This subtraction helps suppress ambient tones and also helps cancel low frequency noise and drifts internal to the AFE. Closer the position of the ambient and LED phases, better is the suppression of the ambient tones. Defining and combining multiple ambient phases can result in improved ambient cancellation.
7. Lowering the filter bandwidth setting provides more aggressive noise bandwidth limitation for noise from the sensor and the receiver.
8. Ensure that none of the signal phases saturates the signal chain. Performance of the receiver in phases immediately following a saturated phase could be worse than the expected performance. Ambient cancellation can also degrade with saturation in channels adjacent to the signal phases of interest.
9. The differential connection of the PD to the AFE causes the PD to operate close to zero bias. However, a slight forward bias may be developed across the PD especially in the presence of a signal current in the PD. It is therefore important to use a PD that has a relatively flat sensitivity between zero bias and ~150 mV of forward bias.

8.3 Power Supply Recommendations

The power supply recommendations for AFE4950 are listed below:

1. Choose the voltages on the supply rails based on the ranges listed in the *Recommended Operating Conditions* section. Ensure that the voltages never exceed the values listed in the *Absolute Maximum Ratings* table.
2. Follow the supply ramp-up sequence suggested in the [Section 8.3.1](#) while powering up the device, and while using the hardware power-down mode. A failure to follow the suggested sequence could result in an erroneous operation of the device.
3. Never operate the device for any extended duration of time with any one of the supplies switched ON (or OFF) and the other two supplies switched OFF (or ON).
4. Refer to the PSRR plots in the [Section 6.11.1](#) to determine the maximum allowed ripple in the RX_SUP rail. Select between the LDO enable and LDO bypass modes based on the extent of ripple on the RX_SUP rail. Use appropriate values of decoupling capacitors on all the supply rails.
5. If using a boost converter to drive the TX_SUP rail, check if the PSRR of the LED driver is within acceptable limits based on the switching frequency of the boost converter and the estimated ripple.

8.3.1 Power supply ramp-up

The suggested sequence of operations while powering up the device and entering/ exiting hardware power-down mode is illustrated in [Figure 8-8](#). The corresponding parameters are listed in [Table 8-3](#).

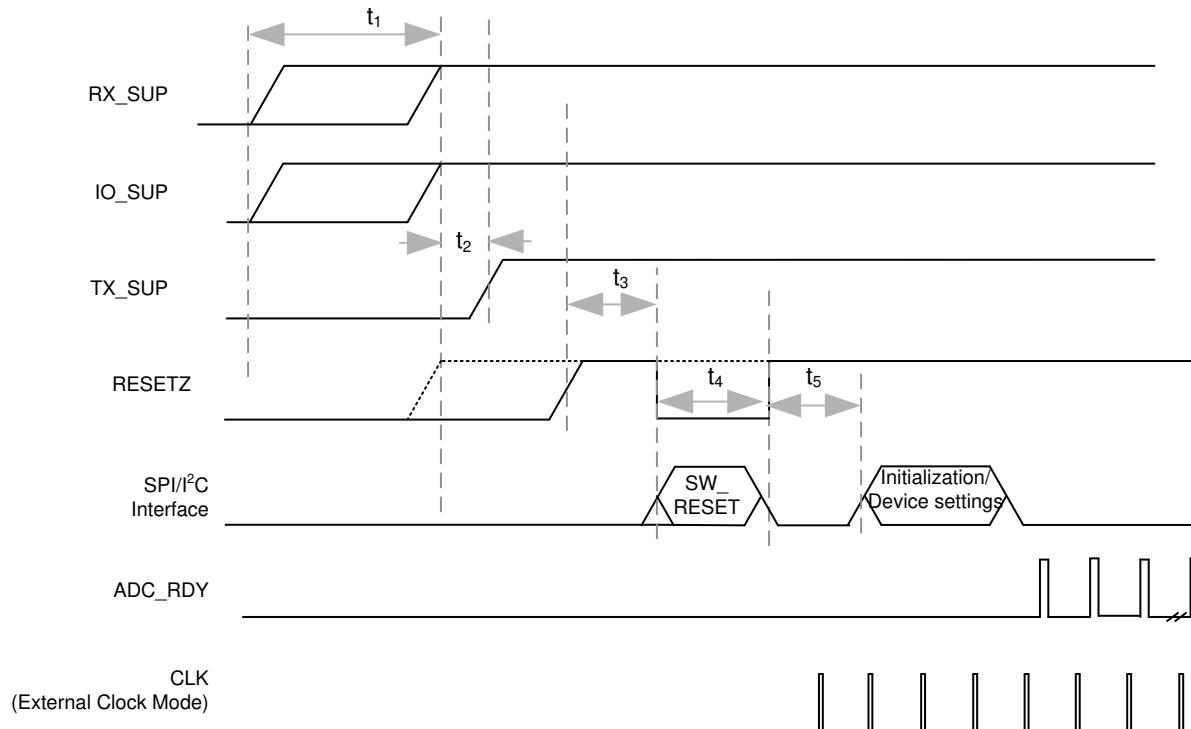


Figure 8-8. Suggested Sequence of Operations while Powering up the Device

Table 8-3. Parameters associated with powering up the device and entering/ exiting hardware power-down mode

		VALUE
t ₁	RX_SUP/IO_SUP Ramp-up window– these two supplies may ramp up in sequence during this window	Keep t ₁ as small as possible (for example, < 100 ms)
t ₂	Time between the end of the RX_SUP/IO_SUP Ramp-up window and the ramp-up of TX_SUP	Keep t ₂ small and no more than 100 ms
t ₃ ⁽¹⁾	Time between RESETZ getting pulled high for the first time (after power up) and applying a reset to the device	> 1 ms
t ₄ ⁽²⁾	Width of the active low hardware reset pulse	Between 25 μ s and 50 μ s
t ₅	Time between applying a reset (software or hardware reset) and writing registers for Device initialization and configuration	>1 ms

(1) RESETZ can be pulled high simultaneously with, or any time after IO_SUP has been pulled high. If RESETZ has been pulled high inside the t₁ window, then the start point for the t₃ delay is the end point of the t₁ window.

(2) t₄ parameter is applicable only in the case of Hardware reset. It is not a relevant parameter if the reset is done using the software reset register bit

8.3.2 Initialization Set Up

8.3.2.1 Initialization sequence after power up

After the AFE has been powered up with all supplies switched on, use the following sequence to initialize the device:

1. Wait for 1 ms.
2. Apply a reset (software or hardware).
3. Write PAGE_SEL to '1'.
4. Write the per-phase register settings in Page 1 of the register map. REG_NUMPHASE need not be set prior to this, however, *all the per-phase registers associated with the intended number of phases (1... NUMPHASE) should be written*. This applies even to per-phase registers which do not contain functions intended for use, and which need to have all bits set to zero. Per-phase registers do not have default values and do not get reset. Therefore, not writing all the per-phase registers explicitly can result in one or more bits have unintended values.
5. Write PAGE_SEL to '0'.
6. Program the registers in Page 0. The registers can be programmed in any order with the exception that register with address 1Dh should be written at the end (Step 8).
7. It is recommended that the Interrupt service routine in the MCU is enabled to service interrupts from the AFE only after Step 6, to prevent the MCU from responding to a spurious interrupt that could have come during device power up or during the middle of the initialization sequence.
8. Program register 1Dh, programming the PRPCT to the desired PRF setting, and simultaneously setting the TIMER_ENABLE and PRF_COUNTER_ENABLE bits to '1'. With register 1Dh thus programmed, the timing engine starts running and the FIFO starts off in an initialized state.

This initialization sequence needs to be followed after every power-up cycle of the device and every time the device comes out of hardware powerdown. The same device initialization sequence can be performed when coming out of the software power down mode. However, during software power down, the registers retain their state and need not be reprogrammed if there is no change required in their values.

8.3.2.2 Sequence to reconfigure the FIFO

If PRF or the number of signal phases in a PRF needs to be changed, or if any of the FIFO configuration needs to be changed or if the FIFO needs to be reset and fresh signal needs to be acquired in the FIFO, the FIFO needs to be first disabled (set FIFO_EN to '0'). To re-enable the FIFO, follow the below sequence:

1. Program register 1Dh, setting bits TIMER_ENABLE AND PRF_COUNTER_ENABLE to '0'.
2. Program register 00h in Page 0, setting TM_COUNT_RST bit to '1' (with FIFO_EN still set to '0').
3. Make changes to any of the parameters in Page 0 or Page 1 except registers with address 1Dh and 00h in Page 0.
4. Program register 00h in Page 0, setting FIFO_EN to '1' and TM_COUNT_RST to '0'.
5. Program register 1Dh, programming the PRPCT to the desired PRF setting, and simultaneously setting the TIMER_ENABLE and PRF_COUNTER_ENABLE bits to '1'. With register 1Dh thus programmed, the timing engine once again starts running and the FIFO starts off in an initialized state.

This initialization sequence can also be followed every time the device comes out of software powerdown mode.

The operation of the FIFO immediately after enabling it is illustrated in [Figure 8-9](#).

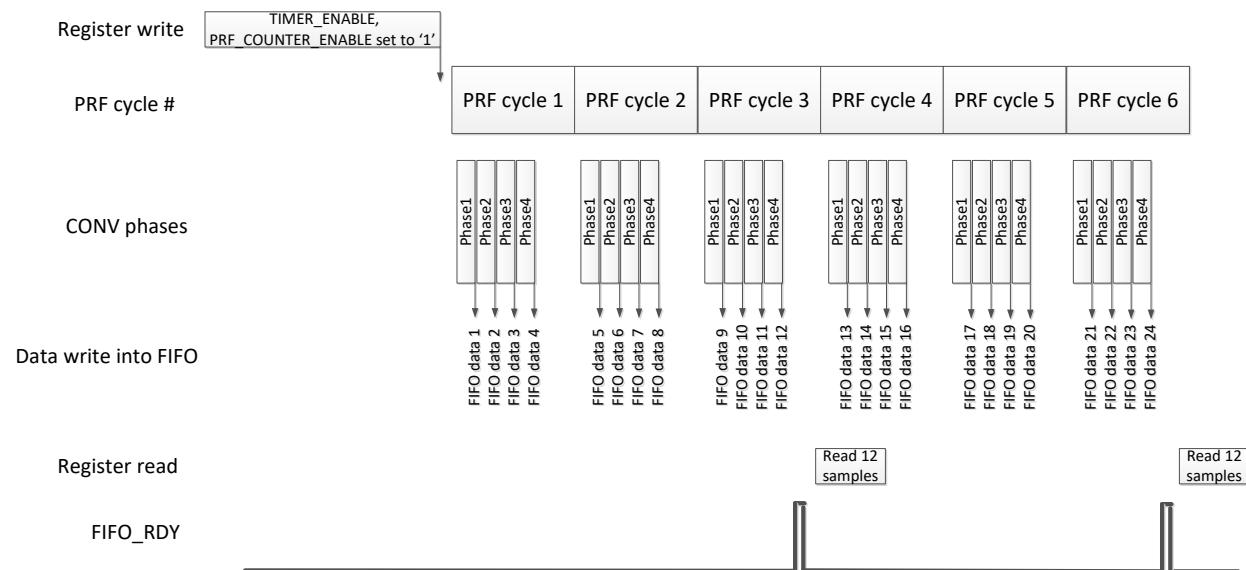


Figure 8-9. Timing of FIFO Operation Every Time the FIFO is Freshly Enabled (NUMPHASE = 4, WM_FIFO=12)

8.3.2.3 Sequence to change any signal chain parameters

If any of the parameters related to the signal chain (like Rf, Cf, LED current, offset DAC and so on) are required to be changed on-the-fly during the device operation and if these changes do not involve any parameters determining the FIFO data streaming, then follow the below guidelines:

1. Wait for the FIFO_RDY interrupt.
2. On receiving the FIFO_RDY interrupt, change the signal chain parameters (program only the registers that need change).
3. Complete all the programming within the deep sleep window before the start of the next PRF cycle.

8.4 Layout

8.4.1 Layout Guidelines

The key layout guidelines are:

1. TX pins are fast-switching lines and must be routed away from sensitive lines (such as the ECG and PPG inputs).
2. The device can draw high-switching currents from the TX_SUP pin. A decoupling capacitor must be electrically close to the pin. The extra routing drops in the path of the LEDs should be kept low to minimize resistive losses.
3. The routing from the ECG electrodes to the ECG input pins of the AFE are extremely sensitive and should be shielded from any switching signals.

8.4.2 Layout Example

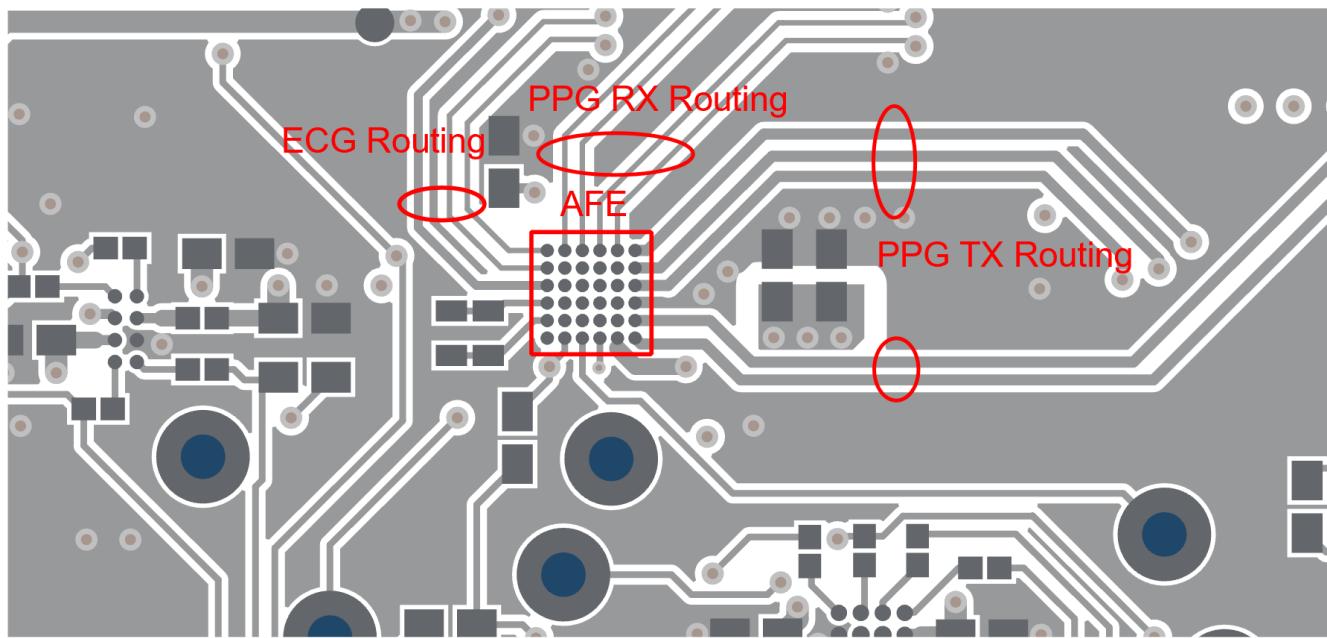


Figure 8-10. Example Layout

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Package Option Addendum

10.1.1 Packaging Information

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁴⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(5) (6)}
AFE4950YBGR	PREVIEW	DSBGA	YBG	36	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-20 to 85 °C	AFE4950
AFE4950YBGT	PREVIEW	DSBGA	YBG	36	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-20 to 85 °C	AFE4950

- (1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

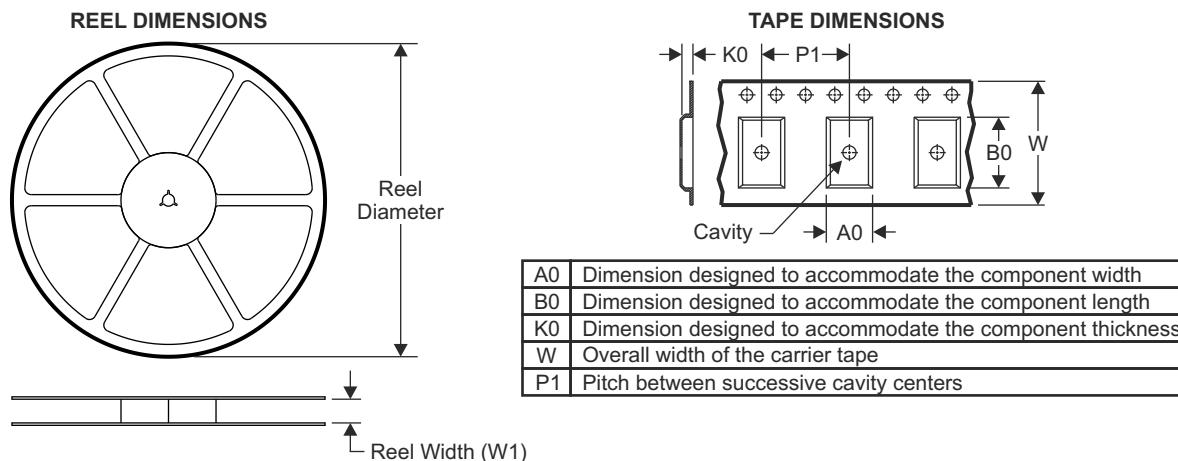
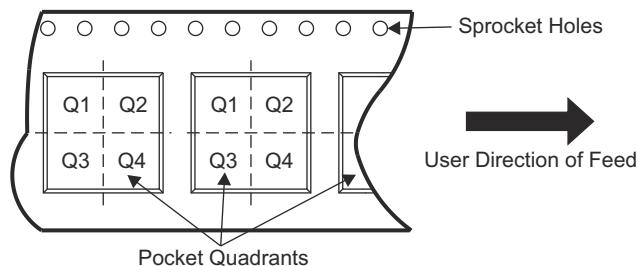
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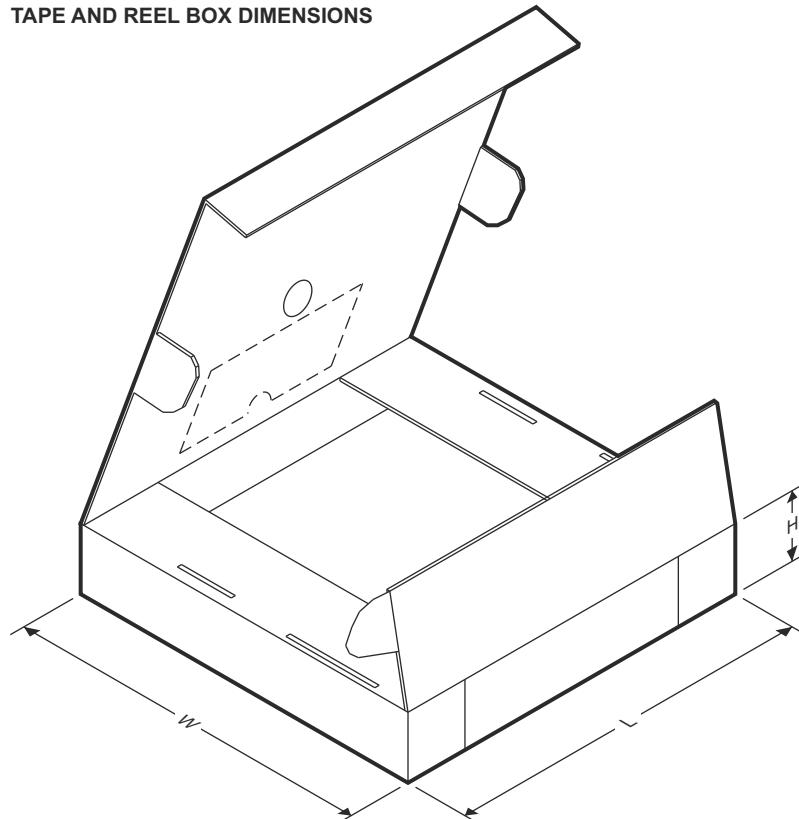
AFE4950

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10.1.2 Tape and Reel Information

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

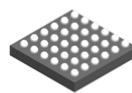
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE4950YBGR	DSBGA	YBG	36	3000	330.0	12.4	2.64	2.8	0.74	8.0	12.0	Q1
AFE4950YBGT	DSBGA	YBG	36	250	330.0	12.4	2.64	2.8	0.74	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

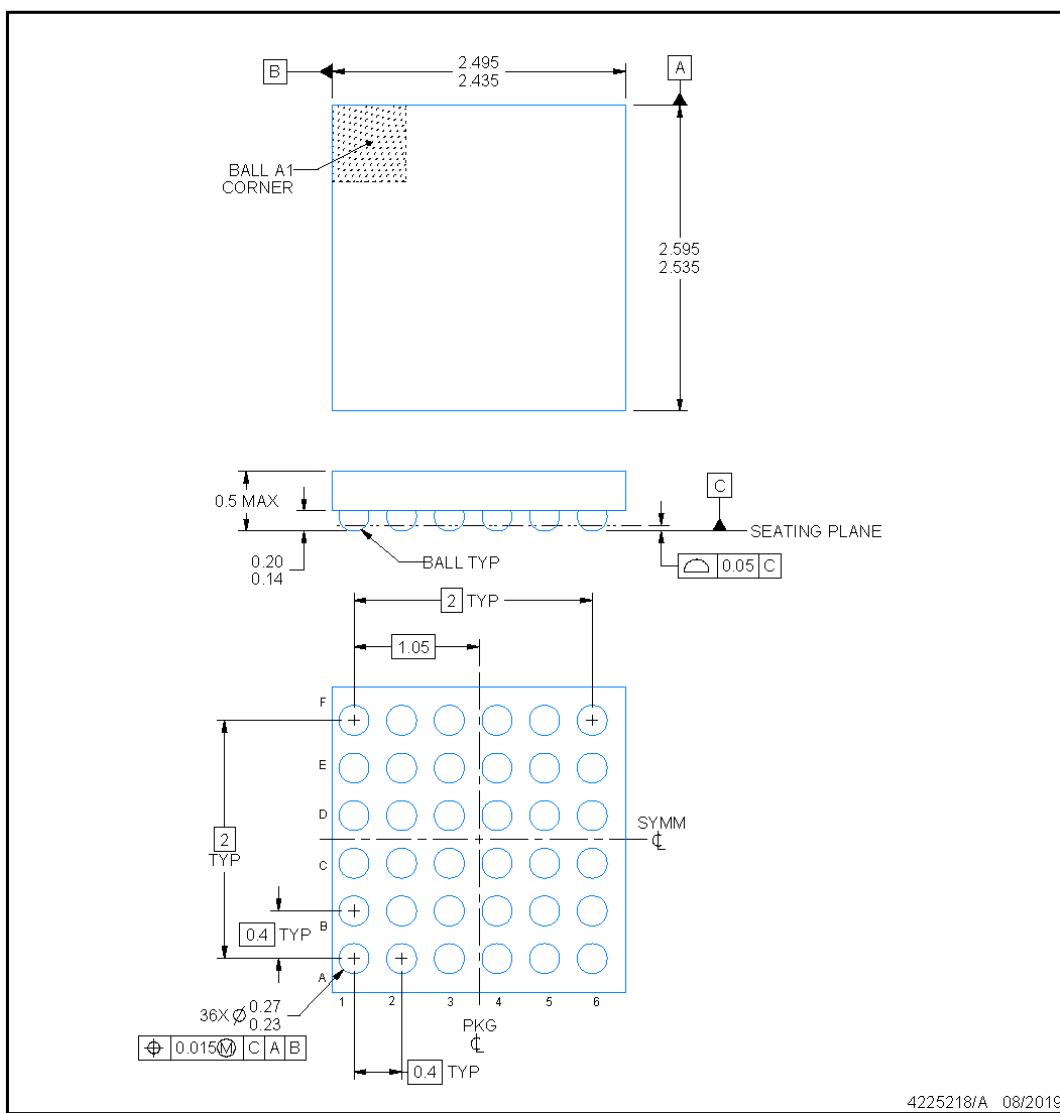
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE4950YBGR	DSBGA	YBG	36	3000	345.0	365.0	55.0
AFE4950YBGT	DSBGA	YBG	36	250	345.0	365.0	55.0

AFE4950

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YBG0036-C01**PACKAGE OUTLINE****DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY

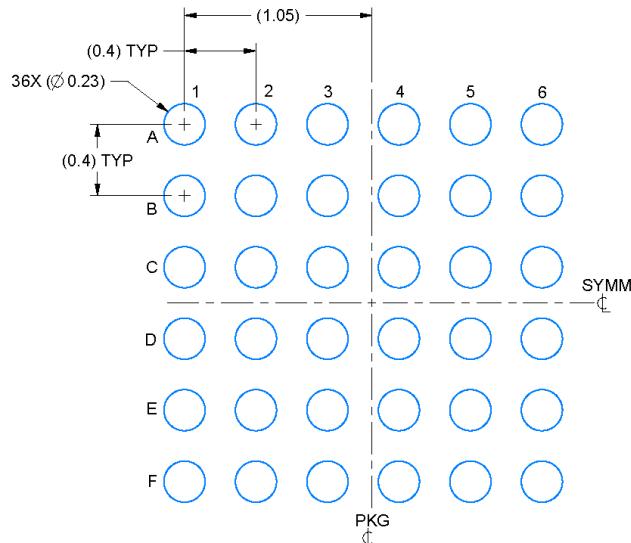


NOTES:

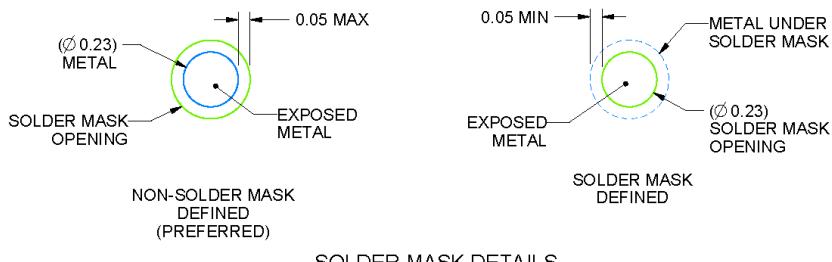
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT**YBG0036-C01****DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



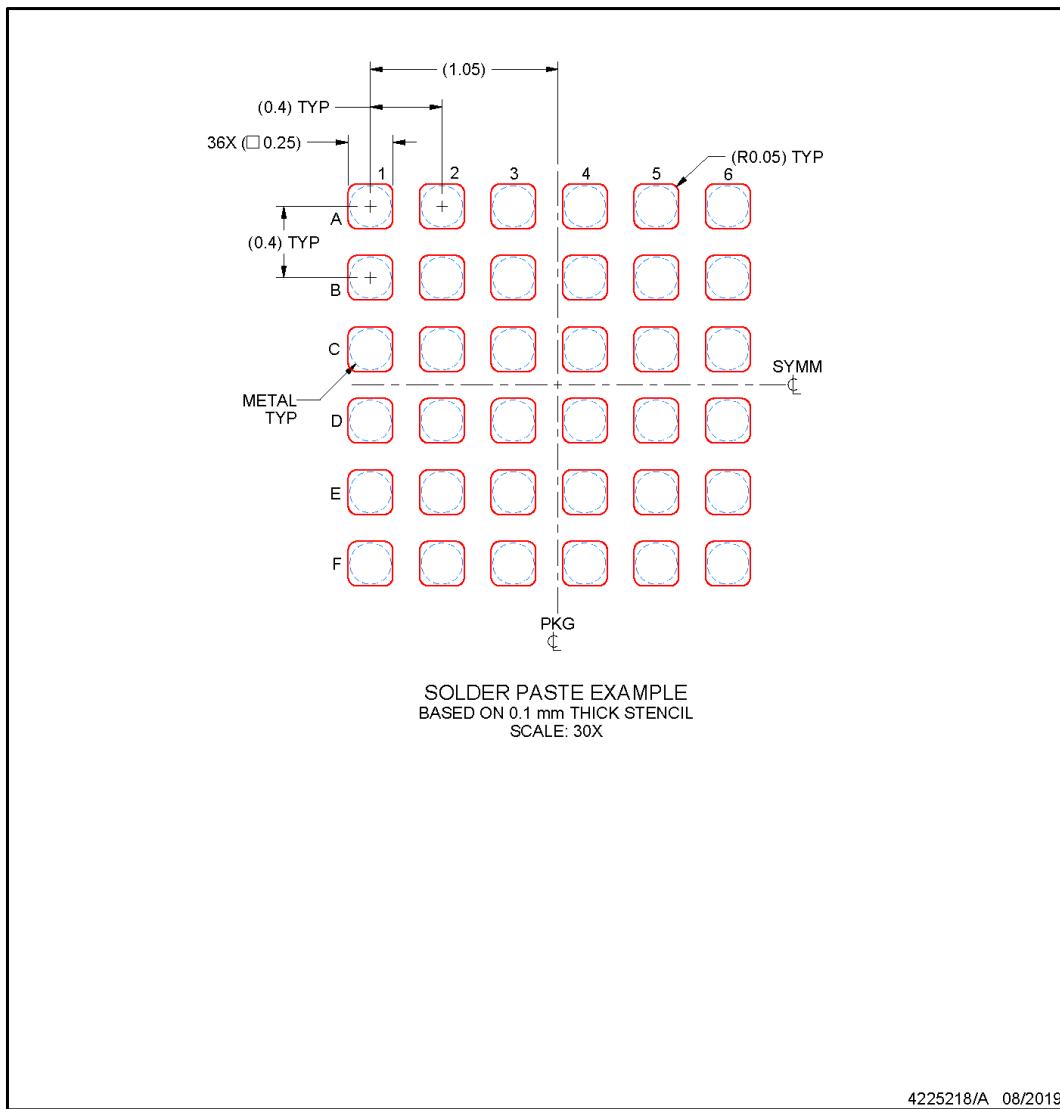
4225218/A 08/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN**YBG0036-C01****DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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