Debugging Tips

Outline

- Module Instantiation
- Print out signal
- Waveform
- Breakpoint
- Schematic

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Module Instantiation

- Parameter value assignment by order
  - ProgramCounter PC(
    clk_i,
    rst_i,
    pc_in,
    pc_out);
- Parameter value assignment by name
  - ProgramCounter PC(
    .clk_i(clk_i),
    .pc_in_i(pc_in),
    .rst_i(rst_i),
    .pc_out_o(pc_out));

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Values of signals

- $monitor ("%0dns :\$monitor: a=%b b=%b" , $stime, a, b);
  - Print parameters every time as one of its parameters changes.
- $display ("%0dns :\$display: a=%b b=%b" , $stime, a, b);
  - Like printf in C, only print parameters once.

Values of signals

- $fwrite(fp, "%0dns :\$fwrite : a=%b b=%b\n", $stime, a, b);
  - Like fprintf in C.
  - Used with $fopen and $fclose.
  - $fdisplay is similar with $fwrite but append “\n” automatically

Values of signals

```
ProgramCounter PC(
        .clk_i(clk_i),
        .rst_i (rst_i),
        .pc_in_i(pc_in) ,
        .pc_out_o(pc_out));
```

- $display("a = %d, b = %d",
  PC.pc_in_i, PC.pc_out_o);

- $monitor("a = %d, b = %d",
  PC.pc_in_i, PC.pc_out_o);

Values of signals

- $monitor
  - 1ns :$monitor: a=0 b=1
- $display
  - 2ns :$display: a=1 b=0
- $fwrite
  - In a certain text file.
  - 1ns :$fwrite : a=0 b=1

Comparison

- $display displays the result of simulation only when the display task occurs in your code.
- $monitor continuously MONITORS its variables, when a variable changes its value, monitor displays the results.
- $fwrite writes data into a text file.

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Waveform

- Add following code:

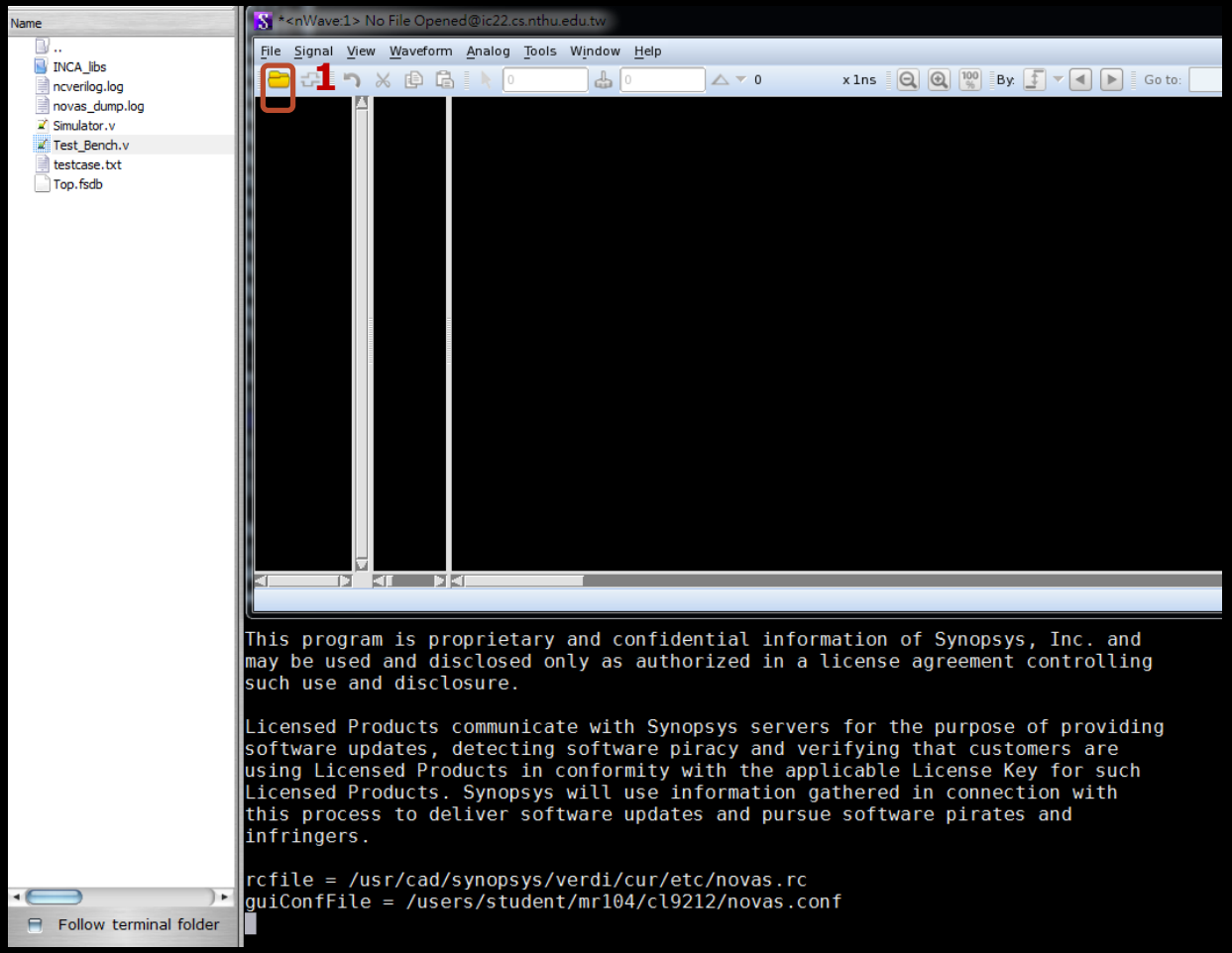
```
initial begin
    $fsdbDumpfile("Top.fsdb");
    /*waveform file*/
    $fsdbDumpvars(0, "+mda");
    /*also dump 2D register*/
end
```

Waveform

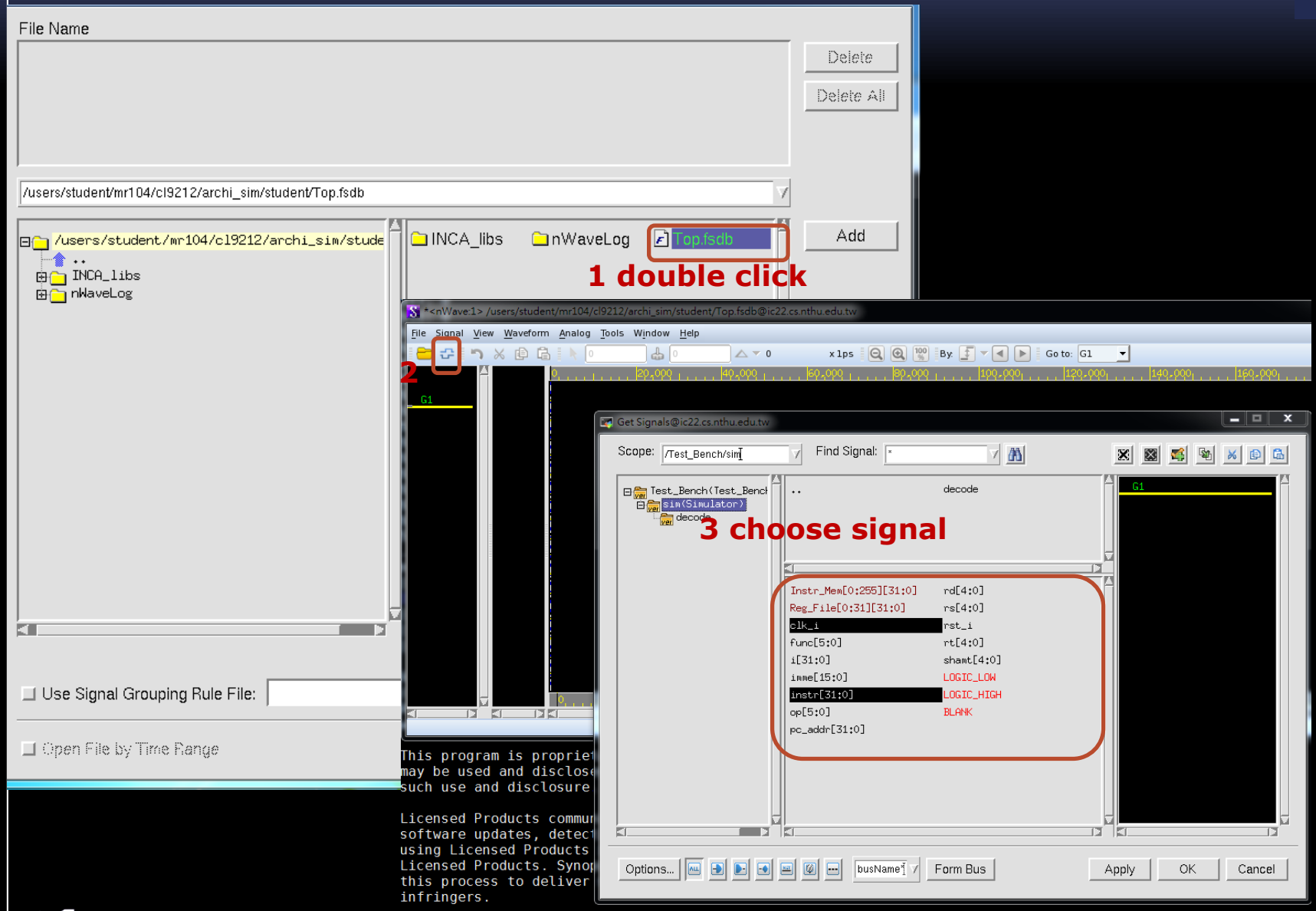
- Make sure you connect workstation with ssh –X icXX
  - -X: set display IP to the computer you are using
- Execute NC Verilog with parameter "+access+r"
  - $ ncverilog Simulator.v Test_Bench.v +access+r
- Use nWave to view waveform

Waveform

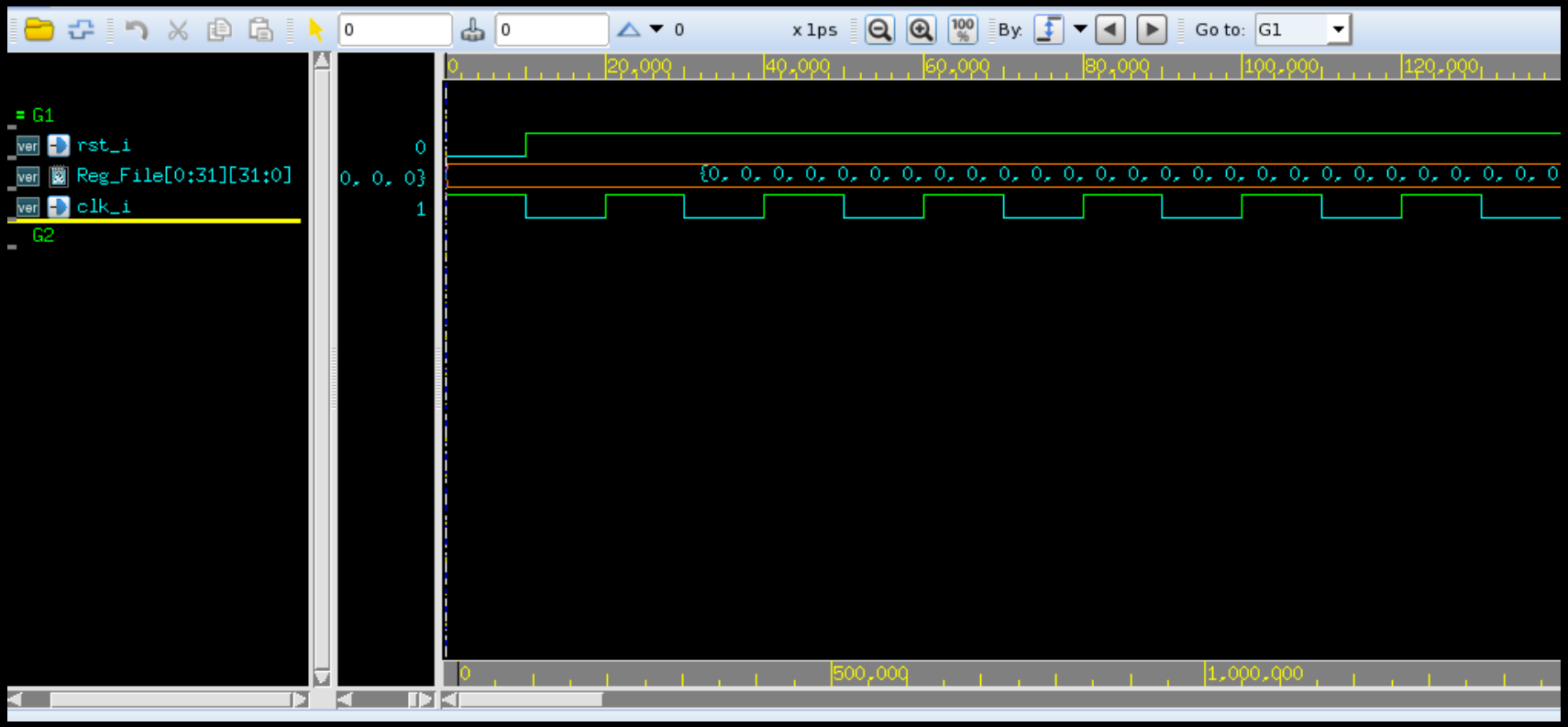
- $nWave &



Waveform


File Name
Delete
Delete All
/users/student/mr104/cl9212/archi_sim/student/Top.fsdb
/users/student/mr104/cl9212/archi_sim/stude
..
INCA_libs
nWaveLog
INCA_libs
nWaveLog
Top.fsdb
Add
1 double click
Use Signal Grouping Rule File:
Open File by Time Range
*<nWave:1> /users/student/mr104/cl9212/archi_sim/student/Top.fsdb@ic22.cs.nthu.edu.tw
File Signal View Waveform Analog Tools Window Help
2
G1
Get Signals@ic22.cs.nthu.edu.tw
Scope: /Test_Bench/sim
Find Signal:
Test_Bench(Test_Bench
sim(Simulator)
decode
3 choose signal
decode
G1
Instr_Mem[0:255][31:0]
Reg_File[0:31][31:0]
clk_i
func[5:0]
i[31:0]
imme[15:0]
instr[31:0]
op[5:0]
pc_addr[31:0]
rd[4:0]
rs[4:0]
rst_i
rt[4:0]
shamt[4:0]
LOGIC_LOW
LOGIC_HIGH
BLANK
Options...
busName
Form Bus
Apply
OK
Cancel
This program is proprie
may be used and disclos
such use and disclosure
Licensed Products commu
software updates, detec
using Licensed Products
Licensed Products. Syno
this process to deliver
infringers.

Waveform


0
0
0
x 1ps
By:
Go to:
G1
20,000
40,000
60,000
80,000
100,000
120,000
G1
rst_i
Reg_File[0:31][31:0]
clk_i
G2
0
0, 0, 0}
1
{0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0
0
500,000
1,000,000

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Breakpoint

- Insert “$stop;” where you want to set breakpoint

```
else begin
    instr = Instr_Mem[pc_addr/4];
    decode;
    $stop;
    if(op == 6'd0)begin //R-type
```

- It will stop simulation when it encounter $stop

```
            103000000
Simulation stopped via $stop(1) at time 20 NS + 1
./Simulator.v:97                $stop;
ncsim>
```

Breakpoint

- Continue simulation by “.” or “run”

```
Simulation stopped via $stop(1) at time 60 NS + 1
./Simulator.v:97                $stop;
ncsim> .
```

- You can also restart from the beginning by “reset” and type “.” or “run” to start simulation

```
Simulation stopped via $stop(1) at time 60 NS + 1
./Simulator.v:97                $stop;
ncsim> reset
Loaded snapshot worklib.Top:v
ncsim> run
```

Breakpoint

- “finish” or “exit” to exit simulation

```
Simulation stopped via $stop(1) at time 40 NS + 1
./Simulator.v:97                $stop;
ncsim> finish
```

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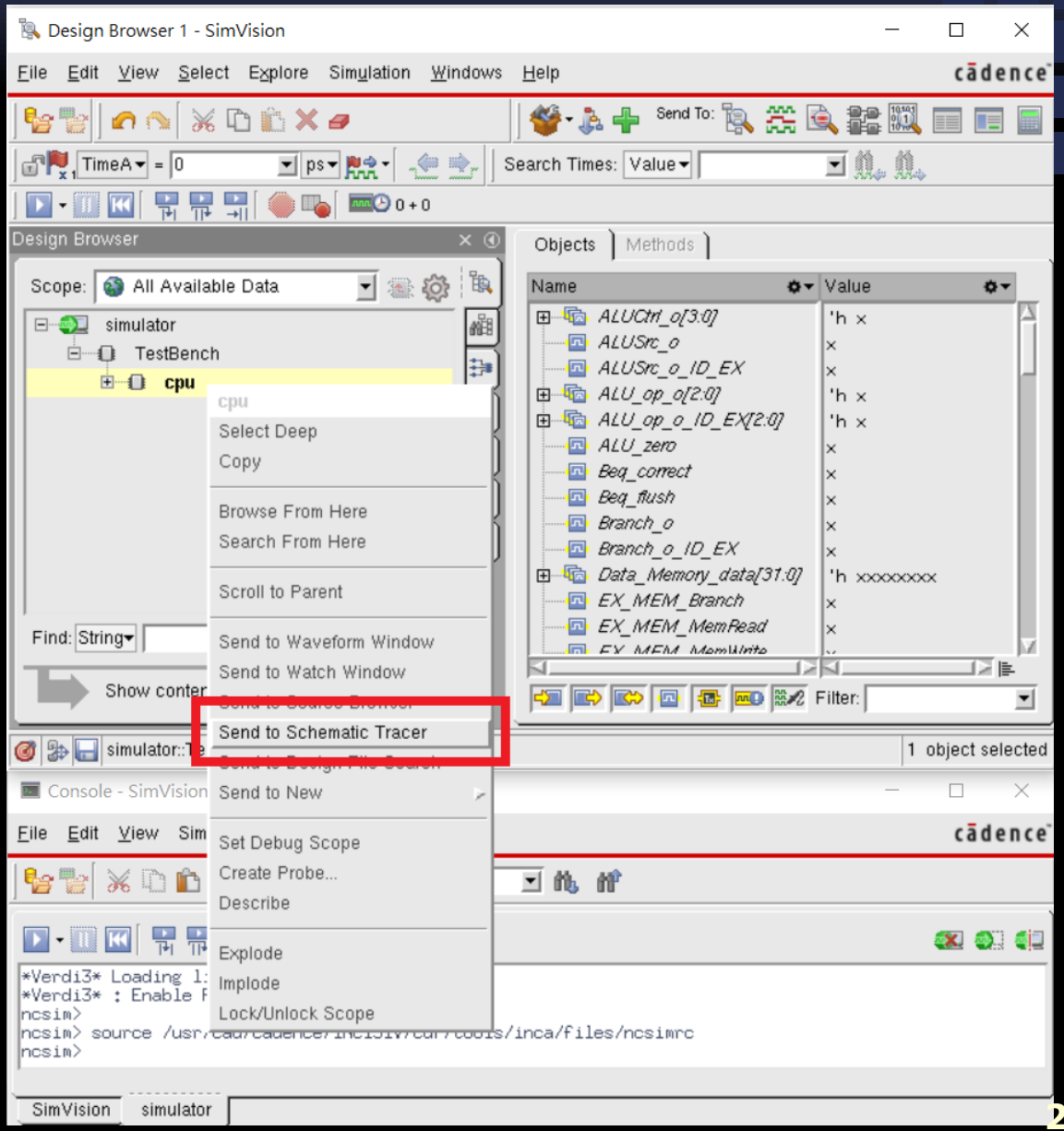
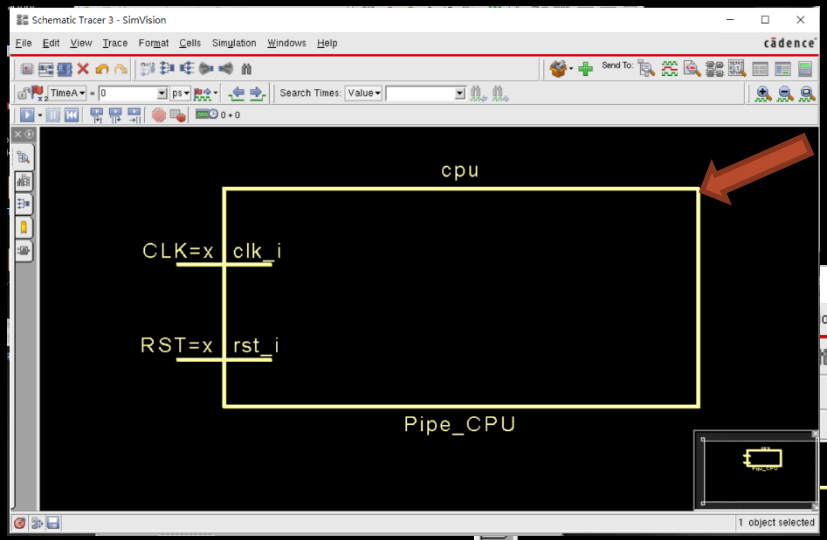
Compile with gui

- Make sure you connect workstation with ssh –X icXX
  - -X: set display IP to the computer you are using
- Execute NC Verilog with parameter "+access+r" and "+gui"
  - $ ncverilog +access+r *all your codes* +gui

Schematic

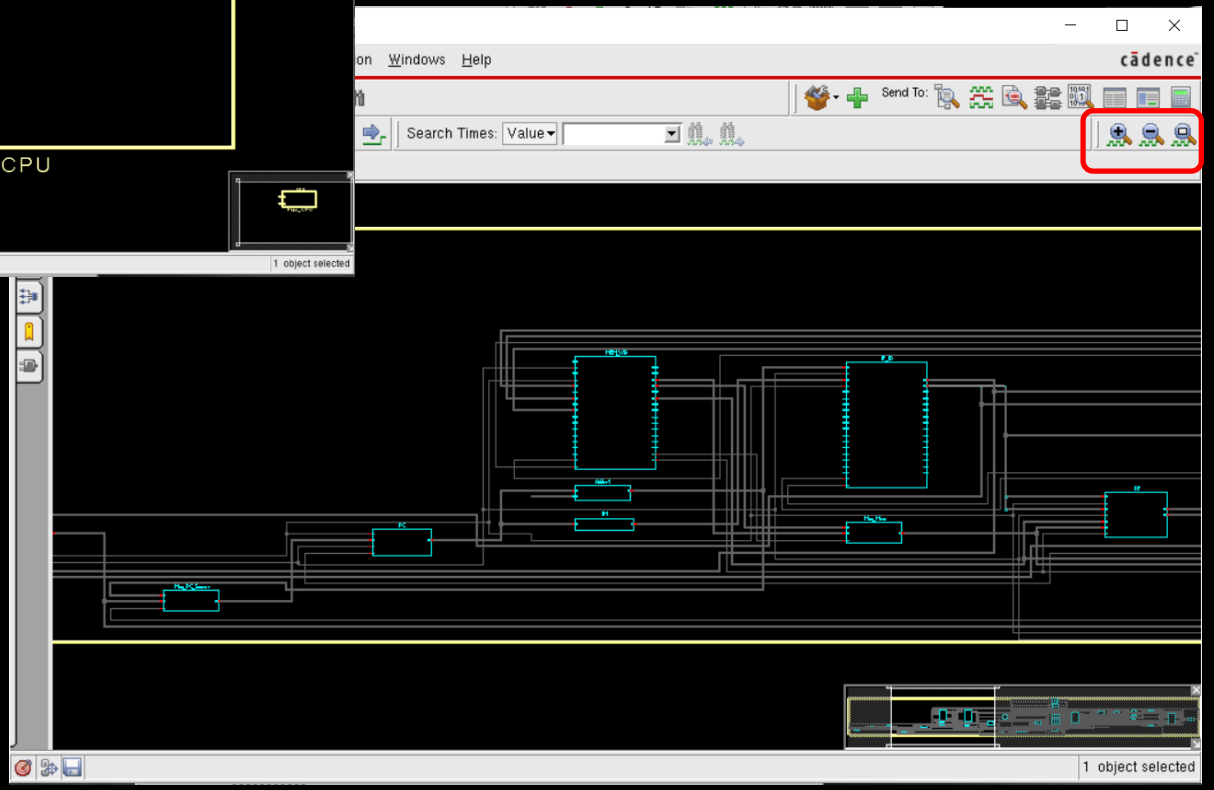

Design Browser 1 - SimVision
File Edit View Select Explore Simulation Windows Help
cadence
Send To:
TimeA = 0 ps
Search Times: Value
0 + 0
Design Browser
Scope: All Available Data
simulator
TestBench
cpu
Objects
Methods
Name
Value
ALUCtrl_o[3:0]
ALUSrc_o
ALUSrc_o_ID_EX
ALU_op_o[2:0]
ALU_op_o_ID_EX[2:0]
ALU_zero
Beq_correct
Beq_flush
Branch_o
Branch_o_ID_EX
Data_Memory_data[31:0]
EX_MEM_Branch
EX_MEM_MemRead
Find: String
Show conter
Filter:
1 object selected
cpu
Select Deep
Copy
Browse From Here
Search From Here
Scroll to Parent
Send to Waveform Window
Send to Watch Window
Send to Schematic Tracer
Send to New
Set Debug Scope
Create Probe...
Describe
Explode
Implode
Lock/Unlock Scope
Console - SimVision
File Edit View
cadence
Verdi3 Loading l
Verdi3 : Enable
ncsim>
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim>
SimVision
simulator

Schematic



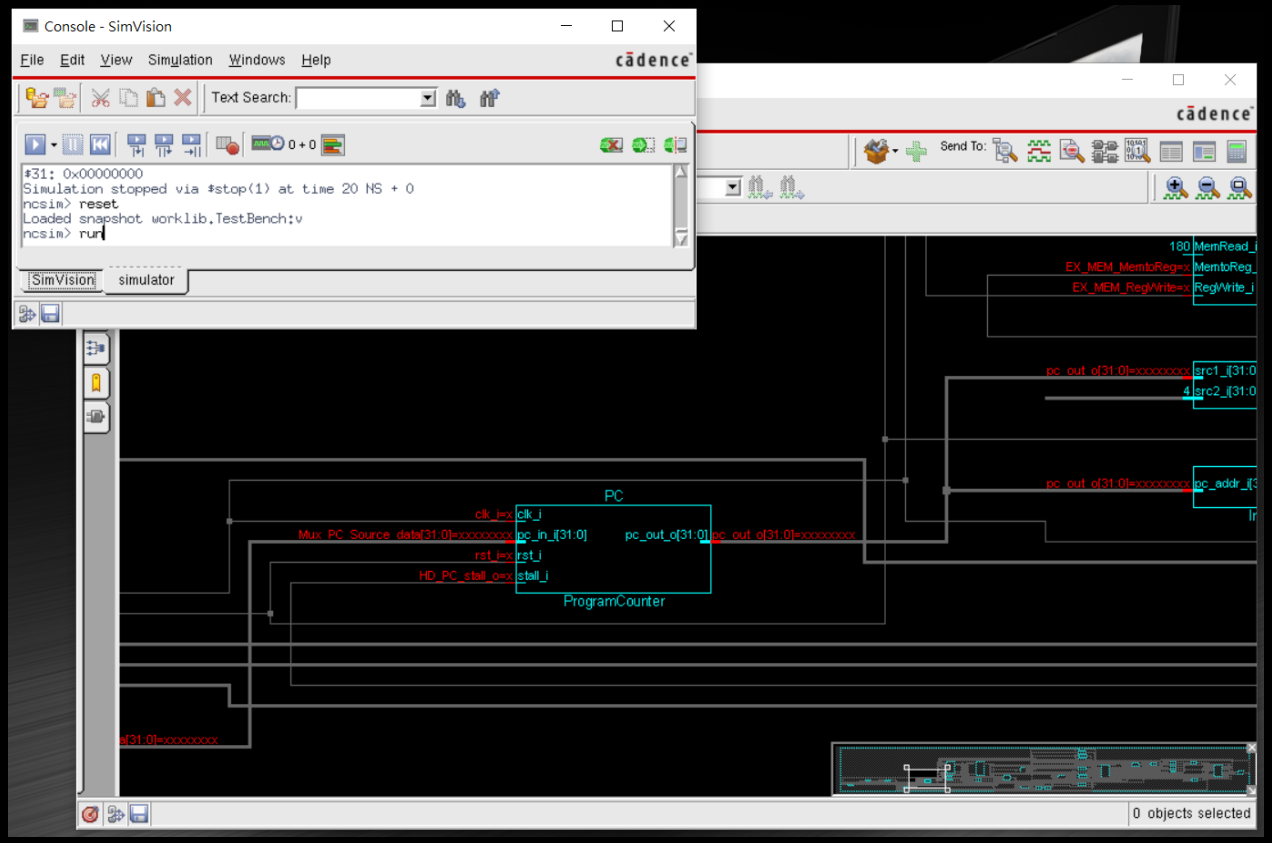
Double click

Adjust view



Schematic + breakpoint

- Type “run” or “.” to start, as mentioned in section “breakpoint”



Schematic + breakpoint

- It will show values of each block when encounter breakpoint