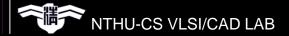
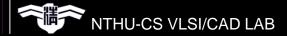
2017 Architecture

Project – Environment Setting



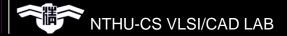
Outline

- Workstation setting : MobaXterm
- Makefile



Outline

- Workstation setting : MobaXterm
- Makefile



MobaXterm Download

- Download the free version of MobaXterm
 - http://www.azofreeware.com/2014/11/mobaxterm-portable.html





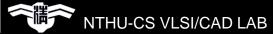
MobaXterm Installation

Installation

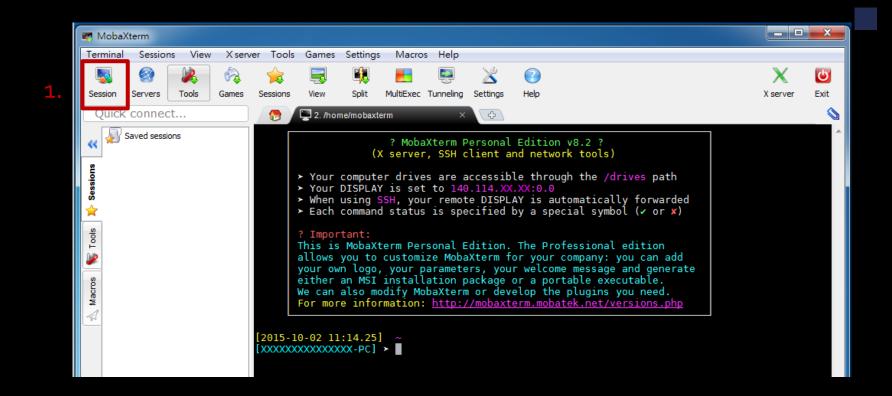


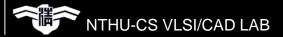
Click the icon in the folder





Workstation Setup

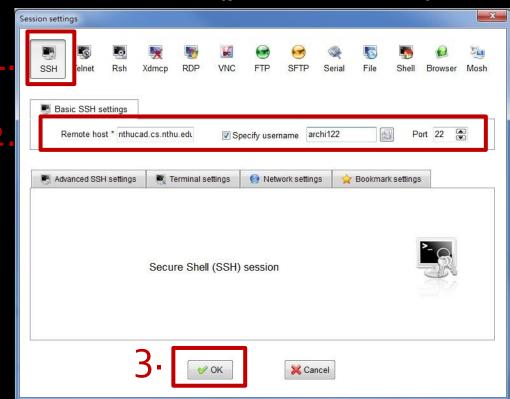




Workstation Setup (Cont.)

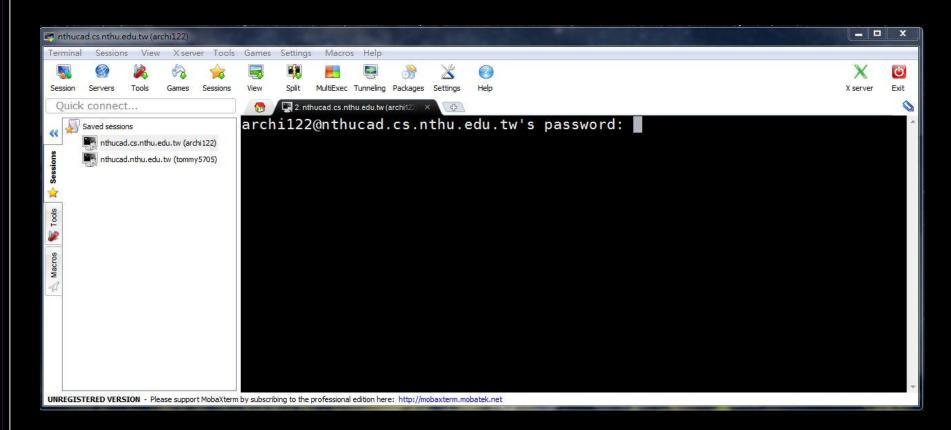
- Enter the following blank
 - Remote host: nthucad.cs.nthu.edu.tw
 - Specify username : archXX (your account)
 - Port : 22

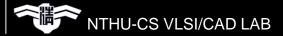
Click "OK"



Login at the First Time

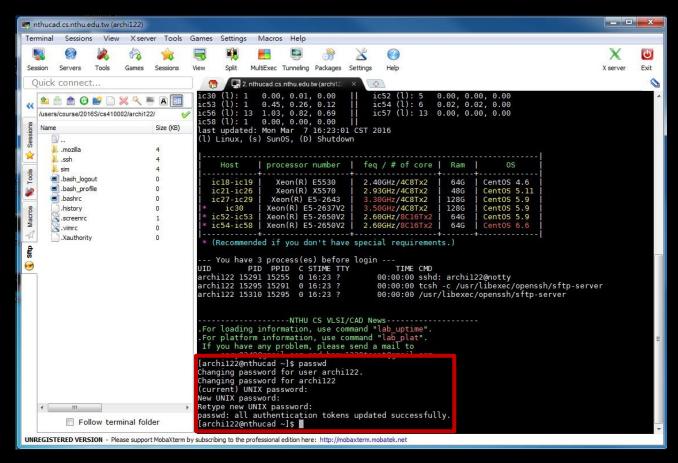
Key in your initial password from e-mail

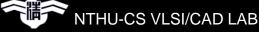




Change Your Password

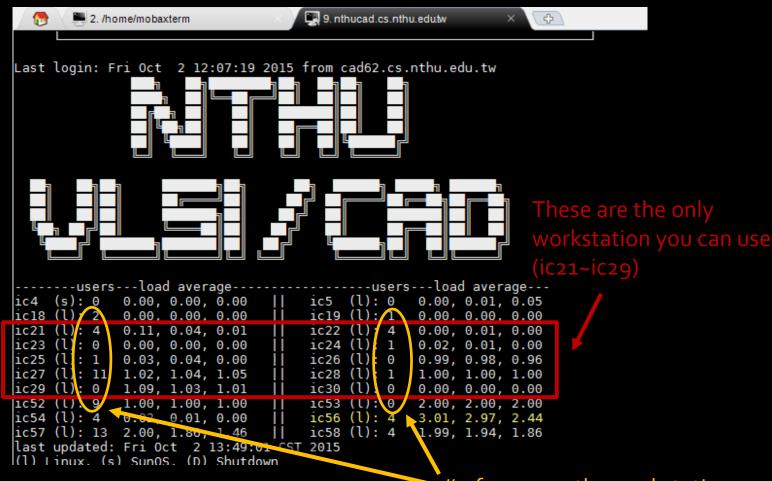
Type "passwd" to change your password





Connecting to Workstation

- You can only choose on workstation from ic21 ~ ic29
- Find a workstation with less user



Connecting to Workstation (Cont.)

- Connect to a workstation (Important)
 - ssh -X icXX

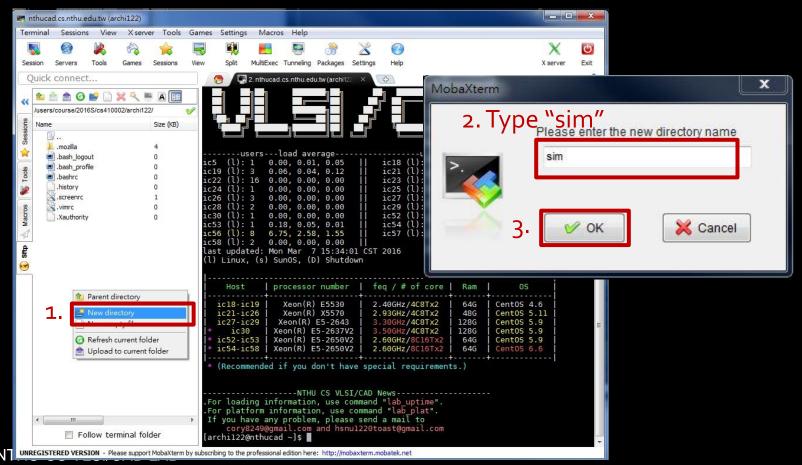
```
3. nthucad.cs.nthu.edu.tw (archi12 ×
        -----NTHU CS VLSI/CAD News-----
.For loading information, use command "lab uptime".
.For platform information, use command "lab plat".
 If you have any problem, please send a mail to
[archi122@nthucad ~]$ ssh -X ic21
The authenticity of host 'ic21 (192.168.75.51)' can't be established.
RSA key fingerprint is e0:06:4a:9a:6d:b2:a1:c7:c7:f6:49:b0:39:54:8c:7a.
Are you sure you want to continue connecting (yes/no)? yes
                                                                                      Type "yes"
Warning: Permanently added 'ic21,192.168.75.51' (RSA) to the list of known hosts.
archi122@ic21's password:
             0.00, 0.01, 0.05
                                                  0.00, 0.00, 0.00
             0.00, 0.00, 0.00
                                     ic21 (l): 3
                                                  0.02, 0.01, 0.00
             0.00, 0.00, 0.00
                                     ic23 (l): 17 2.03, 1.97, 1.57
             0.00. 0.00. 0.00
                                                  0.00. 0.00. 0.00
             0.00, 0.00, 0.00
                                                  0.08, 0.07, 0.02
             0.00, 0.00, 0.00
                                                  0.01, 0.02, 0.00
             0.00, 0.00, 0.00
                                                  0.00, 0.03, 0.05
             0.01, 0.09, 0.08
                                     ic54 (l): 6
                                                  0.63, 0.18, 0.05
ic56 (l): 13 1.02, 0.79, 0.74
                                     ic57 (l): 13 0.00, 0.00, 0.00
ic58 (l): 1 0.00, 0.00, 0.00
last updated: Mon Mar 7 16:07:01 CST 2016
(l) Linux, (s) SunOS, (D) Shutdown
       -----NTHU CS VLSI/CAD News-----
.For loading information, use command "lab uptime".
.For platform information, use command "lab plat".
 If you have any problem, please send a mail to
     cory8249@gmail.com and hsnu1220toast@gmail.com
Synopsys licenses have set!
                               2. Should be [XXX@icXX ~] s after connecting
[archi122@ic21 ~]$
```



NTHU-CS VLSI/CAD LAB

Create directory

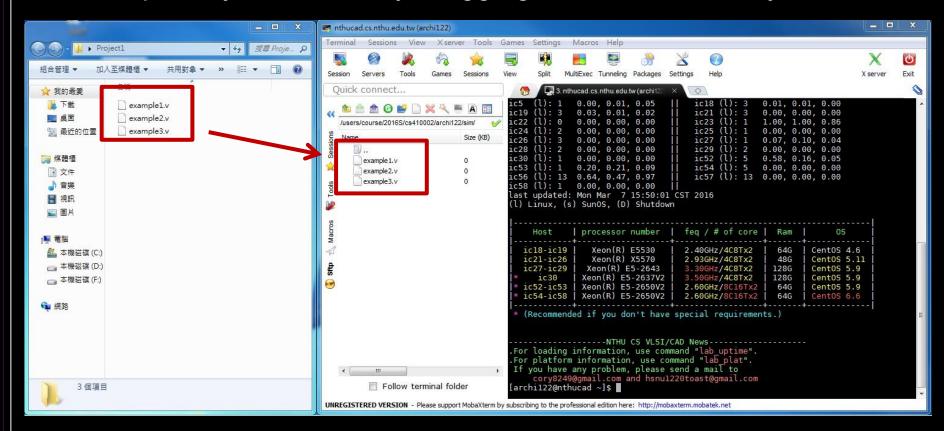
Right click to create new directory "sim" or by command line "mkdir sim"





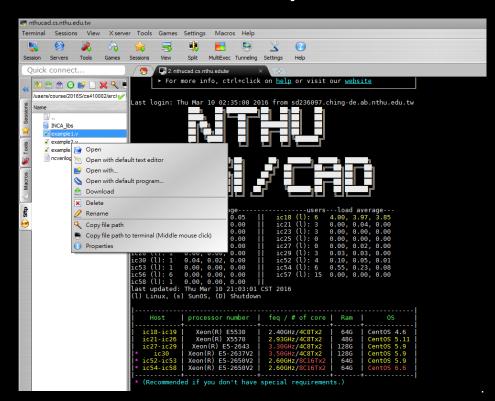
Uploading .v Files

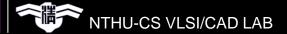
- Upload files
 - Upload your .v files by dragging them into directory



Edit files in workstation

- Right click → open with mobaXterm's editor
- Vim is available in workstation
- You can also edit in Windows then upload it

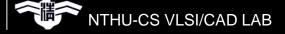




Run simulation

- Use "NC verilog" as standard simulation platform
 - Commercial software by Cadence

You can use any IDE/Editor to program



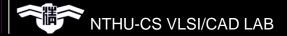
Run simulation

- \$ ncverilog all .v file you need
 - i.e. \$ncverilog Simulator.v Test_Bench.v

```
Initial blocks:
             Pseudo assignments:
             Simulation timescale: 1ps
      Writing initial simulation snapshot: worklib.Test Bench:v
*Verdi3* Loading libsscore ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
Simulation complete via $finish(1) at time 2010 NS + 0
                  #(`CYCLE TIME*`END CYCLE) $finish;
```

Outline

- Workstation setting : MobaXterm
- Makefile

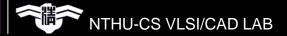


Makefile - introduction

A tool helps you compile your program with multiple commands and arguments

We provide you a simple makefile for the projects in this course

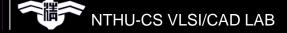
Put the makefile in your project directory so that it works for you



Makefile - purpose

- Multiple source files in a project
 - you have to type a lot in a single command
 - i.e. \$ncverilog file1.v file2.v file3.v testbench.v

- Additional function with any tool/complier
 - you have to add some parameters at the end
 - i.e. \$ncverilog (all .v files) +access+r +gui
- Makefile can do the things above for us!



Makefile – simple syntax

```
1 VLOG = ncverilog
2 Test = Test_bench.v
3 CPU = Simulator.v
4
5 all:
6 $(VLOG) $(CPU) $(Test) [TAB][rule]
```

- all is the default target name
 - You can define other targets
- \$make or \$make all
 - This makefile will do: ncverilog Simulator.v Test_bench.v
- For detailed and advanced makefile writing skills, please find them online

