Bridge of Life Education

Advanced SOC Design Lab - Synopsys-Flow

(team work)

Jiin Lai

Outline

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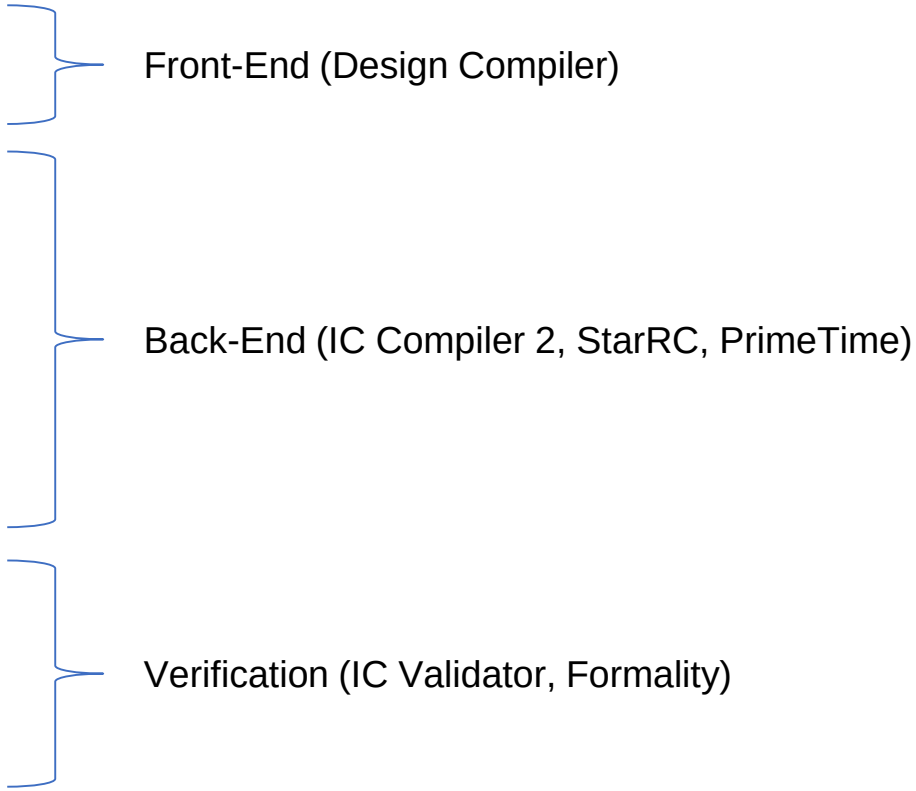
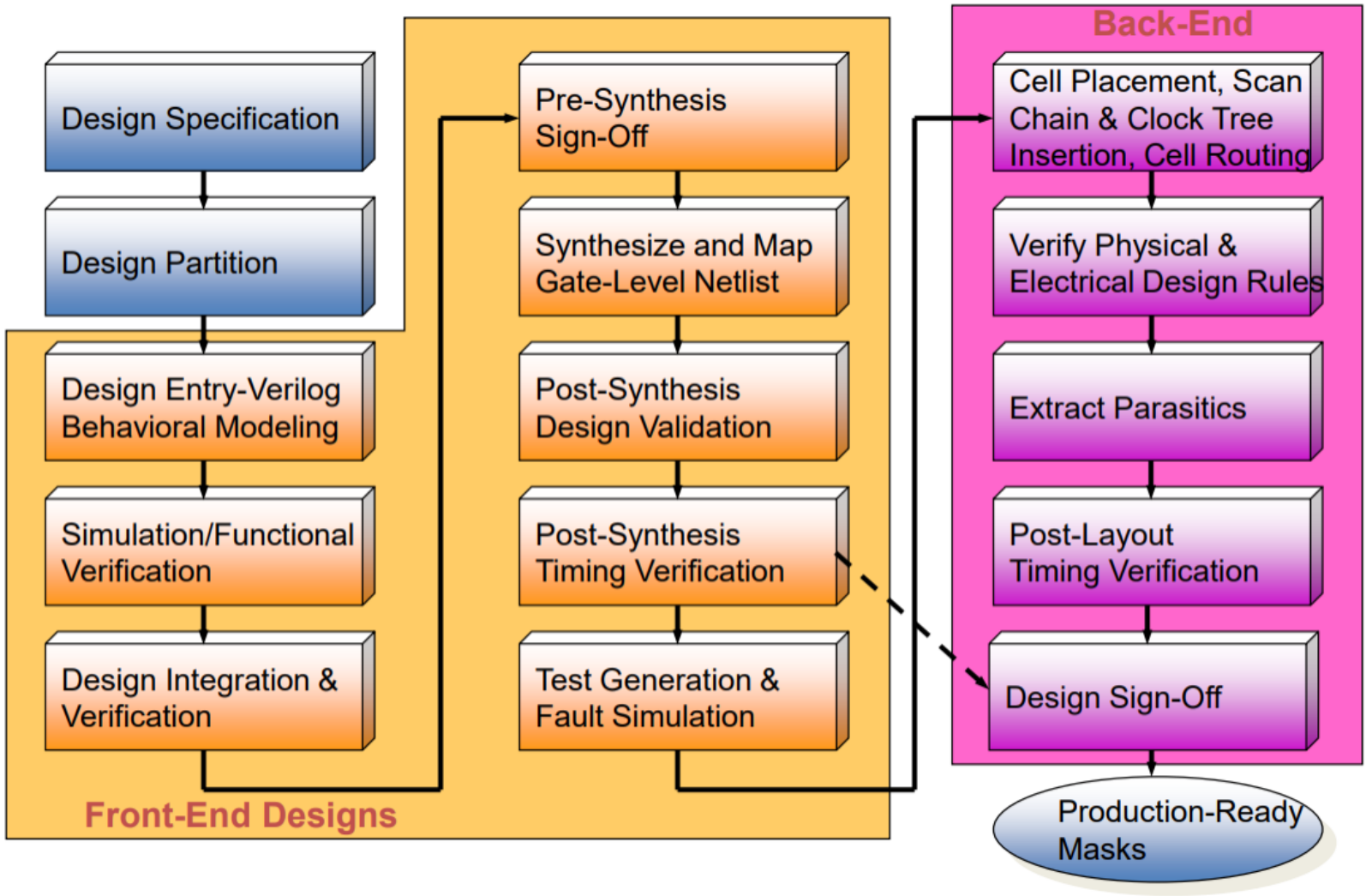
- Lab1 Floorplan
- Lab2 Placement & Route
- Lab StarRC
- Lab PrimeTime
- Lab4 Chip Finishing
- Lab IC Validator - DRC
- Lab IC Validator – LVS
- Lab formality



ASIC Design flow (cell-based)



Environment Settings

- Goal: setup the EDA environment and library for your design
- Source EDA tools licence
  - ~~Ex: source asoc.cshrc~~

Don’t forget to modify this according to where you want to put this directory!

For NTHU

```
cp -R /home/course/ee5252/lab_snps_flow/lab_formal_release/lab_formal_release <your_lab3_directory>
```

~~In your ~/.tcshrc file, add a line: source /home/course/ee5252/lab_snps_flow/asoc.cshrc~~

(<update in version2> You don’t need to do this; instead, please refer to the next page.)

<This page is added in lab-snps-flow-workbook_NTHU版_version2>

For NTHU

1. In your ~/.tcshrc file, add the commands below:

```
source /usr/cadtool/user_setup/08-synthesis.csh
setenv SYNOPSYS_LC_ROOT /usr/cad/synopsys/lc/cur
source /usr/cadtool/user_setup/08-primetime.csh
source /usr/cadtool/user_setup/08-verdi.csh
source /usr/cad/synopsys/CIC/astro.cshrc
source /usr/cadtool/user_setup/08-tmax.csh
source /usr/cadtool/user_setup/03-ic.csh
source /usr/cadtool/mentor/cic_setup/calibre_ixl_2021.csh
source /usr/cadtool/user_setup/03-confrml.csh
source /usr/cadtool/user_setup/03-innovus.csh
source /usr/cadtool/user_setup/08-hspice.csh
source /usr/cadtool/user_setup/03-assura.csh
source /usr/cadtool/user_setup/08-spyglass.csh
source /usr/cadtool/user_setup/08-vcs.csh
source /usr/cadtool/user_setup/08-icc2.csh
source /usr/cad/synopsys/CIC/icc.csh
setenv ICV_HOME_DIR "/usr/cadtool/cad/synopsys/icvalidator/2021.06"
set path = (/usr/cadtool/cad/synopsys/icvalidator/2021.06/bin/LINUX.64 $path)
source /usr/cadtool/user_setup/08-star-rcxt.csh
source /usr/cadtool/user_setup/08-formality.csh
source /usr/cadtool/user_setup/05-catapult.csh
source /usr/cadtool/user_setup/05-questasim.csh
```

2. Log out EE workstation, and log in again, in order to reload .tcshrc file.

Environment Settings

- Directory: ./lab_formal_release/common/common.tcl
  - set DESIGN_REF_PATH “<lib path>/SAED14_EDK_LAB“
  - <lib path>: confirm with the TA
- Directory: ./lab_formal_release/common/common_setup.tcl
  - set DESIGN_REF_PATH “<lib path>/SAED14_EDK_LAB“
  - <lib path>: confirm with the TA

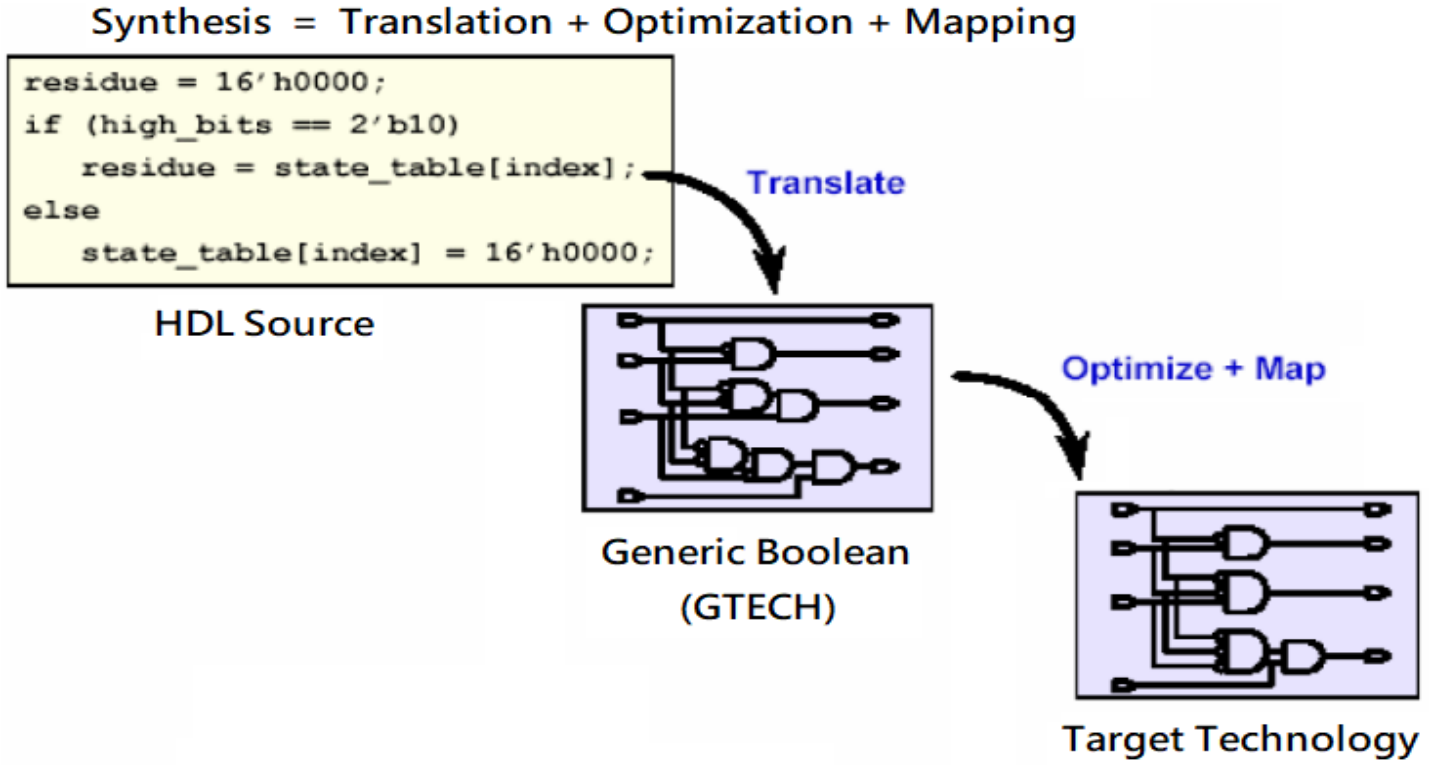
For NTHU

<lib path> is “/home/course/ee5252/lab_snps_flow/SAED14_EDK_LAB/SAED14_EDK_LAB”

Please modify the above files according to this path.

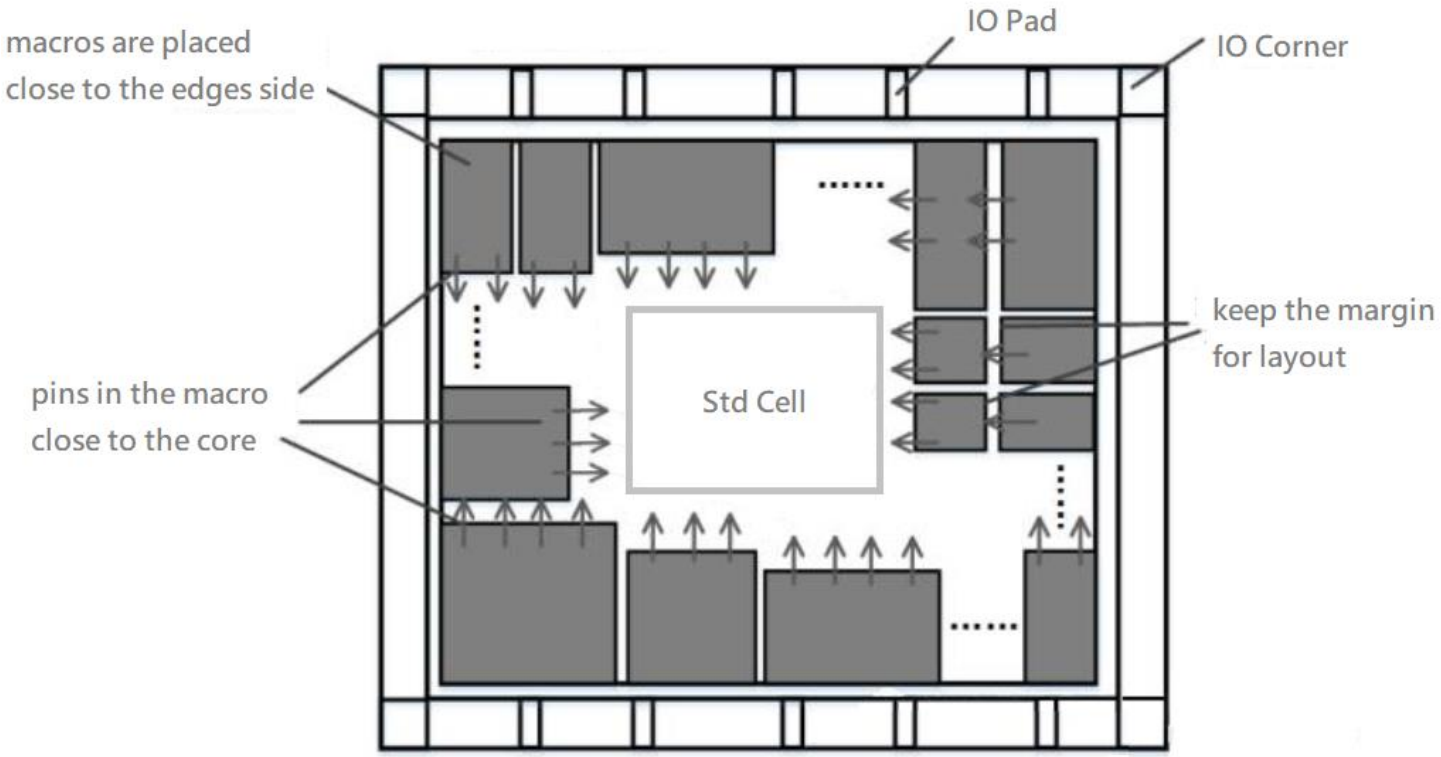
Lab Synthesis

- Goal: analyze and synthesis HDL code from RTL to gate-netlist



Lab1 Floorplan

- Goal: design initiation and chip floorplan

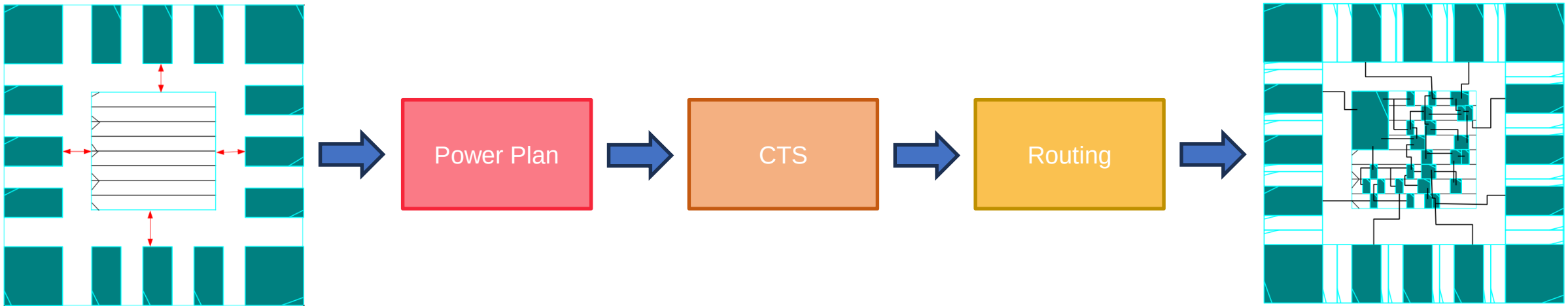


Lab2 Placement & Route

For NTHU

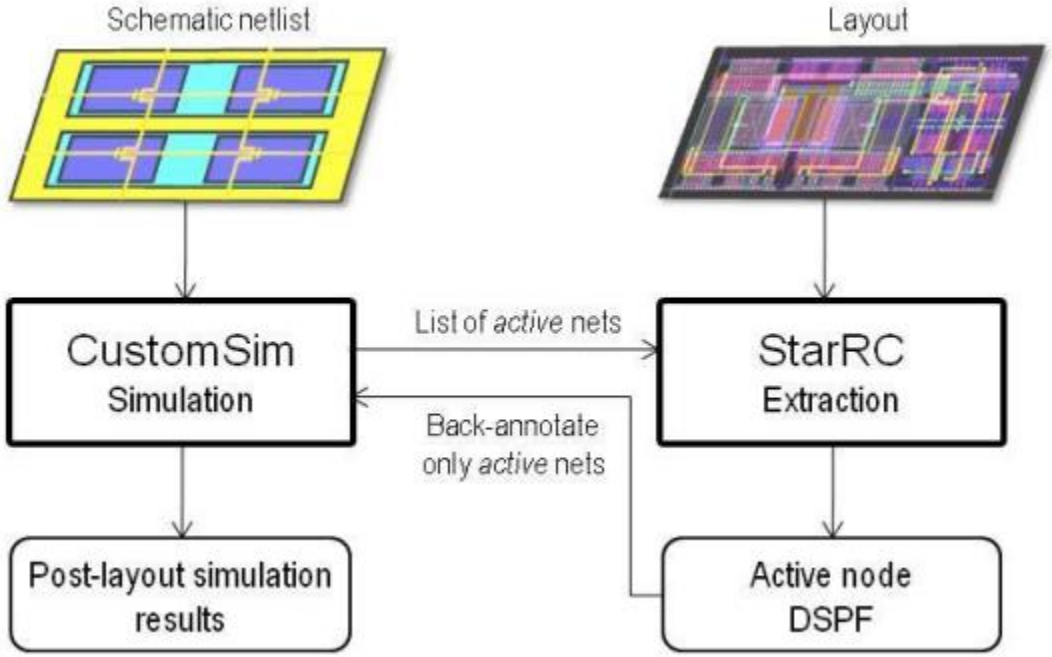
If it encounters a fatal error (Internal system error, Error code=6), please try to use another “ws” server, like ws27.

- Goal: macro/std-cell placement and route



Lab StarRC

- Goal: extract the information of parasitic devices for simulation and analysis

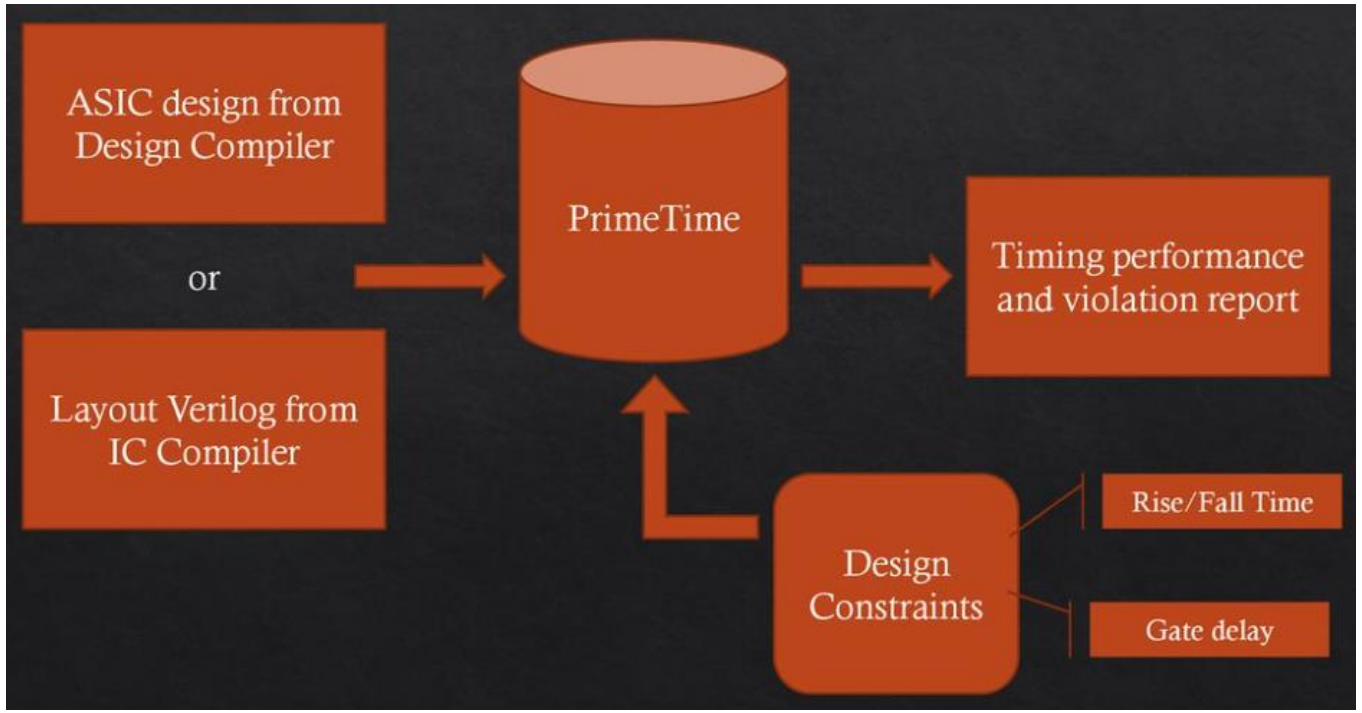


Lab PrimeTime

For NTHU

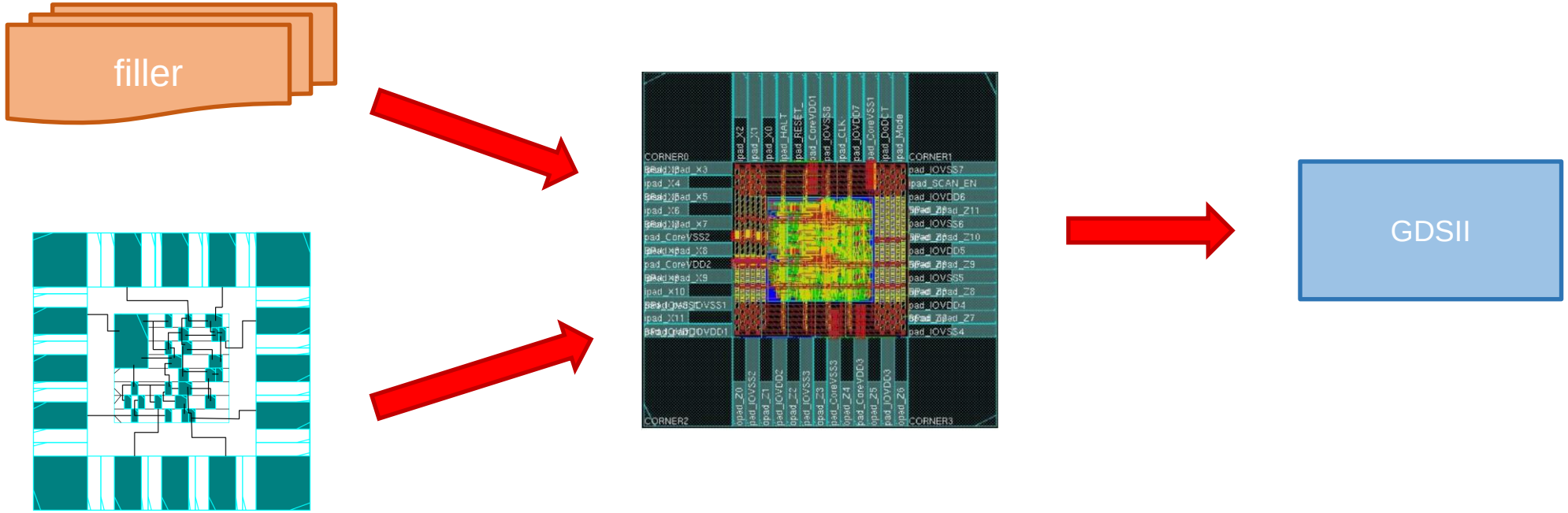
Please change from 「/bin/tclsh」 to 「tclsh」 in /lab_pt/work/Makefile

- Goal: Static Timing Analysis and Power analysis



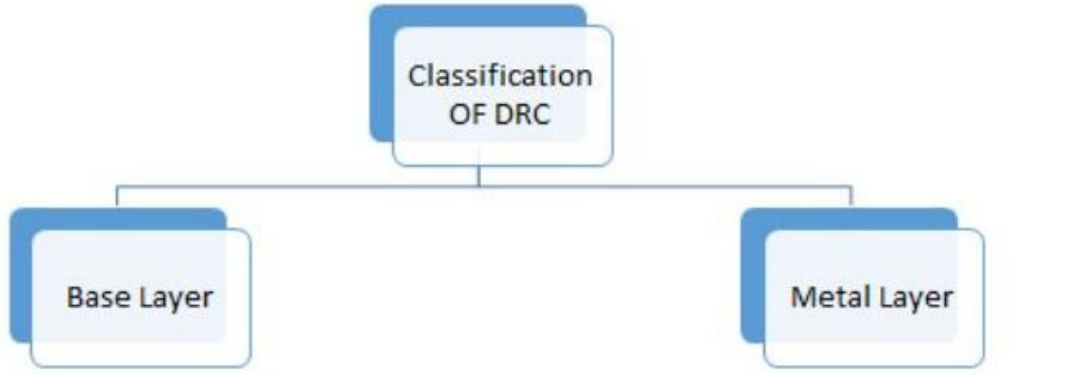
Lab4 Chip Finishing

- Goal: insert filler and export GDSII file for chip tap out



Lab IC Validator - DRC

- Goal: verify Design Rule Check for the target technology



Depending on its Naming Convention (TSMC specific), DRC has been categorized as below:

Pattern	Description
DN , *DM*	Density related
LUP*	LATCHUP related
CPO or *TPO*	CutPoly or Trim Poly Rule
NW	(NWell)Between two different well Potential
PO	Poly related
VT	Implant Spacing and Width related
OD	Oxide and Diffusion related

Pattern	Description
G.*	Geometry related check
.S.	Spacing related check
.A.	Area related check
.G0.	DPT Related check
CM	CutMetal Related
*CM*O*	CutMetal Overlap Related

Lab IC Validator - DRC

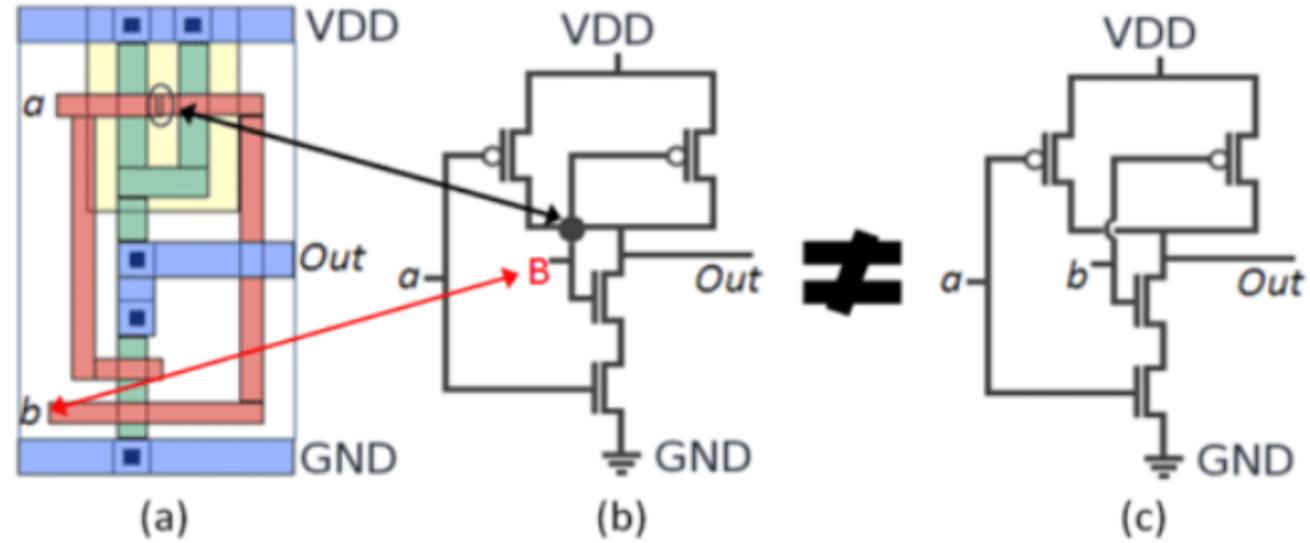
- Directory: ./lab_formal_release/lab_icv_drc/work/Makefile
  - TECH_DIR = <lib path>/SAED14_EDK_LAB/tech
  - <lib path>: confirm with the TA

For NTHU

Please modify as `TECH_DIR = /home/course/ee5252/lab_snps_flow/SAED14_EDK_LAB/SAED14_EDK_LAB/tech`

Lab IC Validator - LVS

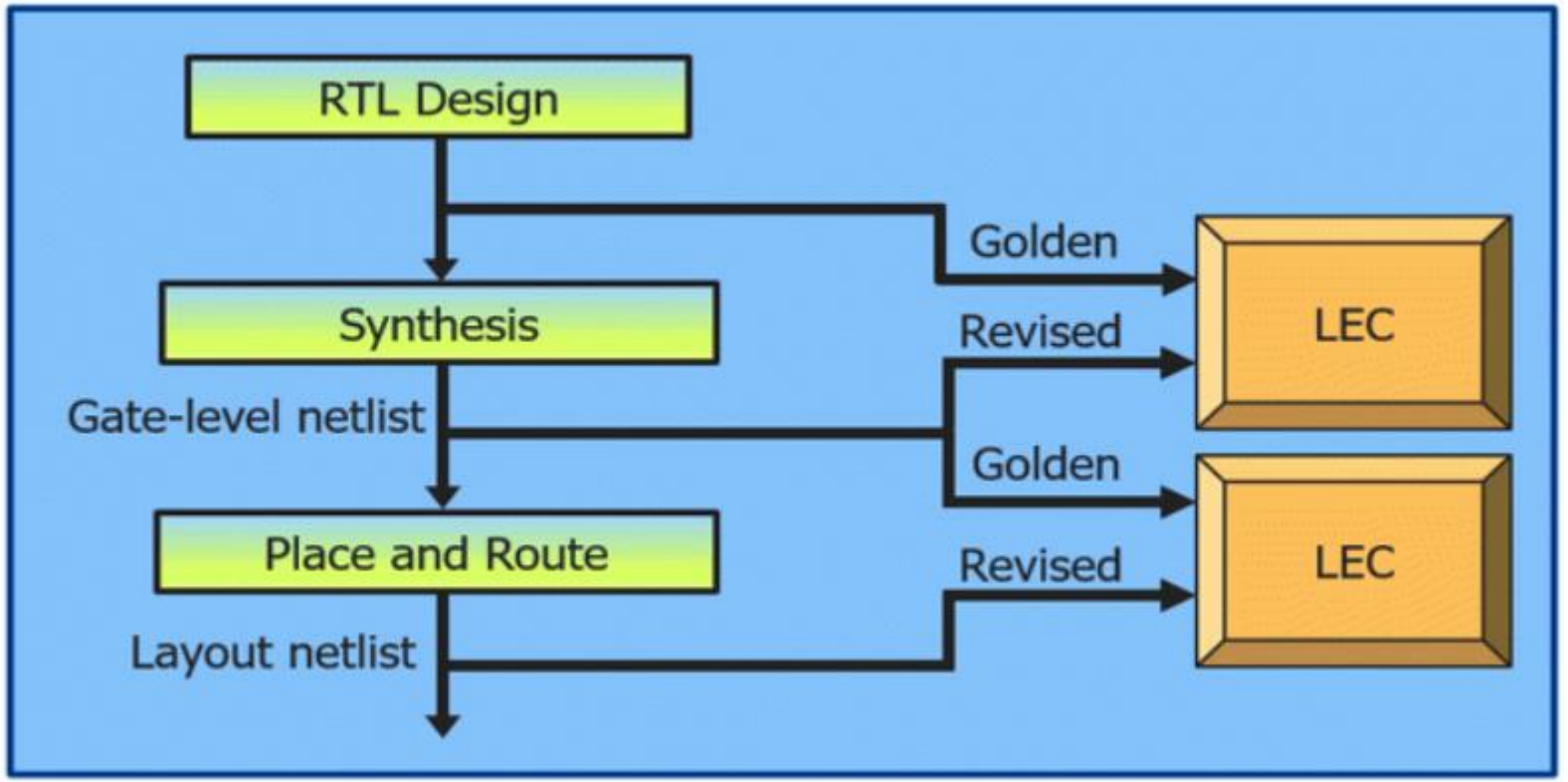
- Goal: verify Layout Versus Schematic matching the design



LVS procedure: (a) cell layout, (b) extracted schematic, and (c) targeted schematic

Lab formality

- Goal: verify the behavior of circuit and layout that



Lab formality

- Directory: ./lab_formal_release/lab_formal/script/run_formality_cmd.tcl

- read_verilog -r \
  <absolute path>/lab_formal_release/lab_formal/work/../../input/i2c_master_top.v -work_library WORK

- read_verilog -i \
  <absolute path>/lab_formal_release/lab_formal/work/../../results/i2c_master_top.pt.v.gz

For NTHU

In addition to the above two modifications, you also need to:

1. change from 「/bin/tclsh」 to 「tclsh」 in /lab_formal/work/Makefile
2. change from 「FM_EXEC = fm_shell」 to 「FM_EXEC = /usr/cad/synopsys/formality/2021.06/bin/fm_shell」 in /lab_formal/work/Makefile

You need to do …

- cd directory: ./lab_formal_release/lab_xxx/work
- Run the Makefile in the entire design flow
  - make all
    - Run all scripts in this stage
  - make clean
    - Clear whole results

Submission

- Please submit the following files to {NTHU eeclass / NTU COOL / NYCU E3} before **2024/4/28** :
  1. **report_TeamID.pdf**
  2. **Report contents must include the description of command in scripts (tcl file)**
  3. **The screenshot of every stage in design flow**
  4. **Discussion and observation**