Bridge of Life Education

Advanced SOC Design

Lab Plan

Jiin Lai

Lab List

Mandatory

1. fsic-sim – FSIC Simulation Environment
    1. fsic-sim (individual)
    2. fsic-plus – FSIC Improvement (team)
2. catapult-hls – Catapult HLS tool setup / HLS
    1. catapult-fir (individual)
    2. catapult-edgedetect (team)
3. snp-flow – Synopsys Front end and Back-end (team)
4. fsic-fpga – Caravel-FSIC + FPGA-FSIC + DMA (team)
5. hls-ap - HLS Application Accelerator – Kernel (team)
6. fsic-final – FSIC Final Project – FPGA & ASIC flow (team)

Optional

snp-lp – lower power design

snp-dft – design for testing

Sign-up IC Lab Account

Apply for Synopsys University Program

Fill-in the form below

https://docs.google.com/forms/d/e/1FAIpQLSeRX3jhYxEQuej5rRBainVW56eZKPLk2Mo1KrrtODhPkrVdDA/viewform?usp=sharing

FPGA – KV260

- KV260 – Embedded System
  - Vivado HLS – C-sim, Co-sim, IP-generation
  - Vivado Design Suite – IP integration, block-design, generate bit-stream
  - Download to PYNQ and run Jupyter Notebook

- Note: KV260 is twice of PYNQ-Z2 FPGA capacity

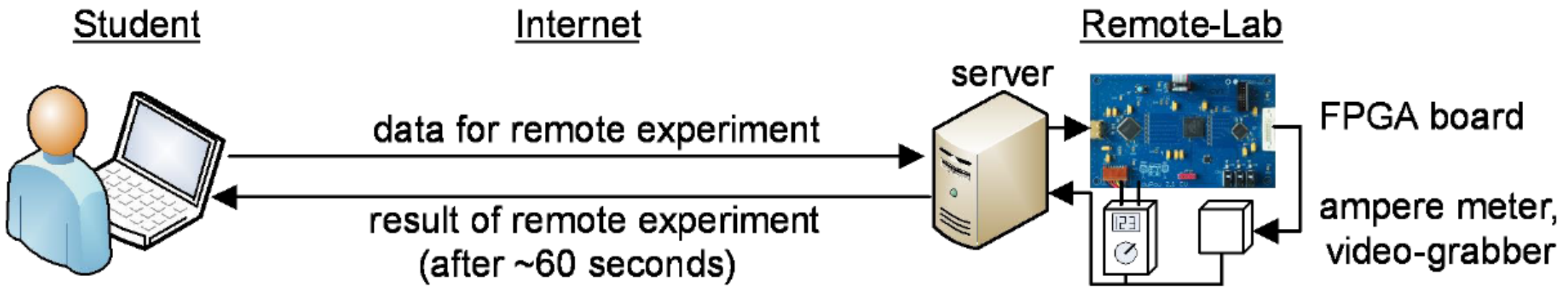
Build your Lab work on KV260

Tools

- Vitis/Vivado/Vitis HLS Software 2022.1
- Simens/Mentor Catapult/QuestaSim - Access from ICLab
- Synopsys - Access from ICLab
  - Design Compiler
  - ICC2
  - IC-Validator
  - Star-RC
  - Primetime

Online FPGA

- FPGA design software (Xilinx Vitis HLS) installed on student's computer
- Use Jupyter Notebook to access remote FPGA
- Locally compiled, simulated, and upload FPGA binary to remote FPGA
- Result of experiments shown in Jupyter Notebook
- Lab facilities
  - Cluster of Pynq-Z2/KV260 boards
  - Automate the FPGA board management (Demo)



Online FPGA Access

User Manual: (PYNQ-Z2/KV260)

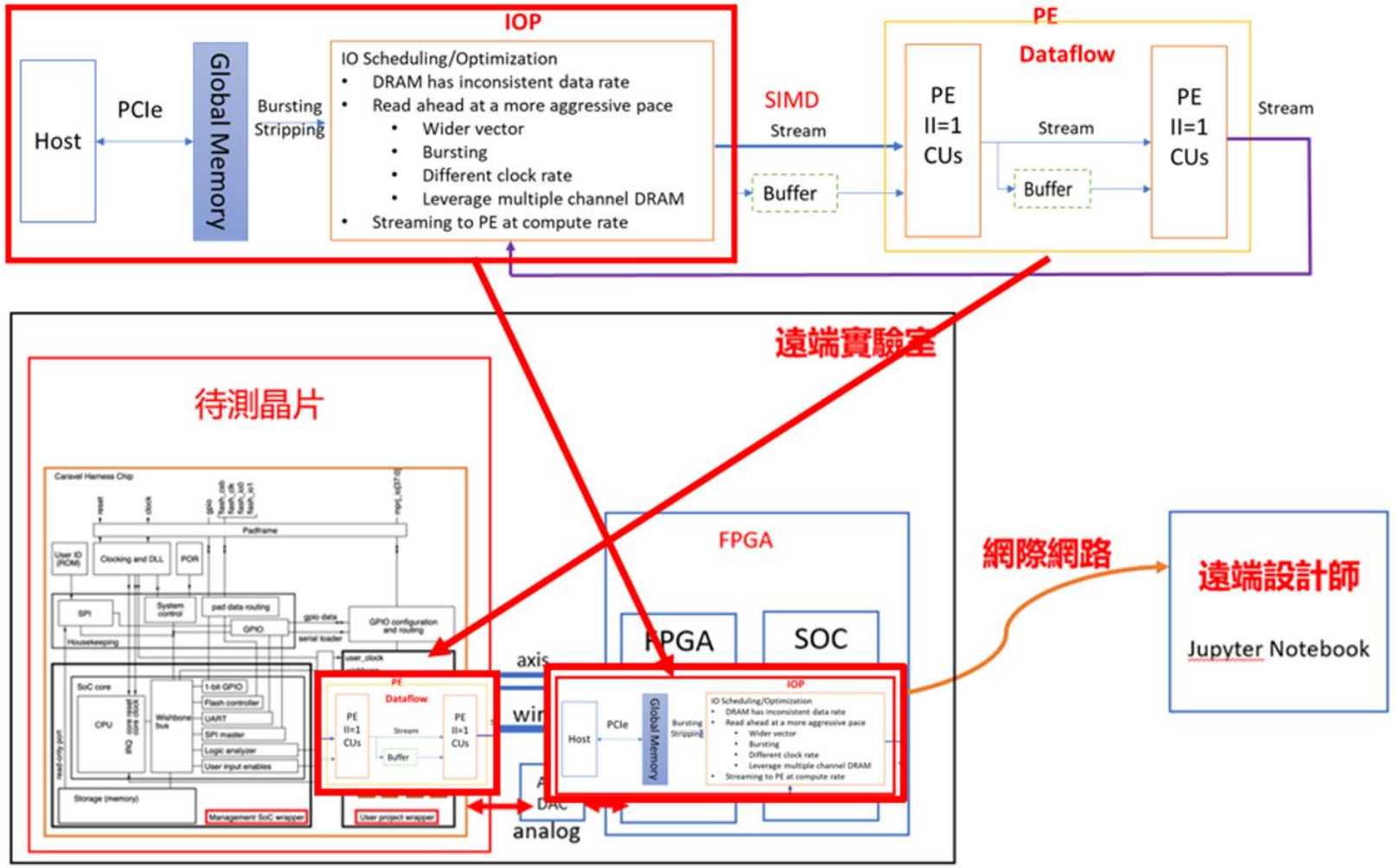
- https://drive.google.com/file/d/1Vx0e3m9EviOuqPVhowYVbgVunZxD828i/view

Advanced SOC Lab – Application Accelerator System

- Design an application accelerator system using HLS (Catapult) including
  - Kernel – Implemented in Caravel User Project Area (Catapult HLS)
  - IOP (Memory Subsystem) – Implemented in Xilinx KV260 (Vitis-HLS)
  - Firmware – Run on Caravel RISC-V
  - Application & Driver runs on KV260/PS ARM
- FPGA Validation
- Synopsys Signoff Flow

Selected final project for Chip tapeout

FSIC – Full-Stack IC System



Lab- fsic-sim – FSIC Simulation Environment

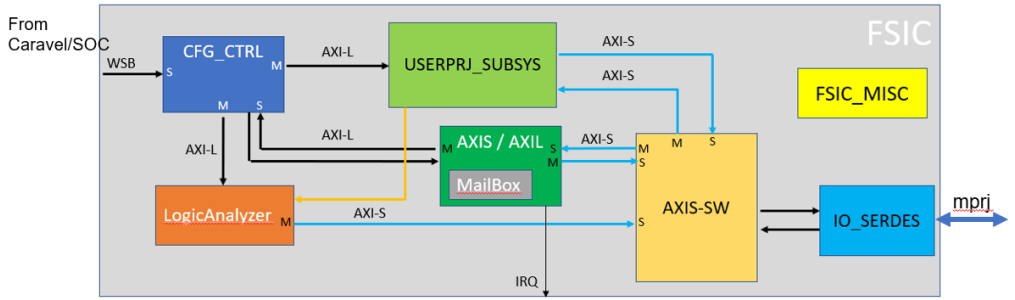
Target Goal

- Build up FSIC simulation environment
- Learn to integrate user project with FSIC

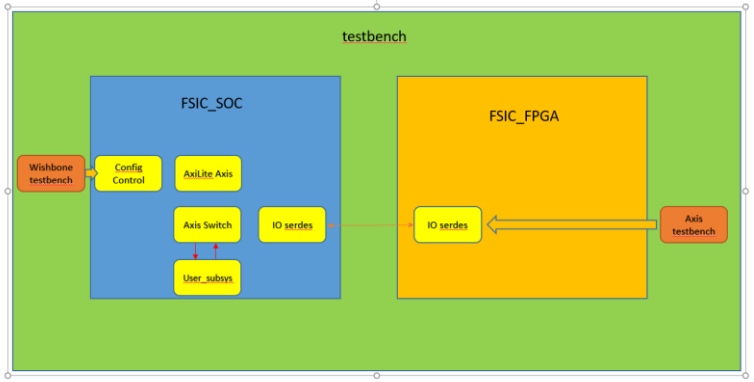
Implementation

- Integrate FIR (from SOC design course) into FSIC
- Develop Testbench
- Verify FIR in FSIC simulation environment

User Project Wrapper



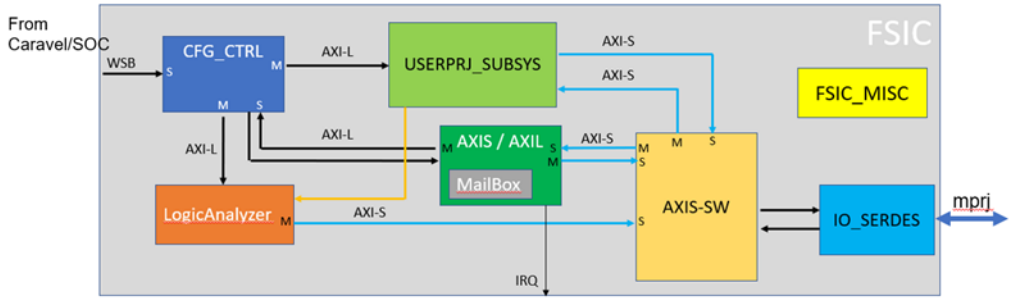
FSIC module testbench in fsic_tony



- Github: https://github.com/bol-edu/fsic_fpga/tree/main
- Reference: https://hackmd.io/@TonyHo/rk6Siw0k6

Lab – fsic-plus – Improve FSIC Design

- Each team choose a different topic
  - 6 topics: CC, AA, AS, IS, LA, testbench
- Improvement area
  - Better coding style
  - Area reduction
  - Cycle transaction latency reduction
  - Integration and verification – using FIR
- Report
  - Design document – data/control path
  - Compare the resource usage
  - cycle transaction latency reduction
  - Show code before and after
- Code review in Class



Lab - catapult-hls

Target Goal

- Learn Catapult HLS Tool
- Learn to design an accelerator with HLS & integrate with FSIC

Lab - catapult-fir (individual)

- Build up tool, and try out Catapult flow - there is no design effort

Lab - catapult-edgedetect (team)

- Based on 01_edgedetect/hls_c code, add the following
  1. Unroll to allow compute 4 pixels in a cycle
  2. Remove angle compute
  3. Edge magnitude changes from square root to sum of absolute difference. And compute its accuracy
  4. Perform crc32 generation for output stream, and crc32 checking for input stream.
  5. Output stream optionally selects bypass input stream or edge magnitude.
- Integrate with FSIC
- Integrate with Caravel SOC

Submission

Catapult Lab material:
https://drive.google.com/drive/folders/1tpe2SgbqCUe2RVJ2XSKtJIEjCsYz3gOX?usp=drive_link

Synopsys Training Course

1. **中文教學影片（Jumpstart Training by TW AEs）**
   - **平台：Synopsys Taiwan Webinar**
   - **網址：https://webinars.synopsys.com.tw/snpsdigitaldesign**

2. **英文教學影片（完整教學by 新思總部的客戶訓練團隊）**
   - **平台：Synopsys Learning Center**
   - **網址：https://training.synopsys.com/learn**

Synopsys Training Course

No	Video Title	Duration	Video Link
1	Design Compiler NXT - RTL Synthesis - Jumpstart	30 mins	https://training.synopsys.com/learn/course/internal/view/elearning/509/design-compiler-nxt-rtl-synthesis-jumpstart
2	Design Compiler NXT - RTL Synthesis - Foundation	10 hrs	https://training.synopsys.com/learn/course/internal/view/elearning/507/design-compiler-nxt-rtl-synthesis
3	IC Compiler II - Block Level Implementation - Jumpstart	30 mins	https://training.synopsys.com/learn/course/internal/view/elearning/519/ic-compiler-ii-block-level-implementation-jumpstart
4	IC Compiler II - Block Level Implementation - Foundation	21 hrs	https://training.synopsys.com/learn/course/557/ic-compiler-ii-block-level-implementation
6	StarRC Foundation	3 hrs 45 mins	https://training.synopsys.com/learn/course/internal/view/elearning/568/starrc-foundation
8	PrimeTime: Foundation	4 hrs 10 mins	https://training.synopsys.com/learn/course/internal/view/elearning/1194/primetime
9	PrimeTime: Jumpstart (Chinese)	1 hr	https://training.synopsys.com/learn/course/1287/play/6756/primetime-jumpstart-chinese
10	PrimeTime: Foundation (Chinese)	5 hrs	https://training.synopsys.com/learn/course/internal/view/elearning/1948/primetime-foundation-chinese
11	IC Validator: DRC Runset	6 hr	https://training.synopsys.com/learn/course/1682/ic-validator-drc-runset

Synopsys Flow Study

- Reference
  - Online courses
  - Tool documents
  - Lab scripts & flow
- Key topics - Each group assigned one of the following topics
  1. Design-compiler
  2. ICC2 - Floorplan
  3. ICC2 - Placement & Clock Tree Synthesis
  4. ICC2 - Routing & Finishing
  5. ICC2 - Multi-Voltage
  6. StartRC
  7. ICValidator
  8. PrimeTime

Lab - snp-flow : Synopsys IC flow

Target Goal: Learn IC frond-end and back-end design flow, including

- lab-synthesis
- lab1_planning
- lab2_pnr
- lab_startRC
- lab_pt
- lab_finishing
- lab_icv_drc
- lab_icv_lvs
- Lab_formal

- Implementation
  - Use FSIC-FIR to go through the flow
- Submission

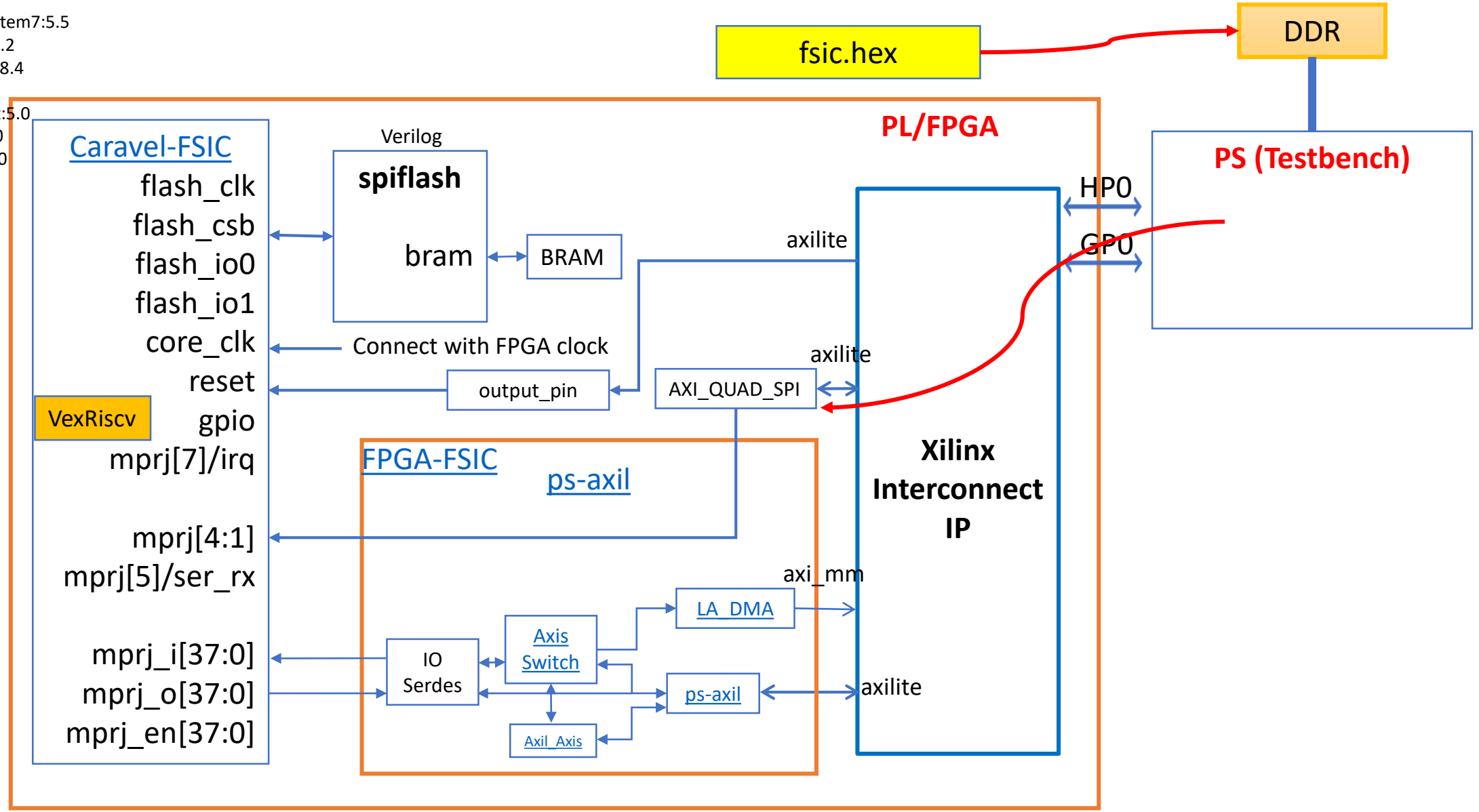
https://www.youtube.com/watch?v=C7NllCjs-9g

Lab fsic-fpga – Caravel+FSIC FPGA System

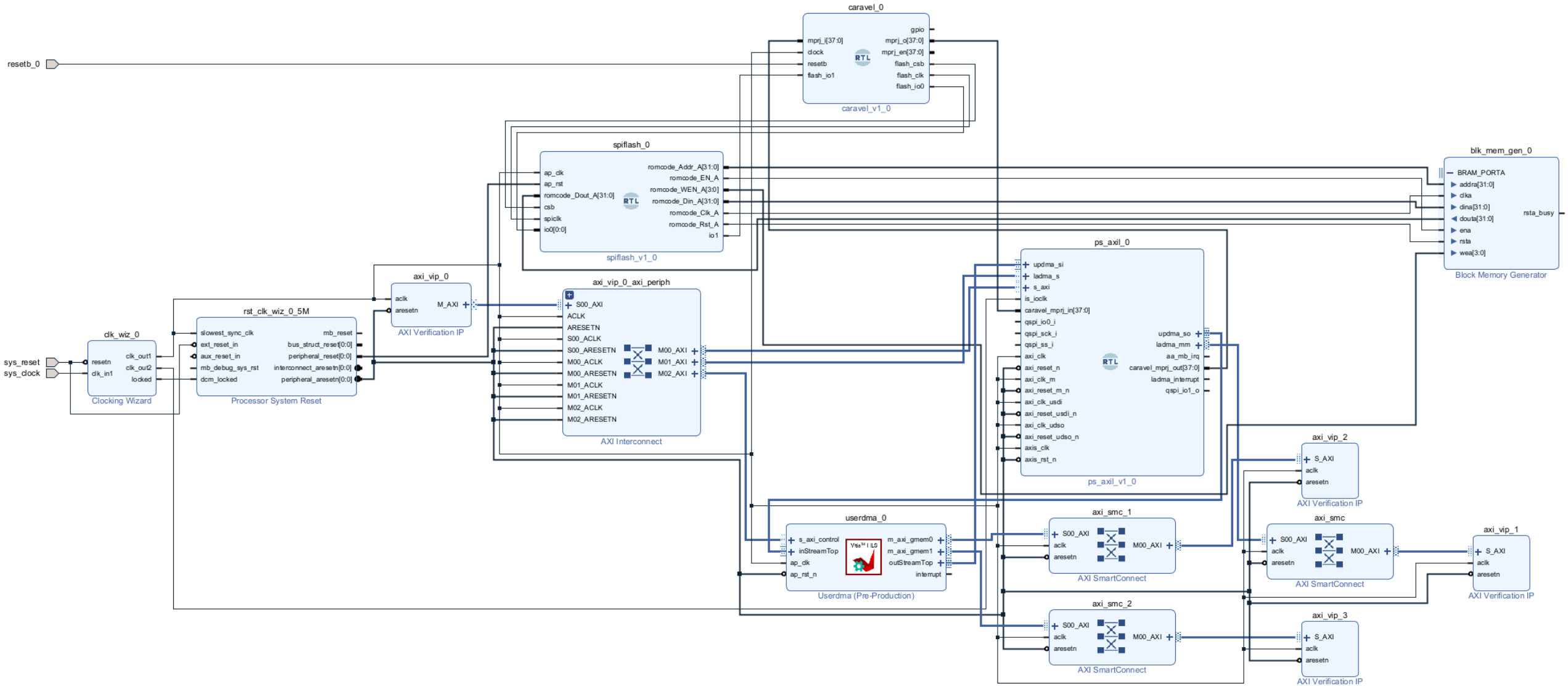
- Target goal
  - Implement complete Caravel-FSIC, FPGA-FSIC and HLS-DMA
  - Use for Caravel Chip pre-tapeout validation
- Implementation
  - Replicate and study the Github implementation
    - Caravel-FSIC FPGA Simulation
    - Caravel-FSIC FPGA Validation
  - Integrate FIR design into user project
    - Add User-DMA for FIR in FPGA
    - System validation with Python

Caravel-FSIC + FPGA-FSIC

xilinx.com:ip:processing_system7:5.5
xilinx.com:ip:axi_quad_spi:3.2
xilinx.com:ip:blk_mem_gen:8.4
xilinx.com:ip:clk_wiz:6.0
xilinx.com:ip:proc_sys_reset:5.0
xilinx.com:hls:caravel_ps:0.0
xilinx.com:hls:output_pin:0.0



Caravel-FSIC FPGA Simulation Block Design



Lab **hls-ap** – HLS Application Accelerator

Target Goal

- Develop an application accelerator and its DMA

Implementation

- Develop an application accelerator with axilite + axis interface using Catapult HLS
- Verify AP in FSIC-SIM environment
- Integrate AP + Caravel SOC and verify in simulation

Reference: Provide list of references

/home/raid7_4/raid1_1/linux/mentor/Catapult/2023.2/Mgc_home/shared/examples

Lab fsic-final – FSIC Final Project

Implementation

- Integrate AP into Caravel-FSIC FPGA (as in **lab fsic-fpga**)
- FPGA validation（**lab fsic-fpga**）
- Go through Synopsys IC flow (**lab snps-flow**)

Lab snps-dft – Design for Test (Optional)

- Refer to Design for test tutorial lab
- Implementation
  - Use FSIC+FIR design
  - DFT synthesis with Design Compiler
  - ATPG generation
- Detail pending on Synopsys AE

Lab snps-lp – Low Power Design (optional)

- Refer to lpmm lab
- Use FSIC + FIR (lab fsic-sim) to exercise
  - Clock_gating
  - Multi_voltage
  - multi_vt
  - Power_gating (power-gate FIR module)
- Detail pending on Synopsys AE