SOC Course-lab_3 Report

110000107 陳柏翰

- Briefly introduction of the system:
  - Just like lab2, but this time we had to using our own Verilog code to implement FIR.
  - Using two interfaces, AXI-Lite and Stream, to implement finite impulse response filter.
  - What's FIR?
    - A Finite Impulse Response (FIR) filter is a type of digital filter used in signal processing and digital signal processing. It is characterized by having a finite-duration response to an input signal, which means that the output of the filter is determined solely by a finite number of past and present input samples. In other words, the output of an FIR filter is based on a weighted sum of the input signal's samples within a finite time window.

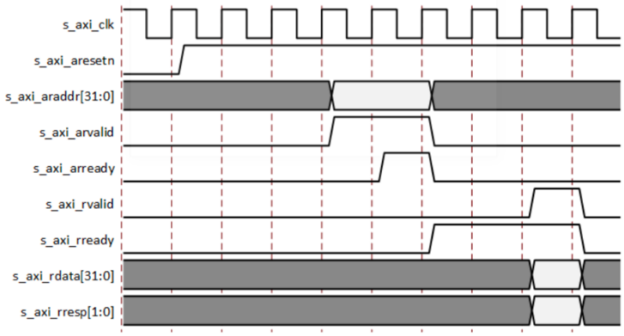
- What's observed and learned?
  - What's the properties of FIR?
    - Require no feedback. This means that any rounding errors are not compounded by summed iterations. The same relative error occurs in each calculation. This also makes implementation simpler.
    - Are inherently stable, since the output is a sum of a finite number of finite multiples of the input values, so can be no greater than times the largest value appearing in the input.
    - Can easily be designed to be linear phase by making the coefficient sequence symmetric. This property is sometimes desired for phase-sensitive applications, for

example data communications, seismology, crossover filters, and mastering.

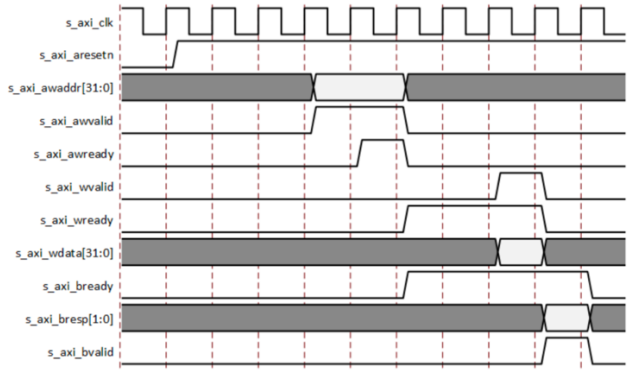
- $$y[n] = b_0 x[n] + b_1 x[n-1] + \cdots + b_N x[n-N]$$
$$= \sum_{i=0}^{N} b_i \cdot x[n-i],$$

- Verilog:
  - Using our own Verilog code to implement FIR, to get more familiar with Verilog design including the timing issue which is the most difficult task to debug.
  - How to implement the pipeline calculation is also a big learning in this lab from calculating the address and dealing with all the control signals.
  - Determine which signal is asynchronous or synchronous is also vital in this lab.

- AXI-Lite:
  - AXI Lite Interface has Master components, Interconnect, and Slave Components . User Logic connected to AXI-Lite Masters and AXI-Lite Slaves, and AXI-Lite Master and Slaves are connected via AXI-Lite Interconnect.
  - Transaction
    - Read

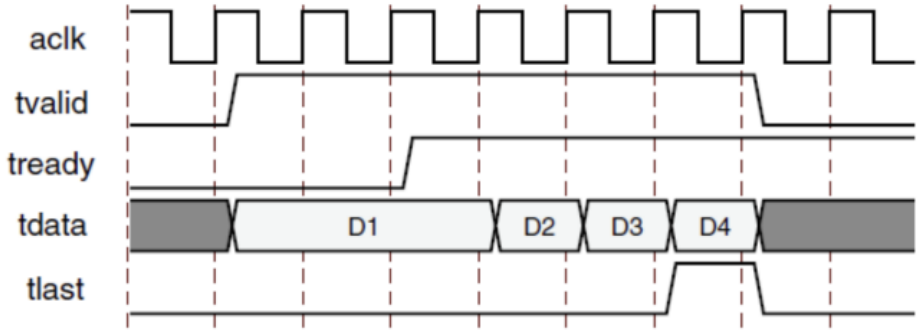


- Write



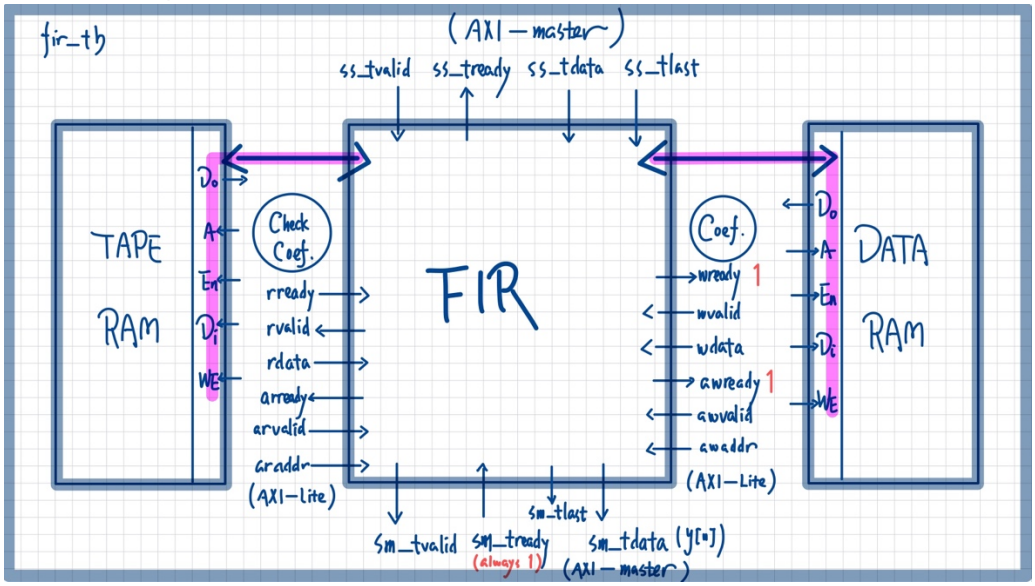
  - AXI-Stream:
    - Basic handshake:

      The following figure shows the transfer of data in an AXI4-Stream channel. The tvalid signal is driven by the source (master) side of the channel and tready is driven by the destination (slave) side. The tvalid signal indicates that the values in the payload fields (tdata and tlast) are valid. The tready signal indicates that the slave is ready to accept data. When both tvalid and tready are asserted in the same clock cycle, a transfer occurs.
    - Data transfer :

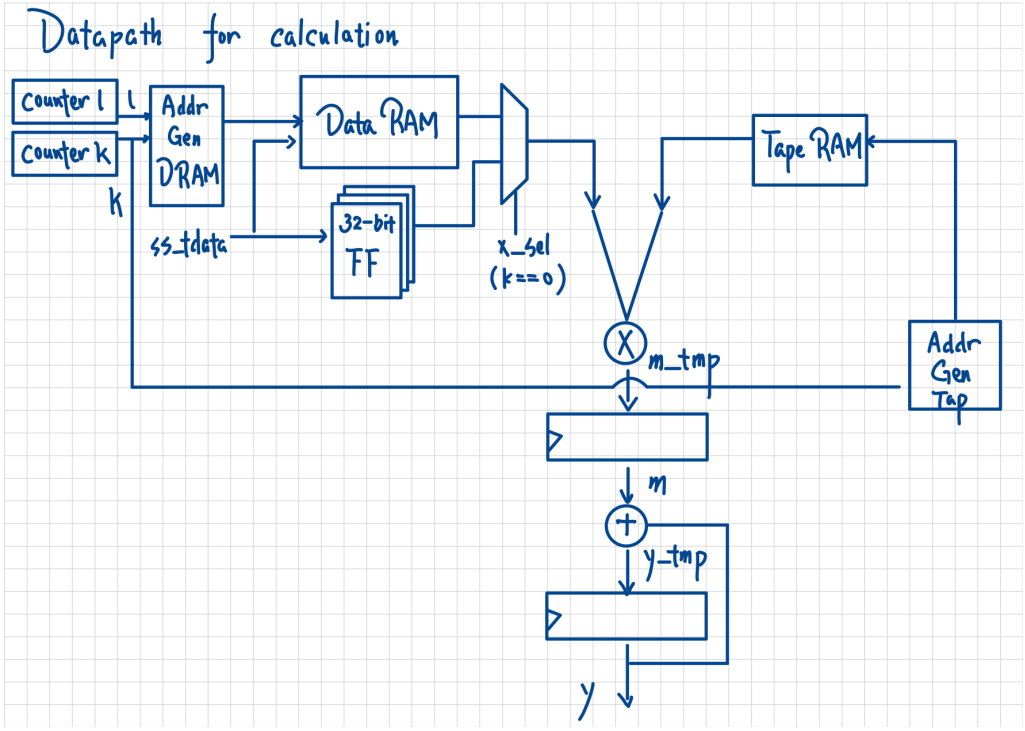


- Verilog Implementation:

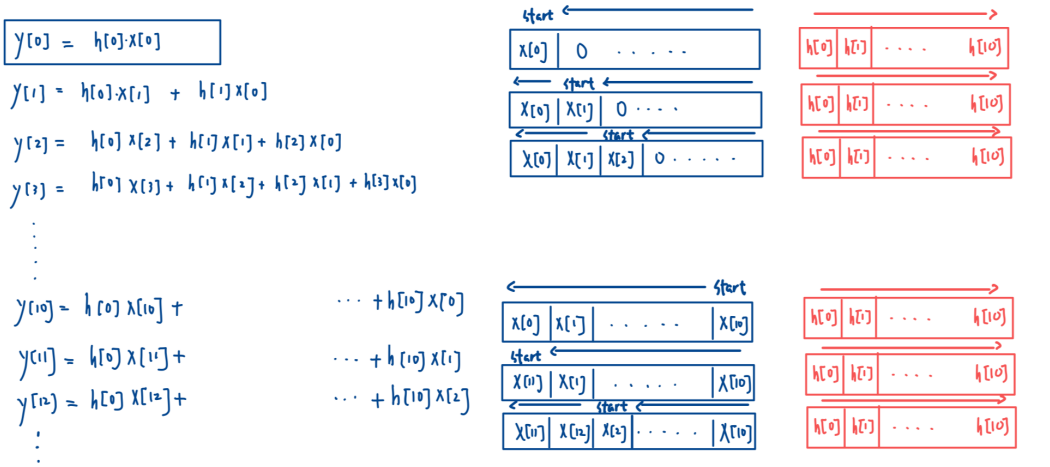
- Block diagram (with I/O)

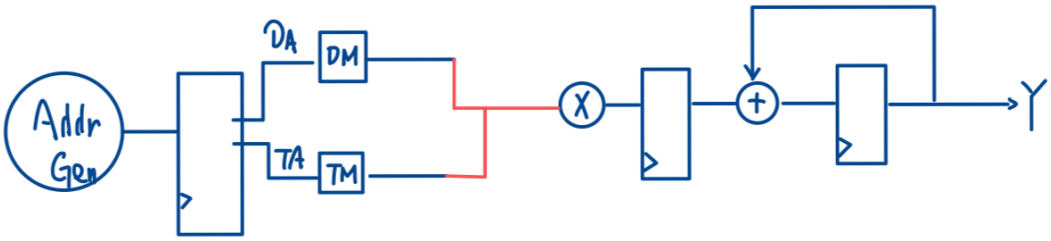


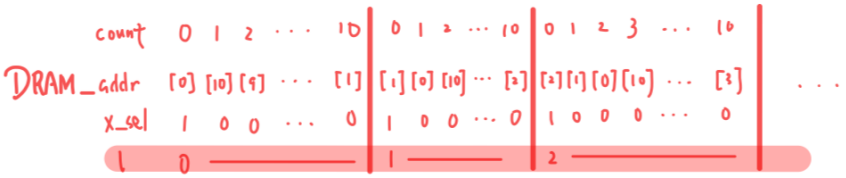
- Datapath for calculation



- FIR flow and ram arrangement








```
// ------ Address Generator for DRAM ------ //
reg [5:0] data_A_tmp;           // temp data address
reg [5:0] data_A_init;

always @* begin
    if (count <= 1) data_A_tmp = 6'd4 * (1 - count);
    else data_A_tmp = 6'd4 * (11 + 1 - count);
end
```

- Timing report
  - Timing constraint

```
create_clock -period 10.000 -name clk -waveform {0.000 5.000} -add [get_ports axis_clk]
set _xlnx_shared_i0 [all_inputs]
set_input_delay 2.000 $_xlnx_shared_i0
set _xlnx_shared_i1 [all_outputs]
set_output_delay -1.000 $_xlnx_shared_i1
```

- Timing summary

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.061 ns	Worst Hold Slack (WHS):	0.140 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	374	Total Number of Endpoints:	374	Total Number of Endpoints:	97

All user specified timing constraints are met.

- Longest path

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             0.061ns  (required time - arrival time)
  Source:                 val_count_reg[1]/C
                            (rising edge-triggered cell FDCE clocked by clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            rdata[1]
                            (output port clocked by clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             clk
  Path Type:              Max at Slow Process Corner
  Requirement:            10.000ns  (clk rise@10.000ns - clk rise@0.000ns)
  Data Path Delay:        8.447ns  (logic 4.275ns (50.614%)  route 4.172ns (49.386%))
  Logic Levels:           7  (CARRY4=1 LUT2=1 LUT6=4 OBUF=1)
  Output Delay:           -1.000ns
  Clock Path Skew:        -2.456ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    0.000ns = ( 10.000 - 10.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.000ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

- Max CLK cycle: 10ns

- Utilization

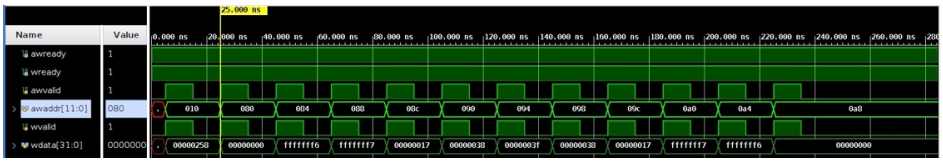
Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	131	0	0	53200	0.25
LUT as Logic	131	0	0	53200	0.25
LUT as Memory	0	0	0	17400	0.00
Slice Registers	94	0	0	106400	0.09
Register as Flip Flop	94	0	0	106400	0.09
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

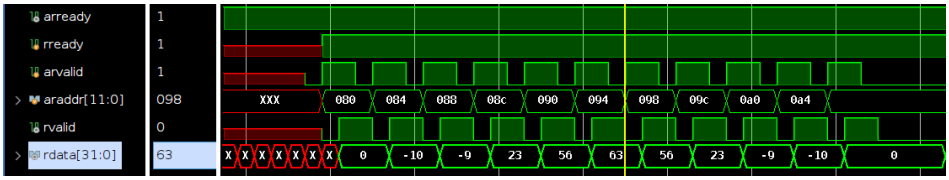
LUT	FF	BRAM	URAM	DSP
131	94	0	0	3

- Simulation Waveform

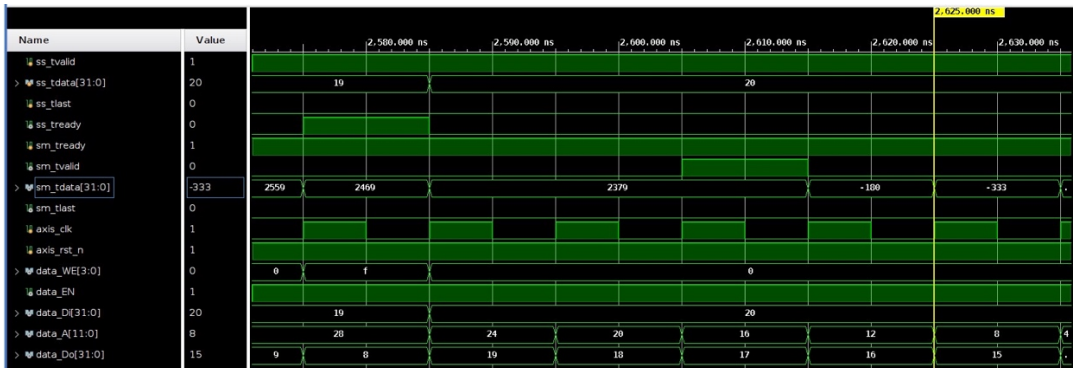
- Coefficient program and read back
  - Write coefficient



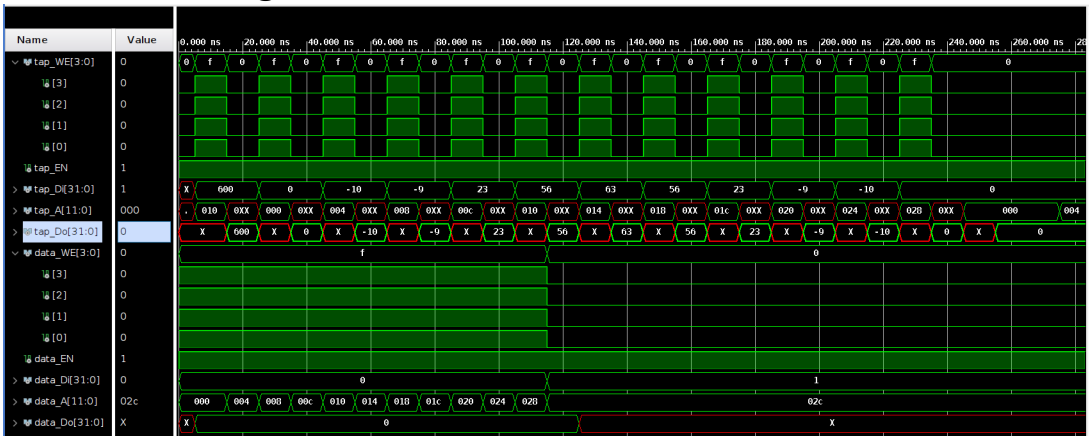
  - Read



- Data-in stream-in and Data-out stream-out



- RAM control signals



遲交理由：virtual machine 一直當機，所以我重載 ubuntu，加上住在宿舍，一直有停電問題，因此需要多這三天的 deadline 延期。