HSR
HOCHSCHULE FÜR TECHNIK
RAPPERSWIL
FHO Fachhochschule Ostschweiz

Very low-noise, programmable dual reference signal source from 1 to 400MHz

A compact hardware solution for phase noise measurement applications

Bachelor Thesis 2011/12

Advisor: Simon Flepp

Examiner: Prof. Dr. Heinz Mathis

Expert: Stefan Hänggi

Subject Area: Mobile Communication

Candidates: Alejandro Neff, Ramon Pfiffner

AnaPico of Switzerland

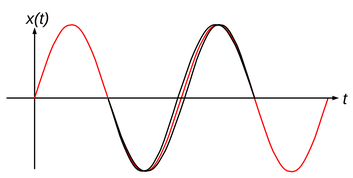
Introduction

Today's mobile communication systems are part of every day's life and their features and capabilities increase every year. Especially, modern modulation techniques allowing higher data rates make high demands on the signal precision.

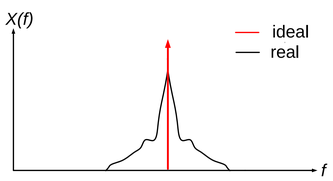
Phase noise is one of the most important parameters for signal precision and must continuously be improved to meet the increasing demands.

Generally, to be able to measure phase noise of a device under test (DUT), the measurement instrument requires a reference signal source with a much lower phase noise than the DUT.

The industrial project partner AnaPico AG manufactures phase noise measurement instruments based on the cross correlation method, requiring two adjustable and independent reference signal sources.



Jitter (time domain)



Phase noise (frequency domain)

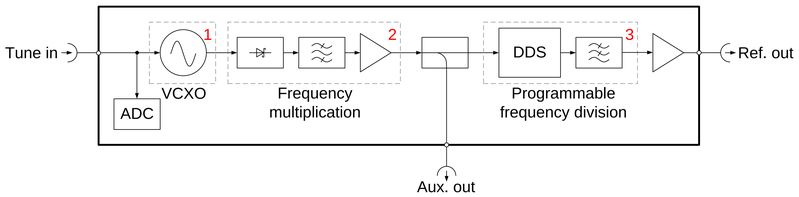
Task

The task of this thesis is to develop, build and test a reference signal source extension board for the existing hardware, according to following specifications:

- output frequency range: 1 to 400MHz
  - programmable by software
  - fine tunable by an external voltage signal
- phase noise: lower than -135dBc/Hz at 100MHz and 1kHz offset
- constant output power level: 13dBm ±1.5dB
- max. power consumption: approx. 3W per source
- overall PCB dimensions: 16×10cm (max. height approx. 2.5cm)

Design

Each reference signal source is designed according to the following block diagram:



Simplified overview of one reference signal source

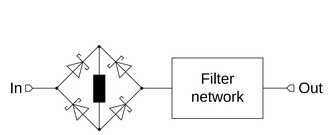
1. The frequency is generated and fine tunable by a voltage controlled crystal oscillator (VCXO).

2. A frequency multiplication system provides the system clock with low undesired harmonic and noise levels.

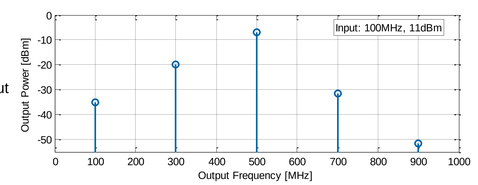
3. A programmable frequency divider is implemented with a direct digital synthesizer (DDS).

A high-order frequency multiplication

Odd-order harmonic generation is realized by a full-wave rectifier using Schottky diodes for low input power levels and low insertion loss.



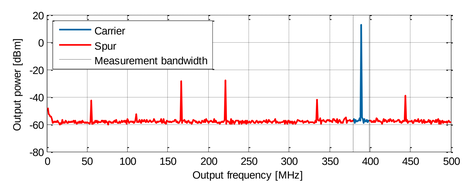
Bridge with inductor load



Schematic and simulated output frequency spectrum of the frequency multiplier

Spurious analysis

Spurs are aliasing products, generated by the time-sampling process and internal non-linearities of the DDS.

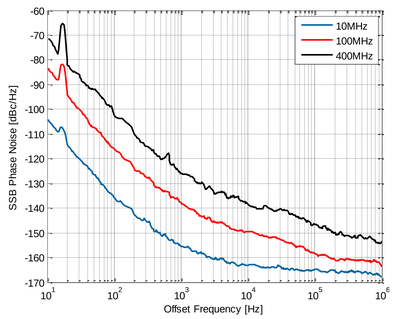


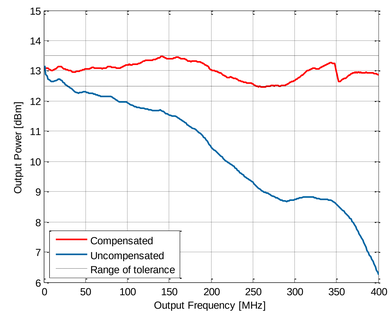
Output frequency spectrum with carrier and according spurious frequencies

Results

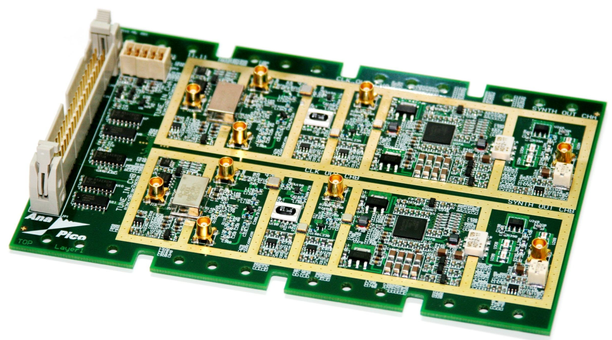
A fully functional system prototype is realized successfully. All required specifications are met. In addition, a specially designed software allows parameter setting adjustments for enhanced test and measurement purposes.

- The overall phase noise of every system depends on the actual oscillator used and is further increased by all following stages.
  The given VCXO has a phase noise value of -140dBc/Hz at 100MHz and 1kHz offset.
- The overall phase noise of each reference signal source is -138.5dBc/Hz at 100MHz and 1kHz offset, meaning the total degradation of the full system is only 1.5dB.
- An output power level tolerance of only ±0.5dB is achieved by applying a frequency-dependent compensation function in the firmware.
- The worst-case spurious free dynamic range value (SFDR) is -41dBc at 389MHz.





Output phase noise performance and frequency characteristic of the reference signal source



Assembled PCB with two equal reference signal sources