Modular System-Level Architecture for Concurrent Cell Balancing

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ABSTRACT

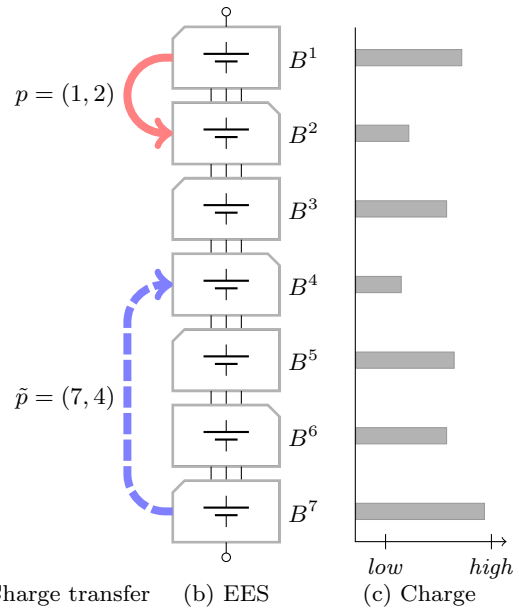
This paper proposes a novel modular architecture for Electrical Energy Storages (EESs), consisting of multiple series-connected cells. In contrast to state-of-the-art architectures, the presented approach significantly improves the energy utilization, safety, and availability of EESs. For this purpose, each cell is equipped with a circuit that enables an individual control within a homogeneous architecture. One major advantage of our approach is a direct and concurrent charge transfer between each cell of the EES using inductors. To enable a system-level modeling and performance analysis of the architecture, a detailed investigation of the components and their interaction with the Pulse Width Modulation (PWM) control was performed at transistor-level. At system-level, we propose a control algorithm for the charge transfer that aims at minimizing the energy loss and balancing time. The results give evidence of the significant advantages of our architecture over existing passive and active balancing methods in terms of energy efficiency and charge equalization time.

Categories and Subject Descriptors: B.7.1 [Integrated Circuits]: Types and Design Styles
General Terms: Algorithms, Design
Keywords: Active Cell Balancing, Charge Equalization, Battery Management, Modeling, Simulation

1 Introduction

Electrical Energy Storages (EESs) are widely used in many applications such as mobile devices, electric vehicles, or smart grids. To cope with high power and energy demands, series-connected EES topologies of Lithium-Ion (Li-Ion) cells are used in many domains. For instance, electric vehicles require a voltage of about $300V$ to $400V$ to drive the electric motor, resulting in about 100 Li-Ion series-connected cell modules with an individual voltage of about $3.7V$.

State-of-the-art EES architectures are strictly static and do not enable a charge transfer between cells. The drawback of these common architectures is a severe lack of flexibility, requiring a passive cell balancing such that the weakest cell determines the capacity of the entire EES. As a result, the lifetime, availability, and efficiency of these systems are deteriorated. To cope with these drawbacks, major efforts have been made within the recent years to reduce variations of individual Li-Ion cells in the manufacturing process. However, this had even further negative effects since it leads to very high production costs and prevents innovations in cell chemistries that often come along with significant variations.



(a) Charge transfer (b) EES (c) Charge

Figure 1: Illustration of the concurrent charge transfer (a) between adjacent cells B^1 and B^2 and non-adjacent cells B^7 and B^4 using the proposed EES architecture (b) to equalize the charge of the cells (c).

As a remedy, improved architectures were proposed that use balancing circuits, allowing a charge transfer between cells. These active cell balancing methods can cope with variances in the energy capacity and discharge behavior of different cells, improving the total capacity and lifetime of EESs. However, known approaches are still in an early development and require detailed investigations at system-level and transistor-level. Moreover, these approaches only allow balancing between adjacent cells, reducing the efficiency significantly. Therefore, we propose a novel modular architecture that enables bi-directional and non-adjacent active cell balancing, considering the control at system-level and the interaction with the transistor-level.

Contributions of the paper. In this paper, we propose a novel EES architecture and control as illustrated in Fig. 1. A major advantage of the proposed architecture over other approaches is the bi-directional and non-adjacent active cell balancing that is performed concurrently at runtime. This significantly reduces energy loss during balancing, cell fatigue,

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and also the time that is required to perform the cell balancing. As a result, the lifetime, availability, and efficiency of this EES is significantly improved. Moreover, by enabling the usage of low-cost cells with high variations, the additional costs of the balancing circuits might be compensated.

The contributions of this paper comprise (1) a novel homogeneous architecture based on basic building block circuits, (2) a switching scheme that enables the charge transfer between non-adjacent cells, (3) an analytical nonlinear closed-form model for the charge transfer behavior, and (4) a system-level control algorithm for charge transfer that takes advantage of the proposed architecture:

1. We propose an EES architecture that consists of homogeneous modular blocks, combining a cell with six power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and an inductor. This enables the exchange of charge between individual cells while it also makes the the overall cell integration more flexible.

2. Our proposed switching scheme enables a concurrent charge transfer between non-adjacent cells in both directions. This significantly reduces the energy loss and improves the charge transfer time compared to other known active cell balancing architectures.

3. We propose an analytical nonlinear closed-form model for the charge transfer behavior that not only applies to our circuit, but that also enables a detailed analysis of related work that until now relied on time-consuming numerical simulation. A speed-up of three orders of magnitude can be achieved at similar accuracy. This enables the development of control algorithms and system-level optimization techniques for charge transfer beyond the scope of this paper.

4. At system-level, we propose a control algorithm that performs the charge transfer for the proposed architecture. The case study gives evidence of the practicability of the proposed balancing architecture and control by significantly reducing overall energy loss and charge equalization time compared to passive balancing and other active balancing methods.

Organization of the paper. The remainder of the paper is organized as follows: Section 2 discusses related work in the domain of architectures and control for EESs. Our novel balancing architecture is introduced in Section 3, comprising the architecture and switching scheme. In Section 4, an analytical model is proposed that enables a system-level analysis and a development of a control algorithm for the charge balancing. Section 5 presents a model validation and a detailed case study, comparing the proposed architecture and model to results from previous work. Finally, Section 6 makes concluding remarks.

2 Related Work

With a growing amount of electronics and control in EESs, the design of complex EESs is becoming increasingly relevant in the embedded systems domain. Already common system-level battery management systems as discussed in [1] require a significant amount of embedded control. In [2] and [3], hybrid EESs and appropriate control strategies are discussed, proposing an optimization for cycle efficiency and charge management algorithms, respectively. Integrating more intelligence at the cell-level of a modular battery and thus decentralizing its management is discussed in [4].

In all architectures, cell balancing is a crucial part of the EES control and a system-level analysis and optimization is becoming increasingly important. A comprehensive overview of cell balancing methods is presented in [5]. In [6], a passive cell balancing is presented where energy dissipation of cells with higher charge levels is realized using switched resistors. Although this approach is easy to implement and very common, it is wasting energy during balancing in form of heat. An approach to isolate cells from the series-connected battery is introduced in [7] with the goal to reach an equal charge level during a charging process. However, an active balancing with this approach is not possible.

Active cell balancing approaches aim at equalizing the charge of cells in an EES. Charge equalization using an inductor as an active charge transfer element is proposed in [8] while another DC-DC converter based balancing technique is presented in [9]. However, all these approaches have the drawback that the charge transfer is only possible between adjacent cells or with further circuit complexity between close cells [10]. Therefore, significant energy losses occur when transferring charge between distant cells in a series-connected EES.

In this paper, we propose an architecture that enables active cell balancing between non-adjacent cells, improving the efficiency of the EES significantly compared to all existing approaches. The proposed architecture consists of modular building blocks that make a flexible and extensible EES design possible. Furthermore, a system-level model has been developed that allows a fast and accurate analysis of our architecture in a high-level EES framework to propose and simulate charge transfer control algorithms.

3 EES Architecture

In this section, the proposed EES architecture is introduced. First, the system-level concept for charge transfer is presented before the basic blocks are explained. A switching scheme to enable the concurrent charge transfer between non-adjacent cells is proposed and explained based on the example from Fig. 1.

System-level charge transfer. The charge transfer at system-level is controlled by the set of pairs $\mathcal{P}$ that is determined at each time step. The set $\mathcal{P}$ consists of elements $p = (\sigma, \delta)$ where σ denotes the source cell and δ denotes the destination cell of a charge transfer. An example of this charge transfer at system-level is illustrated in Fig. 1 where $\mathcal{P} = \{(1,2),(7,4)\}$. Note that $\sigma, \delta \in \mathbb{N}$ are cell indexes denoting a cell's position in the series-connected EES.

The set $\mathcal{P}$ needs to fulfill the following requirements to be considered feasible for charge transfer. Source and destination of a transfer cannot be identical:

$$\sigma \neq \delta \quad \forall p = (\sigma, \delta) \in \mathcal{P} \tag{1}$$

Additionally, transfers have to be performed on disjoint sets of cells with at least one cell between pairs from $\mathcal{P}$. This avoids merging currents of concurrent balancing processes. Formally, it has to hold for any $n \in \mathbb{N}$ and any two non-identical pairs $p = (\sigma, \delta), \tilde{p} = (\tilde{\sigma}, \tilde{\delta}) \in \mathcal{P}$:

$$\big(n \in [\min(\sigma,\delta) - 1, \max(\sigma,\delta) + 1]\big) \Rightarrow \big(n \notin [\min(\tilde{\sigma},\tilde{\delta}), \max(\tilde{\sigma},\tilde{\delta})]\big) \tag{2}$$

Module-level charge transfer building block. Our proposed architecture consists of homogeneous modular charge transfer blocks, comprising the individual cells as illustrated in Fig. 2. Note that each cell might be a parallel composition of single cells, increasing the energy capacity of the EESs. The blocks are asymmetrically (observe the location of L^i) connected in series as illustrated in Fig. 1 while Fig. 3 illustrates the identical architecture at module-level.

One basic building block consists of six power MOSFETs used as switches as well as one inductor. Each MOSFET might be *closed* or *open*, corresponding to the N-MOS tran-

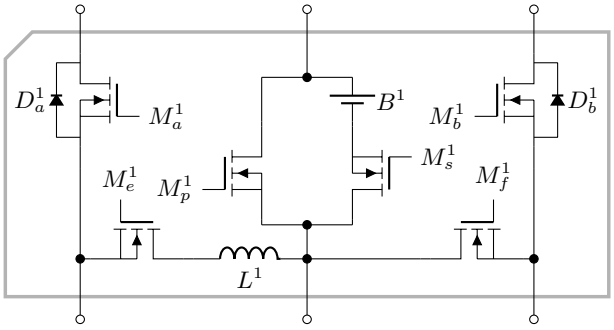

Figure 2: The basic building block of the modular charge transfer circuit attached to a cell (B^1), consisting of six MOSFETs and an inductor.

sistor conducting in state *ON* (closed switch, logical 1) and not conducting in state *OFF* (open switch, logical 0), respectively. The M_s^i is in series with the cell while the parallel M_p^i adds the capability of bypassing or isolating cells which is used to increase the safety and reliability of the EES in case of failure of one cell. During normal operation of the EES where all cells are series-connected, all M_s^i are closed while the M_p^i remain open. For balancing purposes, M_a^i and M_b^i can be controlled via PWM signals, enabling the active charge transfer process via the inductors. Diodes D_a^i and D_b^i are protection diodes of the power MOSFETs, preventing destructive voltage spikes during switching of the PWM when the inductor current cannot flow across a transistor. M_e^i and M_f^i are routing switches that are required to avoid horizontal currents. Most of the MOSFETs can remain constant during one particular balancing operation.

While the MOSFETs M_s^i and M_p^i have to be capable of coping with high voltages and currents, the remaining MOSFETs are only exposed to significantly lower voltages and currents that occur during the cell balancing. This ensures that the charge transfer block remains a cost-efficient solution.

Switching scheme. To ensure the correct charge transfer for a given $\mathcal{P}$, the MOSFETs have to be switched correctly. For this purpose, we define the function

$$x_{M_j^i} : 2^{\mathcal{P}} \to \{0, 1, PWM, \overline{PWM}\} \tag{3}$$

that determines whether the corresponding switch is open (0), closed (1), or controlled by a PWM signal (PWM or $\overline{PWM}$). Here, M_j^i refers to MOSFET j in the i-th cell of the string. More precisely, superscript $i \in \{1, \ldots, 7\}$ in Fig. 3 and subscript $j \in \{a, b, p, s, e, f\}$. The switching rules are defined in Section S1.

Note that accurately controlled signals PWM and $\overline{PWM}$ minimize usage of the protection diodes of the MOSFETs, resulting in a significantly improved efficiency over previous approaches that used diodes instead of a non-overlapping PWM control. For this purpose, the discharge time of the inductor determining T_{OFF} needs to be calculated very precisely such that the cell cannot discharge itself through the inductor.

Switching scheme example. For a better understanding of the circuit and the switching scheme, the example depicted in Fig. 3 is considered. The resulting switching is summarized in Table 1 and explained in the following.

First, the transfer of charge between adjacent cells shall be considered which is the case for the transfer from B^1 to B^2. We thus transfer the excess charge via inductor L^1. M_s^1 and M_s^2 are closed and M_p^1 and M_p^2 open in order to discharge and charge the cells, respectively. Note that M_p^3 and M_s^3 are open to isolate the current charge transfer process. M_a^1

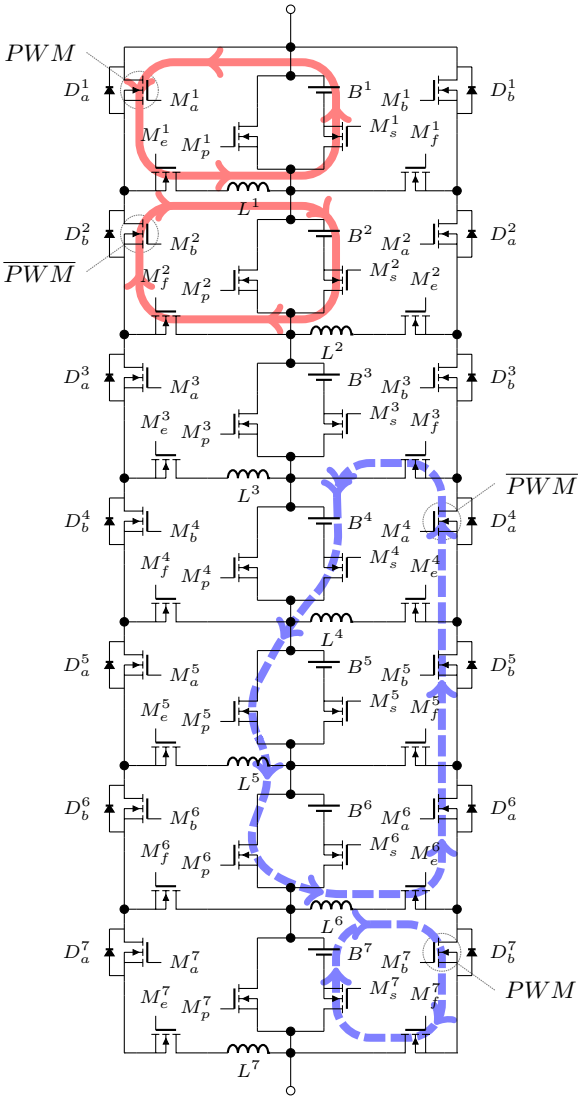

Figure 3: Illustration of the charge transfer in the proposed EES architecture for a determined MOSFET switching. Charge is transfered concurrently between neighbor cells with $p = (1, 2)$ ( ) and non-adjacent cells with $\tilde{p} = (7, 4)$ ( ).

and M_b^1 are activated by an alternating PWM signal. During the time the signal PWM closes M_a^1 – a period that we will refer to as T_{ON} – inductor L^1 is charged from cell B^1 via M_a^1. Afterwards, M_a^1 is opened for a time of T_{OFF} and the inductor is discharged through M_b^2 into cell B^2. M_b^2 is closed by the corresponding non-overlapping signal $\overline{PWM}$, see Fig. 4. Non-overlapping signals are required in order to avoid energy loss due to shortened current paths by introducing a dead time. Note that charge transfer would even be possible if the charge level of B^2 was higher than that of B^1 due to the DC-DC converter behavior of the circuit.

In addition to charge transfer between adjacent cells, the proposed architecture can directly transfer charge between non-adjacent cells. This is illustrated in Fig. 3 where cell B^7 transfers charge to cell B^4. For this purpose, M_s^i is closed for $i = 4, 7$ while M_p^i is opened for $i = 5, 6$. This isolates cells B^5 and B^6 from the electric circuit and allows the current flow to bypass them. Switch M_a^7 is activated by signal PWM

i	M_a^i	M_b^i	M_e^i	M_f^i	M_p^i	M_s^i
1	PWM	1	1	0	0	1
2	1	$\overline{PWM}$	0	1	0	1
3	1	1	0	1	0	0
4	$\overline{PWM}$	1	0	0	0	1
5	1	1	0	0	1	0
6	1	1	1	0	1	0
7	1	PWM	0	1	0	1

Table 1: MOSFET switch states for concurrent charge transfer from B^1 to B^2 and from B^7 to B^4. 0 denotes OFF (open) and 1 denotes ON (closed). Note that inductors L^i of adjacent cells are on opposite sides.

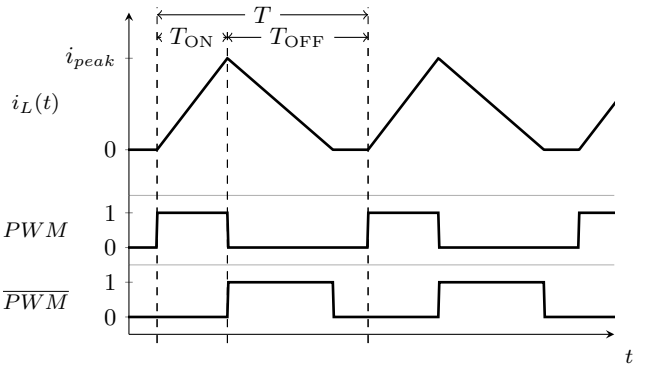

Figure 4: Inductor current $i_L(t)$ during T_{ON} and T_{OFF} with corresponding signals PWM and $\overline{PWM}$.

and M_a^4 by its non-overlapping corresponding $\overline{PWM}$. During T_{ON}, cell B^7 charges inductor L^6 which – during T_{OFF} – discharges into cell B^4 using the path $M_e^6 \rightarrow M_a^6 \rightarrow M_b^5 \rightarrow M_a^4 \rightarrow M_f^3 \rightarrow B^4 \rightarrow M_s^4 \rightarrow M_p^5 \rightarrow M_p^6$. To prevent horizontal currents during T_{OFF}, switches M_e^4 and M_f^5 remain open. Switches M_b^5 and M_a^6 remain closed to avoid the voltage drop incurred from routing over the diodes.

4 System-level Model

In this section, the development of a nonlinear analytical closed-form model for the behavior of the proposed circuit is presented that enables system-level simulation, optimization, and control algorithm engineering.

Analytical system-level model for transistor-level abstraction. A verification of the qualitative behavior of the proposed balancing circuit from Section 3 is possible, using analog circuit simulators such as LTspice IV [11] where cells are modeled by a capacitance-based model. This is, however, only feasible for a small number of our building blocks as the numerical simulation is not well scalable. The numerical solver of the simulator uses very short time steps for the iterative solutions of the system that contains continuous analog behavior in conjunction with discrete PWM signals, resulting in very long computation times. Furthermore, analog circuit simulators run into numerical problems for complex systems like full scale EESs. Hence, a transistor-level analysis of the proposed architecture with numerical approaches becomes infeasible and a system-level model has to be developed for the analysis of balancing algorithms for the EES.

It is therefore necessary to develop faster, scalable, and more abstract simulation models that retain the accuracy of the transistor-level analysis at system-level. The goal is to capture the quantitative behavior of 100 and more circuit building blocks within a real-world EES for an accurate analysis, enabling the development of system-level charge routing algorithms.

For an accurate analysis of the circuit behavior, the system configurations during T_{ON} and T_{OFF} need to be considered separately. Fig. 4 illustrates the behavior of the inductor current $i_L(t)$ of one basic building block controlled by PWM and $\overline{PWM}$, respectively. For each of the phases T_{ON} and T_{OFF}, an equivalent circuit can be identified for the path of the current flow through the inductor, cell, and transistors. For these components in the current flow, according to Kirchhoff's Voltage Law, an equation can be set up to describe the circuit behavior. Consider, for instance, the loop of the current flow through cell B^1 in Fig. 3. Applying Kirchhoff's Voltage Law to this part of the circuit results in the following equation:

$$L \cdot \frac{\mathrm{d}}{\mathrm{d}t} i + R_\sigma \cdot i + \frac{1}{C} \int_0^{T_{\text{ON}}} i(\tau)\ \mathrm{d}\tau - V_1 = 0 \qquad (4)$$

The series resistance R_σ models the inductor series resistance R_L, the cell series resistance R_C, and the ON-resistance R_M of the MOSFETs in the current path. All other current flow equations within the system can be modeled correspondingly as described in detail in Section S2 by adapting the series resistance R_σ as described in Table 3. Once R_σ is obtained as well as suitable initial conditions, we can treat the various cases using methods from [12] to determine a very accurate *nonlinear* closed-form solution for the charge transfer. This proposed nonlinear equation system is detailed in Section S2. To simplify and implicitly speed-up the nonlinear model with a reasonable loss in accuracy (see Section 5.1), a *linear* model is obtained by assuming a linear inductor current as presented in Section S2.6.

The individual PWM signals between charge transfer pairs in $\mathcal{P}$ do not need to be synchronized mutually. Instead for each $p = (\sigma, \delta) \in \mathcal{P}$, the source σ and destination δ need to synchronize their respective PWM and $\overline{PWM}$ signals. In the following, we consider the peak current i_{peak} as in Fig. 4 as input from the control level. We can then calculate T_{ON} and T_{OFF} using the formulas from Section S2.3 to S2.6.

System-level cell balancing control algorithm. In order to enable the cell balancing for the presented architecture from a system-level perspective, we propose a control algorithm $A_{K,r}$ that is outlined in Algorithm 1. The main parameters that can be used to adjust the behavior are K that is the number of maximal concurrent transfers and r that is the maximal allowed distance for charge transfer. The algorithm balances the charge levels Q of N cells until a normalized variance of the charge level falls below a predefined threshold (line 1). The charge equalization is performed in time steps T_M by defining the charge transfer pairs $\mathcal{P}$. Initially, the set $\mathcal{P}$ is empty while $\mathcal{V}$ is the set of all available cells that can be used for the charge transfer (line 2). In each time step, the algorithm determines pairs for charge transfer iteratively until there are no available cells or the maximum of concurrent transfers K is reached (line 3). The control scheme selects as sender σ the available cell with the highest charge (line 4) and transfers from there into the direction of the lower mean. For this purpose, the average charge levels of cells preceding and succeeding the sender σ, $\bar{Q}_{\text{prec}}$ and $\bar{Q}_{\text{succ}}$, respectively, are calculated and compared to determine the direction 1 or -1, respectively (line 5-7). Once the transfer direction is determined, the algorithm checks for the maximal possible distance ν that allows a transfer via available cells (line 8). The destination cell δ is then chosen as the cell with the least amount of charge among those between σ and ν in the determined direction (line 9). If the difference in charge levels of σ and δ is above a certain threshold (line 10),

Algorithm 1 System-level cell balancing control algorithm $A_{K,r}$ where K is the number of maximal concurrent transfers and r is the maximal distance for charge transfer.

IN: Unbalanced charge array Q, macro step size T_M
OUT: Balanced Charge Array Q

1: **while** $\mathrm{Var}(Q)/\mathrm{avg}(Q) > 0.01$ **do**
2: $\quad\mathcal{P} = \{\}, \mathcal{V} = \{1, \ldots, N\}$
3: $\quad$**while** $\mathcal{V} \neq \{\} \wedge |\mathcal{P}| < K$ **do**
4: $\quad\quad\sigma = \arg\max_{j \in \mathcal{V}} Q^{(j)}$
5: $\quad\quad\bar{Q}_{\mathrm{prec}} = \frac{1}{\sigma - 1} \sum_{j=1}^{\sigma-1} Q^{(j)}$
6: $\quad\quad\bar{Q}_{\mathrm{succ}} = \frac{1}{N - \sigma - 1} \sum_{j=\sigma+1}^{N} Q^{(j)}$
7: $\quad\quad\mathrm{dir} = \mathrm{signum}(\bar{Q}_{\mathrm{prec}} - \bar{Q}_{\mathrm{succ}})$
8: $\quad\quad\nu = \max\left\{k \in \mathbb{N}_{[0,r]} \;\middle|\; (\sigma + \mathrm{dir} \cdot l) \in \mathcal{V} \quad \forall l \in \mathbb{N}_{[0,k]}\right\}$
9: $\quad\quad\delta = \underset{j \in \{\sigma, \ldots, \sigma + \mathrm{dir} \cdot \nu\}}{\arg\min} Q^{(j)}$
10: $\quad\quad$**if** $\left|Q^{(\sigma)} - Q^{(\delta)}\right| > 0.001$ **then**
11: $\quad\quad\quad\mathcal{P} = \mathcal{P} \cup \{(\sigma, \delta)\}$
12: $\quad\quad\quad\mathcal{V} = \mathcal{V} \backslash \{\min(\sigma, \delta) - 1, \ldots, \max(\sigma, \delta) + 1\}$
13: $\quad\quad$**else**
14: $\quad\quad\quad\mathcal{V} = \mathcal{V} \backslash \{\sigma\}$
15: $\quad\quad$**end if**
16: $\quad$**end while**
17: $\quad$Perform transfers in $\mathcal{P}$ for a duration of T_M
18: $\quad$Adjust Q according to transfers
19: **end while**

(σ, δ) is added to $\mathcal{P}$ (line 11) while all cells in between and the outer neighbor cells are removed from the set of available cells (line 12). Otherwise, only the current source cell is removed from the set of available cells (line 14). After the set $\mathcal{P}$ is determined, the circuit then transfers charge according to $\mathcal{P}$ for the selected macro time T_M (line 17), before adjusting the Q values and continuing in the next time step (line 18). This is repeated until distortion measure $\mathrm{Var}(Q)/\mathrm{avg}(Q)$ is sufficiently small, i.e., until the cells are considered balanced (line 1).

Note that K is the most important adaptation parameter. If it is small, energy conservation is valued higher, if it is large, balancing time is given more attention. On the other hand, r is constrained by the circuit which is $r = 1$ for active cell balancing with adjacent charge transfer only and for the non-adjacent charge transfer circuit in the proposed approach it can be chosen more flexibly with $r \leq N$.

5 Experimental Results

This section presents experimental results on the validation of our analytical system-level model as well as a case study to illustrate the benefits of our EES architecture and the proposed control algorithm. All experiments were carried out on an Intel i5 @ 2.50 Ghz with 4GB RAM.

5.1 Model Validation

In this section, we compare the analytical nonlinear model and its linear approximation described in Section 4 and detailed in Section S2 to the LT SPICE IV [11] numerical simulation for validation purposes.

Accuracy. To determine the accuracy of the proposed analytical approach, we compared a simulation run in SPICE with the results from our system-level model. Both the nonlinear and linear model stay within a very close range of the SPICE simulation. The linear model for $i(t)$ does not exceed a relative error of 1% to the SPICE reference solution while the nonlinear model remains within even tighter bounds, not exceeding 0.1% relative error.

	T_{ON} $[ms]$	T_{OFF} $[ms]$	q_σ $[As]$	q_δ $[As]$
SPICE	0.12539	0.16582	3.14e-4	4.14e-4
linear	0.125	0.16442	3.1447e-4	4.1102e-4
rel. error	0.3%	1%	0.1%	0.7%
nonlinear	0.12546	0.16552	3.1371e-4	4.1288e-4
rel. error	0.05%	0.2%	0.1%	0.2%

Table 2: Comparison of the results of the switching time and transferred charge of the linear and nonlinear analytical model to the SPICE simulation. The relative error remains very small, validating the proposed system-level models.

Additionally, we compared the different approaches for calculating the PWM periods T_{ON} and T_{OFF} as well as the transferred charge amounts q_σ and q_δ. T_{ON} and T_{OFF} are obtained from the SPICE simulation as the points in time where $i(t)$ crosses the corresponding threshold values $i(t) = 0$ and $i(t) = i_{\mathrm{peak}}$, respectively. The values q_σ and q_δ are the changes in charge that correspond to T_{ON} and T_{OFF} in SPICE. Section S2 details how the nonlinear and the linear models handle these computations. Table 2 summarizes the results of a representative comparison with $i_{\mathrm{peak}} = 5.0A$ (see Fig. 4). Again, the relative error of the linear model remains below 1% while the nonlinear model achieves almost negligible relative errors of less than 0.3%.

Speed-up. To estimate the speed-up of the analytical solutions over the numerical SPICE simulation, we ran various simulations over a length of 200 PWM cycles. The SPICE simulator averaged a runtime of $130s$ over different scenarios with optimized solver settings which was compared to our prototypical Python Scipy [13] implementation. Note that every PWM cycle was evaluated individually. Further speed-up might be obtained by combining PWM cycles and extending the evaluation of the first cycle to all of them. The nonlinear model ran for $0.1277s$ on average (min: $0.1207s$, max: $0.1627s$) while the average runtime of the linear model is further reduced to $0.0221s$ (min: $0.0201s$, max: $0.0366s$). This corresponds to a speed-up of more than 1000 for the nonlinear model and more than 5000 for the linear model, enabling a fast and accurate system-level model for the charge transfer control algorithm.

5.2 Case Study

In this section, we present the results of a case study, analyzing the cell balancing of an EES using the system-level model of our architecture, controlled by Algorithm 1 in comparison to state-of-the-art approaches.

Setup. To compare the capabilities of the proposed circuit, we considered the charge balancing of an EES of $N = 100$ cells. We randomly initialized the cell voltages according to

$$V^{(i)} \sim \mathcal{N}(3.6, 0.05^2)[V] \tag{5}$$

and calculated the corresponding initial charge vector using $Q = C \cdot V$. Other parameters were:

$$\begin{aligned} R_M &= 1m\Omega & R_L &= 1m\Omega & R_C &= 1m\Omega \\ L &= 100\mu H & C &= 10kF & V_d &= 0.8V \end{aligned} \tag{6}$$

Additionally, we set $i_{\mathrm{peak}} = 5A$ (see Fig. 4) – a balance between speed and energy dissipation in the switches – and assumed a charging efficiency of the cells of $\eta = 0.97$, meaning that 3% of energy is dissipated if a cell is charged.

Balancing strategies. In our case study, we compared four different strategies. *Passive* balancing simply dissipates all excess energy over a small resistor. We assumed a dissipation

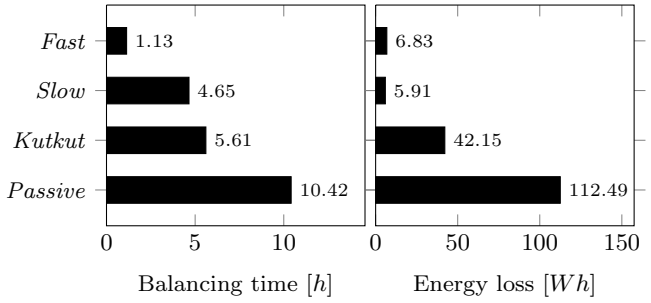

Figure 5: Results of the case study comparing balancing time and energy loss between different approaches.

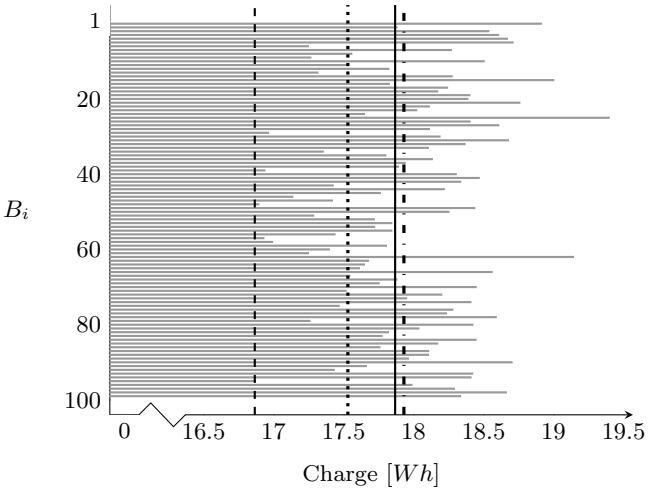

Figure 6: Illustration of the initial charge distribution and the lowest final charge of the case study with 100 cells. Most charge is preserved with the *Slow* strategy (- . -) followed by *Fast* (——) still clearly outperforming *Kutkut* (.....) while the *Passive* (- - -) balancing reduces the charge to the level of the lowest cell.

rate of $10.8W$ as it would be achieved by nine MAX11068 [14] battery management micro-controllers, each handling up to twelve cells. *Kutkut* is a fully concurrent but neighbor-only balancing approach which is carried out on the circuit from [8]. Since [8] only proposes the architecture but no control algorithm for charge transfer, we assume a strategy corresponding to Algorithm 1 with $K = N$ and $r = 1$ that can be simulated using our analytical modeling approach by taking the lower MOSFET count and the diode in the current path of this circuit into account as denoted in Table 3. *Slow* and *Fast* are strategies for our proposed architecture, fully employing its long-range charge transfer capabilities. *Slow* (Algorithm 1 with $K = 1, r = N$) is a non-concurrent approach and therefore only does the energy-optimal transfers. *Fast* (Algorithm 1 with $K = N, r = N$) is fully concurrent and therefore compromises on energy efficiency to reduce balancing time.

Results. Fig. 6 shows the initial distribution of the randomly initialized cell charge. The four vertical lines indicate the minimal charge levels in the pack after cell balancing of each respective approach is finished. The passive cell balancing corresponds to the lowest initial charge of a cell to which all other cells are discharged for equalization. The *Kutkut* strategy is significantly better than passive balancing, but is still clearly outperformed by the *Fast* strategy, using our proposed architecture. Moreover, the *Slow* strategy using our proposed architecture has the lowest energy loss.

A comparison of the various strategies performed with respect to balancing time and dissipated energy is given in Fig. 5. As expected, the *Passive* approach is both the slowest and dissipates by far the most energy. Among the remaining strategies, *Fast* is both 80% faster than *Kutkut* and dissipates 85% less energy. *Slow* further reduces the energy loss by another 15%, but needs four times as long – which is still almost 20% faster than *Kutkut*.

The results show that our proposed architecture controlled by Algorithm 1 is by far outperforming previous approaches. They also give evidence that Algorithm 1 can be adapted by parameter K with respect to the achieved balancing time and energy loss where *Fast* with $K = N$ has fastest equalization speed and *Slow* with $K = 1$ provides the best energy conservation. A supplemental case study is presented in Section S3.

6 Concluding Remarks

This paper introduces and thoroughly analyzes a novel efficient architecture and control for active cell balancing of EES. In contrast to state-of-the-art approaches, the underlying proposed circuit allows to transfer charges between non-adjacent cells in a concurrent fashion. An analytical nonlinear model has been developed for the circuit and further approximated to a linear model, enabling fast and accurate simulations of a complete charge equalization process of an EES at system-level. A speed-up of three orders of magnitude over SPICE-level analysis has been achieved. Finally, a detailed case study shows that our approach with the proposed charge transfer control algorithm significantly outperforms existing approaches in terms of energy efficiency and balancing time.

7 References

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APPENDIX

S1 Switching Scheme

In the following, the switching rules for the proposed balancing architecture are proposed. The switching rules are defined as follows:

$$x_{M_s^i}(\mathcal{P}) = \begin{cases} 1 & \text{if } \exists(\sigma,\delta) \in \mathcal{P} : \sigma = i \vee \delta = i \\ 0 & \text{otherwise} \end{cases} \tag{7}$$

$$x_{M_p^i}(\mathcal{P}) = \begin{cases} 1 & \text{if } \exists(\sigma,\delta) \in \mathcal{P} : \\ & \quad i \in [\min(\sigma,\delta)+1, \max(\sigma,\delta)-1] \\ 0 & \text{otherwise} \end{cases} \tag{8}$$

$$x_{M_a^i}(\mathcal{P}) = \begin{cases} PWM & \text{if } \exists p \in \mathcal{P} : \sigma = i \wedge \sigma < \delta \\ \overline{PWM} & \text{if } \exists p \in \mathcal{P} : \delta = i \wedge (\sigma > \delta \oplus |\delta - \sigma| \% 2 = 0) \\ 1 & \text{otherwise} \end{cases} \tag{9}$$

$$x_{M_b^i}(\mathcal{P}) = \begin{cases} PWM & \text{if } \exists p \in \mathcal{P} : s = i \wedge \sigma > \delta \\ \overline{PWM} & \text{if } \exists p \in P : \delta = i \wedge (\sigma > \delta \oplus |\delta - \sigma| \% 2 = 1) \\ 1 & \text{otherwise} \end{cases} \tag{10}$$

$$x_{M_e^i}(\mathcal{P}) = \begin{cases} 1 & \text{if } \exists(\sigma,\delta) \in \mathcal{P} : (\sigma < \delta \wedge \sigma = i) \vee \\ & \qquad (\sigma < \delta \wedge \delta = i \wedge |\delta - \delta| \% 2 = 0) \vee \\ & \qquad (\sigma > \delta \wedge \sigma - 1 = i) \vee \\ & \qquad (\sigma > \delta \wedge \delta - 1 = i \wedge |\delta - \sigma| \% 2 = 0) \\ 0 & \text{otherwise} \end{cases} \tag{11}$$

$$x_{M_f^i}(\mathcal{P}) = \begin{cases} 1 & \text{if } \exists(\sigma,\delta) \in \mathcal{P} : (\sigma > \delta \wedge \sigma = i) \vee \\ & \qquad (\sigma < \delta \wedge \delta = i \wedge |\delta - \sigma| \% 2 = 1) \vee \\ & \qquad (\sigma < \delta \wedge \sigma - 1 = i) \vee \\ & \qquad (\sigma > \delta \wedge \delta - 1 = i \wedge |\delta - \sigma| \% 2 = 1) \\ 0 & \text{otherwise} \end{cases} \tag{12}$$

Eq. (7) controls M_s^i and closes it in case the respective cell is a source or destination of charge, otherwise it remains open. Eq. (8) controls M_p^i and closes it when charge is transfered between a preceding and succeeding cell, otherwise it remains open. Eq. (9) and (10), respectively, are used to generate the PWM signals. If charge is transfered forward, M_a^i is used for the PWM signal at the block of the source cell. Correspondingly, for transfer of charge backwards, M_b^i is used for the PWM signal. The $\overline{PWM}$ signal is used for controlling the charging of the destination cell that depends on the direction of charge transfer and the absolute distance of the cells. Eq. (11) and (12), respectively, are used to close the electric circuits and prevent horizontal currents.

S2 Model Derivation

The contribution of this section is the detailed development of an analytical model for the proposed circuit. Starting from a circuit analysis for phases T_{ON} and T_{OFF}, the analytical solution of the resulting second-order nonlinear Ordinary Differential Equation (ODE) system is presented. The relevant distinction between different damping cases is then introduced. Finally, a linearization of the inductor current behavior leads to a simplified linear model.

S2.1 From Circuit to Equation

Numerical circuit simulation can be slow for large-scale systems as discussed in Section 4. Hence it is desirable to obtain analytical, closed-form solutions that describe the system behavior as accurately as possible and at the same time execute orders of magnitude faster than the numerical simulation.

We consider the system configurations during T_{ON} and T_{OFF} separately since the behavior significantly changes after the current routing is altered by the PWM signal. Fig. 7 shows the equivalent circuit for the relevant part of the architecture during T_{ON} when the inductor is being charged.

The structure of the equivalent circuit does not depend upon whether transfer occurs only between neighbors as in [8] or more flexibly as in the proposed architecture. The only difference is the amount of series resistance R_σ that we have to introduce to model the inductor series resistance R_L, the cell series resistance R_C, and the ON-resistance of the MOSFETs R_M. The contributions to R_σ are summarized in Table 3.

Circuit behavior during $\mathbf{T_{ON}}$. Applying KIRCHHOFF's Voltage Law to the circuit in Fig. 7 results in

$$L \cdot \frac{\mathrm{d}}{\mathrm{d}t} i + R \cdot i + \frac{1}{C} \int_0^{T_{\text{ON}}} i(\tau)\ \mathrm{d}\tau - V_1 = 0 \tag{13}$$

with $R = R_\sigma$. Differentiating with respect to t, we obtain the following second-order ODE:

$$L \cdot \frac{\mathrm{d}^2}{\mathrm{d}t^2} i + R \cdot \frac{\mathrm{d}}{\mathrm{d}t} i + \frac{1}{C} i = 0 \tag{14}$$

For such a second-order ODE system to have a unique solution, two initial conditions need to be provided. We assume the inductor is fully discharged initially, $i(0) = i_0 := 0$, which gives the first condition. Applying this, we can deduce the second condition from Eq. (13) with

$$L \cdot \frac{\mathrm{d}}{\mathrm{d}t} i(0) + 0 + 0 - V_1 = 0 \tag{15}$$

and therefore

$$\Rightarrow \frac{\mathrm{d}}{\mathrm{d}t} i(0) = \mathrm{d}i_0 := \frac{V_1}{L}. \tag{16}$$

Circuit behavior during $\mathbf{T_{OFF}}$. The equivalent circuit of the architecture segment that is relevant during T_{OFF} is shown in Fig. 8. R_δ summarizes series resistances similarly to R_σ. Its calculation is also detailed in Table 3. Applying KIRCHHOFF's Voltage Law yields

$$L \cdot \frac{\mathrm{d}}{\mathrm{d}t} i + R \cdot i + \int_0^{T_{\text{ON}}} i(\tau)\ \mathrm{d}\tau + V_d + V_2 = 0 \tag{17}$$

with $R = R_\delta$. We can differentiate with respect to t and obtain Eq. (14) again. Concerning the initial values, we can assume the current to start where it ended during T_{ON}, meaning $i(0) = i_0 := i_{\text{peak}}$. With this in mind, transforming Eq. (17) yields the second condition.

$$\begin{aligned} 0 &= L \cdot \frac{\mathrm{d}}{\mathrm{d}t} i(0) + R \cdot i_{\text{peak}} + 0 + V_d + V_2 \\ \Rightarrow \frac{\mathrm{d}}{\mathrm{d}t} i(0) &= \mathrm{d}i_0 := -\frac{V_2 + V_d + R i_{\text{peak}}}{L} \end{aligned} \tag{18}$$

Circ.	Symb.	$\lvert\boldsymbol{\sigma - \delta}\rvert \bmod 2 = 1$	$\lvert\boldsymbol{\sigma - \delta}\rvert \bmod 2 = 0$
K	R_σ	$R_C + R_L + R_M$	-
	R_δ	$R_C + R_L$	-
	V_d	V_d	-
N	R_σ	$R_C + R_L + 3R_M$	$R_C + R_L + 3R_M$
	R_δ	$R_\sigma + (2d-1)R_M$	$R_\sigma + R_L + (2d-1)R_M$
	V_d	0	0

Table 3: Lookup table for the sum of the series resistances and the diode voltage drop V_d. $d = \lvert\boldsymbol{\sigma - \delta}\rvert$ is the distance between source and destination cell. K: Circuit from [8], N: Proposed circuit employing non-overlapping PWM signal.

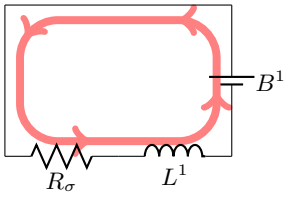

Figure 7: Equivalent circuit of the architecture segment relevant during T_{ON}.

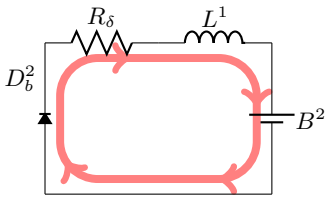

Figure 8: Equivalent circuit of the architecture segment relevant during T_{OFF}.

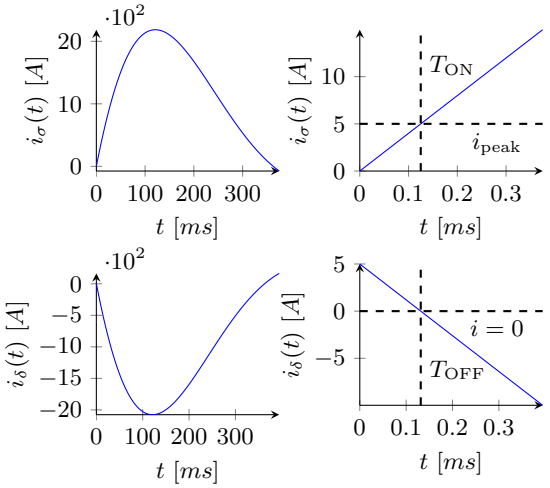

Figure 9: Current plots for the under-damped case; upper row: charging current i_σ; lower row: discharging current i_δ.

S2.2 Ordinary Differential Equation (ODE) Solution

This section presented a solution approach for the ODE in Eq. (14) with initial conditions in Eq. (16) and Eq. (18) for T_{ON} and T_{OFF}, respectively. Combined, they form the following system:

$$L \cdot \frac{\mathrm{d}^2}{\mathrm{d}t^2} i + R \cdot \frac{\mathrm{d}}{\mathrm{d}t} i + \frac{1}{C} i = 0$$
$$i(0) = i_0 \qquad \frac{\mathrm{d}}{\mathrm{d}t} i(0) = \mathrm{d}i_0 \tag{19}$$

The solution process of such a second-order system is detailed in control engineering literature such as [12]. Following these solution processes, we rewrite Eq. (19) to

$$0 = \frac{\mathrm{d}^2}{\mathrm{d}t^2} i + \frac{R}{L} \cdot \frac{\mathrm{d}}{\mathrm{d}t} i + \frac{1}{LC} i =: \frac{\mathrm{d}^2}{\mathrm{d}t^2} i + 2\xi\omega_n \cdot \frac{\mathrm{d}}{\mathrm{d}t} i + \omega_n^2 i. \tag{20}$$

The behavior of the system largely depends upon its natural frequency ω_n and its damping ratio ξ. In case of the proposed circuit, ω_n and ξ are given by the following equations:

$$\omega_n = \frac{1}{\sqrt{LC}} \qquad \xi = \frac{1}{2} \frac{R}{L} \sqrt{LC} \tag{21}$$

The characteristic equation of the ODE whose roots lead to the general solution of the system can be obtained by introducing variable s and modeling Eq. (20) as:

$$s^2 + 2\xi\omega_n \cdot s + \omega_n^2 \tag{22}$$

The roots of the characteristic Eq. (22) of the ODE results in

$$s_{1/2} = -\xi\omega_n \pm \omega_n \sqrt{\xi^2 - 1} \tag{23}$$

and the general time domain solution of ODE system in Eq. (19) is therefore given by:

$$i(t) = \gamma_1 e^{s_1 t} + \gamma_2 e^{s_2 t} \tag{24}$$

Solving for the constants γ_1 and γ_2, using the initial values from Eq. (19) yields the following relation:

$$i(t) = \frac{\mathrm{d}i_0 - i_0 s_2}{s_1 - s_2} e^{s_1 t} - \frac{\mathrm{d}i_0 - i_0 s_1}{s_1 - s_2} e^{s_2 t} \tag{25}$$

Using Eq. (23), this can be further reformulated to:

$$i(t) = e^{-\xi\omega_n t} \cdot \Bigg\{ \frac{\mathrm{d}i_0 - i_0(-\xi\omega_n - \omega_n\sqrt{\xi^2 - 1})}{2\omega_n\sqrt{\xi^2 - 1}} e^{(\omega_n\sqrt{xi^2 - 1})t} - \frac{\mathrm{d}i_0 - i_0(-\xi\omega_n + \omega_n\sqrt{\xi^2 - 1})}{2\omega_n\sqrt{\xi^2 - 1}} e^{-(\omega_n\sqrt{xi^2 - 1})t} \Bigg\} \tag{26}$$

From this point, we need to differentiate between three cases, $\xi < 1$ (*under-damping*), $\xi = 1$ (*critical damping*) and $\xi > 1$ (*over-damping*) because they represent entirely different system behaviors. Under-damping leads to a resonating signal that is slowly damped away. Over-damping on the other hand is not resonating, but creeps very slowly to its equilibrium. Critical damping is an interim situation where the system signal resonates exactly once and is then damped away. This is the fastest way to reach the equilibrium and critical damping is therefore used as a design methodology in certain situations. Since our approach ends the system signals prematurely, all three cases can be handled and do in fact barely differ on the relevant time scale as we will see in the following sections.

S2.3 Under-Damping($\xi < 1$)

If $\xi < 1$, the roots of the characteristic equation are not real, but complex:

$$s_{1/2} = -\xi\omega_n \pm j\omega_n\sqrt{1 - \xi^2} \tag{27}$$

Using this, we can transform Eq. (26):

$$i(t) = e^{-\xi\omega_n t} \cdot \Bigg\{ \frac{\mathrm{d}i_0 - i_0(-\xi\omega_n - j\omega_n\sqrt{1 - \xi^2})}{2j\omega_n\sqrt{1 - \xi^2}} \cdot (\cos(\omega_n\sqrt{xi^2 - 1})t) + j\sin(\omega_n\sqrt{xi^2 - 1}t) - \frac{\mathrm{d}i_0 - i_0(-\xi\omega_n + j\omega_n\sqrt{1 - \xi^2})}{2j\omega_n\sqrt{1 - \xi^2}} \cdot (\cos(\omega_n\sqrt{xi^2 - 1})t) - j\sin(\omega_n\sqrt{xi^2 - 1}t) \Bigg\}$$

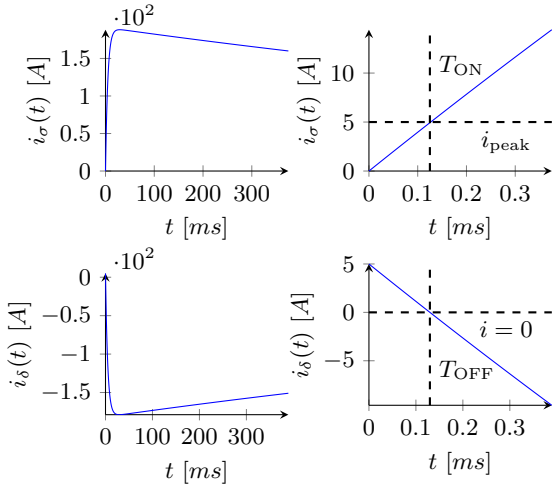

Figure 10: Current plots for the over-damped case; upper row: charging current i_σ; lower row: discharging current i_δ.

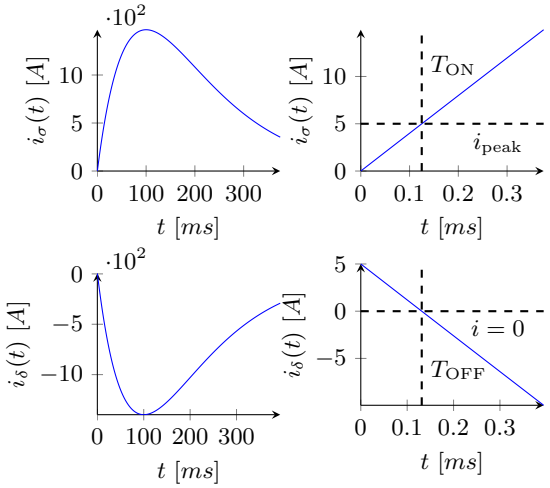

Figure 11: Current plots for the critically damped case; upper row: charging current i_σ; lower row: discharging current i_δ.

$$\begin{aligned} i(t) =& e^{-\xi\omega_n t} \cdot \{ i_0 \cos(\omega_n \sqrt{1-\xi^2} t) \\ &+ \frac{\mathrm{d}i_0 + i_0 \xi \omega_n}{\omega_n \sqrt{1-\xi^2}} \sin(\omega_n \sqrt{1-\xi^2} t) \} \end{aligned} \tag{28}$$

Abstracting $i(t) = e^{-ct}\big(A\cos(at) + B\sin(at)\big)$, we can integrate Eq. (28) to obtain the transferred charge q.

$$\begin{aligned} q(T) =& \frac{-A}{a^2+c^2}\Big[c(e^{-Tc}\cos(Ta) - 1) - ae^{-Tc}\sin(Ta)\Big] \\ &- \frac{B}{a^2+c^2}\Big[a(e^{-Tc}\cos(Ta) - 1) + ce^{-Tc}\sin(Ta)\Big] \end{aligned} \tag{29}$$

The remaining task is to calculate T. For the charging phase, we can use $T = T_{\text{ON}}$, but for $T = T_{\text{OFF}}$, we need to calculate when the inductor is actually empty, i.e., we solve the following:

$$\begin{aligned} & 0 = A\cos(at) + B\sin(at) \\ \Leftrightarrow & -\frac{A}{B} = \frac{\sin(at)}{\cos(at)} \\ \Leftrightarrow & at = \arctan(-\frac{A}{B}) \end{aligned} \tag{30}$$

Since there is no closed-form for T_{ON} in the nonlinear model, a short binary search using the nonlinear model can be used to improve the accuracy of the linear estimation. Fig. 9 gives an impression on how i_σ and i_δ behave and how small T_{ON}, T_{OFF} are relatively to the time constants of the sine waves.

S2.4 Over-Damping ($\xi > 1$)

If $s_{1/2} \in \mathbb{R}$, we can directly abstract $i(t) = e^{-ct}\left[Ae^{at} - Be^{-at}\right]$ from Eq. (26) and integrate it to obtain:

$$q(T) = \frac{B}{a+c}\Big[e^{-Ta-Tc} - 1\Big] + \frac{A}{a-c}\Big[e^{Ta-Tc} - 1\Big] \tag{31}$$

To calculate T_{OFF}, we need to solve the following:

$$\begin{aligned} & 0 = Ae^{at} - Be^{-at} \\ \Leftrightarrow & \log(e^{at}) = \log(\frac{B}{A}e^{-at}) = \log(\frac{B}{A}) + -at \\ \Leftrightarrow & 2at = \log(\frac{B}{A}) \end{aligned} \tag{32}$$

As illustrated in Fig. 10, it becomes obvious that the damping actually has only little influence during the time frame we are interested in.

S2.5 Critical Damping ($\xi = 1$)

If $\xi = 1$, the characteristic equation has co-located roots and the solution therefore becomes

$$i(t) = (A + Bt)e^{-ct} \tag{33}$$

with $A = i_0$, $B = \mathrm{d}i_0 + \omega_n i_0$, $c = \omega_n$. Fig. 11 shows the corresponding plots. Again, the behavior does not differ much from the other cases as far as very short intervals are concerned. Integrating $i(t)$ yields the transferred charge as in the other cases:

$$q(T) = \frac{B}{c^2}\big(1 - (Tc+1)e^{-Tc}\big) - \frac{A}{c}\big(e^{-Tc} - 1\big) \tag{34}$$

The calculation of T_{OFF} is done with Eq. (33). We have to solve the following:

$$0 = A + Bt \qquad \Rightarrow t = \frac{-A}{B} \tag{35}$$

S2.6 Linear Analysis

We developed a nonlinear model in Section S2.2. It results in many different cases to consider and it might become tedious to implement certain cases. Optimization and control scenarios in particular need the system model to be as simple as possible. If we assume the current to be linear – a reasonable assumption for the small time steps we are treating as seen in Figs. 9, 10 and 11 – we can model i_σ and i_δ as

$$i(t) = i_0 + \mathrm{d}i_0 \cdot t \tag{36}$$

with i_0, $\mathrm{d}i_0$ as in Eq. (16) or Eq. (18) for T_{ON} and T_{OFF}, respectively. In practice, this results in:

$$\begin{aligned} i_\sigma(t) =& \frac{V_1}{L} \cdot t \\ i_\delta(t) =& i_{\text{peak}} - \frac{V_2 + V_d + R_\delta i_{\text{peak}}}{L} \cdot t \end{aligned} \tag{37}$$

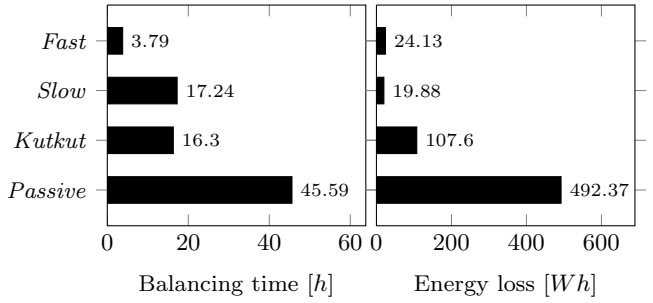

Figure 12: Results of the supplemental case study with a higher variance in charge levels, comparing balancing time and energy loss between different approaches. *Fast* and *Slow* are two proposed approaches for the presented architecture while *Kutkut* and *Passive* constitute state-of-the-art approaches.

From there, we can again integrate to obtain the transferred charge $q(T)$ and obtain the following:

$$\begin{aligned} q_\sigma(T) &= \int_0^T i_\sigma(\tau)\,\mathrm{d}\tau = \int_0^T \frac{V_1}{L}\cdot\tau\,\mathrm{d}\tau \\ &= \frac{V_1}{L}\cdot\frac{T^2}{2} \end{aligned} \tag{38}$$

$$\begin{aligned} q_\delta(T) &= \int_0^T \left[i_{\text{peak}} - \frac{V_2+V_d+R_\delta i_{\text{peak}}}{L}\cdot\tau\right]\mathrm{d}\tau \\ &= i_{\text{peak}}T - \frac{V_2+V_d+R_\delta i_{\text{peak}}}{L}\cdot\frac{T^2}{2} \end{aligned} \tag{39}$$

Again, we need to provide values for T. In the linearized case, we can calculate both T_{ON} and T_{OFF} directly from Eq. (37). We obtain the following:

$$\begin{aligned} T_{\text{ON}} &= i_{\text{peak}}\frac{L}{V_1} \\ T_{\text{OFF}} &= i_{\text{peak}}\frac{L}{V_2+V_d+R_\delta i_{\text{peak}}} \end{aligned} \tag{40}$$

With two system models available that are both suitable for system-level analysis, the user is left with a choice. Both methods are significantly faster than transistor-level simulations and both provide sufficient accuracy as shown in our experimental results in Section 5.1.

S3 Supplemental Case-study with Higher Variance

To validate the results from section 5.2, we performed a supplemental case-study with significantly higher initial distortion of the charge levels. This poses a greater challenge to all balancing methodologies and it can be expected that their individual strengths and weaknesses become even more apparent than in Section 5.2. We initialized the cell voltages according to

$$V^{(i)} \sim \mathcal{N}(3.6, 0.2^2) \tag{41}$$

and left the other parameters from Eq. (6) unchanged. The strategies under consideration are still *Passive* balancing, the *Kutkut* approach, as well as our *Fast* and *Slow* methodology as defined in Section 5.2.

Figs. 12 and 13 give an overview of the performed simulation. As expected with higher initial variance among the cells, the final charge values in Fig. 13 are lower than those from Fig. 6. A similar observation can be made when comparing Fig. 12 to Fig. 5. The balancing time as well as the unrecoverable energy is increased among all the approaches.

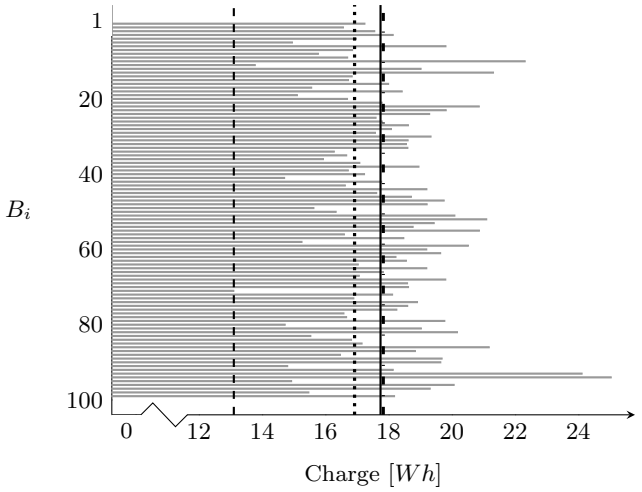

Figure 13: Illustration of the initial and final charge distribution of the supplemental case study with a higher variance in charge levels. Most charge is preserved with the *Slow* strategy (- · -) followed by *Fast* (——) still clearly outperforming *Kutkut* (……) while the *Passive* (- - -) balancing reduces the charge to the level of the lowest cell.

Between the different strategies, we observe that active balancing now performs even better than before with respect to the *Passive* approach. For instance, *Fast* improved from 85% time savings and almost 95% less energy dissipation to 92% and over 95%, respectively. With respect to the other active approaches, *Fast* keeps its lead in balancing speed of over 75%. At the same time, it requires only 25% more energy than *Slow*, making it a very good choice for most scenarios. Concerning balancing speed, *Slow* is now only on par with *Kutkut*. On the other hand, it firmly establishes itself as the first choice with respect to energy dissipation outperforming *Kutkut* by over 80% and *Fast* by 18%.

S4 Nomenclature

	Charge Transfer
σ	Source cell
δ	Destination cell
p	Cell pair (σ, δ), indicating a transfer from σ to δ
$\mathcal{P}$	Set of concurrent transfers $\mathcal{P} = \{p_1, \ldots, p_n\}$
	Circuit Elements
R	Resistance
R_s	Series resistance during T_{ON} (see Table 3)
R_d	Series resistance during T_{OFF} (see Table 3)
L	Inductance
C	Capacitance
B	Battery cell
M	MOSFET or switch for current routing
	Time-Dependent Functions
$i(t)$	Current at time t
$q(T)$	Charge transferred until time T
V	Voltage
	Pulse Width Modulation (PWM)
PWM	PWM controlled signal during T_{ON}
$\overline{PWM}$	PWM controlled signal during T_{OFF}
T_{ON}	Duration of PWM ON interval
T_{OFF}	Duration of PWM OFF interval