

Summary of β Instruction Formats

Operate Class:

31	26	25	21	20	16	15	11	10	0
10xxxx	Rc	Ra	Rb	unused					

Register	Symbol	Usage
R31	R31	Always zero
R30	XP	Exception pointer
R29	SP	Stack pointer
R28	LP	Linkage pointer
R27	BP	Base of frame pointer

OP(Ra,Rb,Rc): $\text{Reg}[Rc] \leftarrow \text{Reg}[Ra] \text{ op } \text{Reg}[Rb]$

Opcodes: **ADD** (plus), **SUB** (minus), **MUL** (multiply), **DIV** (divided by)
AND (bitwise and), **OR** (bitwise or), **XOR** (bitwise exclusive or), **XNOR** (bitwise exclusive nor),
CMPEQ (equal), **CMPLT** (less than), **CMPLE** (less than or equal) [result = 1 if true, 0 if false]
SHL (left shift), **SHR** (right shift w/o sign extension), **SRA** (right shift w/ sign extension)

31	26	25	21	20	16	15	0
11xxxx	Rc	Ra	literal (two's complement)				

OPC(Ra,literal,Rc): $\text{Reg}[Rc] \leftarrow \text{Reg}[Ra] \text{ op } \text{SEXT}(\text{literal})$

Opcodes: **ADDC** (plus), **SUBC** (minus), **MULC** (multiply), **DIVC** (divided by)
ANDC (bitwise and), **ORC** (bitwise or), **XORC** (bitwise exclusive or), **XNORC** (bitwise exclusive nor)
CMPEQC (equal), **CMPLTC** (less than), **CMPLEC** (less than or equal) [result = 1 if true, 0 if false]
SHLC (left shift), **SHRC** (right shift w/o sign extension), **SRAC** (right shift w/ sign extension)

Other:

31	26	25	21	20	16	15	0
01xxxx	Rc	Ra	literal (two's complement)				

LD(Ra,literal,Rc): $\text{Reg}[Rc] \leftarrow \text{Mem}[\text{Reg}[Ra] + \text{SEXT}(\text{literal})]$
ST(Rc,literal,Ra): $\text{Mem}[\text{Reg}[Ra] + \text{SEXT}(\text{literal})] \leftarrow \text{Reg}[Rc]$
JMP(Ra,Rc): $\text{Reg}[Rc] \leftarrow \text{PC} + 4; \text{PC} \leftarrow \text{Reg}[Ra]$
BEQ/BF(Ra,label,Rc): $\text{Reg}[Rc] \leftarrow \text{PC} + 4; \text{if } \text{Reg}[Ra] = 0 \text{ then } \text{PC} \leftarrow \text{PC} + 4 + 4 * \text{SEXT}(\text{literal})$
BNE/BT(Ra,label,Rc): $\text{Reg}[Rc] \leftarrow \text{PC} + 4; \text{if } \text{Reg}[Ra] \neq 0 \text{ then } \text{PC} \leftarrow \text{PC} + 4 + 4 * \text{SEXT}(\text{literal})$
LDR(label,Rc): $\text{Reg}[Rc] \leftarrow \text{Mem}[\text{PC} + 4 + 4 * \text{SEXT}(\text{literal})]$

Opcode Table: (*optional opcodes)

5:3	2:0	000	001	010	011	100	101	110	111
000									
001									
010									
011	LD	ST		JMP	BEQ	BNE		LDR	
100	ADD	SUB	MUL*	DIV*	CMPEQ	CMPLT	CMPLE		
101	AND	OR	XOR	XNOR	SHL	SHR	SRA		
110	ADDC	SUBC	MULC*	DIVC*	CMPEQC	CMPLTC	CMPLEC		
111	ANDC	ORC	XORC	XNORC	SHLC	SHRC	SRAC		