Pre-Lab 4: Designing a Seven-Segment Display Decoder and ALU **Name:**
EGCP 281: Designing with VHDL
Due Date: Tuesday, October 15, 2019 by 11:00 AM
8 points possible

Either submit your completed assignment during class/lab or slide it under the instructor's office door (E-211) prior to the due date

You may discuss this assignment with others, but this assignment must be completed individually. *Please recall that academic dishonesty will not be tolerated. By submitting this assignment, you understand penalties will be assessed if you submit work for credit that is not your own.*

Solve the following problems. For each problem, cite all references used and students consulted.

1. [2 pts] Use a VHDL when or with-select statement to implement a 4-to-1 mux. Assume a 4-bit input bus "I" and a 2-bit select bus "S" are used as the inputs and "Y" is the output signal.

2. [1 pt] Suppose an enable input is added to the 4-to-1 mux from prelab problem 1. The enable input operates in the following manner: if enable = '1', then the mux will operate normally, otherwise, if enable = '0', then the output Y will be '0'. How must you change your VHDL code in order to correctly add and implement this enable signal? Please explain (you do not need to write the new VHDL code).
   Hint: You may want to revisit the lecture slides on std_logic_vectors to see how you can manipulate bits

3. [2 pts] Use a VHDL when or with-select statement to implement a 3-to-8 binary decoder. Assume a 3-bit bus “I” is used as the input and an 8-bit bus “Y” is used as the output.

4. [1 pt] Suppose an enable input is added to the 3-to-8 decoder from prelab problem 3. The enable input operates in the following manner: if enable = ‘1’, then the decoder will operate normally, otherwise, if enable = ‘0’, then all outputs will be ‘0’. How must you change your VHDL code in order to correctly add and implement this enable signal? Please explain (you do not need to write the new VHDL code).
Hint: You may want to revisit the lecture slides on std_logic_vectors to see how you can manipulate bits

5. [2 pts] Construct a truth table for the seven-segment display decoder that you will create in task 1 of this lab. This seven-segment display will display **hexadecimal digits**: the numerals 0-9 as well as the letters A, b, C, d, E, and F. Note that the LED segment patterns for the numerals 0-9 are shown in *Digilent Real Digital Module 6*. And remember, each LED segment is **active low** (requires a logic 0 to illuminate). I have started the truth table for you:

Digit	**N(3)**	**N(2)**	**N(1)**	**N(0)**	**A**	**B**	**C**	**D**	**E**	**F**	**G**
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2											
3											
4											
5											
6											
7											
8											
9											
A											
b											
C											
d											
E											
F	1	1	1	1	0	1	1	1	0	0	0

6. List the references you used for this assignment (e.g. sources/websites used or students with whom you discussed this assignment)