



MEC4126F: Integrated Embedded Systems

Prac 7
08 May 2025

Total marks: 51

Instructions to students

1. This template file contains space for the answers to the written questions of Prac 7.
2. Ensure that you copy-paste your answers inside the space allocated for each question.
3. Provide your numerical answers to **TWO (2)** significant decimal points, unless stated otherwise.

PeopleSoft ID: 1906643

Question 1

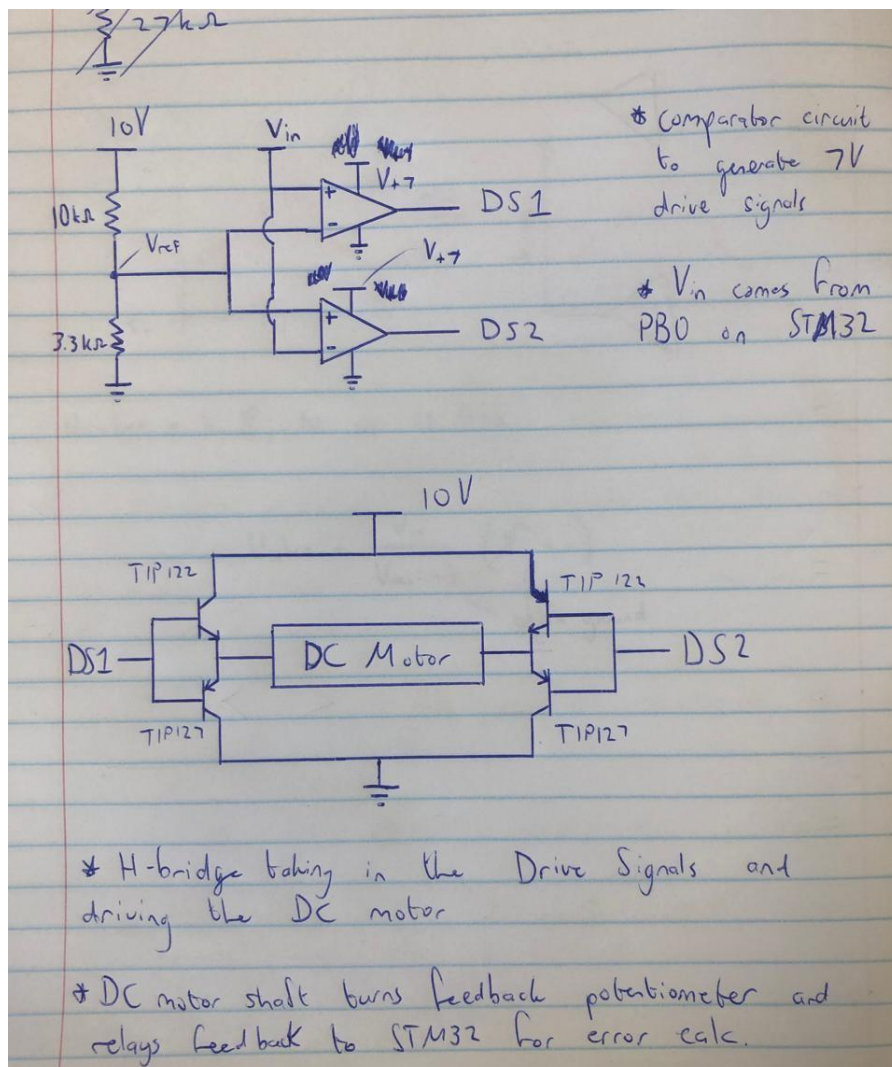
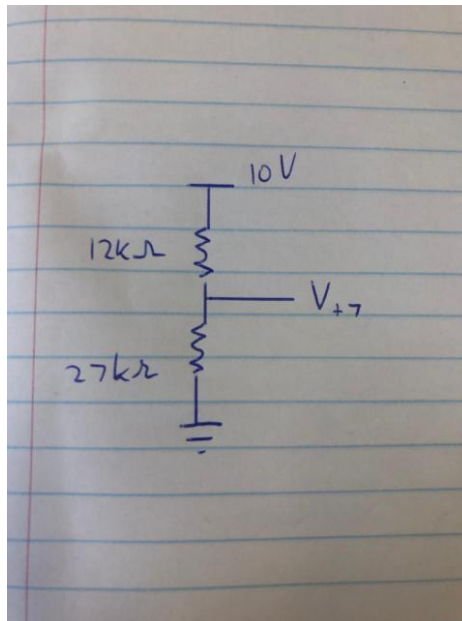
By demonstrating and submitting this practical I agree that:

- I know that plagiarism is a serious form of academic dishonesty.
- I have read the document about avoiding plagiarism, am familiar with its contents and have avoided all forms of plagiarism mentioned there.
- Where I have used the words of others, I have indicated this by the use of quotation marks.
- I have referenced all quotations and other ideas borrowed from others.
- I have not and shall not allow others to plagiarise my work.
- I have not used an AI language model to generate the code or answers submitted here.

Name: Luke Bruchhausen

Signature: Luke Michael Bruchhausen

Question 1



Question 2 (3 marks)

Question 2

$$V_{ref} = \frac{10}{13300} (3300) = 2.481 \text{ V}$$

V_{in}	DS1	DS2
$> V_{ref}$	8.52	0.8
$< V_{ref}$	0.8	8.52

The rails had to be set to 10V instead of using the 7V output of the voltage divider due to the circuit not working as expected when including the divider.

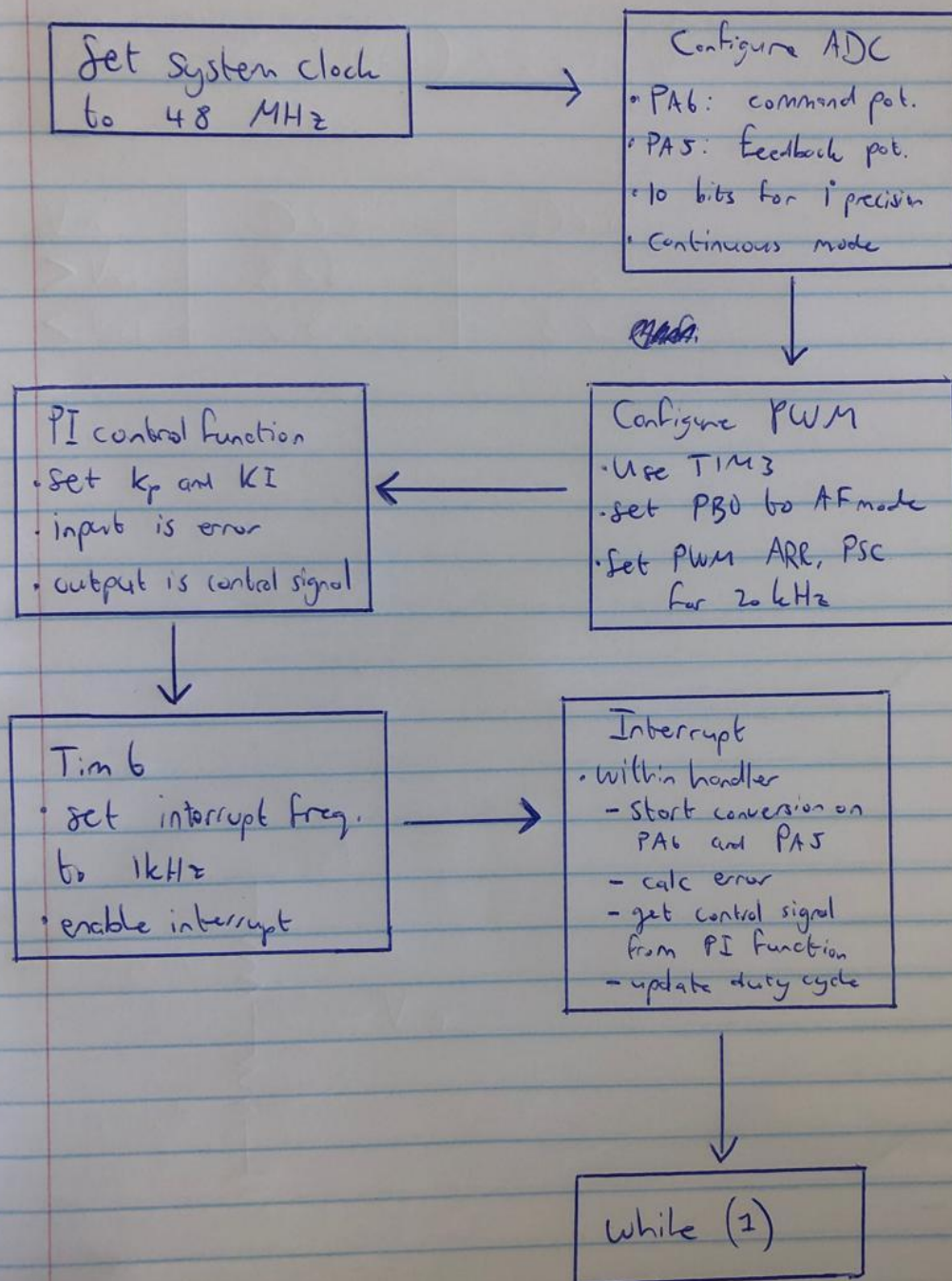
Question 3 (3 marks)

Question 3

DS1	DS2	V_{load}
1	0	4.68
0	1	-4.66

Question 4 (14 marks)

Question 4



Question 5 (6 marks)

Increasing the proportional gain of the system raises the overall loop gain. This improves the response speed and decreases steady state error. It can lead to increased overshoot and decrease stability. It causes the system to respond more strongly to error, making it faster but less damped. Too high a proportional gain will lead to unwanted oscillations.

The integral term accumulates past error and drives the steady-state error to zero. Increasing the term eliminates offset but this integral action is slow and leads to phase lag. It also speeds up the elimination of the offset error but if increased too much, it will lead to overshoot.

In a discrete PI controller, the sampling interval effectively adds a delay of up to one sample period. A smaller sampling interval improves performance while a larger sampling interval slows the control response and introduces phase lag.

Question 6 (10 marks)

Question 6

- with a slew rate of roughly $0.5 \text{ V}/\mu\text{s}$

$$7\text{V}: t = \frac{7}{0.5} = 14 \mu\text{s}$$
$$T_{\text{pwm}} > \frac{14 \mu\text{s}}{0.01} = 1.4 \text{ ms}$$
$$f_{\text{pwm}} \leq \frac{1}{1.4 \times 10^{-3}} = 714.3 \text{ Hz}$$

- the maximum freq. is 714 Hz

$$T = \frac{(PSC+1)(ARR+1)}{48 \times 10^6}$$

let $PSC = 80$, $ARR = 830$

