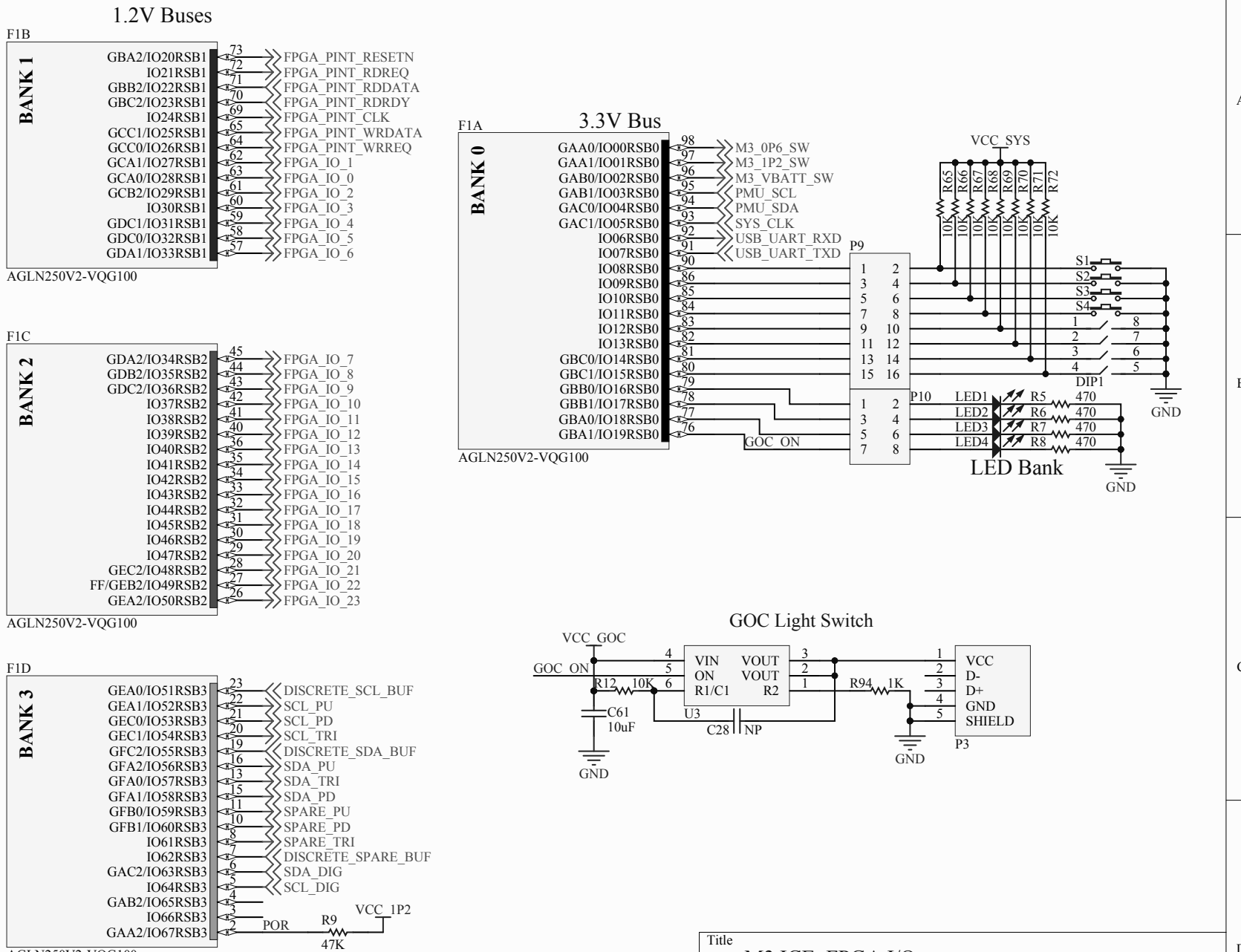
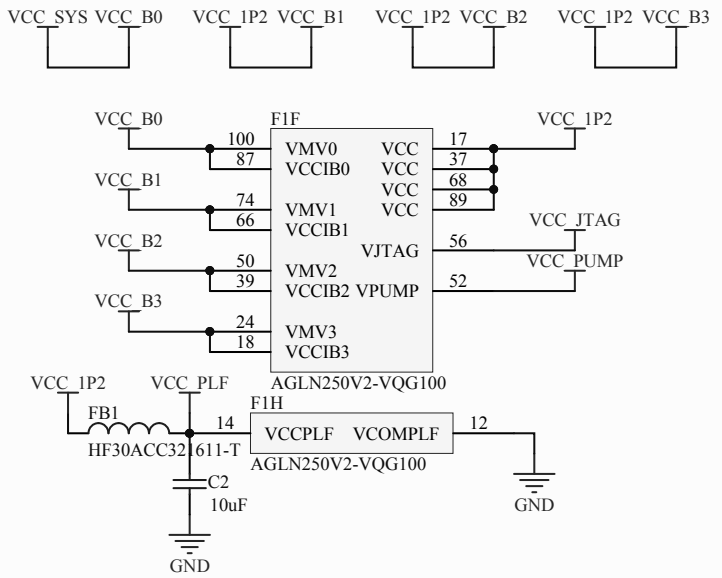
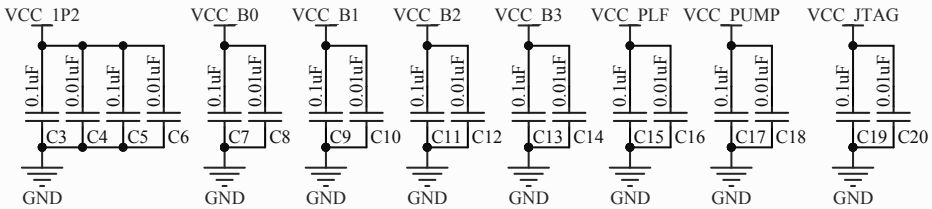


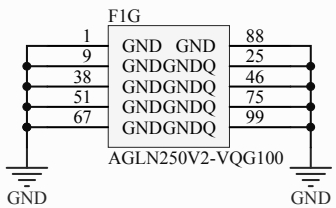
Title	M3 ICE: FPGA I/O		
Size	Number		Revision
A			
Date:	10/7/2013	Sheet of	
File:	C:\Users\..\FPGA_IO.SchDoc	Drawn By:	

FPGA Power

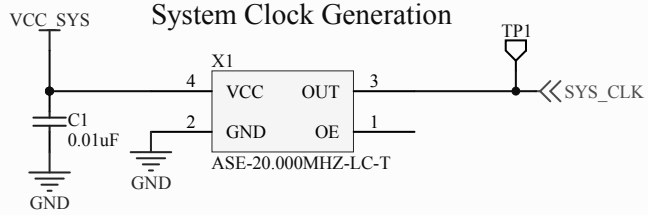


FPGA Decoupling Caps

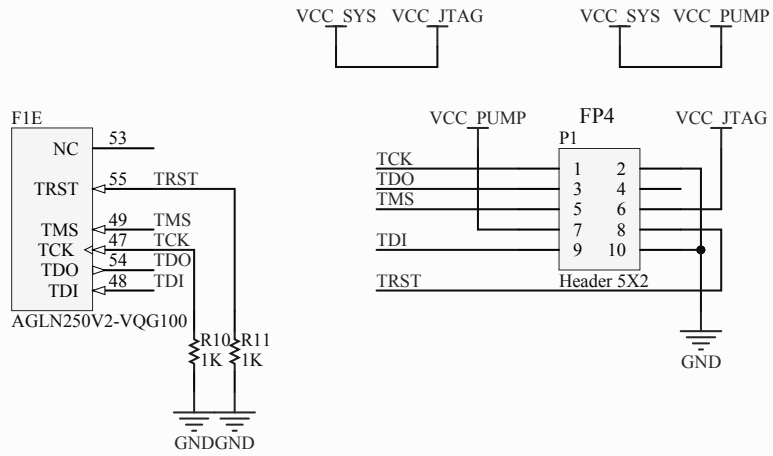




System Clock Generation

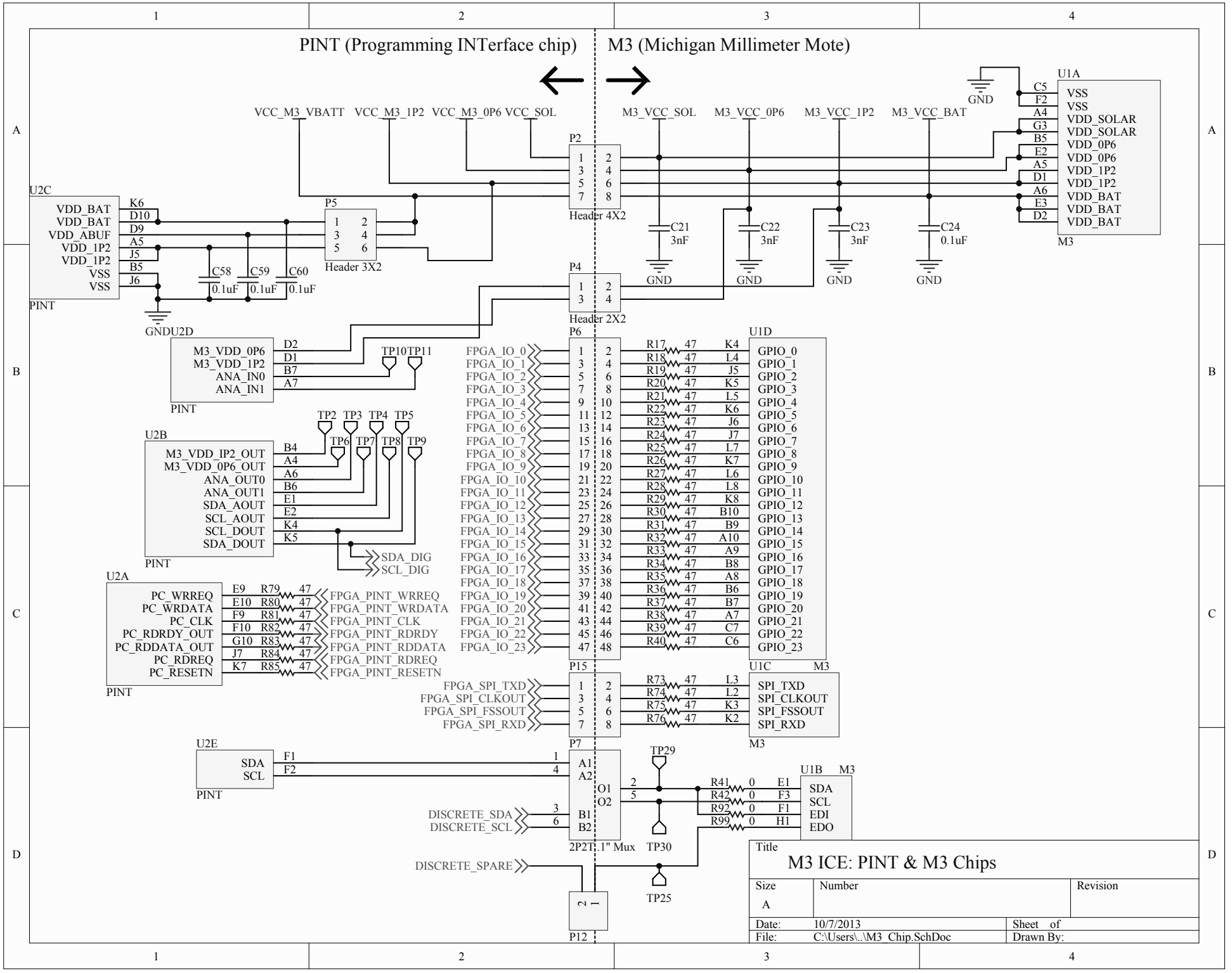


JTAG Connectors

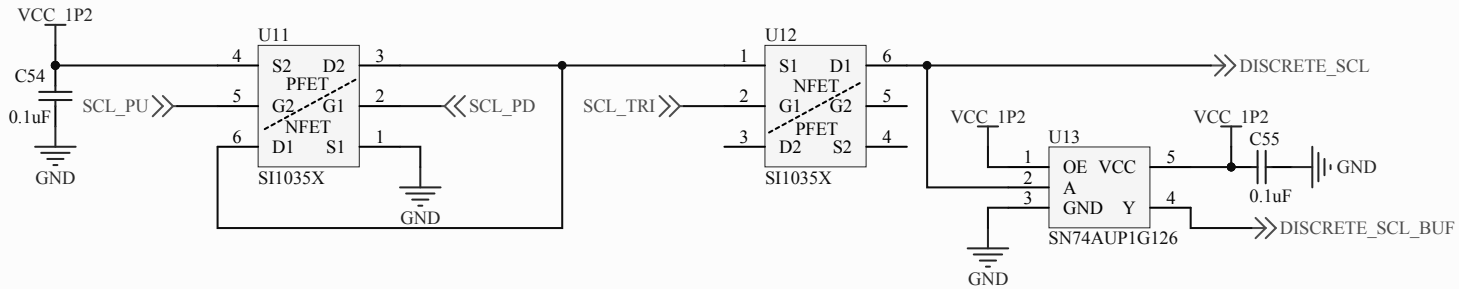


TODO: Is VCC_JTAG supposed to be 3.3V?

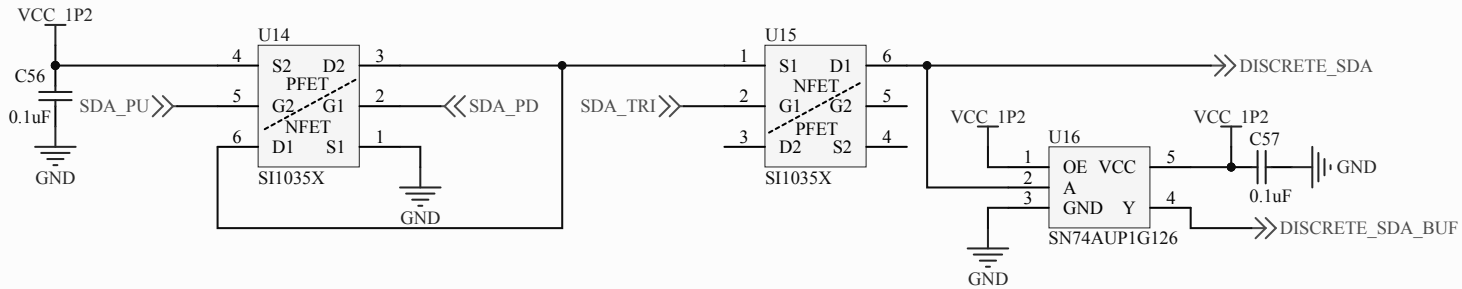
Title: M3 ICE: FPGA Power & Miscellaneous		
Size: A	Number:	Revision:
Date: 10/7/2013		Sheet of
File: C:\Users\..\FPGA_misc.SchDoc		Drawn By:


PINT (Programming INTerface chip)
M3 (Michigan Millimeter Mote)
VCC_M3_VBATT
VCC_M3_1P2
VCC_M3_0P6
VCC_SOL
M3_VCC_SOL
M3_VCC_0P6
M3_VCC_1P2
M3_VCC_BAT
GND
U1A
VSS
VDD_SOLAR
VDD_0P6
VDD_1P2
VDD_BAT
M3
U2C
VDD_BAT
VDD_ABUF
VDD_1P2
VSS
PINT
P2
Header 4X2
P5
Header 3X2
C21
3nF
C22
3nF
C23
3nF
C24
0.1uF
C58
C59
C60
0.1uF
P4
Header 2X2
U2D
M3_VDD_0P6
M3_VDD_1P2
ANA_IN0
ANA_IN1
TP10
TP11
P6
U1D
FPGA_IO_0
FPGA_IO_1
FPGA_IO_2
FPGA_IO_3
FPGA_IO_4
FPGA_IO_5
FPGA_IO_6
FPGA_IO_7
FPGA_IO_8
FPGA_IO_9
FPGA_IO_10
FPGA_IO_11
FPGA_IO_12
FPGA_IO_13
FPGA_IO_14
FPGA_IO_15
FPGA_IO_16
FPGA_IO_17
FPGA_IO_18
FPGA_IO_19
FPGA_IO_20
FPGA_IO_21
FPGA_IO_22
FPGA_IO_23
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_15
GPIO_16
GPIO_17
GPIO_18
GPIO_19
GPIO_20
GPIO_21
GPIO_22
GPIO_23
U2B
M3_VDD_IP2_OUT
M3_VDD_0P6_OUT
ANA_OUT0
ANA_OUT1
SDA_AOUT
SCL_AOUT
SDA_DOUT
SCL_DOUT
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
SDA_DIG
SCL_DIG
U2A
PC_WRREQ
PC_WRDATA
PC_CLK
PC_RDRDY_OUT
PC_RDDATA_OUT
PC_RDREQ
PC_RESETN
FPGA_PINT_WRREQ
FPGA_PINT_WRDATA
FPGA_PINT_CLK
FPGA_PINT_RDRDY
FPGA_PINT_RDDATA
FPGA_PINT_RDREQ
FPGA_PINT_RESETN
P15
U1C
FPGA_SPI_TXD
FPGA_SPI_CLKOUT
FPGA_SPI_FSSOUT
FPGA_SPI_RXD
SPI_TXD
SPI_CLKOUT
SPI_FSSOUT
SPI_RXD
U2E
SDA
SCL
P7
2P2T, .1" Mux
TP29
TP30
TP25
U1B
EDI
EDO
DISCRETE_SDA
DISCRETE_SCL
DISCRETE_SPARE
P12
Title
M3 ICE: PINT & M3 Chips
Size
A
Number
Revision
Date:
10/7/2013
Sheet of
File:
C:\Users\..\M3_Chip.SchDoc
Drawn By:

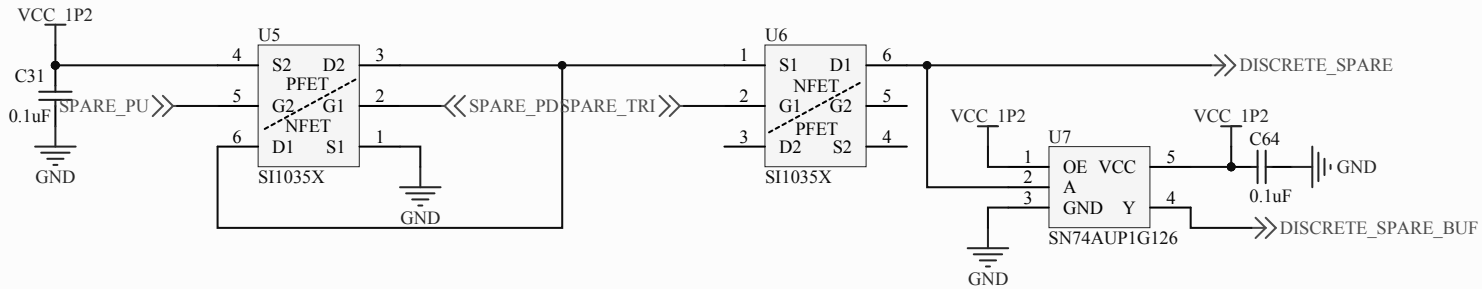
Discrete SCL Interface



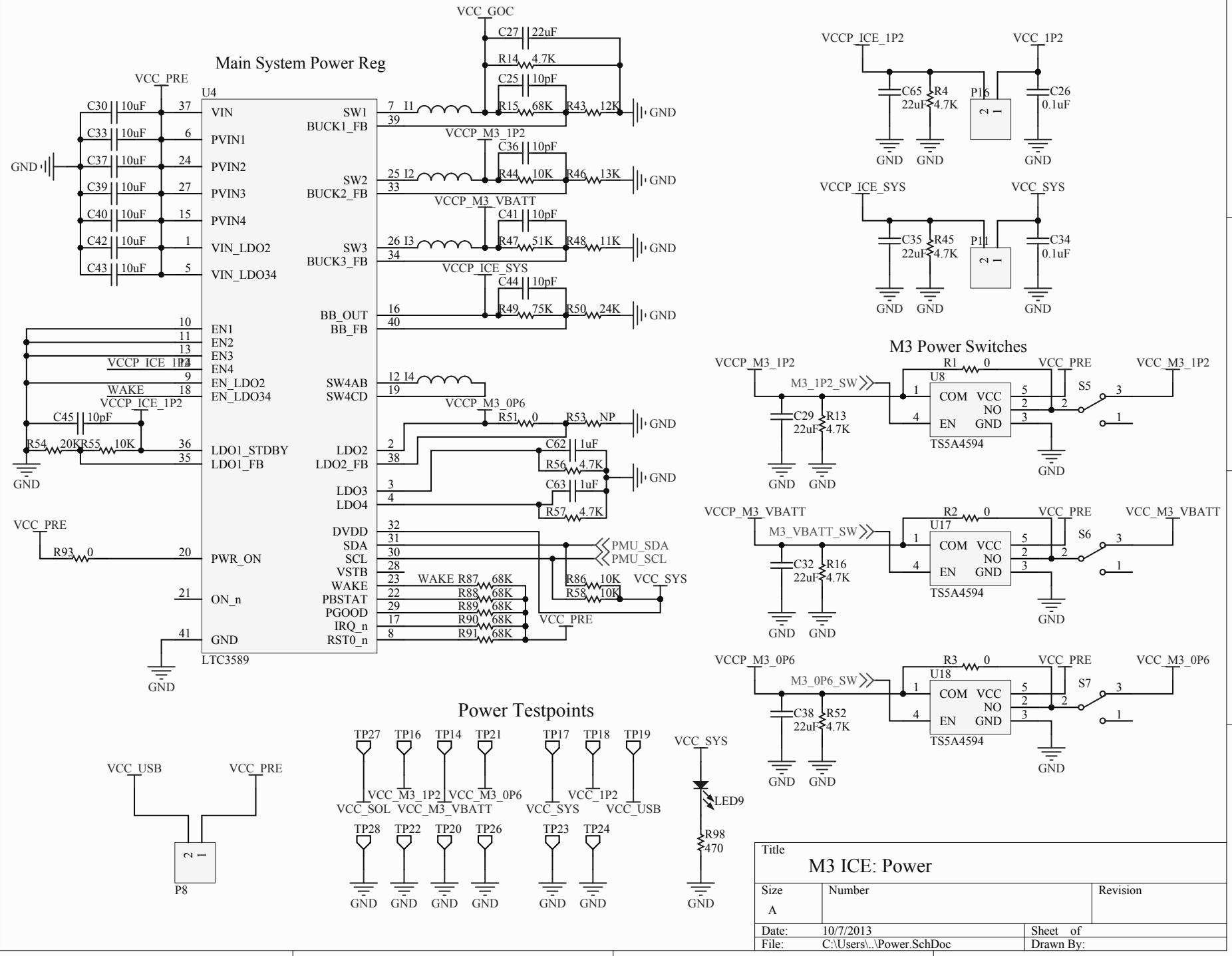
Discrete SDA Interface

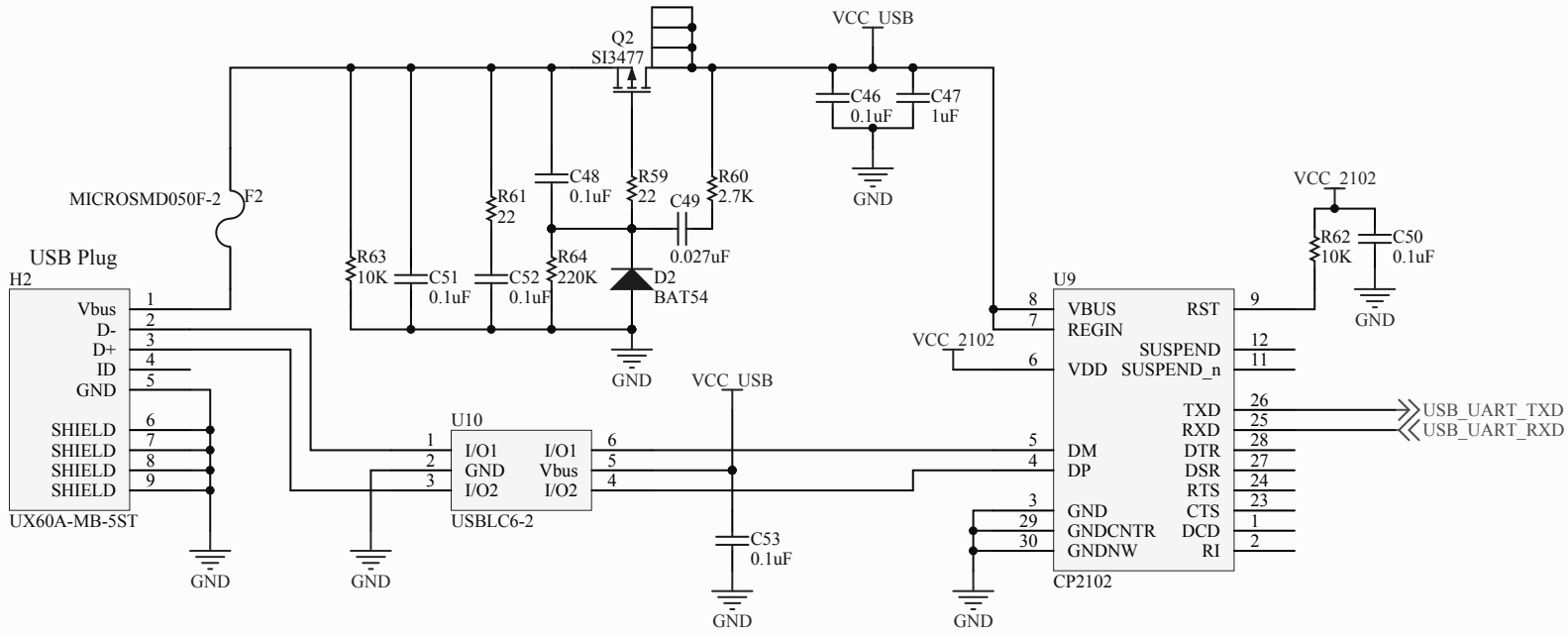


Miscellaneous Interface for New Bus?



Title: M3 ICE: Discrete M3 Interface		
Size: A	Number:	Revision:
Date: 10/7/2013		Sheet of
File: C:\Users\..\M3_Discrete_Interface.SchDoc		Drawn By:


Main System Power Reg
U4
LTC3589
VIN
PVIN1
PVIN2
PVIN3
PVIN4
VIN_LDO2
VIN_LDO34
EN1
EN2
EN3
EN4
EN_LDO2
EN_LDO34
LDO1_STDBY
LDO1_FB
PWR_ON
ON_n
GND
SW1
BUCK1_FB
SW2
BUCK2_FB
SW3
BUCK3_FB
BB_OUT
BB_FB
SW4AB
SW4CD
LDO2
LDO2_FB
LDO3
LDO4
DVDD
SDA
SCL
VSTB
WAKE
PBSTAT
PGOOD
IRQ_n
RST0_n
VCC_GOC
VCC_PRE
VCCP_M3_1P2
VCCP_M3_VBATT
VCCP_ICE_SYS
VCCP_ICE_1P2
WAKE
PMU_SDA
PMU_SCL
VCC_SYS
C27 22uF
R14 4.7K
C25 10pF
R15 68K
R43 12K
C36 10pF
R44 10K
R46 13K
C41 10pF
R47 51K
R48 11K
C44 10pF
R49 75K
R50 24K
C30 10uF
C33 10uF
C37 10uF
C39 10uF
C40 10uF
C42 10uF
C43 10uF
C45 10pF
R54 20K
R55 10K
R93 0
R51 0
R53 NP
C62 1uF
R56 4.7K
C63 1uF
R57 4.7K
R87 68K
R88 68K
R89 68K
R90 68K
R91 68K
R86 10K
R58 10K
VCCP_ICE_1P2
VCC_1P2
C65 22uF
R4 4.7K
P16
C26 0.1uF
VCCP_ICE_SYS
VCC_SYS
C35 22uF
R45 4.7K
P11
C34 0.1uF
M3 Power Switches
VCCP_M3_1P2
M3_1P2_SW
R1 0
U8
C29 22uF
R13 4.7K
TS5A4594
S5
VCC_M3_1P2
VCCP_M3_VBATT
M3_VBATT_SW
R2 0
U17
C32 22uF
R16 4.7K
S6
VCC_M3_VBATT
VCCP_M3_0P6
M3_0P6_SW
R3 0
U18
C38 22uF
R52 4.7K
S7
VCC_M3_0P6
COM
VCC
NO
EN
GND
Power Testpoints
TP27
TP16
TP14
TP21
TP17
TP18
TP19
TP28
TP22
TP20
TP26
TP23
TP24
VCC_M3_1P2
VCC_M3_0P6
VCC_SOL
VCC_M3_VBATT
VCC_1P2
VCC_USB
VCC_SYS
LED9
R98 470
VCC_USB
VCC_PRE
P8
Title
M3 ICE: Power
Size
A
Number
Revision
Date: 10/7/2013
Sheet of
File: C:\Users\..\Power.SchDoc
Drawn By:



Title		
M3 ICE: USB-to-UART Bridge		
Size: A	Number:	Revision:
Date: 10/7/2013		Sheet of
File: C:\Users\..\USB_to_UART.SchDoc		Drawn By: