Monday, Oct 5, 2020: 2 hours
Writing design document and figuring out processor specifics: stack-based, addressing, registers

Tuesday, Oct 6, 2020: 2 hours
Writing sample programs in assembly
Converting said assembly to machine code

M2 task assignment: 1st meeting: break instructions into small steps and move data from one register to another, determine single-cycle or multi-cycle
Luke & Austin: RTL Description of each instruction
Jinhao & Yiju: A list of generic components specifications needed for RTL

2nd meeting: debug and test the processor through Xilinx ISE and fix existed problems

Wednesday, Oct 14, 2020: 1.5 hours
Reviewing Luke's RTL descriptions
Creating Executive Summary

3rd meeting: Create design diagram
Begin Xilinx work
Begin Xilinx testing