Austin Swatek: 232-2v Project Work Log

Milestone 1

Monday, Oct 5, 2020: 2 hours
Writing design document and figuring out processor specifics: stack-based, addressing, registers

Tuesday, Oct 6, 2020: 2 hours
Writing sample programs in assembly
Converting said assembly to machine code

M2 task assignment:
1st meeting: break instructions into small steps and move data from one register to another, determine single-cycle or multi-cycle
Luke & Austin: RTL Description of each instruction
Jinhao & Yiju: A list of generic components specifications needed for RTL

Milestone 2

2nd meeting: debug and test the processor through Xilinx ISE and fix existed problems

Wednesday, Oct 14, 2020: 1.5 hours
Reviewing Luke's RTL descriptions
Creating Executive Summary

M3 task assignment: Create design diagram
Begin Xilinx work
Begin Xilinx testing

Milestone 3

Sunday, Oct 18, 2020: 2.5 hours
Verifying RTL
Created initial datapath design

Tuesday, Oct 20, 2020: 1.5 hours
Created ALU with unique operations

Created ALU testing program

Wednesday, Oct 21, 2020: 2 hours
Came up with integration plan
Refine datapath, unit specification

M4 task assignment:
Things for Milestone 4

- Continue implementing necessary components and adding unit tests
  - Jinhao - sign-extender
  - Austin - adder
  - Jinhao - left-shifter
  - Luke - register
  - Someone - memory blocks
- Start on integration testing plans
  - Group Meetings (might split out individual work later)
- Implement Control
  - Luke

Milestone 4

Sunday, Oct 25, 2020: 2 hours with team
Integration of the stack register and ALU. This makes it possible to push/pop to/from the stack. Testing of integration and refining the integration based on the results of tests was done to make sure it worked properly, and will continue to work properly as other components are integrated.

Monday, Oct 26, 2020: 1.5 hours
Began working on integrating the PC and updating the PC. Determining inputs and outputs for each component to integrate. Did not finish Verilog integration. Did not create tests.

Tuesday, Oct 27, 2020: 1.5 hours with team
Started anew with integration of PC and PC updating. Decided to use Spartan 3E's integrated FD16RE: 16-bit data register during integration. Simple testing was done to check PC changes correctly.

Milestone 5

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