Jinhao Sheng WORK LOG

MILESTONE 1 WORK

Monday, October 5, 2020 Met

with team[120 min]

We decided to build a stack based processor. We created a Google doc to begin our design document. We then decide to have two stacks and no registers and implement two types of instructions.

Tuesday, October 6, 2020

Design procedure call convention[30 min]

Met with team[120 min]

We drafted out example assembly programs like relprime and other fractions. We also wrote the machine code for each example programs.

M2 task assignment:

- 1st meeting: break instructions into small steps and move data from one register to another, determine single-cycle or multi-cycle
- Luke & Austin: RTL Description of each instruction\
  Jinhao & Yiju : A list of generic components specifications needed for RTL
- 2nd meeting: debug and test the processor through Xilinx ISE and fix existed problems

MILESTONE 2 WORK

Wednesday, October 14, 2020

Read through Design Document

MILESTONE 3 WORK

Saturday, October 17, 2020

Design Datapath for O-type Instruction[30 min]

Sunday, October 18, 2020

Met with team[120 min]

We verified our RTL by iterate each instruction on a whiteboard. We then drafted out our initial design of our datapath.

Monday, October 18, 2020

Met with team[60 min]

We designed our stack register, and also finished design our datapath.

Drawing datapath on draw.io[30min]

Tuesday, October 20, 2020

Write out unit testing for multiplexer[60min]

Wednesday, October 21, 2020

Met with team[90min]

Refine datapath, Unit Specification, and write out integration plan

Things for Milestone 4

- Continue implementing necessary components and adding unit tests
    - Jinhao - sign-extender
    - Austin - adder
    - Jinhao - left-shifter
    - Luke - register
    - Someone - memory blocks
- Start on integration testing plans
    - Group Meetings (might split out individual work later)
- Implement Control
    - Luke