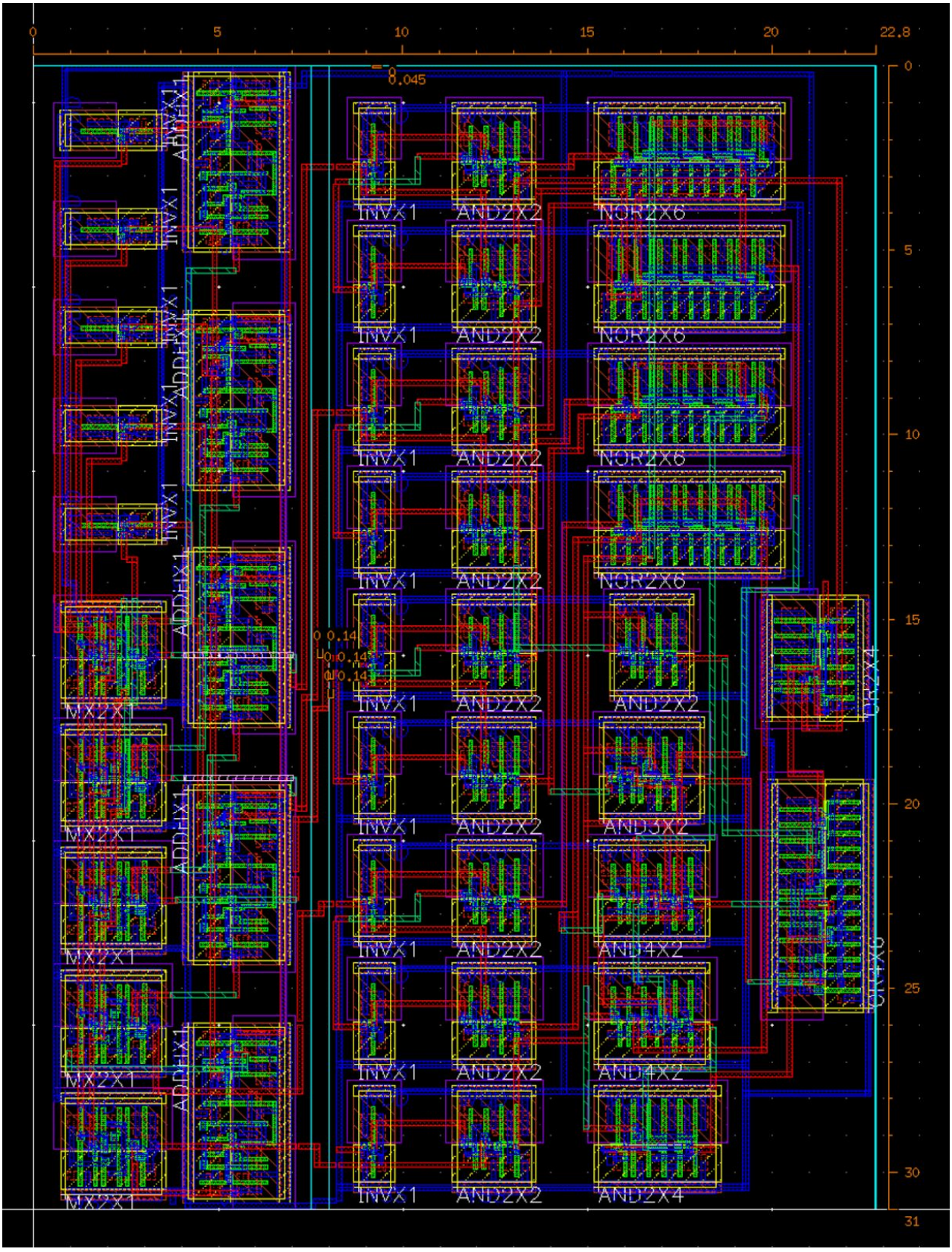
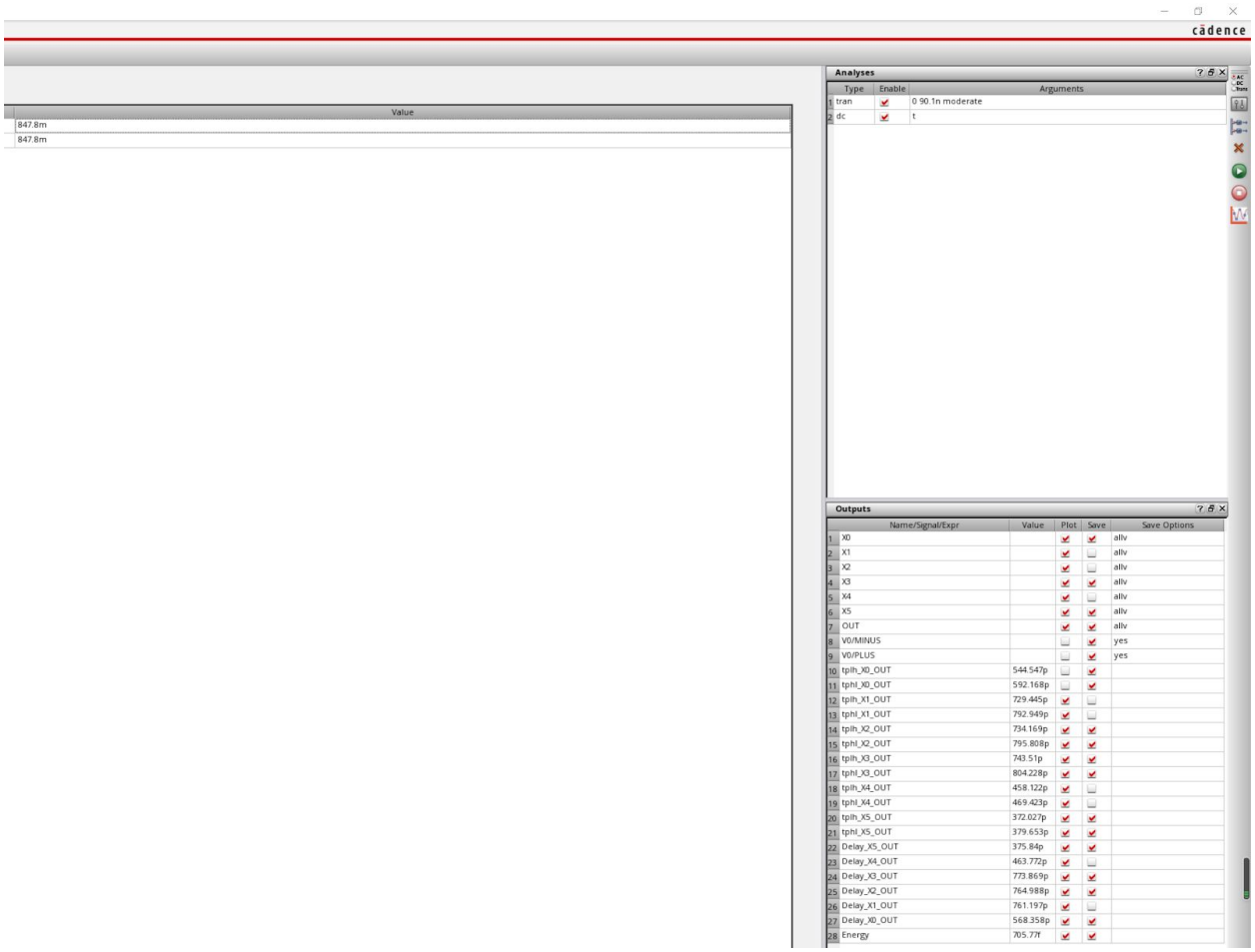
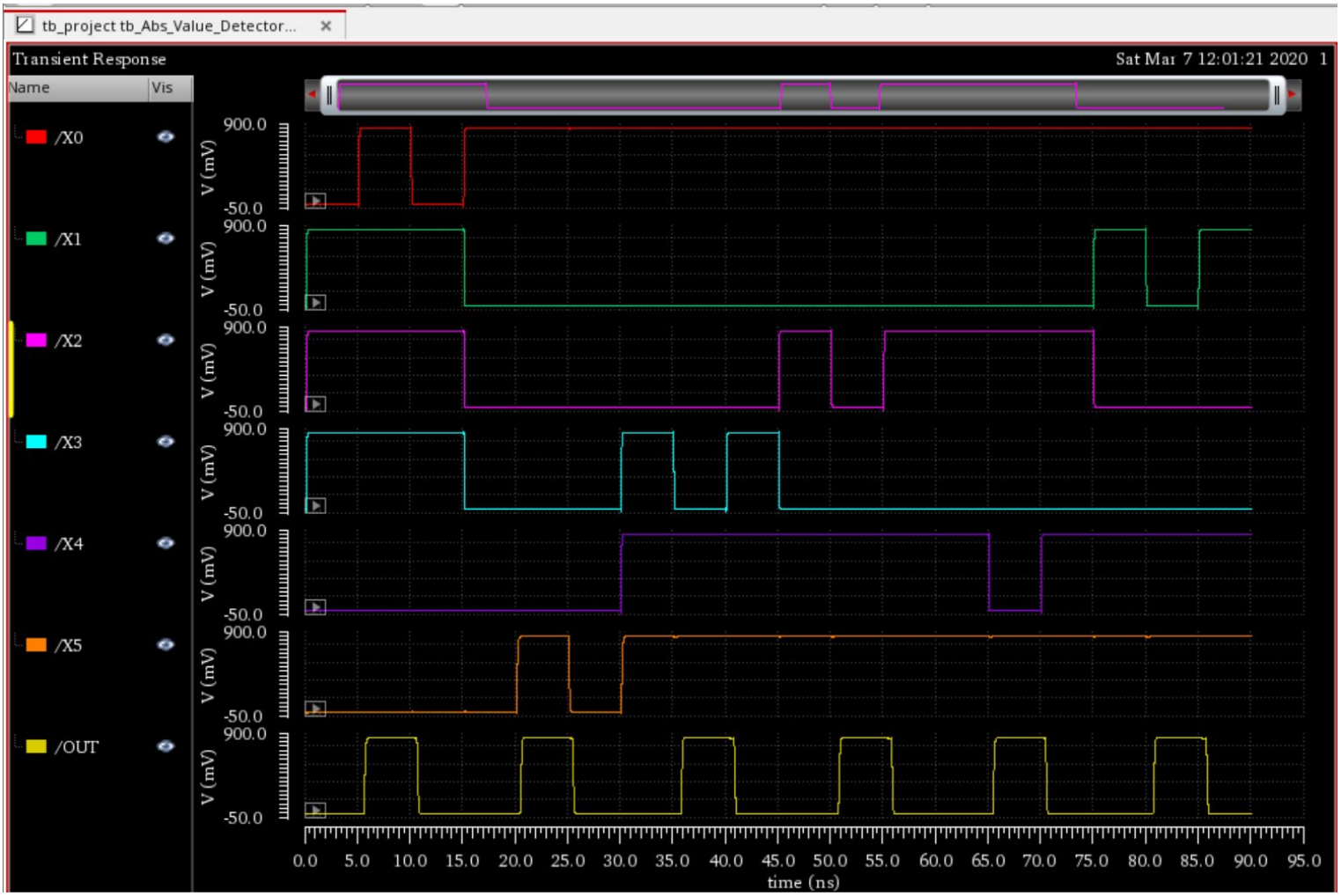
Layout Area

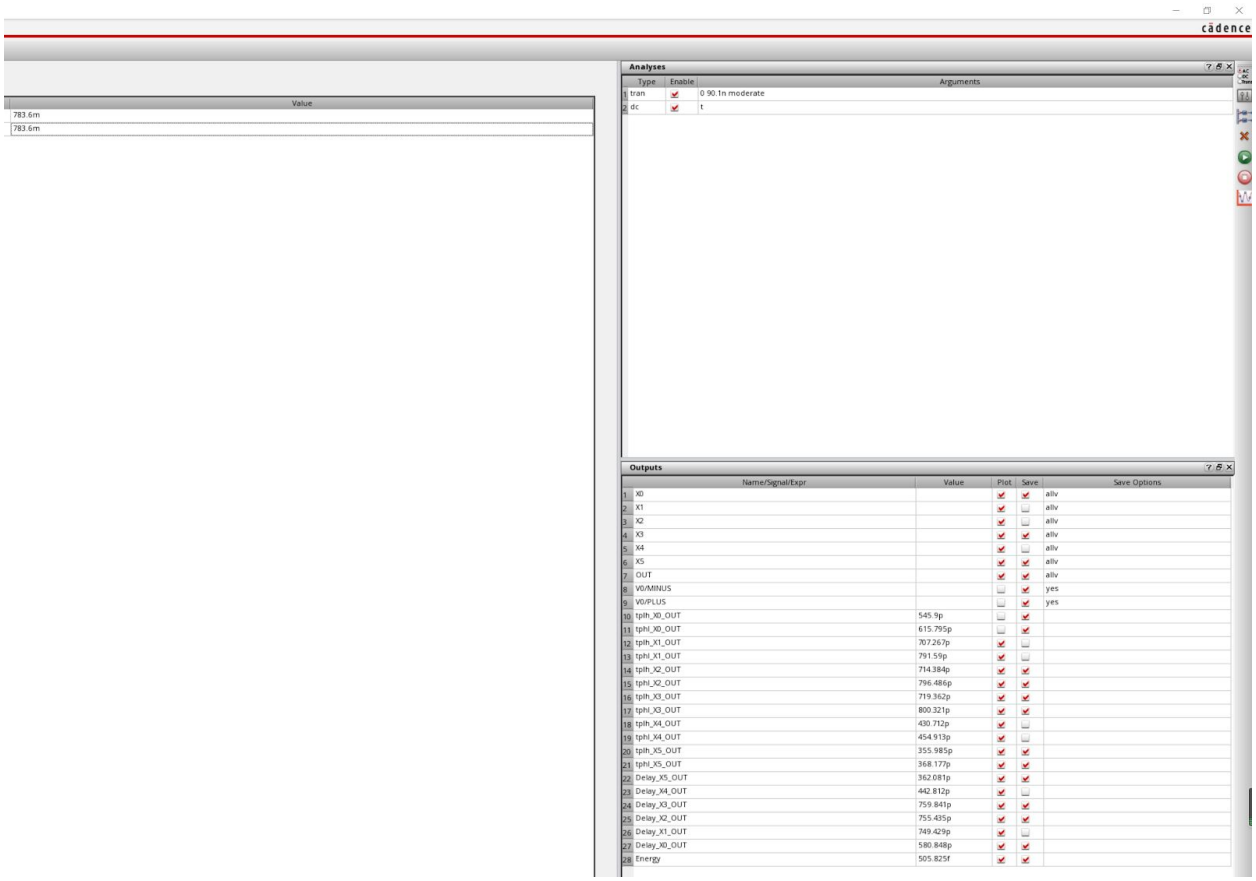

0
5
10
15
20
22.8
8.045
ADDHX1
INVX1
AND2X2
NOR2X6
AND3X2
AND4X2
AND2X4
OR4X6
MX2X1
0 0.14
0.14
0.14
0
5
10
15
20
25
30
31

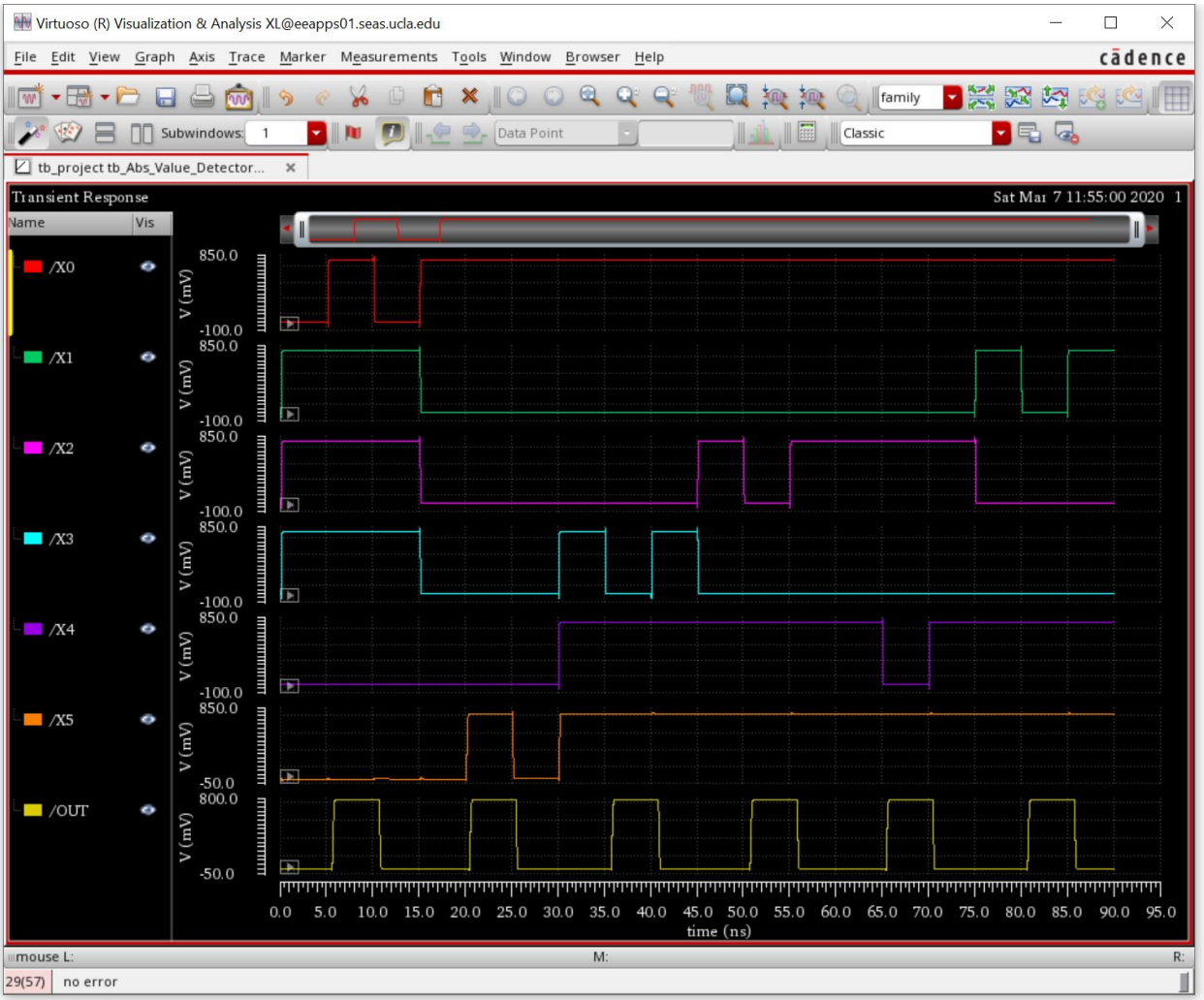
Run with post-layout simulation



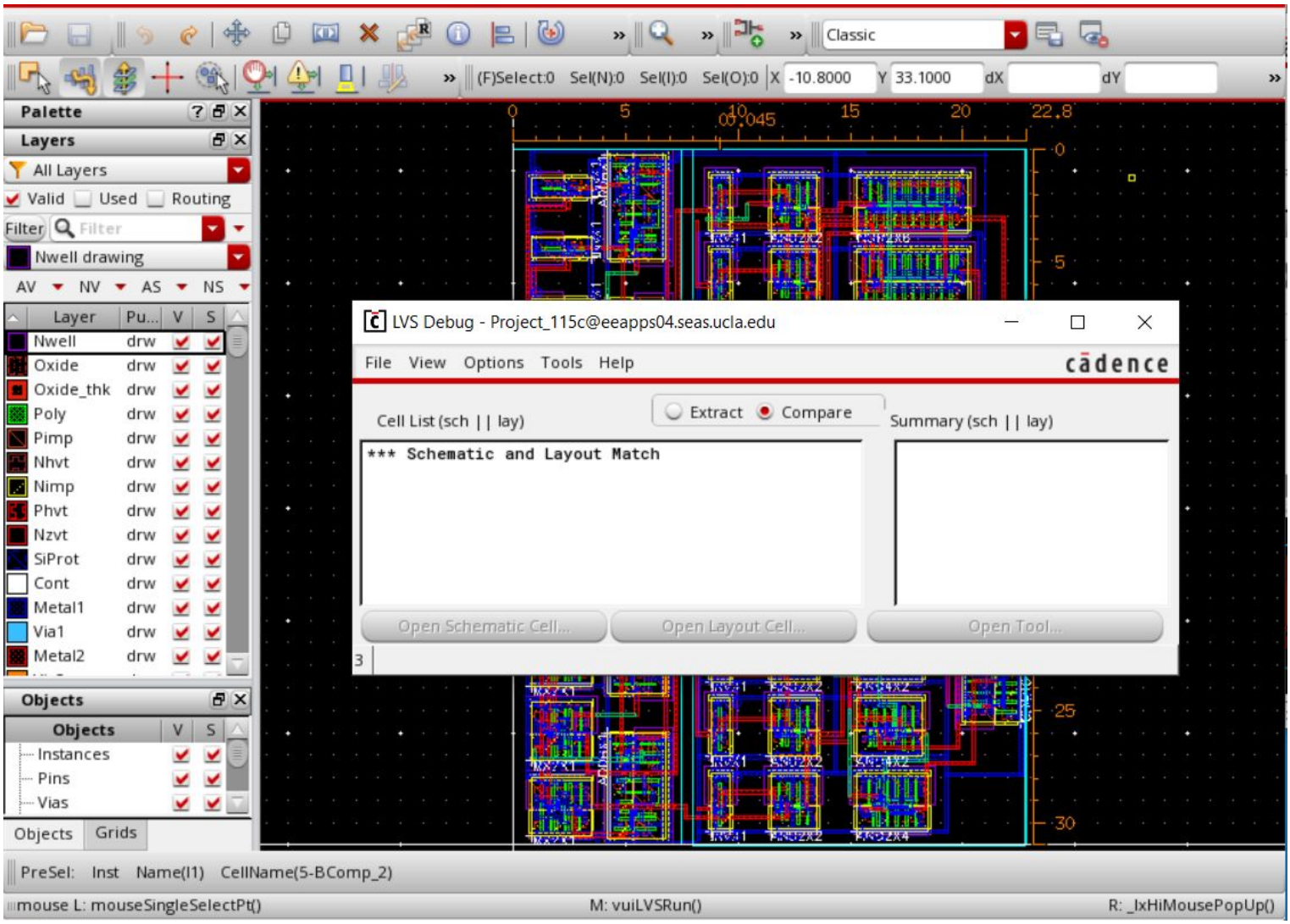


Run with schematic

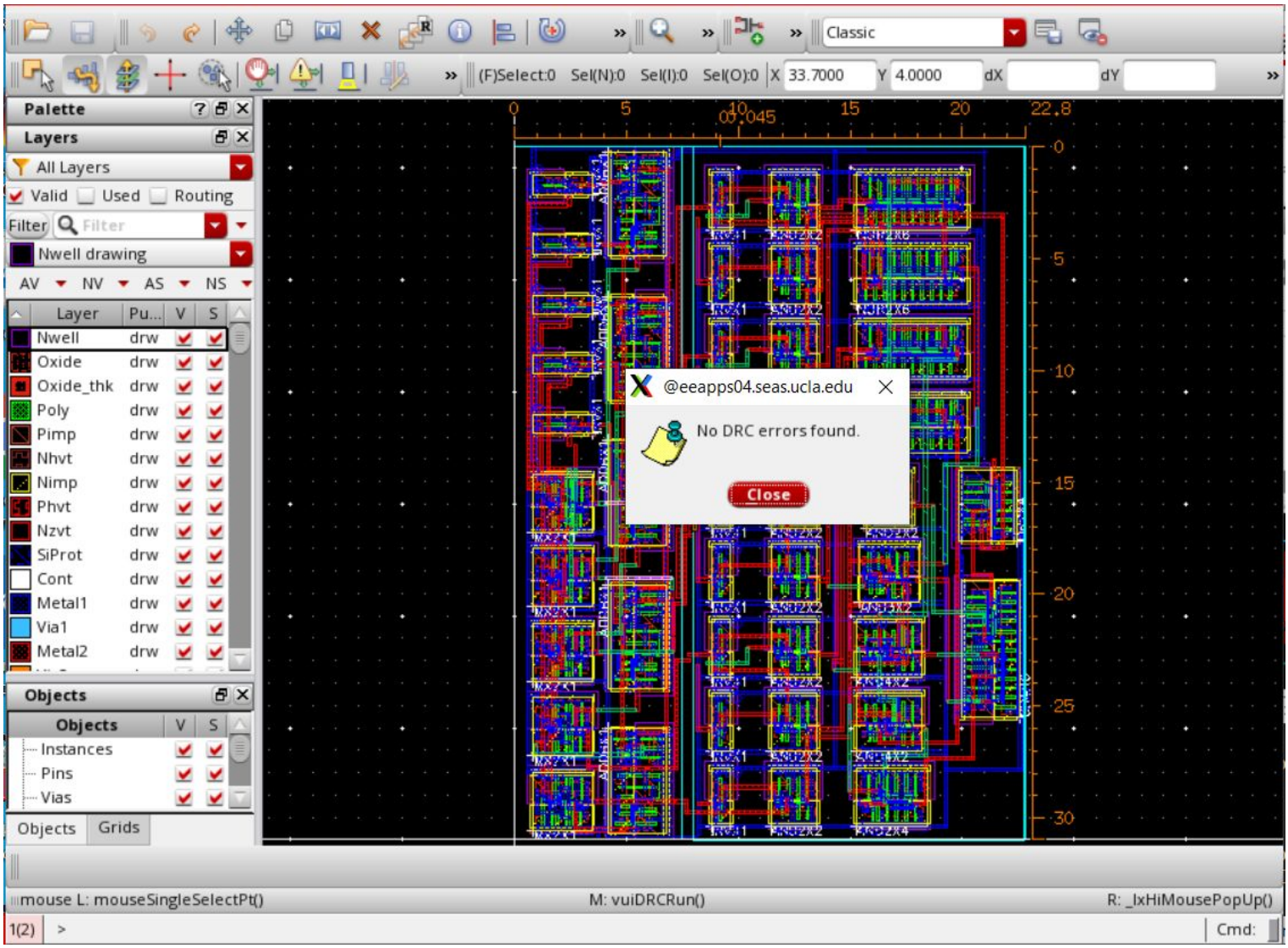




Passed LVS:

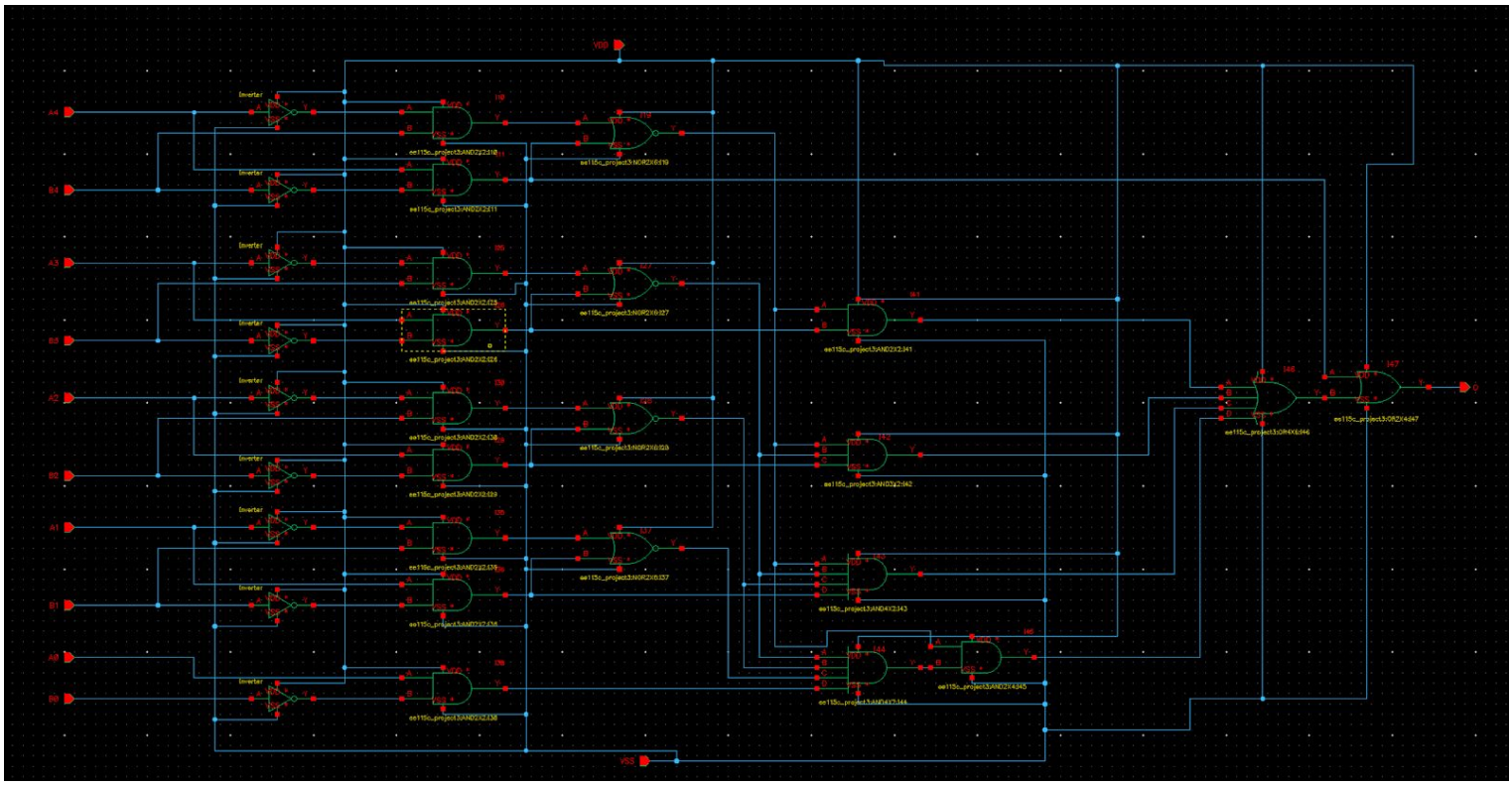

Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X -10.8000 Y 33.1000 dX dY
Palette
Layers
All Layers
Valid Used Routing
Filter
Nwell drawing
AV NV AS NS
Layer Pu... V S
Nwell drw
Oxide drw
Oxide_thk drw
Poly drw
Pimp drw
Nhvt drw
Nimp drw
Phvt drw
Nzvt drw
SiProt drw
Cont drw
Metal1 drw
Via1 drw
Metal2 drw
Objects
Objects V S
Instances
Pins
Vias
Objects Grids
LVS Debug - Project_115c@eeapps04.seas.ucla.edu
File View Options Tools Help
cadence
Extract Compare
Cell List (sch || lay)
Summary (sch || lay)
*** Schematic and Layout Match
Open Schematic Cell...
Open Layout Cell...
Open Tool...
PreSel: Inst Name(I1) CellName(5-BComp_2)
mouse L: mouseSingleSelectPt()
M: vuiLVSRun()
R: _lxHiMousePopUp()

Passed DRC:

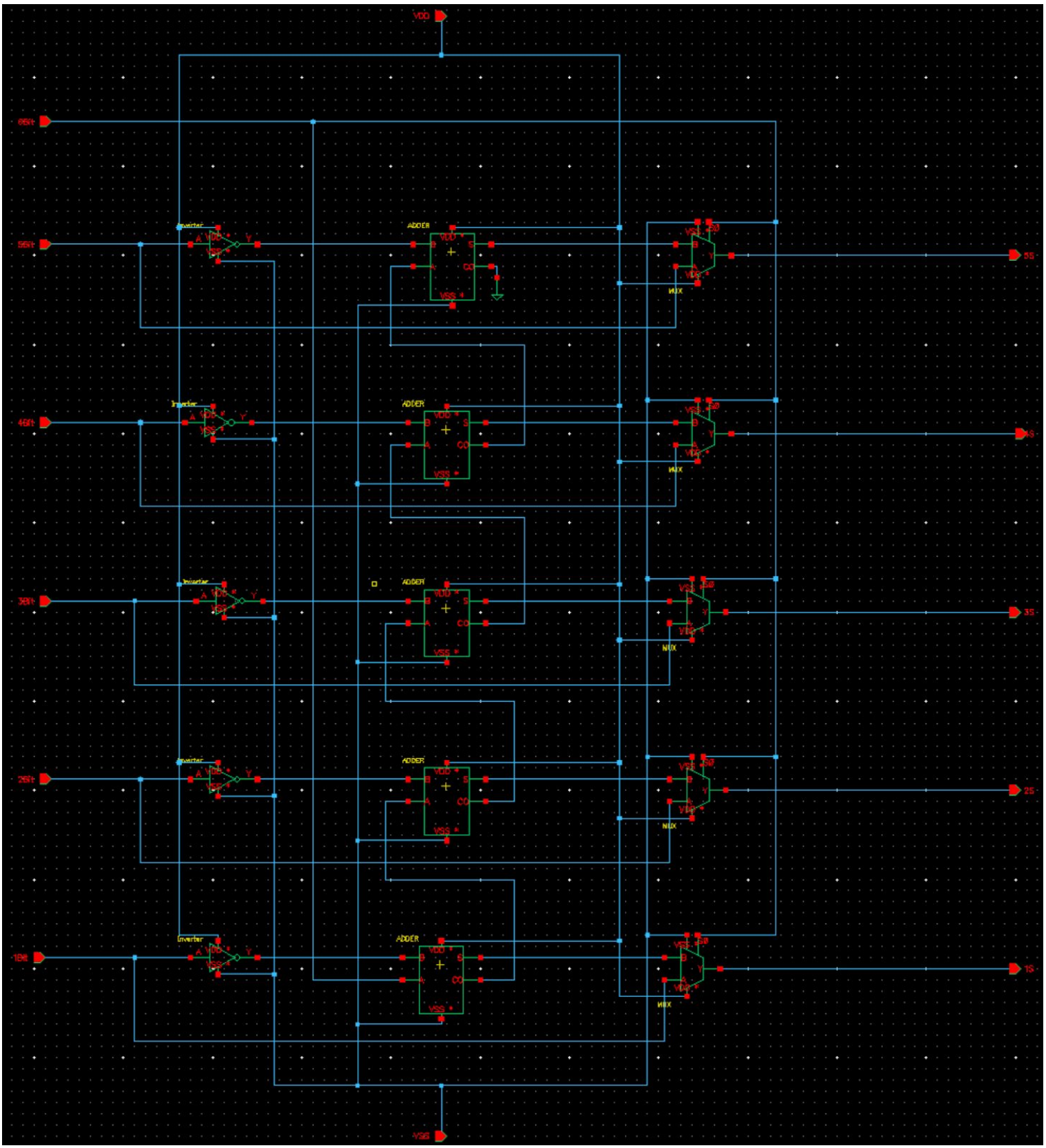

Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X 33.7000 Y 4.0000 dX dY
Palette
Layers
All Layers
Valid Used Routing
Filter
Nwell drawing
AV NV AS NS
Layer Pu... V S
Nwell drw
Oxide drw
Oxide_thk drw
Poly drw
Pimp drw
Nhvt drw
Nimp drw
Phvt drw
Nzvt drw
SiProt drw
Cont drw
Metal1 drw
Via1 drw
Metal2 drw
Objects
Objects V S
Instances
Pins
Vias
Objects Grids
@eeapps04.seas.ucla.edu
No DRC errors found.
Close
mouse L: mouseSingleSelectPt()
M: vuiDRCRun()
R: _lxHiMousePopUp()
1(2)
Cmd:

Schematic

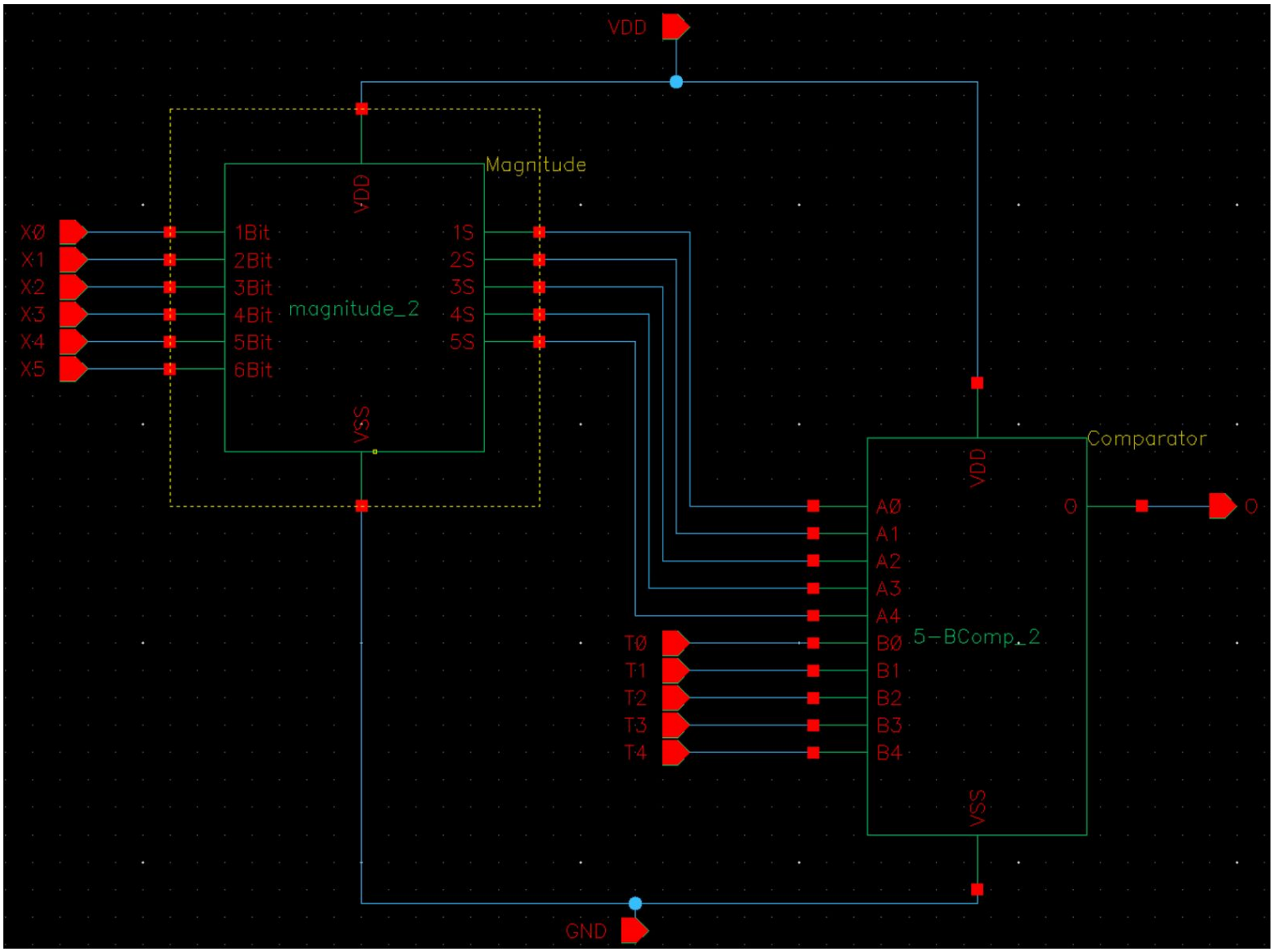
Comparator



Absolute value



Top cell


VDD
Magnitude
VDD
X0
X1
X2
X3
X4
X5
1Bit
2Bit
3Bit
4Bit
5Bit
6Bit
magnitude_2
1S
2S
3S
4S
5S
VSS
Comparator
VDD
A0
A1
A2
A3
A4
O
O
T0
T1
T2
T3
T4
B0
B1
B2
B3
B4
5-BComp_2
VSS
GND