ECE216B   VLSI Signal Processing   **Winter 2021**
Prof. Dejan Marković   Homework #2

Due: Wednesday February 10, 10am

Problem 1: DSP Arithmetic

The objective of this problem is to compare two divider designs: CORDIC and Newton-Rhapson, using MATLAB/Simulink blockset. You need to calculate 1/N, where N is an 8-bit input operand with 5 fractional bits, signed (8, 5). Assume that minimum value for N is 2^{-5}.

a)   Realize the fixed-point divider using bit-parallel CORDIC architecture in Simulink (using basic Simulink blocks). Determine the number of bits at the output to be within 0.001% of the ideal output. How many iterations are needed to converge to the desired accuracy?

b)   Realize the divider (in Simulink) using Newton-Rhapson iterative formula. For the same number of bits as in 1a, how many iterations are needed to converge to the same accuracy? Choose initial condition so that the algorithm is guaranteed to converge. Compare the results with 1a.

c)   Implement the initial condition circuit that guarantees convergence in 4 iterations.

Problem 2: Iteration Bound

Consider critical path for the two dividers from 1. What is the iteration bound? The iteration bound is defined as max{loop delay / number of registers in the loop}.

PROBLEM 3: Quantization Effects and General Knowledge

a) We need to add two finite-precision numbers with (12,4) and (7,3) bits. The numbers indicate (*total*, *fractional*) bits. What is the required wordlength that doesn't degrade the accuracy of the result for the following cases:

    2's complement:

    Sign-magnitude:

    1's complement:

b) 2's complement has lower switching activity than sign-magnitude arithmetic: **T**   **F**

Due to:

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c) Each bit of quantization improves SNR by 3dB: **T**   **F**

Explanation:

_____

d) Truncation works well in feedback systems: **T**   **F**

Because:

_____

e) Pipelining can reduce energy by _____,

or increase throughput because   _____.

f) Inserting pipeline registers into recursive loops does not alter functionality.   **T**   **F**

Explanation:

_____

g) In leakage-limited scaling, voltage can decrease faster than transistor size.   **T**   **F**

Because:

_____

h) Dark silicon (utilization wall) occurs

because _____