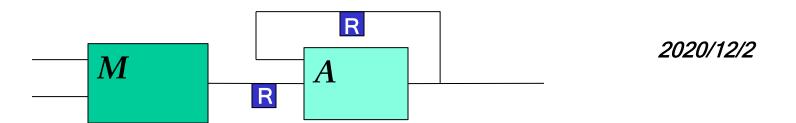
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Design Features

- Used only 10 multipliers and 10 adders. Less area and minimum number of blocks design.
- Combined with pipelining and parallelism design. Each neuron has only 1 multiplier and 1 adder with pipelining process. 10 neurons with parallelism structure.
- Feedback loop design allows one adder to add up all values.
- Object oriented design. Put max_selector and neuron as the sub-module and use them in Image_Classifier which is the top module

Synthesis Result

Technology	Synopsys 32nm	
Core Area	Total cell area: 0.543418 mm^2 Total area: 0.932017 mm^2	
Power	Internal power: 3.35 mW Switching power: 0.497 mW Leakage Power: 0.903 W Total Power: 0.942 W	
Energy/Image	Ptotal*Nclk*Tclk= 0.7687 uJ/Image	
Energy-Area Product	0.716 uJ*mm^2	

Clock Period	1ns
N clk Cycles to finish	816
Delay	1632ns

Accuracy result

89% for 200 images

85% for 10000 images

84% for 500 images

Improvement:

I used a lot of FSM states in my logic. It might try to optimize the code to reduce the states.

98% for 1000 images