



MIPS Instruction Set

-simplified -

Data Transfer Instructions

	Instruction		Example	D
li	\$reg, imm	li \$t0,	0x100	L
la	\$reg, <i>label</i>	la \$a1,	. Label	L
lui	\$reg0, imm	lui \$a0,	0x1F80	L
move	\$ren0 \$ren1	move \$a0	\$c1	_

Description

Loads an Immediate (constant) value into a register.

Loads the Address that a label points to into a register.

Loads Upper Immediate loads a value in the upper part of a register $[\,0x\text{UUUU}--\,]$

Copies the value from one register to another.

Load Instructions (From Memory)

Instruction	Example
<pre>lw \$reg, offset(baseaddr)</pre>	lw \$t1, 0x0060(\$t0)
<pre>1h \$reg, offset(baseaddr)</pre>	lh \$t1, 0x0060(\$t0)
<pre>1b \$reg, offset(baseaddr)</pre>	1b \$t1, 0x0060(\$t0)
lwu \$reg, offset(baseaddr)	lwu \$t1, 0x0060(\$t0)
<pre>1hu \$reg, offset(baseaddr)</pre>	lhu \$t1, 0x0060(\$t0)
lbu \$reg, offset(baseaddr)	1bu \$t1, 0x0060(\$t0)

Description

Loads Word (32 bits) from an address, where the final address is an immediate offset from a baseaddr that must be stored in a register.

Loads Half (16 bits) from an address, where the final address is an $\,$ immediate offset from a baseaddr that must be stored in a register.

Loads Byte (8 bits) from an address, where the final address is an

Loads Word (32 bits) Unsigned from an address, where the final address is

an immediate offset from a baseaddr that must be stored in a register. Loads Half (16 bits) Unsigned from an address, where the final address is an

immediate offset from a baseaddr that must be stored in a register. Loads Byte (8 bits) Unsigned from an address, where the final address is an

immediate offset from a baseaddr that must be stored in a register

Store Instructions (To Memory)

Instruction	Example
sw \$reg, offset(base	eaddr) sw \$t1, 0x0060(\$t0)
sh \$reg, offset(base	eaddr) sh \$t1, 0x0060(\$t0)
sb \$reg, offset(base	eaddr) sb \$t1, 0x0060(\$t0)
swu \$reg, offset(base	eaddr) swu \$t1, 0x0060(\$t0)
shu \$reg, offset(base	eaddr) shu \$t1, 0x0060(\$t0)
sbu \$reg, offset(base	eaddr) sbu \$t1, 0x0060(\$t0)

Description

Store Word (32 bits) from a register to an address, where the final address is an immediate offset from a baseaddr that must be stored in a register

Store Half (16 bits) from a register to an address, where the final address is an immediate offset from a baseaddr that must be stored in a register

Store Byte (8 bits) from a register to an address, where the final address is an immediate offset from a baseaddr that must be stored in a register.

Store Word (32 bits) Unsigned from a register to an address, where the final $\,$ address is an immediate offset from a baseaddr that must be stored in a register. Store Half (16 bits) Unsigned from a register to an address, where the final address is an immediate offset from a baseaddr that must be stored in a register.

Store Byte (8 bits) Unsigned from a register to an address, where the final address is an immediate offset from a baseaddr that must be stored in a register.

Shift Instructions

		nstr	UCTION		-	xampı	e
sll	. \$a,	\$b,	imm	sll	\$t0,	\$t0,	1
srl	. \$a,	\$b,	imm	srl	\$t0,	\$t0,	2
sra	\$a,	\$b,	imm	sra	\$t0,	\$t0,	1
sll	v \$a,	\$b,	\$c	sllv	\$t0,	\$t0,	\$t1
srl	v \$a,	\$b,	\$c	srlv	\$t0,	\$t0,	\$t2
sra	v \$a,	\$b,	\$c	srav	\$t0,	\$t1,	\$t2

Description

Shift Left Logical by a constant amount of bits. \$a = \$b << *imm* Shift Right Logical by a constant amount of bits. \$a = \$b >>> *imm* Shift Right Arithmetic by a constant amount of bits. \$a = \$b >> imm Shift Left Logical by the amount in the register. Shift Right Logical by the amount in the register.

\$a = \$b << *\$c* \$a = \$b >>> *\$c* Shift Right Arithmetic by the amount in the register. a = b >> c

Addition Instructions

Instruction	Example
add \$a, \$b, \$c	add \$t0, \$t0, \$t1
addu \$a, \$b, \$c	addu \$t0, \$t1, \$t2
addi \$a, \$b, imm	addi \$t0, \$t1, 5
addiu \$a, \$b, <i>imm</i>	addiu \$t0, \$t0, 1

Description

Adds (signed) numbers from registers. a = b + ca = b + cAdds Unsigned numbers from registers. Adds an Immediate (signed) number. a = b + imma = b + immAdds Immediate Unsigned numbers.

Subtraction Instructions

Instruction	Example
sub \$a, \$b, \$c	sub \$t0, \$t0, \$t1
suhu \$a \$h \$c	subu \$t0 \$t1 \$t2

Description

Subtracts (signed) numbers from registers. a = b - cSubtracts Unsigned numbers from registers. a = b - c

Multiplication Instructions

Instruction	Example		
mult \$a, \$b	mult \$t0, \$t1		
multu \$a, \$b	multu \$t0, \$t1		

Description

Division Instructions

Instruction	Example		
div \$a, \$b	div \$t0, \$t1		
divu \$a, \$b	divu \$t0, \$t1		

Description

 ${\it Multiply (signed) numbers from two registers.}$ Multiply Unsigned numbers from two registers.

Divide (signed) numbers from two registers.

Divide Unsigned numbers from two registers.

store their results in two additional regiters, HI and LO. We can fetch the contents from **HI** and **LO** using the instructions **mfhi** and **mflo**.

Multiply & Divide instructions will

mfhi \$reg mflo \$reg

Logical Bitwise Instructions

	I	nstru	uction		E	xampl	e	
and	\$a,	\$b,	\$c	and	\$t0,	\$t0,	\$t1	L
andi	\$a,	\$b,	\$c	andi	\$t0,	\$t1,	0xF000	L
or	\$a,	\$b,	\$c	or	\$t0,	\$t0,	\$t1	L
ori	\$a,	\$b,	\$c	ori	\$t0,	\$t1,	0x00FF	L
xor	\$a,	\$b,	\$c	xor	\$t0,	\$t0,	\$t1	L
xori	\$a,	\$b,	\$c	xori	\$t0,	\$t0,	0xFFFF	L

Description

Logical bitwise AND a = b & cLogical bitwise AND Immediate \$a = \$b & imm Logical bitwise OR $a = b \mid c$ Logical bitwise OR Immediate \$a = \$b | imm Logical bitwise Exclusive-OR $a = b ^ sc$ Logical bitwise Exclusive-OR Immediate \$a = \$b ^ imm

Branch Instructions

Instruction	Example	Description
beq a, b, label	beq \$t0, \$t1, Label	Branch if Equals
bne a, b, label	bne \$t0, 100, Label	Branch if Not Equals
blt a, b, label	blt \$t0, \$t2, Label	Branch if Less Than
ble a, b, label	ble \$t0, \$t2, Label	Branch if Less or Equals
bgt a, b, label	bgt \$t0, 5, Label	Branch if Greater Than
bge a, b, label	bge \$t0, \$t2, Label	Branch if Greater or Equals
bltu a, <i>b</i> , label	bltu \$t0, \$t2, Label	Branch if Less Than (unsigned)
bleu a, b, label	bleu \$t0, \$t2, Label	Branch if Less or Equals (unsig
bgtu a, b, label	bgtu \$t0, 5, Label	Branch if Greater Than (unsigne
bgeu a, b, label	bgeu \$t0, \$t2, Label	Branch if Greater or Equals (uns

if (a == b) then jump to label if (a != b) then jump to label if (a < b) then jump to label if (a <= b) then $jump\ to\ label$ if (a > b) then jump to label if (a >= b) then jump to label if (a < b) then jump to label if (a <= b) then jump to labelif (a > b) then jump to label ned) if (a >= b) then jump to label nsigned)

b can be either a register or an immediate

Jump Instructions

	Instruction	Example	Description
j	label	j Loop	Unconditional jump to Label (address)
ja	l label	jal Subroutine	Jump & Link stores the return address in the register \$ra .
jr	\$reg	jr \$t1	Jump to Register jumps to an address in a register
ja	l r \$reg	jalr \$t0	Jump & Link Register jumps to an address in a register and stores the return address in \$ra .