A Novel Multi-Shape Chaotic Attractor and Its FPGA Implementation

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***Abstract*—This brief introduces a novel multi-shape chaotic system which can generate a $2n+2$-scroll chaotic attractor in *y-x* plane, a $2n+2$-star chaotic attractor in *z-y* plane, a $2n+2$-flower chaotic attractor in *z-x* plane and a $2n+2$-multiple layer spiral chaotic attractor in *z-w* plane with the natural number *n*. Various chaotic attractors are illustrated not only by computer simulation but also by FPGA implementation. This novel multi-shape chaotic system is suitable for the potential application of secure communication.**

***Index Terms*—Multi-scroll chaotic attractor, multi-star chaotic attractor, multi-flower chaotic attractor, multi-layer spiral chaotic attractor, FPGA.**

I. Introduction

Recently, theoretical design of various chaos generators has been a topic of increasing interest because of their potential in many real-world engineering fields, such as secure communication. Particularly, since Suykens and Vandewalle firstly introduced a family of *n*-double scroll chaotic attractors based on the so-called quasi-linear function approach [1], chaotic systems that can generate multiple chaotic attractors have been intensively investigated for their potential applications, and many valuable results have been proposed [2]–[10]. For example, based on the Chua circuit and a sine function, Tang *et al.* designed a multi-scroll chaotic system that can generate multi-scroll chaotic attractors [2]. By using a smooth hyperbolic tangent function, Ozoguz *et al.* introduced an *n*-scroll chaotic attractor generator [3]. In [4], Lü and Chen presented an overview of methods for generating multi-scroll chaotic attractors and their corresponding realizations. Also, based on saturated function series and a given 3-*D* linear autonomous system, Lu *et al.* designed and analyzed a multi-scroll chaotic system that can generate 1-*D* *n*-scroll, 2-*D* $n \times m$-grid scroll and $3 - Dn \times m \times l$-grid scroll chaotic attractors, and provided experimental verifications [5]. Luo *et al.* proposed a fourth-order chaotic system with saturated function series that can generate multi-scroll chaotic attractors [6]. Zidan *et al.* proposed a V-shape multi-scroll chaotic system and deigned a circuit topology for realization [8]. Also, Chen *et al.* proposed a hyperchaotic multi-scroll system with a fractional order [9]. Aside from multi-scroll chaotic attractors, other shapes of chaotic attractors, such as multi-wing chaotic attractors and multi-folded chaotic attractors, have also been proposed in the open literatures [11]–[16]. Additionally, in [17], Yang *et al.* proposed a chaotic system with a saturated function that can generate a 2-star chaotic attractor in *y-x* plane and a 2-flower chaotic attractor in *y-w* plane. Moreover, in [18], Zhou *et al.* proposed a chaotic system with a saturated function which can generate a 2-scroll chaotic attractor in *y-x* plane, a 2-star chaotic attractor in *y-z* plane, a 2-flower chaotic attractor in *y-w* plane and a 2-layer spiral chaotic attractor in *z-w* plane.

Implementations for chaotic systems that can generate multi-shape chaotic attractors have also been intensively investigated. To date, there have been a few methods for their implementations: electronic circuits based on passive components and IC chips [19], [20], DSP [21], ARM [22], [23], Arduino [24], [25], FPGA [26]–[29]. For example, in [19], Wu *et al.* designed an electronic circuit based on current feedback operational amplifiers for implementation of a multi-scroll chaotic system. Yu *et al.* applied digital signal processors (DSP) for realization of a general multi-scroll Lorenz system [21]. Chen *et al.* used ARM to implement a chaotic system for secure communication [22]. Pan-Azucena *et al.* applied Arduino to generate multi-directional multi-scroll chaotic oscillators for application of chaotic secure communication [25]. Tlelo-Cuautle *et al.* studied FPGA realization of a multi-scroll chaotic oscillator [26]. All these implementation methods for multi-shape chaotic systems are very important for developing chaos applications. Generally speaking, among these methods, FPGA implementation is the most popular because it offers both lower cost and shorter design periods despite high barriers to entry, and it can be used effectively in digital secure communications [30]–[33].

In this brief, we propose a novel chaotic system that can generate multi-shape chaotic attractors. This brief is organized

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as follows. In Section II, the basic dynamical behavior of new multi-shape chaotic system is analyzed. Then, multiple attractor generation is presented in Section III. In Section IV, FPGA implementation of the proposed chaotic system is designed, and some experimental results are presented for confirmation.

II. New Multi-Shape Chaotic System and Its Properties

In this brief, a new chaotic system that includes signum function series is proposed and its expression is shown as follows

$$\begin{cases} \dot{x} = -ax + y - k\sum_{i=-n}^{n} \operatorname{sgn}(m(y+z)+i) \\ \dot{y} = -x + by - 2bk\sum_{i=-n}^{n} \operatorname{sgn}(m(y+z)+i) \\ \dot{z} = -cz - w + 2ck\sum_{i=-n}^{n} \operatorname{sgn}(m(y+z)+i) \\ \dot{w} = z - dw - k\sum_{i=-n}^{n} \operatorname{sgn}(m(y+z)+i) \end{cases} \tag{1}$$

where a, b, c, d, and k are parameters, and x, y, z, and w are variables of system (1). Also, n is a natural number, m is a positive number, and sgn is the signum function.

Taking $a = 1/64$, $b = 1/16$, $c = 1/8$, $d = 1/8$, $k = 1/16$, $m = 4$, $n = 0$ and the right-hand side of system (1) equals zero, the following form can be obtained

$$\begin{cases} -ax + y - k\operatorname{sgn}(m(y+z)) = 0 \\ -x + by - 2bk\operatorname{sgn}(m(y+z)) = 0 \\ -cz - w + 2ck\operatorname{sgn}(m(y+z)) = 0 \\ z - dw - k\operatorname{sgn}(m(y+z)) = 0 \end{cases} \tag{2}$$

According to the characteristics of the signum function, the area will be divided into three parts

$$\operatorname{sgn}(m(y+z)) = \begin{cases} 1, & y+z > 0 \\ 0, & y+z = 0 \\ -1, & y+z < 0 \end{cases} \tag{3}$$

Therefore, there is only one equilibrium point in each part from solving formula (2):

$$S = \begin{cases} \left(-\frac{kb}{1-ab}, \frac{k(1-2ab)}{1-ab}, \frac{k(1+2cd)}{1+cd}, \frac{kc}{1+cd}\right), & y+z > 0 \\ (0,0,0,0), & y+z = 0 \\ \left(\frac{kb}{1-ab}, -\frac{k(1-2ab)}{1-ab}, -\frac{k(1+2cd)}{1+cd}, -\frac{kc}{1+cd}\right), & y+z < 0 \end{cases} \tag{4}$$

By linearing the system (1) at each equilibrium point, the Jacobian matrix can be obtained as

$$J = \begin{bmatrix} -a & 1 & 0 & 0 \\ -1 & b & 0 & 0 \\ 0 & 0 & -c & -1 \\ 0 & 0 & 1 & -d \end{bmatrix} \tag{5}$$

From (5), one can see that parameter k is not included so that it cannot influence the stability of system. Also, because the characteristic root from the Jacobian matrix at each equilibrium point is the same: $0.0234 + 0.9992i$, $0.0234 - 0.9992i$, $-0.1250 + 1.0000i$, and $-0.1250 - 1.0000i$, so that each equilibrium point is unstable. Therefore, the system trajectory will not stay at any equilibrium point. In fact, for a given initial value, as time progresses, the trajectory of system (1) spirally diverges around its equilibrium point or changes to another. Moreover, based on the method for calculating the Lyapunov exponents in [34] and [35], the Lyapunov exponents of the proposed chaotic system can also be calculated, and the results are, 0.0399, 0, -0.1016, and -0.1366. Thus, after a long period of time, the trajectory will overflow the whole chaotic area, and a 2-scroll chaotic attractor in y-x plane, a 2-star chaotic attractor in z-y plane, a 2-flower chaotic attractor in z-x plane, and a 2-multiple layer spiral chaotic attractor in z-w plane can be obtained, as shown in Fig. 1. Note that, in Fig. 1(d), it is also a heteroclinic cycle [36].

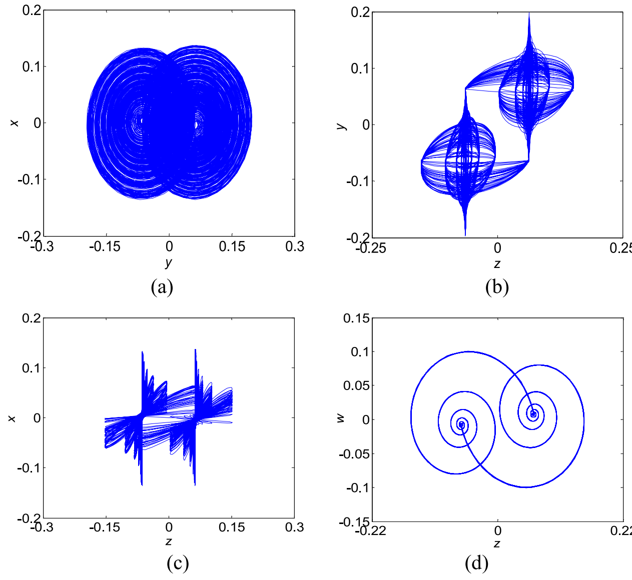

Fig. 1. Phase portrait of chaotic system with $n = 0$: (a) 2-scroll chaotic attractor; (b) 2-star chaotic attractor; (c) 2-flower chaotic attractor; (d) 2-multiple layer spiral chaotic attractor.

III. Multiple Attractor Generation

When $n = 2$ and m is a positive number, the equilibrium points of the system are

$$S = \begin{cases} \left(-\frac{5kb}{1-ab}, \frac{5k(1-2ab)}{1-ab}, \frac{5k(1+2cd)}{1+cd}, \frac{5kc}{1+cd}\right), & \frac{2}{m} < y+z \\ \left(-\frac{3kb}{1-ab}, \frac{3k(1-2ab)}{1-ab}, \frac{3k(1+2cd)}{1+cd}, \frac{3kc}{1+cd}\right), & \frac{1}{m} < y+z < \frac{2}{m} \\ \left(-\frac{kb}{1-ab}, \frac{k(1-2ab)}{1-ab}, \frac{k(1+2cd)}{1+cd}, \frac{kc}{1+cd}\right), & 0 < y+z < \frac{1}{m} \\ (0,0,0,0), & y+z = 0 \\ \left(\frac{kb}{1-ab}, -\frac{k(1-2ab)}{1-ab}, -\frac{k(1+2cd)}{1+cd}, -\frac{kc}{1+cd}\right), & -\frac{1}{m} < y+z < 0 \\ \left(\frac{3kb}{1-ab}, -\frac{3k(1-2ab)}{1-ab}, -\frac{3k(1+2cd)}{1+cd}, -\frac{3kc}{1+cd}\right), & -\frac{2}{m} < y+z < -\frac{1}{m} \\ \left(\frac{5kb}{1-ab}, -\frac{5k(1-2ab)}{1-ab}, -\frac{5k(1+2cd)}{1+cd}, -\frac{5kc}{1+cd}\right), & y+z < -\frac{2}{m} \end{cases} \tag{6}$$

However, the Jacobian matrix of (1) under $n = 2$ is the same as that under $n = 0$. Therefore, the system is also in unstable operation under $n = 2$ at each equilibrium point. Then, a 6-scroll chaotic attractor in y-x plane, a 6-star chaotic attractor in z-y plane, a 6-flower chaotic attractor in z-x plane, and a 6-multiple layer spiral chaotic attractor in z-w plane can be obtained, as shown in Fig. 2. Note that, in Fig. 2(d), it is also a heteroclinic cycle [36]. Likewise, with natural number n increasing, a $2n+2$-scroll chaotic attractor in y-x plane, a $2n+2$-star chaotic attractor in y-z plane, a $2n+2$-flower chaotic attractor in y-w plane, and a $2n+2$-multiple layer spiral chaotic attractor in z-w plane can be generated easily.

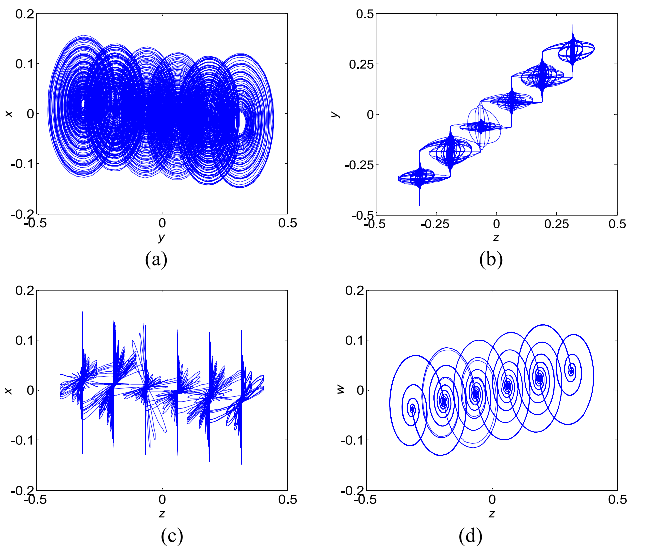

Fig. 2. Phase portrait of chaotic system with $n = 2$: (a) 6-scroll chaotic attractor; (b) 6-star chaotic attractor; (c) 6-flower chaotic attractor; (d) 6-multiple layer spiral chaotic attractor.

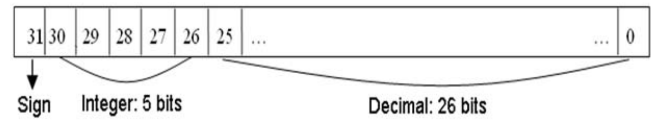

Fig. 3. Adopted fixed-point format: 1 bit for sign, 5 bits for integer, and 26 bits for decimal.

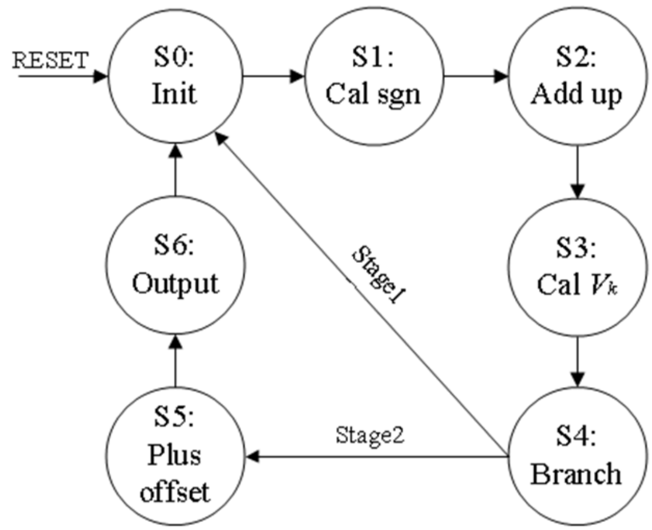

Fig. 4. State machine flowchart.

IV. FPGA Implementation

FPGA-based digital chaotic generation is important and convenient for applications of digital secure communication [31]–[33]. In this section, the iteration formulas based on the 2-order Runge-Kutta method are shown, and then the fixed- point data format is presented. Subsequently the implementation framework of a Verilog HDL (Hardware Description Language) program is followed, and the hardware platform and some experimental results are presented for validation.

A. Two-Stage Iteration

The discrete description of the proposed chaotic system is

$$\begin{cases} x_{k+1} = x_k + dt * (-ax_k + y_k - k\sum_{i=-n}^{n} \mathrm{sgn}(m(y_k + z_k) + i)) \\ y_{k+1} = y_k + dt * (-x_k + by_k - 2bk\sum_{i=-n}^{n} \mathrm{sgn}(m(y_k + z_k) + i)) \\ z_{k+1} = z_k + dt * (-cz_k - w_k + 2ck\sum_{i=-n}^{n} \mathrm{sgn}(m(y_k + z_k) + i)) \\ w_{k+1} = w_k + dt * (z_k - dw_k - k\sum_{i=-n}^{n} \mathrm{sgn}(m(y_k + z_k) + i)) \end{cases} \tag{7}$$

where dt is the discrete time step.

Denoting the state vector in step k as $V_k = (x_k,\ y_k,\ z_k,\ w_k)^T$, then the chaotic system can be expressed as $dV_k/dt = G(V_k)$, and formula (7) is shown as

$$V_{k+1} = V_k + dt * G(V_k) \tag{8}$$

According to the 2-order Runge-Kutta method, the two-stage iteration routine can be shown as follows.

In stage 1, the state vector is updated as follows

$$\begin{cases} dt = \frac{h}{2} \\ V_{k+\frac{1}{2}} = V_k + dt * G(V_k) \end{cases} \tag{9}$$

where state vector $V_{k+1/2}$ indicates the intermediate results in a half step, and h represents the discrete time gap, normally taken as $h = 1/128$.

In stage 2, the state vector is updated based on $V_{k+1/2}$ from stage 1, and then state vector V_{k+1} for step $k + 1$ can be obtained.

$$\begin{cases} dt = h \\ V_{k+1} = V_k + dt * G\Big(V_{k+\frac{1}{2}}\Big). \end{cases} \tag{10}$$

B. Fixed-Point Format

Here, the 32Q26 signed fixed-point format is adopted here, as shown in Fig. 3. It can be seen that 1 bit is the sign part, 5 bits is the integer part, and 26 bits is the decimal part. Therefore, numerical precision can be up to $1.49e^{-8}$.

C. Verilog HDL Implementation

Verilog HDL programming is adopted here to realize the digital chaotic system's implementation in FPGA. The logic function and operation defined by Verilog HDL language can be converted into a hardware netlist and then configured into FPGA to generate the corresponding complex digital circuit. Because of the high flexibility of parallel implementation in FPGA, the digital chaotic generator can work at high speed. In programming, state machine method is used to split the digital chaotic generator into several subprocesses. The state machine adopted here includes seven states: S_0, S_1, S_2, S_3, S_4, S_5, S_6, as shown in Fig. 4.

- S_0: Initialize the values of register variables in the circuit, including the values of $(x_k,\ y_k,\ z_k,\ w_k)^T$
- S_1: Parallel implementation of $\mathrm{sgn}(m(y+z)+i)$ operations, where $i = -n : n$.
- S_2: Add up all $\mathrm{sgn}(m(y+z)+i)$; parallel implementation of ax, by, cz, dw operations

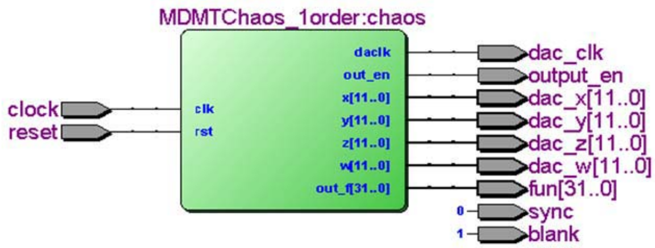

Fig. 5. Top-layer RTL of the proposed chaotic system.

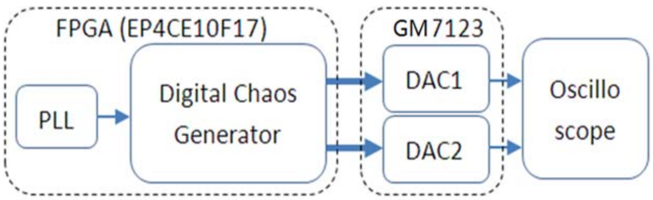

Fig. 6. Experimental hardware platform for the proposed chaotic system.

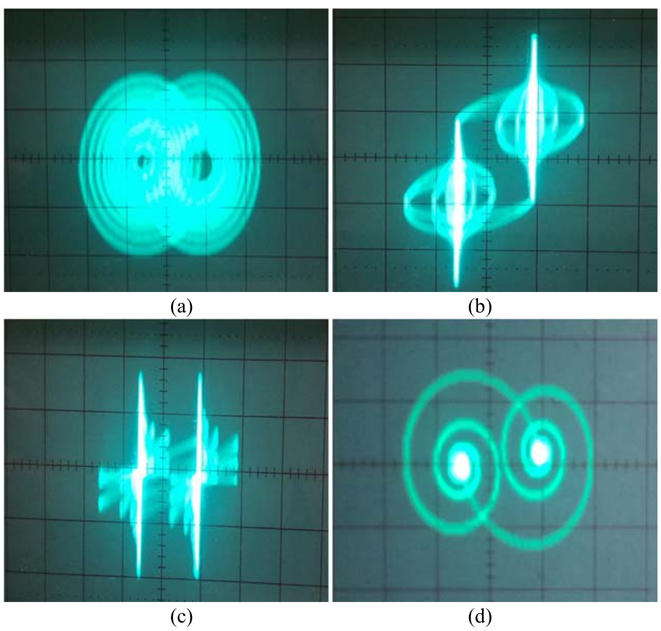

Fig. 7. Phase portrait of chaotic system with $n = 0$: (a) 2-scroll chaotic attractor; (b) 2-star chaotic attractor; (c) 2-flower chaotic attractor; (d) 2-multiple layer spiral chaotic attractor.

S_3: Parallel implementations to get the results of $\dot{x}$, $\dot{y}$, $\dot{z}$, and $\dot{w}$.

S_4: If in stage 1, implement the operation in (9); direct to state S_0. If in stage 2, implement the operation in (10); direct to state S_5

S5: Add a positive offset into the results obtained in state S_4 to avoid negative outputs

S6: Output the digital chaotic signal to the external digital-to- Analog converter (DAC) chip; direct to state S_0

The top-layer RTL viewer of the above realization is shown in Fig. 5, where the outputs of block include: “dac_clk” (the clock for external DAC chip), “ouput_en” (the high level signal indicates the output is valid), “dac_x[11…0]” (the digital output of x in each step), “dac_y[11…0]” (the digital output of y in each step), “dac_z[11…0]” (the digital output of z in each step), “dac_w[11…0]” (the digital output of w in each step), “fun[31…0]” (the output probe of internal function $\mathrm{sgn}(y + z + i)$ for debug), “sync” (the control signals for the external DAC chip) and “blank” (the control signals for the external DAC chip).

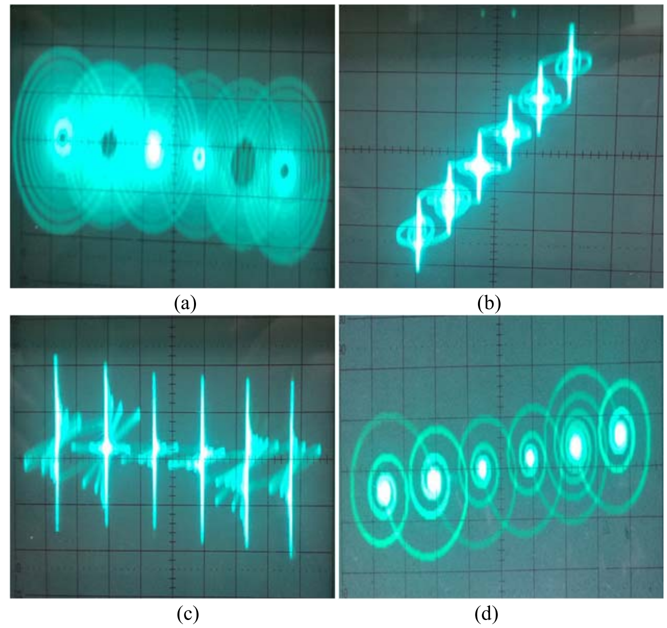

Fig. 8. Phase portrait of chaotic system with $n = 2$: (a) 6-scroll chaotic attractor; (b) 6-star chaotic attractor; (c) 6-flower chaotic attractor; (d) 6-multiple layer spiral chaotic attractor.

D. Experimental Results

The hardware platform is developed with an Altera Cyclone IV EP4CE10F17C8 FPGA and an external DAC chip GM7123. The architecture of this hardware platform is shown in Fig. 6, and the experimental results are shown in Figs. 7 and 8. By comparing Figs. 1 and 2 and Figs. 7 and 8, respectively, one can see that the results are in good agreement. Note that, in this FPGA implementation, the clock with frequency can up to 117.4 MHz, and the corresponding total power dissipation is 123.35 mW. Additionally, 20% of the logic elements, 24% of the memory bits, and 0% of the embedded multipliers of the Altera Cyclone IV EP4CE10F17C8 FPGA are occupied.

V. Conclusion

In this brief, a novel multi-shape chaotic system constructed by combination of a linear system and signum function series is proposed and analyzed, and is implemented in FPGA. This proposed chaotic system, with different natural numbers n, can generate a $2n + 2$-scroll chaotic attractor in y-x plane, a $2n + 2$-star chaotic attractor in z-y plane, a $2n + 2$-flower chaotic attractor in z-x plane, and a $2n+2$-multiple layer spiral chaotic attractor in z-w plane. The proposed system is different from other chaotic systems that can generate only multi-scroll or multi-wing chaotic attractors. It is anticipated that chaos applications to engineering problems would benefit from the results of this brief.

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