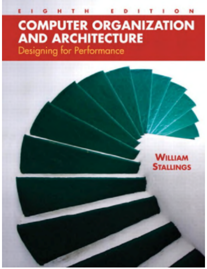
Lecture 01: Introduction to Microcomputer & Embedded Systems

Reference Book:

William Stallings Computer Organization and Architecture

- Chapter 1 & 2

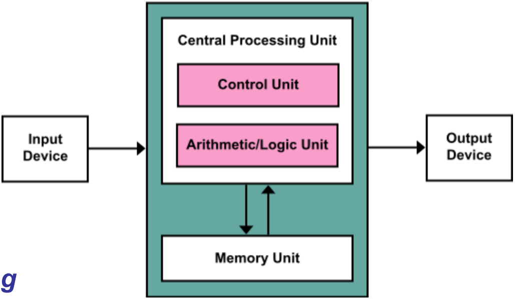

EIGHTH EDITION
COMPUTER ORGANIZATION AND ARCHITECTURE
Designing for Performance
WILLIAM STALLINGS

微型计算机原理与接口技术（第四版）

- 第一章

What is a computer?

Von Neumann Architecture 冯诺依曼结构



1.Five components partitioning

- Input 输入
- Output 输出
- Memory 存储器
- ALU 算术逻辑单元
- Control unit 控制单元

I/O devices

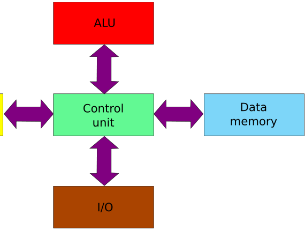
Memory

CPU

CU
ALU
Registers.

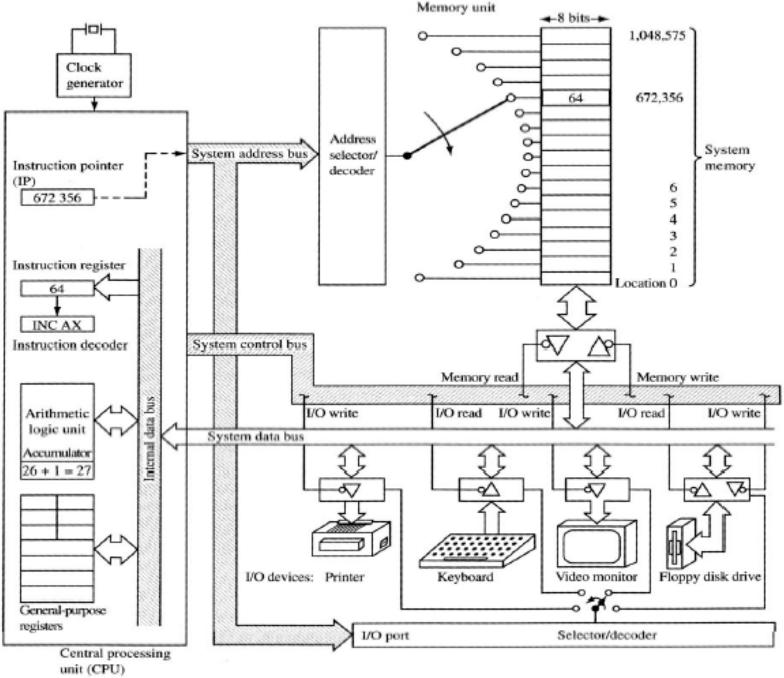
2. Three key concepts:

- Both ***instructions*** and ***data*** are stored in a **single** read-write memory
- The contents of memory are **addressable** by location, without regard to the type of data
- Execution occurs in a **sequential** fashion 顺序执行



Harvard architecture

Stored Program Concept



Microprocessor 微处理器

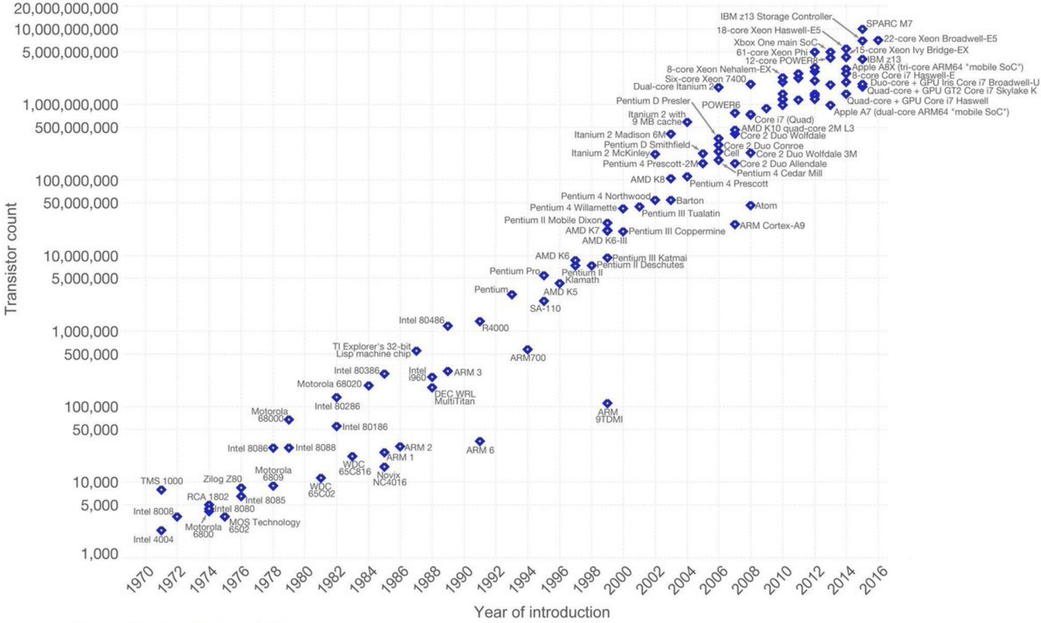
- Microprocessors
  - the CPU circuitry can been reduced to *IC* (Integrated Circuit) *s*cale, consisting of ***ALU***, ***CU*** and ***registers***
  - contains **no** RAM, ROM, or I/O ports on the chip itself
  - e.g., Intel’s x86 family (8088, 8086, 80386, 80386, 80486, Pentium); Motorola’s 680x0 family (68000, 68010, 68020, etc)

Moore's Law – The number of transistors on integrated circuit chips (1971-2016)

Our World in Data

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are strongly linked to Moore's law.

晶体管的数量每两年增加1倍.



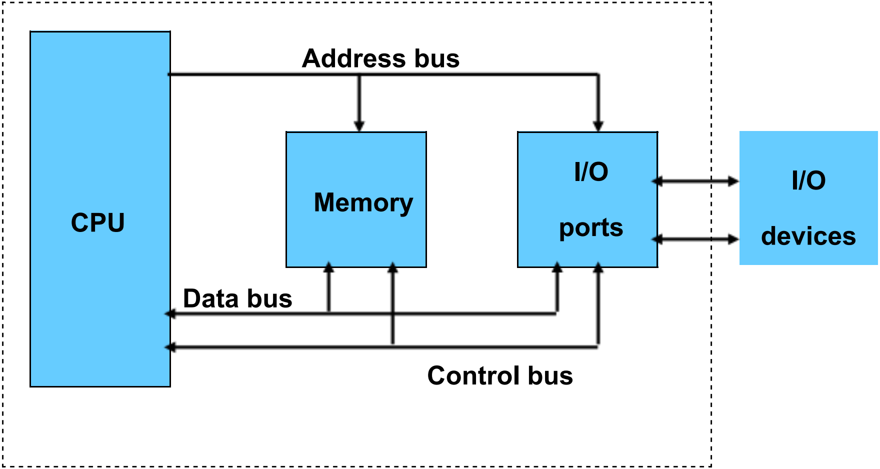
Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Microcomputer 微型计算机

微处理器.

- *CPU: processes information stored in the memory*
  - *Microprocessor*
- *Memory: stores both instructions and data*
  - ROM, RAM
- *Input/Output ports, I/O**接口**: provide a means of communicating with the CPU*
  - Connecting I/O devices, e.g., keyboard, monitor, tape, disk, printer and etc.
- *BUS **总线**: interconnecting all parts together*
  - Address bus
  - Data bus
  - Control bus

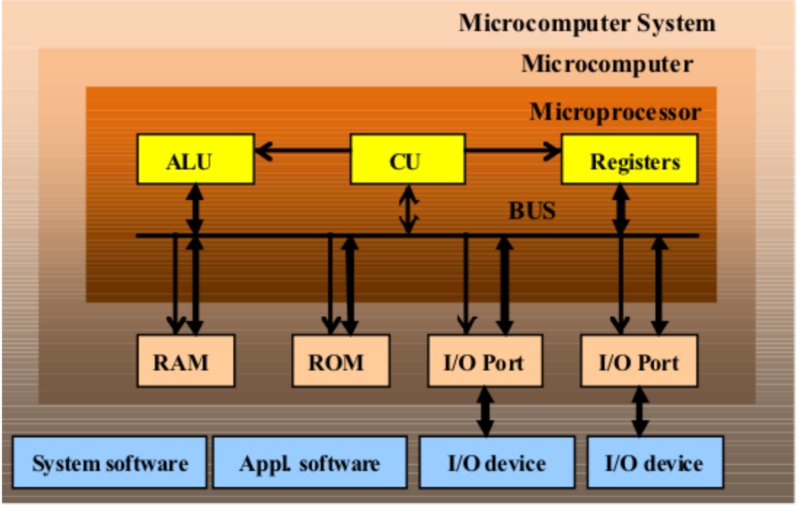
Microcomputer Structure



Microcomputer System

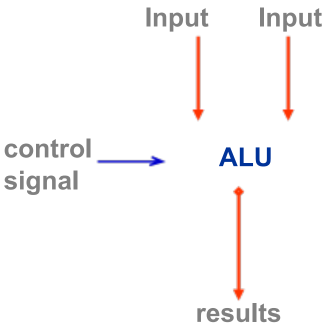
- Microcomputer
- Peripheral I/O devices
- Software
  - System software
    - e.g., OS, compilers, drivers
  - Application software
    - e.g. Word, MatLab, Media player, Latex…

Microcomputer System Structure



Hardware: CPU (1) - ALU

- Arithmetic Logic Unit (ALU) 算术逻辑单元.
  - Arithmetic functions: add, subtract, multiply and divide
  - Logic functions: AND, OR, and NOT
- ALU is a multifunctional calculator
  - What specific calculation will be taken depends on the particular control signal
- Two inputs
- Calculation result can be temporarily stored in one of the *registers*



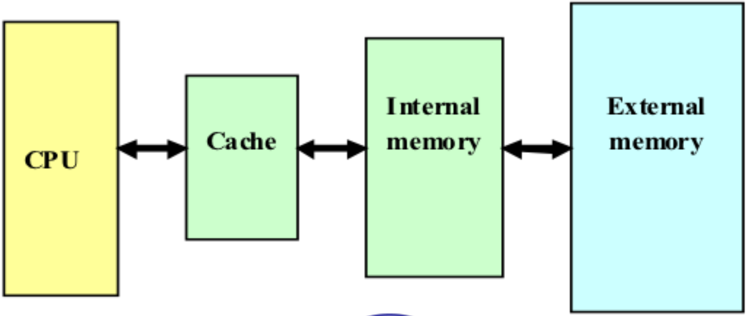
Hardware: CPU (2) - CU

- Control Unit works under *instructions 指令*
- An instruction is a pre-defined code which defines a specific operation, processing and exchanging information among CPU, memory and I/O devices.
- CU contains an *instruction decoder 指令解码器*
  - decodes an instruction and generates all control signals, coordinating all activities within the computer
- CU contains a *program counter 程序计数器*
  - points to the address of the next instruction to be executed

Hardware: CPU (3) – Instruction Set

- The instruction set 指令集
  - All recognizable instructions by the instruction decoder
- CISC (Complex Instruction Set Computers)
  - Variable instruction length (1 **word-** *n* words)
  - Variable execution time of different format instructions
  - More instruction formats
  - Upwardly compatible (new instruction set contains earlier generation's instructions)
  - e.g., 80x86 family has more than 3000 instructions
- RISC (Reduced Instruction Set Computers)
  - Fixed size (1 word)
  - Fixed time for all instructions
  - Easy to **pipeline** the RISC instructions (fast)
  - Fewer formats (simple hardware, shorter design cycle)
  - e.g., PowerPC, MIPS, ARM, PIC's MCU

Hardware: Memory



- Memory **hierarchy**
  - *Registers*
  - *Cache*
  - 硬盘 内存
    Primary memory: ROM, RAM
  - *Secondary memory: magnetic disk, optical memory, tape, …*

Hardware: Memory

- *Bit (b):* a binary digit that can have the value 0 or 1
- *Byte (B):* consists of 8 bits 字节→编址
  - smallest unit that can be addressed in microcomputers

1	0	1	0	1	0	1	0

- ***Nibble:*** is half a byte (4bits)
- ***Word, 字:*** the maximum number of bits that a CPU can process at one time
  - depends on the width of the CPU's registers and that of the data bus
    - e.g., if the width of the data bus is 16 bits, then a word is 16 bits; if the width of the data bus is 32 bits, then a word is 32 bits
- *Double word, 双字*
- Kilo, Mega, Giga, Tera, Peta, …

1Kb = 2^{10} bit

1M = 2^{20} bit

1G = 2^{30} bit

Memory Module Organization

To organize a memory module with given memory chips

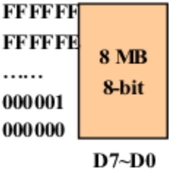
n

To organize a memory module：

u If the module needs bigger **unit of transfer** than that of given memory chips, ***bit extension***

u If the module needs larger number of words than that of given memory chips, ***word extension***

- **8-bit**

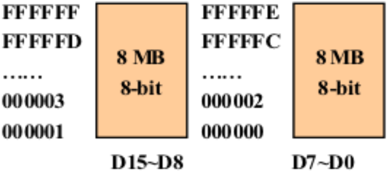


FFFFFF
FFFFFE
……
000001
000000

8 MB
8-bit

D7~D0

- **16-bit**



FFFFFF
FFFFFD
……
000003
000001

8 MB
8-bit

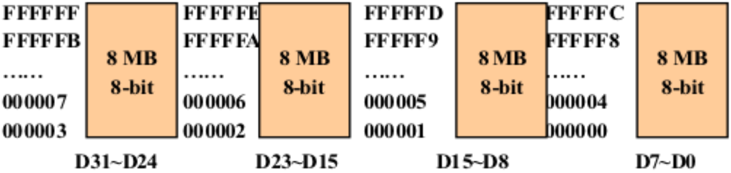
D15~D8

FFFFFE
FFFFFC
……
000002
000000

8 MB
8-bit

D7~D0

- **32-bit**



FFFFFF
FFFFFB
……
000007
000003

8 MB
8-bit

D31~D24

FFFFFE
FFFFFA
……
000006
000002

8 MB
8-bit

D23~D15

FFFFFD
FFFFF9
……
000005
000001

8 MB
8-bit

D15~D8

FFFFFC
FFFFF8
……
000004
000000

8 MB
8-bit

D7~D0

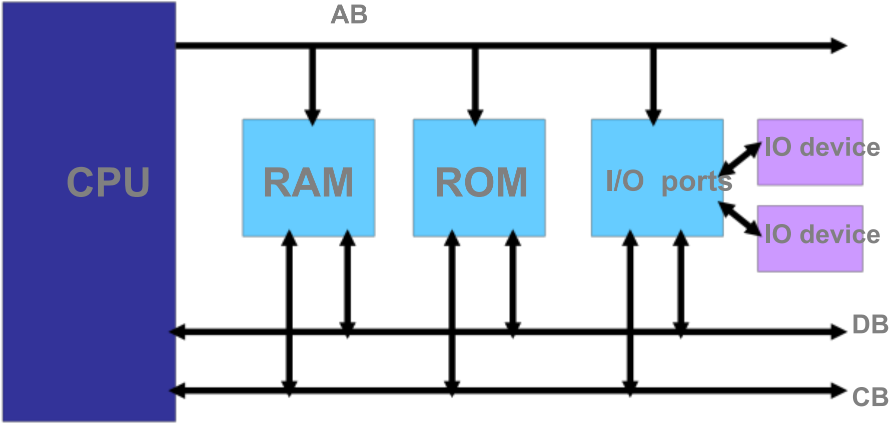
Hardware: Bus

- **A bus is a communication pathway connecting two or more devices**
  - A **shared** transmission medium: so one device at a time
  - **System bus:** connects major computer components (processor, memory, I/O)
  - ***Arbitration, 仲裁？***
    - Distributed protocols 访问的权限相同.
      - e.g., CSMA/CD in Ethernet
    - Centralized scheme: 有主从关系
      - Master/Slave
        - » Master activates a bus
        - » Slave passively waits for the Master's commands

Hardware: Bus

- **Type**
  - Dedicated (e.g., physical dedication)/Multiplexed (e.g., time multiplexing)
- **Arbitration**
  - Centralized: *bus controller* responsible for allocating time on a bus
  - Distributed: each module has access control logic and collaborate
- **Timing**
  - Synchronous: events on the bus is determined by a global clock, a single 1-0 transmission is referred to as a *bus cycle*
  - Asynchronous: devices have their own clocks and communicate before and after an event

Single-bus Structure

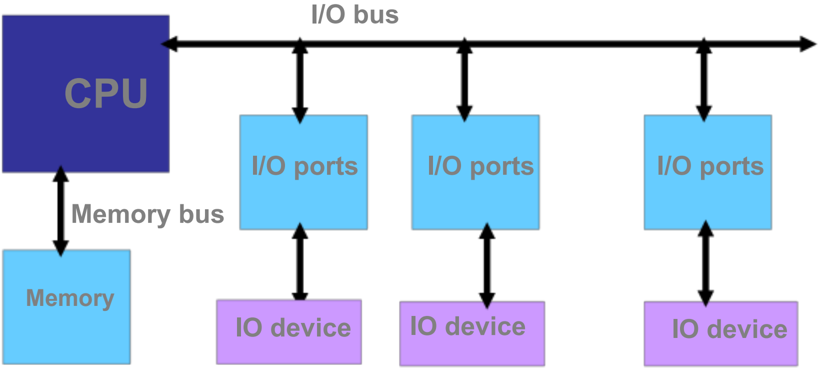


A bus connects all modules

- pro： simple
- con： poor performance in terms of throughput 吞吐量

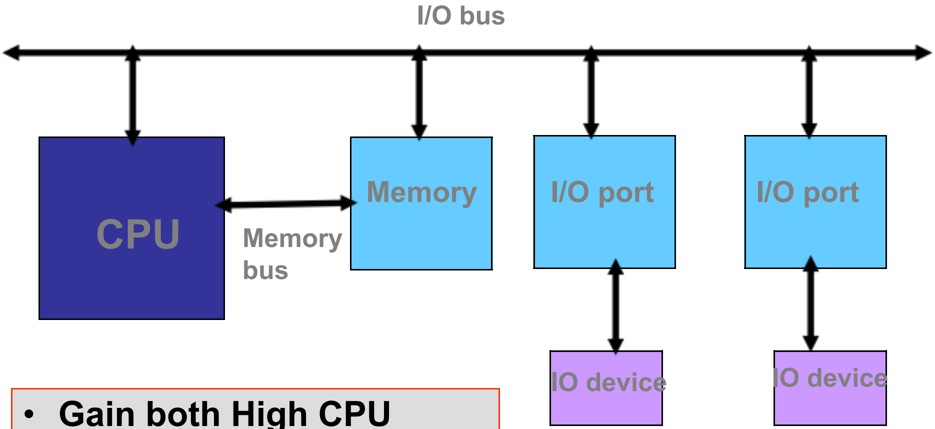
Why

CPU-Central Dual-Bus Structure



- A dedicated bus between CPU and memory, and a dedicated bus between CPU and I/O devices
- pro： efficient in terms of data transfer
- con： information between memory and I/O devices has to go through CPU. Therefore, poor CPU performance

Memory-Central Dual-Bus Structure



- Gain both High CPU performance and data transfer throughput

Hardware: BUS (1) – Data Bus

- Used to provide a path for moving data between system modules
- Bidirectional
  - CPU **read**: Memory (I/O device) -> CPU
  - CPU **write**: CPU -> Memory (I/O device)
- The width of data bus
  - is as wide as the registers of a CPU (i.e. the width of a ***word***)
  - determines how much data the processor can read or write in one memory or I/O cycle
  - Which also defines a **word** of this computer

Hardware: BUS (2) - Address Bus

- Used to designate the source or destination of the data on the address bus that the processor intends to communicate with
- Unidirectional 单向的
  - CPU → memory or I/O devices
- The width of the address bus, *n*
  - determines the total number of memory locations addressable by a given CPU, which is **2*n***
  - *e.g.*, 8086 has a 20-bit address bus which corresponds to 220 addresses or 1M (1 Meg) addresses or memory locations;
  - *Pentium has 32-bit address bus, what is the size of its addressable memory?*
  - *How to calculate the capacity (size) of memory that a CPU can support then?*

Hardware: BUS (3) – Control Bus

- Used to control each module and the use of data and address buses
  - Command and timing information between modules
  - e.g., memory read/write, IO read/write, Bus request/grant
- Consists of two sets of unidirectional control signals
  - Command signal: CPU → Memory (I/O device)
  - State signal: Memory (I/O device) → CPU
- Input/Output is defined from the processor's point of view
  - e.g., when Memory (I/O device) Read is active, data is input to the processor

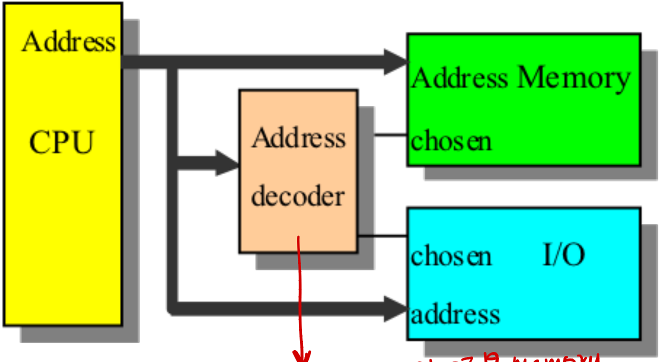
Addressing Schemes 寻址方式

- **Memory-mapped I/O, 存储器映像寻址方式**
  - One single address space for both memory and I/O
  - Status and data registers of I/O modules are treated as memory locations I/O与memory不分开
  - Using the same machine instructions to access both
  - e.g., ARM 用address decoder区分.

- **Isolated I/O, I/O单独编址方式**
  - Two separate address spaces for memory and I/O modules
  - Using different sets of accessing instructions
  - e.g., Intel 8086

Memory-mapped I/O

↑ 只需要一套指令.

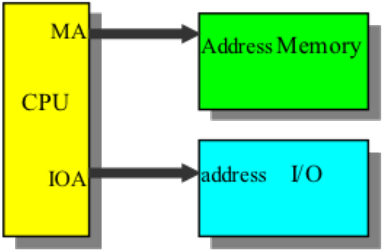


分析是访问 I/O 还是 memory.

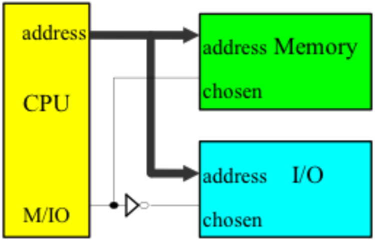
Isolated I/O

用两套指令，一套用于memory，一套用于I/O

8086



Dedicated address lines



better

Multiplexing address lines

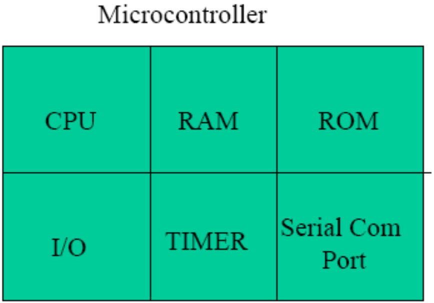
What is the essential difference between the memory-mapped and isolated I/O addressing schemes?

CPU是否知道指令的地址是 memory 还是 I/O.

Microcontrollers (MCS) 微控制器

A microcontroller has a CPU in addition to a fixed amount of RAM, ROM, I/O ports on one single chip

- Ideal for applications in which cost and space are critical
- Example: a TV remote control does not need the computing power of a 486



Microcontroller

CPU	RAM	ROM
I/O	TIMER	Serial Com Port

Embedded Systems 嵌入式系统

- An embedded system uses a ***microcontroller*** or a ***microprocessor*** to do one task and one task only
  - Example: toys, TV remote, keyless entry, etc.
- Using microcontrollers is cheap but sometimes inadequate for the task
- Microcontrollers differ in terms of their RAM,ROM, I/O sizes and type.
  - ROM (often used as program memory, like BIOS)
    - OTP (One Time-Programmable)
    - UV-ROM, EEPROM
    - Flash memory
  - RAM (can be used as both program mem and data mem)
    - SRAM(static RAM):cache
    - DRAM(Dynamic RAM): main memory
      - SDRAM (Synchrous DRAM)
      - DDR DRAM (Double Data Rate DRAM)
      - DDRII

Assignment One

- Go Jbox/Canvas site and download the Assignment One
  - https://jbox.sjtu.edu.cn/l/5odWhf (Password:EI209)
  - https://oc.sjtu.edu.cn
- Due on March 4.