计算机系统结构 CS2305

- QQ群号：

- 课程canvas主页:
  - https://oc.sjtu.edu.cn/courses/40743
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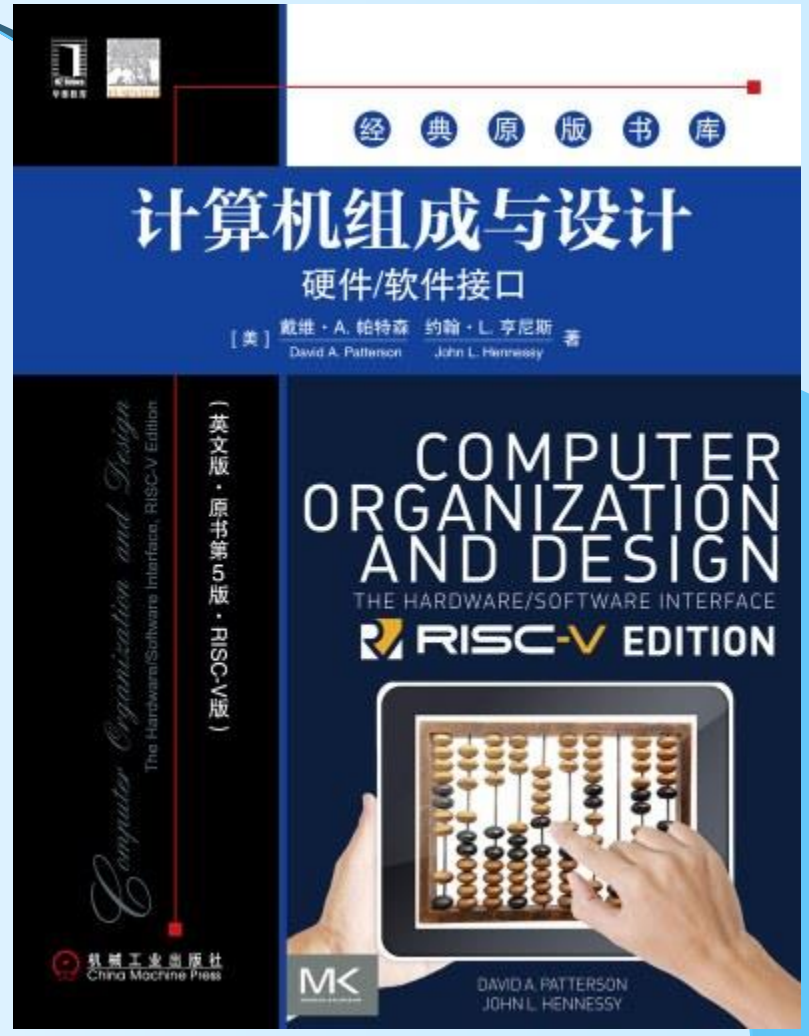
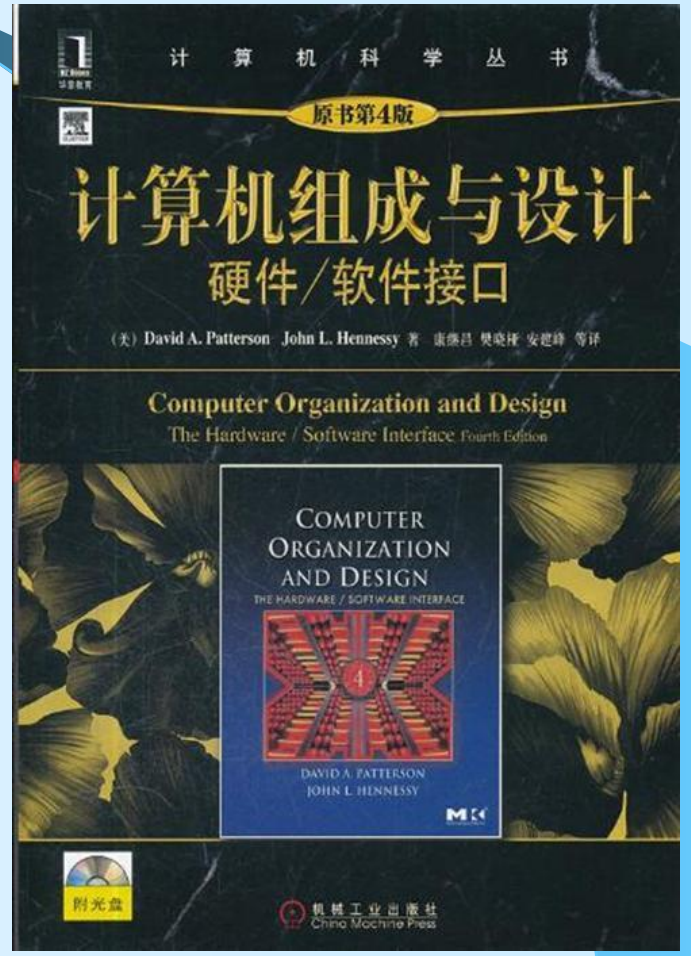
教材

- David A. Patterson, John L.Hennessy. Computer Organization & Design: A Hardware/Software Interface, RISC-V edition. 计算机组成与设计：硬件/软件接口（第5版），机械工业出版社 。



教材：： why both？

- David A. Patterson, John L.Hennessy.
  Computer Organization & Design: A Hardware/Software Interface，4th edition. 计算机组成与设计：硬件/软件接口（第4版,MIPS版），机械工业出版社。



本节纲要

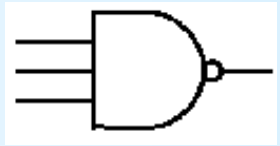
- 什么是计算机系统结构?
- 计算机系统结构中最重要的思想
- 本课程内容及评分标准

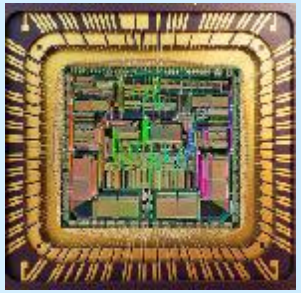
什么是Architecture ？

- **Architecture**
  - **Science and art of interconnecting building materials to construct various buildings, subject to constraints**
  - **– Materials: brick, concrete, glass, etc.**
  - **– Buildings: house, office, auditorium, etc.**
  - **– Constraints: cost, safety, time, etc.**

什么是计算机系统结构

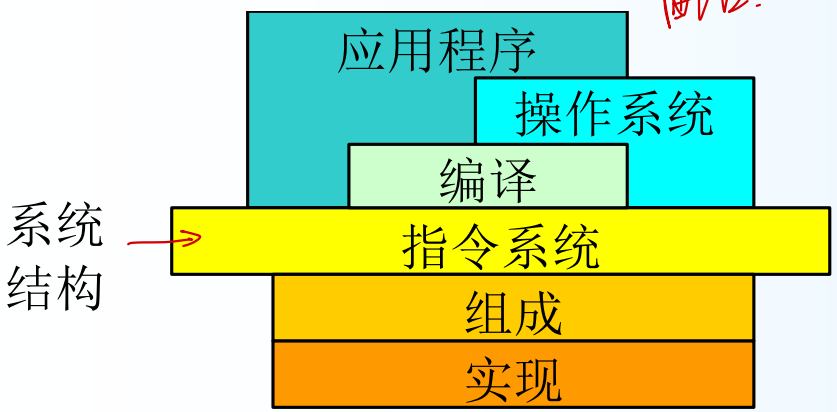
- **Computer Architecture**
  - Science and art of interconnecting hardware components to create computers, subject to constraints
  - – Hardware components: circuits, gates, chips, etc.
  - – Computers: desktop, server, mobile phone, etc.
  - – Constraints: performance, energy, cost, etc.



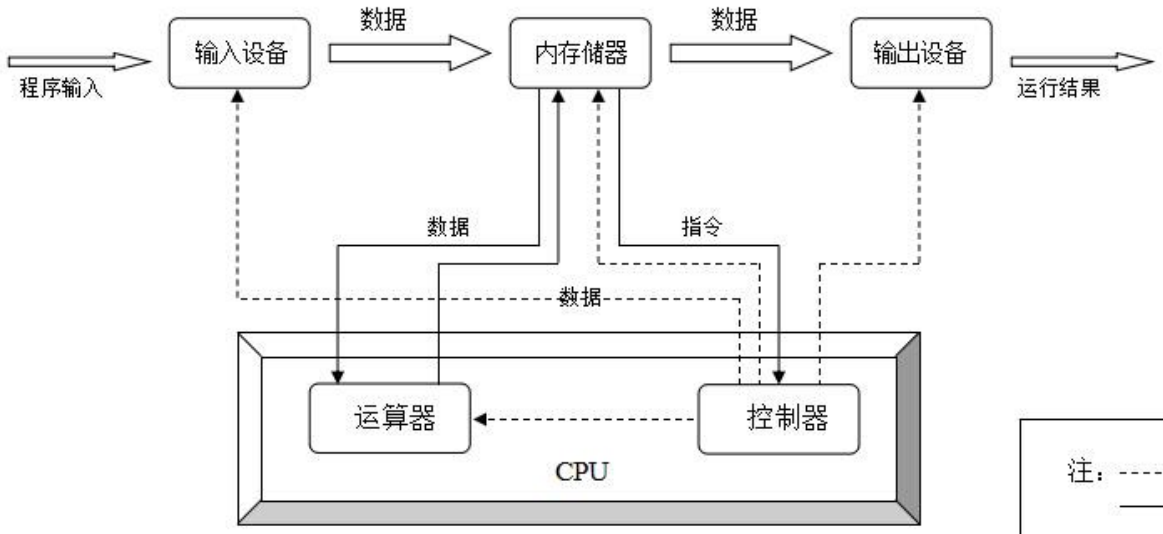


系统结构、组成的区别与联系

- 计算机体系结构：系统程序员所看到的计算机的属性
- 计算机组成：是系统结构的具体实现、是Micro-Architecture



- 计算机组成的五个部分：
  - CPU：控制器，运算器，
  - 存储器
  - 输入设备/输出设备



计算机的工作原理示意图

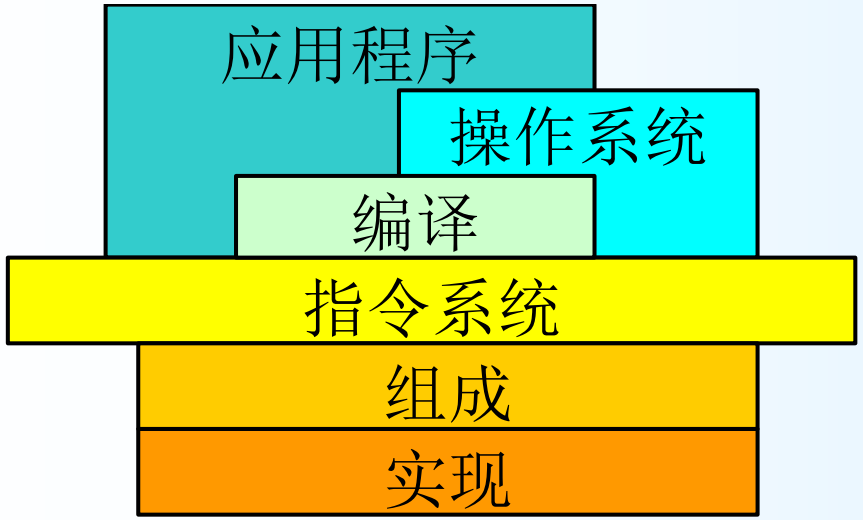
系统结构的研究范围

- 外特性 → 指令集
  - 指令系统
  - 数据表示
  - 寻址方式
  - 寄存器集
- 界面设计
  - 确定硬件功能

- 新型系统结构设计
  - 并行性
  - 数据流
  - 张量处理单元（TPU）
  - 神经网
- 性能成本评价
  - 运算速度
  - 存储容量
  - I/O带宽

“广义”的计算机系统结构

系统结构



Application Requirements:
Suggest how to improve architecture

Architecture provides feedback to guide application and technology research directions

Technology Constraints:
- **Restrict what can be done efficiently**
- **New technologies make new arch possible**

技术影响体系结构

1970s

- Multi-Chip CPUs
- Memory very expensive
- Complex instruction sets(good density)
- Microcoded control

1980s

- 5k- 500k transistiors
- Single-chip, pipelined CPU
- simple hardwire control
- simple instruction sets
- Small on-chip caches

1990s

复杂指令集

- 1M-64M transistiors
- Complex control to exploit instruction level parallelism
- Deep pipeline
- Multi-level caches

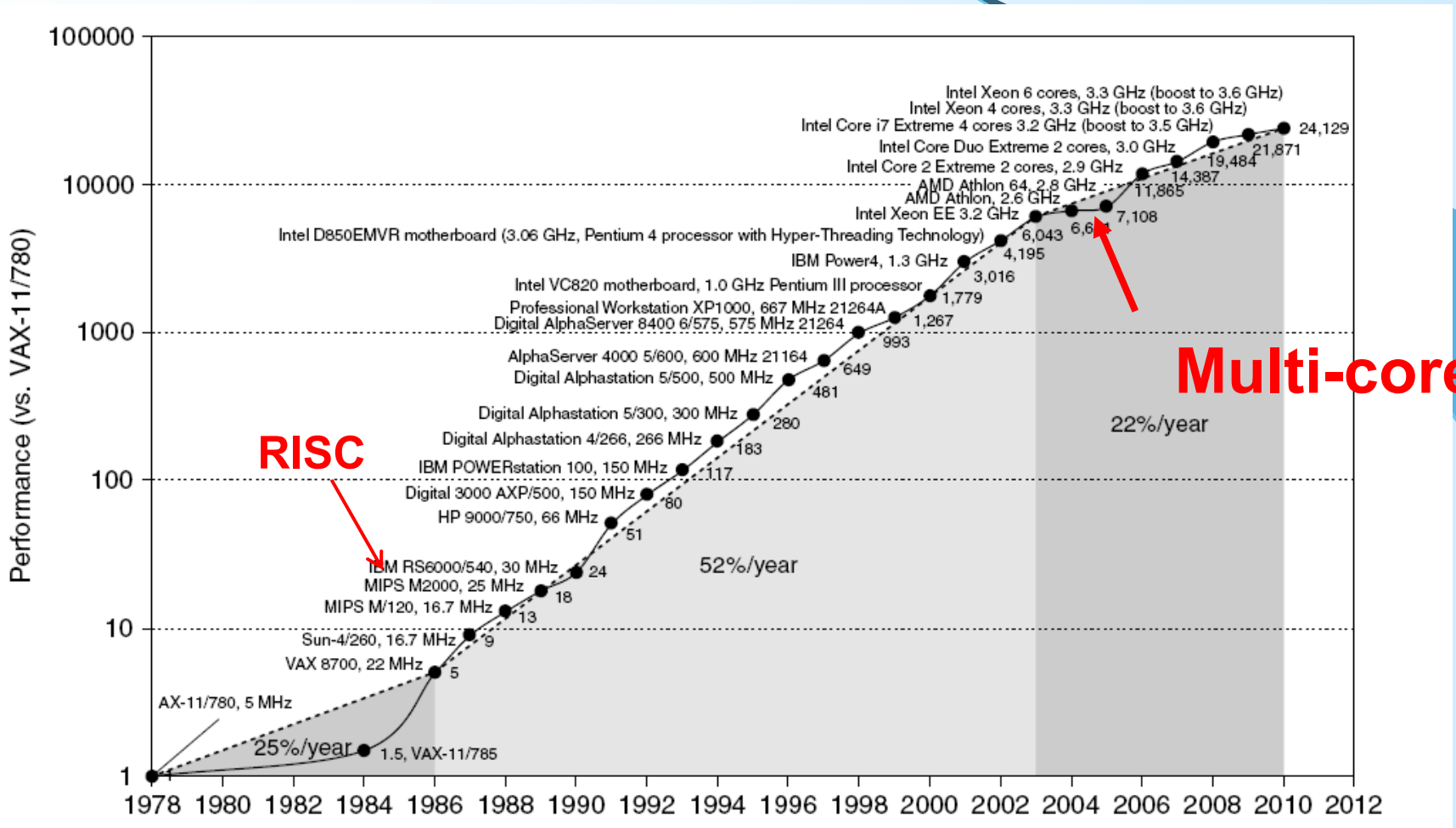
2000s

单核→多核

- 100M- 5B transistiors
- Slow wires, power consumption, design complexity, memory latency..
- Multi-core, heterogeneous systems
- Support for parallelism 异构

体系结构的变化对性能的影响

摩尔定律



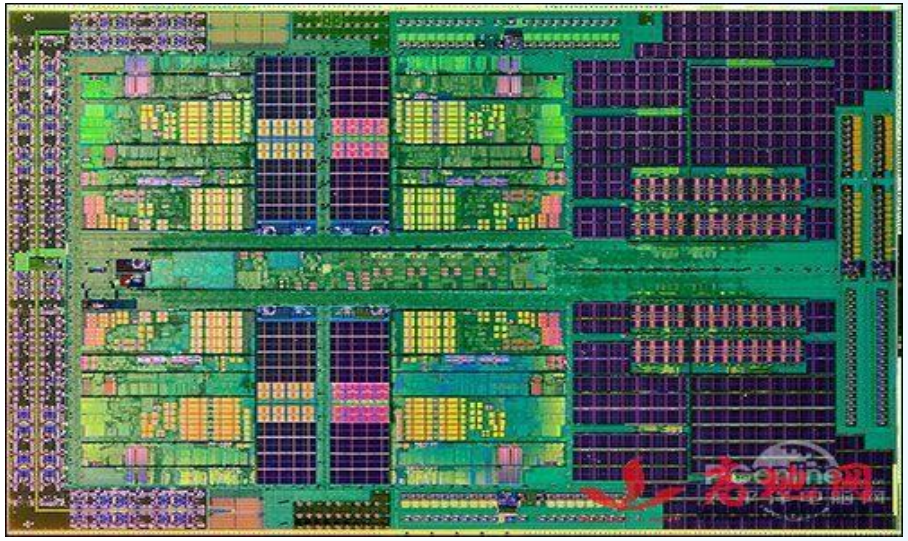
不同的应用类型对性能的要求

- **Personal Mobile Device (PMD)**
  - e.g. start phones, tablet computers
  - Emphasis on energy efficiency（能效比） and real-time（实时性）
- **Desktop Computing**
  - Emphasis on price-performance（性价比）
- **Servers** 服务器
  - Emphasis on availability（可用性）, scalability（可扩展性）, throughput（吞吐率）
- **Clusters / Warehouse Scale Computers**
  - Used for “Software as a Service (SaaS)”
  - Emphasis on availability（可用性） and price-performance
  - Sub-class: Supercomputers, emphasis: floating-point performance and fast internal networks
- **Embedded Computers**
  - Emphasis: price（价格、体积）

面向不同应用的同一种体系结构

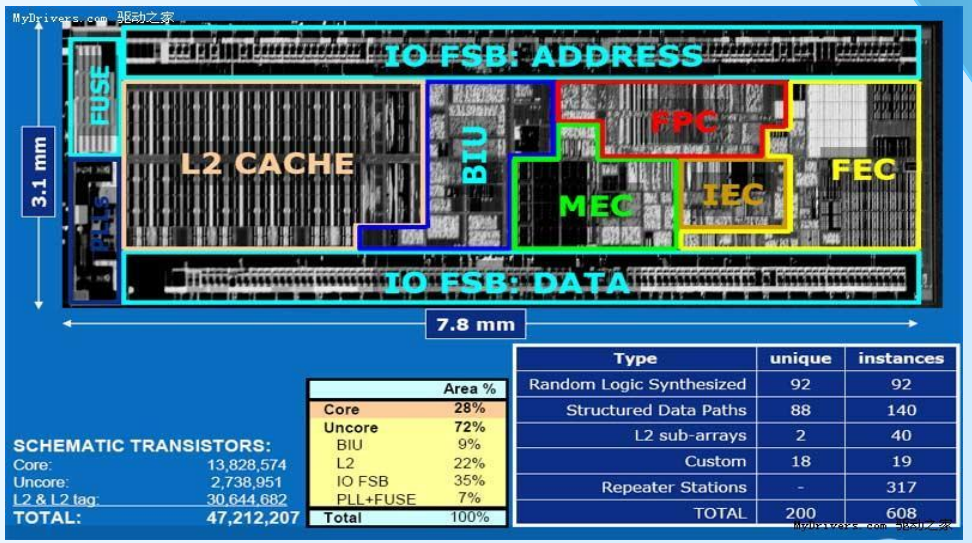
AMD Phenom II X4 945

- X86 Instruction Set
- Quad Core, 125W
- Decode 3 Instructions/Cycle/Core
- 64KB L1 I Cache, 64KB L1 D Cache
- 512KB L2 Cache
- Out of order
- 2.6GHz



Intel Atom

- X86 Instruction Set
  Single Core, •2W
- Decode 2 instructions/Cycle/Core
- 32KB L1 I Cache, 24KB L1 D Cache
- 512KB L2 Cache
- In order
- 1.6GHz



技术影响体系结构：ARM的演化

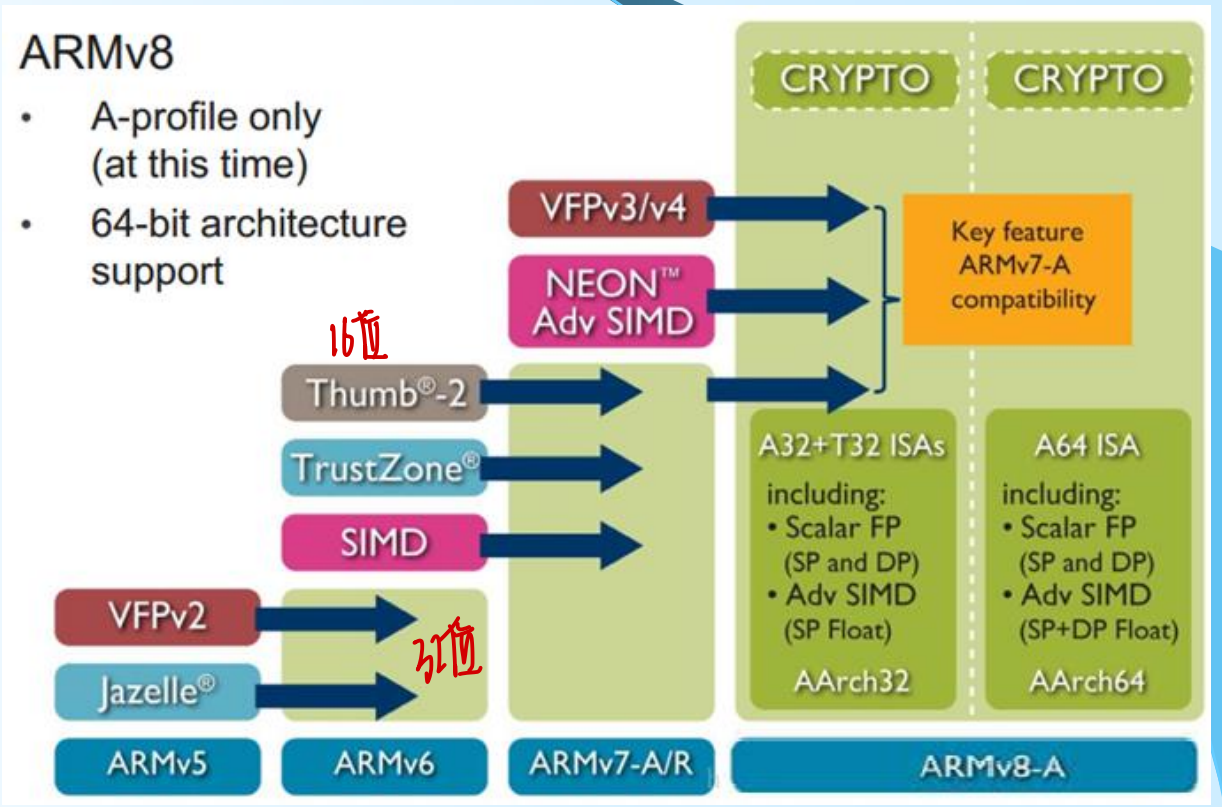
Armv体系结构的减法和加法

举例：条件执行指令：

```
if (i > j)
        i -= j;
else    j -= i;
```

```
CMP Ri ,  Rj
SUBGT Ri, Ri, Rj ;
SUBLT  Rj, Rj, Ri ;
// ARM V8 取消了很多这样的指令
```

只有1条成功写入

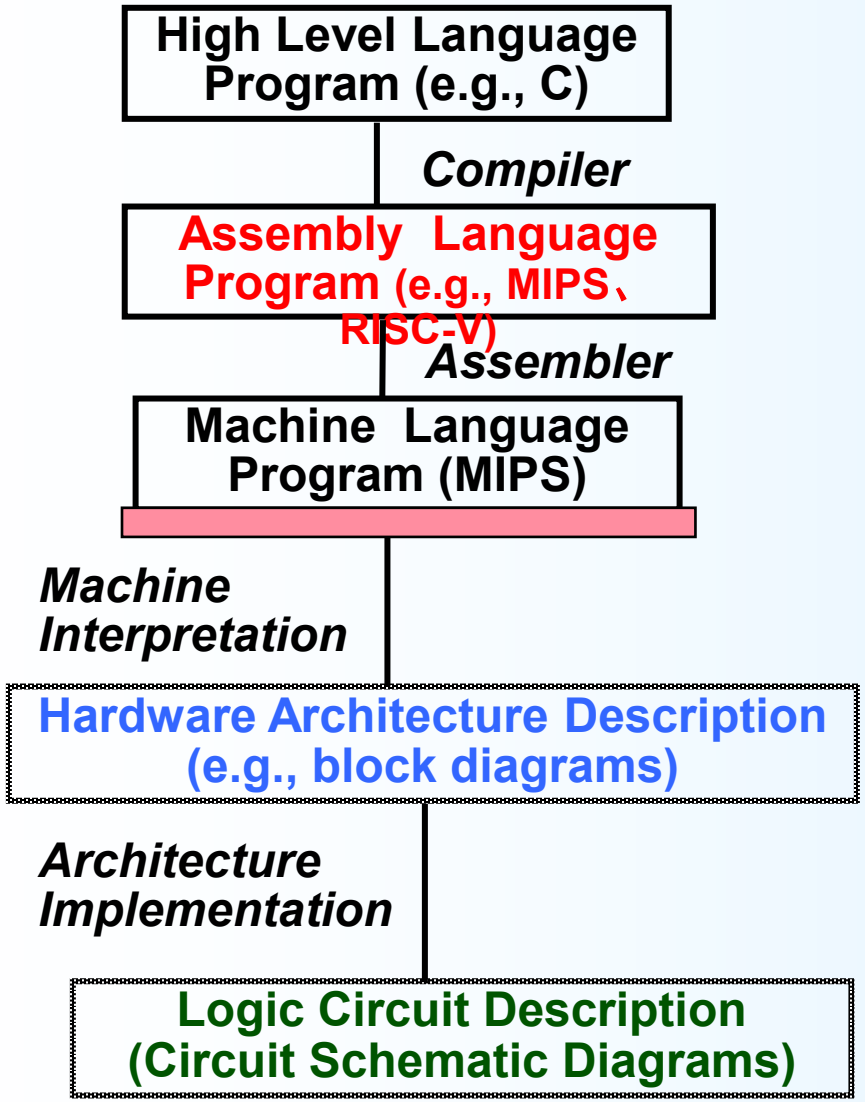


图片来源： ARM v8 白皮书

计算机体系结构中一些重要思想

- Abstraction (Layers of Representation/Interpretation)
- Moore's Law
- Principle of Locality/Memory Hierarchy
- Parallelism
- Dependability via Redundancy

Great Idea： 不同层次的抽象

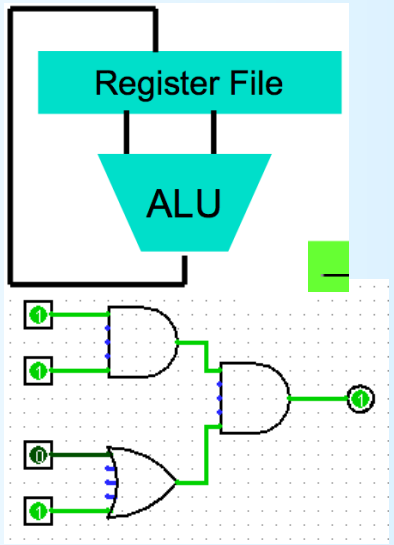



```
temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;
```

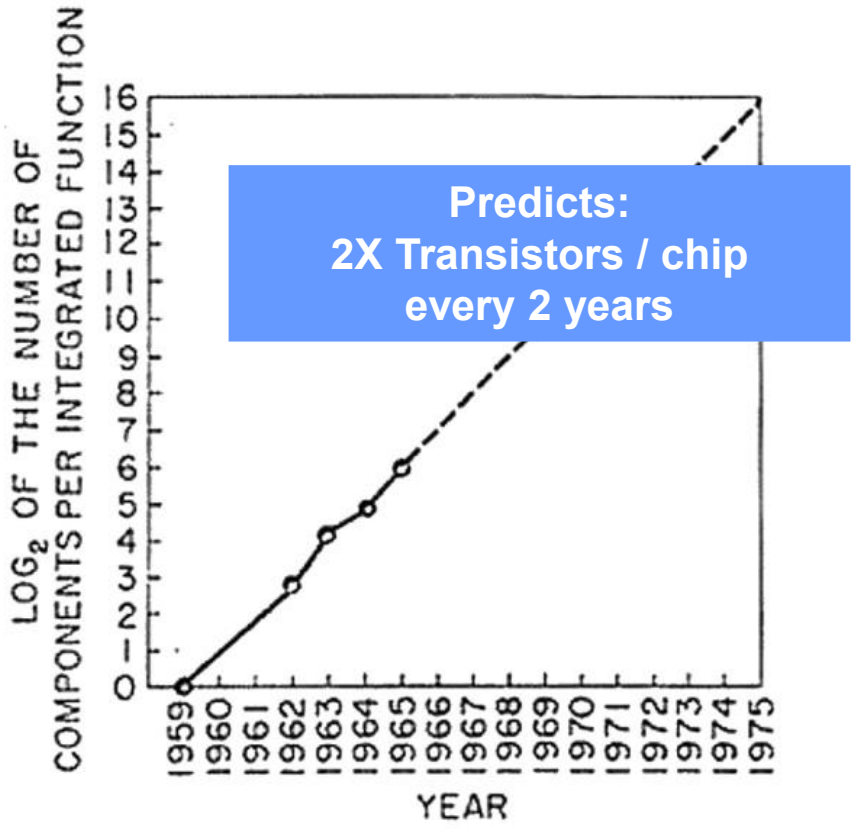
```
lw   $t0, 0($2)
lw   $t1, 4($2)
sw   $t1, 0($2)
sw   $t0, 4($2)
```

Anything can be represented as a *number*, i.e., data or instructions

```
0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111
```



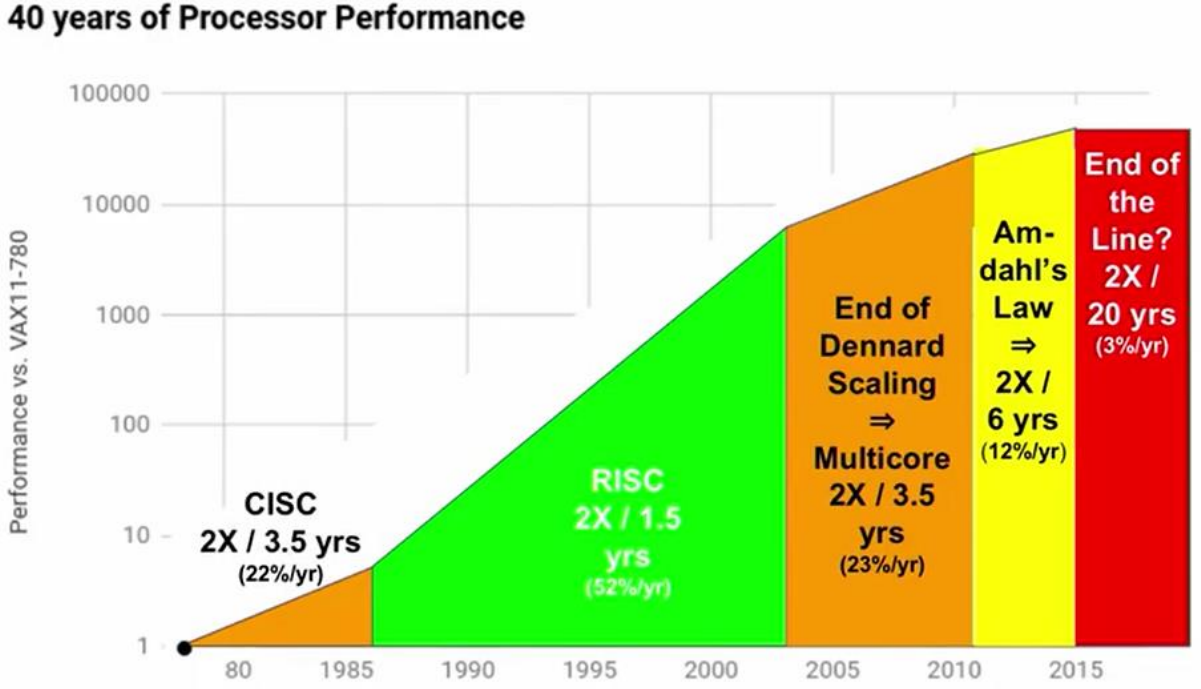
Great Idea : Moore's Law



Predicts:
2X Transistors / chip
every 2 years

Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.

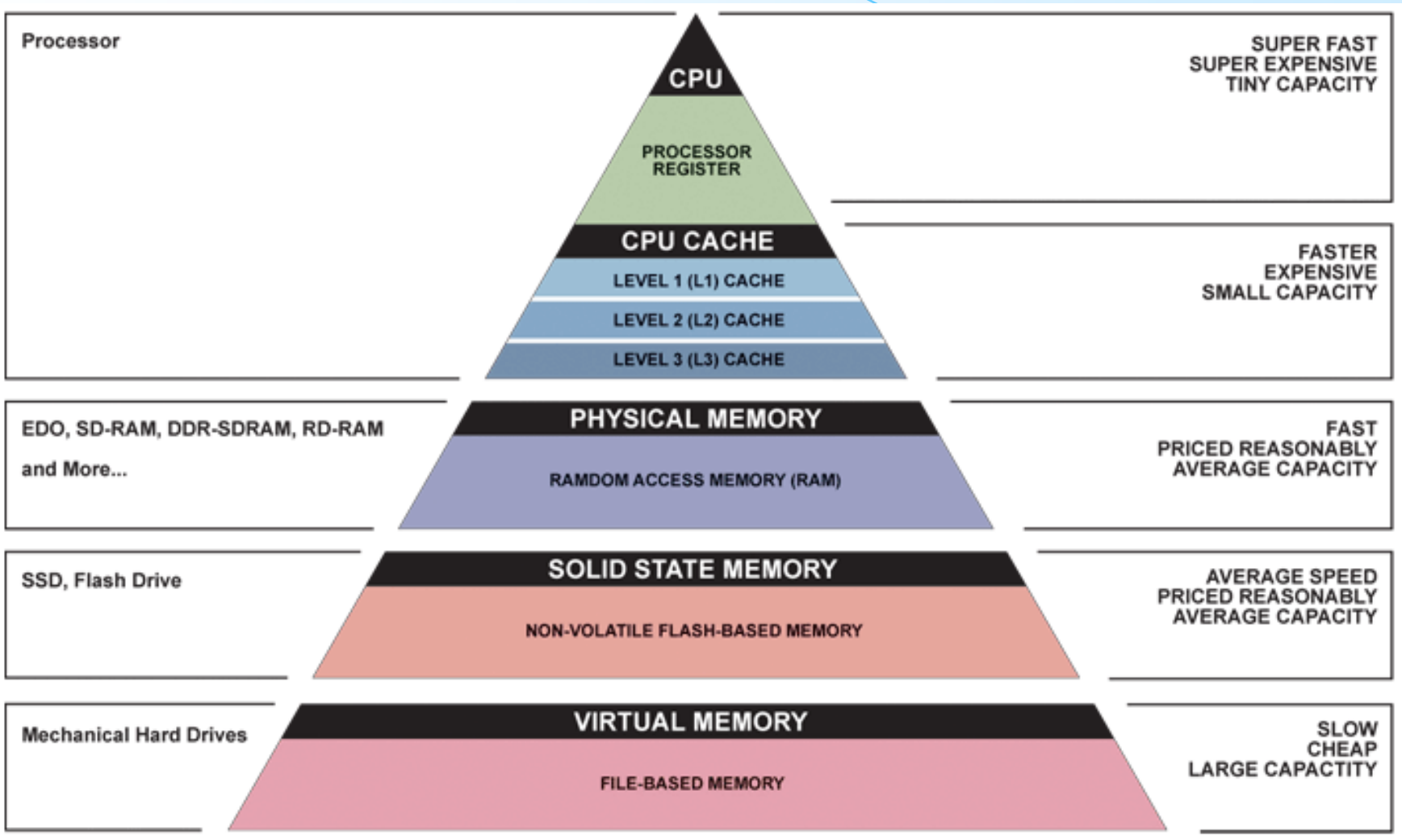
End of Growth of Single Program Speed?



Based on SPECintCPU. Source: John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e. 2018

Apple A12 single thread performance (RISC ISA) = x86 Skylake single thread perf (SPEC), at much lower power, *Anandtech* 10/8/18

Great Idea： Principle of Locality / Memory Hierarchy



Great Idea #4:Parallelism

Software

- Parallel Requests
  Assigned to computer
  e.g., Search "cats"
- Parallel Threads
  Assigned to core
  e.g., Lookup, Ads
- Parallel Instructions
  >1 instruction @ one time
  e.g., 5 pipelined instructions
- Parallel Data
  >1 data item @ one time
  e.g., Add of 4 pairs of words
- Hardware descriptions
  All gates functioning in parallel at same time

Harness Parallelism & Achieve High Performance

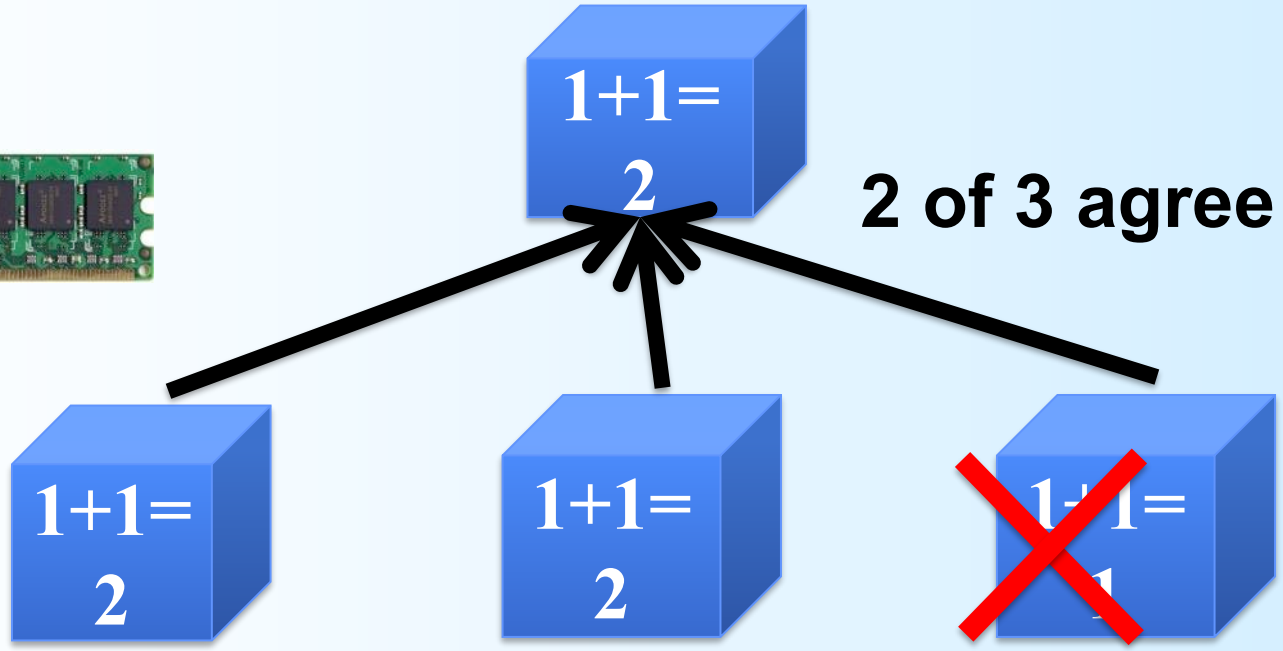
Hardware

Warehouse -Scale Computer

Smart Phone

Great Idea #5: Dependability via Redundancy

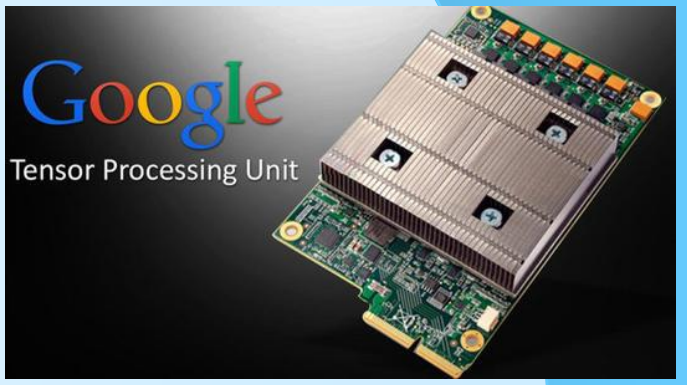
冗余性



Increasing transistor density reduces the cost of redundancy

计算机系统结构的发展趋势

- Open-source hardware: RISC-V
- Very complex processor designs
- Parallelism at the chip level
- Power-conscious designs
- Specialization: domain-specific processors
- Security



本课程内容

- 计算机系统性能指标
- 数据的表示和运算
- 指令系统
  - CISC和RISC
  - MIPS、RISC-V指令系统
  - 对比X86-64指令系统
- 存储器层次结构
- 中央处理器(CPU)
  - 数据通路
  - 控制器的功能和
  - 指令流水线的原理
  - 超标量和动态流水线
- 并行和异构处理
  - 多核、多线程
  - GPU

评分标准

- 课堂参与 10 %
- 线上成绩 10 % 中国大学MOOC 计算机组成与系统结构 上海交通大学
- 作业 30%
  - 3次书面作业
    - 数的表示与运算
    - 存储层次结构
    - 流水线与超标量处理器
  - 3次编程作业：指令系统、cache及性能优化、 并行编程
- 期终考试 Final Exam 50 %

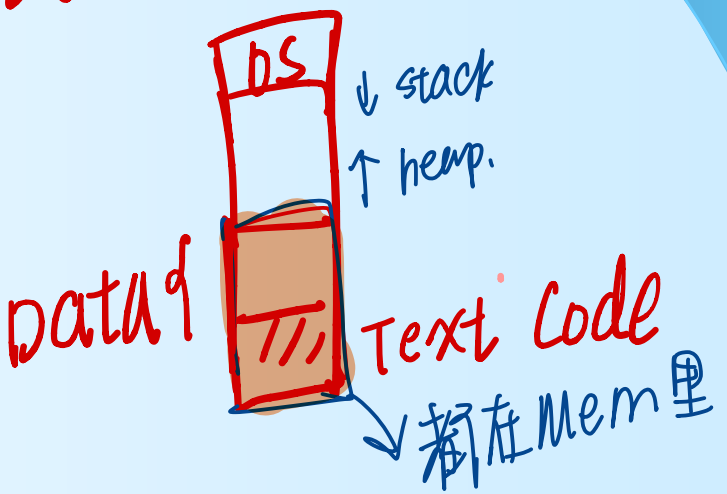
课堂提问

☆☆

* 1. 冯诺伊曼计算机中，CPU区分从存储器取出的是指令还是数据的依据是：

* 2. 冯诺伊曼计算机的工作方式的基本特点是 → stored program（程序与数据同等地位，存储在memory里）

☆ ☆☆



```
int i
if(i>0)  i*i>0
```
永真 X

```
float f
if(f>0)  f*f>0
```
为真 V

```
for(i=0; i<N; i++)
    sum += a[0][i]
for(i=0; j<N; i++)
    sum += a[i][0]
```
数据连续存储.

总结：系统结构的研究范围

- 外特性
  - 指令系统
  - 数据表示
  - 寻址方式
  - 寄存器集
- 界面设计
  - 确定硬件功能

- 新型系统结构设计
  - 并行性
  - 图形处理单元（GPU）
  - 张量处理单元（TPU）
  - 神经网络加速单元
- 性能成本评价
  - 运算速度
  - 存储容量
  - I/O带宽