3. Consider a system using multilevel paging scheme. The page size is 1 MB. The memory is byte addressable and virtual address is 64 bits long. The page table entry size is 4 bytes.
   1) How many levels of page table will be required?
   2) Please give the structures of physical address and virtual address.

1) 1页有 $\frac{1MB}{4B} = 2^{18}$ 项 PTE

由于 VA = 64 bits，1页的页偏移有 20 bit，故页地址有 64−20 = 44 bits.

虚拟地址中有 2^{44} 页.

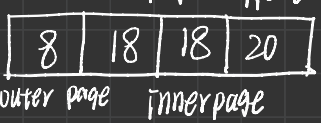
故有 $\frac{2^{44}}{2^{18}} = 2^{26}$ 页 inner table.

有 $\frac{2^{26}}{2^{18}} = 2^{8}$ 页 (outer page)

有 $\lceil \frac{2^{8}}{2^{18}} \rceil$ = 1页 2nd outer page

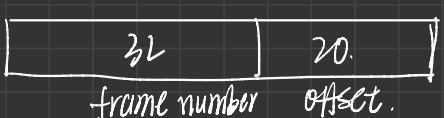
故有3个level.

2) virtual address:



由于 1个 PTE = 4B = 32 bit. number of frams = 2^{32}

有 frame = page. 故偏移有20位. 余下有 32 bits 的帧号.



① int Ben = Jerry = 0

② spoon mutex = pen mutex = 1

Ben mutex = Jerry mutex = 1

Speed = 5

Ben:

```
If (Ben<w)
} wait (Ben mutex)
  Ben++
  wait (sm)
  // taste
  signal (sm)

  wait (Speed)

  wait (PM)
  // sign
  signal (PM)
  signal (Ben mutex)

}
```