Ve373 Microprocessor Based System Design
Lab 5. Voltmeter – ADC Application

OBJECTIVE

- Implement a simple voltmeter with the PIC32 microcontroller.
- Understand the configuration of relevant peripheral modules
- Improve lab skills in building microprocessor based circuit

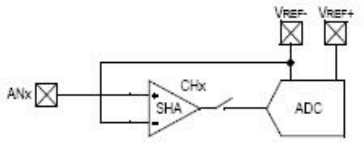
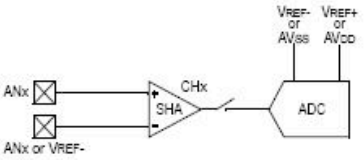
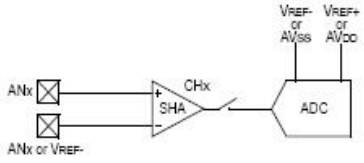
PROJECT DESCRIPTION

In this lab, you are asked to build a voltmeter that measures analog voltage signal in the range of 0 ~ 3.3 Volts with sample rate of 500Hz. The measured result should be displayed on the LCD module built in the previous lab once the analog voltage signal is applied. The result should be displayed to the second digit after the decimal point.

HARDWARE DEVELOPMENT AND SAFETY

You are required to use the PIC32 Ethernet Starter Kit, PIC32 I/O Expansion board, and other electronic parts if necessary to implement the application. You will configure the ADC module to acquire and convert the input analog signal. The ADC module may be configured in any operation mode as long as the required functionality is achieved. Make sure the SYSCLK, PBCLK and T_{AD} is configured to meet the minimum timing requirements suggested by the following figures.

TABLE 31-37: 10-BIT CONVERSION RATE PARAMETERS

PIC32MX 10-bit A/D Converter Conversion Rates(2)						
ADC Speed	**TAD Minimum**	**Sampling Time Min**	**Rs Max**	**VDD**	**Temperature**	**ADC Channels Configuration**
1 Msps to 400 ksps(1)	65 ns	132 ns	500Ω	3.0V to 3.6V	-40°C to +85°C	
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	-40°C to +85°C	
Up to 300 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	-40°C to +85°C	

Note: CPIN value depends on device package and is not tested. Effect of CPIN negligible if Rs ≤ 5 kΩ.

The input analog voltage MUST NOT be out of the specified range. Otherwise, damages may be caused to the board. Consult with the following electronic characteristics (from DS61156D – PIC32MX Data Sheet) before testing your system.

TABLE 31-36: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module Vss Supply	Vss	—	Vss + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.0	—	AVDD	V	**(Note 1)**
AD05a			2.5	—	3.6	V	VREFH = AVDD **(Note 3)**
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	**(Note 1)**
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	**(Note 3)**
AD08	IREF	Current Drain	—	250 —	400 3	µA µA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
		Leakage Current	—	+/- 0.001	+/-0.610	µA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10 kΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5K	Ω	**(Note 1)**

DELIVERABLES

One submission is required for each team and should be submitted electronically by one of the team members. Make sure names of all team members are clearly shown in the file. Each submission should include:

1. Lab report, including a brief discussion of the lab, software development work (such as algorithms, pseudo code, flow charts, etc.), answers to questions if asked in the lab manual, test plan, test results, as well as all your source codes.
2. Evaluation report, each student should also submit an evaluation to describing your own contribution to the lab and to evaluate the performance of every other team member.
3. Zipped working directory for your project
4. Any other related documents

A team must successfully demonstrate their lab results to receive full credits.

GRADING

Total points: 200 points. The lab will be graded as follows:

Lab Report and Evaluation	20%
Executable program	20%
Demonstration	30%
Completion	20%
Individual Performance	10%

DUE DATE

The lab should be demonstrated to the TAs before your lab session is over.

The lab report and evaluation report is due by **noon of July 9, 2017**.