

Instructions

Before starting the exam, read carefully the following information:

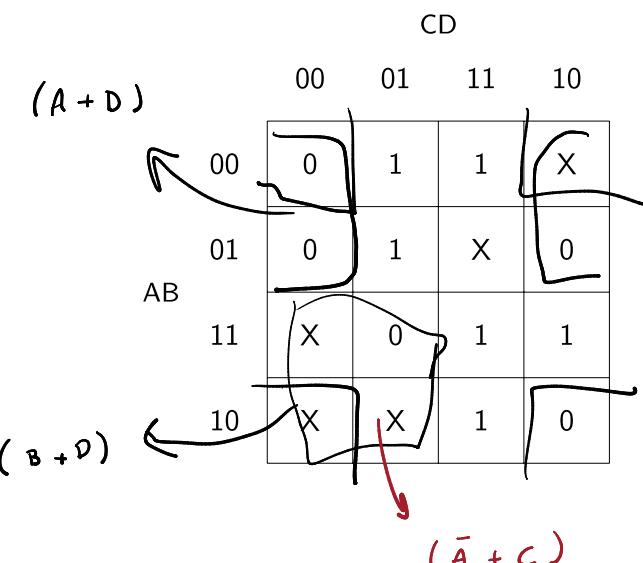
- There are (at least) nine different versions of this exam.
- Although the exam comprises a total of 16 pages, there are two distinct volumes that should be handled as follows:
 - **Volume 1** corresponds to the question list and comprises pages 1 to 13. These pages do not need to be identified because they will be discarded at the end of the exam;
 - **Volume 2** corresponds to the answers sheet and comprises pages 13 to 16. All pages of this volume **MUST** be identified with the **student's name** and **number**.
 - At the end of the exam, all pages of **Volume 2** will be separated. Consequently, all non-identified pages will not be considered.
- The exam is composed of three parts (Part I, II and III) and has a duration of 2 (two) hours.
 - **Part I** comprises N_1 multiple choice questions and awards a total of $P_1 = 15$ points.
 - * Each correct answer awards $C = P_1/N_1$ points;
 - * Each wrong answer awards $W = -C/(A-1)$ points (negative value), where A denotes the number of possible answers offered to each question;
 - * Each non-answered question awards 0 points.
 - **Part II** comprises an open-answer problem about combinatorial circuits and awards a total of $P_2 = 2.5$ points.
 - **Part III** comprises an open-answer problem about sequential circuits and awards a total of $P_3 = 2.5$ points.
 - All question answers **MUST** be replied in the allotted space of **Volume 2**.
- At the end of **Part I of Volume 1** you will find an empty page - you can use it for auxiliary calculations, but this page will not be delivered at the end. This means that all answers **MUST** be replied (and properly justified) in the allotted space of **Volume 2**.
- Each question includes a Portuguese translation of the corresponding text. In case of a mismatch between the English text and its translation, the English text will be the one to be considered in the evaluation¹.
- You cannot use or consult any material during the exam. On your desk you can only have a pen and your student identity card.

¹Cada pergunta inclui uma tradução para Português do referido texto. Em caso de incoerência entre o texto em Inglês e a sua tradução, será o texto em Inglês que será considerado na avaliação.

Volume 1 - Part I

- A. Which of the following expressions corresponds to the minimal function represented in the Karnaugh-map?
 [Qual das seguintes expressões corresponde à função mínima representada no mapa de Karnaugh?]

- [1]: $(B + \bar{D})(A + C)(\bar{B} + C)$
- [2]: $(C + D)(\bar{A} + \underline{C})(\bar{B} + C)$
- [3]: $(C + D)(A + \bar{D})(\bar{A} + D)$
- [4]: $(B + \bar{D})(A + D)(\bar{B} + C)$
- [5]:** $(B + \underline{D})(\underline{A} + D)(\bar{A} + C)$
- [6]: None of the other options [Nenhuma das outras opções]



- B. Select the canonical conjunctive normal form (product of sums) of the function $(X + \bar{Z})(\bar{X} + \bar{Y})$ with three variables.

[Indique qual das seguintes expressões corresponde à forma canónica conjuntiva (produto de somas) da função $(X + \bar{Z})(\bar{X} + \bar{Y})$ com três variáveis.]

- [1]: $(\bar{X} + Y + \bar{Z})(X + \bar{Y} + Z)(\bar{X} + \bar{Y} + Z)(\bar{X} + \bar{Y} + \bar{Z})$
- [2]: $(X + Y + \bar{Z})(X + \bar{Y} + Z)(\bar{X} + \bar{Y} + Z)(\bar{X} + Y + Z)$
- [3]:** $(X + \bar{Y} + \bar{Z})(\bar{X} + \bar{Y} + Z)(\bar{X} + \bar{Y} + \bar{Z})(X + Y + \bar{Z})$
- [4]: $(X + \bar{Y} + \bar{Z})(X + \bar{Y} + Z)(\bar{X} + \bar{Y} + Z)(\bar{X} + \bar{Y} + \bar{Z})$
- [5]: $(\bar{X} + Y + \bar{Z})(X + \bar{Y} + \bar{Z})(\bar{X} + Y + Z)(\bar{X} + \bar{Y} + \bar{Z})$
- [6]: None of the other options [Nenhuma das outras opções]

$$\begin{aligned} x + \bar{z} &= (\underline{x} + y + \bar{z})(x + \bar{y} + \bar{z}) & \checkmark \\ \bar{x} + \bar{y} &= (\bar{x} + \bar{y} + \bar{z})(\bar{x} + \bar{y} + z) & \checkmark \\ && \checkmark \end{aligned}$$

- C. What is the 8-bit two's complement representation of -47 ?

[Qual é a representação em complemento para dois com 8-bits de -47 ?]

- [1]: 11010000
- [4]: 10101110

- [2]:** 11010001
- [5]:** 10101111

- [3]: 00101111
- [6]: None of the other options
 [Nenhuma das outras opções]

$$47_2 = 32 + 8 + 4 + 2 + 1$$

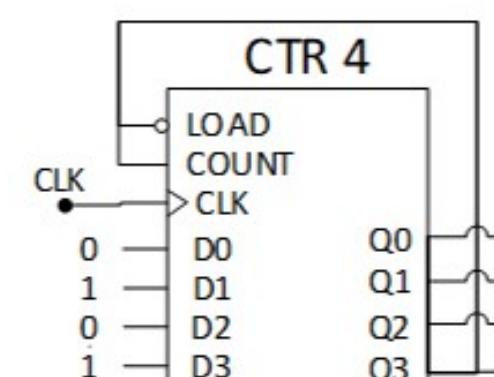
$\begin{smallmatrix} 0 & 0 & 1 & 0 & 1 & 1 & 1 & 1 \\ & & & & & & & \\ 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \end{smallmatrix}$	$\begin{smallmatrix} 1 & 1 & 0 & 0 \\ & & & \\ 1 & 1 & 0 & 1 \end{smallmatrix}$
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- D. Consider the following circuit with a 4-bit counter. The initial state of the circuit is $Q_3 Q_2 Q_1 Q_0 = 1011$. What are the next two states of the circuit?

[Considere o seguinte circuito com um contador de 4-bits. O estado inicial do circuito é $Q_3 Q_2 Q_1 Q_0 = 1011$. Quais serão os próximos dois estados do circuito?]

- [1]: 1010, 1011
- [2]: 1010, 0101
- [3]:** 1100, 1101
- [4]: 0100, 1010
- [5]: 1101, 1110
- [6]: None of the other options [Nenhuma das outras opções]

$$\begin{array}{c} 1011 \\ \left(\begin{array}{l} Q_3 = COUNT / LOAD \\ 1100 \\ 1101 \end{array} \right) \\ 1100 \\ 1101 \end{array}$$



E. Represent $D5_{16}$ in base 10.

[Represente $D5_{16}$ na base 10.]

[1]: 229
[4]: 181

[2]: 205
[5]: 213

[3]: 197
[6]: None of the other options
[Nenhuma das outras opções]

$$D5_{(16)} = \underbrace{1\ 1\ 0\ 1}_{13} \underbrace{0\ 1\ 0\ 1}_{05} (2)$$

$$\begin{aligned} &= 1 + 4 + 16 + 64 + 128 \\ &= 213_{(10)} \end{aligned}$$

F. Consider the following memory system. Compute the size (in number of bits, i.e., number of words \times number of bits per word) of the address space in which it is possible to write values.

[Considere o seguinte sistema de memória. Calcule a dimensão (número de bits, isto é, número de palavras \times número de bits por palavra) do espaço de endereçamento em que é possível escrever valores.]

[1]: 256×32

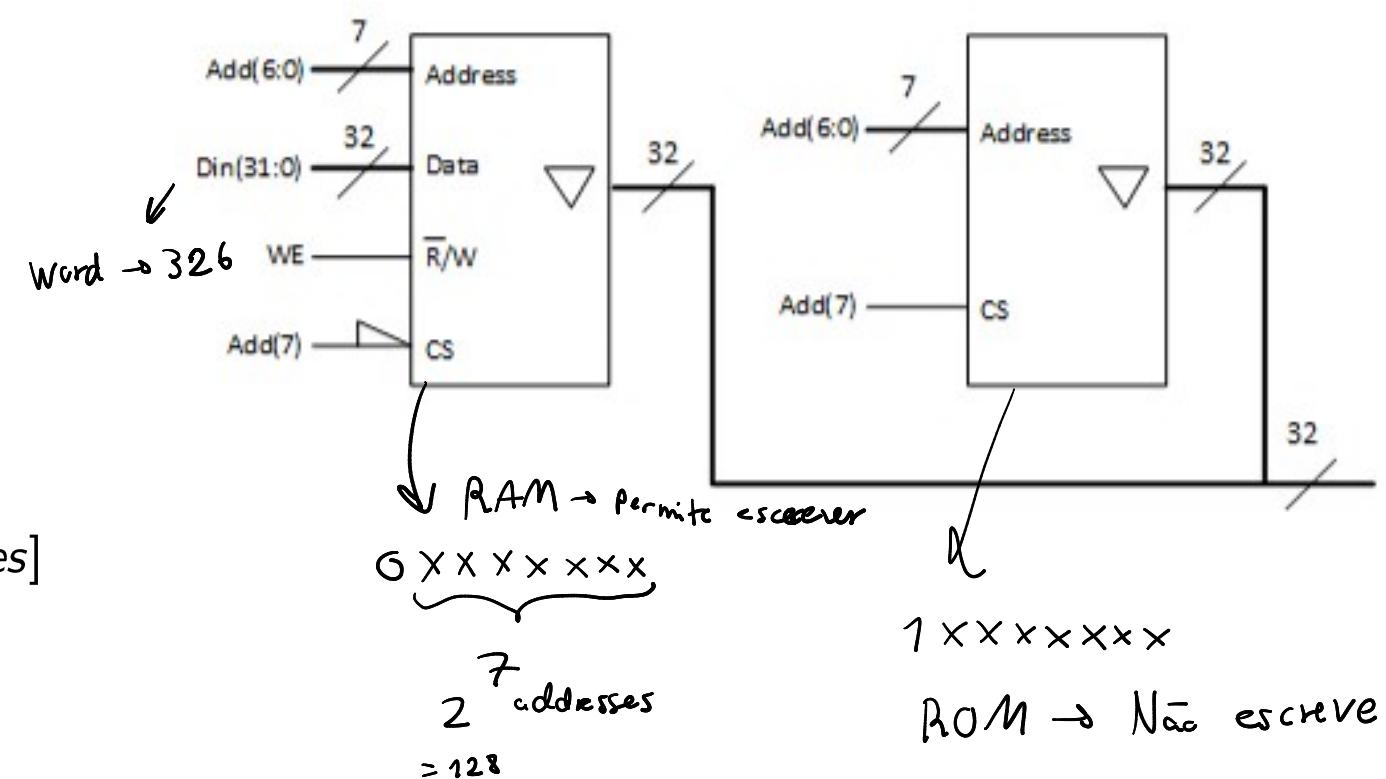
[2]: 128×32

[3]: 256×64

[4]: 64×32

[5]: 128×64

[6]: None of the other options
[Nenhuma das outras opções]



G. Consider the following state diagram with two inputs $X_1 X_0$ and where each state $S_i (i = 1, \dots, 8)$ is implemented with D flip-flops, with input D_i (next state) and output Q_i (current state). Select, only for the state S_3 , the correct option for D_3 as a function of X_1 and X_0 and the current states Q_i .

[Considere o seguinte diagrama de estados com duas entradas $X_1 X_0$ em que cada estado $S_i (i = 1, \dots, 8)$ é implementado com flip-flops do tipo D, com entradas D_i (próximo estado) e saída Q_i (estado actual). Indique, para o estado S_3 , a expressão de D_3 como função de X_1 e X_0 e os estados actuais Q_i .]

[1]: $D_3 = \overline{X_1} X_0 Q_2 + \overline{X_1} X_0 Q_3 + \overline{X_1} X_0 Q_4 + \overline{X_1} \overline{X_0} Q_5$

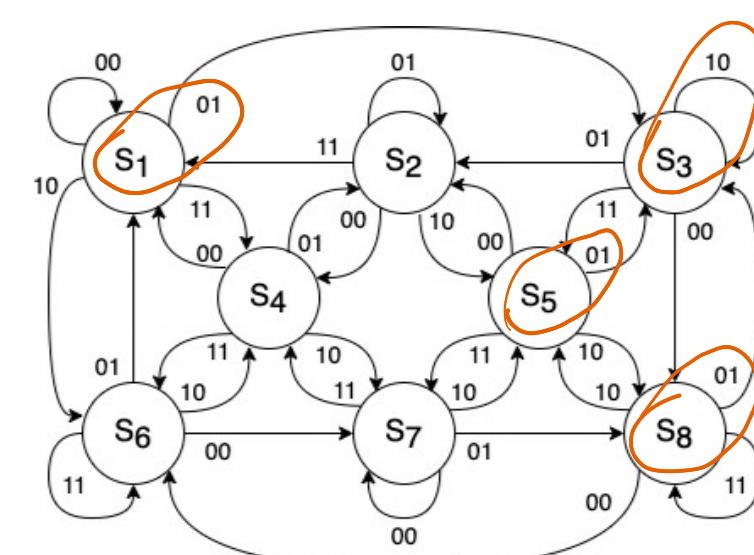
[2]: $D_3 = X_1 X_0 Q_1 + \overline{X_1} \overline{X_0} Q_2 + X_1 \overline{X_0} Q_6 + X_1 X_0 Q_7$

[3]: $D_3 = X_1 \overline{X_0} Q_2 + X_1 X_0 Q_3 + X_1 \overline{X_0} Q_7 + X_1 \overline{X_0} Q_8$

[4]: $D_3 = \overline{X_1} X_0 Q_1 + X_1 \overline{X_0} Q_3 + \overline{X_1} X_0 Q_5 + \overline{X_1} X_0 Q_8$

[5]: $D_3 = \overline{X_1} \overline{X_0} Q_1 + X_1 X_0 Q_2 + \overline{X_1}$

[6]: None of the other options [Nenhuma das outras opções]

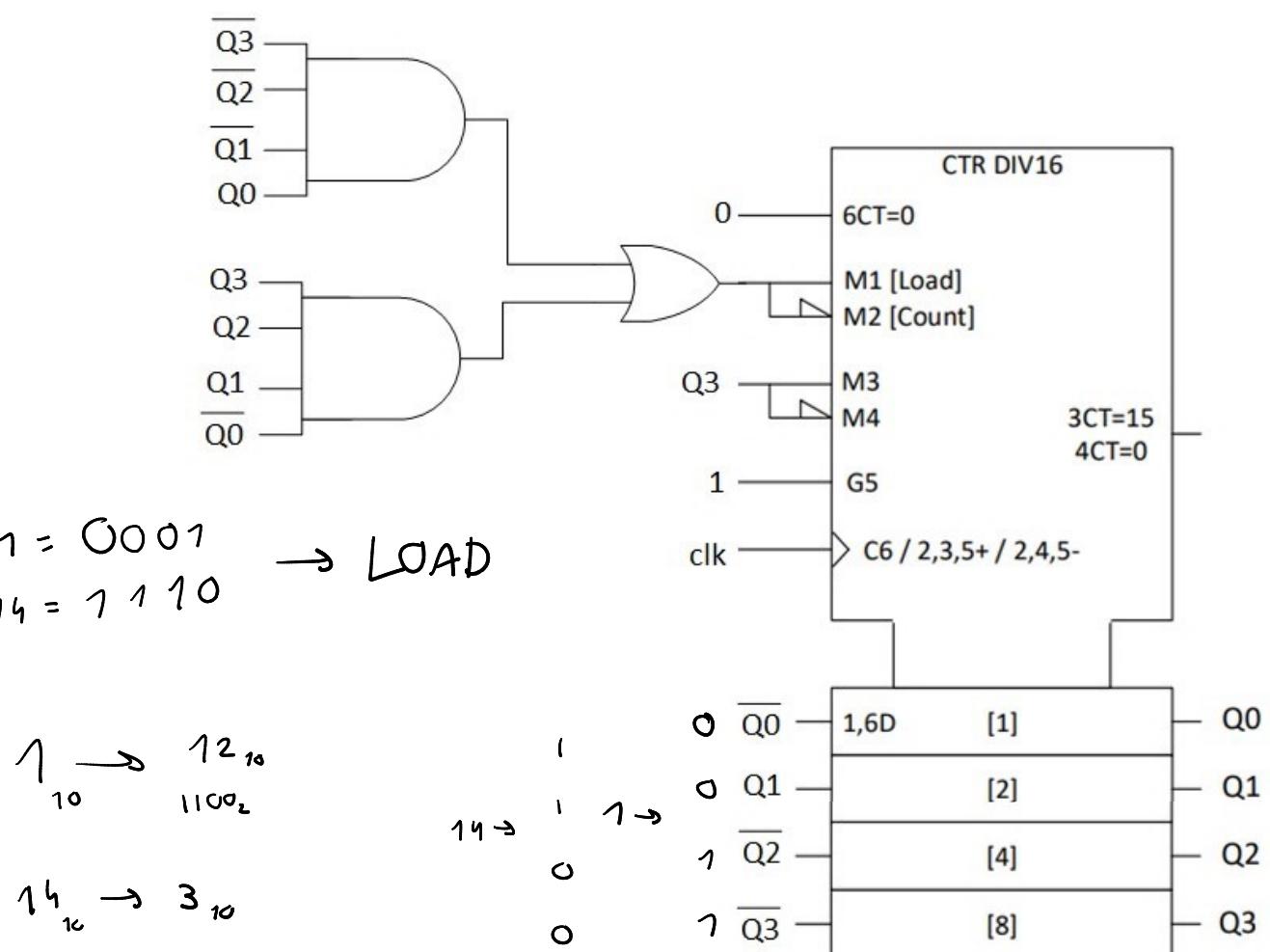


- H. Which of the following options corresponds to the sequence, in stationary mode, in decimal format at the output of the circuit in the figure below? (suggestion: start by analyzing a "load" situation.)

[Qual das seguintes opções corresponde à sequência de saída do seguinte circuito, em regime estacionário e em formato decimal? (sugestão: comece por analisar a situação de carregamento ("load") de dados.)]

- [1]: ... 11 - 3 - 4 - 5 - 13 - 12 - 11 ...
- [2]: ... 10 - 7 - 6 - 5 - 8 - 9 - 10 ...
- [3]: ... 12 - 1 - 2 - 3 - 14 - 13 - 12 ...
- [4]:** ... 14 - 3 - 2 - 1 - 12 - 13 - 14 ... $1 = 0001$ → LOAD
- [5]: ... 13 - 5 - 4 - 3 - 11 - 12 - 13 ... $14 = 1110$

- [6]: None of the other options
[Nenhuma das outras opções]



$$\begin{array}{l} 1 \rightarrow 12_{10} \\ \downarrow \\ 10 \end{array}$$

$$\begin{array}{l} 14 \rightarrow 1 \\ \downarrow \\ 0 \end{array}$$

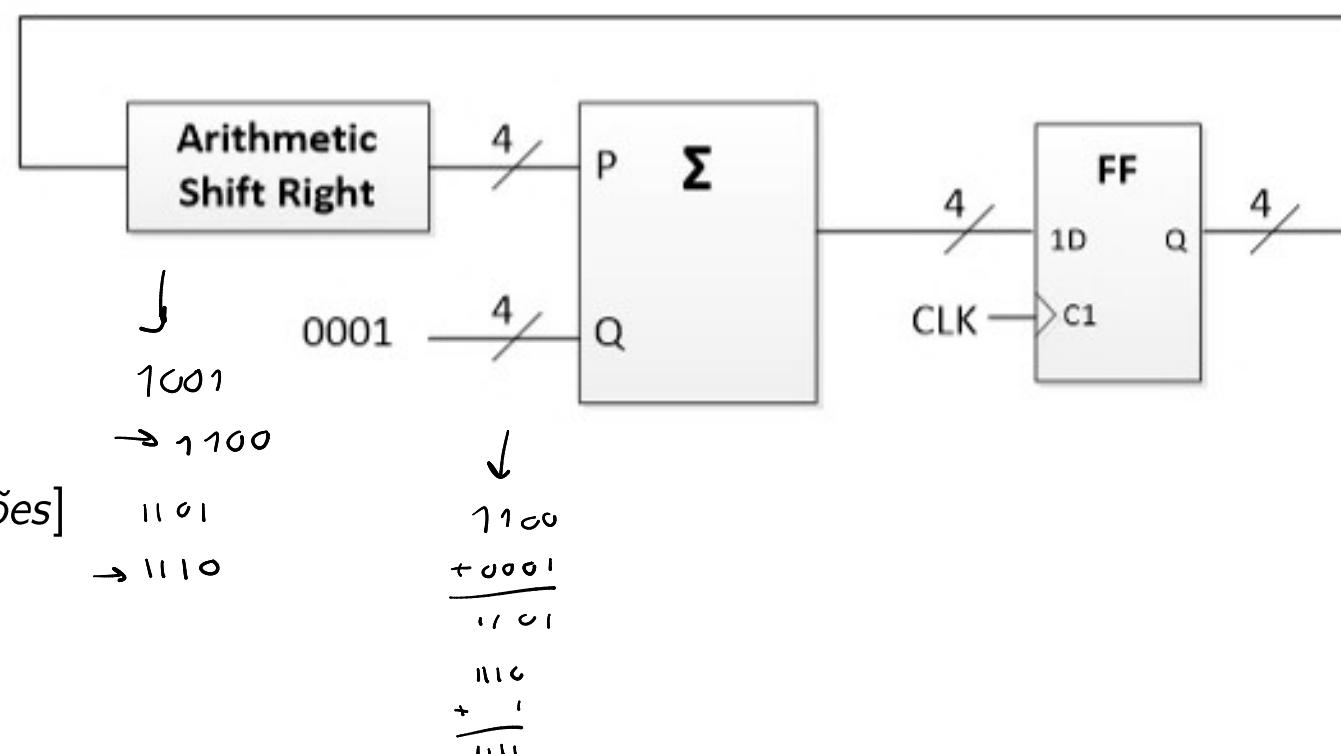
$$\begin{array}{l} 14 \rightarrow 3_{10} \\ \downarrow \\ 10 \end{array}$$

- I. Consider the following circuit with an adder, a register (4 FF's) and a combinational logic circuit. Assuming that the current state is $Q(3:0) = 1001$, what are the next two states of the circuit?

[Considere o seguinte circuito com um somador, um registo (4 FF's) e lógica combinatória. Assumindo que o estado actual é $Q(3:0) = 1001$, quais serão os próximos dois estados do circuito?]

- [1]: 0101, 0011
- [2]: 1011, 1111
- [3]:** 1101, 1111
- [4]: 0011, 0111
- [5]: 1100, 1110

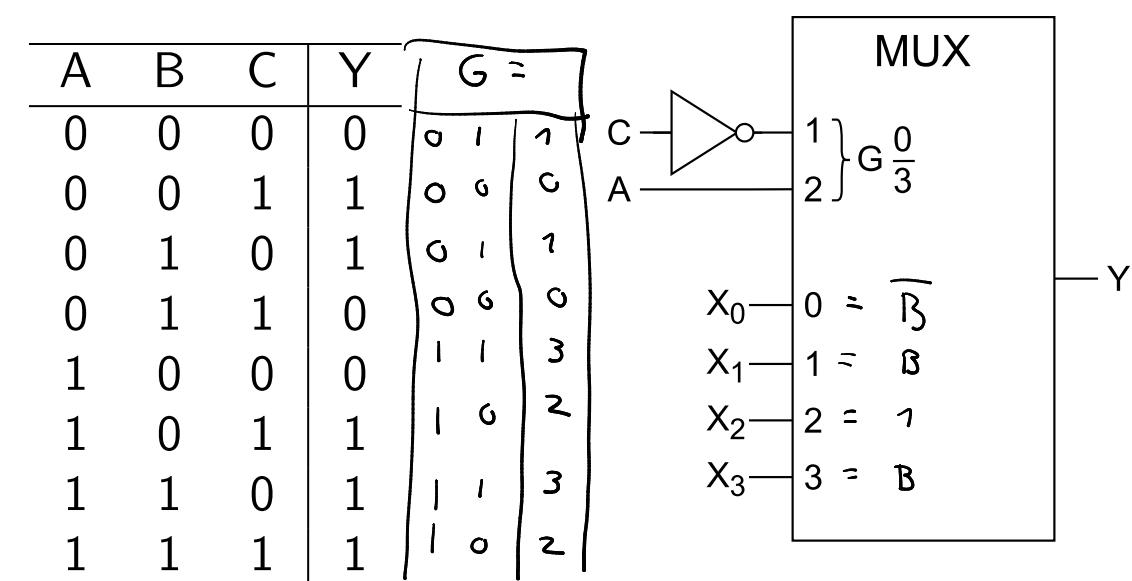
- [6]: None of the other options
[Nenhuma das outras opções]



- J. Consider the following circuit and truth table. Select the multiplexer inputs $\{X_3; X_2; X_1; X_0\}$ that result in the given truth table.

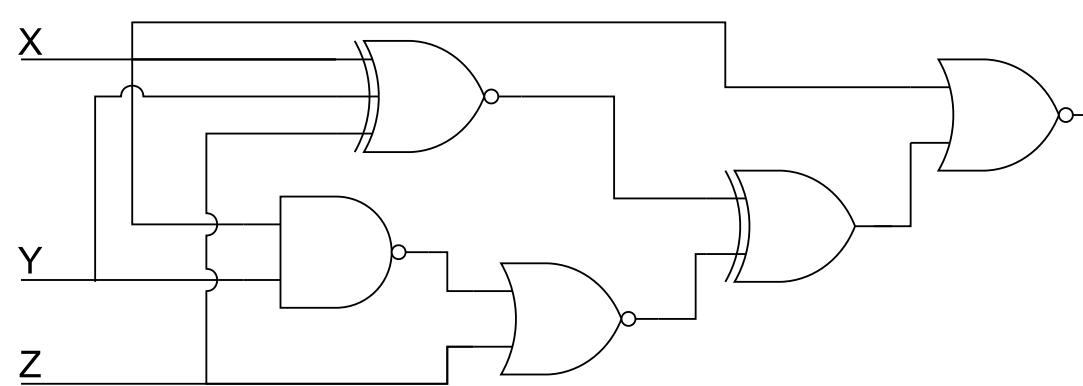
[Considere o seguinte circuito e tabela de verdade. Selecione as entradas do multiplexer $\{X_3; X_2; X_1; X_0\}$ que resultam na tabela apresentada.]

- [1]:** $\{X_3; X_2; X_1; X_0\} = \{B; 1; B; \bar{B}\}$
- [2]: $\{X_3; X_2; X_1; X_0\} = \{\bar{B}; 1; B; \bar{B}\}$
- [3]: $\{X_3; X_2; X_1; X_0\} = \{B; 1; \bar{B}; 0\}$
- [4]: $\{X_3; X_2; X_1; X_0\} = \{B; 0; \bar{B}; \bar{B}\}$
- [5]: $\{X_3; X_2; X_1; X_0\} = \{0; 1; B; \bar{B}\}$
- [6]: None of the other options
[Nenhuma das outras opções]



K. What is the worst case for the propagation time of the following circuit?

[Qual é o pior caso para o tempo de propagação do seguinte circuito?]



Gate	tp [ns]
NAND2	8
NOR2	9
XOR2	15
XNOR2	16
XNOR3	18

[1]: 50
[4]: 44

[2]: 42
[5]: 40

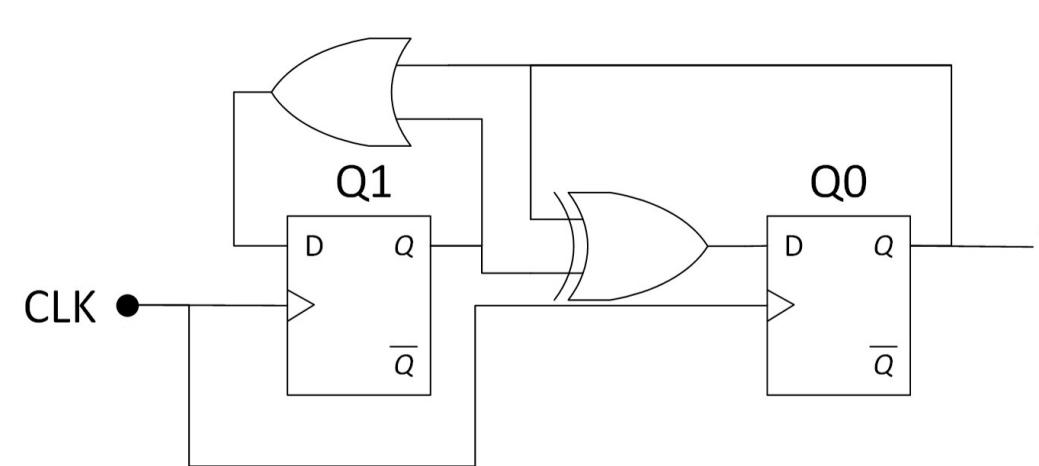
[3]: 41
[6]: None of the other options
[Nenhuma das outras opções]

$$XNOR3 + XOR2 + NOR2 = 18 + 15 + 9 = 42$$

$$NAND2 + NOR2 + XOR2 + NOR2 = 8 + 9 + 15 + 9 = 41$$

L. Consider the following circuit. Which state diagram corresponds to the circuit?

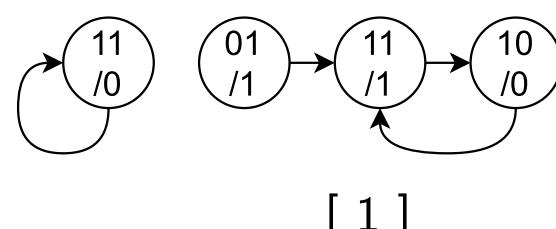
[Considere o seguinte circuito. Qual dos diagramas de estado corresponde ao funcionamento do circuito?]



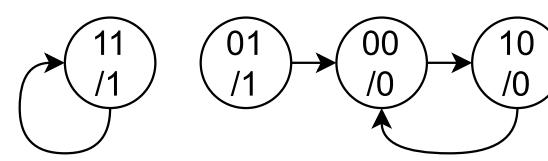
$$D_0 = Q_0 \oplus Q_1$$

$$D_1 = Q_0 + Q_1$$

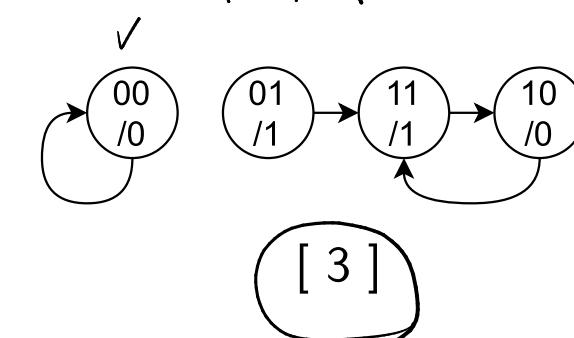
Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0
0	1	1	1	1
1	0	1	1	0
1	1	1	0	1



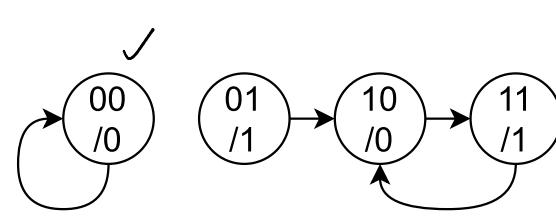
[1]



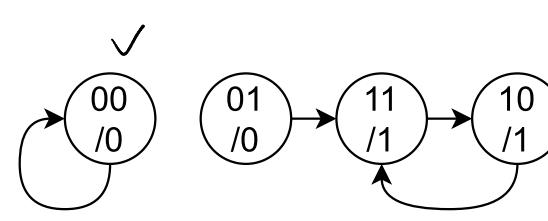
[2]



[3]



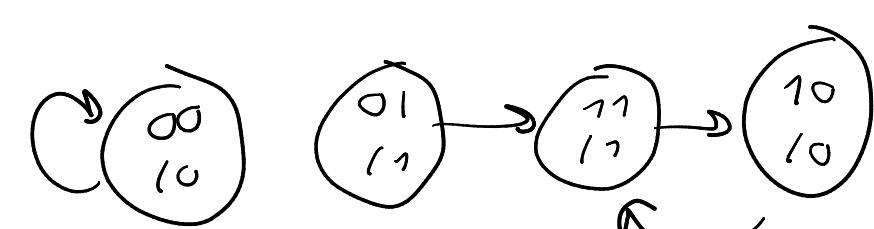
[4]



[5]

None of the other options
[Nenhuma das outras opções]

[6]



M. Represent 11101101₂ in octal.

[Represente 11101101₂ em octal.]

355

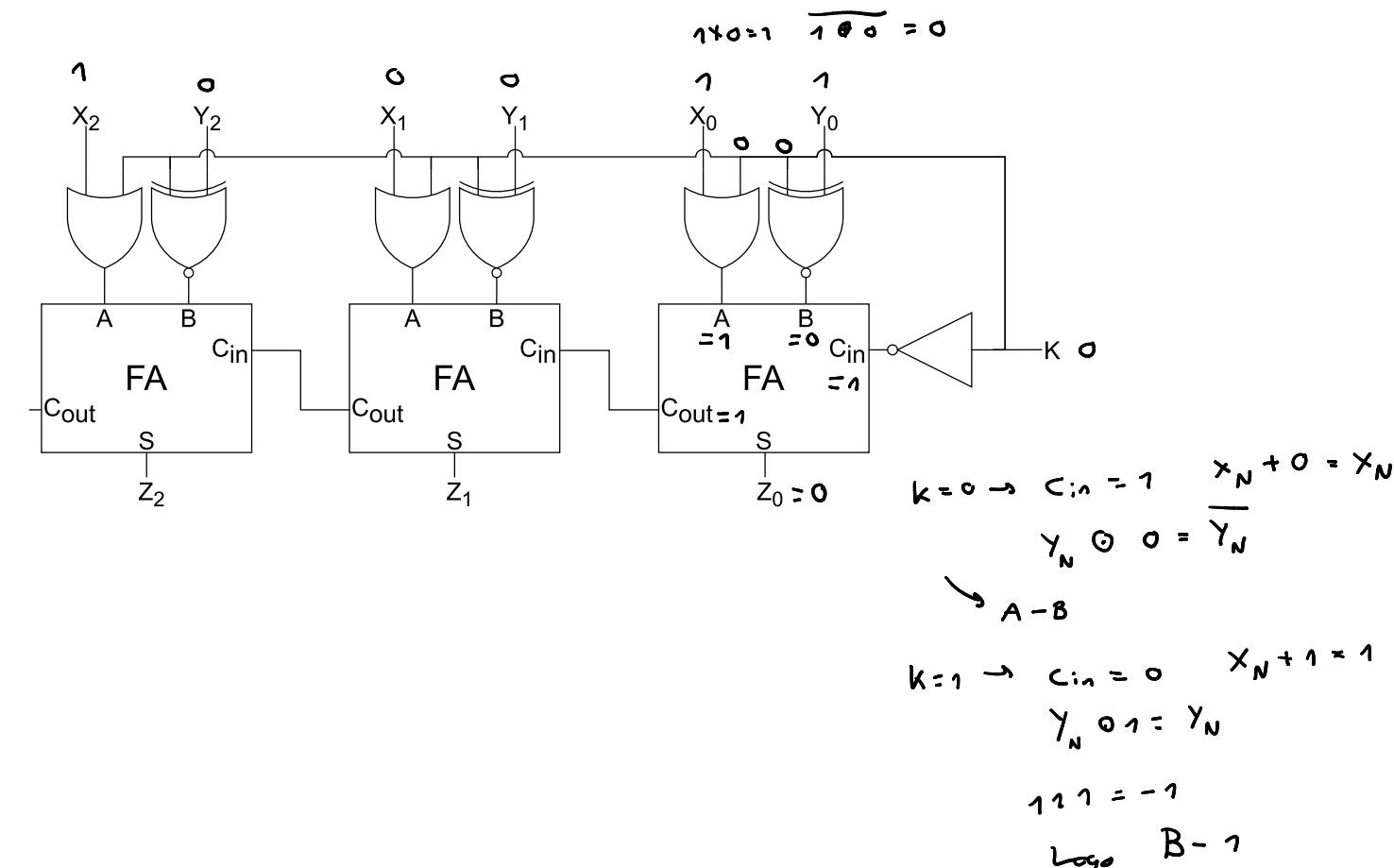
[1]: 237
[4]: 155

[2]: 205
[5]: 255

[3]: 355
[6]: None of the other options
[Nenhuma das outras opções]

- N. Which function is implemented by the following circuit? Consider that X and Y are 3-bit signed numbers (two's complement).
 [Qual é a função desempenhada pelo seguinte circuito? Assuma que X e Y são números com sinal com 3-bits (em complemento para dois).]

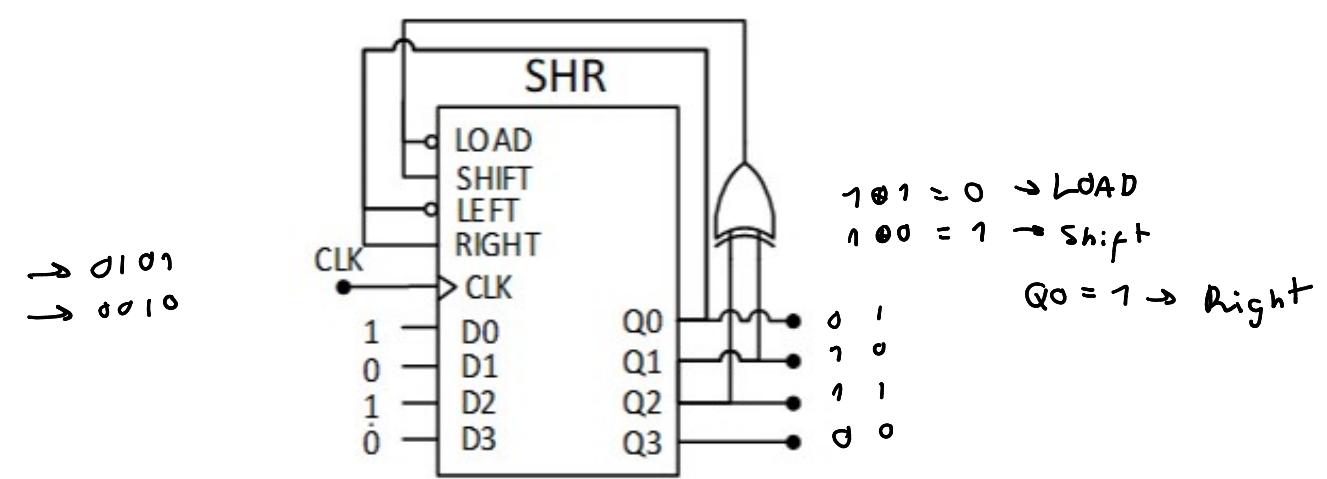
- [1]: K=0: $Z=X+Y$; K=1: $Z=Y-1$
- [2]: K=0: $Z=X+1$; K=1: $Z=X-Y$
- [3]: K=0: $Z=X-Y$; K=1: $Z=Y+1$
- [4]:** K=0: $Z=X-Y$; K=1: $Z=Y-1$
- [5]: K=0: $Z=X-1$; K=1: $Z=X+Y$
- [6]: None of the other options
 [Nenhuma das outras opções]



- O. Consider the following circuit with a 4-bit shift register where the serial data inputs are always zero. The current state is Q3 Q2 Q1 Q0 = 0110. What are the next two states of the circuit?

[Considere o seguinte circuito com um registo de deslocamento de 4-bits em que as entradas de dados série são sempre zero. O estado actual é Q3 Q2 Q1 Q0 = 0110. Quais serão os próximos dois estados?]

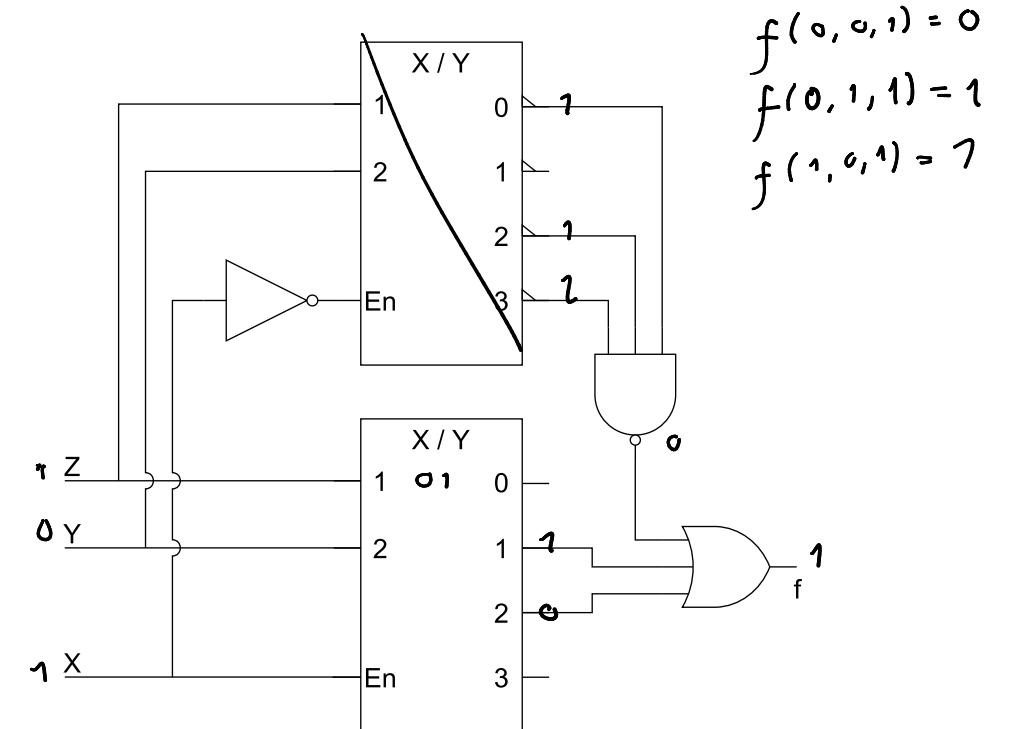
- [1]: 1011, 1100
- [2]:** 0101, 0010
- [3]: 1010, 0101
- [4]: 1100, 1000
- [5]: 0011, 1010
- [6]: None of the other options [Nenhuma das outras opções]



- P. Select the option corresponding to the output $f(X, Y, Z)$ of the circuit shown below, when the inputs (X, Y, Z) have the values $(0, 0, 1), (0, 1, 1)$, and $(1, 0, 1)$.

[Indique qual das opções corresponde à saída $f(X, Y, Z)$ do circuito apresentado em baixo, quando as entradas (X, Y, Z) tomam os valores $(0, 0, 1), (0, 1, 1)$, e $(1, 0, 1)$.]

- [1]:** $\{f(0, 0, 1); f(0, 1, 1); f(1, 0, 1)\} = \{0; 1; 1\}$
- [2]: $\{f(0, 0, 1); f(0, 1, 1); f(1, 0, 1)\} = \{0; 0; 1\}$
- [3]: $\{f(0, 0, 1); f(0, 1, 1); f(1, 0, 1)\} = \{1; 0; 1\}$
- [4]: $\{f(0, 0, 1); f(0, 1, 1); f(1, 0, 1)\} = \{0; 1; 0\}$
- [5]: $\{f(0, 0, 1); f(0, 1, 1); f(1, 0, 1)\} = \{1; 0; 0\}$
- [6]: None of the other options [Nenhuma das outras opções]

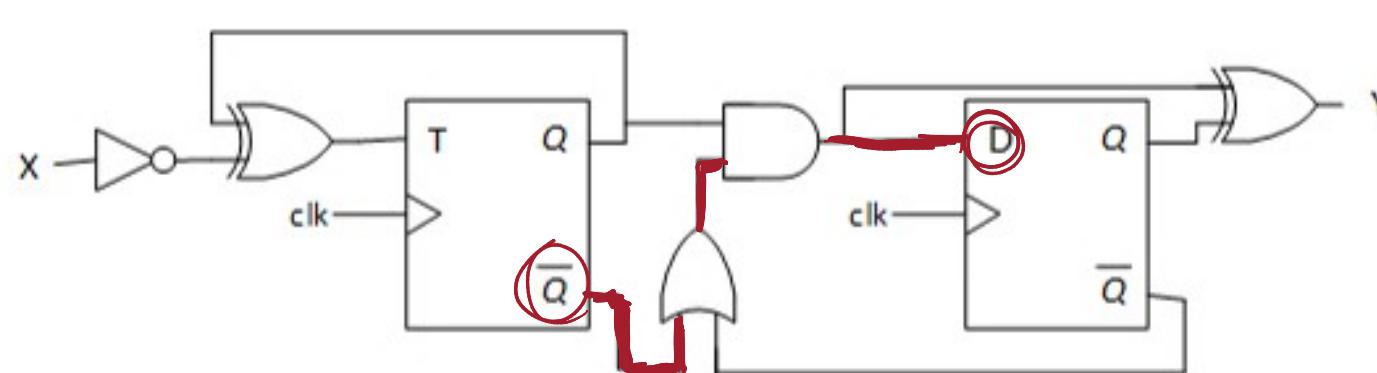


Regular Exam

Digital Systems (2021/2022)

February 12th, 2022

- Q. What is the minimum clock period of the following circuit, given the table values (in ns)?
 [Qual é o período de relógio mínimo do seguinte circuito, assumindo os valores da tabela (em ns)?]



	tp [ns]	tsu [ns]	th [ns]
FF D	13	6	5
FF T	14	7	7
AND	10		
OR	8		
XOR	12		
NOT	4		

$$T_p = t_{p_{FFT}} + t_{p_{AND}} + t_{p_{OR}} + t_{su\ FFD}$$

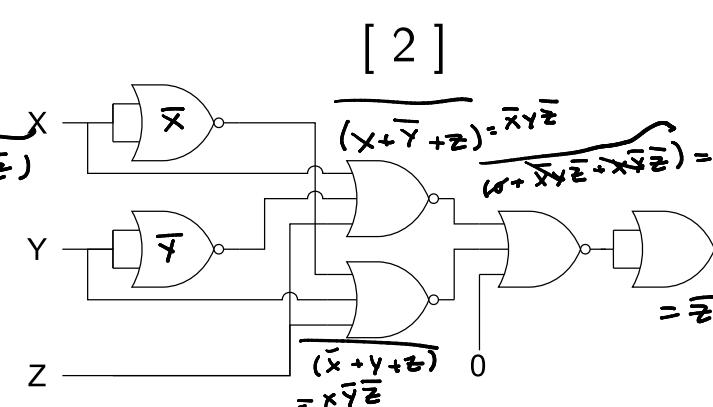
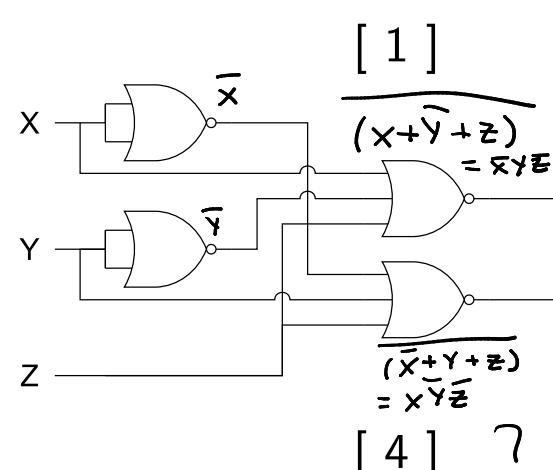
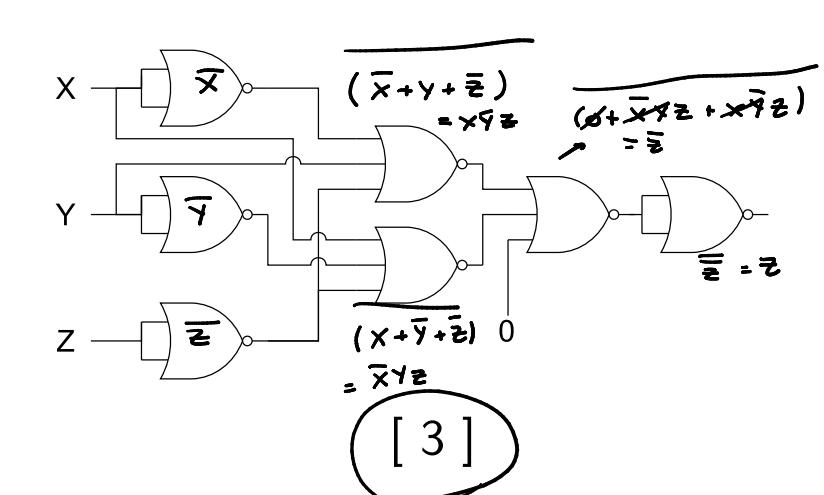
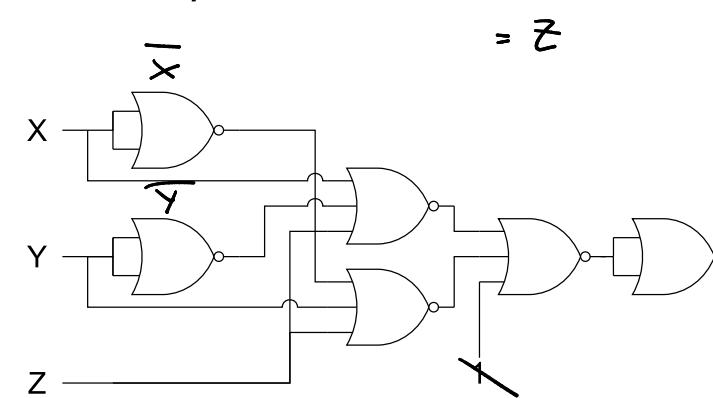
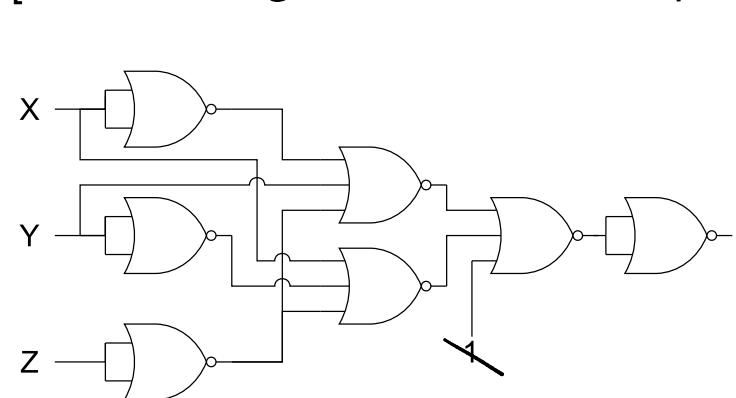
$$= 14 + 10 + 8 + 6 = 38$$

[1]: 50
 [4]: 66

[2]: 33
 [5]: 37

[3] 38
 [6]: None of the other options
 [Nenhuma das outras opções]

- R. Which of the following circuits implements the expression $X \bar{Y}Z + \bar{X}YZ$?
 [Qual dos seguintes circuitos implementa a expressão $X \bar{Y}Z + \bar{X}YZ$?]



None of the other options
 [Nenhuma das outras opções]

[6]

(This space was intentionally left blank for you auxiliary calculations.)

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Regular Exam

Digital Systems (2021/2022)

February 12th, 2022

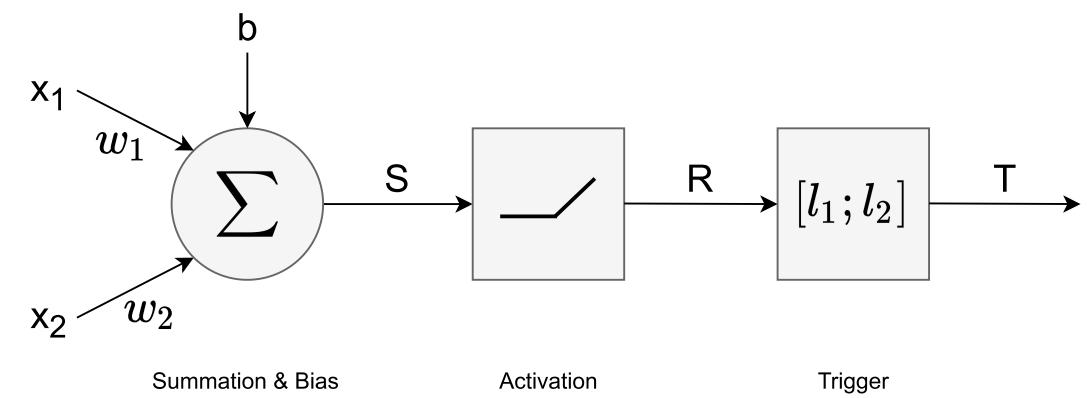
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Volume 1 - Part II

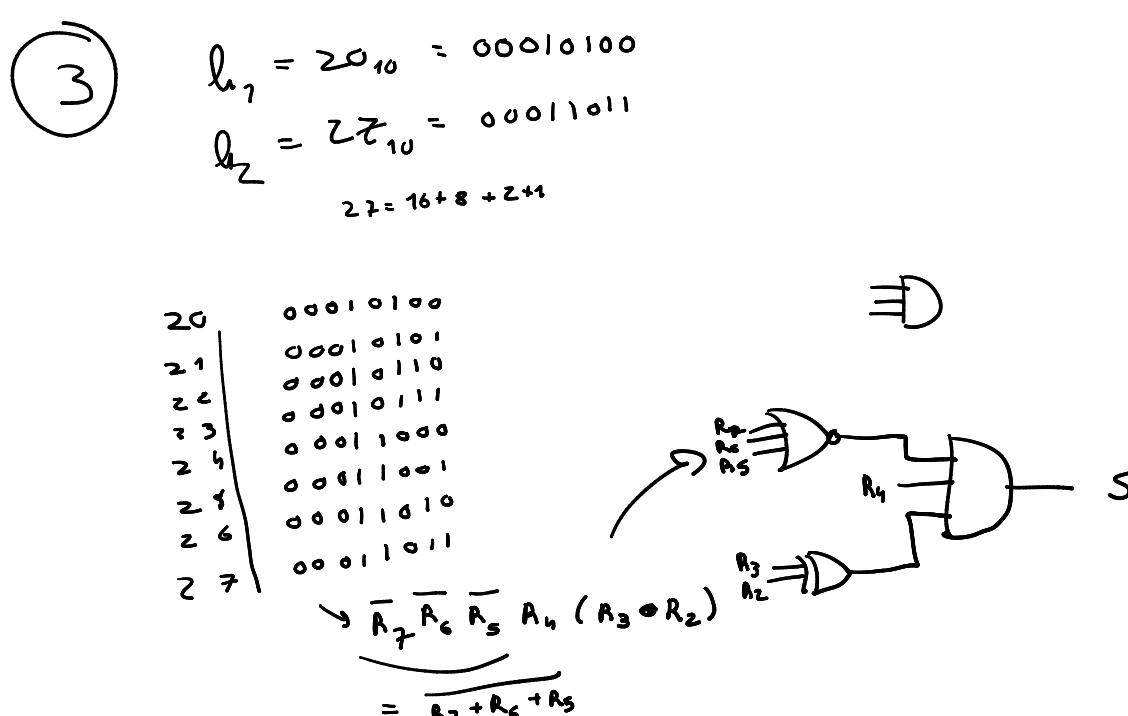
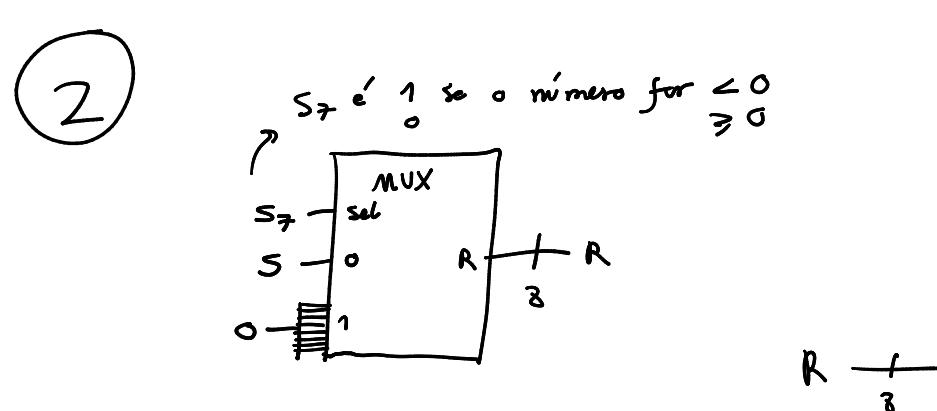
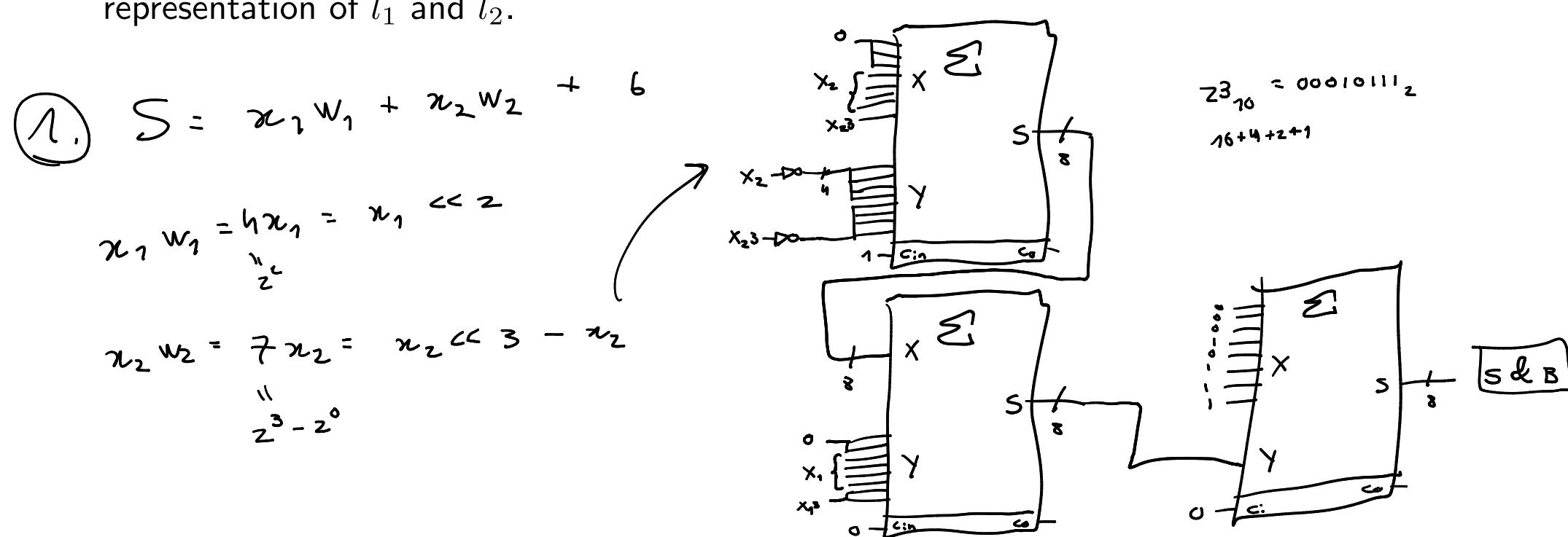
NOTE: Portuguese version in the following page

[Question score partitioning: 50% + 20% + 30%]

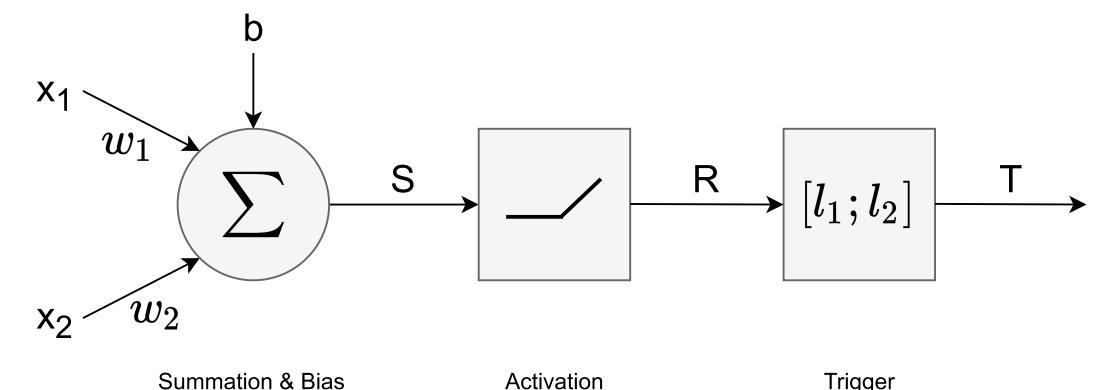
The neural network depicted in the figure comprises three layers that implement the *Summation & Bias*, the *ReLU Activation* function, and the *Trigger* function, respectively. The network processes a 2-D input vector (x_1, x_2) , where each input x_i is a signed integer represented with 4-bits. The final output T is a binary value (1-bit). In the following exercises, consider the utilization of 8-bit adders and assume an 8-bit precision in all intermediary calculations:



1. Design the circuit that implements the *Summation & Bias* layer, whose function is given by $S = \sum_{i=1}^{i=2} x_i \cdot w_i + b$. Assume the following parameterization: $w_1 = 4$, $w_2 = 7$, and $b = -23$.
2. Implement the circuit of the *ReLU Activation* function, given by $R(s) = \begin{cases} s & \text{if } s \geq 0; \\ 0 & \text{if } s < 0. \end{cases}$
3. By using the minimum hardware resources as possible, design the circuit that implements the *Trigger* function $T(x)$, whose output is equal to 1 when $l_1 \leq x \leq l_2$, by assuming $l_1 = 20$ and $l_2 = 27$. Hint: look at the binary representation of l_1 and l_2 .



A rede neuronal representada na figura inclui três camadas que implementam a *Summation & Bias*, a função *ReLU Activation*, e a função *Trigger*, respectivamente. A rede processa um vector 2-D (x_1, x_2) de entrada, onde cada entrada x_i é um inteiro com sinal representado com 4-bits. A saída final T é um valor binário (1-bit). Nos seguintes exercícios, considere a utilização de somadores de 8-bits e assuma precisão de 8-bits em todos os cálculos intermédios:



1. Desenhe o circuito que implementa a camada *Summation & Bias*, cuja função é dada por $S = \sum_{i=1}^{i=2} x_i \cdot w_i + b$. Assuma a seguinte parametrização: $w_1 = 4$, $w_2 = 7$, e $b = -23$.
2. Implemente o circuito da função *ReLU Activation*, dada por $R(s) = \begin{cases} s & \text{se } s \geq 0; \\ 0 & \text{se } s < 0. \end{cases}$.
3. Utilizando o mínimo possível de recursos de hardware, projecte o circuito que implementa a função *Trigger* $T(x)$, cuja saída é igual a 1 quando $l_1 \leq x \leq l_2$, assumindo que $l_1 = 20$ e $l_2 = 27$. Sugestão: analise com atenção a representação binária de l_1 e l_2 .

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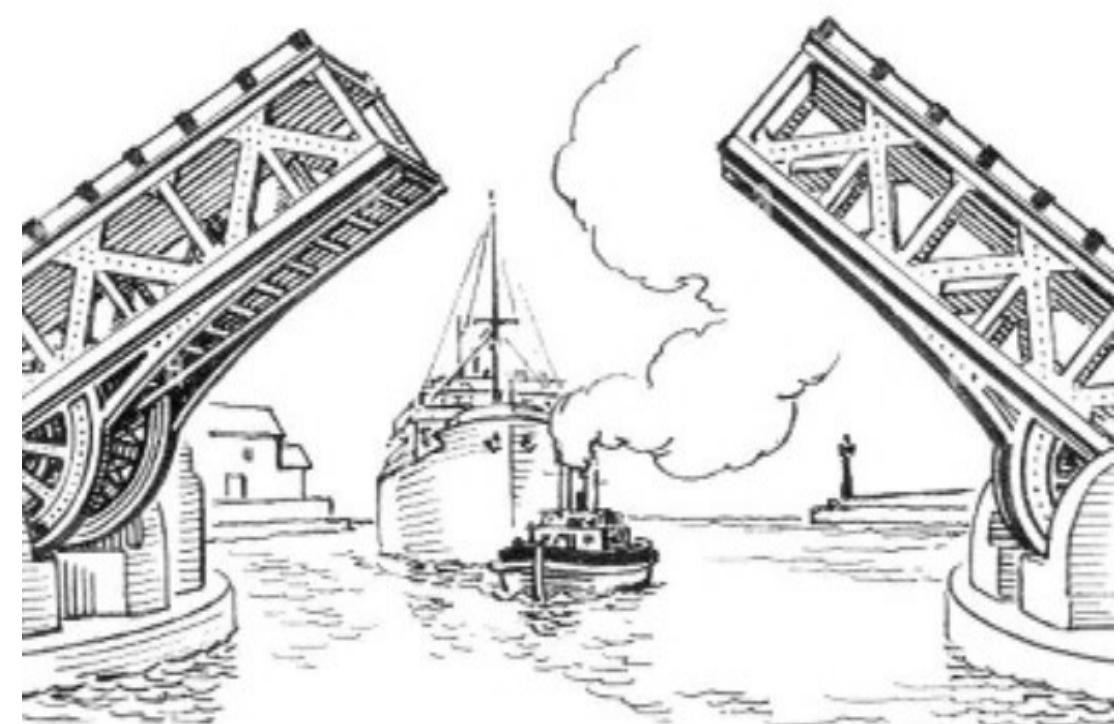
Volume 1 - Part III

NOTE: Portuguese version in the following page

[Question score partitioning: 50% + 50%]

Question A:

Design a circuit that controls a bascule bridge over a river. Since the bridge is relatively low, boats can only pass when the bridge is open (i.e., elevated). The operation of the bascule bridge is automated, with safety being guaranteed by radars and traffic lights. A set of radars detects cars crossing the bridge (CR) and another set detects boats approaching the bridge (BR). For both, detection means logical value '1'. There is a set of traffic lights for cars (CS) and another for boats (BS). The traffic lights include two lights: green (logical value '1') and red (logical value '0'). A signal (EU) activates the mechanism to open the bridge, and another signal (ED) activates the mechanism to close the bridge. The system includes a timer, able to count intervals of 15s. The timer is activated when the enabling signal (AT) has value '1', and keeps counting while that value is kept; it resets to inactive when that signal has value '0'; it activates signal TE when it expires at the end of 15s. The operation of the bridge obeys to the following rules:



- The initial state of the bridge is in the closed (i.e., down) position, with EU, ED and AT inactive, CS green and BS red. Starting from this state, when BR is activated by approaching boats, CS immediately becomes red. After CR detects that there are no cars crossing the bridge, EU is activated (value '1') until the bridge is completely open, which takes 15s.
- When the bridge is completely open, BS becomes green, and it remains so until no boats are detected by BR. Once no boats are detected, BS becomes immediately red. ED is activated (value '1') until the bridge is completely closed, which takes 15s. Then, the system goes back to the initial state.
- If, while the bridge is being elevated, a car is detected, the elevation stops until cars are no longer detected. After this, elevation resumes.
- It is more difficult to stop a boat than a car. If, while the bridge is lowering, a boat is detected, the bridge must be elevated again.
- In this bridge model, there are no other mechanisms to detect that the bridge is open or closed other than the known timings of the elevation and lowering operations. In case of doubt, the worst case must be considered.

Design the Moore machine of the circuit, presenting its state diagram, and defining all state transitions and output values for each state. "Don't cares" must be used for the inputs whose value does not matter for given a state transition. In the diagram, indicate the inputs/outputs according to the following order:

- Order of the inputs: BR, CR, TE.
- Order of the outputs: BS, CS, EU, ED, AT.

Explain succinctly the operation of the state machine and clearly indicate the meaning of each state.

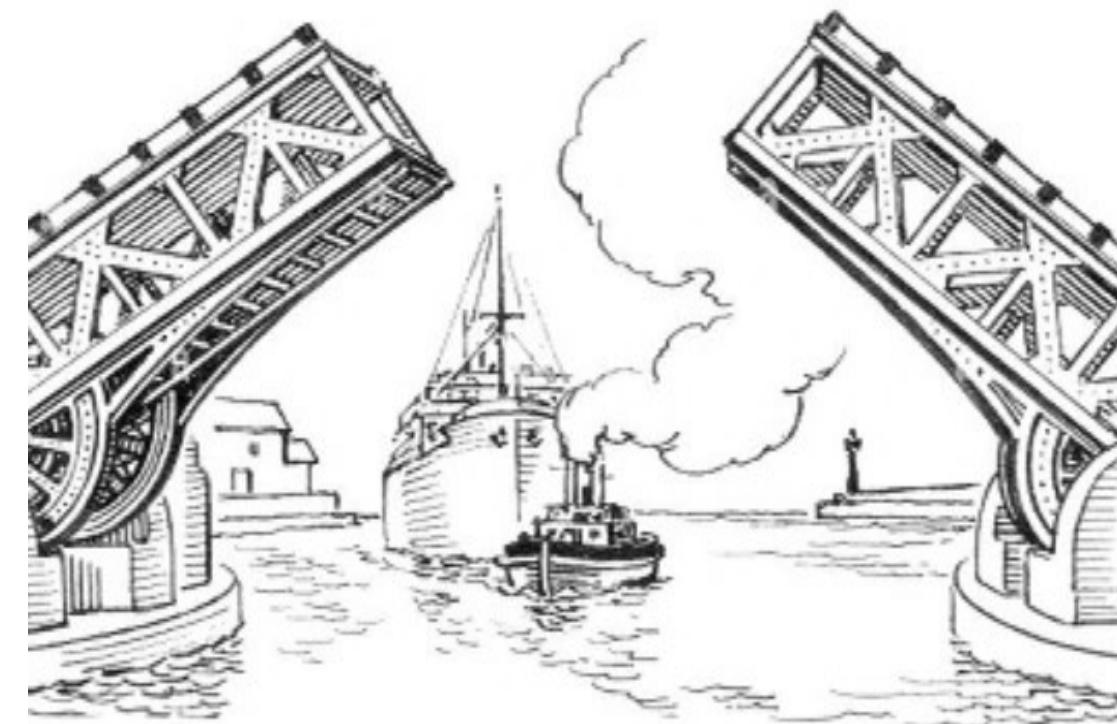
Question B:

The state transition table on the right describes the behavior of a machine with 4 states, one input E and one output Y. Design a circuit that implements it using 1 flip-flop T (FF0), and 1 flip-flop D (FF1), as well as AND, OR and NOT gates. Obtain the logical expressions (in minimal form) for the flip-flop input signals, as well as the output of the circuit.

Q1(n)	Q0(n)	E	Q1(n+1)	Q0(n+1)	Y
0	0	0	1	1	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	1	0
1	1	1	0	1	1

Pergunta A:

Projecte um sistema de controlo de uma ponte basculante entre as duas margens de um rio. Como a ponte é relativamente baixa, as embarcações só podem passar quando a ponte está aberta (i.e., elevada). A operação da ponte basculante está automatizada, sendo a segurança garantida por radares e semáforos. Um conjunto de radares detecta automóveis a atravessar a ponte (CR), e outro detecta embarcações a aproximar-se da ponte (BR). Para ambos, o nível lógico '1' significa que houve detecção. Existe um conjunto de semáforos para automóveis (CS) e outro para embarcações (BS). Os semáforos incluem duas luzes: verde (valor lógico '1') e vermelho (valor lógico '0'). Um sinal (EU) activa o mecanismo para abrir a ponte, e outro sinal (ED) activa o mecanismo para fechar a ponte. O sistema inclui um temporizador, capaz de contar intervalos de 15s. O temporizador é activado quando o seu sinal de activação (AT) tem valor '1', e continua a contar enquanto aquele valor for mantido; o temporizador reinicializa e fica inactivo quando aquele sinal tem valor '0'; quando expira ao fim de 15s, o temporizador activa o sinal TE. A operação da ponte obedece às seguintes regras:



- O estado inicial da ponte é fechada (i.e., em baixo), com EU, ED e AT inactivos, CS verde e BS vermelho. Partindo deste estado, quando BR é activado por embarcações em aproximação, CS passa imediatamente a vermelho. Quando CR já não detectar carros a atravessar, EU é activado (valor '1') até que a ponte fique completamente aberta, o que acontece ao fim de 15s.
- Quando a ponte está completamente aberta, BS fica verde, e permanece assim até que nenhuma embarcação seja detectada por BR. Assim que isto acontecer, BS fica imediatamente vermelho. ED é activado (valor '1') até que a ponte fique completamente fechada, o que acontece ao fim de 15s. Uma vez aqui, o sistema volta ao estado inicial.
- Se, enquanto a ponte está a ser elevada, um automóvel for detectado, a elevação pára até que já não sejam detectados automóveis. Depois disto, a elevação da ponte continua.
- é mais difícil travar uma embarcação do que um automóvel. Se, enquanto a ponte está a baixar, uma embarcação for detectada, a ponte tem de ser elevada novamente.
- Neste modelo de ponte, não há outros mecanismos para detectar que a ponte está aberta ou fechada que não sejam os tempos bem conhecidos de elevação e abaixamento. Em caso de dúvida, tem de se considerar o pior caso.

Projecte a máquina de Moore do circuito, apresentando o diagrama de estados, e definindo todas as transições de estado e valores de saída de cada estado. As "indiferenças" têm de ser obrigatoriamente usadas para entradas que não tenham influência numa determinada transição de estado. No diagrama, as entradas/saídas têm de ser indicadas de acordo com a ordem seguinte:

- Ordem das entradas: BR, CR, TE.
- Ordem das saídas: BS, CS, EU, ED, AT.

Explique sucintamente a operação da máquina de estados e indique de forma clara o significado de cada estado.

Pergunta B:

A tabela de transição de estados à direita descreve uma máquina com 4 estados, uma entrada E e uma saída Y. Projecte o circuito que a implementa utilizando 1 flip-flop T (FF0), e 1 flip-flop D (FF1), assim como portas AND, OR e NOT. Obtenha as expressões algébricas (na forma mínima)

Q1(n)	Q0(n)	E	Q1(n+1)	Q0(n+1)	Y
0	0	0	1	1	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	0	0	1



**Don't forget to identify this and the following pages!
Only these pages will be considered for your evaluation.**

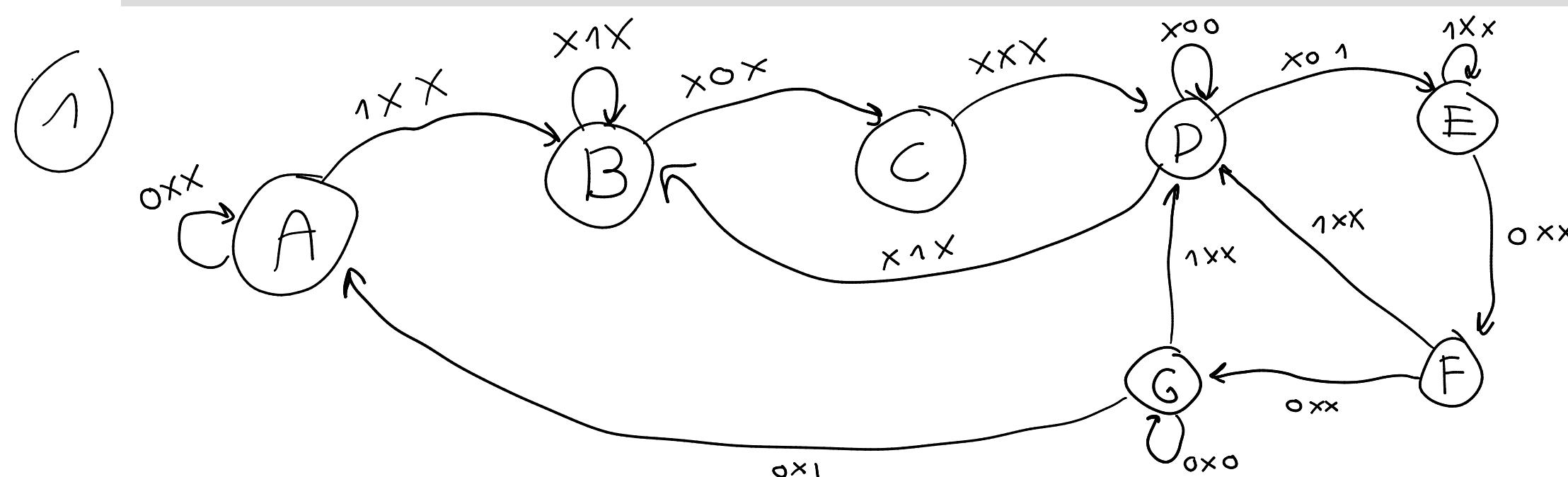
Volume 2 - Part I

For each question of Part I (question A, B, C, ...), fill in the number of the correct answer from the supplied multiple-choice list (answer 1, 2, 3, ...):

*	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1																					X	X	X	X	X	X

NOTE: Leave blank (or fill in with 0) all questions that you do not wish to answer.

Volume 2 - Part II



A - Fechado, CS verde e BS vermelho

out: 01000

B - Barco Detetado

out: 00000

C - Não há carros na ponte

out: 00000

D - Começar temporizador, carro subindo

out: 00101

G - Baixar a ponte - Temporizador - Voltar a subir se detectar barco
out: 00011

H - Ponte em baixo completamente
out: 01000

E - ponte destruída
out : 10000

F - já não é detectado barco
out : 00000

Number: _____

Name: _____

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Volume 2 - Part II (Cont.)

2

Pergunta B:

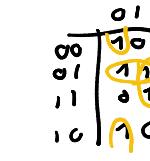
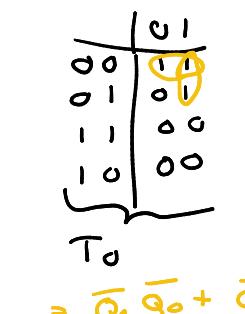
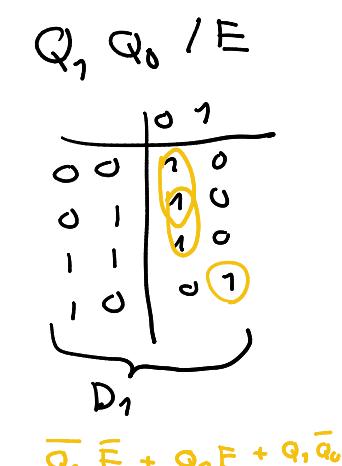
A tabela de transição de estados à direita descreve uma máquina com 4 estados, uma entrada E e uma saída Y. Projetar o circuito que a implementa utilizando 1 flip-flop T (FF0), e 1 flip-flop D (FF1), assim como portas AND, OR e NOT. Obtenha as expressões algébricas (na forma mínima) para os sinais de entrada dos flip-flops, assim como da saída do circuito.

$$T_0 = \dots$$

$$D_1 = \dots$$

$$Y = \dots$$

$Q_1(n)$	$Q_0(n)$	E	$Q_1(n+1)$	T_0	$Q_0(n+1)$	Y
0	0	0	1	1	1	1
0	0	1	0	1	1	0
0	1	0	1	1	0	1
0	1	1	0	0	1	1
1	0	0	0	0	0	1
1	0	1	1	0	0	0
1	1	0	1	0	1	0
1	1	1	0	0	1	1



$$\overline{Q}_1 \overline{E} + \overline{Q}_1 E$$

$$\overline{Q}_1 \overline{Q}_0$$

$$\overline{Q}_0 \overline{Q}_1$$

$$Y = \overline{Q}_0 \overline{E} + \overline{Q}_1 Q_0 + Q_0 E$$

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Volume 2 - Part III

Number: _____

Name: _____

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Volume 2 - Part III (Cont.)

IMPORTANT: Do not forget to identify the previous page.

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Instructions

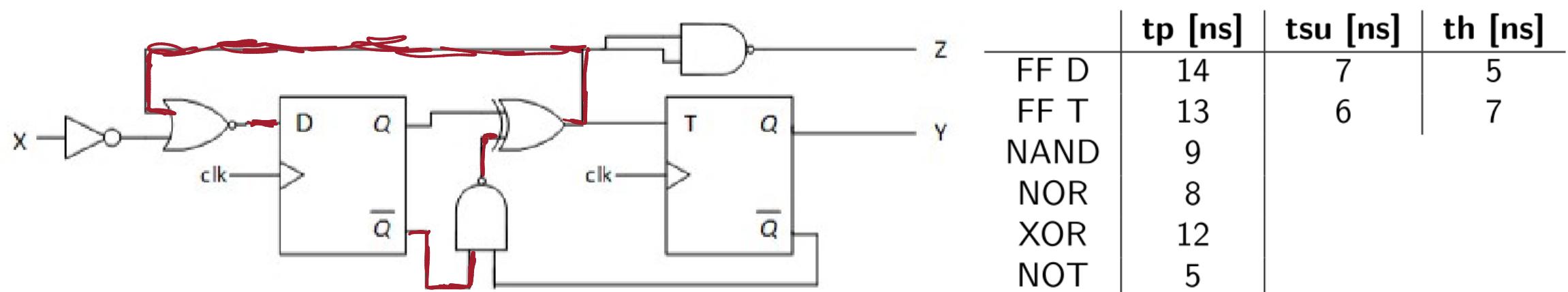
Before starting the exam, read carefully the following information:

- There are (at least) nine different versions of this exam.
- Although the exam comprises a total of 16 pages, there are two distinct volumes that should be handled as follows:
 - **Volume 1** corresponds to the question list and comprises pages 1 to 12. These pages do not need to be identified because they will be discarded at the end of the exam;
 - **Volume 2** corresponds to the answers sheet and comprises pages 13 to 16. All pages of this volume **MUST** be identified with the student's name and number.
 - At the end of the exam, all pages of **Volume 2** will be separated. Consequently, all non-identified pages will not be considered.
- The exam is composed of three parts (Part I, II and III) and has a duration of 2 (two) hours.
 - **Part I** comprises N_1 multiple choice questions and awards a total of $P_1 = 15$ points.
 - * Each correct answer awards $C = P_1/N_1$ points;
 - * Each wrong answer awards $W = -C/(A - 1)$ points (negative value), where A denotes the number of possible answers offered to each question;
 - * Each non-answered question awards 0 points.
 - **Part II** comprises an open-answer problem about combinatorial circuits and awards a total of $P_2 = 2.5$ points.
 - **Part III** comprises an open-answer problem about sequential circuits and awards a total of $P_3 = 2.5$ points.
 - All question answers **MUST** be replied in the allotted space of **Volume 2**.
- At the end of **Part I of Volume 1** you will find an empty page - you can use it for auxiliary calculations, but this page will not be delivered at the end. This means that all answers **MUST** be replied (and properly justified) in the allotted space of **Volume 2**.
- Each question includes a Portuguese translation of the corresponding text. In case of a mismatch between the English text and its translation, the English text will be the one to be considered in the evaluation¹.
- You cannot use or consult any material during the exam. On your desk you can only have a pen and your student identity card.

¹Cada pergunta inclui uma tradução para Português do referido texto. Em caso de incoerência entre o texto em Inglês e a sua tradução, será o texto em Inglês que será considerado na avaliação.

Volume 1 - Part I

- A. What is the minimum clock period of the following circuit, given the table values (in ns)?
 [Qual é o período de relógio mínimo do seguinte circuito, assumindo os valores da tabela (em ns)?]



[1]: 41
 (4) 50

[2]: 57
 [5]: 49

[3]: 44
 [6]: None of the other options [Nenhuma das outras opções]

$$T_{PD} + \text{NAND} + \text{XOR} + \text{NOR} + T_{SU\ D} = 50\text{ns}$$

- B. Consider the following state transition table with two inputs *Init* and *X*, two outputs *Y1* and *Y0*, where each state $S_i (i = 0, \dots, 3)$ is implemented with D flip-flops, with input D_i (next state) and output Q_i (current state). Select, only for the state S_2 , the correct option for D_2 as a function of *Init* and *X* and the current states Q_i .

[Considere a seguinte tabela de transição de estados com duas entradas *Init* e *X*, duas saídas *Y1* e *Y0*, em que cada estado $S_i (i = 0, \dots, 3)$ é implementado com flip-flops do tipo D, com entradas D_i (próximo estado) e saídas Q_i (estado actual). Indique, para o estado S_2 , a expressão de D_2 como função de *Init* e *X* e os estados actuais Q_i .]

$Q3(n)$	$Q2(n)$	$Q1(n)$	$Q0(n)$	$Init$	X	$Q3(n+1)$	$Q2(n+1)$	$Q1(n+1)$	$Q0(n+1)$	$Y1$	$Y0$
0	0	0	1	0	0	1	0	0	0	0	1
0	0	0	1	0	1	0	1	0	0	1	1
0	0	1	0	0	0	1	0	0	0	0	0
0	0	1	0	0	1	0	0	0	1	1	0
0	1	0	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	1	0	0	1
1	0	0	0	0	0	1	0	0	0	1	1
1	0	0	0	0	1	0	1	0	0	0	0
-	-	-	-	1	-	0	1	0	0	0	0

[1]: $D_2 = X \cdot Q_1 + \bar{X} \cdot Q_2 \cdot Y_0 + X \cdot Q_3$

[3]: $D_2 = X \cdot Q_0 + \bar{X} \cdot Q_2 \cdot Y_1 + X \cdot Q_3 \cdot Y_0$

[5]: $D_2 = Init \cdot (\bar{X} \cdot Q_0 + \bar{X} \cdot Q_2 + X \cdot Q_3)$

[2]: $D_2 = \underline{Init} + \underline{X} \cdot \underline{Q_0} + \bar{X} \cdot \underline{Q_1} + \underline{X} \cdot \underline{Q_2}$

[4]: $D_2 = \underline{Init} + \bar{X} \cdot \underline{Q_0} + \bar{X} \cdot \underline{Q_2} + X \cdot \underline{Q_3}$

[6] None of the other options
 [Nenhuma das outras opções]

C. Represent 10110110_2 in octal.

[Represente 10110110_2 em octal.]

~~[1]~~: 146
[4]: 136

[2]: 246
~~[5]~~: 266

~~[3]~~: 166
[6]: None of the other options [Nenhuma das outras opções]

D. Consider the following circuit with an adder, a register (4 FF's) and a combinational logic circuit. Assuming that the current state is $Q(3:0) = 1010$, what are the next two states of the circuit?

[Considere o seguinte circuito com um somador, um registo (4 FF's) e lógica combinatória. Assumindo que o estado actual é $Q(3:0) = 1010$, quais serão os próximos dois estados do circuito?]

[1]: 0011, 1110

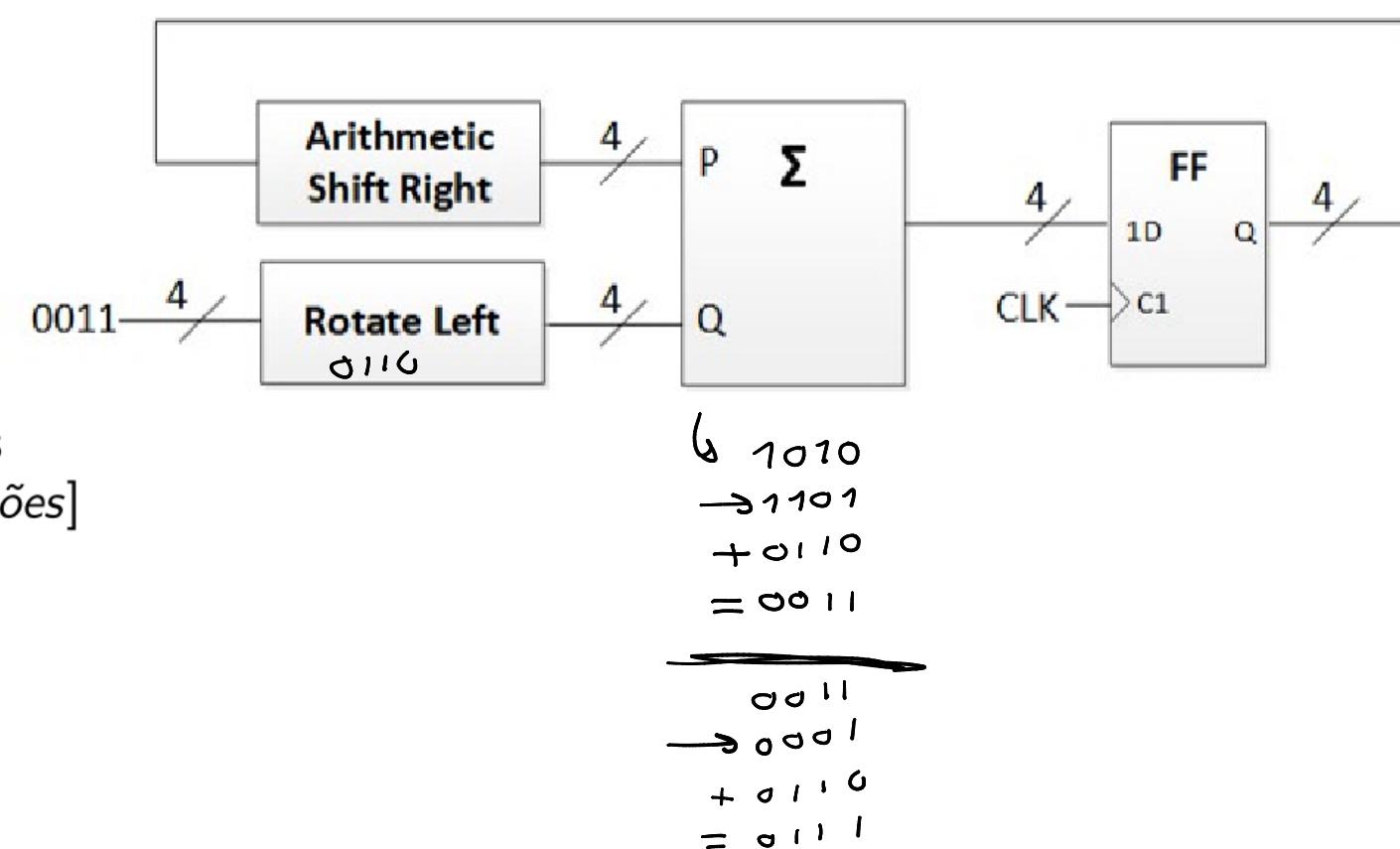
[2]: 1100, 1000

[3]: 0111, 1111

[4]: 1110, 1111

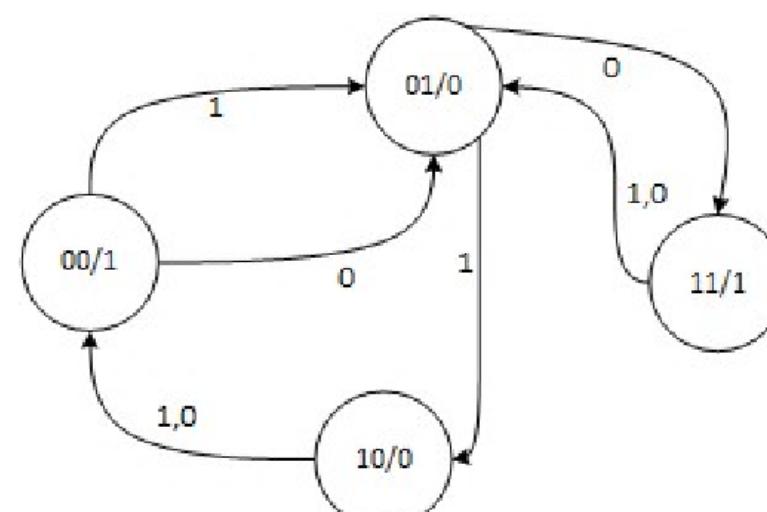
~~[5]~~: 0011, 0111

[6]: None of the other options
[Nenhuma das outras opções]



E. Consider the following state diagram. Select the output value for each state and the value of the next state for each state and input.

[Considere o seguinte diagrama de estados. Indique o valor da saída do circuito para cada estado e o valor do próximo estado para cada valor do estado e entrada.]



$Q(n)$	$Y(n)$	$Q(n+1)$	$Q(n+1)$
		$x=0$	$x=1$
00	1	10	11
01	1	00	10
10	1	10	10
11	1	11	01

[1]

$Q(n)$	$Y(n)$	$Q(n+1)$	$Q(n+1)$
		$x=0$	$x=1$
00	1	01	01
01	0	11	10
10	0	00	00
11	1	01	01

[2]

$Q(n)$	$Y(n)$	$Q(n+1)$	$Q(n+1)$
		$x=0$	$x=1$
00	1	10	01
01	0	11	10
10	1	00	00
11	1	01	01

[3]

$Q(n)$	$Y(n)$	$Q(n+1)$	$Q(n+1)$
		$x=0$	$x=1$
00	0	10	00
01	1	10	11
10	0	10	01
11	1	11	01

[4]

$Q(n)$	$Y(n)$	$Q(n+1)$	$Q(n+1)$
		$x=0$	$x=1$
00	1	10	01
01	0	11	10
10	0	00	00
11	1	01	01

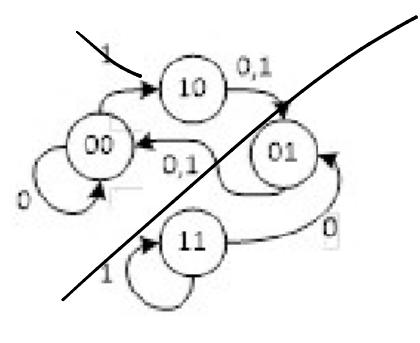
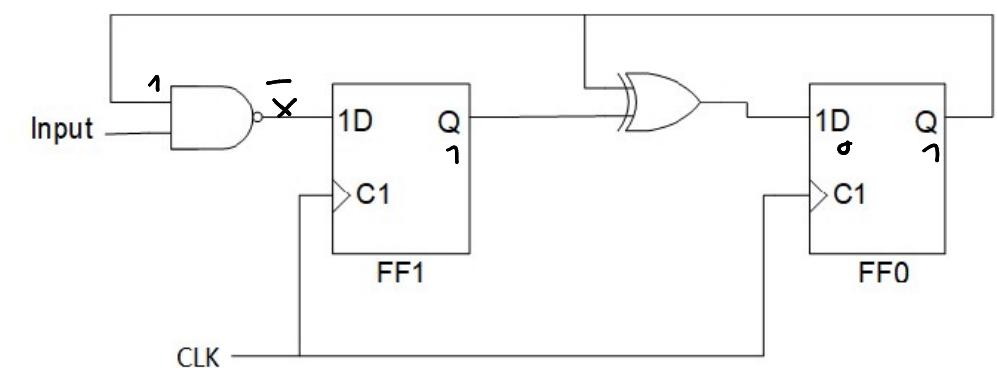
[5]

None of the other options
[Nenhuma das outras opções]

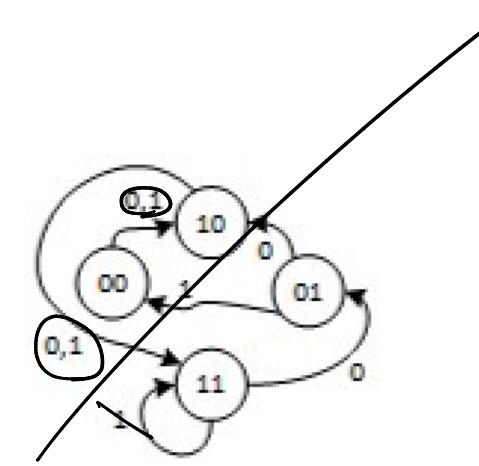
[6]

- F. Consider the following circuit. Which state diagram corresponds to the circuit?

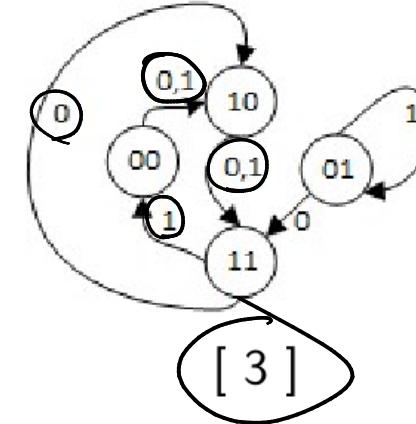
[*Considere o seguinte circuito. Qual dos diagramas de estado corresponde ao funcionamento do circuito?*]



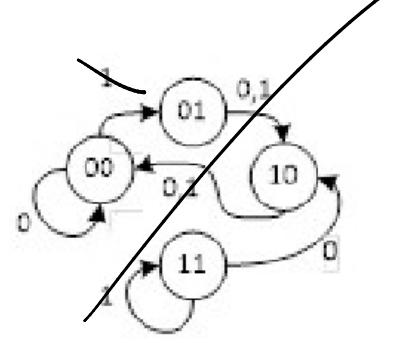
[1]



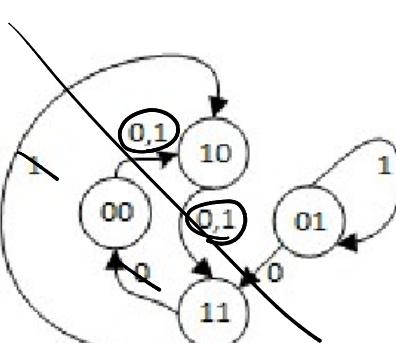
[2]



[3]



[4]



[5]

None of the other options
[*Nenhuma das outras opções*]

[6]

- G. Which function is implemented by the following circuit? Consider that X and Y are 4-bit signed numbers (two's complement).

[*Qual é a função desempenhada pelo seguinte circuito? Assuma que X e Y são números com sinal com 4-bits (em complemento para dois).*]

[1]: $K=0: Z=X-1 ; K=1: Z=X+Y$

[2]: $K=0: Z=X+1 ; K=1: Z=X-Y$

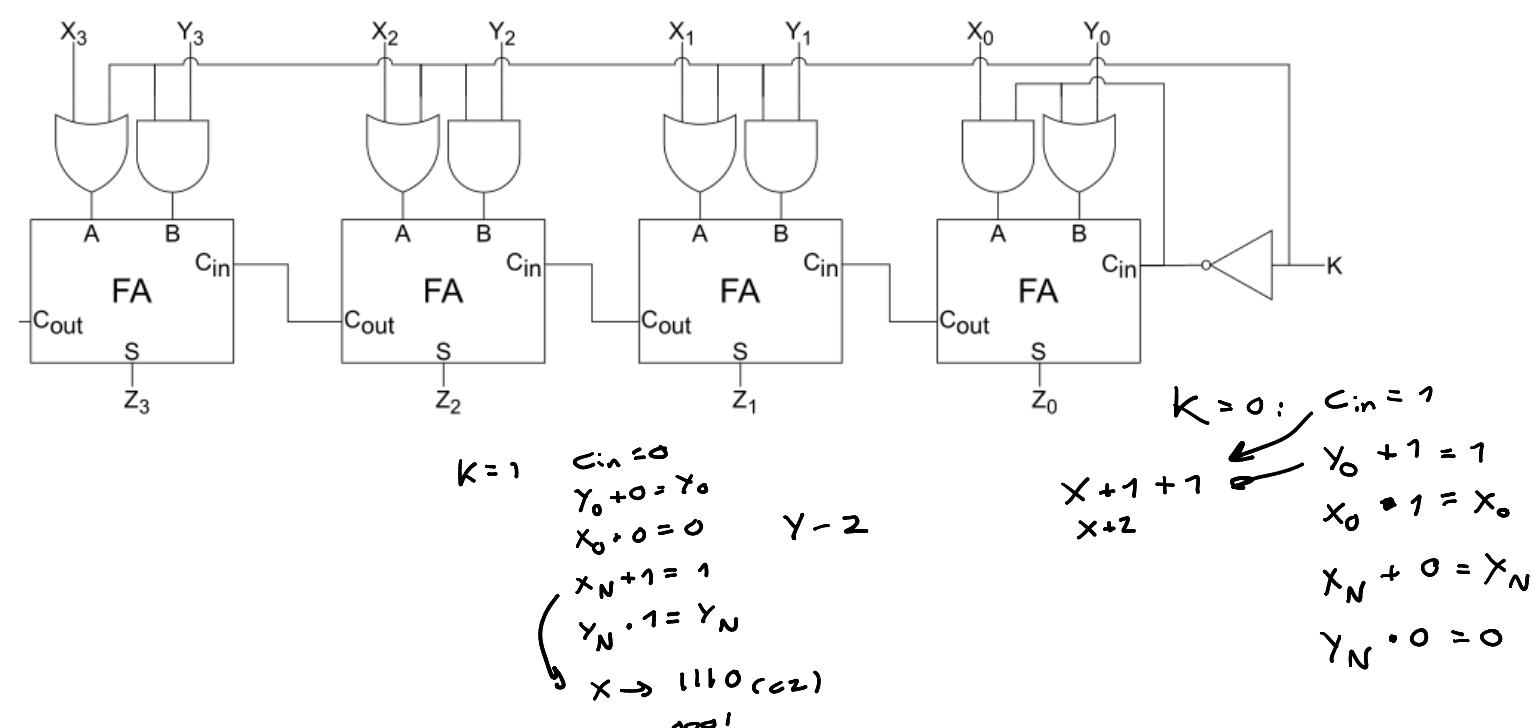
[3]: $K=0: Z=X-Y ; K=1: Z=Y+1$

[4]: $K=0: Z=X+Y ; K=1: Z=Y-1$

[5]: $K=0: Z=X+2 ; K=1: Z=Y-2$

[6]: None of the other options

[*Nenhuma das outras opções*]



- H. Which of the following expressions corresponds to the minimal function (defined as a product-of-sums) represented in the Karnaugh-map?

[*Qual das seguintes expressões corresponde à função mínima (definida como um produto de somas) representada no mapa de Karnaugh?*]

[1]: $(A + \bar{D})(\bar{A} + D)(B + \bar{D})$

[2]: $(\bar{B} + D)(A + \bar{C})(\bar{B} + \bar{D})$

[3]: $(\bar{A} + C)(\bar{B} + \bar{D})(C + \bar{A})$

[4]: $(A + \bar{B})(\bar{B} + D)(\bar{B} + \bar{A})$

[5]: $(B + \bar{C})(\bar{B} + D)(C + \bar{D})$

[6]: None of the other options

- I. Represent $C9_{16}$ in base 10.
[Represente $C9_{16}$ na base 10.]

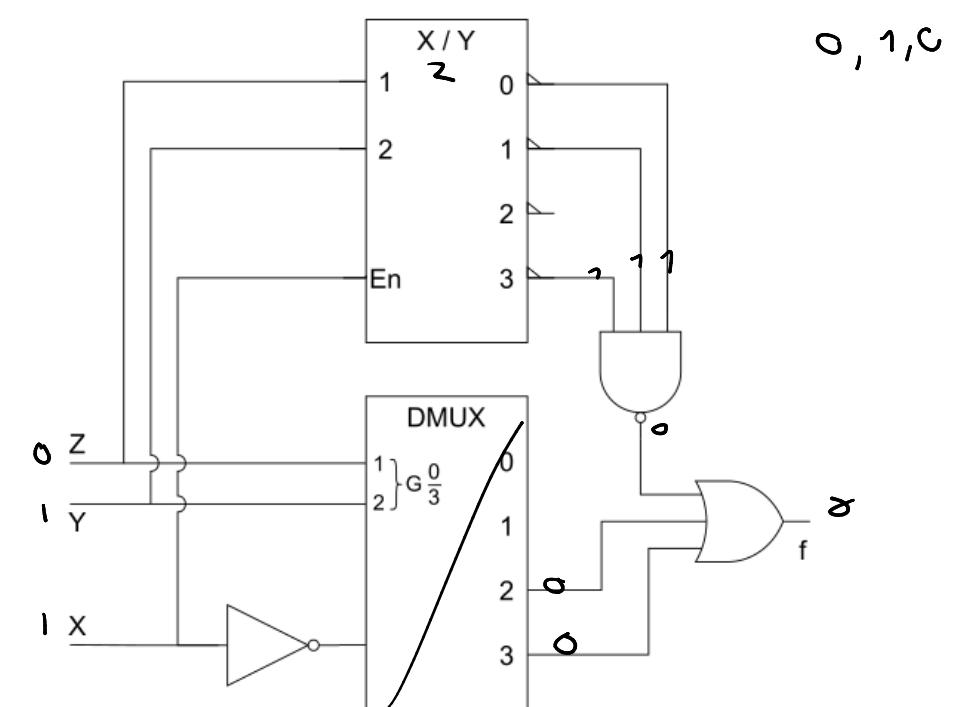
$$\begin{array}{ll} [1]: 181 & \begin{array}{l} 12 \\ \cdot 16 \\ \hline 192 \\ 221 - 192 \\ \hline 29 \\ 9 + 12 \cdot 16 \\ \hline 192 + 9 = 201 \end{array} \\ [4]: 221 & \text{[5]}: 201 \end{array}$$

- [3]: 215
[6]: None of the other options [Nenhuma das outras opções]

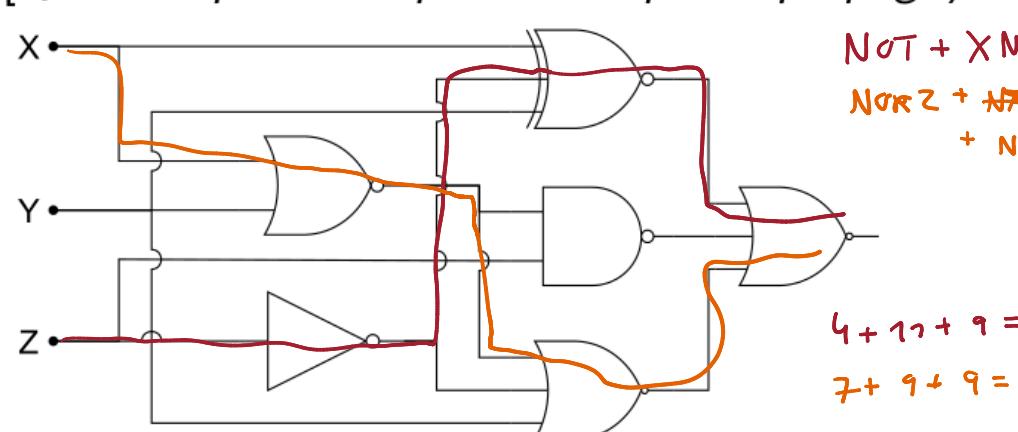
- J. Select the option corresponding to the output $f(X, Y, Z)$ of the circuit shown below, when the inputs (X, Y, Z) have the values $(0, 0, 1), (0, 1, 1)$, and $(1, 1, 0)$.

[Indique qual das opções corresponde à saída $f(X, Y, Z)$ do circuito apresentado em baixo, quando as entradas (X, Y, Z) tomam os valores $(0, 0, 1), (0, 1, 1)$, e $(1, 1, 0)$.]

- [1]: $\{f(0, 0, 1); f(0, 1, 1); f(1, 1, 0)\} = \{0; 1; 0\}$
 [2]: $\{f(0, 0, 1); f(0, 1, 1); f(1, 1, 0)\} = \{1; 0; 1\}$
 [3]: $\{f(0, 0, 1); f(0, 1, 1); f(1, 1, 0)\} = \{1; 0; 0\}$
 [4]: $\{f(0, 0, 1); f(0, 1, 1); f(1, 1, 0)\} = \{0; 0; 1\}$
 [5]: $\{f(0, 0, 1); f(0, 1, 1); f(1, 1, 0)\} = \{0; 1; 1\}$
 [6]: None of the other options [Nenhuma das outras opções]



- K. What is the worst case for the propagation time of the following circuit?
[Qual é o pior caso para o tempo de propagação do seguinte circuito?]



$$\begin{aligned} & \text{NOT} + X \text{NOR3} + \text{NOR3} \\ & \text{NOR2} + \text{NAND2} \\ & + \text{NOR3} + \text{NOR3} \\ & 4 + 11 + 9 = 24 \\ & 7 + 9 + 9 = 25 \end{aligned}$$

Gate	tp [ns]
NOT	4
NAND2	8
NOR2	7
NOR3	9
XNOR3	11

- [1]: 26
[4]: 28

- [3]: 25

- [6]: None of the other options [Nenhuma das outras opções]

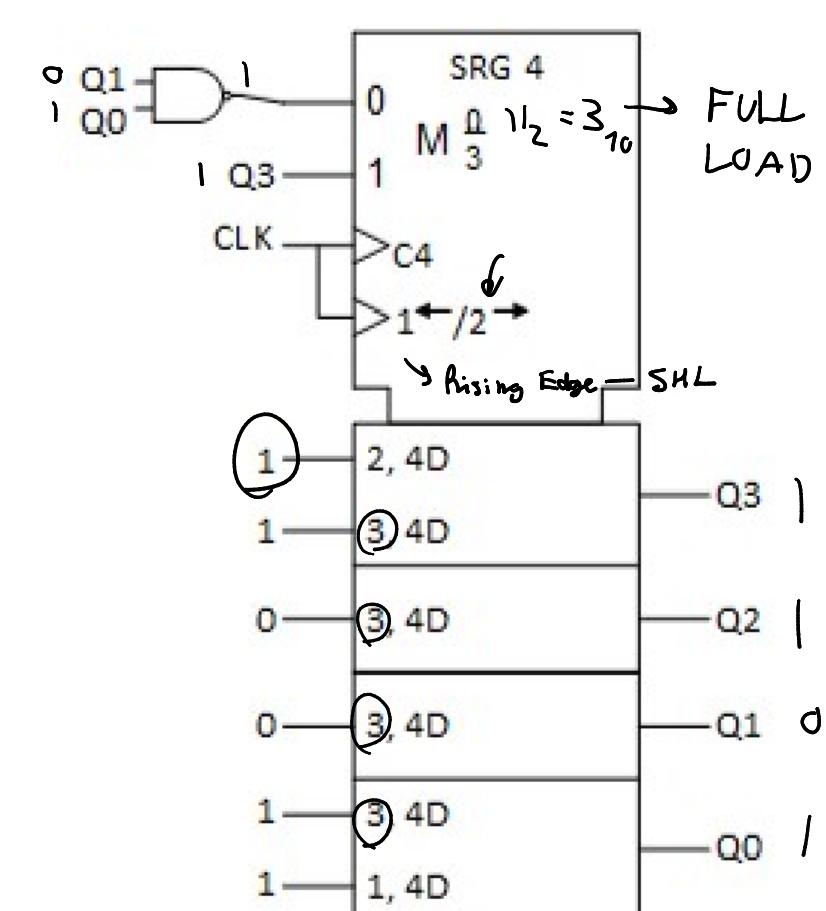
- L. Consider the following circuit with a 4-bit shift register, as depicted in the figure. The current state is $Q_3 Q_2 Q_1 Q_0 = 1011$. What are the next two states of the circuit?

[Considere o seguinte circuito com um registo de deslocamento de 4-bits representado na figura. O estado actual é $Q_3 Q_2 Q_1 Q_0 = 1011$. Quais serão os próximos dois estados?]

- [1]: 1010, 0110
 [2]: 1011, 0110
 [3]: 1001, 1001
 [4]: 1001, 1100
 [5]: 0011, 1111

- [6]: None of the other options
[Nenhuma das outras opções]

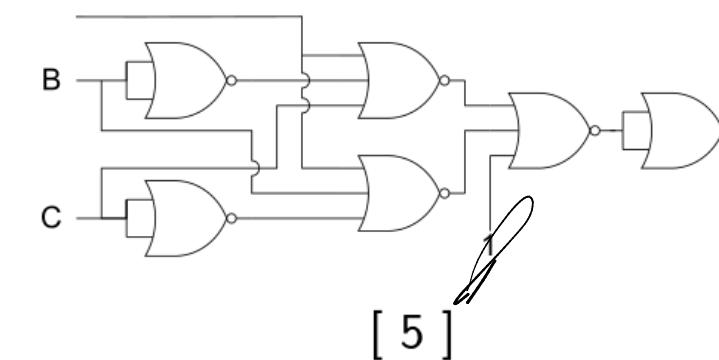
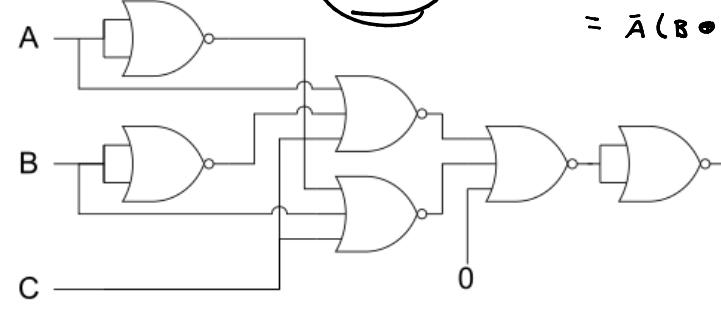
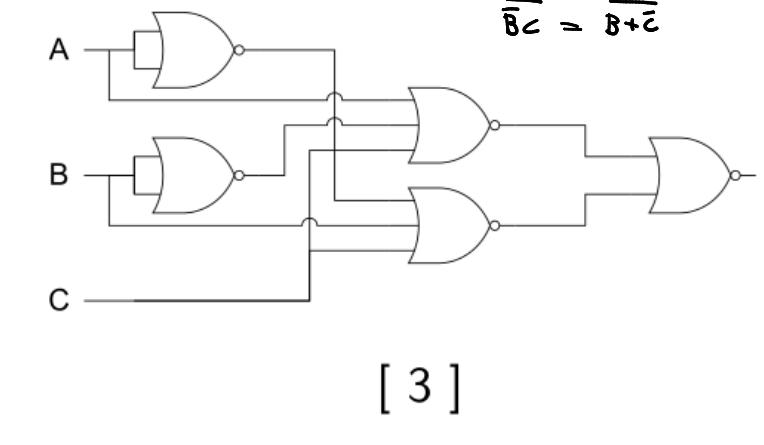
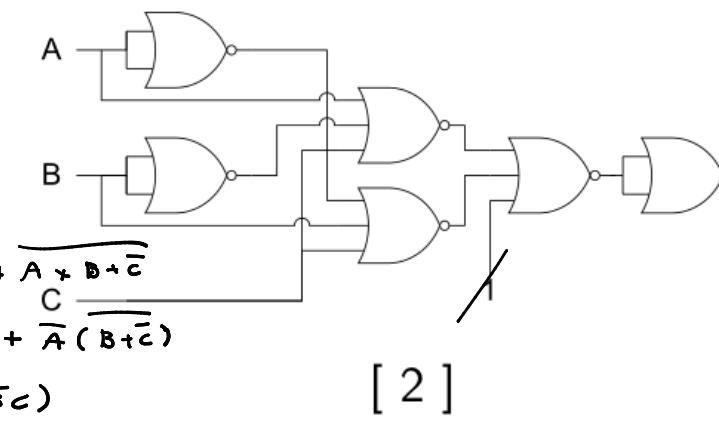
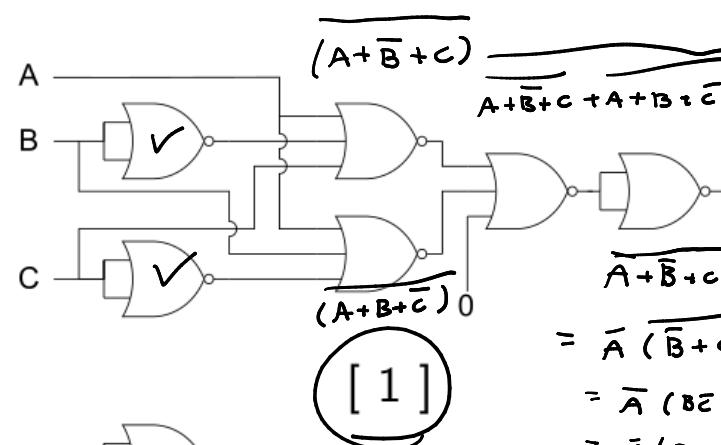
$$\begin{array}{c} \rightarrow 1011 \\ \text{LOAD } 1101 \\ \hline 1101 \\ \text{F.LOAD } 1001 \end{array}$$



M. Which of the following circuits implements the expression $\overline{A} \cdot (\overline{B} \oplus C)$? [Qual dos seguintes circuitos implementa a expressão $\overline{A} \cdot (\overline{B} \oplus C)$?]

$$\overline{A} \cdot (\overline{B} \overline{C} + \overline{B} C) = A + (\overline{B} \overline{C} + B \overline{C}) = A + \overline{B} + C + B \overline{C}$$

$$\overline{B} \overline{C} = \overline{B} + \overline{C}$$

$$\overline{B} C = B + \overline{C}$$


None of the other options
[Nenhuma das outras opções]

[6]

N. Consider the following circuit and truth table. Select the multiplexer inputs $\{X_3; X_2; X_1; X_0\}$ that result in the given truth table.

[Considere o seguinte circuito e tabela de verdade. Selecione as entradas do multiplexer $\{X_3; X_2; X_1; X_0\}$ que resultam na tabela apresentada.]

[1]: $\{X_3; X_2; X_1; X_0\} = \{\overline{C}; 0; C; C\}$

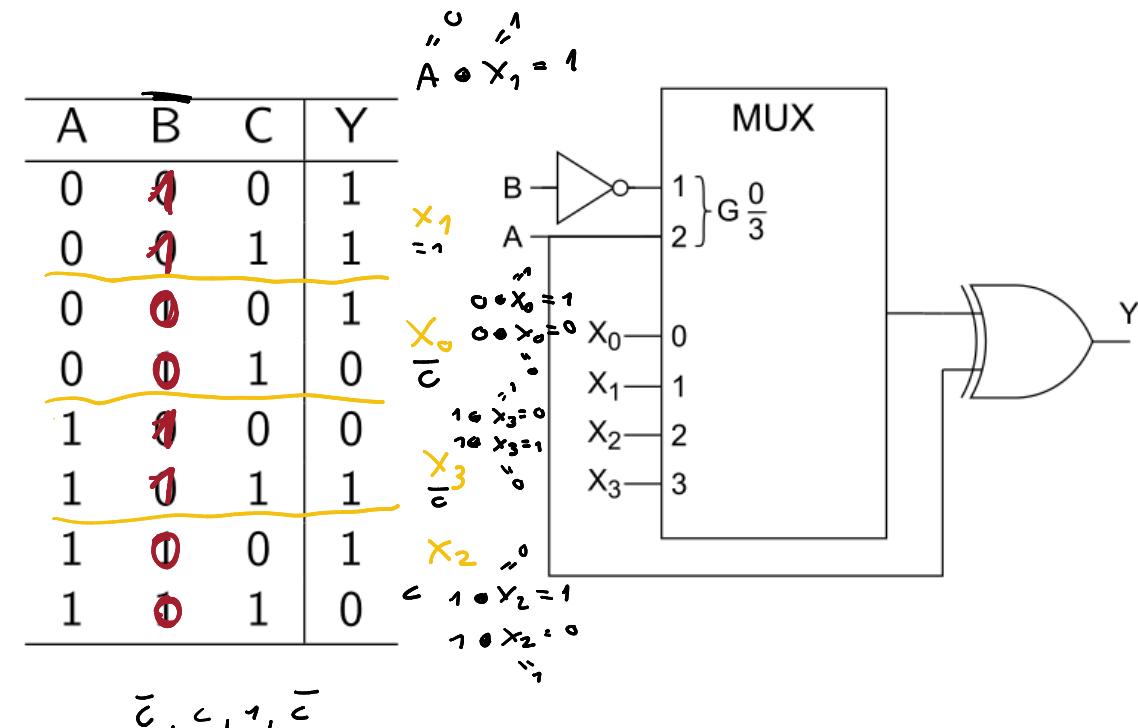
[2]: $\{X_3; X_2; X_1; X_0\} = \{C; \overline{C}; 1; C\}$

[3]: $\{X_3; X_2; X_1; X_0\} = \{\overline{C}; 1; C; \overline{C}\}$

[4]: $\{X_3; X_2; X_1; X_0\} = \{C; \overline{C}; 1; \overline{C}\}$

[5]: $\{X_3; X_2; X_1; X_0\} = \{\overline{C}; C; 1; \overline{C}\}$

[6]: None of the other options
[Nenhuma das outras opções]



O. Consider the following memory system. Indicate the range of addresses that correspond to RAM and EPROM.

[Considere o seguinte sistema de memória. Indique os intervalos de endereços que correspondem a RAM e EPROM.]

[1]: RAM:B000h..EFFFh; EPROM:1000h..2FFFh

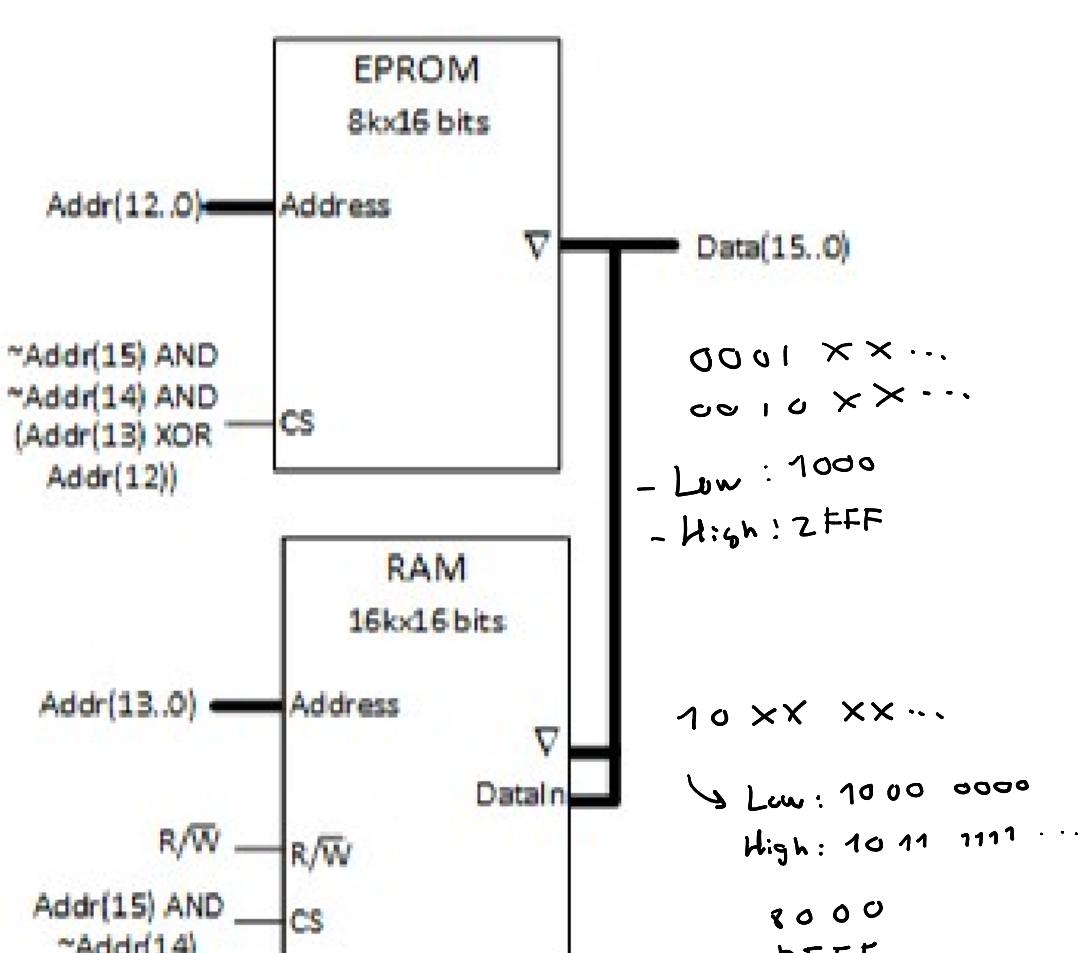
[2]: RAM:B000h..EFFFh; EPROM:2000h..3FFFh

[3]: RAM:8000h..BFFFh; EPROM:2000h..3FFFh

[4]: RAM:8000h..BFFFh; EPROM:1000h..2FFFh

[5]: RAM:C000h..FFFFh; EPROM:1000h..2FFFh

[6]: None of the other options
[Nenhuma das outras opções]



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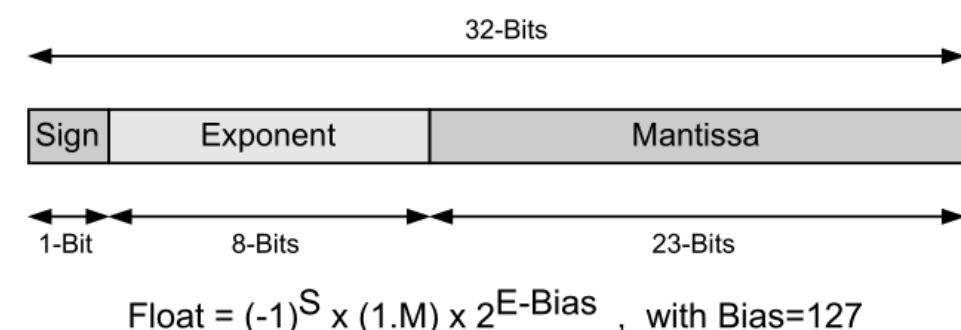
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- P. The following 32-bit words correspond to signed rational numbers represented in fixed-point and floating-point. Which of the options presented below corresponds to an ascending ordering of these words?

[As seguintes palavras de 32-bits correspondem a números racionais com sinal representados em vírgula fixa e em vírgula flutuante. Qual das opções corresponde à ordenação crescente destas palavras?]

$$A = 3FB70A3Dh \text{ (IEEE-754)} \quad B = C8000000h \text{ (Q2.30)} \quad C = 30000000h \text{ (Q1.31)}$$

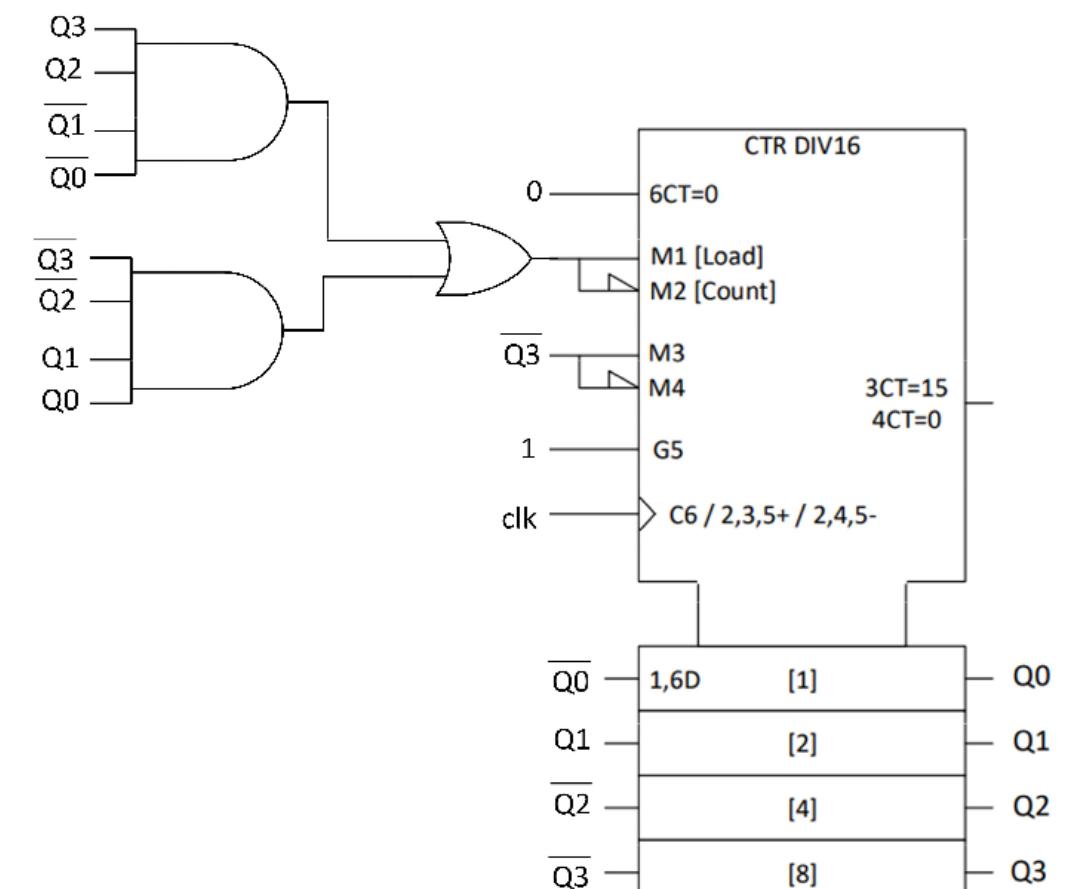
- [1]: A,C,B [2]: A,B,C [3]: B,A,C
 [4]: C,A,B [5]: B,C,A [6]: C,B,A



- Q. Which of the following options corresponds to the sequence, in stationary mode, in decimal format at the output of the circuit in the figure below? (suggestion: start by analyzing a "load" situation.)

[Qual das seguintes opções corresponde à sequência de saída do seguinte circuito, em regime estacionário e em formato decimal? (sugestão: comece por analisar a situação de carregamento ("load") de dados.)]

- [1]: ... 12 - 1 - 2 - 3 - 14 - 13 - 12 ...
 [2]: ... 13 - 5 - 4 - 3 - 11 - 12 - 13 ...
 [3]: ... 11 - 3 - 4 - 5 - 13 - 12 - 11 ...
 [4]: ... 10 - 7 - 6 - 5 - 8 - 9 - 10 ...
 [5]: ... 14 - 3 - 2 - 1 - 12 - 13 - 14 ...
 [6]: None of the other options
 [Nenhuma das outras opções]



- R. What is the 8-bit two's complement representation of -51 ?

[Qual é a representação em complemento para dois com 8-bits de -51 ?]

- [1]: 11001100 [2]: 11001110 [3]: 00110001
 [4]: 10110001 [5]: 11001101 [6]: None of the other options [Nenhuma das outras opções]

(This space was intentionally left blank for your auxiliary calculations.)

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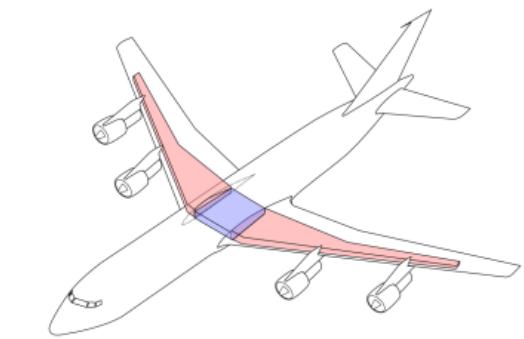
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Volume 1 - Part II**NOTE:** Portuguese version in the following page

[Question score partitioning: 33% + 34% + 33%]

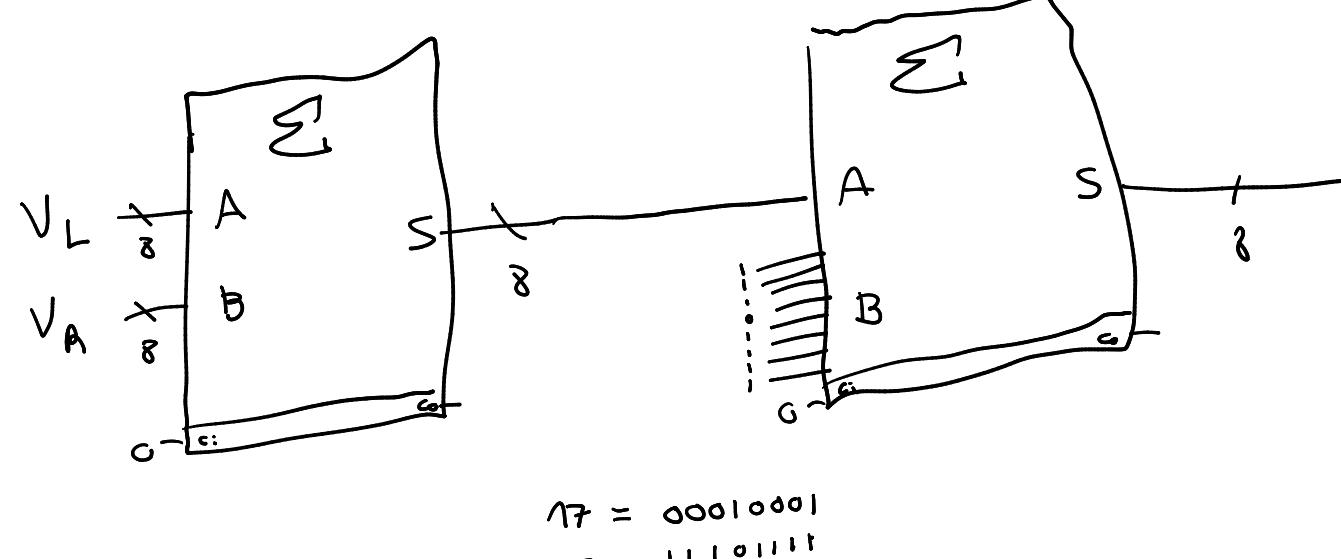
The amount of fuel stored in the two tanks located on the left and right wings of an aircraft is an important safety parameter not only when taking off (since the weight of the fuel makes it difficult for the plane to climb) but also during flight (to ensure that the plane arrives at its destination). Each of these tanks has a sensor that indicates the amount of fuel stored (in thousands of liters), respectively V_L and V_R , with an 8-bit precision. From this value it is necessary to subtract a correction term associated with the deformation of the wings, with a constant value corresponding to 8500 liters (in each wing).



NOTE: In questions (1) and (2) consider the utilization of 8-bit adders; in question (3) consider the utilization of 4-bit adders. Assume an 8-bit precision in all intermediate calculations and try to minimize the amount of hardware resources as much as possible.:.

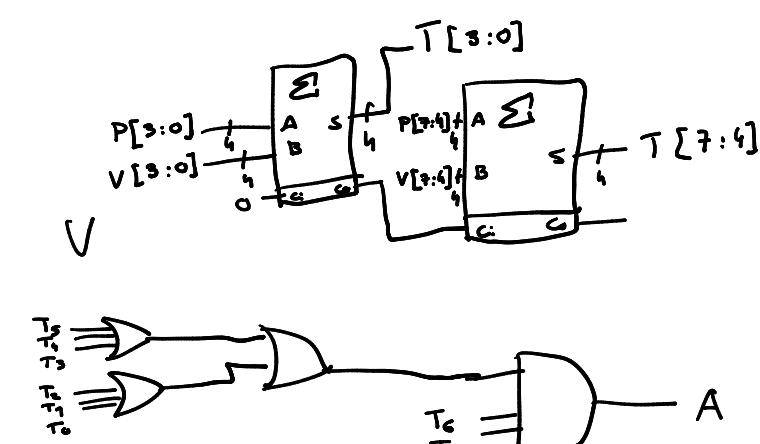
1. Design the circuit that calculates the amount (V) of fuel onboard (in thousands of liters).
2. By taking into account that the Jet-A1 gasoline density is approximately 0.75 kg/liter, implement a circuit that calculates the weight of the fuel (J) onboard (in tons).
Hint: remember that $0.75 = \frac{3}{4}$.
3. To support the crew in its decision-making, the handling team informs the pilot about the total weight (luggage + passengers) onboard (P , measured in tons). Considering that the maximum load allowed at take-off is 192 tons, implement a circuit that activates an alarm (A) to prevent the aircraft from operating when the total loaded load (including fuel) exceeds the allowed threshold.
Attention: to answer this line you should use 4-bits adders.
Hint: remember that $192 = 128 + 64$.

$$\textcircled{1} \quad V = V_L + V_R + \underbrace{Z \cdot 8500}_{17000}$$

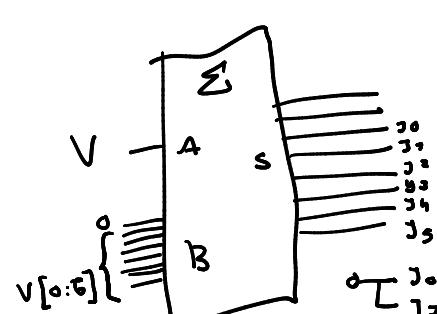


$$\textcircled{3} \quad T = P + V$$

$$A = T_7 T_6 (T_5 + T_4 + T_3 + T_2 + T_1 + T_0)$$



$$\textcircled{2} \quad J = V \cdot \frac{3}{4} = (2V + V) \cdot 2^{-2} = (V \ll 1 + V) \gg 2$$

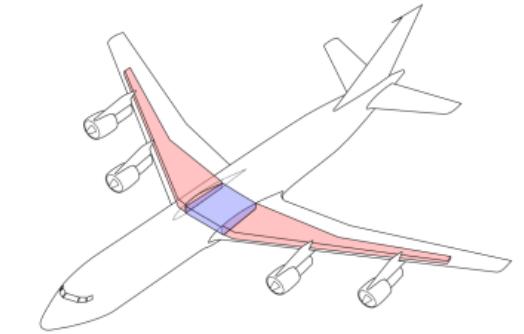


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A quantidade de combustível armazenada nos dois tanques localizados nas asas esquerda e direita de uma aeronave é um importante parâmetro de segurança não só aquando da sua descolagem (pois o peso do combustível dificulta a subida do avião) mas também durante o voo (para garantir que o avião chega ao seu destino). Cada um destes tanques dispõe de um sensor que indica a quantidade de combustível armazenado (em milhares de litros), respectivamente V_L e V_R , com uma precisão de 8-bits. A este valor é necessário subtrair uma correção associada à deformação das asas, de valor constante e correspondente a 8500 litros (em cada asa).



NOTA: Nas perguntas (1) e (2) considere a utilização de somadores de 8-bits; na pergunta (3) considere a utilização de somadores de 4-bits. Assuma uma precisão de 8-bit em todos os cálculos intermédios e procure minimizar os recursos de hardware utilizados:

1. Projecte o circuito que calcula a quantidade total (V) de combustível disponível (em milhares de litros).
2. Tendo em conta que a densidade da gasolina Jet-A1 é de aproximadamente 0.75 kg/litro, implemente um circuito que calcula o peso do combustível (J) a bordo (em toneladas).
Sugestão: lembre-se que $0.75 = \frac{3}{4}$.
3. Para apoiar a tripulação nas tomadas de decisão, a equipa de *handling* transmite ao piloto o peso total (porão + passageiros) embarcado (P , medido em toneladas). Considerando que a carga máxima permitida na descolagem é de 192 toneladas, implemente um circuito que active um alarme (A) de modo a impedir a operação do avião quando a carga total embarcada (contando com o combustível) excede o limiar permitido.
Atenção: para responder a esta alínea deve utilizar somadores de 4-bits.
Sugestão: lembre-se que $192 = 128 + 64$.

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Volume 1 - Part III**NOTE:** Portuguese version in the following page

[Question score partitioning: 50% + 50%]

Design a circuit that controls the gate of an aircraft hangar. The gate operates vertically, with the electromechanical device located above the entrance. The control mechanism of the gate works as follows:



- All the signals are Active High.
- Input signal S1 indicates that the gate is completely open. Input signal S2 indicates that the gate is completely closed. Input signal S3 indicates that an object was detected in the middle of the entrance.
- Output signals A1 and A2 respectively cause the electromechanical device to raise or lower the gate. The movement of the gate requires that one and only one of the signals A1 or A2 is active, otherwise the mechanism stops.
- The remote control can select between two modes of operation, manual or auto, which correspond to the input signals MA and AU, respectively, in the control circuit. In order to change the mode of operation, the gate must be closed, it being enough that the respective signal is active during a single clock cycle. MA has priority over AU.
- The remote control also generates input signals UP and DN, to trigger raising or lowering of the gate, respectively. The effect of these signals depends on the mode of operation. UP and DN have priority over MA and AU.
- In auto mode, activation of the UP signal (at least one clock cycle) will trigger the raising of the gate, which will only stop when the gate is completely open. After this, a timer will start (the transition of signal AT to active status starts the timer), and, once it expires (activation of input signal TR), the gate will automatically start to lower. Lowering of the gate will continue until the gate is completely closed, or signal S3 is detected active (at least one clock cycle). In this later case, raising is automatically triggered as if the UP signal had been generated. In auto mode, the DN button has no action associated.
- In manual mode, the UP and DN signals must be continuously active in order to move the gate up or down, respectively. Once the UP signal is active, it must be first deactivated to allow DN to have effect, and vice versa.
- In the initial state, the gate is closed, and operating in auto mode.

Consider the incomplete state diagram of the Moore machine of the circuit (see Volume 2, Part III).

Complete the diagram, defining the values of the input signals associated with all state transitions, as well as the values of the output signals associated with each state. "Don't cares" must be used for the inputs whose value does not matter for given a state transition. In the diagram, indicate the inputs/outputs according to the following order:

- Order of the inputs: TR, S1, S2, S3, MA, AU, UP, DN.
- Order of the outputs: A1, A2, AT.

Question B:

The state transition table on the right describes the behavior of a machine with 4 states, one input E and one output Y. A circuit that implements it using two flip-flops of type D (FF0 and FF1), as well as AND, OR and NOT gates, is to be projected. Obtain the logical expressions (in minimal form) for the flip-flop input signals, as well as the output of the circuit.

Q1(n)	Q0(n)	E	Q1(n+1)	Q0(n+1)	Y
0	0	0	1	0	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	0	1
1	0	0	0	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	0	0

Pergunta A:

Projecte um circuito para controlar o portão do *hangar* de uma aeronave. O portão abre e fecha verticalmente, estando o dispositivo eletro-mecânico localizado na parte de cima da entrada. O mecanismo de controlo funciona da forma seguinte:



- Todos os sinais são Ativos a High.
- O sinal de entrada S1 indica que o portão está completamente aberto. O sinal de entrada S2 indica que o portão está completamente fechado. O sinal S3 indica que um objecto foi detectado na entrada do portão.
- Os sinais de saída A1 e A2, fazem com que o dispositivo eletro-mecânico eleve ou baixe o portão, respetivamente. O movimento do portão só ocorre se um e apenas um dos sinais A1 ou A2 estiver ativo, caso contrário o mecanismo pára o movimento.
- O controlo remoto pode selecionar um entre dois modos de funcionamento, manual ou automático, o que corresponde à geração dos sinais de entrada MA e AU, respetivamente. Para que se possa alterar o modo de funcionamento, o portão tem de estar fechado, bastando que o respetivo sinal fique ativo durante um ciclo de relógio. MA tem prioridade sobre AU.
- O controlo remoto também gera sinais UP e DN, para despoletar a elevação e abaixamento do portão. O efeito destes sinais depende do modo de funcionamento. UP e DN têm prioridade sobre MA e AU.
- No modo automático, a ativação do sinal UP (pelo menos um ciclo de relógio) irá despoletar a elevação do portão, a qual irá parar uma vez que o portão esteja completamente aberto. Depois disso, um temporizador irá arrancar (o arranque é despoletado pela transição do sinal AT para ativo), e, uma vez que o temporizador expire (ativação do sinal de entrada TR), o portão começará automaticamente a baixar. O abaixamento do portão irá continuar até o portão estar completamente fechado, ou até o sinal S3 ficar ativo (pelo menos um ciclo de relógio). Neste último caso, a elevação do portão recomeça automaticamente, como se o sinal UP tivesse sido gerado. No modo automático, o sinal DN não tem nenhuma acção associada.
- No modo manual, os sinais UP e DN têm de estar continuamente ativos para elevar ou baixar o portão, respetivamente. Assim que o sinal UP fica ativo, tem de ser primeiro desativado para que DN possa ter efeito, e vice versa.
- No estado inicial, o portão está fechado e em modo automático.

Considere o diagrama de estados incompleto da máquina de Moore do circuito (ver Volume 2, Parte III). Complete o diagrama, definindo os valores dos sinais de entrada que desencadeiam todas as transições de estado, assim como os valores de saída de cada estado. As "indiferenças" têm de ser obrigatoriamente usadas para entradas que não tenham influência numa determinada transição de estado. As entradas/saídas têm de ser indicadas de acordo com a ordem seguinte:

- Ordem das entradas: TR, S1, S2, S3, MA, AU, UP, DN.
- Ordem das saídas: A1, A2, AT.

Pergunta B:

A tabela de transição de estados à direita descreve uma máquina com 4 estados, uma entrada E e uma saída Y. Projecte o circuito que a implementa utilizando dois flip-flops D (FF0 e FF1), assim como portas AND, OR e NOT. Obtenha as expressões algébricas (na forma mínima) para os sinais de entrada dos flip-flops, assim como da saída do circuito.

Q1(n)	Q0(n)	E	Q1(n+1)	Q0(n+1)	Y
0	0	0	1	0	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	0	1
1	0	0	0	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	0	0



Don't forget to identify this and the following pages!
Only these pages will be considered for your evaluation.

Volume 2 - Part I

For each question of Part I (question A, B, C, ...), fill in the number of the **correct answer** from the supplied multiple-choice list (answer 1, 2, 3, ...):

1	*	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

NOTE: Leave blank (or fill in with 0) all questions that you do not wish to answer.

Volume 2 - Part II

Number: _____ Name: _____
Degree: LEEC LEAer LEFT

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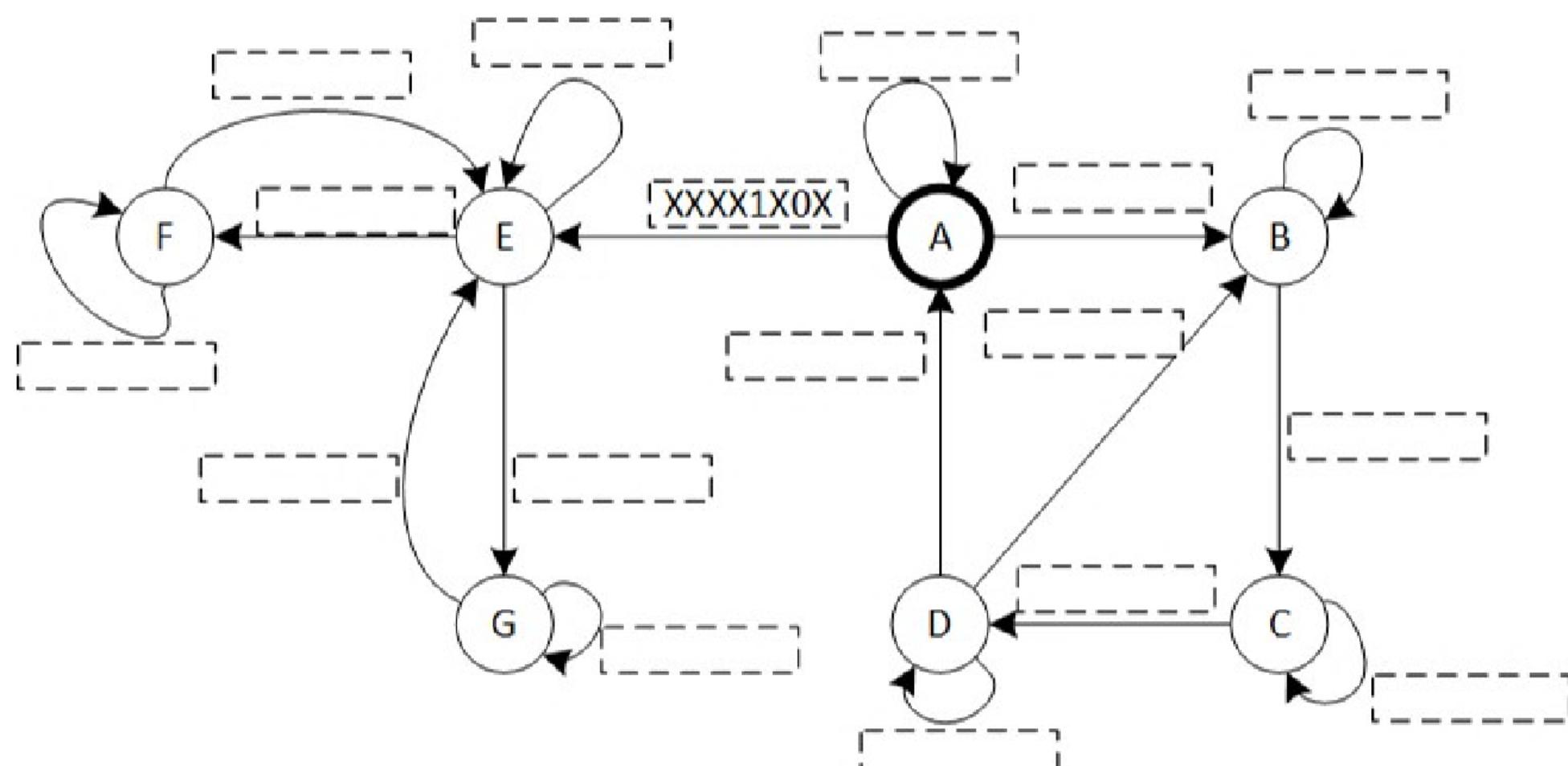
January 27th, 2023

Volume 2 - Part II (Cont.)

Volume 2 - Part III

Meaning of the states [*Significado dos estados*]:

- A: Initial state, auto mode, gate closed [*Estado inicial, modo automático, portão fechado*];
 - B: Auto mode, raising the gate [*Modo automático, elevando o portão*];
 - C: Auto mode, gate fully open [*Modo automático, portão completamente aberto*];
 - D: Auto mode, lowering the gate [*Modo automático, baixando o portão*];
 - E: Manual mode, gate closed [*Modo manual, portão fechado*];
 - F: Manual mode, raising the gate [*Modo manual, elevando o portão*];
 - G: Manual mode, lowering the gate [*Modo manual, baixando o portão*];



For each state, define the values of the inputs (in the diagram) and of the outputs (below) according to the following order:
[Para cada estado, indique os valores das entradas (no diagrama) e das saídas (em baixo) de acordo com a seguinte ordem]:

- Order of the inputs [*Ordem das entradas*]: TR, S1, S2, S3, MA, AU, UP, DN.
 - Order of the outputs [*Ordem das saídas*]: AT, A1, A2.

- A: _____
 - B: _____
 - C: _____
 - D: _____

- E: _____
- F: _____
- G: _____

Number: _____

Name: _____

Degree: LEEC LEAer LEFT

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Volume 2 - Part III (Cont.)

IMPORTANT: Do not forget to identify the previous page.

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Instructions

Before starting the exam, read carefully the following information:

- There are (at least) nine different versions of this exam.
- Although the exam comprises a total of 16 pages, there are two distinct volumes that should be handled as follows:
 - **Volume 1** corresponds to the question list and comprises pages 1 to 12. These pages do not need to be identified because they will be discarded at the end of the exam;
 - **Volume 2** corresponds to the answers sheet and comprises pages 13 to 16. All pages of this volume **MUST** be identified with the **student's name** and **number**.
 - At the end of the exam, all pages of **Volume 2** will be separated. Consequently, all non-identified pages will not be considered.
- The exam is composed of three parts (Part I, II and III) and has a duration of 2 (two) hours.
 - **Part I** comprises N_1 multiple choice questions and awards a total of $P_1 = 15$ points.
 - * Each correct answer awards $C = P_1/N_1$ points;
 - * Each wrong answer awards $W = -C/(A-1)$ points (negative value), where A denotes the number of possible answers offered to each question;
 - * Each non-answered question awards 0 points.
 - **Part II** comprises an open-answer problem about combinatorial circuits and awards a total of $P_2 = 2.5$ points.
 - **Part III** comprises an open-answer problem about sequential circuits and awards a total of $P_3 = 2.5$ points.
 - All question answers **MUST** be replied in the allotted space of **Volume 2**.
- At the end of **Part I of Volume 1** you will find an empty page - you can use it for auxiliary calculations, but this page will not be delivered at the end. This means that all answers **MUST** be replied (and properly justified) in the allotted space of **Volume 2**.
- Each question includes a Portuguese translation of the corresponding text. In case of a mismatch between the English text and its translation, the English text will be the one to be considered in the evaluation¹.
- You cannot use or consult any material during the exam. On your desk you can only have a pen and your student identity card.

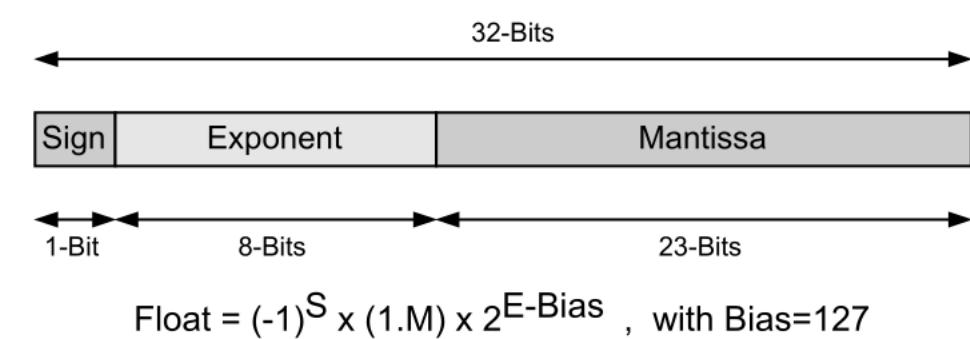
¹Cada pergunta inclui uma tradução para Português do referido texto. Em caso de incoerência entre o texto em Inglês e a sua tradução, será o texto em Inglês que será considerado na avaliação.

Volume 1 - Part I

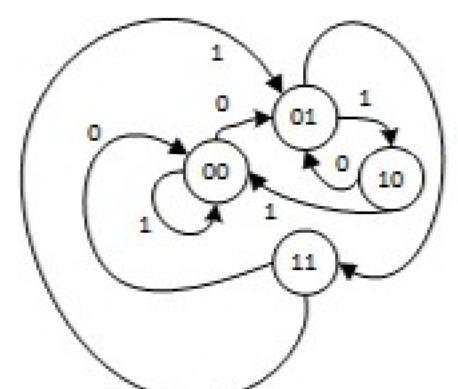
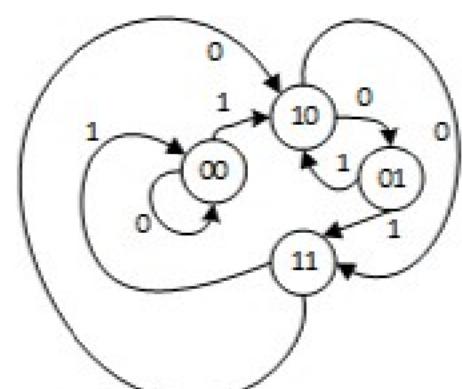
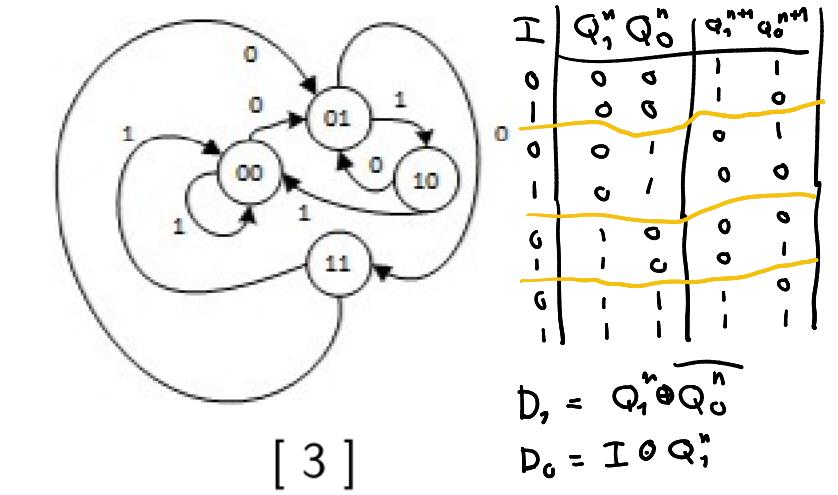
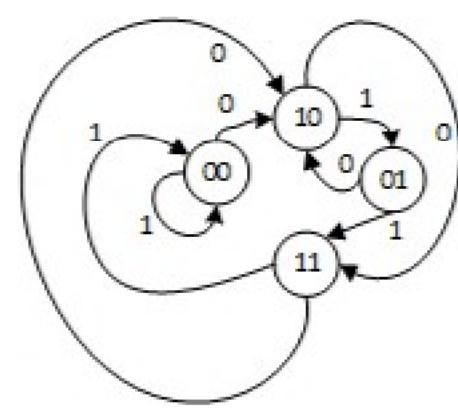
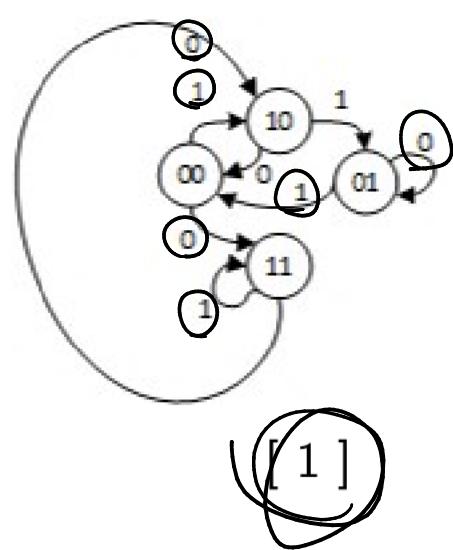
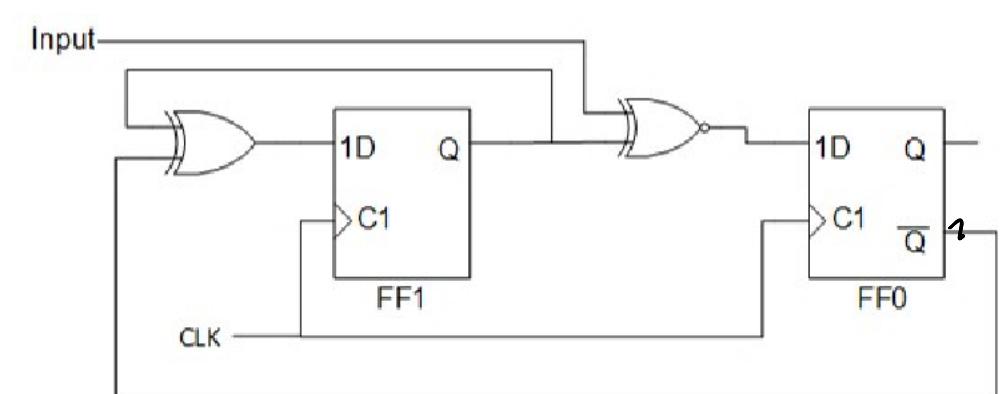
- A. The following 32-bit words correspond to signed rational numbers represented in fixed-point and floating-point. Which of the options presented below corresponds to an ascending ordering of these words?
 [As seguintes palavras de 32-bits correspondem a números racionais com sinal representados em vírgula fixa e em vírgula flutuante. Qual das opções corresponde à ordenação crescente destas palavras?]

$$A = 3FD5C28Fh \text{ (IEEE-754)} \quad B = 77AE147Bh \text{ (Q2.30)} \quad C = C02AE148h \text{ (IEEE-754)}$$

- [1]: A,B,C [2]: B,C,A [3]: B,A,C
 [4]: C,A,B [5]: A,C,B [6]: C,B,A



- B. Consider the following circuit. Which state diagram corresponds to the circuit?
 [Considere o seguinte circuito. Qual dos diagramas de estado corresponde ao funcionamento do circuito?]



None of the other options
 [Nenhuma das outras opções]

[6]

C. Select the option corresponding to the output $f(X, Y, Z)$ of the circuit shown below, when the inputs (X, Y, Z) have the values $(0, 0, 1), (0, 1, 0)$, and $(1, 1, 0)$.

[Indique qual das opções corresponde à saída $f(X, Y, Z)$ do circuito apresentado em baixo, quando as entradas (X, Y, Z) tomam os valores $(0, 0, 1), (0, 1, 0)$, and $(1, 1, 0)$.]

- [1]: $\{f(0,0,1) ; f(0,1,0) ; f(1,1,0)\} = \{1 ; 0 ; 1\}$

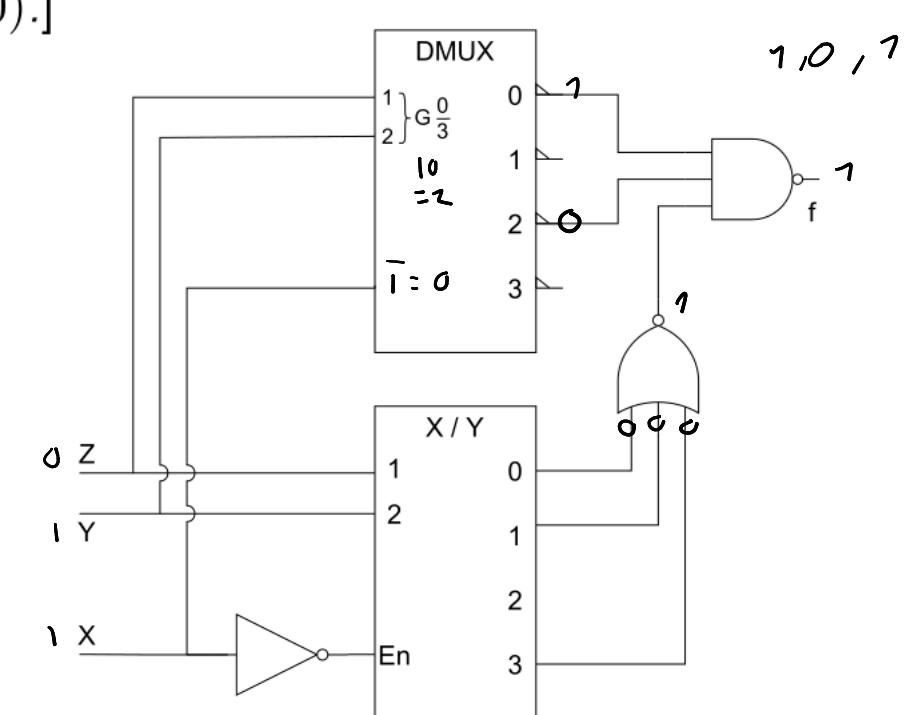
[2]: $\{f(0,0,1) ; f(0,1,0) ; f(1,1,0)\} = \{1 ; 1 ; 0\}$

[3]: $\{f(0,0,1) ; f(0,1,0) ; f(1,1,0)\} = \{0 ; 0 ; 1\}$

[4]: $\{f(0,0,1) ; f(0,1,0) ; f(1,1,0)\} = \{0 ; 1 ; 1\}$

[5]: $\{f(0,0,1) ; f(0,1,0) ; f(1,1,0)\} = \{0 ; 1 ; 0\}$

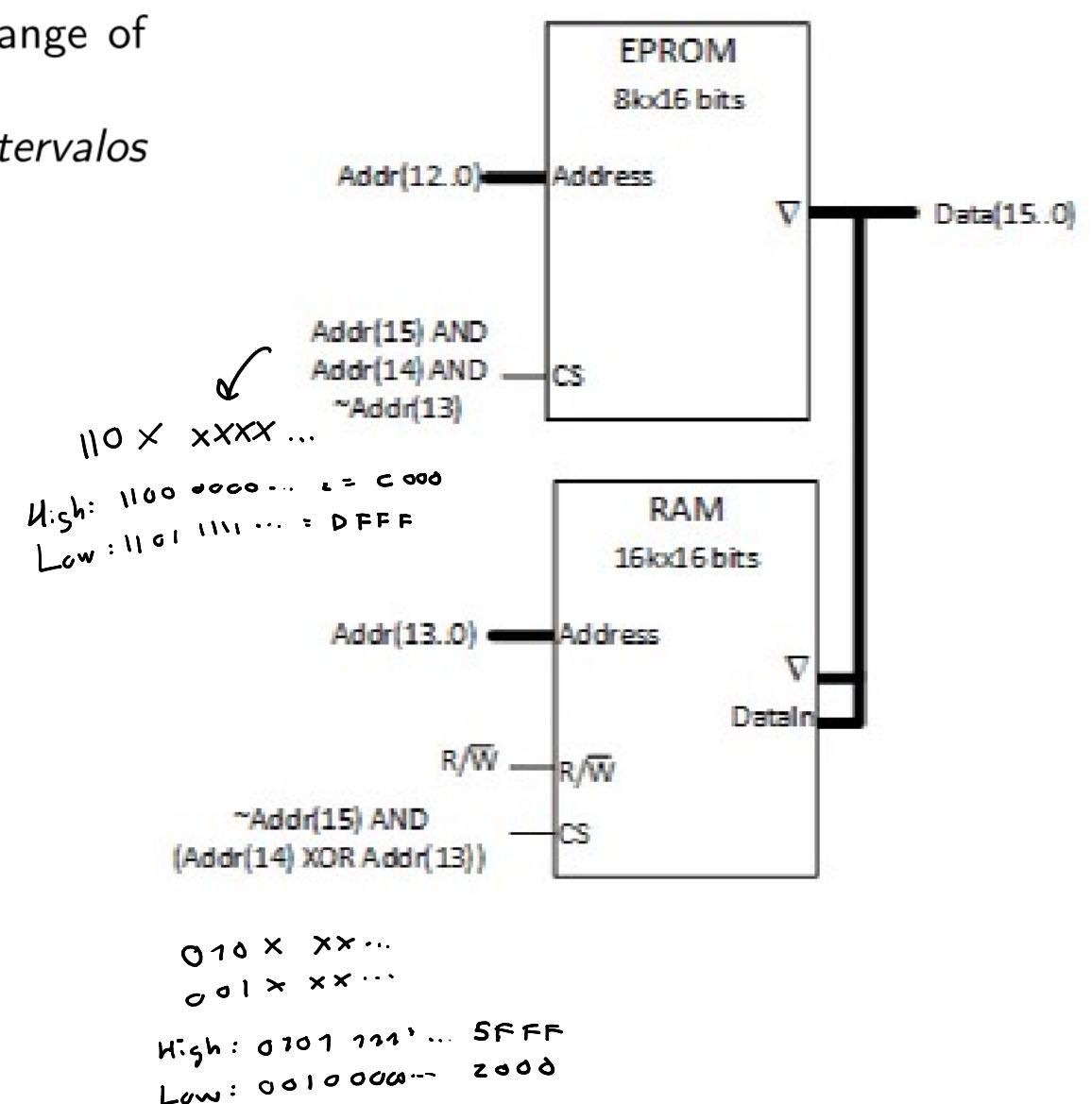
[6]: None of the other options [Nenhuma das outras opções]



D. Consider the following memory system. Indicate the range of addresses that correspond to RAM and EPROM.

[Considere o seguinte sistema de memória. Indique os intervalos de endereços que correspondem a RAM e EPROM.]

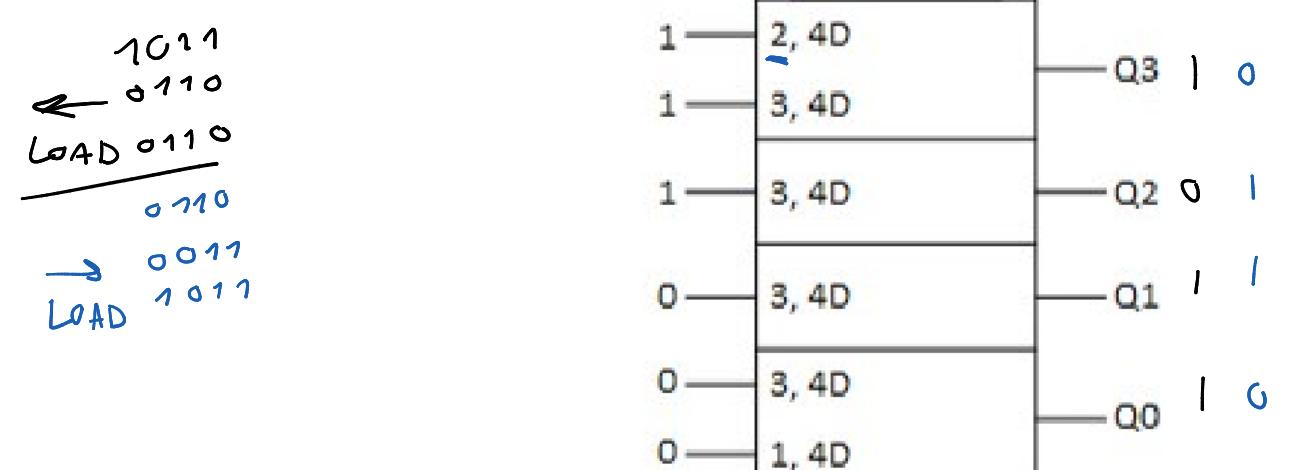
- [1]: RAM:C000h..FFFFh; EPROM:B000h..FFFFh
 - [2]: RAM:8000h..BFFFh; EPROM:2000h..3FFFh
 - [3]: RAM:A000h..5FFFh; EPROM:C000h..DFFFh
 - [4]: RAM:8000h..BFFFh; EPROM:1000h..2FFFh
 - [5]: RAM:4000h..7FFFh; EPROM:B000h..FFFFh
 - [6] None of the other options
[Nenhuma das outras opções]



E. Consider the following circuit with a 4-bit shift register, as depicted in the figure. The current state is $Q_3\ Q_2\ Q_1\ Q_0 = 1011$. What are the next two states of the circuit?

[Considere o seguinte circuito com um registo de deslocamento de 4-bits representado na figura. O estado actual é Q₃ Q₂ Q₁ Q₀ = 1011. Quais serão os próximos dois estados?]

- [1]: 0110, 1011
 - [2]: 1010, 0110
 - [3]: 0011, 1111
 - [4]: 1011, 0110
 - [5]: 1001, 1001
 - [6]: None of the other options
Nenhuma das outras opções



F. Represent $6DE3_{16}$ in octal.

[Represente $6DE3_{16}$ em octal.]

[1]: 31513
 [2]: 37363
 [4]: 65633

[5]: 66743

[3]: 46723

[6]: None of the other options [Nenhuma das outras opções]

G. What is the 8-bit two's complement representation of -49 ?

[Qual é a representação em complemento para dois com 8-bits de -49 ?]

[1]: 11010000
 [4]: 11001110

[2]: 11001111
 [5]: 00110001

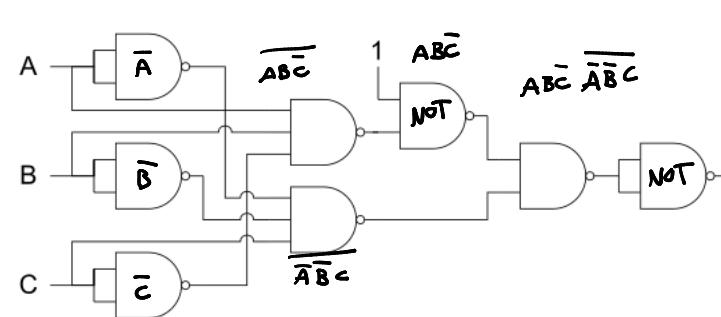
[3]: 10110001

[6]: None of the other options [Nenhuma das outras opções]

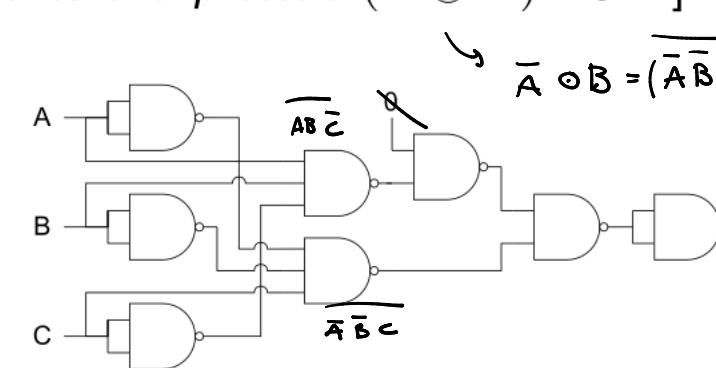
$$\begin{array}{r} 49 \rightarrow 00110001 \\ -49 \rightarrow 11001110 \\ +1 \quad 11001111 \end{array}$$

H. Which of the following circuits implements the expression $(\overline{A} \odot B) \cdot \overline{C}$?

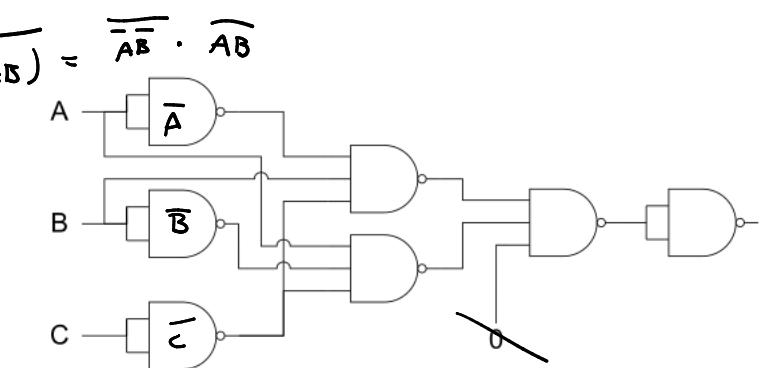
[Qual dos seguintes circuitos implementa a expressão $(\overline{A} \odot B) \cdot \overline{C}$?]



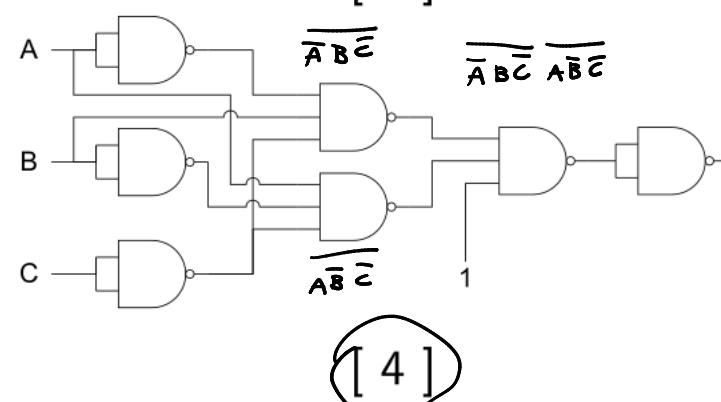
[1]



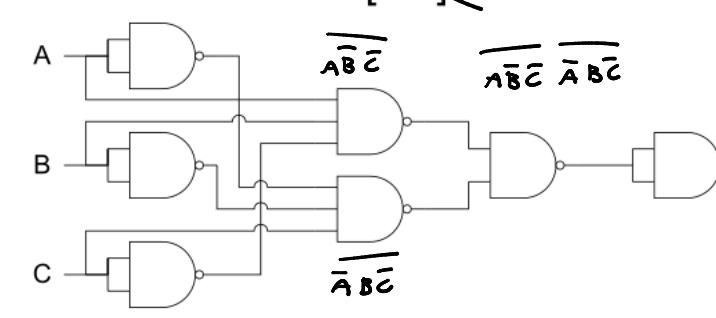
[2]



[3]



[4]



[5]

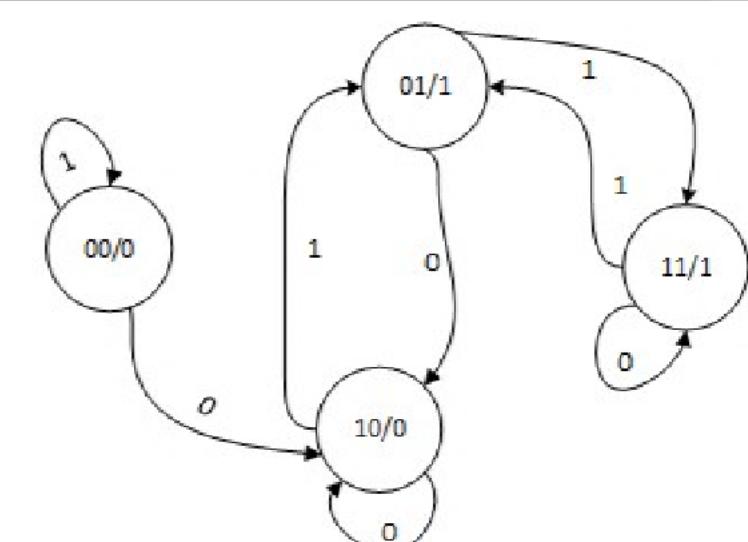
None of the other options
 [Nenhuma das outras opções]

[6]

I.

Consider the following state diagram. Select the output value for each state and the value of the next state for each state and input.

[Considere o seguinte diagrama de estados. Indique o valor da saída do circuito para cada estado e o valor do próximo estado para cada valor do estado e entrada.]



		Q(n+1)	Q(n+1)
Q(n)	Y(n)	x=0	x=1
00	1	10	01
01	0	11	10
10	0	00	00
11	1	01	01

[1]

		Q(n+1)	Q(n+1)
Q(n)	Y(n)	x=0	x=1
00	1	01	01
01	0	11	10
10	0	00	00
11	1	01	01

[2]

		Q(n+1)	Q(n+1)
Q(n)	Y(n)	x=0	x=1
00	0	10	00
01	1	10	11
10	0	10	01
11	1	11	01

[3]

		Q(n+1)	Q(n+1)
Q(n)	Y(n)	x=0	x=1
00	1	10	01
01	0	11	10
10	1	00	00
11	1	01	01

[4]

		Q(n+1)	Q(n+1)
Q(n)	Y(n)	x=0	x=1
00	1	10	11
01	1	00	10
10	1	10	10
11	1	11	01

[5]

[6]

None of the other options
[Nenhuma das outras opções]

J. Represent 375₈ in base 10.
[Represente 375₈ na base 10.]

[1]: 242
[4]: 175

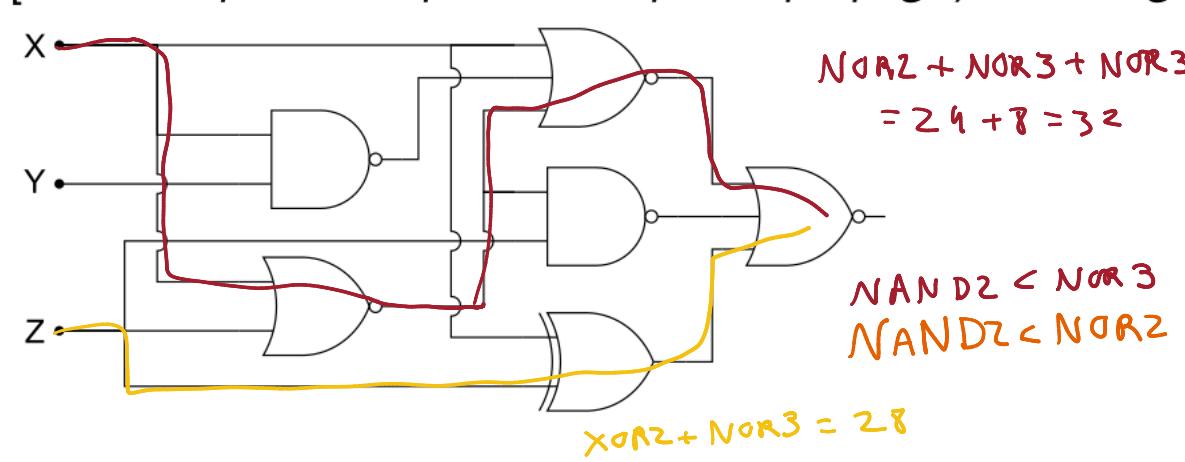
$$\begin{array}{r} 111 \ 101 \\ -2 -2 = 253 \end{array}$$

[2]: 253
[5]: 230

[3]: 215

[6]: None of the other options [Nenhuma das outras opções]

K. What is the worst case for the propagation time of the following circuit?
[Qual é o pior caso para o tempo de propagação do seguinte circuito?]



Gate	tp [ns]
NAND2	7
NOR2	8
NOR3	12
XOR2	16

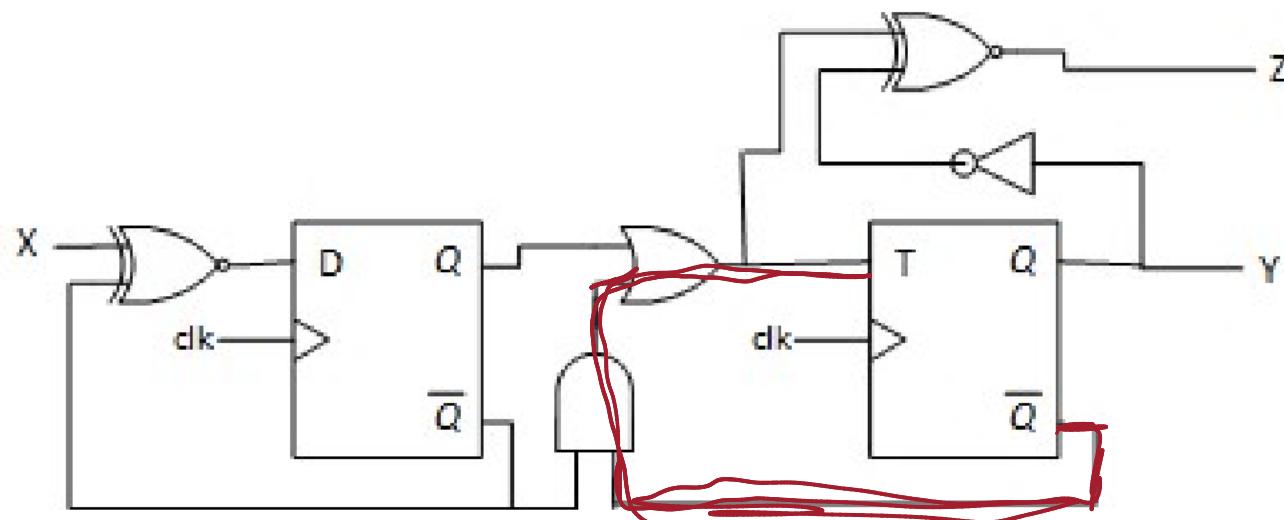
[1]: 28
[4]: 27

[2]: 34
[5]: 32

[3]: 31
[6]: None of the other options [Nenhuma das outras opções]

L. What is the minimum clock period of the following circuit, given the table values (in ns)?

[Qual é o período de relógio mínimo do seguinte circuito, assumindo os valores da tabela (em ns)?]



	tp [ns]	tsu [ns]	th [ns]
FF D	12	5	5
FF T	15	7	7
AND	7		
OR	9		
XNOR	13		
NOT	5		

$$T_{PT} + AND + OR + T_{SU} = 75 + 7 + 9 + 7 = 24 + 14 = 38$$

- [1]: 35
[4]: 34

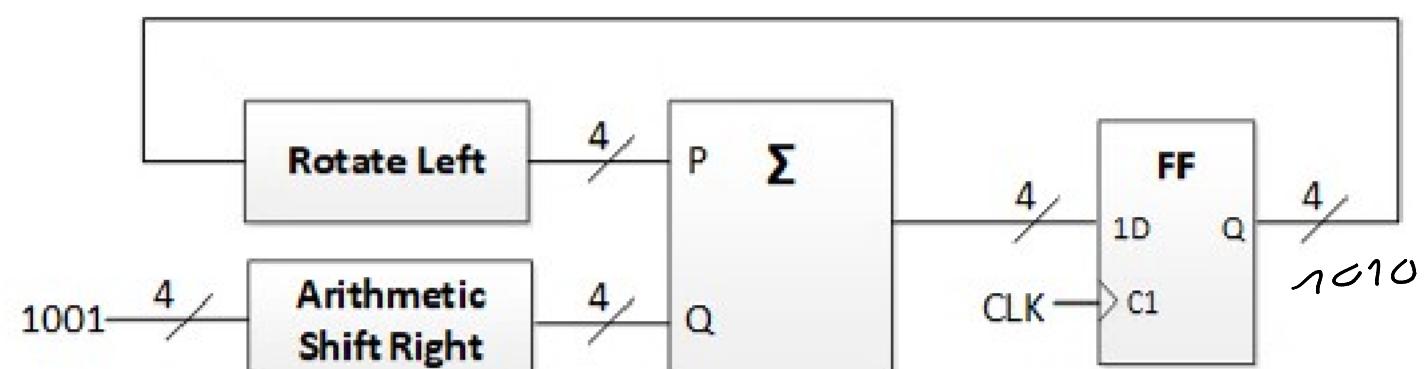
- [2]: 29
[5]: 38

- [3]: 30
[6]: No

M. Consider the following circuit with an adder, a register (4 FF's) and a combinational logic circuit. Assuming that the current state is $Q(3:0) = 1010$, what are the next two states of the circuit?
[Considere o seguinte circuito com um somador, um registo (4 FF's) e lógica combinatória. Assumindo que o estado actual é $Q(3:0) = 1010$, quais serão os próximos dois estados do circuito?]

- [1]: 0011, 1110
 - [2]: 1110, 1111
 - [3]: 0111, 1111
 - [4]: 1100, 1000
 - [5]: 0001, 1110

[6]: None of the other options
[*Nenhuma das outras opções*]



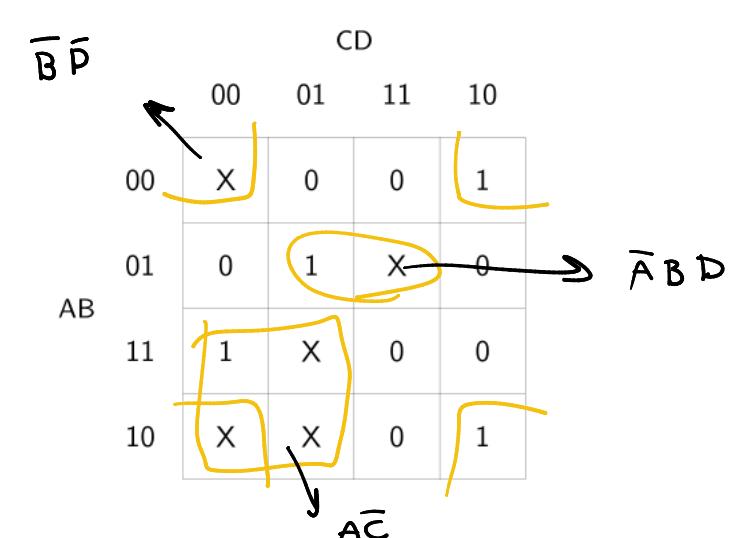
$$\begin{array}{r}
 1010 \\
 0101 \\
 + 1100 \\
 \hline
 = 0001
 \end{array}$$

- N. Which of the following expressions corresponds to the minimal function (defined as a sum of products) represented in the Karnaugh-map?

[Qual das seguintes expressões corresponde à função mínima (definida como uma soma de produtos) representada no mapa de Karnaugh?]

- [1]: $\overline{C}.A + \overline{C}.B.\overline{D} + B.D$
 - [2]: $\overline{B}.\overline{D} + \overline{C}.B.D + \overline{A}.D$
 - [3]: $\overline{C}.\overline{D} + A.\overline{B}.\overline{D} + A.D$
 - [4]: $\overline{B}.C + \overline{A}.B.\overline{C} + \overline{A}.\overline{D}$
 - [5]: $\overline{B}.\overline{D} + \overline{A}.B.D + A.\overline{C}$

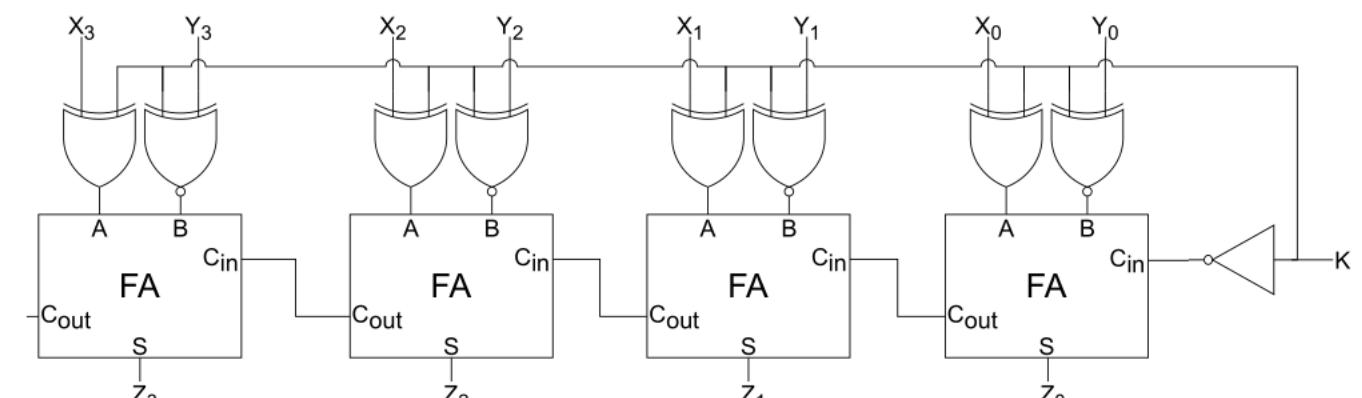
[6]: None of the other options [Nenhuma das outras opções]



- O. Which function is implemented by the following circuit? Consider that X and Y are 4-bit signed numbers (two's complement).

[Qual é a função desempenhada pelo seguinte circuito? Assuma que X e Y são números com sinal com 4-bits (em complemento para dois).]

- [1]: K=0: Z=X-1 ; K=1: Z=Y+1
- [2]: K=0: Z=-X ; K=1: Z=X+Y
- [3]: K=0: Z=X-Y ; K=1: Z=X+Y+1
- [4]: K=0: Z=-Y ; K=1: Z=X+Y
- [5]:** K=0: Z=X-Y ; K=1: Z=-(X-Y)-1
- [6]: None of the other options
[Nenhuma das outras opções]



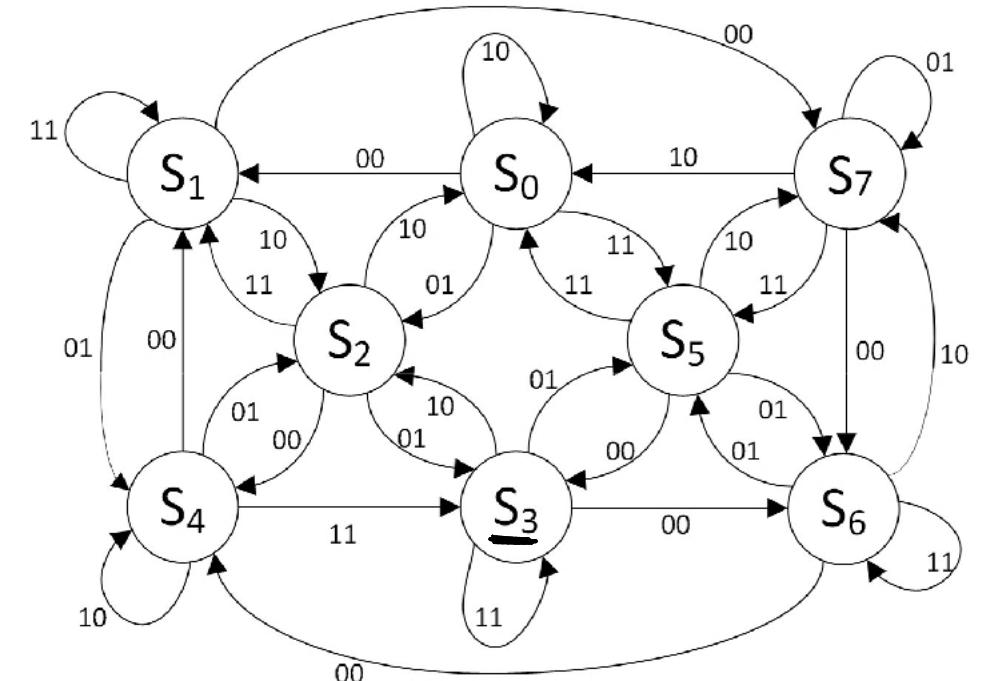
$$\begin{aligned} k=1 : \quad & C_{in} = 0 \\ & Y \oplus 1 = Y \\ & X \oplus 1 = \overline{X} \\ & \rightarrow -X-1 + Y = -(X-Y)-1 \\ & \text{b (pálto 1 por c2)} \end{aligned}$$

$$\begin{aligned} k=0 : \quad & C_{in} = 1 \rightarrow X-Y \\ & Y \oplus 0 = \overline{Y} \\ & X \oplus 0 = X \end{aligned}$$

- P. Consider the following state diagram with two inputs X_1X_0 , one-hot encoding, and where each state $S_i (i = 0, \dots, 7)$ is implemented with D flip-flops, with input D_i (next state) and output Q_i (current state). Select, only for the state S_3 , the correct option for D_3 as a function of X_1 and X_0 and the current states Q_i .

[Considere o seguinte diagrama de estados com duas entradas X_1X_0 , codificação one-hot, em que cada estado $S_i (i = 0, \dots, 7)$ é implementado com flip-flops do tipo D, com entradas D_i (próximo estado) e saída Q_i (estado actual). Indique, para o estado S_3 , a expressão de D_3 como função de X_1 e X_0 e os estados actuais Q_i .]

- [1]: $D_3 = X_1\overline{X_0}Q_2 + X_1X_0Q_3 + \overline{X_1}X_0Q_5 + \overline{X_1}\overline{X_0}Q_6$
- [2]: $D_3 = \overline{X_1}X_0Q_1 + X_1\overline{X_0}Q_3 + \overline{X_1}X_0(Q_5 + Q_7)$
- [3]: $D_3 = X_1\overline{X_0}Q_2 + X_1X_0Q_3 + X_1\overline{X_0}Q_6 + X_1\overline{X_0}Q_7$
- [4]: $D_3 = X_1X_0Q_1 + \overline{X_1}\overline{X_0}Q_2 + X_1\overline{X_0}Q_6 + X_1X_0Q_7$
- [5]:** $D_3 = \overline{X_1}X_0Q_2 + X_1X_0(Q_3 + Q_4) + \overline{X_1}\overline{X_0}Q_5$
- [6]: None of the other options
[Nenhuma das outras opções]



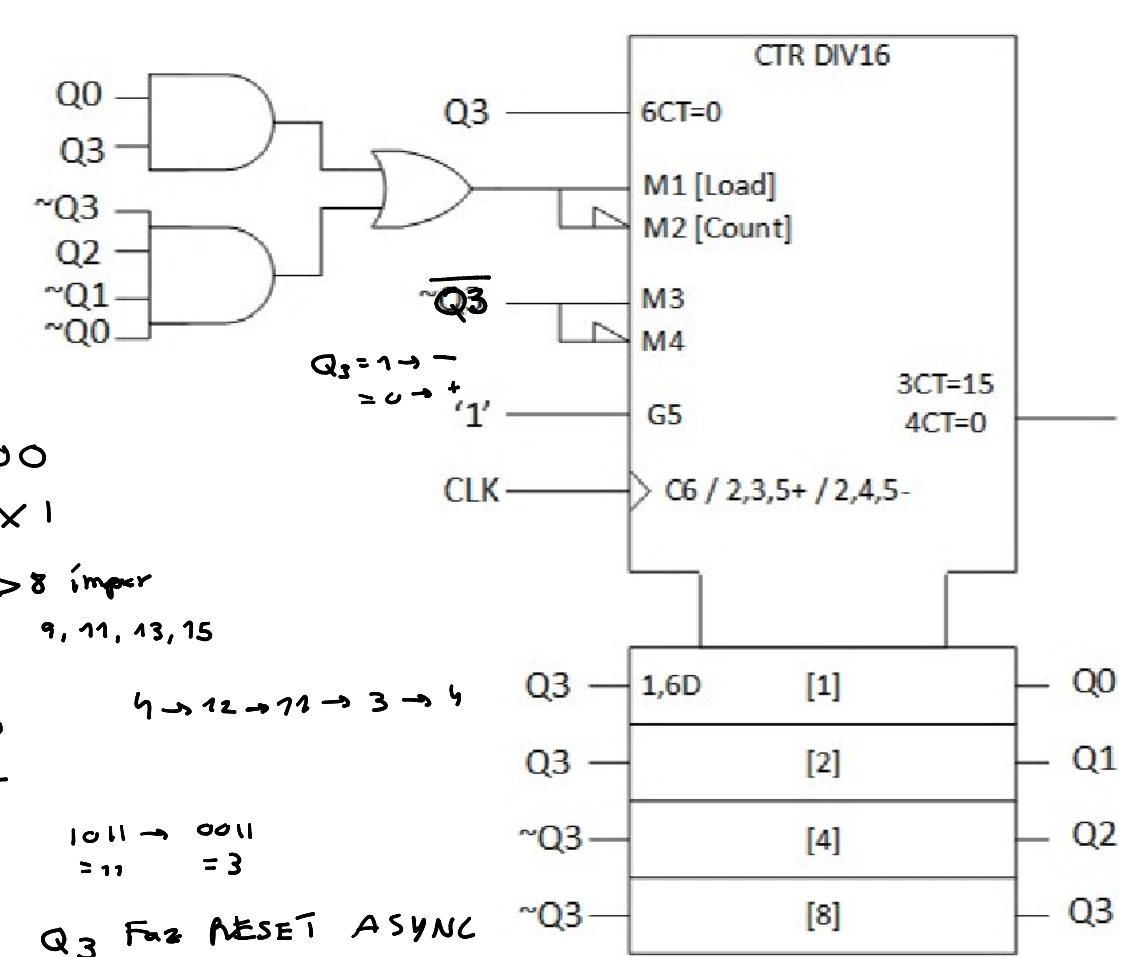
- Q. Which of the following options corresponds to the sequence, in stationary mode, in decimal format at the output of the circuit in the figure below? (suggestion: start by analyzing a "load" situation.)

[Qual das seguintes opções corresponde à sequência de saída do seguinte circuito, em regime estacionário e em formato decimal? (sugestão: comece por analisar a situação de carregamento ("load") de dados.)]

- [1]: ... 4 - 12 - 11 - 3 - 4 ...
- [2]: ... 13 - 0 - 1 - 2 - 3 - 4 - 13 ...
- [3]:** ... 4 - 12 - 0 - 1 - 2 - 3 - 4 ...
- [4]: ... 12 - 1 - 2 - 3 - 14 - 13 - 12 ...
- [5]: ... 9 - 8 - 7 - 6 - 5 - 4 - 9 ...
- [6]: None of the other options
[Nenhuma das outras opções]

LOAD: 0100
1XX1
↳ > 8 ímpar
9, 11, 13, 15

0100 → 1100
= 4 = 12
1101 → 0011
= 13 = 3
1100 → 1111
= 12 = 11
0011 → 0100
= 3 = 4



Recovery Exam

Digital Systems (2022/2023)

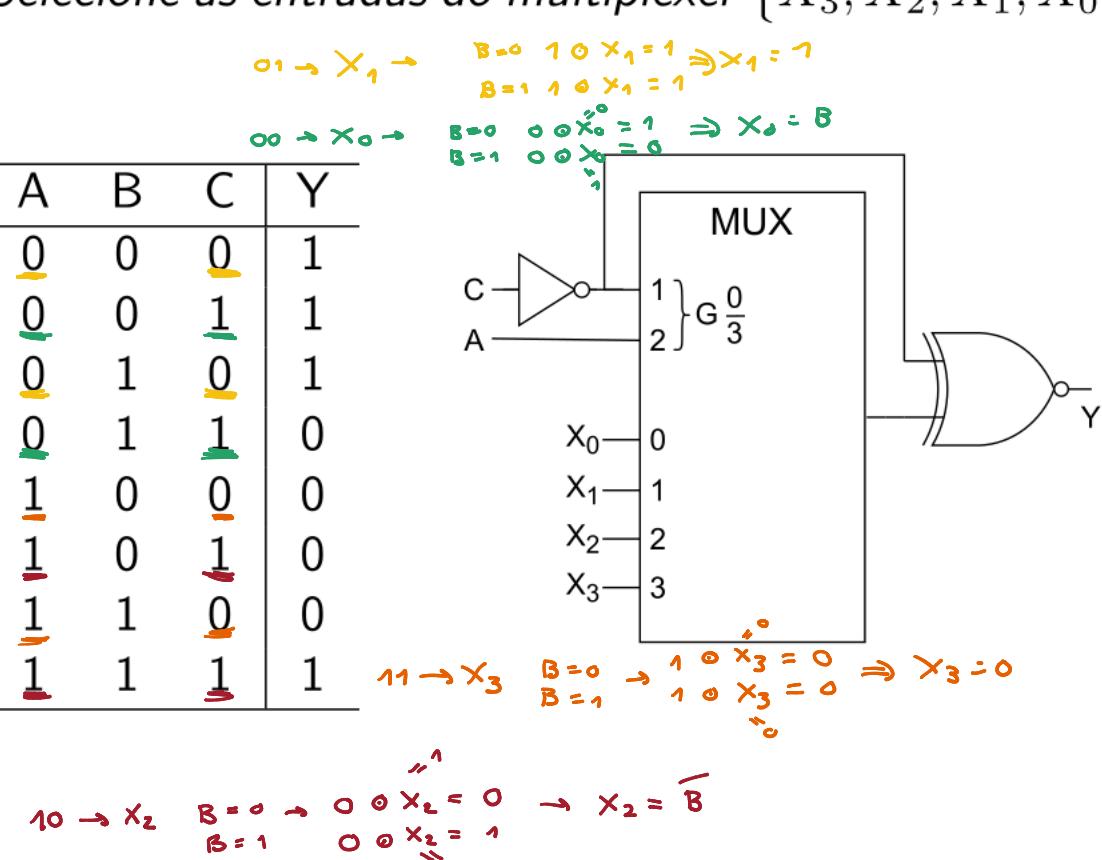
February 9th, 2023

- R. Consider the following circuit and truth table. Select the multiplexer inputs $\{X_3; X_2; X_1; X_0\}$ that result in the given truth table.

[Considere o seguinte circuito e tabela de verdade. Selecione as entradas do multiplexer $\{X_3; X_2; X_1; X_0\}$ que resultam na tabela apresentada.]

- [1]: $\{X_3; X_2; X_1; X_0\} = \{1; B; 0; \overline{B}\}$
 - [2]: $\{X_3; X_2; X_1; X_0\} = \{0; B; 1; \overline{B}\}$
 - [3]: $\{X_3; X_2; X_1; X_0\} = \{1; \overline{B}; 0; B\}$
 - [4]: $\{X_3; X_2; X_1; X_0\} = \{0; \overline{B}; 1; \overline{B}\}$
 - [5]: $\{X_3; X_2; X_1; X_0\} = \{0; \overline{B}; 1; B\}$
 - [6]: None of the other options
Nenhuma das outras opções

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



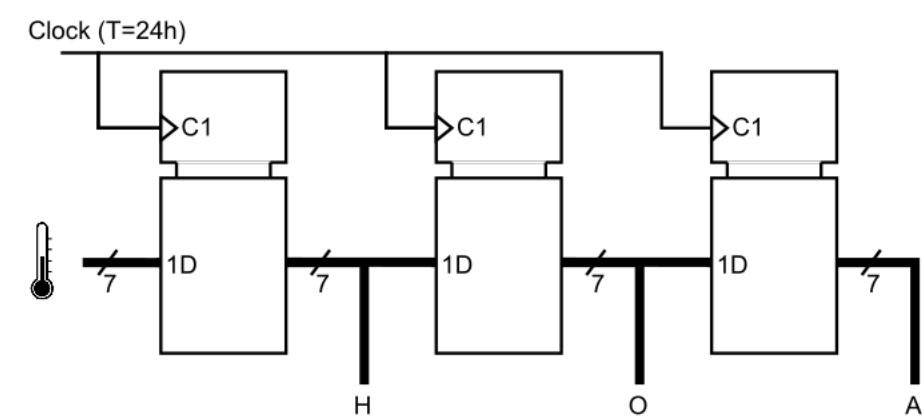
(This space was intentionally left blank for your auxiliary calculations.)

Volume 1 - Part II

NOTE: Portuguese version in the following page

[Question score partitioning: 35% + 30% + 35%]

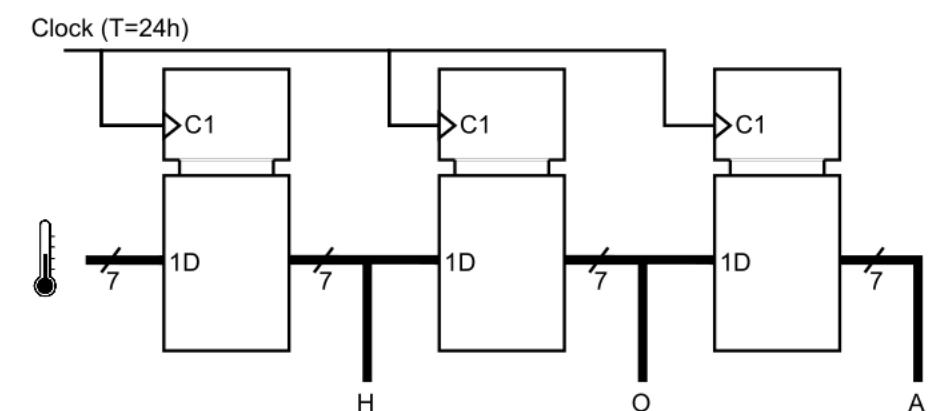
To control the temperature of a greenhouse, it was adopted a set of registers as shown in the figure, which allows the recording of the temperature values measured on three consecutive days: today (H), yesterday (O) and the day before yesterday (A). The measured temperature has a dynamic range between -64°C and $+63^{\circ}\text{C}$, with a 7-bit precision. In the following exercises, consider the use of 8-bit adders:



1. Design the circuit that computes the weighted average $T_M = 0.5 \times T_H + 0.375 \times T_O + 0.25 \times T_A$ with an 8-bit precision.
Hint: remember that $0.375 = 3/8$.
2. Without using adders, implement a circuit that activates the alarm signal ($X = 1$) when $T_M \geq 24^{\circ}\text{C}$.
Hint: design a combinational circuit to detect the pattern $T_M \geq +24$.
3. In order to evaluate the variation rate (i.e., derivative) of the observed temperature over the last three days, implement a circuit that activates a signal ($Z = 1$) when $(T_O - T_H) \geq 2 \times (T_A - T_O)$.
Hint: remember that $(T_O - T_H) \geq 2 \times (T_A - T_O) \Leftrightarrow 2 \times (T_A - T_O) + (T_H - T_O) < 0$.

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Para controlar a temperatura de uma estufa foi instalado o sistema de registos apresentado na figura que permite armazenar os valores de temperatura medidos em três dias consecutivos: hoje (H), ontem (O), e anteontem (A). A temperatura medida tem uma gama dinâmica entre -64°C e $+63^{\circ}\text{C}$, com uma precisão de 7-bits. Nos seguintes exercícios, considere a utilização de somadores de 8-bit:



1. Projecte o circuito que calcula o valor da média pesada $T_M = 0.5 \times T_H + 0.375 \times T_O + 0.25 \times T_A$ com uma precisão de 8-bits.
Sugestão: recorde que $0.375 = 3/8$.
2. Sem utilizar somadores, implemente um circuito que activa o sinal de alarme ($X = 1$) quando $T_M \geq 24^{\circ}\text{C}$.
Sugestão: projecte um circuito combinatório que detecte o padrão $T_M \geq +24$.
3. De modo a avaliar o ritmo de variação (i.e., derivada) da temperatura observada ao longo dos últimos três dias, implemente um circuito que active um sinal ($Z = 1$) quando $(T_O - T_H) \geq 2 \times (T_A - T_O)$.
Sugestão: recorde que $(T_O - T_H) \geq 2 \times (T_A - T_O) \Leftrightarrow 2 \times (T_A - T_O) + (T_H - T_O) < 0$.

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Volume 1 - Part III

NOTE: Portuguese version in the following page

[Question score partitioning: 50% + 50%]

Question A:

Design a circuit that controls a toaster. The toaster works as follows:



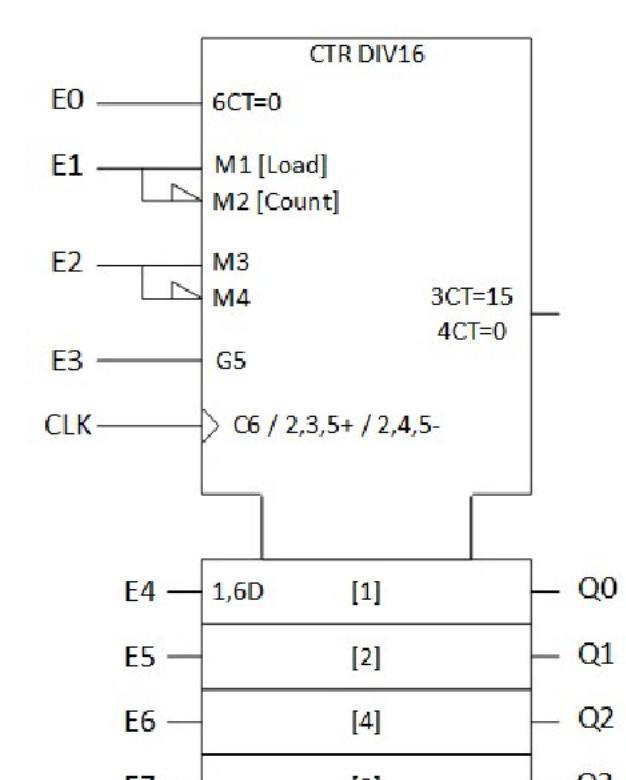
- The toaster has five input signals:
 - STOP_H: Aborts the toasting process, returning to a standby state.
 - ACT_H: Lever that lowers the bread and starts the toasting mechanism.
 - LONG_H: Button that sets the toasting time (active: $2TA$; inactive: $1TA$), where TA is the period of the auxiliary timer (see below).
 - THERM_H: Warning from sensing circuit when the temperature is above 50°C .
 - TIMEOUT_H: This signal is active during one clock period when the auxiliary timer expires.
- The toaster has four output signals:
 - LED_H: LED is on while the toaster is switched on, or the temperature is above 50°C .
 - TOAST_H: Activates the heating mechanism of the toaster.
 - FINISH_H: Activated during one clock period to disconnect the heating and free the bread.
 - TIMER_ACT_H: A transition from 0 to 1 in this signal starts the timer; a transition from 1 to 0 prepares the timer for a new activation.
- There are two standby states: with LED switched off (temperature lower or equal than 50°C indicated by THERM_H=0), and with LED switched on (temperature higher than 50°C , indicated by THERM_H=1).
- The initial state is a standby state with the LED switched off. After the user introduces the bread, presses the lever, activating ACT_H. The toaster starts, activating the timer (TIMER_ACT_H) and the heating (TOAST_H).
- Toasting will continue during 1 or 2 successive activations of the timer, depending on the value of LONG_H.
- After the timer expires for the last time (depending on LONG_H), the signal FINISH_H is active during one clock period.
- After FINISH_H is activated, the toasting operation is finished, the toaster returns to a standby state, and it is assumed that the lever automatically returns to the initial position. However, the red LED will remain lit (standby state with LED switched on) until the temperature becomes lower or equal than 50°C . This state behaves similarly to the initial state, except for the LED.

Complete the state diagram (see Volume 2, Part IIIA) defining the values of the input signals associated with all state transitions, as well as the values of the output signals in each state. "Don't cares" must be used for the inputs whose value does not matter for given a state transition. In the diagram, the inputs/outputs must be indicated in the following order:

- Order of the inputs: STOP_H, ACT_H, LONG_H, THERM_H, TIMEOUT_H.
- Order of the outputs: LED_H, TOAST_H, FINISH_H, TIMER_ACT_H.

Question B:

1. Consider a state machine with input A and state bits Q3, Q2, Q1 and Q0, implemented with the circuit depicted in the figure. Complete the state transition table (see Volume 2, Part IIIB), considering the provided state transitions. Justify, identifying the operation performed by the circuit in each transition. **Note: The parallel LOAD operation will only be accepted in case there is no other alternative leading to the same result. The signals that don't care to a given operation must mandatorily be marked as don't cares.**



2. Indicate the algebraic expressions of the signals E0 and E1 in the disjunctive

Pergunta A:

Projecte um controlador de uma torradeira que funciona da seguinte forma:

- A torradeira tem cinco sinais de entrada:
 - STOP_H: Aborta a operação da torradeira, retornando a um estado de *standby*.
 - ACT_H: Alavanca que baixa o pão e liga o mecanismo de aquecimento.
 - LONG_H: Botão que define o tempo de operação (activo: $2TA$; inativo: $1TA$), sendo TA o período do temporizador auxiliar (ver em baixo).
 - THERM_H: Aviso de um sensor de temperatura quando a temperatura da torradeira é superior a 50°C .
 - TIMEOUT_H: Ativo durante um período de relógio quando o temporizador auxiliar expira.
- A torradeira tem quatro sinais de saída:
 - LED_H: LED acende enquanto a torradeira está em operação, ou a temperatura é superior a 50°C .
 - TOAST_H: ativa o mecanismo de aquecimento da torradeira.
 - FINISH_H: ativado durante um período de relógio para desligar o aquecimento e libertar o pão.
 - TIMER_ACT_H: Uma transição de 0 para 1 neste sinal inicia o temporizador; uma transição de 1 para 0 reinicializa o gatilho do temporizador para poder receber uma nova activação.
- Existem dois estados de *standby*: com o LED apagado (temperatura menor ou igual a 50°C indicada por $\text{THERM_H}=0$), e LED aceso (temperatura superior a 50°C , indicada por $\text{THERM_H}=1$).
- O estado inicial é o estado de *standby* com o LED apagado. Depois de o utilizador introduzir o pão, pressiona a alavanca, ativando ACT_H. A torradeira inicia assim a sua operação, ativando o temporizador (TIMER_ACT_H) e o aquecimento (TOAST_H).
- A operação continua durante 1 ou 2 activações (sucessivas) do temporizador, consoante o valor de LONG_H.
- O sinal FINISH_H é ativado durante um período de relógio depois de o temporizador expirar pela última vez (que depende de LONG_H).
- Depois de FINISH_H ser ativado, a operação da torradeira termina, a torradeira volta a ficar num estado de *standby*, e assume-se que a alavanca voltou automaticamente à posição inicial. No entanto, o LED vermelho permanecerá aceso (estado *standby* com LED aceso) até que a temperatura passe a ser menor ou igual a 50°C . Este estado comporta-se de forma semelhante ao estado inicial, à exceção do LED.



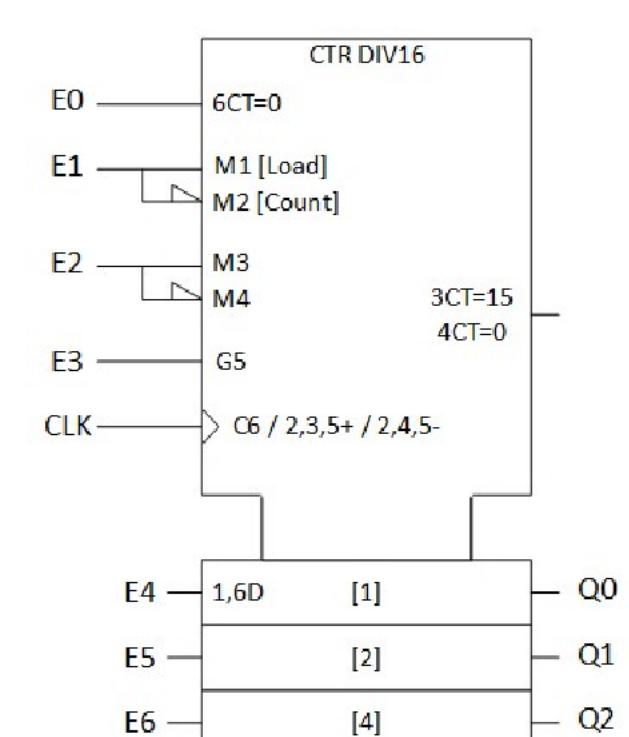
Complete o diagrama de estados (ver Volume 2, Parte IIIA), definindo os valores dos sinais de entrada que desencadeiam todas as transições de estado, assim como os valores de saída de cada estado. As "indiferenças" têm de ser obrigatoriamente usadas para entradas que não tenham influência numa determinada transição de estado. As entradas/saídas têm de ser indicadas de acordo com a ordem seguinte:

- Ordem das entradas: STOP_H, ACT_H, LONG_H, THERM_H, TIMEOUT_H.
- Ordem das saídas: LED_H, TOAST_H, FINISH_H, TIMER_ACT_H.

Pergunta B:

Considere uma máquina de estados com entrada A e bits de estado Q3, Q2, Q1 e Q0, realizada com base no circuito da figura.

1. Complete a tabela de transição de estados (ver Volume 2, Parte IIIB), considerando as transições nela representadas. Justifique, identificando na tabela as operações realizadas em cada transição. **Nota: A operação de carregamento em paralelo (LOAD) só será aceite se não houver uma operação alternativa que conduza ao mesmo resultado. Os sinais indiferentes para determinada operação têm obrigatoriamente de ser marcados como indiferenças.**



2. Indique as expressões para os sinais E0 e E1 na forma canónica disjuntiva, igno-

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Don't forget to identify this and the following pages!
Only these pages will be considered for your evaluation.

Volume 2 - Part I

For each question of Part I (question A, B, C, ...), fill in the number of the **correct answer** from the supplied multiple-choice list (answer 1, 2, 3, ...):

★	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1																		X	X	X	X	X	X	X	X	

NOTE: Leave blank (or fill in with 0) all questions that you do not wish to answer.

Volume 2 - Part II

Number: _____ Name: _____
Degree: LEEC LEAer LEFT

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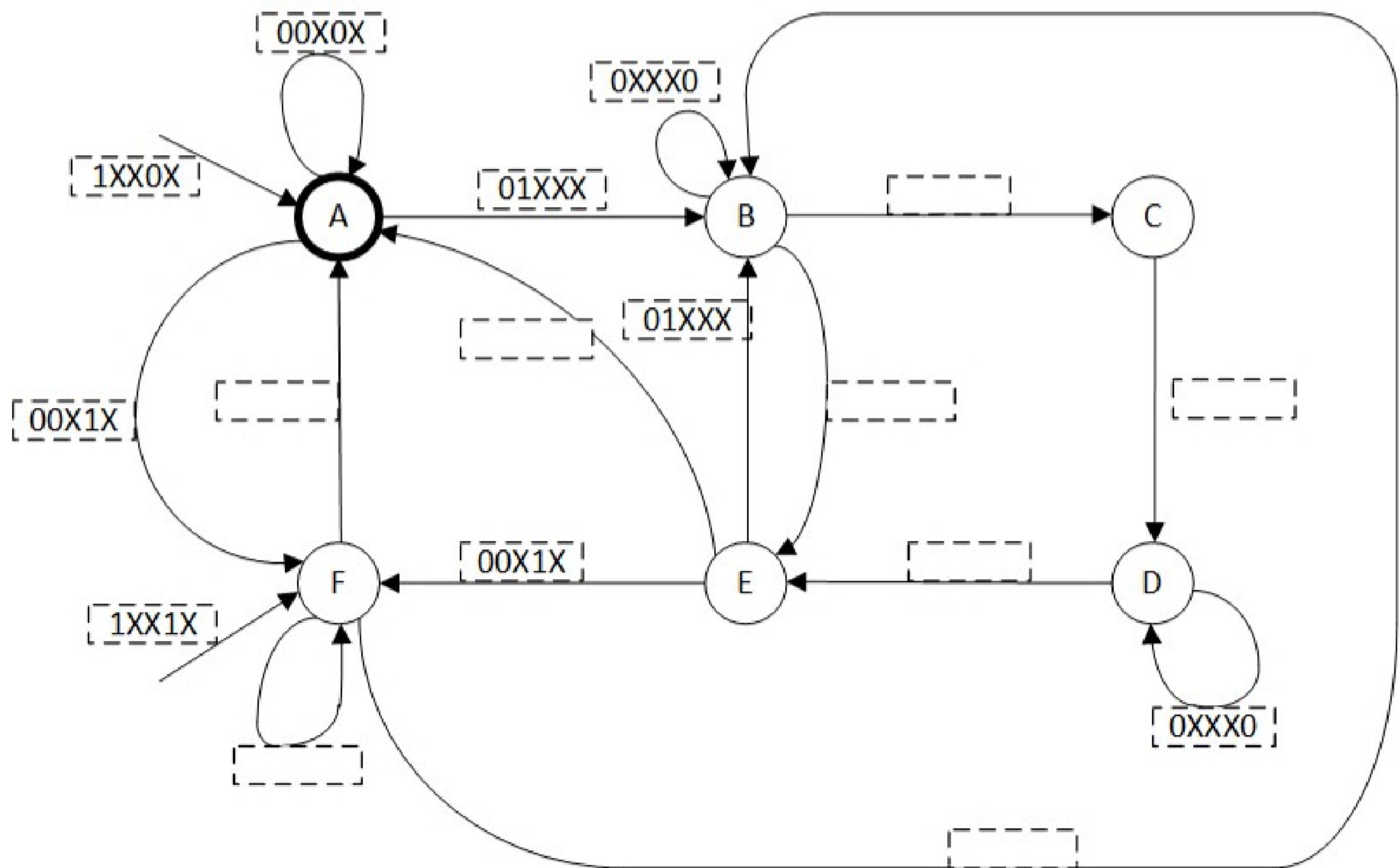
Volume 2 - Part II (Cont.)

Volume 2 - Part III

Pergunta A:

Meaning of the states [Significado dos estados]:

- A: Standby state w/ temperature ≤ 50 ; **initial state** [Estado standby com temperatura ≤ 50 ; **estado inicial**];
- B: Toaster switched on during the first timer period [Torradeira ligada durante o primeiro período do temporizador];
- C: Toaster switched on, re-initialize timer trigger before starting the second timer period [Torradeira ligada, reinicializar gatilho do temporizador antes de iniciar segundo período do temporizador];
- D: Toaster switched on during the second timer period [Torradeira ligada durante o segundo período do temporizador];
- E: Finish [Terminar];
- F: Standby state w/ temperature > 50 [Estado standby com temperatura > 50];



For each state, define the values of the inputs (in the diagram) and of the outputs (below) according to the following order:
[Para cada estado, indique os valores das entradas (no diagrama) e das saídas (em baixo) de acordo com a seguinte ordem]:

- Ordem das entradas: STOP_H, ACT_H, LONG_H, THERM_H, TIMEOUT_H.
- Ordem das saídas: LED_H, TOAST_H, FINISH_H, TIMER_ACT_H.

- A: _____
- B: _____
- C: _____

- D: _____
- E: _____
- F: _____

Number: _____

Name: _____

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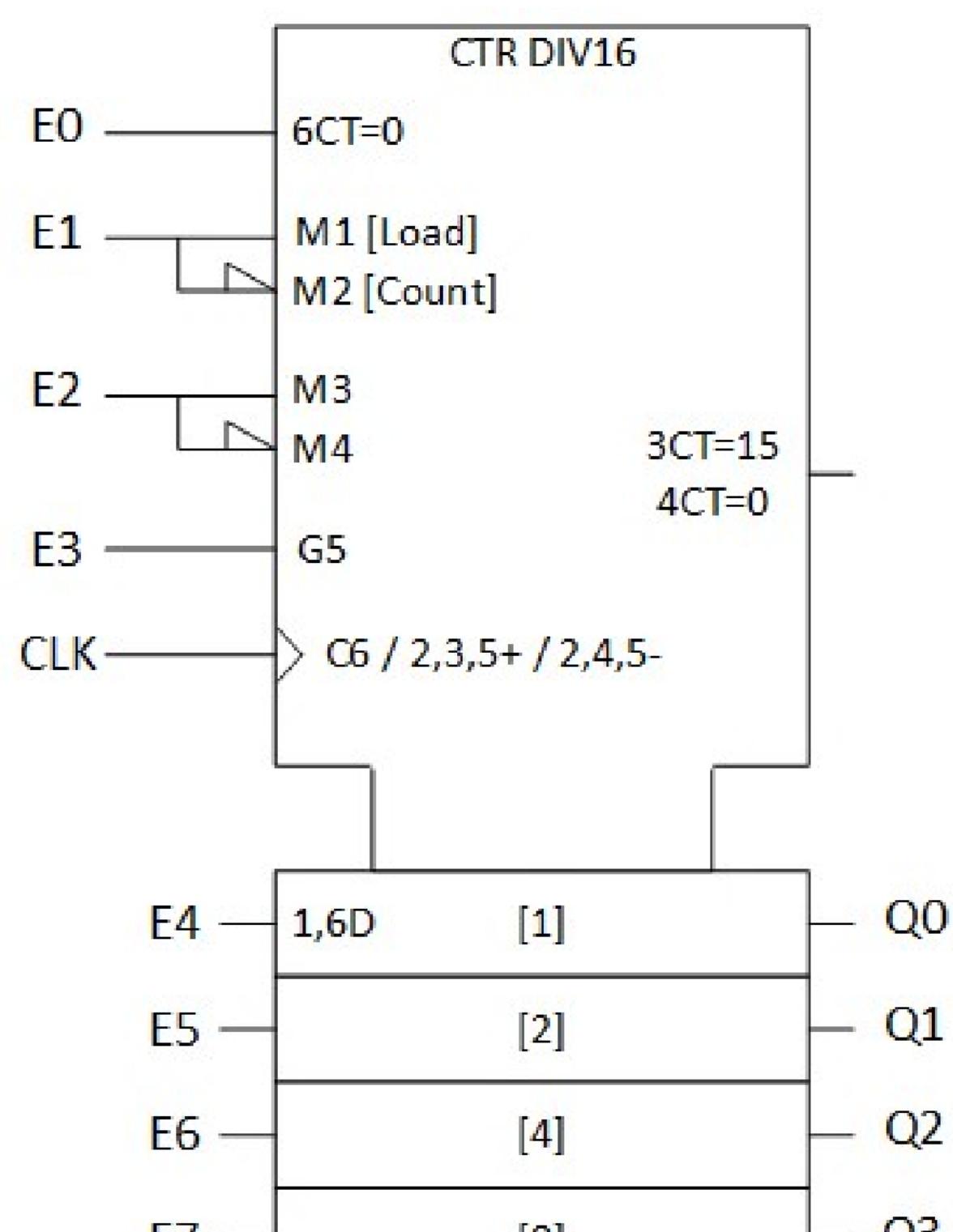
Volume 2 - Part III (Cont.)

Pergunta B:

$Q_3^n Q_2^n Q_1^n Q_0^n$	A	E0	E1	E2	E3	E4	E5	E6	E7	$Q_3^{n+1} Q_2^{n+1} Q_1^{n+1} Q_0^{n+1}$	Operation
0000	0	0	0							0001	
0000	1	0	0							1111	
0001	0	0	0							0010	
0001	1	0	1							0011	
0100	0	1	X							0000	
0100	1	0	0							0011	
1001	0	0	0							1010	
1001	1	0	1							1011	
1111	0	0	0							1110	
1111	1	0	1							1101	

• E0 = _____

• E1 = _____



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