

Specification for 7.5 inch EPD

Model NO. : DEPG0750RWF86BF30

DKE's Confirmation:

Prepared by	Checked by	Approved by

Customer approval:

Customer	Approved by	Date

Revision History

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1. Over View

DEPG0750RWF86BF30 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black and red full display capabilities. The 7.5 inch active area contains 480×800 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- ◆ 480×800 pixels display
- ◆ High contrast High reflectance
- ◆ Ultra wide viewing angle Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape portrait modes
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform can stored in On-chip OTP or written by MCU
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I²C signal master interface to read external temperature sensor
- ◆ Built-in temperature sensor

3. Mechanical and Optical Specification

Parameter	Specifications	Unit	Remark
Screen Size	7.5	Inch	
Display Resolution	800(H)×480(V)	Pixel	DPI:124
Active Area	163.2×97.92	mm	
Pixel Pitch	0.204×0.204	mm	
Pixel Configuration	Rectangle		
Outline Dimension	170.2(H)×111.2 (V) ×1.20(D)	mm	
Weight	43.9±0.5	g	

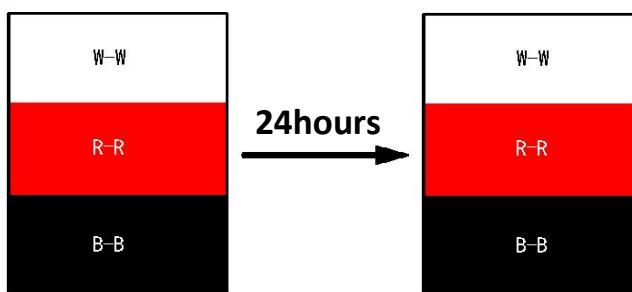
Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
KS	Black State L* value		-	13	15		3-1
	Black State A* value		-	4	6		3-1
	Black Ghosting Δ L		-	1	-		3-1
	After 24hour colour changed		-	2	-		3-4
WS	White State L* value		62	65	-		3-1
	White State A* value		-	0	1		3-1
	White Ghosting Δ L		-	1	-		3-1
	After 24hour colour changed		-	2	-		3-4
RS	Red State L* value		27	28	32		3-1
	Red State A* value		36	40	45		3-1
	Red Ghosting Δ E		-	3	-		3-1
	After 24hour colour changed		-	2	-		3-4
T update	Image update time	at 23 °C	-	20	-	sec	
R	White Reflectivity	White	30	34	-	%	3-1
CR	Contrast Ratio	Indoor	15:1	20	-		3-1 3-2
GN	2Grey Level	-	-	-	-		
Life		Temp:23±3°C Humidity:55±10%RH		5years			3-3

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3. When the product is stored. The display screen should be kept white and face up.

3-4. After 24hour Colour Changed:



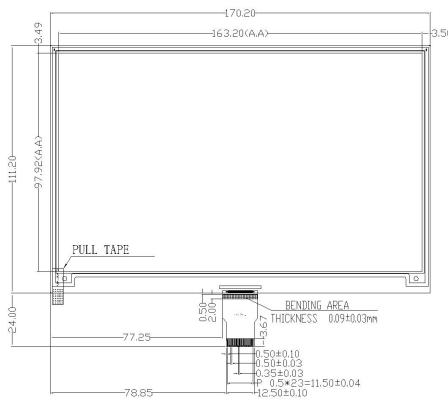
W: Max Δ E(W-W)<2, K: Max Δ E(B-B)<2, R: Max Δ Eab(R-R)<2.

4.Mechanical Drawing of EPD Module

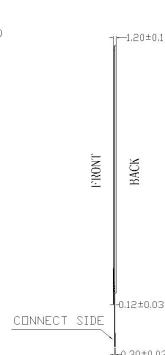
Confirmation:

DATE	REV.	MODIFICATION
2020-08-06	A	FIRST ISSUE

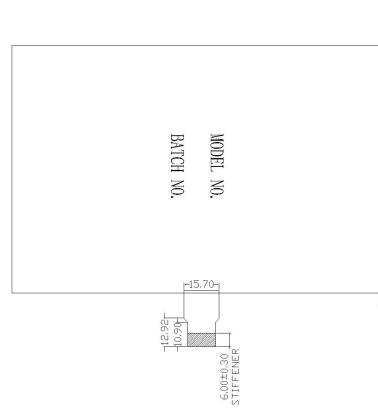
TOP VIEW



SIDE VIEW



BOTTOM VIEW



PIN	SIGNAL
1	NC
2	GDR
3	RESE
4	NC
5	VSH2
6	SDI
7	TSDA
8	BS1
9	BUSY
10	REF#
11	D/C#
12	CS#
13	SDA
14	SDB
15	VID0
16	VC1
17	VSS
18	VDD
19	VPP
20	VSH
21	VGH
22	VLS
23	VCL
24	VCOM



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NOTE

- 1 DISPLAY MODULE 7.5" ARRAY FOR EPD
- 2 DRIVER IC:JD7968BB
- 3 RESOLUTION:480gateX800source
- 4 PIXEL SIZE:0.204mmX0.204mm

TOLERANCES UNMARKED ANGLES±5°	TITLE: EPD	PROJECT: DEPG0750_F86BF30	REV.: A	DATE: 20.08.06	CUST. P/N:
.X=±0.4mm .XX=±0.20mm .XXX=±0.20mm	NN ZHAO	CC ZHENG	XF NIE	mm	
BYK.	CHK.	APPR.	UNIT: mm	3RD ANGLE:	PAGE: 1/1

5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	Note 5-6
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	Note 5-6
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin Low when -Outputting display waveform -Communicating with digital temperature sensor.

Note 5-5: Bus interface selection pin

Note 5-6: This pin connect to the VSS if there is no external temperature sensor.

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.3 to +6.0	V
Logic Input voltage	VIN	-0.3 to VCI +0.3	V
Operating Temp range	TOPR	0 to +40	°C.
Storage Temp range	TSTG	-25 to+40	°C.
Optimal Storage Temp	TSTGo	23±3	°C.
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

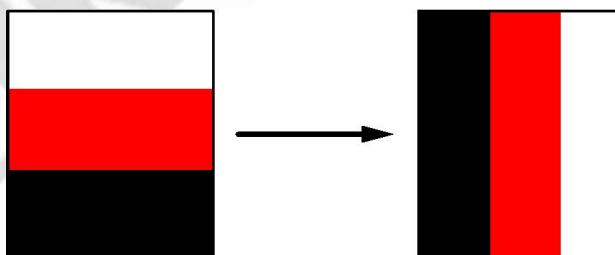
1. Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
2. We guarantee the single pixel display quality for 0-35°C, but we only guarantee the barcode readable for 35-40°C.
3. The storage time is within 10 days for -25°C ~ 0°C or 40°C ~ 60°C.
The display screen should be kept white and face up.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	Vss	-		-	0	-	V
Logic supply voltage	VCI	-	VCI	2.3	3.0	3.6	V
Digital/Analog supply voltage	VDD		VDD	2.3	3.0	3.6	V
High level input voltage	VIH	-	-	0.7 VCI	-	-	V
Low level input voltage	VIL	-	-	GND	-	0.3VDD	V
High level output voltage	VOH	IOH = 400uA	-	VCI -0.4	-	-	V
Low level output voltage	VOL	IOL = - 400uA	-	-	-	GND +0.4	V
Typical power	P _{TYP}	VCI =3.0V	-	-	30	-	mW
Deep sleep mode	P _{STPY}	VCI =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_VCI	VCI =3.0V	-	-	10	-	mA
Image update time	-	23 °C	-	-	20	-	sec
Typical peak current	Iopr_VCI	2.3~3.6V			100	200	mA
Sleep mode current	Islp_VCI	DC/DC off No clock No input load Ram data retain	-	-	20	-	uA
Deep sleep mode current	Idslp_VCI	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 3 scale pattern to vertical 3 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by DKE.
4. Electrical measurement: Tektronix oscilloscope - MDO3024,
Tektronix current probe - TCP0030A.

6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-3-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

Table 6-3-1: MCU interface assignment under different bus interface mode

6.3.2 MCU Serial Interface (4-wire SPI)

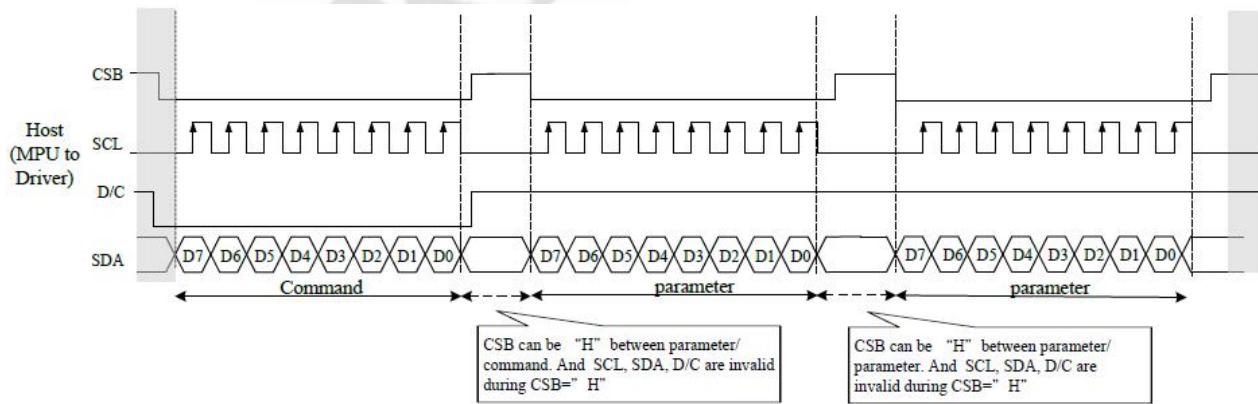
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

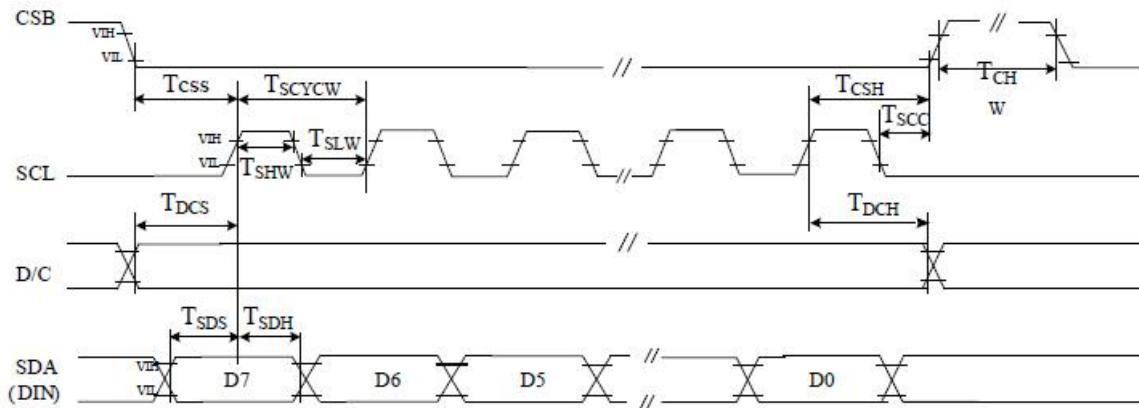
Table 6-3-2: Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

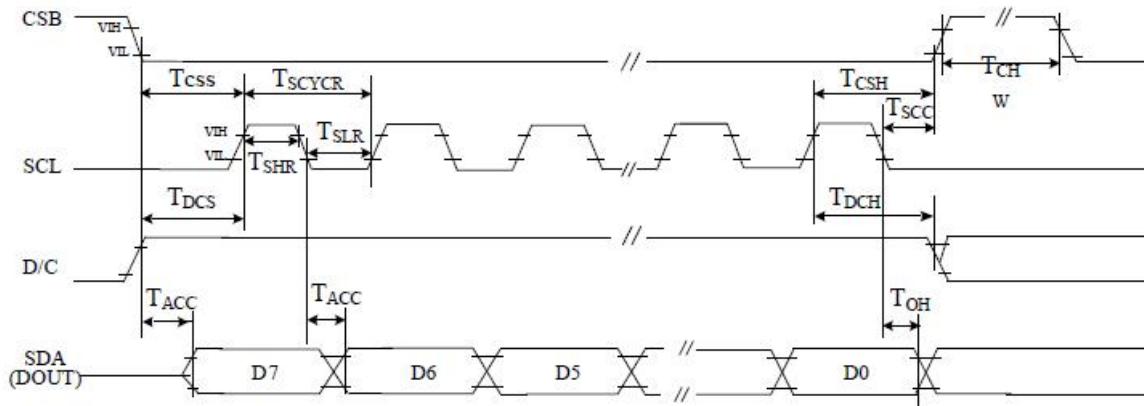
Figure 6-3-3: 4-wire SPI mode



6.3.3 Interface Timing (4-wire SPI)



4-wire serial interface characteristics(write mode)



4-wire serial interface characteristics(read mode)

6.3.4 MCU Serial Interface (3-wire SPI)

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Table 6-3-4: Control pins of 3-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

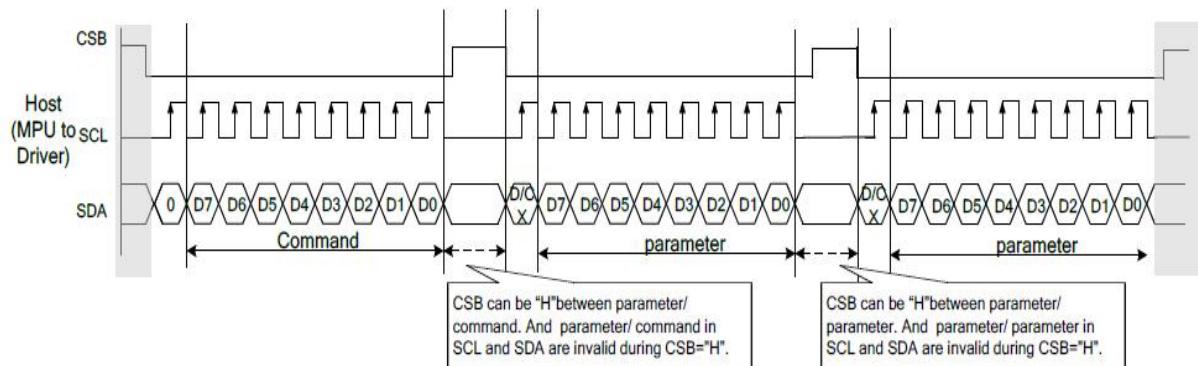
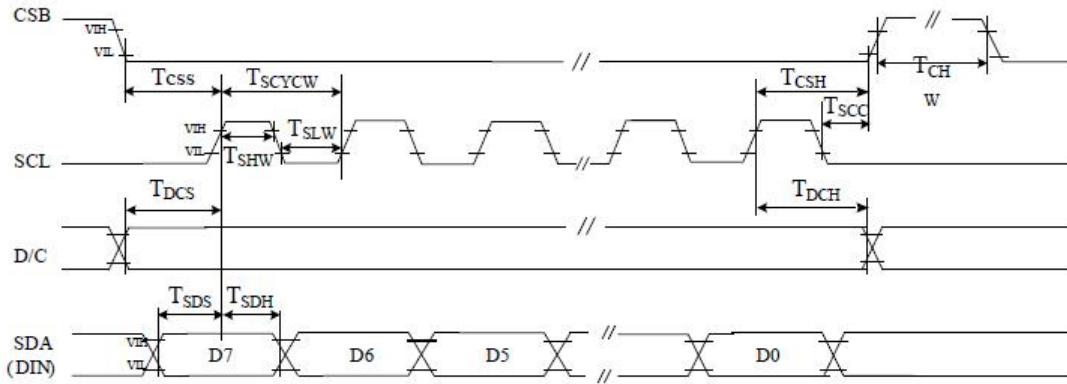
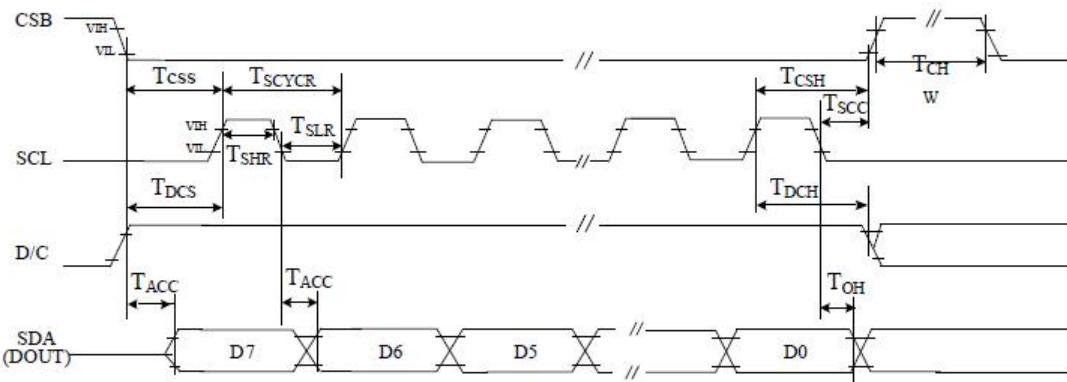


Figure 6-3-5: 3-wire SPI mode

6.3.5 Interface Timing (3-wire SPI)



3-wire serial interface characteristics(write mode)



3-wire serial interface characteristics(read mode)

6.3.6 Serial Interface Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T _{CS}	60			ns	Chip select setup time
	T _{CSH}	65			ns	Chip select hold time
	T _{SCC}	20			ns	Chip select CSB setup time
	T _{CHW}	40			ns	Chip select setup time
SCL	T _{SCYCW}	100			ns	Serial clock cycle (Write)
	T _{SHW}	35			ns	SCL "H" pulse width (Write)
	T _{SLW}	35			ns	SCL "L" pulse width (Write)
	T _{SCYCR}	150			ns	Serial clock cycle (Read)
	T _{SHR}	60			ns	SCL "H" pulse width (Read)
	T _{SLR}	60			ns	SCL "L" pulse width (Read)
SDA (DIN) (DOUT)	T _{SDS}	30			ns	Data setup time
	T _{SDH}	30			ns	Data hold time
	T _{ACC}		50		ns	Access time
	T _{OH}	15			ns	Output disable time
D/C	T _{DCS}	20			ns	DC setup time
	T _{DCH}	20			ns	DC hold time
RC loading						
Source driver output loading	RL_S		1.96k		Ω	
	CL_S		31.11		pf	
Gate driver output loading	RL_S		2.78k		Ω	
	CL_S		27.68		pf	
VCOM output loading	RL_com		61.26		Ω	
	CL_com		3365.7		pf	

7.Command Table

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Defau lt
1	Panel Setting (PSR)	W	0	0	0	0	0	0	0	0	0	00h
		W	1	RES[1]	RES[0]	REG-EN	BWR	UD	SHL	SHD-N	RST-N	C7h
		W	1	-	IMCP	-	VCMZ	TS AUTO	VGLTIEG	NORG	VC LUTZ	09h
2	Power Setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
		W	1	-	-	-	VCOM_H V	VGHL LV [3]	VGHL LV [2]	VGHL LV [1]	VGHL LV [0]	00h
		W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	3Fh
		W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	3Fh
		W	1	OPTEN	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	0Fh
3	Power OFF (POF)	W	0	0	0	0	0	0	0	1	0	02H
4	Power OFF Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	-	-	T_VDS_O FF[1]	T_VDS_O FF[0]	T_VSHR OFF[1]	T_VSHR OFF[0]	-	-	00h
5	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
6	Power ON Measure (PMES)	W	0	0	0	0	0	0	1	0	1	05H
7	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	BT_PHA[7]	BT_PHA[6]	BT_PHA[5]	BT_PHA[4]	BT_PHA[3]	BT_PHA[2]	BT_PHA[1]	BT_PHA[0]	17h
		W	1	BT_PHB[7]	BT_PHB[6]	BT_PHB[5]	BT_PHB[4]	BT_PHB[3]	BT_PHB[2]	BT_PHB[1]	BT_PHB[0]	17h
		W	1	-	-	BT_PHC1[5]	BT_PHC1[4]	BT_PHC1[3]	BT_PHC1[2]	BT_PHC1[1]	BT_PHC1[0]	17h
		W	1	PHC2EN	-	BT_PHC2[5]	BT_PHC2[4]	BT_PHC2[3]	BT_PHC2[2]	BT_PHC2[1]	BT_PHC2[0]	17h
		W	1	0	0	0	0	FT_RHA[3]	FT_RHA[2]	FT_RHA[1]	FT_RHA[0]	08h
		W	1	FT_RHC[3]	FT_RHC[2]	FT_RHC[1]	FT_RHC[0]	FT_RHB[3]	FT_RHB[2]	FT_RHB[1]	FT_RHB[0]	88h
8	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
9	Data Start Transmission 1 (DTM1)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
10	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0	12h
12	Data Start transmission 2(DTM2)	W	0	0	0	0	1	0	0	1	1	13H
		W	1	#	#	#	#	#	#	#	#	00h
13	LUT for VCOM (LUT1)	W	0	0	0	1	0	0	0	0	0	20H
		W	1	#	#	#	#	#	#	#	#	00h
14	White to White LUT (LUTWW)	W	0	0	0	1	0	0	0	0	1	21H
		W	1	#	#	#	#	#	#	#	#	00h
15	Black to White LUT (LUTBW/LUTR)	W	0	0	0	1	0	0	0	1	0	22H
		W	1	#	#	#	#	#	#	#	#	00h
16	White to Black LUT	W	0	0	0	1	0	0	0	1	1	23H

	(LUTWB/LUTW)	W	1	#	#	#	#	#	#	#	00h
17	Black to Black LUT (LUTBB/LUTB)	W	0	0	0	1	0	0	1	0	24H
		W	1	#	#	#	#	#	#	#	00h
18	Set LUT States (SET_GROUP)	W	0	0	0	1	0	0	1	1	26H
		W	1	0	0	0	0	0	0	b2w_stg_sel[1:0]	00h
19	LUT option	W	0	0	0	1	0	1	0	1	2AH
		W	1	EOPT	-	-	-	-	-	-	00h
		W	1	STATE_XON[7:0]							00h
		W	1	STATE_XON[15:8]							00h
		W	0	0	0	1	1	0	0	0	30h
20	PLL control (PLL)	W	1	-	M[2:0]			N[2:0]			3Ch
		W	0	0	0	1	1	0	0	0	31h
21	PLL mode selection	W	1	0	0	0	0	0	0	PLLoption	01h
		W	0	0	0	1	1	0	0	1	32h
22	Group frame rate	W	1	Group 1 M[2:0]			Group 1 N[2:0]				3Ch
		W	1	Group 2 M[2:0]			Group 2 N[2:0]				3Ch
		W	1	Group 3 M[2:0]			Group 3 N[2:0]				3Ch
		W	1	Group 4 M[2:0]			Group 4 N[2:0]				3Ch
		W	1	Group 5 M[2:0]			Group 5 N[2:0]				3Ch
		W	1	Group 6 M[2:0]			Group 6 N[2:0]				3Ch
		W	1	Group 7 M[2:0]			Group 7 N[2:0]				3Ch
		W	1	Group 8 M[2:0]			Group 8 N[2:0]				3Ch
23	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	40H
		R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]
		R	1	D2/TS[1]	D1/TS[0]	D0	-	-	-	-	--
24	Temperature Sensor Calibration(TSE)	W	0	0	1	0	0	0	0	0	41H
		W	1	TSE	-	TO[5]	TO[4]	TO[3]	TO[2]	TO[1]	TO0]
25	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	42H
		W	1	WATTR [7]	WATTR [6]	WATTR [5]	WATTR [4]	WATTR [3]	WATTR [2]	WATTR [1]	WATTR [0]
		W	1	WMSB [7]	WMSB [6]	WMSB [5]	WMSB [4]	WMSB [3]	WMSB [2]	WMSB [1]	WMSB [0]
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]
26	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]
27	Vcom and data interval setting(CDI)	W	0	0	1	0	1	0	0	0	50H
		W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]
28	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD
		R	1	GHD	SHD	SLD	SHRD	-	-	-	-
29	TCON setting (TCON)	W	0	0	1	1	0	0	0	0	60H
		W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]
30	TCON resolution	W	0	0	1	1	0	0	0	1	61H

	(TRES)	W	1							HRES(9)	HRES(8)	00h
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00h
		W	1							VRES(9)	VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
31	Source & gate start setting	W	0	0	1	1	0	0	0	1	0	62H
		W	1							S_start (9)	S_start (8)	00h
		W	1	S_start (7)	S_start (6)	S_start (5)	S_start (4)	S_start (3)	-	-	-	00h
		W	1				gscan				G_start [8]	00h
		W	1	G_start (7)	G_start (6)	G_start (6)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	00h
32	Revision (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	#	#	#	#	#	#	#	#	-
33	Get Status(FLG)	W	0	0	1	1	1	0	0	0	1	71H
		R	1	Con_fb	PTL_flag	I2C_ERR	I ² C_BUSYN	Data_flag	PON	POF	BUSY_N	-
34	Auto Measurement Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80H
		W	1	-	-	AMVT [1]	AMVT [0]	XON	AMVS	AMV	AMVE	10h
35	Vcom Value(VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	-
36	VCM_DC Setting register (VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	VCDS[6]	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	1Fh
37	Partial Window (PTL)	W	0	1	0	0	1	0	0	0	0	90h
		W	1	-	-	-	-	-	-	HRST[9]	HRST[8]	00h
				HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	0	0	0	00h
		W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
				HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	1	1	1	00h
		W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h
		W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h
		W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	00h
		W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	00h
		W	1	-	-	-	-	-	-	-	PT_SCA	00h
38	Partial In(PTIN)	W	0	1	0	0	1	0	0	0	1	91h
39	Partial Out(PTOUT)	W	0	1	0	0	1	0	0	1	0	92h
40	Program Mode (PGM)	W	0	1	0	1	0	0	0	0	0	A0H
		W	1	1	0	1	0	0	0	0	1	A1h
41	Active program(APG)	W	0	1	0	1	0	0	0	0	1	A1H
42	Read OTP Data (ROTP)	W	0	1	0	1	0	0	0	1	0	A2H
		R	1	#	#	#	#	#	#	#	#	-
43	Force Temperature	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	TS_SET [7]	TS_SET [6]	TS_SET [5]	TS_SET [4]	TS_SET [3]	TS_SET [2]	TS_SET [1]	TS_SET [0]	00h
44	Temperature	W	0	1	1	1	0	0	1	1	1	E7H

	Boundary Phase-C2 (TS_PHC2)	R	1	TS_PHC2 [7]	TS_PHC2 [6]	TS_PHC2 [5]	TS_PHC2 [4]	TS_PHC2 [3]	TS_PHC2 [2]	TS_PHC2 [1]	TS_PHC2 [0]	00h
45	Power saving	W	0	1	1	1	0	1	0	0	0	E8H
		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00h

COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: -: Don't Care

1) Panel Setting (PSR) (R00H)

R00H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
PSR	W	0	0	0	0	0	0	0	0	0	
1 st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	
2 nd Parameter	W	1	-	IMCP	-	VCMZ	TS_AUTO	VGLTIEG	NORG	VC_LUTZ	

The command defines as :

1st parameter

Bit	Name	Description
[0]	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating
[1]	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. (default)
[2]	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →...→S2→Last data=S1. 1: Shift right: First data=S1→S2 →...→Sn-1→Last data=Sn. (default)
[3]	UD	UD function 0:Scan down; First line=Gn→Gn-1 →...→G2→Last line=G1. 1:Scan up; First line=G1→G2 →...→Gn-1→Last line=Gn. (default)
[4]	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. (default) 1: Pixel with B/W. Run LU1 only
[5]	REG_EN	LUT selection setting 0 : Using LUT from OTP(default) 1 : Using LUT from register
[7:6]	RES[1,0]	Resolution setting 00: Display resolution is 600x448 01: Display resolution is 640x480 10: Display resolution is 720x540 11: Display resolution is 800x600

Notes:

- When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turnoff. SD output and VCOM will base on previous condition and keep floating.
- When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.

2nd parameter

Bit	Name	Description
[0]	VC_LUTZ	VCOM status function 0 : Display off, VCOM keep to power off 1 : Display off, VCOM is set to floating (default)
[1]	NORG	VCOM status function 0 : No effect (default) 1 : Expect refreshing display, VCOM is tied to GND
[2]	VGLTIEG	VGL power off status function 0 : Power off, VGL will be floating (default) 1 : Power off, VGL will be tied to GND
[3]	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling refresh, temperature sensing on 1 : Before enabling booster, temperature sensing on (default)
[4]	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
[6]	IMCP	1/0 : copy new sram data to old sram data after refreshing

Priority of VCOM setting: VCMZ > NORG > VC_LUTZ

2) Power setting Register (PWR) (R01H)

R01H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
PWR	W	0	0	0	0	0	0	0	0	1	
1 st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	
2 nd Parameter	W	1	-	-	-	VCOM_HV	VGHL_LV [3]	VGHL_LV [2]	VGHL_LV [1]	VGHL_LV [0]	
3 rd Parameter	W	1	-	-	VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	
4 th Parameter	W	1	-	-	VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	
5 th Parameter	W	1	OPTEN	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	

The command defines as :

1st Parameter:

Bit	Name	Description
[0]	VDG_EN	Gate power selection. 0 : External VDGS power from VGH/VGL pins. (VDNG_EN open) 1 : Internal DCDC function for generate VGH/VGL. (default)
[1]	VDS_EN	Source power selection. 0 : External source power from VSH/VSL pins. 1 : Internal DC/DC function for generate VSH/VSL. (default)

2nd Parameter:

Bit	Name	Description
[3:0]	VGHL_LV	VGHL_LV Voltage Level
		code
		VGH / VGL Voltage
		0000 VGH=20V, VGL=-20V (default)
		0001 VGH=19V, VGL=-19V
		0010 VGH=18V, VGL=-18V
		0011 VGH=17V, VGL=-17V
		0100 VGH=16V, VGL=-16V
		0101 VGH=15V, VGL=-15V
		0110 VGH=14V, VGL=-14V
		0111 VGH=13V, VGL=-13V
		1000 VGH=12V, VGL=-12V
		1001 VGH=11V, VGL=-11V
		1010 VGH=10V, VGL=-10V
		1011 -
		1100 -
		1101 VGH=9V, VGL=-9V
		1110 VGH=8V, VGL=-8V
		1111 VGH=7V, VGL=-7V
[4]	VCOM_HV	VCOM Voltage Level 0: VCOMH=VSH+VCOMDC, VCOML=VSL+VCOMDC (default) 1: VCOMH=VGH, VCOML=VGL

3rd Parameter: Internal VSH power selection for B/W LUT. (Default value: 111111b)

Bit	Name	Description		
5-0	VSH	Internal VSH power selection.		
		VSH[5:0]		Voltage(V)
		000000	00h	2.4
		000001	01h	2.6
		000010	02h	2.8
		000011	03h	3.0
	
		111110	3Eh	14.8
111111		3Fh	15(default)	

4th Parameter: Internal VSL power selection for B/W LUT. (Default value: 111111b)

Bit	Name	Description	
5-0	VSL	Internal VSL power selection.	
		VSH[5:0]	Voltage(V)
		000000	00h -2.4
		000001	01h -2.6
		000010	02h -2.8
		000011	03h -3.0
	
		111110	3Eh -14.8
		111111	3Fh -15(default)

5th Parameter: Internal VSHR power selection for Red LUT. (Default value: 00001111b)

OPTEN=0:enable step =0.2 voltage selection(2.4~15V)

Internal VSHR power selection for Red LUT.

Bit	Name	Description	
5-0	VSHR	Internal VSH power selection.	
		VSH[5:0]	Voltage(V)
		000000	00h -2.4
		000001	01h -2.6
		000010	02h -2.8
		000011	03h -3.0
	
		001111	0Fh 5.4(default)
	
		111101	3Dh -14.6
		111110	3Eh -14.8
		111111	3Fh -15

OPTEN=1:enable step =0.1 voltage selection(2.4~15V)

Internal VSHR power selection for Red LUT.

Bit	Name	Description	
6-0	VSHR	Internal VSH power selection.	
		VSH[6:0]	Voltage(V)
		0000000	00h -2.4
		0000001	01h -2.5
		0000010	02h -2.6
		0000011	03h -2.7
		0000100	04h -2.8
		0000101	05h -2.9
	
		1111100	7Ch -14.8
		1111101	7Dh -14.9
		1111110	7Eh -15

Note: VSH>VSHR

3) Power OFF Command (POF)(R02H)

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
POF	W	0	0	0	0	0	0	0	1	0	

The command defines as :

After power off command, driver will power off base on power off sequence.

After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high.

Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off.

SD output and VCOM will keep floating.

4) Power off Sequence Setting Register (PFS)(R03H)

R03H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
PFS	W	0	0	0	0	0	0	0	1	1	
1st Parameter	W	1	-	-	T_VDS_OFF [1]	T_VDS_OFF [0]	T_VSHR_OFF [1]	T_VSHR_OFF [0]	-	-	

The command defines as :

Bit	Name	Description									
[5:4]	T_VDS_OFF	code	VDS_OFF								
		00	1 frame (default)								
		01	2 frame								
		10	3 frame								
		11	4 frame								
[3:2]	T_VSHR_OFF	code	VSHR_OFF								
		00	1 frame (default)								
		01	2 frame								
		10	3 frame								
		11	4 frame								

5) Power ON Command (PON)(R04H)

R04H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
PON	W	0	0	0	0	0	0	1	0	0	

The command defines as :

After power on command, driver will power on base on power on sequence.

After power on command, BUSY_N signal will drop from high to low. When finishing the poweron sequence, BUSY_N signal will rise from low to high.

This command only active when BUSY_N = “1” .

6) Power ON Measure Command(PMES)(R05H)

R05H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
PMES	W	0	0	0	0	0	0	1	0	1	

The command defines as :

If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant command with Low Power detection (R51H) and temperature measurement. (R40H).

7) Booster Soft Start Command(BTST)(R06H)

R06H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
PWR	W	0	0	0	0	0	0	1	1	0	
1 st Parameter	W	1	BT_PHA [7]	BT_PHA [6]	BT_PHA [5]	BT_PHA [4]	BT_PHA [3]	BT_PHA [2]	BT_PHA [1]	BT_PHA [0]	
2 nd Parameter	W	1	BT_PHB [7]	BT_PHB [6]	BT_PHB [5]	BT_PHB [4]	BT_PHB [3]	BT_PHB [2]	BT_PHB [1]	BT_PHB [0]	
3 rd Parameter	W	1	-	-	BT_PHC1 [5]	BT_PHC1 [4]	BT_PHC1 [3]	BT_PHC1 [2]	BT_PHC1 [1]	BT_PHC1 [0]	
4 th Parameter	W	1	PHC2EN		BT_PHC2 [5]	BT_PHC2 [4]	BT_PHC2 [3]	BT_PHC2 [2]	BT_PHC2 [1]	BT_PHC2 [0]	
5 th Parameter	W	1	0	0	0	0	FT_PHA [3]	FT_PHA [2]	FT_PHA [1]	FT_PHA [0]	
6 th Parameter	W	1	FT_PHC [3]	FT_PHC [2]	FT_PHC [1]	FT_PHC [0]	FT_PHB [3]	FT_PHB [2]	FT_PHB [1]	FT_PHB [0]	

The command define as follows:

1st Parameter:

Bit	Name	Description
[2:0]	Driving strength of phase A	code description
		000 period 1
		001 period 2
		010 period 3
		011 period 4
		100 period 5
		101 period 6
		110 period 7
[5:3]	Driving strength of phase A	code description
		000 strength 1
		001 strength 2
		010 strength 3 (default)
		011 strength 4
		100 strength 5
		101 strength 6
		110 strength 7
[7:6]	Soft start period of phase A	code description
		00 10ms (default)
		01 20ms
		10 30ms
		11 40ms

2nd Parameter:

Bit	Name	Description
[2:0]	Driving strength of phase B	code description
		000 period 1
		001 period 2
		010 period 3
		011 period 4
		100 period 5
		101 period 6
		110 period 7
[5:3]	Driving strength of phase B	code description
		000 strength 1
		001 strength 2
		010 strength 3 (default)
		011 strength 4
		100 strength 5
		101 strength 6
		110 strength 7
[7:6]	Soft start period of phase B	code description
		00 10ms (default)
		01 20ms
		10 30ms
		11 40ms

3rd Parameter:

Bit	Name	Description	
[2:0]	Minimum OFF time setting of GDR in phase C1	code	description
		000	period 1
		001	period 2
		010	period 3
		011	period 4
		100	period 5
		101	period 6
		110	period 7
		111	period 8 (default)

Bit	Name	Description	
[5:3]	Driving strength of phase C1	code	description
		000	strength 1
		001	strength 2
		010	strength 3 (default)
		011	strength 4
		100	strength 5
		101	strength 6
		110	strength 7
		111	strength 8

4th Parameter:

Bit	Name	Description	
[2:0]	Minimum OFF time setting of GDR in phase C2	code	description
		000	period 1
		001	period 2
		010	period 3
		011	period 4
		100	period 5
		101	period 6
		110	period 7
		111	period 8 (default)

Bit	Name	Description	
[5:3]	Driving strength of phase C2	code	description
		000	strength 1
		001	strength 2
		010	strength 3 (default)
		011	strength 4
		100	strength 5
		101	strength 6
		110	strength 7
		111	strength 8

Bit	Name	Description	
[7]	PHC2EN:	code	description
		0	Booster phase-C2 disable Phase-C1 setting always is applied for booster phase-C.
		1	Booster phase-C2 enable If temperature > temperature boundary phase-C2 , phase-C1 setting is applied for booster phase-C. If temperature <= temperature boundary phase-C2 , phase-C2 setting is applied for booster phase-C. temperature boundary phase-C2(RE7h[7:0])

5th Parameter:

Bit	Name	Description	
[1:0]	Minimum OFF time setting of GDR in phase A	code	description
		00	period sel 4 (default)
		01	period sel 3
		10	period sel 2
		11	period sel 1

Bit	Name	Description	
[3:2]	Driving strength of phase A	code	description
		00	strength sel 4
		01	strength sel 3
		10	strength sel 2 (default)
		11	strength sel 1

6th Parameter:

Bit	Name	Description	
[1:0]	Minimum OFF time setting of GDR in phase B	code	description
		00	period sel 4 (default)
		01	period sel 3
		10	period sel 2
[3:2]	Driving strength of phase B	code	description
		00	strength sel 4
		01	strength sel 3
		10	strength sel 2 (default)
[5:4]	Minimum OFF time setting of GDR in phase C	code	description
		00	period sel 4 (default)
		01	period sel 3
		10	period sel 2
[7:6]	Driving strength of phase C	code	description
		00	strength sel 4
		01	strength sel 3
		10	strength sel 2 (default)
		11	strength sel 1

8) Deep Sleep (DSLP)(R07H)

R07H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
DSLP	W	0	0	0	0	0	0	1	1	1
1 st Parameter	W	1	1	0	1	0	0	1	0	1

The command define as follows:

After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excited if check code = 0xA5.

This command only active when BUSY_N = “1” .

9) Data Start transmission 1 Register(DTM1)(R10H)

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
DTM1	W	0	0		0		1	0	0	0	
1 st Parameter	W	1	KPixel1		KPixel2		KPixel3	KPixel4	KPixel5	KPixel6	
2 nd Parameter	W	1									
...	W	1									
M th Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	

The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes “OLD” data to SRAM.

In B/W/Red mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

10) Display Stop Command(DSP)(R11H)

R11H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
DRF	W	0	0	0	0	1	0	0	0	1
1 st Parameter	R	1	Data_flag	-	-	-	-	-	-	-

The command defines as :

While finished the data transmitting, user must send this command to driver and read Data_flag information.

1st Parameter:

Bit	Name	Description
[7]	-	0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data.

After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.

This command only actives when BUSY_N = "1".

11) Display Refresh Command(DRF)(R12H)

R12H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
DRF	W	0	0	0	0	1	0	0	1	0

The command defines as :

While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0" .

This command only actives when BUSY_N = "1".

12) Data Start transmission 2 Register (DTM2)(R13H)

R13H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
DTM2	W	0	0	0	0	1	0	0	1	1
1 st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8
2 nd Parameter	W	1								
...	W	1								
M th Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)

The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes "NEW" data to SRAM.

In B/W/Red mode, this command writes "RED" data to SRAM.

13) LUT for VCOM (LUTC)(R20H)

R20H	Bit											
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0		
DTM2	W	0	0	0	1	0	0	0	0	0		
1 st Parameter	W	1	Group repeat times[7:0]									
2 nd Parameter	W	1	level selection1-1 [1:0] Frame Number1-1 [5:0]									
3 rd Parameter	W	1	level selection1-2 [1:0] Frame Number1-2 [5:0]									
4 th Parameter	W	1	level selection2-1 [1:0] Frame Number2-1 [5:0]									
5 th Parameter	W	1	level selection2-2 [1:0] Frame Number2-2 [5:0]									
6 th Parameter	W	1	State 1 repeat times[7:0]									
7 th Parameter	W	1	State 2 repeat times[7:0]									
8 th ~14 th Parameter	W	1	2 nd group									
15 th ~21 st Parameter	W	1	3 rd group									
...	W	1	4 th ~7 th group									
50 th ~56 th Parameter	W	1	8 th group									

This command builds up VCOM Look-Up Table (LUT).

This LUT includes 8 kinds of groups; each group is of 7 bytes, as above.

Each Group is divided to 2 states and “Group Repeat Number”. Each state made up 2 phases. And each phase is combined with “Repeat Number”, “Level selection”, and “Frame Number”.

Byte 2: Group repeat times.

Byte 3-6:

[D7:D6]: Level selection of each phase.

[D5:D0]: Frame number of each phase (state1 & state 2)

Bytes 7~8: state repeat times (state1 & state 2)

Bytes 2,9,16,23,30, ...: Group repeat times

0000 0000b: No repeat

0000 0001b~1111 1111b: 1~255 times

Bytes 3~6, 10~13, 17~20, 24~27, 31~ 34 Level Selection.

[D7:D6]: Level Selection.

00b: VCOM_DC

01b: VSH + VCOM_DC

10b: VSL + VCOM_DC

11b: Floating

[D5:D0]: Number of frames (state1 & state 2)

00 0000b~11 1111b: 0~63 times

Bytes 7~8,14~15,21~22,28~29,35~36, ... :repeat times (state1 & state 2)

0000 0000b: No repeat

0000 0001b~1111 1111b: 1~255 frames

If BWR=0(BWR mode), all 8 groups are used.

If BWR=1(BW mode), only 6 groups are used.

14) White to White LUT Register(LUTWW)(R21H)

R21H	Bit											
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0		
DTM2	W	0	0	0	1	0	0	0	0	1		
1 st Parameter	W	1	Group repeat times[7:0]									
2 nd Parameter	W	1	level selection1-1 [1:0] Frame Number1-1 [5:0]									
3 rd Parameter	W	1	level selection1-2 [1:0] Frame Number1-2 [5:0]									
4 th Parameter	W	1	level selection2-1 [1:0] Frame Number2-1 [5:0]									
5 th Parameter	W	1	level selection2-2 [1:0] Frame Number2-2 [5:0]									
6 th Parameter	W	1	State 1 repeat times[7:0]									
7 th Parameter	W	1	State 2 repeat times[7:0]									
8 th ~14 th Parameter	W	1	2 nd group									
15 th ~21 st Parameter	W	1	3 rd group									
...	W	1	4 th ~7 th group									
50 th ~56 th Parameter	W	1	8 th group									

This command builds LUTWW for White-to- White. This LUT includes 6 kinds of groups; each group is of 7 bytes, as above.

Each group is divided to 2 states and “Group Repeat Number”. Each state made up 2 phases. And each phase is combined with “Repeat Number”, “Level selection”, and “Frame Number”.

Byte 2: Group repeat times.

Byte 3-6:

[D7:D6]: Level selection of each phase.

[D5:D0]: Frame number of each phase (state1 & state 2)

Bytes 7~8: state repeat times (state1 & state 2)

Bytes 2,9,16,23,30, ...: Group repeat times

0000 0000b: No repeat

0000 0001b~1111 1111b: 1~255 times

Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection.

[D7:D6]: Level Selection.

00b: GND

01b: VSH

10b: VSL

11b: VSHR

[D5:D0]: Number of frames (state1 & state 2)

00 0000b~11 1111b: 0~63 times

Bytes 7~8,14~15,21~22,28~29,35~36, ... :repeat times (state1 & state 2)

0000 0000b: No repeat

0000 0001b~1111 1111b: 1~255 frames

If BWR=0(BWR mode), LUTWW is not used.

If BWR=1(BW mode), LUTWW is used.

15) Black to White LUT or Red LUT Register(LUTBW/LUTR) (R22H)

R22H	Bit											
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0		
DTM2	W	0	0	0	1	0	0	0	1	0		
1 st Parameter	W	1	Group repeat times[7:0]									
2 nd Parameter	W	1	level selection1-1 [1:0] Frame Number1-1 [5:0]									
3 rd Parameter	W	1	level selection1-2 [1:0] Frame Number1-2 [5:0]									
4 th Parameter	W	1	level selection2-1 [1:0] Frame Number2-1 [5:0]									
5 th Parameter	W	1	level selection2-2 [1:0] Frame Number2-2 [5:0]									
6 th Parameter	W	1	State 1 repeat times[7:0]									
7 th Parameter	W	1	State 2 repeat times[7:0]									
8 th ~14 th Parameter	W	1	2 nd group									
15 th ~21 st Parameter	W	1	3 rd group									
...	W	1	4 th ~7 th group									
50 th ~56 th Parameter	W	1	8 th group									

This command builds Look-up Table for LUTWB/LUTW. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above.

Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number".

Byte 2: Group repeat times.

Byte 3-6:

[D7:D6]: Level selection of each phase.

[D5:D0]: Frame number of each phase (state1 & state 2)

Bytes 7~8: state repeat times (state1 & state 2)

Bytes 2,9,16,23,30, ...: Group repeat times

0000 0000b: No repeat

0000 0001b~1111 1111b: 1~255 times

Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection.

[D7:D6]: Level Selection.

00b: GND

01b: VSH

10b: VSL

11b: VSHR

[D5:D0]: Number of frames (state1 & state 2)

00 0000b~11 1111b: 0~63 times

Bytes 7~8,14~15,21~22,28~29,35~36, ... :repeat times (state1 & state 2)

0000 0000b: No repeat

0000 0001b~1111 1111b: 1~255 frames

If BWR=0(BWR mode), all 8 groups are used.

If BWR=1(BW mode), only 6 groups are used.

16) White to Black LUT or White LUT Register (LUTWB/LUTW)(R23H)

R23H	Bit											
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0		
DTM2	W	0	0	0	1	0	0	0	1	1		
1 st Parameter	W	1	Group repeat times[7:0]									
2 nd Parameter	W	1	level selection1-1 [1:0] Frame Number1-1 [5:0]									
3 rd Parameter	W	1	level selection1-2 [1:0] Frame Number1-2 [5:0]									
4 th Parameter	W	1	level selection2-1 [1:0] Frame Number2-1 [5:0]									
5 th Parameter	W	1	level selection2-2 [1:0] Frame Number2-2 [5:0]									
6 th Parameter	W	1	State 1 repeat times[7:0]									
7 th Parameter	W	1	State 2 repeat times[7:0]									
8 th ~14 th Parameter	W	1	2 nd group									
15 th ~21 st Parameter	W	1	3 rd group									
...	W	1	4 th ~7 th group									
50 th ~56 th Parameter	W	1	8 th group									

-This command builds Look-up Table for LUTWB/LUTW. This LUT includes 8 kinds of groups; each groups of 7 bytes, as above.

Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number".

Byte 2:Group repeat times.

Byte 3-6:

[D7:D6]: Level selection of each phase.

[D5:D0]: Frame number of each phase (state1 & state 2)

Bytes 7~8: state repeat times (state1 & state 2)

Bytes 2,9,16,23,30,...: Group repeat times

0000 0000b: No repeat

0000 0001b~1111 1111b: 1~255 times

Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection.

[D7:D6]: Level Selection.

00b: GND

01b: VSH

10b: VSL

11b: VSHR

[D5:D0]: Number of frames (state1 & state 2)

00 0000b~11 1111b: 0~63 times

Bytes 7~8,14~15,21~22,28~29,35~36,...: :repeat times (state1 & state 2)

0000 0000b: No repeat

0000 0001b~1111 1111b: 1~255 frames

If BWR=0(BWR mode),all 8 groups are used.

If BWR=1(BW mode),only 6 groups are used.

17) Black to Black LUT or Black LUT Register(LUTBB/LUTB)(R24H)

R23H		Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0		
DTM2	W	0	0	0	1	0	0	1	0	0		
1 st Parameter	W	1	Group repeat times[7:0]									
2 nd Parameter	W	1	level selection1-1 [1:0] Frame Number1-1 [5:0]									
3 rd Parameter	W	1	level selection1-2 [1:0] Frame Number1-2 [5:0]									
4 th Parameter	W	1	level selection2-1 [1:0] Frame Number2-1 [5:0]									
5 th Parameter	W	1	level selection2-2 [1:0] Frame Number2-2 [5:0]									
6 th Parameter	W	1	State 1 repeat times[7:0]									
7 th Parameter	W	1	State 2 repeat times[7:0]									
8 th ~14 th Parameter	W	1	2 nd group									
15 th ~21 st Parameter	W	1	3 rd group									
...	W	1	4 th ~7 th group									
50 th ~56 th Parameter	W	1	8 th group									

-This command builds Look-up Table for LUTBB/LUTB. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above.

Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number".

Byte 2: Group repeat times.

Byte 3-6:

[D7:D6]: Level selection of each phase.

[D5:D0]: Frame number of each phase (state1 & state 2)

Bytes 7~8: state repeat times (state1 & state 2)

Bytes 2,9,16,23,30,...: Group repeat times

0000 0000b: No repeat

0000 0001b~1111 1111b: 1~255 times

Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection.

[D7:D6]: Level Selection.

00b: GND

01b: VSH

10b: VSL

11b: VSHR

[D5:D0]: Number of frames (state1 & state 2)

00 0000b~11 1111b: 0~63 times

Bytes 7~8,14~15,21~22,28~29,35~36,...: repeat times (state1 & state 2)

0000 0000b: No repeat

0000 0001b~1111 1111b: 1~255 frames

If BWR=0(BWR mode), all 8 groups are used.

If BWR=1(BW mode), only 6 groups are used.

18) Set LUT States (SET_GROUP)(R26H)

R26H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
LUTC option	W	0	0	0	1	0	0	1	1	0
1 st Parameter	W	1	-	-	-	-	-	-	-	group_sel[1:0]

This command is used to set LUT states

Function of group_sel [1:0] are shown below

B/W/Red mode(BWR=0)

Value	Group
00	8 (default)
01	7
10	6
11	5

B/W mode (BWR=1)

Value	Group
00	6 (default)
01	5
10	4
11	3

19) LUT Option Register (LUTOPT) (R2AH)

R2AH	Bit											
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0		
SET_STG	W	0	0	0	1	0	1	0	1	0		
1 st Parameter	W	1	EOPT	-	-	-	-	-	-	-		
2 nd Parameter	W	1	STATE_XON[7:0]									
3 rd Parameter	W	1	STATE_XON[15:8]									

- This command sets XON and ending options of source output

STATE_XON[15:0]:

All Gate ON (Each bit controls one sub-state, STATE_XON [0] for state-1, STATE_XON [1] for state-2)

0000 0000 0000 0000b: no All-Gate-ON

0000 0000 0000 0001b: State1 All-Gate-ON

0000 0000 0000 0011b: State1 and State2 All-Gate-ON

...

EOPT:

Option for LUT ending

1st Parameter:

Bit	Name	Description
[7]	EOPT	0: Normal.(Default) 1: Source output level keep previous output before power off

20) PLL Control Register (PLL)(R30H)

R30H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
OSC	W	0	0	0	1	1	0	0	0	0	
1 st Parameter	W	1	-	-	M[2:0]			N[2:0]			

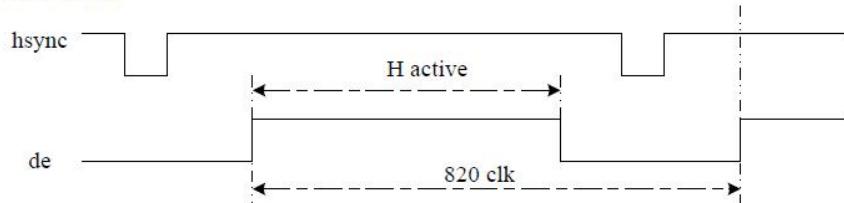
The command defines as:

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

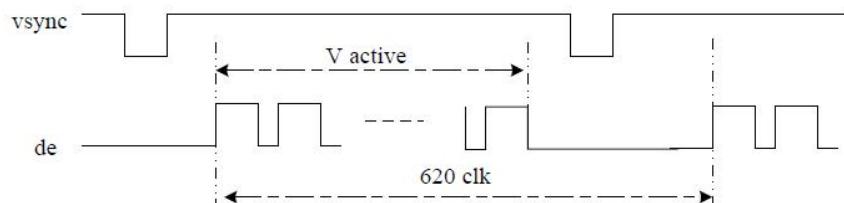
M	N	Frame rate									
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ (default)
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

remark:

-Horizontal



-Vertical



21) PLL mode selection (R40H)

R31H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
OSC	W	0	0	0	1	1	0	0	0	0	
1 st Parameter	W	1	-	-	-	-	-	-	-	PLL option	

The command defines as:

The command controls the R30H (PLL)& R32H (group frame rate) selection.

If PLL option sets to 0, R32H (group frame rate) was decided.

If PLL option sets to 1, R30H (PLL) was decided.

22) Set LUT each group frame rate (GROUP Frame rate)(R32H)

R32H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
SET_GROUP	W	0	0	0	1	1	0	0	1	0	
1 st Parameter	W	1	-	-	Group1 M[2:0]			Group1 N[2:0]			
2 nd Parameter	W	1			Group2 M[2:0]			Group2 N[2:0]			
3 rd Parameter	W	1			Group3 M[2:0]			Group3 N[2:0]			
4 th Parameter	W	1			Group4 M[2:0]			Group4 N[2:0]			
5 th Parameter	W	1			Group5 M[2:0]			Group5 N[2:0]			
6 th Parameter	W	1			Group6 M[2:0]			Group6 N[2:0]			
7 th Parameter	W	1			Group7 M[2:0]			Group7 N[2:0]			
8 th Parameter	W	1			Group8 M[2:0]			Group8 N[2:0]			

This command is used to set LUT states

The command controls the LUT frequency. The PLL structure must support the following frame rates:

M	N	Frame rate									
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

23) Temperature Sensor Command (TSC)(R40H)

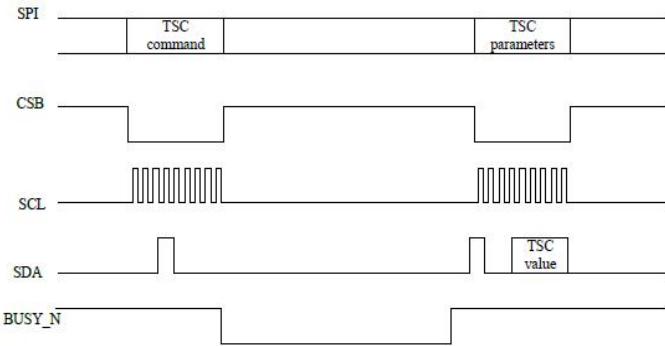
R40H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
TSC	W	0	0	1	0	0	0	0	0	0
1 st Parameter	R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]
2 nd Parameter	R	1	D2/TS[1]	D1/ TS[0]	D0	-	-	-	-	-

The command define as follows:

This command indicates the temperature value.

If R41H (TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H (TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[1:0]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

This command only actives when BUSY_N = "1".

24) Temperature Sensor Calibration Register (TSE)(R41H)

R41H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
TSE	W	0	0	1	0	0	0	0	1	0
1st Parameter	W	1	TSE	-	TO[5]	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]

The command defines as:

This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration

1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Description																																			
[3:0]	<p>Temperature level:</p> <table border="1"> <thead> <tr> <th>code</th> <th>Temp.</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>+0°C (default)</td> </tr> <tr> <td>0001</td> <td>+1°C</td> </tr> <tr> <td>0010</td> <td>+2°C</td> </tr> <tr> <td>0011</td> <td>+3°C</td> </tr> <tr> <td>0100</td> <td>+4°C</td> </tr> <tr> <td>0101</td> <td>+5°C</td> </tr> <tr> <td>0110</td> <td>+6°C</td> </tr> <tr> <td>0111</td> <td>+7°C</td> </tr> <tr> <td>1000</td> <td>-8°C</td> </tr> <tr> <td>1001</td> <td>-7°C</td> </tr> <tr> <td>1010</td> <td>-6°C</td> </tr> <tr> <td>1011</td> <td>-5°C</td> </tr> <tr> <td>1100</td> <td>-4°C</td> </tr> <tr> <td>1101</td> <td>-3°C</td> </tr> <tr> <td>1110</td> <td>-2°C</td> </tr> <tr> <td>1111</td> <td>-1°C</td> </tr> </tbody> </table>		code	Temp.	0000	+0°C (default)	0001	+1°C	0010	+2°C	0011	+3°C	0100	+4°C	0101	+5°C	0110	+6°C	0111	+7°C	1000	-8°C	1001	-7°C	1010	-6°C	1011	-5°C	1100	-4°C	1101	-3°C	1110	-2°C	1111	-1°C
code	Temp.																																			
0000	+0°C (default)																																			
0001	+1°C																																			
0010	+2°C																																			
0011	+3°C																																			
0100	+4°C																																			
0101	+5°C																																			
0110	+6°C																																			
0111	+7°C																																			
1000	-8°C																																			
1001	-7°C																																			
1010	-6°C																																			
1011	-5°C																																			
1100	-4°C																																			
1101	-3°C																																			
1110	-2°C																																			
1111	-1°C																																			
[5:4]	<table border="1"> <thead> <tr> <th>code</th> <th>Temp.</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>+0.00°C (default)</td> </tr> <tr> <td>01</td> <td>+0.25°C</td> </tr> <tr> <td>10</td> <td>+0.5°C</td> </tr> <tr> <td>11</td> <td>+0.75°C</td> </tr> </tbody> </table>		code	Temp.	00	+0.00°C (default)	01	+0.25°C	10	+0.5°C	11	+0.75°C																								
code	Temp.																																			
00	+0.00°C (default)																																			
01	+0.25°C																																			
10	+0.5°C																																			
11	+0.75°C																																			
[7]	<p>Internal temperature sensor enable</p> <p>0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.</p>																																			

25) Temperature Sensor Write Register (TSW)(R42H)

R42H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
TSW	W	0	0	1	0	0	0	0	1	0	
1 st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[5]	WATTR[1]	WATTR[0]	
2 nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	
3 rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	

The command defines as:

This command writes the temperature.

1st Parameter

Bit	temperature
[2:0]	Pointer setting
[5:3]	User-defined address bits (A2, A1, A0)
[7:6]	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter

Bit	temperature
[7:0]	MSByte of write-data to external temperature sensor

3rd Parameter

Bit	temperature
[7:0]	LSByte of write-data to external temperature sensor

This command only actives after R04H(PON) or R05H(PMES)

26) Temperature Sensor Read Register (TSR)(R43H)

R43H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
TSC	W	0	0	1	0	0	0	0	1	1	
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	

The command defines as:

This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	temperature
[7:0]	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	temperature
[7:0]	LSByte of write-data from external temperature sensor

SPI



CSB



SCL



SDA



BUSY_N



This command only actives after R04H(PON) or R05H(PMES)

27) VCOM and DATA interval setting Register (CDI)(R50H)

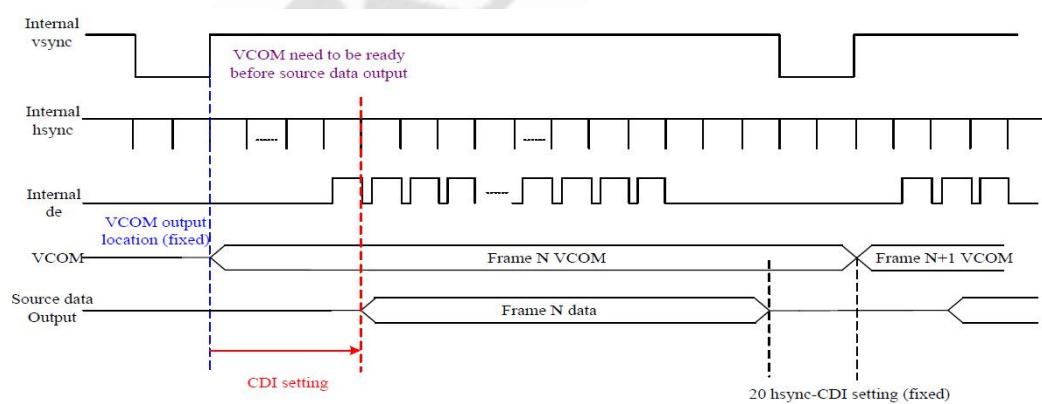
R50H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
CDI	W	0	0	1	0	1	0	0	0	0
1 st Parameter	W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]

The command defines as:

1st Parameter:

CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

Bit	Description	
[3:0]	code	Vcom and data interval
	0000	17 hsync
	0001	16 hsync
	0010	15 hsync
	0011	14 hsync
	0100	13 hsync
	0101	12 hsync
	0110	11 hsync
	0111	10 hsync
	1000	9 hsync
	1001	8 hsync
	1010	7 hsync
	1011	6 hsync
	1100	5 hsync
	1101	4 hsync
	1110	3 hsync
	1111	2 hsync



VBD[1:0]: Border data selection.

B/W/Red mode (BWR=0)

Bit 4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
	00	LUTB
	01	LUTW
	10	LUTR
11 (default)		Floating

B/W mode (BWR=1)

Bit 4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
	00	Floating
	01	LUTBW (1->0)
	10	LUTWB (0->1)
	11	Floating
	00	Floating
	01	LUTWB (0->1)
	10	LUTBW (1->0)
11 (default)		Floating

Border output voltage level: The level selection is based on mapping LUT data.

Level Selection:

code	Border output voltage
00	Vcom
01	VSH
10	VSL
11	VSHR

DDX[1:0]: Data polarity

- 1.DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
- 2.DDX[0] for B/W mode

B/W/Red mode (BWR=0)

DDX[1] is for RED data

DDX[0] is for B/W data

Bit 5-4	Description	
DDX[1:0]	Data (Red/B/W)	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)

DDX[1]=0 is for BW mode with NEW/OLD

Bit 5-4	Description	
DDX[1:0]	Data (Red/B/W)	LUT
00	00	LUTWW (0->0)
	01	LUTBW(1->0)
	10	LUTWB(0->1)
	11	LUTBB(1->1)
01 (default)	00	LUTBB(0->0)
	01	LUTWB(1->0)
	10	LUTBW(0->1)
	11	LUTWW(1->1)

DDX[1]=1 is for BW mode without NEW/OLD

Bit 5-4	Description	
DDX[1:0]	Data (B/W)	LUT
10	0	LUTBW(1->0)
	1	LUTWB(0->1)
11	0	LUTWB(1->0)
	1	LUTBW(0->1)

28) Lower Power Detection Register (LPD)(R51H)

R51H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
LPD	W	0	0	1	0	1	0	0	0	1	
1 st Parameter	R	1	-	-	-	-	-	-	-	LPD	
2 nd Parameter	R	1	GHD	SHD	SLD	SHRD	-	-	-	-	

The command defines as:

This command indicates the input power condition. Host can read this data to understand the battery's condition.

When LPD="1", system input power is normal.

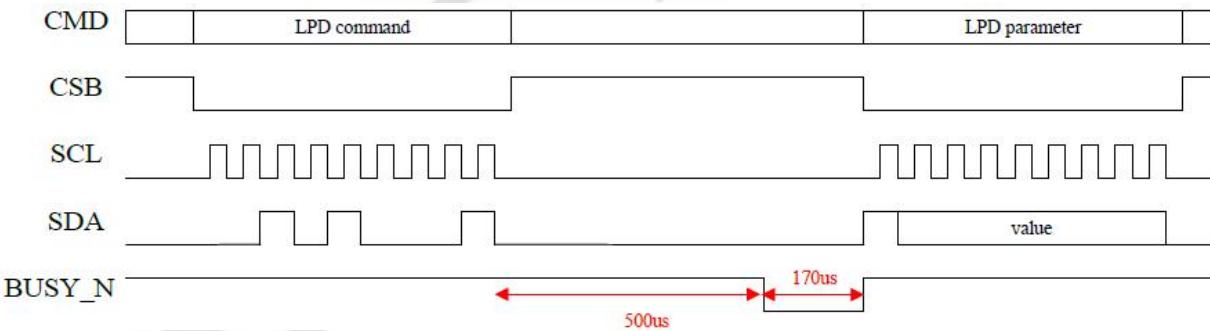
When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)).

1st Parameter:

Bit	Name	Description
[0]	LPD	0: Low power input 1: Normal status

2nd Parameter:

Bit	Name	Description
[4]	SHRD	0: Low power input 1: Normal status
[5]	SLD	0: Detect voltage < 95%VSL 1: Normal status
[6]	SHD	0: Detect voltage < 95%VSH 1: Normal status
[7]	GHD	0: Detect voltage < 95%VGH 1: Normal status



This command only actives when BUSY_N = "1".

This command only actives after R04H(PON) /R05H(PMES)

29) TCON setting (TCON)(R60H)

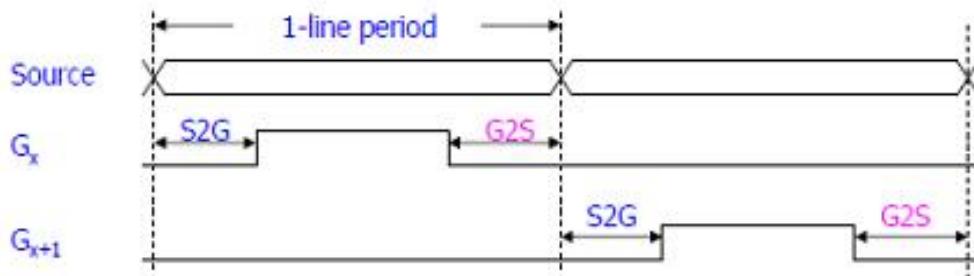
R60H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
TCON	W	0	0	1	1	0	0	0	0	0	
1 st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	

The command define Non-overlap period of gate and source as below:

1st Parameter:

Bit	Period	
	code	Period
S2G[3:0]/G2S[3:0]	0000	2 clock
	0001	4 clock
	0010	6 clock (default)
	0011	8 clock
	0100	10 clock
	0101	12 clock
	0110	14 clock
	0111	16 clock
	1000	18 clock
	1001	20 clock
	1010	22 clock
	1011	24 clock
	1100	26 clock
	1101	28 clock
	1110	30 clock
	1111	32 clock

Period=660ns



30) Resolution setting (TRES)(R61H)

R61H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
TRES	W	0	0	1	1	0	0	0	0	1	
1 st Parameter	W	1							HRES(9)	HRES(8)	
2 nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	
3 rd Parameter	W	1							VRES(9)	VRES(8)	
4 th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	

The command define as follows:

When using register:

Horizontal display resolution = HRES

Vertical display resolution = VRES

Channel disable calculation:

GD : First G active = G0; LAST active GD= first active +VRES[9:0] -1

SD : First active channel: =S0 ; LAST active SD= first active +HRES[9:3]*8-1

EX :128X272

GD: First G active = G0

LAST active GD= 0+272-1= 271; (G271)

SD : First active channel: =S0

LAST active SD=0+16*8-1=127; (S127)

31) Source & gate start setting (TSGS)(R62H)

R62H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
TSGS	W	0	0	1	1	0	0	0	1	0	
1 st Parameter	W	1							S_Start (9)	S_Start (8)	
2 nd Parameter	W	1	S_Start (7)	S_Start (6)	S_Start (5)	S_Start (4)	S_Start (3)	-	-	-	
3 rd Parameter	W	1				gscan			G_Start (9)	G_Start (8)	
4 th Parameter	W	1	G_Start (7)	G_Start (6)	G_Start (5)	G_Start (4)	G_Start (3)	G_Start (2)	G_Start (1)	G_Start (0)	

The command define as follows:

1.S_Start [9:3] describe which source output line is the first date line

2.G_Start[9:0] describe which gate line is the first scan line

3. gscan :Gate scan select

Code	Type
0	Normal scan
1	Cascade type 2 scan

S_Start should be the multiple of 8

32) REVISION register (REV) (R70H)

R70H		Bit										
Inst/Para	R/ W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0		
CAL_CHKSUM	W	0	0	1	1	1	0	0	0	0		
1st Parameter	R	1	User reserved byte0									
2 nd Parameter	R	1	User reserved byte1									
3 rd ~15 th Parameter			User reserved byte2~14									
16 th Parameter	R	1	User reserved byte15									

The command defines as:

The REV is read from:

OTP Bank0 address = 0xBB5~0xBC4

OTP Bank1 address = 0x17B5 ~0x17C4

33) Status register (FLG) (R71H)

R71H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
FLG	W	0	0	1	1	1	0	0	0	1	
1 st Parameter	W	1	Con_fb	PTL_flag	I ² C_ERR	I ² C_BUSYN	Data_flag	PON	POF	BUSY_N	

The command defines as:

This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Function
[7]	Connector status feedback (high: connection failed), use DEBUG[5] & DEBUG[7]
[6]	Partial display status (high: partial mode)
[5]	I2C master error status
[4]	I2C master busy status (low active)
[3]	Driver has already received one frame data
[2]	PON 0: Not in PON mode 1: In PON mode
[1]	POF 0: Not in POF mode(default) 1: In POF mode
[0]	Driver busy status(low active)

User can send this command in any time. It doesn't have restriction of BUSY_N.

The DEBUG[5] & DEBUG[7] is connector detect pin

34) Auto Measure VCOM register (AMV) (R80H)

Bit										
R80H	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
AMV	W	0	1	0	0	0	0	0	0	0

The command defines as:

This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Function											
[0]	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable											
[1]	AMV: Analog signal 0: Get Vcom value from R81h(default) 1: Get Vcom value in analog signal											
[2]	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSHR during Auto Measure VCOM period.											
[3]	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.											
[5:4]	The sensing time of VCOM detection <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>code</th> <th>sensing time</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>3s</td> </tr> <tr style="background-color: yellow;"> <td>01</td> <td>5s (default)</td> </tr> <tr> <td>10</td> <td>8s</td> </tr> <tr> <td>11</td> <td>10s</td> </tr> </tbody> </table>		code	sensing time	00	3s	01	5s (default)	10	8s	11	10s
code	sensing time											
00	3s											
01	5s (default)											
10	8s											
11	10s											

This command only actives when BUSY_N = "1".

35) Vcom Value register (VV) (R81H)

Bit										
R81H	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
VV	W	0	1	0	0	0	0	0	0	1
1 st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]

The command defines as:

This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

VCOM value

VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)
0000000	00h	-0.1	0011011	1Bh	-1.45	0110110	36h	-2.8
0000001	01h	-0.15	0011100	1Ch	-1.5	0110111	37h	-2.85
0000010	02h	-0.2	0011101	1Dh	-1.55	0111000	38h	-2.9
0000011	03h	-0.25	0011110	1Eh	-1.6	0111001	39h	-2.95
0000100	04h	-0.3	0011111	1Fh	-1.65	0111010	3Ah	-3
0000101	05h	-0.35	0100000	20h	-1.7	0111011	3Bh	-3.05
0000110	06h	-0.4	0100001	21h	-1.75	0111100	3Ch	-3.1
0000111	07h	-0.45	0100010	22h	-1.8	0111101	3Dh	-3.15
0001000	08h	-0.5	0100011	23h	-1.85	0111110	3Eh	-3.2
0001001	09h	-0.55	0100100	24h	-1.9	0111111	3Fh	-3.25
0001010	0Ah	-0.6	0100101	25h	-1.95	1000000	40h	-3.3
0001011	0Bh	-0.65	0100110	26h	-2	1000001	41h	-3.35
0001100	0Ch	-0.7	0100111	27h	-2.05	1000010	42h	-3.4
0001101	0Dh	-0.75	0101000	28h	-2.1	1000011	43h	-3.45
0001110	0Eh	-0.8	0101001	29h	-2.15	1000100	44h	-3.5
0001111	0Fh	-0.85	0101010	2Ah	-2.2	1000101	45h	-3.55
0010000	10h	-0.9	0101011	2Bh	-2.25	1000110	46h	-3.6
0010001	11h	-0.95	0101100	2Ch	-2.3	1000111	47h	-3.65
0010010	12h	-1	0101101	2Dh	-2.35	1001000	48h	-3.7
0010011	13h	-1.05	0101110	2Eh	-2.4	1001001	49h	-3.75
0010100	14h	-1.1	0101111	2Fh	-2.45	1001010	4Ah	-3.8
0010101	15h	-1.15	0110000	30h	-2.5	1001011	4Bh	-3.85
0010110	16h	-1.2	0110001	31h	-2.55	1001100	4Ch	-3.9
0010111	17h	-1.25	0110010	32h	-2.6	1001101	4Dh	-3.95
0011000	18h	-1.3	0110011	33h	-2.65	1001110	4Eh	-4
0011001	19h	-1.35	0110100	34h	-2.7	1001111	4Fh	-4.05
0011010	1Ah	-1.4	0110101	35h	-2.75			

36) Vcom_DC setting register (VDCS) (R82H)

R82H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
VDSC	W	0	1	0	0	0	0	0	1	0	
1 st Parameter	W	1	-	VDCS [6]	VDCS [5]	VDCS[4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	

The command defines as:

This command set the VCOM DC value. Driver will base on this value for VCM_DC.

1st Parameter:

VCOM value

VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)
0000000	00h	-0.1	0011011	1Bh	-1.45	0110110	36h	-2.8
0000001	01h	-0.15	0011100	1Ch	-1.5	0110111	37h	-2.85
0000010	02h	-0.2	0011101	1Dh	-1.55	0111000	38h	-2.9
0000011	03h	-0.25	0011110	1Eh	-1.6	0111001	39h	-2.95
0000100	04h	-0.3	0011111	1Fh	-1.65	0111010	3Ah	-3
0000101	05h	-0.35	0100000	20h	-1.7	0111011	3Bh	-3.05
0000110	06h	-0.4	0100001	21h	-1.75	0111100	3Ch	-3.1
0000111	07h	-0.45	0100010	22h	-1.8	0111101	3Dh	-3.15
0001000	08h	-0.5	0100011	23h	-1.85	0111110	3Eh	-3.2
0001001	09h	-0.55	0100100	24h	-1.9	0111111	3Fh	-3.25
0001010	0Ah	-0.6	0100101	25h	-1.95	1000000	40h	-3.3
0001011	0Bh	-0.65	0100110	26h	-2	1000001	41h	-3.35
0001100	0Ch	-0.7	0100111	27h	-2.05	1000010	42h	-3.4
0001101	0Dh	-0.75	0101000	28h	-2.1	1000011	43h	-3.45
0001110	0Eh	-0.8	0101001	29h	-2.15	1000100	44h	-3.5
0001111	0Fh	-0.85	0101010	2Ah	-2.2	1000101	45h	-3.55
0010000	10h	-0.9	0101011	2Bh	-2.25	1000110	46h	-3.6
0010001	11h	-0.95	0101100	2Ch	-2.3	1000111	47h	-3.65
0010010	12h	-1	0101101	2Dh	-2.35	1001000	48h	-3.7
0010011	13h	-1.05	0101110	2Eh	-2.4	1001001	49h	-3.75
0010100	14h	-1.1	0101111	2Fh	-2.45	1001010	4Ah	-3.8
0010101	15h	-1.15	0110000	30h	-2.5	1001011	4Bh	-3.85
0010110	16h	-1.2	0110001	31h	-2.55	1001100	4Ch	-3.9
0010111	17h	-1.25	0110010	32h	-2.6	1001101	4Dh	-3.95
0011000	18h	-1.3	0110011	33h	-2.65	1001110	4Eh	-4
0011001	19h	-1.35	0110100	34h	-2.7	1001111	4Fh	-4.05
0011010	1Ah	-1.4	0110101	35h	-2.75			

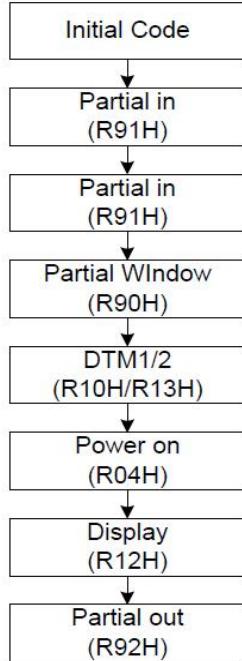
37) Partial Window Register (PTL) (R90H)

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
PTL	W	0	1	0	0	1	0	0	0	0	
1 st Parameter	W	1							HRST[9]	HRST[8]	
2 nd Parameter	W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	0	0	0	
3 rd Parameter	W	1							HRED[9]	HRED[8]	
4 th Parameter	W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	1	1	1	
5 th Parameter	W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	
6 th Parameter	W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	
7 th Parameter	W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	
8 th Parameter	W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	
9 th Parameter	W	1	-	-	-	-	-	-	-	PT_SCAN	

This command sets partial window.

Name	Description
HRST[9:3]	Horizontal start channel bank. (value 00h~99h)
HRED[9:3]	Horizontal end channel bank. (value 00h~99h). HRED must be greater than HRST.
VRST[9:0]	Vertical start line. (value 000h~257h)
VRED[9:0]	Vertical end line. (value 000h~257h). VRED must be greater than VRST.
PT_SCAN	0: Gates scan only inside of the partial window. 1: Gates scan both inside and outside of the partial window.

Partial display flow:



38) Partial In Register (PTIN) (R91H)

R91H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
PTIN	W	0	1	0	0	1	0	0	0	1	

The command define as follows:

This command makes the display enter partial mode.

39) Partial Out Register (PTOUT) (R92H)

R92H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
PTOUT	W	0	1	0	0	1	0	0	1	0	

The command define as follows:

This command makes the display exit partial mode and enter normal mode.

40) Program Mode (PGM) (RA0H)

RA0H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
APG	W	0	1	0	1	0	0	0	0	0	

The command define as follows:

After this command is issued, the chip would enter the program mode.

The mode would return to standby by hardware reset.

41) Active Program (APG) (RA1H)

RA1H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
APG	W	0	1	0	1	0	0	0	0	1	

The command define as follows:

After this command is transmitted, the programming state machine would be activated.

The BUSY flag would change state from 0 to 1 while the programming is completed.

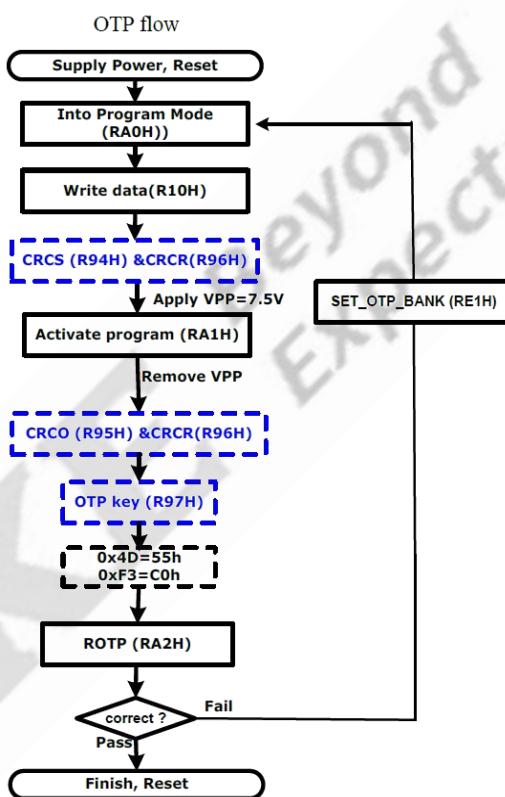
42) Read OTP Data (ROTP) (RA2H)

RA2H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
PTL	W	0	1	0	1	0	0	0	1	0
1 st Parameter	R	1	Dummy							
2 nd Parameter	R	1	The data of address 0x000 in the OTP							
3 rd Parameter	R	1	The data of address 0x001 in the OTP							
4 th Parameter	R	1	:							
5 th Parameter	R	1	The data of address (n-1) in the OTP							
6 th ~(m-1) th Parameter	R	1							
m th Parameter	R	1	The data of address (n) in the OTP							

The command define as follows:

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0FFF.



The sequence of programming OTP

43) Force Temperature (TSSET) (RE5H)

RE5H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
TSSET	W	0	1	1	1	0	0	1	0	1
1 st Parameter	W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[1]

The command define as follows:

This command is used to fix the temperature value of master and slave chip in cascade.

44) Temperature Boundary Phase-C2 (TS_PHC2) (RE7H)

RE7H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
TSSET	W	0	1	1	1	0	0	1	1	1
1 st Parameter	W	1	TS_PHC2 [7]	TS_PHC2 [6]	TS_PHC2 [5]	TS_PHC2 [4]	TS_PHC2 [3]	TS_PHC2 [2]	TS_PHC2 [1]	TS_PHC2 [0]

The command define as follows:

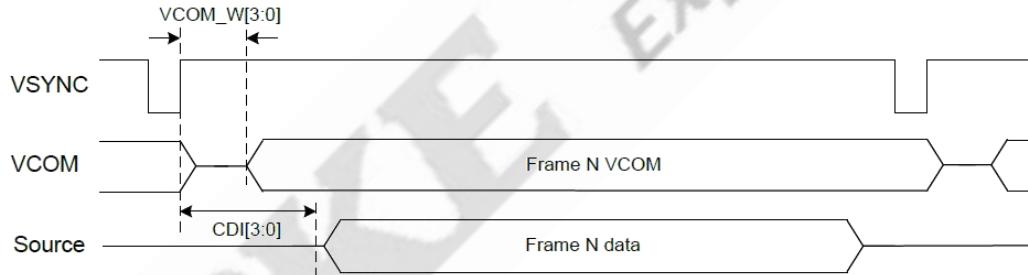
This command is used to set the temperature boundary to judge whether booster phase-C2 is applied or not.

45) Power Saving (PWS) (RE8H)

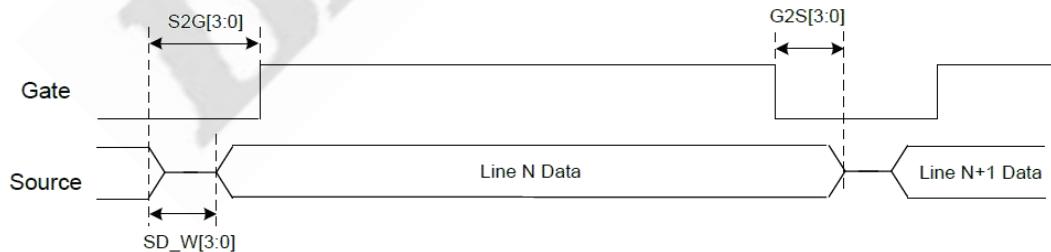
RE8H	Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
TSSET	W	0	1	1	1	0	1	0	0	0
1 st Parameter	W	1								

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

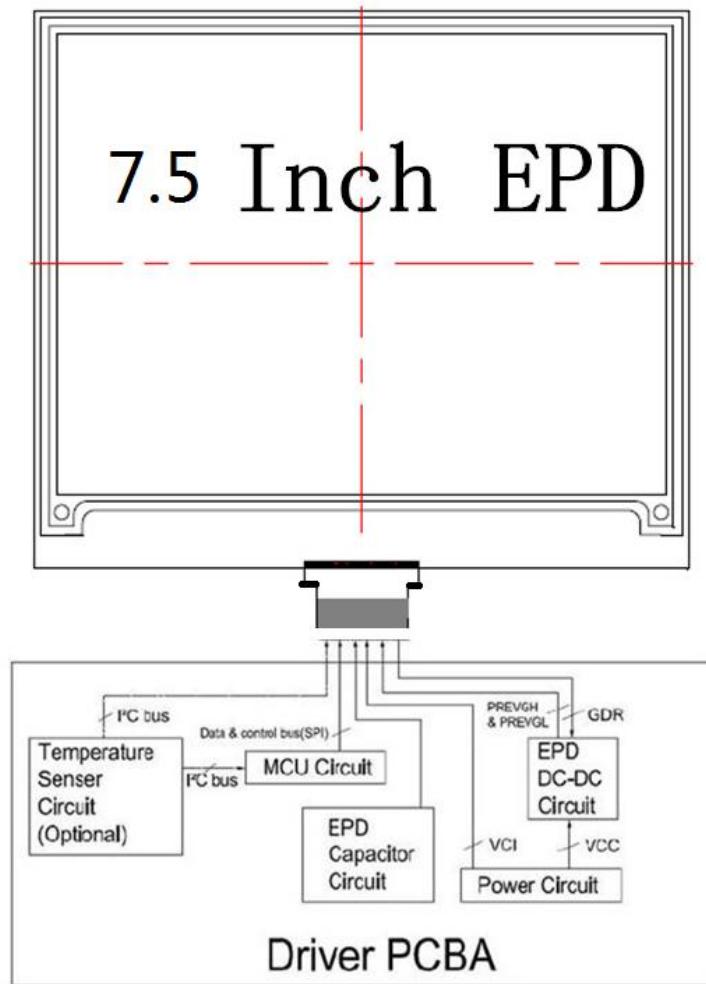
VCOM_W: VCOM power saving width (unit = line period)



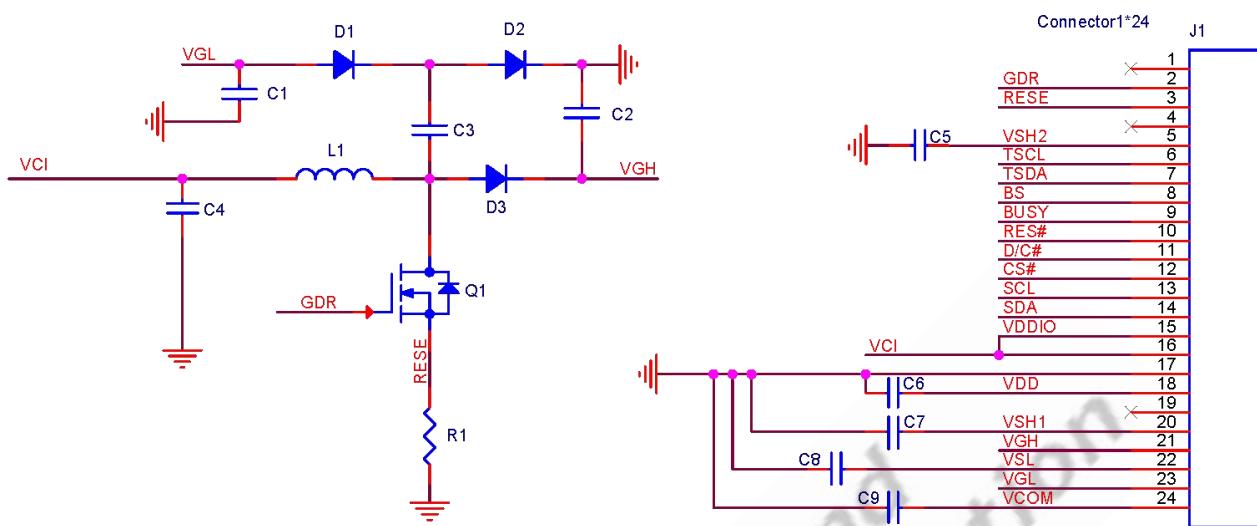
SD_W: Source power saving width (unit = 660nS)



8 Block Diagram



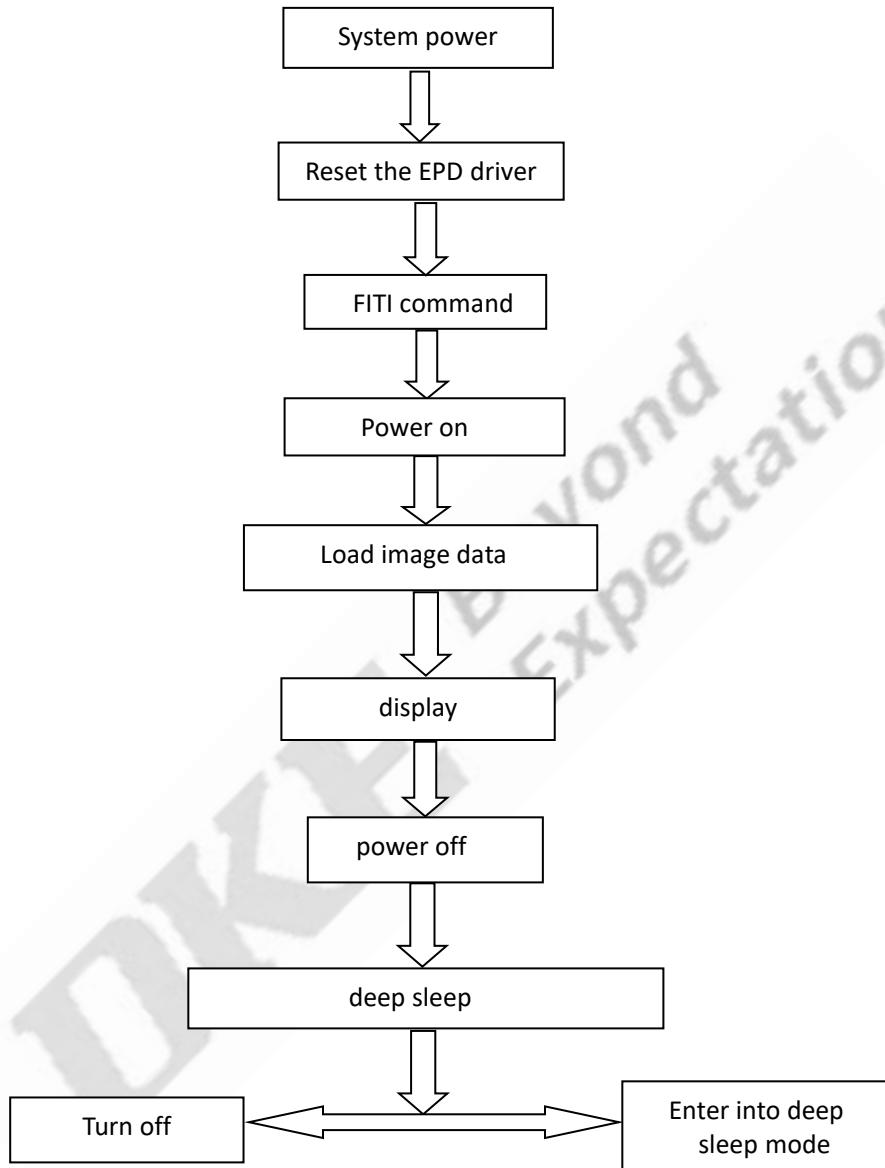
9.Typical Application Circuit with SPI Interface



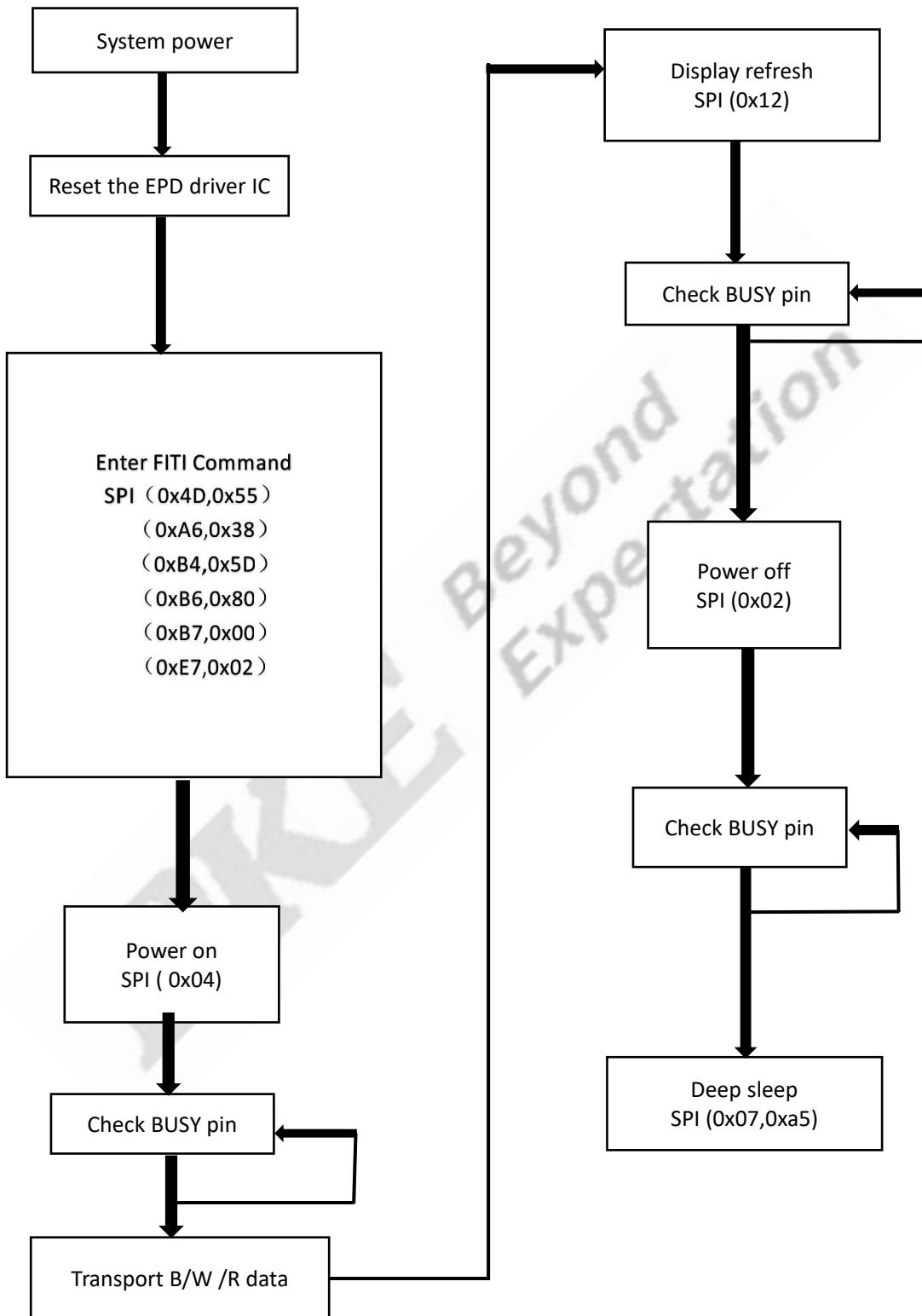
Part Name	Value	Requirements for spare part
C1 C2	4.7uF	0805, X5R/X7R, Voltage Rating:50V
C4 C5 C6 C7 C8	1uF	0603, X5R/X7R, Voltage Rating:25V
C3 C9	1uF	0603, X5R/X7R, Voltage Rating:50V
R1	2.2Ohm	0603; 1% variation
D1 D2 D3	Diode	MBR0530 1. Reverse DC voltage \geq 30V 2. Forward current \geq 500mA
Q1	NMOS	Si1308EDL, Si1304BDL 1. Drain-source break voltage \geq 30V 2. Gate-source threshold voltage \leq 1.5V
L1	47UH	NR4018T470M, CDRH2D18 / LDNP-470NC 1. Maximum DC current~420mA 2. Maximum DC resistance~650m Ω

10 Typical Operating Sequence

10.1 LUT from OTP Operation Flow



10.2 LUT from OTP Operation Reference Program Code



11. Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60°C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T=40°C, RH=35%, 240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=40°C, RH=80%, 240h
6	High Temperature, High Humidity Storage	T=50°C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern
8	ESD Gun	Air+/-8KV;Contact+/-6KV (Naked EPD display,no including IC and FPC area) Air+/-4KV;Contact+/-2KV Contact+/-2KV(HBM C:100pF;R:1.5k ohm) Contact+/-200V(MM C:200pF;R:0 ohm) (Naked EPD display,including IC and FPC area)

Note:

1. Stay white pattern for storage and non-operation test.
2. Operation is black→white-red pattern, the interval is 150s.
3. Put in 20°C--25°C for 1hour after test finished, The function ,appearance and display performance is OK.

12.Quality Assurance

12.1 Environment

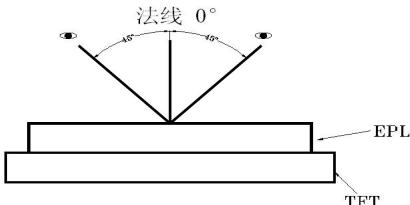
Temperature: $23 \pm 3^{\circ}\text{C}$

Humidity: $55 \pm 10\%\text{RH}$

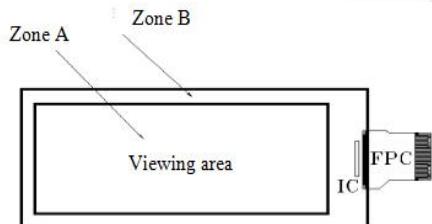
12.2 Illuminance

Brightness: $1200 \sim 1500\text{LUX}$; distance: $20\text{-}30\text{CM}$; Angle: Relate 45° surround.

12.3 Inspect method

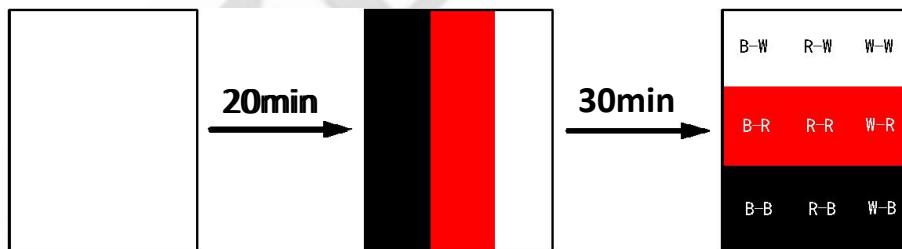


12.4 Display area



12.5 Ghosting test method

Three-color ghosting is measured with following transition from horizontal 3 scale pattern to vertical 3 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by DKE.



1) Measurement Instruments: X-rite i1Pro

2) Ghosting formula:

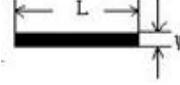
W ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(W-W, R-W), \Delta E_{ab}(W-W, B-W), \Delta E_{ab}(B-W, R-W))$

K ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(B-B, W-B), \Delta E_{ab}(B-B, R-B), \Delta E_{ab}(R-B, W-B))$

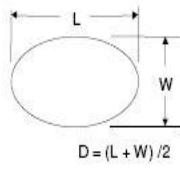
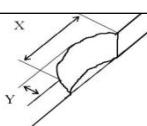
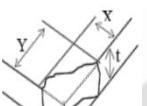
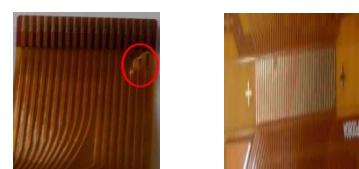
R ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(R-R, W-R), \Delta E_{ab}(R-R, B-R), \Delta E_{ab}(B-R, W-R))$

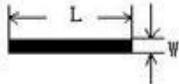
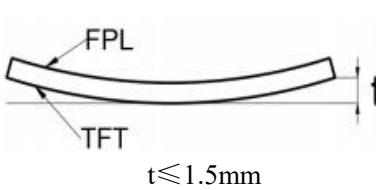
12.6 Inspection standard

12.6.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA		
2	Black/White spots	 $D \leq 0.3\text{mm}$, negligible $0.3\text{mm} < D \leq 0.5\text{mm}$, $N \leq 5$, Allowed $0.5\text{mm} < D$ Not Allow		Visual inspection	
3	Black/White lines (No switch)	 $L \leq 1.0\text{mm}, W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm}, W > 0.5\text{mm}$ is not allowed	MI	Visual/ Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 <p> $D \leq 0.3\text{mm}$, Allowed $0.3\text{mm} < D \leq 0.5\text{mm}$, $N \leq 5$ $D > 0.5\text{mm}$, Not Allow </p>	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A
3	\Dirty	Allowed if can be removed	MI		Zone B
4	Chips/Scratch/ Edge crown	 <p> $X \leq 3\text{mm}$, $Y \leq 0.5\text{mm}$ And without affecting the electrode is permissible $2\text{mm} \leq X$ or $2\text{mm} \leq Y$ Not Allow  $W \leq 0.1\text{mm}$, $L \leq 5\text{mm}$, No harm to the electrodes and $N \leq 2$ allow </p>	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 <p>Not Allow</p>	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	 <p>Not Allow</p>	MA	Visual / Microscope	Zone B

8	B/W Line	 <p> $L \leq 1.0\text{mm}$, $W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm}$, $W > 0.5\text{mm}$ is not allowed </p>	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	<p>TFT edge bulge: $X \leq 3\text{mm}$, $Y \leq 0.3\text{mm}$ Allowed</p> <p>TFT chromatic aberration :Allowed</p>	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	<p>$D \leq 0.25\text{mm}$, allow</p> <p>$0.25\text{mm} < D \leq 0.4\text{mm}$, $n \leq 4$ allow</p> <p>$D > 0.4\text{mm}$ is not allowed</p> <p>($n \leq 8$ items are allowed within 5 mm in diameter)</p>	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	<p>PCB (Circuit area) damaged Not Allow</p> <p>PCB Poor welding Not Allow</p> <p>PCB Curl $\leq 1\%$</p>	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	<p>Edge Adhesives $H \leq PS$ surface (Including protect film) Edge adhesives seep in $\leq 1/2$ Margin width</p> <p>Length excluding Edge adhesives bubble: bubble Width $\leq 1/2$ Margin width; Length $\leq 5.0\text{mm}$. $n \leq 5$</p>	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	Visual Inspection
14	Silicon glue	<p>Thickness $\leq PS$ surface(With protect film): Full cover the IC; Shape:</p> <p>The width on the FPC $\leq 0.5\text{mm}$ (Front) The width on the FPC $\leq 1.0\text{mm}$ (Back)</p> <p>smooth surface, No obvious raised.</p>	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 <p>$t \leq 1.5\text{mm}$</p>	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

13 Packaging

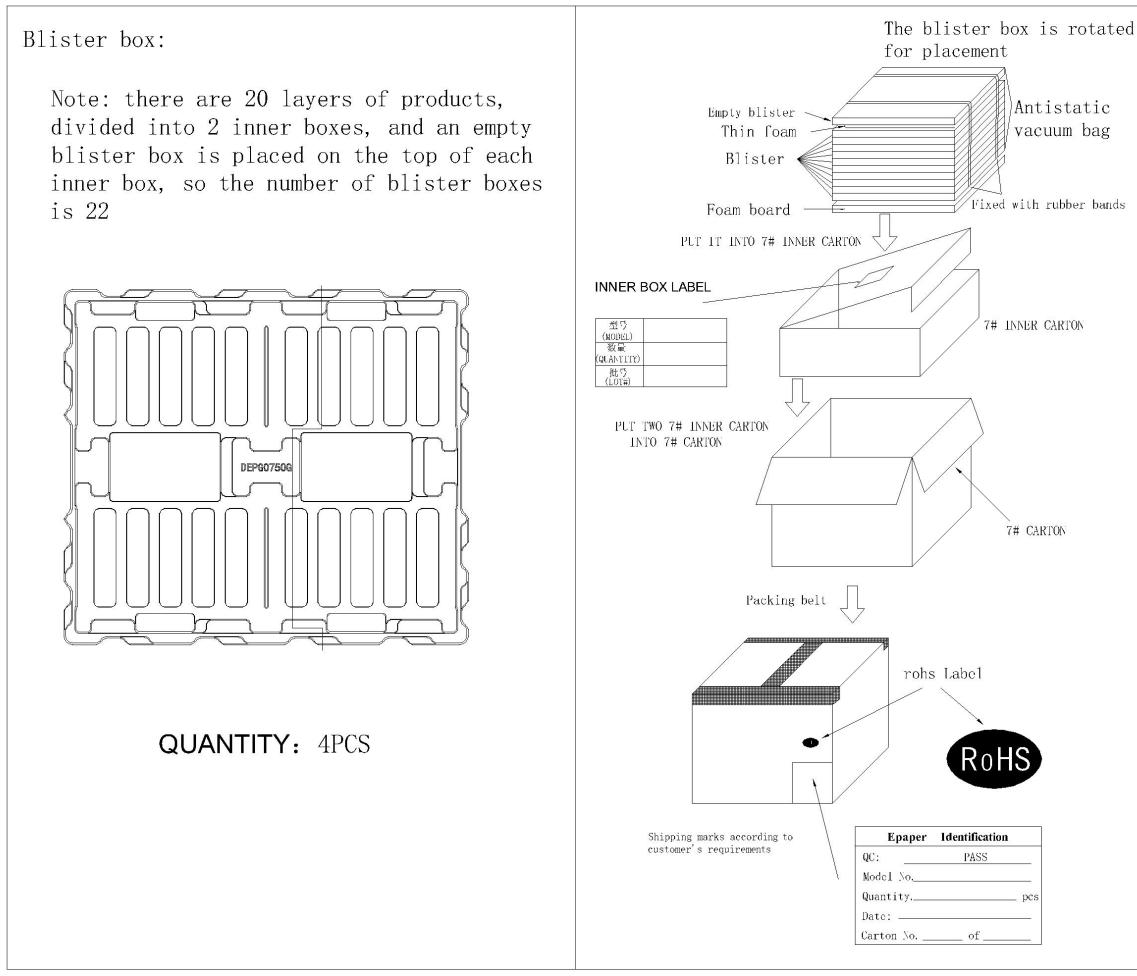
DKE 东方科脉

PACKING INSTRUCTION

P/N	Customer Code	Ref. P/N	Type	PKG Method	Marking	Surface Marks	Pull Tape
DEPG0750			GLASS	Blister	BACK	None	YES

Packing Materials List					4PCS/LAYER, 20LAYER/CTN, TOTAL 80PCS/CTN.
List	Model	Materials	Q'ty	Unit	Pull tape:
Carton	7# 417*362*229 mm	corrugate	1	Piece	
Inner Carton	7#(INNER) 400*343 *95 mm	corrugate	2	Piece	
Blister	DEPG0750G	PET	22	Piece	
Thin foam	341.76*273.8*1.5-1.8mm	EPE	20	Piece	
Antistatic vacuum bag	450*590*0.075		2	Piece	
Foam board	DKE2251-10	EPE	3	Piece	
PULL TAPE	16*5*T0.05		80	Piece	

Detail:



14. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
Product Environmental certification	
ROHS	
REMARK	
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.	
Transport environment	
When the humidity of transportation environment is between 45%RH~70%RH, the product can be stored for 30 days, and the product can be stored for 10 days if it is lower or higher than this range	