LUMOSTUDY

Functional Verification Using System Verilog

Description:
Lumostudy offers training program for students currently doing their B.E/B.Tech, M.E/M.Tech in Electronics/ Instrumentation/Electrical/ Telecommunication. This program is specifically designed to introduce participants to functional verification using SystemVerilog HVL. The participants will get an opportunity to work on a project during the course.

All participants will be awarded a certificate upon successful completion of the program and all the assignments. Seats will be allotted on first -come-first-serve basis. There will also be assignments & online test submission on a weekly basis.

Duration:

- 6-8 weeks(30-40 hours)-(Daily 1 hour)

Pre-requisites:

- Basic of Digital
- Basic Understanding of Verilog

Eligibility Criteria:

- Anyone interested to learn.

Tools/Software

- Online EDA tools.

Key takeaways:

- Participants will be able to write a complete SystemVerilog environment form scratch with all the components including generator, driver, monitor, coverage and scoreboard.
- Create a complete SV environment of a Memory Model from scratch.

Key topics covered:

- Basics of Verilog
- Verilog stratified event queue
- Verilog Simulation Semantics
- SystemVerilog for Design
- Loop, Functions and Tasks in SV
- SV Procedural Blocks
- SV Interfaces
- SV Program Blocks
- SV Event Regions
- SV clocking Blocks and packages
- OOPS concepts
- SV Randomization
- SV IPC threads (Inter Process communication)
- Functional Coverage
- SV complete enviroment

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Key topics covered:

- Detailed list will be release soon.

Registation Link: https://forms.gle/uDdgG7LjEf4TDw2d8