LUMOSTUDY

Digital Design and Verification using Verilog HDL Part 2

Description:
Lumostudy offers 1 month training program for students currently doing their B.E/B.Tech, M.E/M.Tech in Electronics/ Instrumentation/Electrical/ Telecommunication. This program is specifically designed with an objective to spark an interest in core electronics. The participants will get an opportunity to work on a project during the course.

All participants will be awarded a certificate upon successful completion of the program and all the assignments. Seats will be allotted on first -come-first-serve basis. There will also be assignments & online test submission on a weekly basis.

Duration:

- 3 weeks(15 hours)-(Daily 1 hour)

Pre-requisites:

- Basic of Digital
- Basic Understanding of Verilog

Key takeaways:

- Advance Digital Design concepts
- Verilog HDL concepts
- Analyze and use the improvements to tasks and functions
- Self-checking Test Bench Writing
- EDA tools Overview (ModelSim for Mentor)
- **Project:** Design and Verification of Synchronous FIFO

Eligibility Criteria:

- Anyone interested to learn.

Tools/Software

- ModelSim PE student edition

Key topics covered:
Week 1: (5 hrs, 1 hr/Day)

- Introduction to FSM- Melay and Moore FSM-FSM coding guidelines.
- Verilog coding styles for Modeling Melay and Moore—FSM Verification with an efficient testbench.
- Odd-Even example.

Week 2: (5 hrs, 1 hr/Day)

- Introduction to ASM Charts and why it is used.
- Using ASM charts to model a Lift problem and the benefits of using it instead of using FSM.

Week 3: (5 hrs, 1 hr/Day)

- Modeling Memory and writing simple test bench.
- Introduction to FIFO, Design and Verification from scratch.

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Registation Link: https://forms.gle/uDdgG7LjEf4TDw2d8