LUMOSTUDY

Digital Design and Verification using Verilog HDL Part 1

Description:
Lumostudy offers 1 month training program for students currently doing their B.E/B.Tech, M.E/M.Tech in Electronics/ Instrumentation/Electrical/ Telecommunication. This program is specifically designed with an objective to spark an interest in core electronics. The participants will get an opportunity to work on a project during the course.

Seats will be allotted on first -come-first-serve basis.

Duration:

- 3 weeks (15 Hours) –(Daily 1 hour)

Key takeaways:

- Basics of Digital Design
- Hardware Modeling Overview
- Verilog HDL concepts
- Test Bench Writing
- EDA tools Overview (ModelSim for Mentor)

Eligibility Criteria:

- Anyone interested to learn.

Tools/Software

- ModelSim PE student edition

Key topics covered:

Week 1:

- Basic Digital concepts-Basic gates, Half-adder, Full-adder, Mux.
- Introduction to Verilog, Verilog Modeling Styles, Modeling combinational circuits using Structural modeling- Half-adder, full-adder, Ripple carry adder and mux.
- Introduction to ModelSim tool.
- Performing simulation for Verilog Design.

Week 2:

- Introduction to Data flow style, Modeling Mux and adder.
- Introduction to Test bench, Test bench components, TB for adder and mux.
- Introduction to Behavioral modeling, Blocking Assignment statements.
- Introduction to Nonblocking assignment statements, Modeling FFs and latches, Testbenchs for FF and Latches.

Week 3:

- Difference between blocking and Nonblocking assignments statements.
- Modeling counters and shift registers.
- Introduction to self-checking test bench.

Registation Link: https://forms.gle/uDdgG7LjEf4TDw2d8